Promethean Toolkit

Enabling Best Practices
in IC Design & Test

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imec

Promethean Toolkit

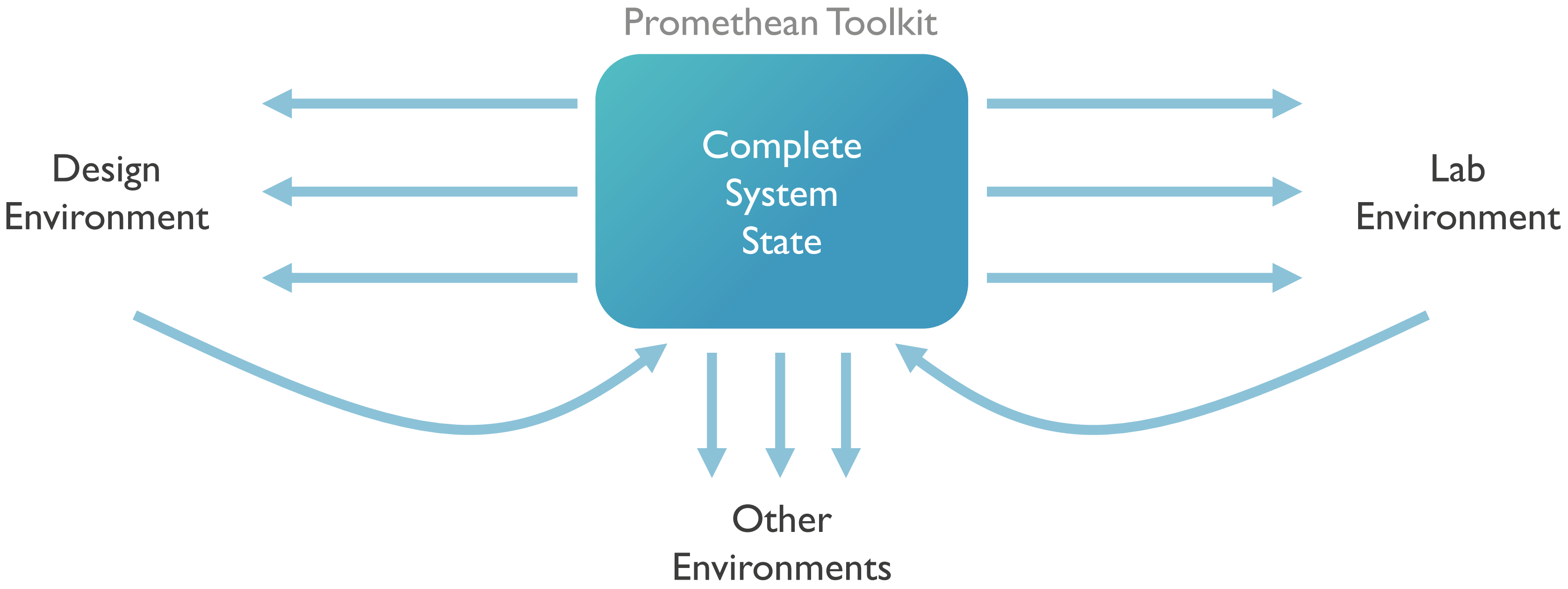
Centralized Design and Test

- Full-fledged application written in Matlab
  - 3 years of development
  - Already in use by ADC team

- Can be used throughout the design process
  - Design in Cadence (or other CAD tools)
  - Measurement in Lab

Centralized Data Source

Everything feeds from a single, central source



Promethean Toolkit

Complete System State

Design Environment

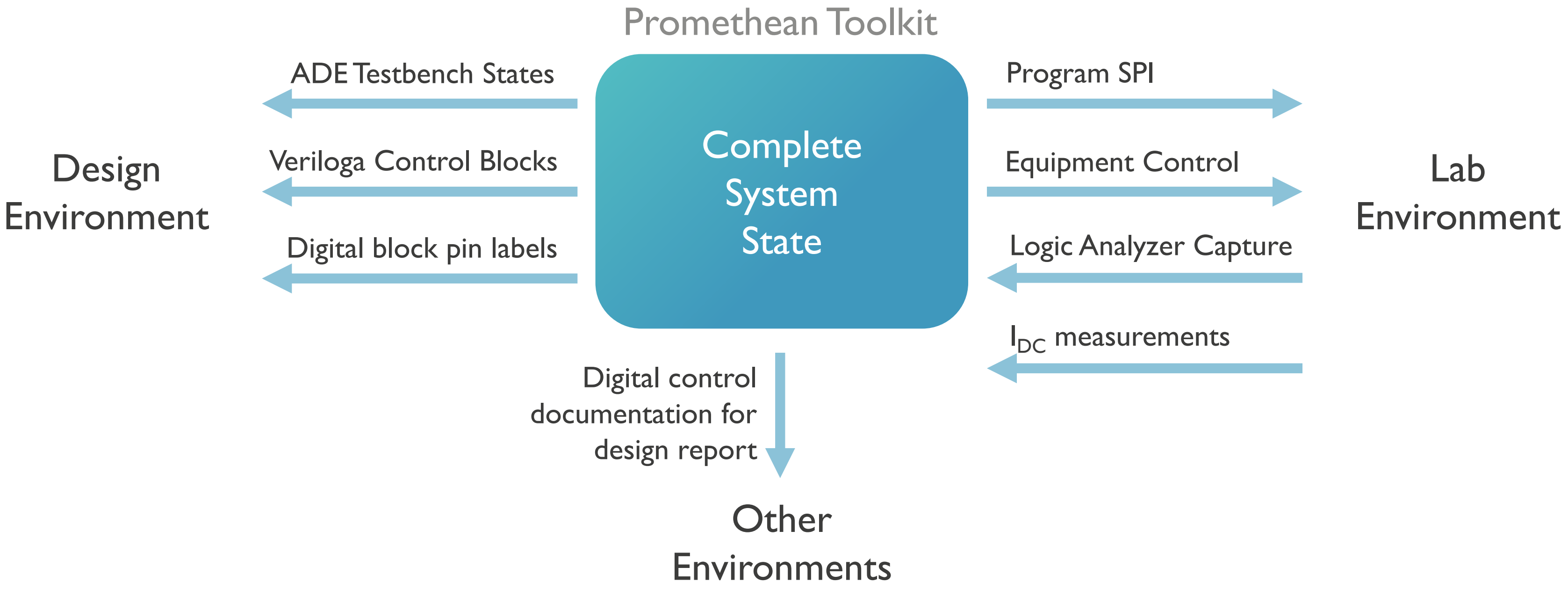
Lab Environment

Other Environments

Centralized Data Source

Everything feeds from a single, central source

Real Example: ringamp ADC



Promethean Toolkit

Complete System State

Design Environment

ADE Testbench States

Veriloga Control Blocks

Digital block pin labels

Lab Environment

Program SPI

Equipment Control

Logic Analyzer Capture

I_{DC} measurements

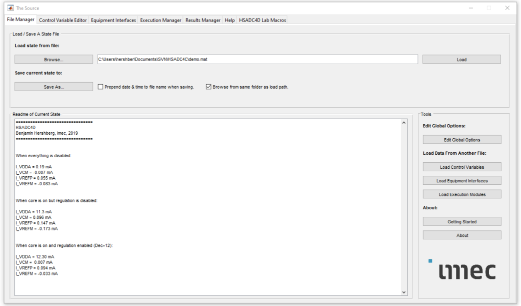
Other Environments

Digital control documentation for design report

The Common Modules

Top-level System Architecture

File Manager:



Load / Save A State File

Load state from file: C:\Users\hershber\Documents\SVN\HSADC4C\demo.mat

Save current state to:

☐ Prepend date & time to file name when saving. ☑ Browse from same folder as load path.

Readme of Current State

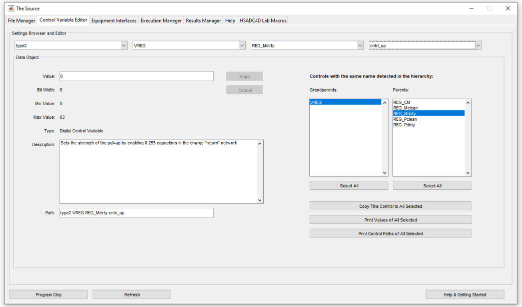
```
================================
HSADC4D
Benjamin Hershberg, imec, 2019
================================


When everything is disabled:

I_VDDA = 0.19 mA
I_VCM = -0.007 mA
I_VREFP = 0.055 mA
I_VREFM = -0.083 mA


When core is on but regulation is disabled:

I_VDDA = 11.3 mA
I_VCM = 0.096 mA
I_VREFP = 0.147 mA
I_VREFM = -0.173 mA


When core is on and regulation enabled (Dec=12):

I_VDDA = 12.30 mA
I_VCM =  0.007 mA
I_VREFP = 0.094 mA
I_VREFM = -0.033 mA
```

Edit Global Options:

Load Data From Another File:

About:

Control Variable Editor:



Settings Browser and Editor: type2 | VREG | REG_Mdirty | cntrl_up

Data Object

Value: 0

Bit Width: 6

Min Value: 0

Max Value: 63

Type: Digital Control Variable

Description: Sets the strength of the pull-up by enabling 0:255 capacitors in the charge "return" network

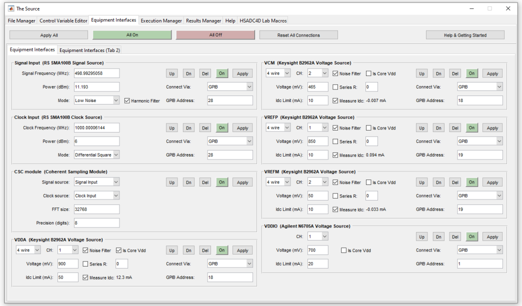
Path: type2.VREG.REG_Mdirty.cntrl_up

Controls with the same name detected in the hierarchy:

Grandparents:
VREG

Parents:
REG_CM
REG_Mclean
REG_Mdirty
REG_Pclean
REG_Pdirty

Equipment Interfaces:



Signal Input (RS SMA100B Signal Source)
Signal Frequency (MHz): 498.99295058
Power (dBm): 11.193
Mode: Low Noise ☑ Harmonic Filter
Connect Via: GPIB
GPIB Address: 28

Clock Input (RS SMA100B Clock Source)
Clock Frequency (MHz): 1000.00006144
Power (dBm): 6
Mode: Differential Square
Connect Via: GPIB
GPIB Address: 28

CSC module (Coherent Sampling Module)
Signal source: Signal Input
Clock source: Clock Input
FFT size: 32768
Precision (digits): 8

VDDA (Keysight B2962A Voltage Source)
4 wire CH: 1 ☑ Noise Filter ☑ Is Core Vdd
Voltage (mV): 900 ☐ Series R: 0
Idc Limit (mA): 50 ☑ Measure Idc: 12.3 mA
Connect Via: GPIB
GPIB Address: 18

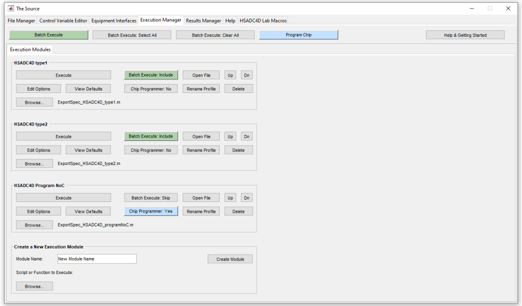
VCM (Keysight B2962A Voltage Source)
4 wire CH: 2 ☑ Noise Filter ☐ Is Core Vdd
Voltage (mV): 465 ☐ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: -0.007 mA
Connect Via: GPIB
GPIB Address: 18

VREFP (Keysight B2962A Voltage Source)
4 wire CH: 1 ☑ Noise Filter ☐ Is Core Vdd
Voltage (mV): 850 ☐ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: 0.094 mA
Connect Via: GPIB
GPIB Address: 19

VREFM (Keysight B2962A Voltage Source)
4 wire CH: 2 ☑ Noise Filter ☐ Is Core Vdd
Voltage (mV): 50 ☐ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: -0.033 mA
Connect Via: GPIB
GPIB Address: 19

VDDIO (Agilent N6705A Voltage Source)
CH: 1
Voltage (mV): 700 ☐ Is Core Vdd
Idc Limit (mA): 20
Connect Via: GPIB
GPIB Address: 1

Execution Manager:



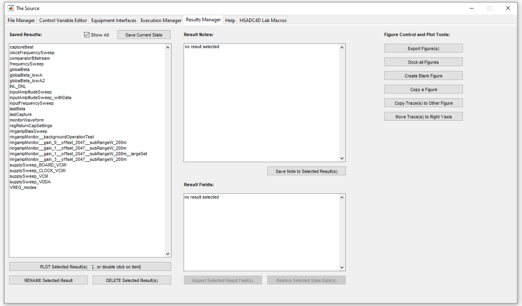
HSADC4D type1
Batch Execute: Include
Chip Programmer: No
ExportSpec_HSADC4D_type1.m

HSADC4D type2
Batch Execute: Include
Chip Programmer: No
ExportSpec_HSADC4D_type2.m

HSADC4D Program NoC
Batch Execute: Skip
Chip Programmer: Yes
ExportSpec_HSADC4D_programNoC.m

Create a New Execution Module
Module Name: New Module Name
Script or Function to Execute:

Results Manager:


The Source
File Manager
Control Variable Editor
Equipment Interfaces
Execution Manager
Results Manager
Help
HSADC4D Lab Macros
Save Current State
Save Note to Selected Result(s)
PLOT Selected Result(s) [...or double click on item]
RENAME Selected Result
DELETE Selected Result(s)
Inspect Selected Result Field(s)
Restore Selected State Data(s)
Export Figure(s)
Dock all Figures
Create Blank Figure
Copy a Figure
Copy Trace(s) to Other Figure
Move Trace(s) to Right Yaxis

Saved Results: ☑ Show All

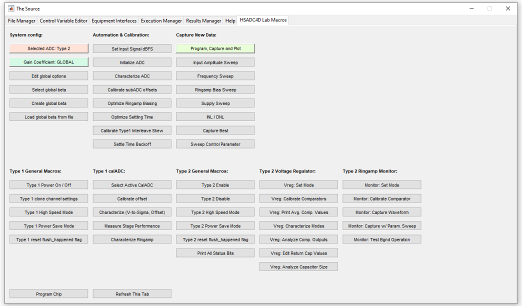
captureBest
clockFrequencySweep
comparatorBitstream
frequencySweep
globalBeta
globalBeta_lowA
globalBeta_lowA2
INL_DNL
inputAmplitudeSweep
inputAmplitudeSweep_withData
inputFrequencySweep
lastBeta
lastCapture
monitorWaveform
regReturnCapSettings
ringampBiasSweep
ringampMonitor__backgroundOperationTest
ringampMonitor__gain_0__offset_2047__subRangeW_200m
ringampMonitor__gain_1__offset_2047__subRangeW_200m
ringampMonitor__gain_1__offset_2047__subRangeW_200m__largeSet
ringampMonitor__gain_3__offset_2047__subRangeW_200m
supplySweep_BOARD_VCMI
supplySweep_CLOCK_VCMI
supplySweep_VCM
supplySweep_VDDA
VREG_modes

Result Notes:
no result selected

Result Fields:
no result selected

Figure Control and Plot Tools:

Custom (User) Defined:

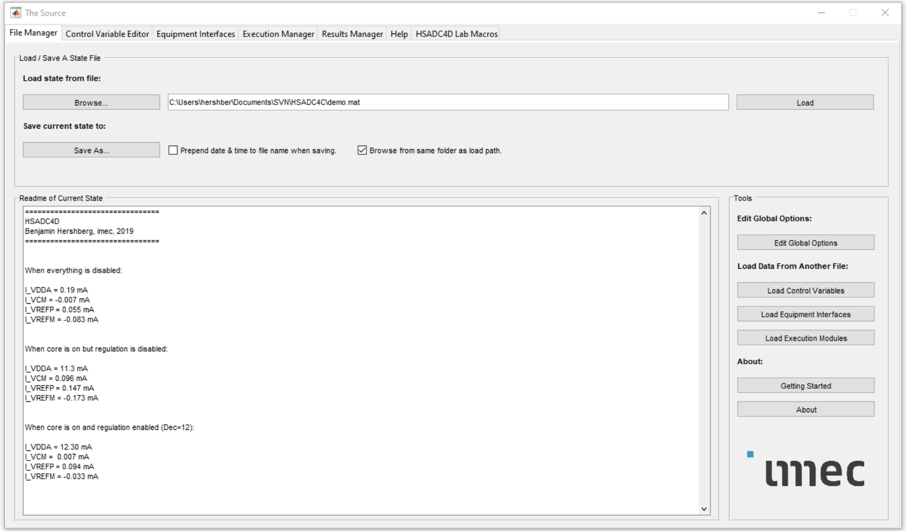


File Manager

Tour of the Common Modules

- Main Purpose
  - Load / Save states

- Features
  - "Readme" scratchpad for annotations
  - Load specific pieces of another file's state
  - Configure the "global options"



C:\Users\hershber\Documents\SVN\HSADC4C\demo.mat

☐ Prepend date & time to file name when saving.

☑ Browse from same folder as load path.

```
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HSADC4D
Benjamin Hershberg, imec, 2019
================================


When everything is disabled:

I_VDDA = 0.19 mA
I_VCM = -0.007 mA
I_VREFP = 0.055 mA
I_VREFM = -0.083 mA


When core is on but regulation is disabled:

I_VDDA = 11.3 mA
I_VCM = 0.096 mA
I_VREFP = 0.147 mA
I_VREFM = -0.173 mA


When core is on and regulation enabled (Dec=12):

I_VDDA = 12.30 mA
I_VCM =  0.007 mA
I_VREFP = 0.094 mA
I_VREFM = -0.033 mA
```
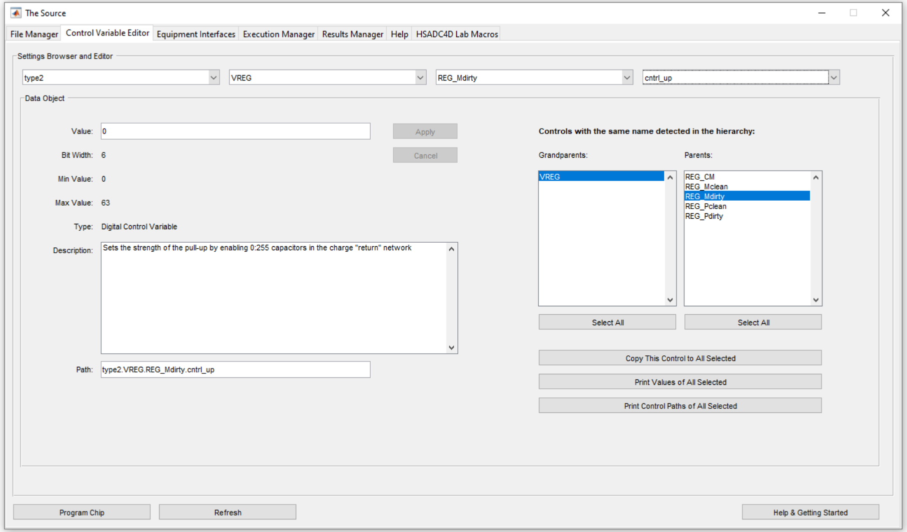

Control Variable Editor

Tour of the Common Modules

- Main Purpose
  - Browse / Edit the control variable tree

- Features
  - Built-in documentation for variables
  - Detects patterns in the control hierarchy and allows for batch analysis & edit
  - Supports both “hard” digital variables and “soft” cadence variables
  - Define control variables with a simple pre-defined hierarchical struct / cell format.
  - Hierarchy organization does not need to match physical system



Settings Browser and Editor

type2 | VREG | REG_Mdirty | cntrl_up

Data Object

Value: 0

Bit Width: 6

Min Value: 0

Max Value: 63

Type: Digital Control Variable

Description: Sets the strength of the pull-up by enabling 0:255 capacitors in the charge "return" network

Path: type2.VREG.REG_Mdirty.cntrl_up

Controls with the same name detected in the hierarchy:

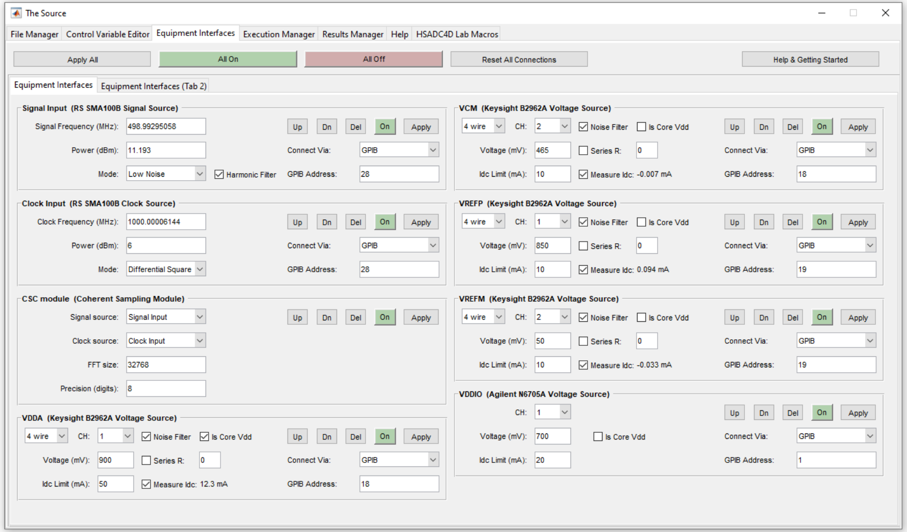
Grandparents:
VREG

Parents:
REG_CM
REG_Mclean
REG_Mdirty
REG_Pclean
REG_Pdirty

Equipment Control

Tour of the Common Modules

- Main Purpose
  - Control lab equipment
- Features
  - Interactive and fully reconfigurable
  - Any connection protocol (GPIB, LAN, Abstraction Layer, etc...)
  - Simple templates show how to add new instruments and interface with low-level drivers (TMControl)



Signal Input (RS SMA100B Signal Source)

Signal Frequency (MHz): 498.99295058

Power (dBm): 11.193

Mode: Low Noise ☑ Harmonic Filter

Connect Via: GPIB

GPIB Address: 28

Clock Input (RS SMA100B Clock Source)

Clock Frequency (MHz): 1000.00006144

Power (dBm): 6

Mode: Differential Square

Connect Via: GPIB

GPIB Address: 28

CSC module (Coherent Sampling Module)

Signal source: Signal Input

Clock source: Clock Input

FFT size: 32768

Precision (digits): 8

VDDA (Keysight B2962A Voltage Source)

4 wire CH: 1 ☑ Noise Filter ☑ Is Core Vdd

Voltage (mV): 900 ☐ Series R: 0

Idc Limit (mA): 50 ☑ Measure Idc: 12.3 mA

Connect Via: GPIB

GPIB Address: 18

VCM (Keysight B2962A Voltage Source)

4 wire CH: 2 ☑ Noise Filter ☐ Is Core Vdd

Voltage (mV): 465 ☐ Series R: 0

Idc Limit (mA): 10 ☑ Measure Idc: -0.007 mA

Connect Via: GPIB

GPIB Address: 18

VREFP (Keysight B2962A Voltage Source)

4 wire CH: 1 ☑ Noise Filter ☐ Is Core Vdd

Voltage (mV): 850 ☐ Series R: 0

Idc Limit (mA): 10 ☑ Measure Idc: 0.094 mA

Connect Via: GPIB

GPIB Address: 19

VREFM (Keysight B2962A Voltage Source)

4 wire CH: 2 ☑ Noise Filter ☐ Is Core Vdd

Voltage (mV): 50 ☐ Series R: 0

Idc Limit (mA): 10 ☑ Measure Idc: -0.033 mA

Connect Via: GPIB

GPIB Address: 19

VDDIO (Agilent N6705A Voltage Source)

CH: 1

Voltage (mV): 700 ☐ Is Core Vdd

Idc Limit (mA): 20

Connect Via: GPIB

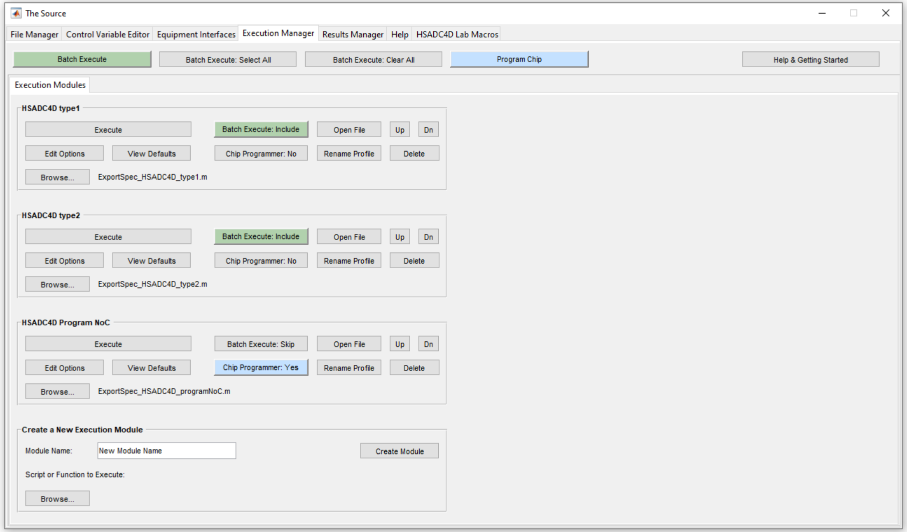
GPIB Address: 1

Export Control

Tour of the Common Modules

- Main Purpose
  - Export internal state to external formats
  - Execute any custom code in the local environment
  - Program your chip

- Features
  - No restrictions. Run whatever code you want.
  - No learning curve.
  - Allows for user-defined parameters to be defined
  - Built-in library with exporters for common formats



HSADC4D type1

Execute | Batch Execute: Include | Chip Programmer: No

ExportSpec_HSADC4D_type1.m

HSADC4D type2

Execute | Batch Execute: Include | Chip Programmer: No

ExportSpec_HSADC4D_type2.m

HSADC4D Program NoC

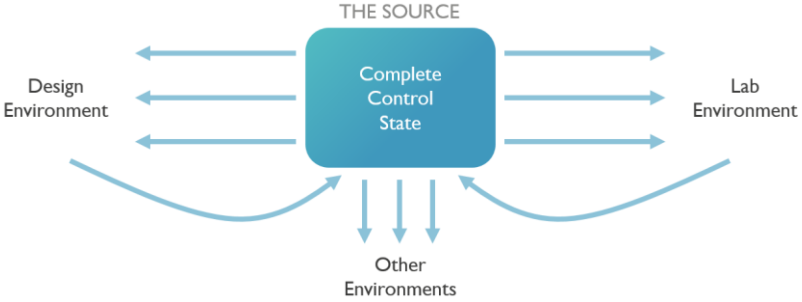
Execute | Batch Execute: Skip | Chip Programmer: Yes

ExportSpec_HSADC4D_programNoC.m

Create a New Execution Module

Module Name: New Module Name

Script or Function to Execute:



THE SOURCE

Complete Control State

Design Environment

Lab Environment

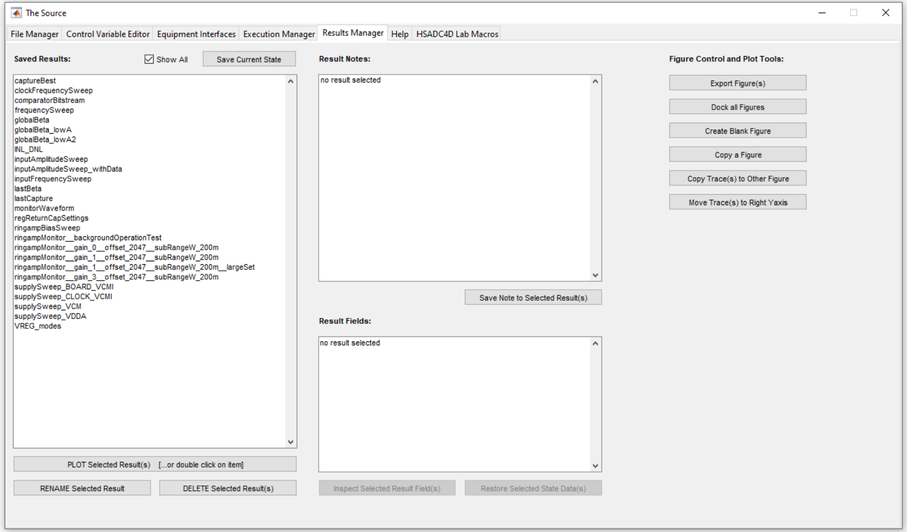
Other Environments

Results Manager

Tour of the Common Modules

- Main Purpose
  - Plot, analyze, organize, and annotate measurement results

- Features
  - “Auto-magically” knows how to plot your result.
  - Interactive plotting and analysis.
  - Helpful tools for creating figures for external reports, publications, etc.


The Source
File Manager
Control Variable Editor
Equipment Interfaces
Execution Manager
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Help
HSADC4D Lab Macros
☑ Show All
Save Current State
PLOT Selected Result(s) [...or double click on item]
RENAME Selected Result
DELETE Selected Result(s)
Save Note to Selected Result(s)
Inspect Selected Result Field(s)
Restore Selected State Data(s)
Figure Control and Plot Tools:
Export Figure(s)
Dock all Figures
Create Blank Figure
Copy a Figure
Copy Trace(s) to Other Figure
Move Trace(s) to Right Yaxis

Saved Results:

captureBest
clockFrequencySweep
comparatorBitstream
frequencySweep
globalBeta
globalBeta_lowA
globalBeta_lowA2
INL_DNL
inputAmplitudeSweep
inputAmplitudeSweep_withData
inputFrequencySweep
lastBeta
lastCapture
monitorWaveform
regReturnCapSettings
ringampBiasSweep
ringampMonitor__backgroundOperationTest
ringampMonitor__gain_0__offset_2047__subRangeW_200m
ringampMonitor__gain_1__offset_2047__subRangeW_200m
ringampMonitor__gain_1__offset_2047__subRangeW_200m__largeSet
ringampMonitor__gain_3__offset_2047__subRangeW_200m
supplySweep_BOARD_VCMI
supplySweep_CLOCK_VCMI
supplySweep_VCM
supplySweep_VDDA
VREG_modes

Result Notes:

no result selected

Result Fields:

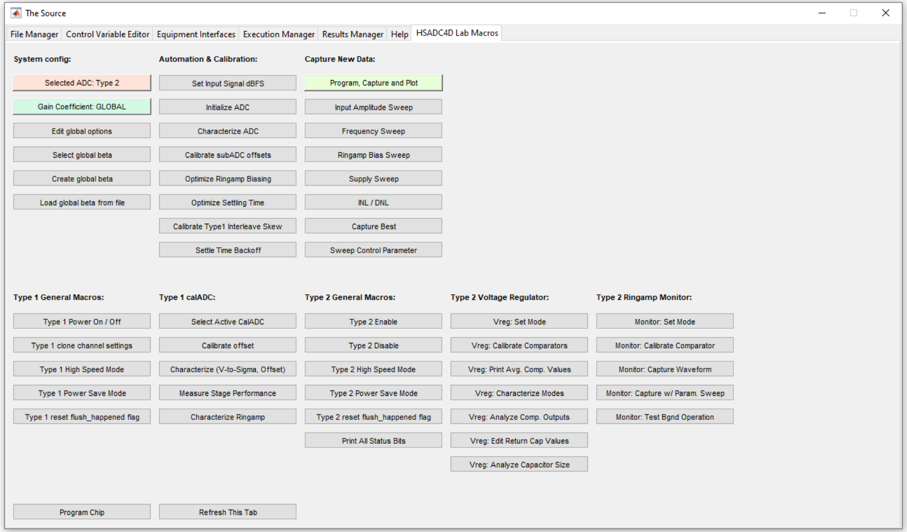
no result selected

Custom (User) Defined

Tour of the Common Modules

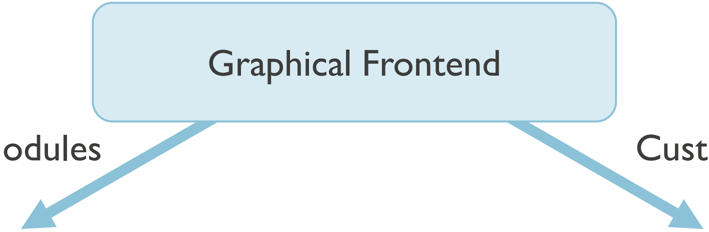
- Main Purpose
  - Customize your setup
  - Whatever you need it to be!

- Features
  - Extensive tools, templates, and examples provided for integrating your custom code into the GUI
  - Method of writing your functions that makes them "auto-magically" interactive
  - Extracts the default options out of your functions and lets the user edit them "auto-magically"



Combining Common & Custom Functionality

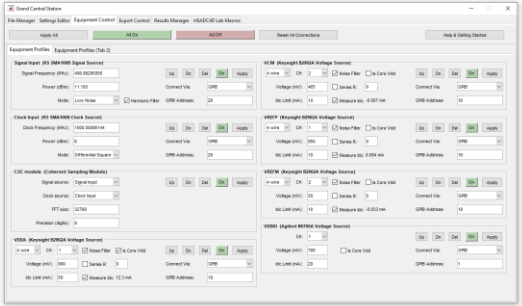
Top-level System Architecture



Graphical Frontend

Common Modules

Custom Modules



Signal Input (RS SMA100B Signal Source)
Signal Frequency (MHz): 498.99295058
Power (dBm): 11.193
Mode: Low Noise ☑ Harmonic Filter
Connect Via: GPIB
GPIB Address: 28

Clock Input (RS SMA100B Clock Source)
Clock Frequency (MHz): 1000.00006144
Power (dBm): 6
Mode: Differential Square
Connect Via: GPIB
GPIB Address: 28

CSC module (Coherent Sampling Module)
Signal source: Signal Input
Clock source: Clock Input
FFT size: 32768
Precision (digits): 8

VDDA (Keysight B2962A Voltage Source)
4 wire CH: 1 ☑ Noise Filter ☑ Is Core Vdd
Voltage (mV): 980 ☐ Series R: 0
Idc Limit (mA): 50 ☑ Measure Idc: 12.3 mA
Connect Via: GPIB
GPIB Address: 18

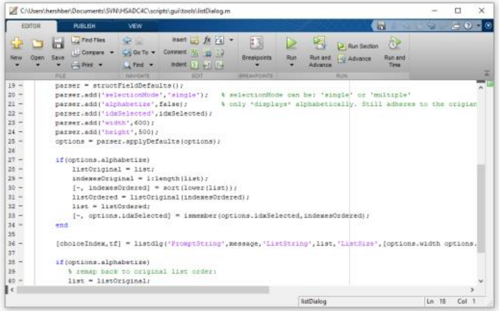
VCM (Keysight B2962A Voltage Source)
4 wire CH: 2 ☑ Noise Filter ☐ Is Core Vdd
Voltage (mV): 485 ☐ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: -0.007 mA
Connect Via: GPIB
GPIB Address: 18

VREFP (Keysight B2962A Voltage Source)
4 wire CH: 1 ☑ Noise Filter ☐ Is Core Vdd
Voltage (mV): 850 ☐ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: 0.094 mA
Connect Via: GPIB
GPIB Address: 19

VREFM (Keysight B2962A Voltage Source)
4 wire CH: 2 ☑ Noise Filter ☐ Is Core Vdd
Voltage (mV): 50 ☐ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: -0.033 mA
Connect Via: GPIB
GPIB Address: 19

VDDIO (Agilent N6705A Voltage Source)
CH: 1
Voltage (mV): 750 ☐ Is Core Vdd
Idc Limit (mA): 20
Connect Via: GPIB
GPIB Address: 1

API for custom code to interact with core code



```
    parser = structFieldDefaults();
    parser.add('selectionMode','single');   % selectionMode can be: 'single' or 'multiple'
    parser.add('alphabetize',false);        % only *displays* alphabetically. Still adheres to the origian
    parser.add('idxSelected',idxSelected);
    parser.add('width',400);
    parser.add('height',500);
    options = parser.applyDefaults(options);

    if(options.alphabetize)
        listOriginal = list;
        indexesOriginal = 1:length(list);
        [~, indexesOrdered] = sort(lower(list));
        listOrdered = listOriginal(indexesOrdered);
        list = listOrdered;
        [~, options.idxSelected] = ismember(options.idxSelected,indexesOrdered);
    end

    [choiceIndex,tf] = listdlg('PromptString',message,'ListString',list,'ListSize',[options.width options.

    if(options.alphabetize)
       % remap back to original list order:
       list = listOriginal;
```

Pre-built tools for graphical control of common tasks

Provided function library and templates to support rapid integration of custom functionality

Customization

Integrating Project-Specific Code

- Templates and examples to guide you the whole way
  - Follows a simple software engineering paradigm, with big benefits

- Code built using the provided templates will "auto-magically" support two modes of execution
  - Interactive mode - for use with the GUI
  - Function mode – for everything else

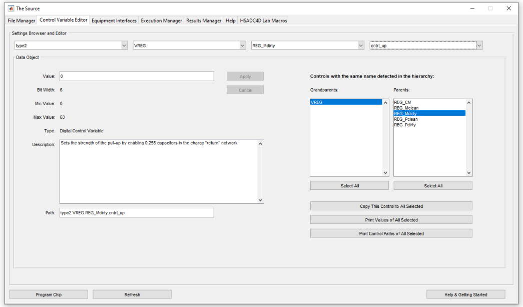
- More details in a future "hands-on" seminar

Key Benefits

Conclusions

- Productivity
  - It cannot be over-stated how much graphical control provides insight and boosts productivity

Visually inspect your chip's digital settings and experiment with different settings on-the-fly…



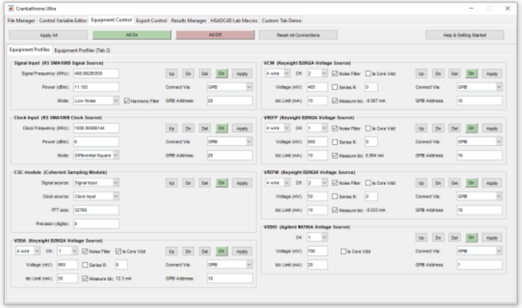
type2 | VREG | REG_Mdirty | cntrl_up

Value: 0
Bit Width: 6
Min Value: 0
Max Value: 63
Type: Digital Control Variable
Description: Sets the strength of the pull-up by enabling 0:255 capacitors in the charge "return" network
Path: type2.VREG.REG_Mdirty.cntrl_up

Grandparents:
VREG

Parents:
REG_CM
REG_Mclean
REG_Mdirty
REG_Pclean
REG_Pdirty

Click a button to sweep a voltage source and immediately see its effect on performance…



Signal Input (RS SMA100B Signal Source)
Signal Frequency (MHz): 498.98295858
Power (dBm): 11.193
Mode: Low Noise ☑ Harmonic Filter
Connect Via: GPIB
GPIB Address: 28

Clock Input (RS SMA100B Clock Source)
Clock Frequency (MHz): 1008.00008144
Power (dBm): 6
Mode: Differential Square
Connect Via: GPIB
GPIB Address: 28

CSC module (Coherent Sampling Module)
Signal source: Signal Input
Clock source: Clock Input
FFT size: 32768
Precision (digits): 8

VDDA (Keysight B2962A Voltage Source)
4 wire CH: 1 ☑ Noise Filter ☑ Is Core Vdd
Voltage (mV): 900 □ Series R: 8
Idc Limit (mA): 50 ☑ Measure Idc: 12.3 mA
Connect Via: GPIB
GPIB Address: 18

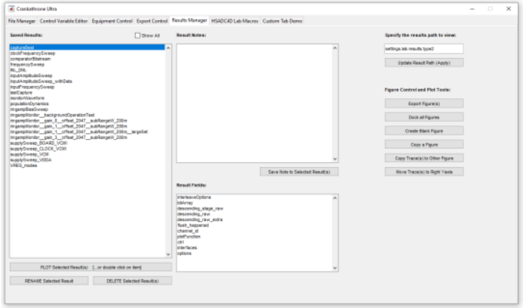
VCM (Keysight B2962A Voltage Source)
4 wire CH: 2 ☑ Noise Filter □ Is Core Vdd
Voltage (mV): 465 □ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: -0.007 mA
Connect Via: GPIB
GPIB Address: 18

VREFP (Keysight B2962A Voltage Source)
4 wire CH: 1 ☑ Noise Filter □ Is Core Vdd
Voltage (mV): 850 □ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: 0.994 mA
Connect Via: GPIB
GPIB Address: 19

VREFM (Keysight B2962A Voltage Source)
4 wire CH: 2 ☑ Noise Filter □ Is Core Vdd
Voltage (mV): 50 □ Series R: 0
Idc Limit (mA): 10 ☑ Measure Idc: -0.033 mA
Connect Via: GPIB
GPIB Address: 19

VDDIO (Agilent N6705A Voltage Source)
CH: 1
Voltage (mV): 700 □ Is Core Vdd
Idc Limit (mA): 20
Connect Via: GPIB
GPIB Address: 1

Run interactive analysis and plotting on the results you've acquired…



Saved Results:
captureBest
clockFrequencySweep
comparatorBitstream
frequencySweep
INL_DNL
inputAmplitudeSweep
inputAmplitudeSweep_withData
inputFrequencySweep
lastCapture
monitorWaveform
populationDynamics
ringampBiasSweep
ringampMonitor__backgroundOperationTest
ringampMonitor__gain_0__offset_2047__subRangeW_200m
ringampMonitor__gain_1__offset_2047__subRangeW_200m
ringampMonitor__gain_1__offset_2047__subRangeW_200m__largeSet
ringampMonitor__gain_3__offset_2047__subRangeW_200m
supplySweep_BOARD_VCM
supplySweep_CLOCK_VCM
supplySweep_VCM
supplySweep_VDDA
VREG_modes

Specify the results path to view: settings.lab.results.type2

Result Fields:
interleaveOptions
bitArray
descending_stage_raw
descending_raw
descending_raw_extra
flush_happened
channel_id
plotFunction
ctrl
interfaces
options

Key Benefits

Conclusions

- Reproducibility
  - Must Save / Load full representation of test setup
  - Must know what state was used to obtain a result
  - Must know what code was run to obtain the result, and with which user-defined parameters

- Usability
  - Graphical control and visualization of the complete system without needed to dig into code
  - Interactive execution flow of code that allows others to use your code without hacking it
  - Easy for others to understand how/where to make modifications

Will a colleague or external client be able to make sense of your work?

Key Benefits

Conclusions

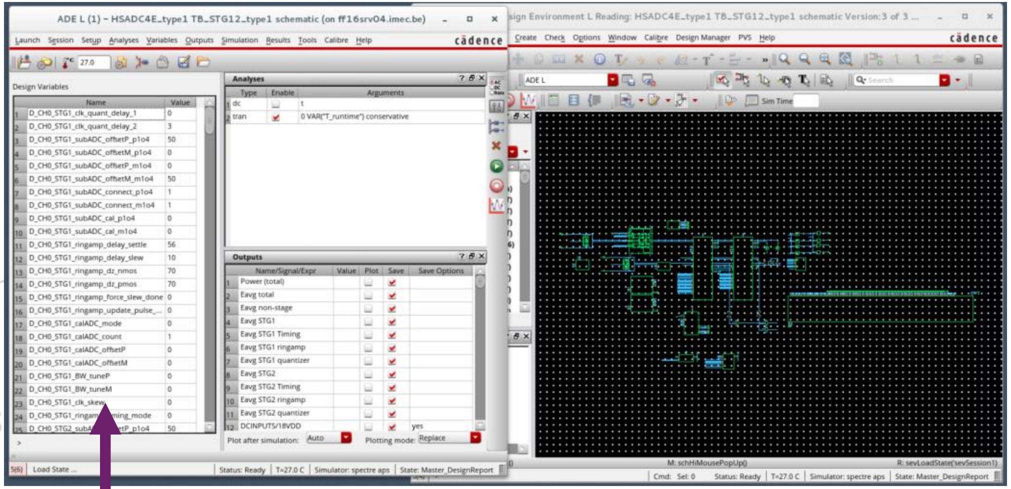
- Transferability
  - Delivery of saved state(s) alongside physical IP to partners
  - Deliver pre-configured or pre-initialized states for each physical sample
    - With the results from our lab attached as a benchmark
  - Partners can send files of their state for debug / advice
  - You can send them files from our lab for them to try

Will a colleague or external client be able to make sense of your work?

Key Benefits

Conclusions

- Your life in Cadence becomes easier
  - All ADE variable names/values in your testber
  - Ever simulated the wrong thing because your
  - Keeps multiple users on a team synchronized
  - Automated generation of digital blocks (e.g. S
- Moving between Cadence and the Lab is trivial
  - When the time comes to test, you're already
  - No problem going from lab back to Cadence (Example: using lab settings to conduct parasi
- Remote testing is awesome & very convenie
  - Reproducibility naturally leads to remote test
  - Just load up a state file and go!



ADE L (1) – HSADC4E_type1 TB_STG12_type1 schematic (on ff16srv04.imec.be)

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cādence
27.0
sign Environment L Reading: HSADC4E_type1 TB_STG12_type1 schematic Version:3 of 3 ...
Create Check Options Window Calibre Design Manager PVS Help
ADE L
Sim Time
M: schHiMousePopUp()
R: sevLoadState('sevSession1)

Design Variables

	Name	Value
1	D_CH0_STG1_clk_quant_delay_1	0
2	D_CH0_STG1_clk_quant_delay_2	3
3	D_CH0_STG1_subADC_offsetP_p1o4	50
4	D_CH0_STG1_subADC_offsetM_p1o4	0
5	D_CH0_STG1_subADC_offsetP_m1o4	0
6	D_CH0_STG1_subADC_offsetM_m1o4	50
7	D_CH0_STG1_subADC_connect_p1o4	1
8	D_CH0_STG1_subADC_connect_m1o4	1
9	D_CH0_STG1_subADC_cal_p1o4	0
10	D_CH0_STG1_subADC_cal_m1o4	0
11	D_CH0_STG1_ringamp_delay_settle	56
12	D_CH0_STG1_ringamp_delay_slew	10
13	D_CH0_STG1_ringamp_dz_nmos	70
14	D_CH0_STG1_ringamp_dz_pmos	70
15	D_CH0_STG1_ringamp_force_slew_done	0
16	D_CH0_STG1_ringamp_update_pulse_...	0
17	D_CH0_STG1_calADC_mode	0
18	D_CH0_STG1_calADC_count	1
19	D_CH0_STG1_calADC_offsetP	0
20	D_CH0_STG1_calADC_offsetM	0
21	D_CH0_STG1_BW_tuneP	0
22	D_CH0_STG1_BW_tuneM	0
23	D_CH0_STG1_clk_skew	0
24	D_CH0_STG1_ringam[illegible]ming_mode	0
25	D_CH0_STG2_subA[illegible]etP_p1o4	50

Analyses

	Type	Enable	Arguments
1	dc	□	t
2	tran	☑	0 VAR("T_runtime") conservative

Outputs

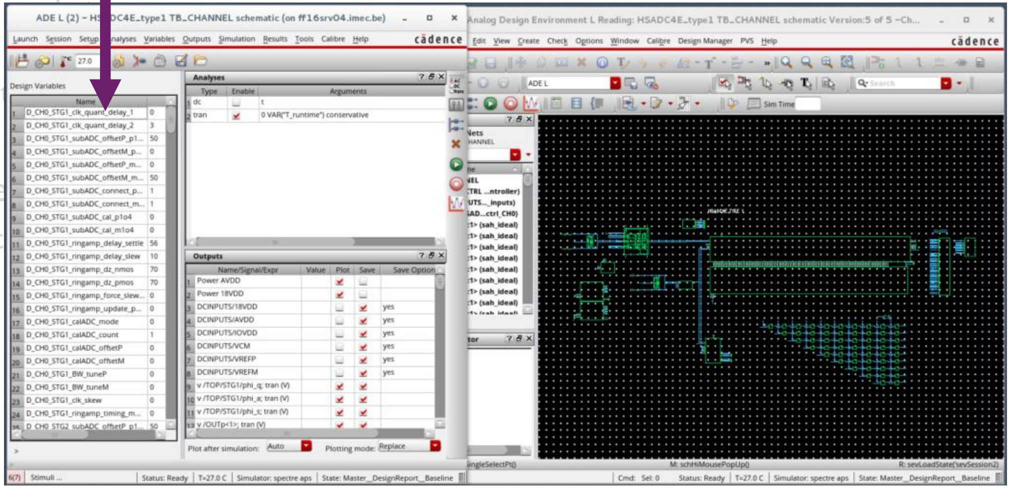
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	Power (total)		□	☑	
2	Eavg total		□	☑	
3	Eavg non-stage		□	☑	
4	Eavg STG1		□	☑	
5	Eavg STG1 Timing		□	☑	
6	Eavg STG1 ringamp		□	☑	
7	Eavg STG1 quantizer		□	☑	
8	Eavg STG2		□	☑	
9	Eavg STG2 Timing		□	☑	
10	Eavg STG2 ringamp		□	☑	
11	Eavg STG2 quantizer		□	☑	
12	DCINPUTS/18VDD		□	☑	yes

Plot after simulation: Auto Plotting mode: Replace

5(6) Load State ... | Status: Ready | T=27.0 C | Simulator: spectre aps | State: Master_DesignReport

Cmd: Sel: 0 | Status: Ready | T=27.0 C | Simulator: spectre aps | State: Master_DesignReport

How do I maintain a synchronized state?



ADE L (2) – HSADC4E_type1 TB_CHANNEL schematic (on ff16srv04.imec.be)

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cādence
27.0
Analog Design Environment L Reading: HSADC4E_type1 TB_CHANNEL schematic Version:5 of 5 –Ch...
Edit View Create Check Options Window Calibre Design Manager PVS Help
ADE L
Sim Time
Nets
M: schHiMousePopUp()
R: sevLoadState('sevSession2)

Design Variables

	Name	
1	D_CH0_STG1_clk_quant_delay_1	0
2	D_CH0_STG1_clk_quant_delay_2	3
3	D_CH0_STG1_subADC_offsetP_p1...	50
4	D_CH0_STG1_subADC_offsetM_p...	0
5	D_CH0_STG1_subADC_offsetP_m...	0
6	D_CH0_STG1_subADC_offsetM_m...	50
7	D_CH0_STG1_subADC_connect_p...	1
8	D_CH0_STG1_subADC_connect_m...	1
9	D_CH0_STG1_subADC_cal_p1o4	0
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11	D_CH0_STG1_ringamp_delay_settle	56
12	D_CH0_STG1_ringamp_delay_slew	10
13	D_CH0_STG1_ringamp_dz_nmos	70
14	D_CH0_STG1_ringamp_dz_pmos	70
15	D_CH0_STG1_ringamp_force_slew...	0
16	D_CH0_STG1_ringamp_update_p...	0
17	D_CH0_STG1_calADC_mode	0
18	D_CH0_STG1_calADC_count	1
19	D_CH0_STG1_calADC_offsetP	0
20	D_CH0_STG1_calADC_offsetM	0
21	D_CH0_STG1_BW_tuneP	0
22	D_CH0_STG1_BW_tuneM	0
23	D_CH0_STG1_clk_skew	0
24	D_CH0_STG1_ringamp_timing_m...	0
25	D_CH0_STG2_subADC_offsetP_p1...	50

Analyses

	Type	Enable	Arguments
1	dc	□	t
2	tran	☑	0 VAR("T_runtime") conservative

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Option
1	Power AVDD		☑	□	
2	Power 18VDD		☑	□	
3	DCINPUTS/18VDD		□	☑	yes
4	DCINPUTS/AVDD		□	☑	yes
5	DCINPUTS/IOVDD		□	☑	yes
6	DCINPUTS/VCM		□	☑	yes
7	DCINPUTS/VREFP		□	☑	yes
8	DCINPUTS/VREFM		□	☑	yes
9	v /TOP/STG1/phi_q; tran (V)		☑	☑	
10	v /TOP/STG1/phi_a; tran (V)		☑	☑	
11	v /TOP/STG1/phi_s; tran (V)		☑	☑	
12	v /OUTp<1>; tran (V)		☑	☑	

Plot after simulation: Auto Plotting mode: Replace

6(7) Stimuli ... | Status: Ready | T=27.0 C | Simulator: spectre aps | State: Master_DesignReport_Baseline

Cmd: Sel: 0 | Status: Ready | T=27.0 C | Simulator: spectre aps | State: Master_DesignReport_Baseline

Key Benefits

Conclusions

- Your life in Cadence becomes easier
  - All ADE variable names/values in your testbenches stay synchronized across the many levels of design hierarchy
  - Ever simulated the wrong thing because your testbench variables weren't setup how you expected?
  - Keeps multiple users on a team synchronized
  - Automated generation of digital blocks (e.g. SPI)

- Moving between Cadence and the Lab is trivial
  - When the time comes to test, you're already ready to go.
  - No problem going from lab back to Cadence either.
    (Example: using lab settings to conduct parasitic extraction investigations in simulation)

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  - Reproducibility naturally leads to remote testing capability
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Key Benefits

Conclusions

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- Remote testing is awesome & very convenient
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Key Benefits

Conclusions

- YOU will love this because it will make your job easier and certainly more fun
- YOUR COLLEAGUES will love this because they will be able to use your work without a master's degree in Spaghetti Code Interpreting
- OUR PARTNERS will love this because they will be able to test physical IP in a way that is reproducible, graphical, and intuitive

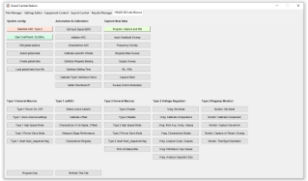
Okay, I'm sold! How do I get started?

- https://github.com/bhershberg/PrometheanToolkit

- Give back to the project
  - Looking for new project mods and code contributors
  - Sharp edges: a lot of code cleanup is still needed 😬

- Help and documentation
  - Templates, Examples, and Explanations already included in the codebase (via 'Help' tab)
  - Possible future work: Video tutorials on YouTube for all key topics
    - (only going to put time into doing this if I see community interest for it)

Questions?

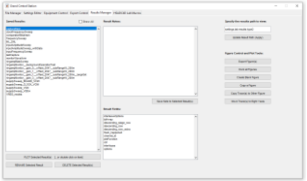


Custom GUI tab allows user to graphically execute custom functions

User graphically specifies the “options” that determine execution flow

```
results = yourCustomFunction(options);
```

Custom code executes



Results are available in the Results Manager for interactive plotting and analysis