Application Note

Beyond BA22 Power Management Unit

Confidential Information

beyond SEMICONDUCTOR

Figure depicts typical usage of power management functions provided by the BA22 processor:

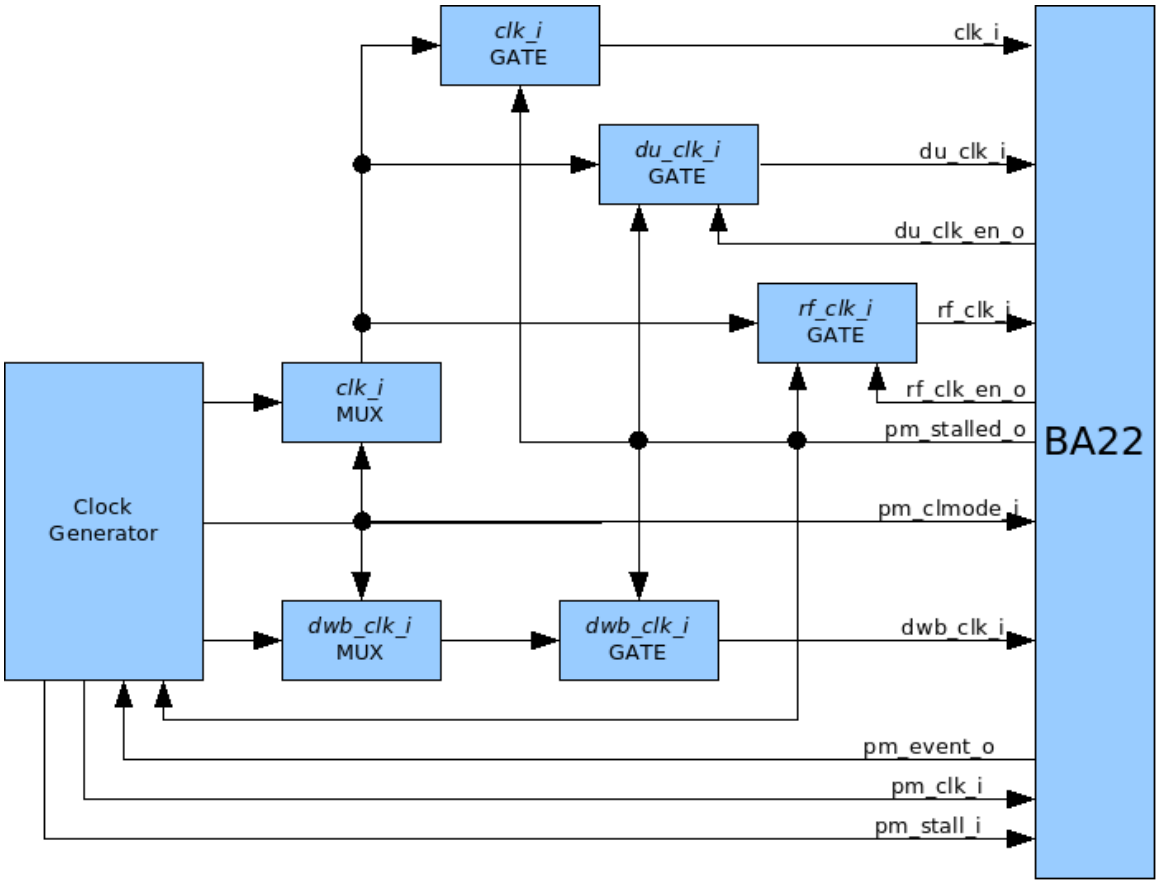

Figure 1: Typical Power Management application

The unit provides a simple handshaking interface to the clock management circuitry. The clock management asserts (high) *pm_stall_i* signal anytime it wants to change CPU's power state. It has to wait for the Power Management Unit to assert its *pm_stalled_o* signal before changing the clock mode and/or putting the CPU to power down mode. While *pm_stall_i* and *pm_stalled_o* are both asserted, external clock management can change clock speeds and ratios or gate the clocks off. If enabled, the Power Management Unit will assert its *pm_event_o* signal in response to internal tick timer and/or programmable interrupt controller interrupt assertion. This can be used to wake the CPU from gated clocks mode. It is recommended that all clocks are turned on and stable and that *pm_clmode_i* value is appropriate before you de-assert the *pm_stall_i* signal.

All handshaking signals are synchronous to *pm_clk_i*.

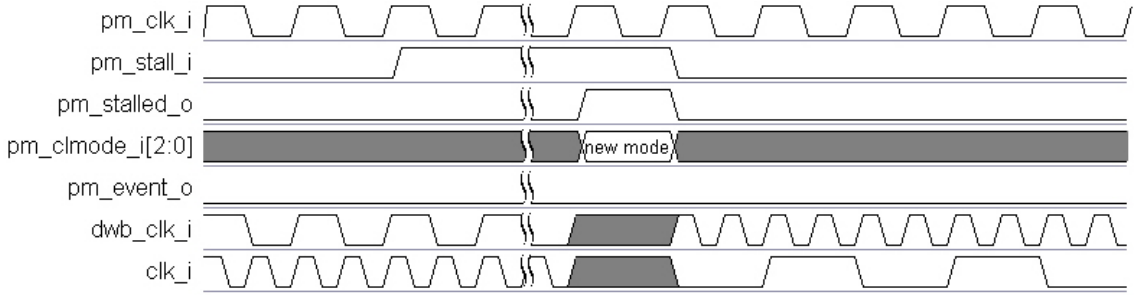

Figure 2: Power Management Clock Mode Change

The time between *pm_stall_i* and *pm_stalled_o* assertion varies depending on what instructions are present in the CPU's pipeline at the time *pm_stall_i* is asserted. Note that combinatorial path exists between *pm_stall_i* and *pm_stalled_o* in order to achieve timing in the diagram. At the time *pm_stall_i* and *pm_stalled_o* are both asserted, *clk_i* and *dwb_clk_i* are marked invalid in the figure to represent that an arbitrary clock ratio is possible at this time. This does not imply clocks can become asynchronous or violate achieved minimum clock period – clock switching must be clean and glitch free.

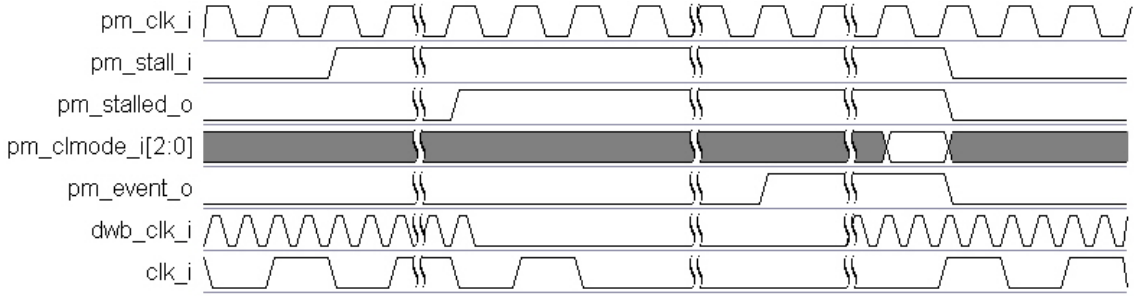

Figure 3: Power Management Clock Gating

The waveform depicts typical clock gating application. External clock management circuit can turn clocks off while both *pm_stall_i* and *pm_stalled_o* are asserted. It may use *pm_event_o* signal to trigger the wakeup procedure or the wakeup procedure can be triggered automatically on other, external conditions. Clock mode is also allowed to change during the wakeup procedure as clock gating and clock mode switch are functionally equivalent.

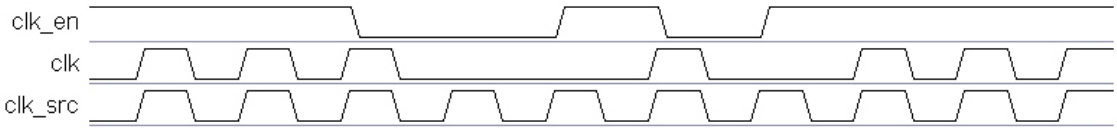

Figure 4: Per Cycle, Per Unit Clock Gating

Waveform shows required relationship between source clock, gated clock and clock gating signal for applicable units (Register File, Debug Unit).

The unit implements its own set of Special Purpose Registers which are software accessible using *mtspr* and *mfspr* instructions. The registers can be accessed in supervisor mode only. When accessed in non-supervisor mode, reads return undefined data and writes are ignored.

Power Management SPRs start at offset 0x4000 (group 8). Register implementations are optional – if a particular register is not implemented, then the functionality it provides is not available. Reads of an unimplemented register return undefined value and writes are ignored.

Power Management Event Control Register

You must define *BA22_PM_EVENT_IMPL* compile time parameter in *ba22_defines.v* file in order to use power management event feature. When not implemented, follow these rules:

- *pm_event_o* signal shall not be used for any purpose.

Register offset is 0x0. Register's layout is described in the table:

Bit(s)	Field	Access	Description
[0]	PIC IRQ PM Event Enable	R/W	Reset value 0b0. Write 1 to this bit, if you want Programmable Interrupt Controller to trigger external Power Management Event *(pm_event_o)*. Event is triggered only if *pm_stall_i* and *pm_stalled_o* are both asserted and *pm_clk_i* is running. If PIC is not implemented, value has no effect.
[1]	TT IRQ PM Event Enable	R/W	Reset value 0b0. Write 1 to this bit, if you want Tick Timer to trigger external Power Management Event *(pm_event_o)*. Event is triggered only if *pm_stall_i* and *pm_stalled_o* are both asserted and *pm_clk_i* is running. If timer is not implemented, value has no effect.
[31:2]	Reserved	NA	Write with 0x0, reads undefined.

Table 1: Power Management Event Control Register

Unit(s) Power Down Control Register

You must define *BA22_PM_UNIT_PD_IMPL* compile time parameter in *ba22_defines.v* if you want features provided by this register to be implemented. When NOT implemented, you must follow these rules:

- *du_clk_en_o* shall not be used for any purpose.
- *du_clk_i* shall be connected to same source as *clk_i*.

Register offset is 0x2. Layout and field descriptions are provided in the table:

Bit(s)	Field	Access	Description
[0]	Debug Unit Enable	R/W	Reset value compile time configurable (BA22_PM_PWR_UP_DU_CLK_EN). Write 0b1 to this field to enable Debug Unit. When Debug Unit disabled, *du_clk_en_o* is de-asserted, which can be used for *du_clk_i* clock gating.
[31:1]	Reserved	NA	Write data discarded, read data undefined.

Table 2: Unit(s) Power Down Control Register