universidade de aveiro

Grupo 1, Lab 3

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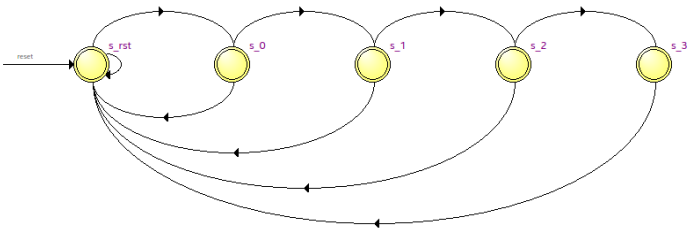
Assignment 1 – Hadamard codes

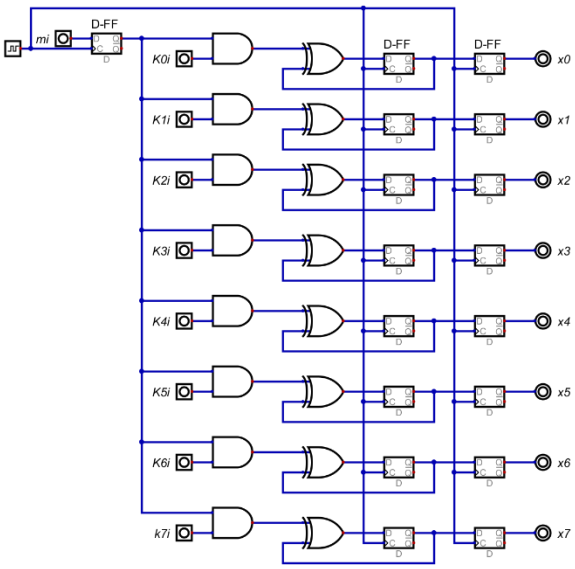
The challenge is to design a solution for an encoder and a decorder that implements a combinatorial algorithm for message transmission with the error correcting properties developed by Richard Hamming using Hadamard codes of class $[8, 4, 4]_2$, described as [n, k, d], were n=blocklength, k=message length and d=minimum distance, or $[2^k, K, 2^{k-1}]$.

An additional requirement stipulates that either one, the encoder or the decoder, should implement a serial(series) input, and the other one a parallel input, so our choice was to implement a serial input encoder and a parallel input decoder.

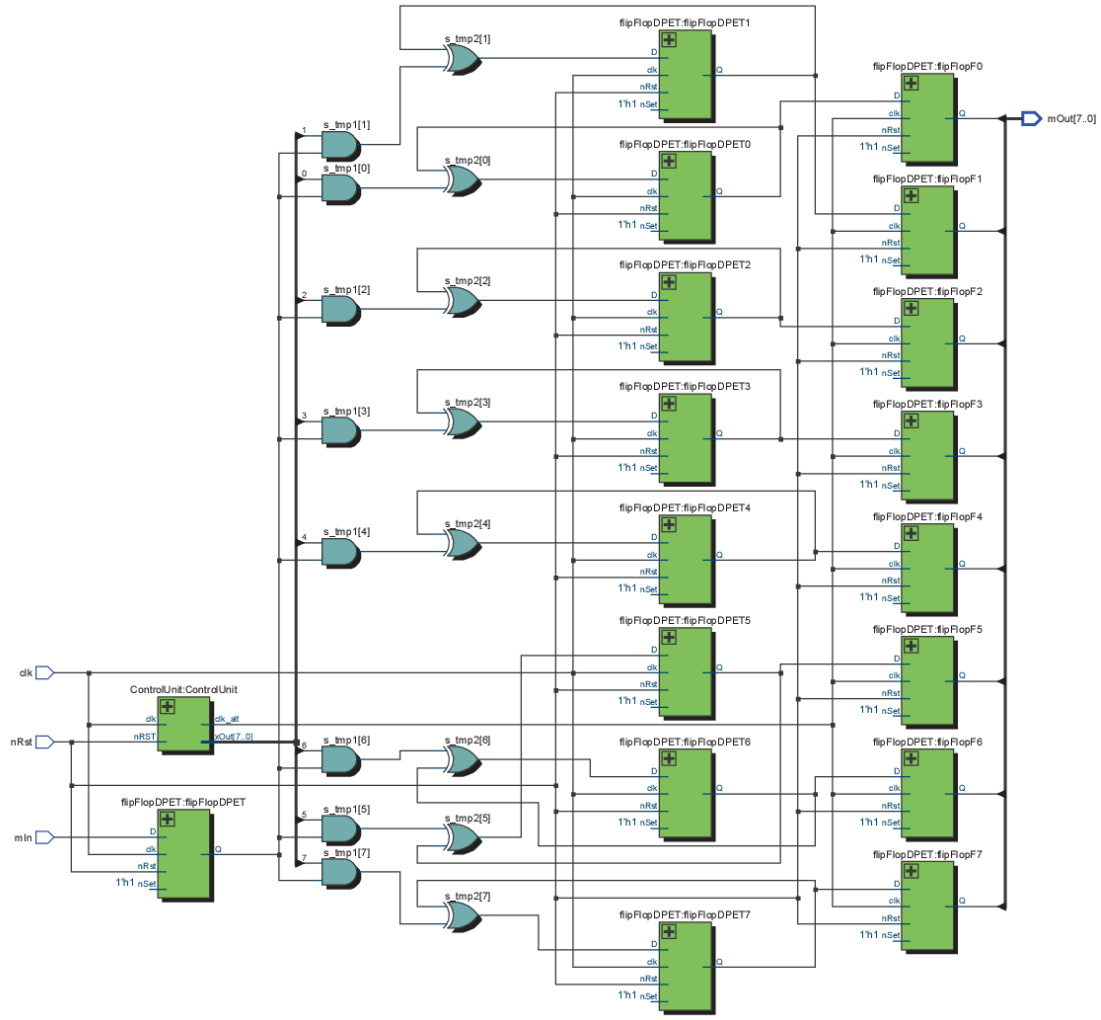
1. Serial input encoder:

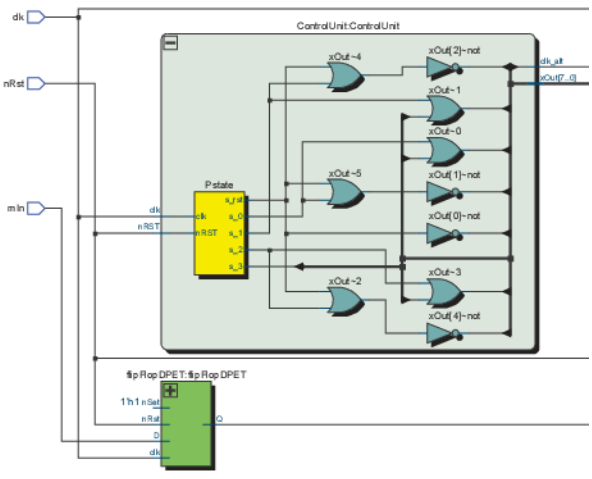
1.1. Data flow and serial-parallel control unit implementation

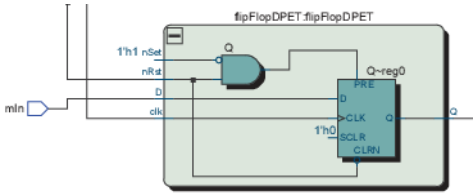




1.2. Circuit interface and schematics of the internal organization:



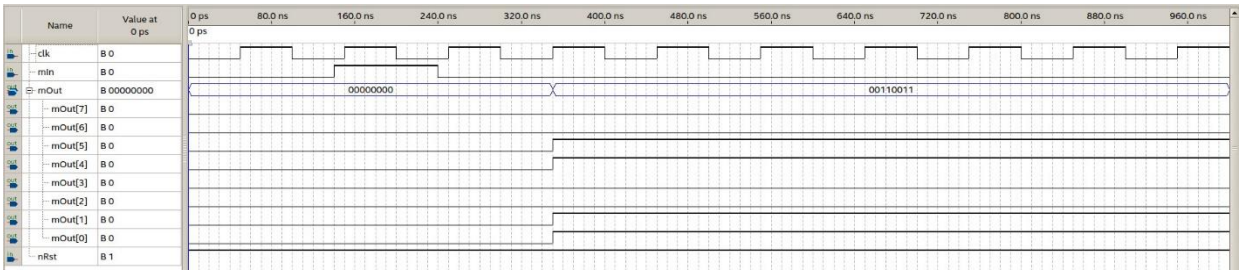




1.3. Implementation cost:

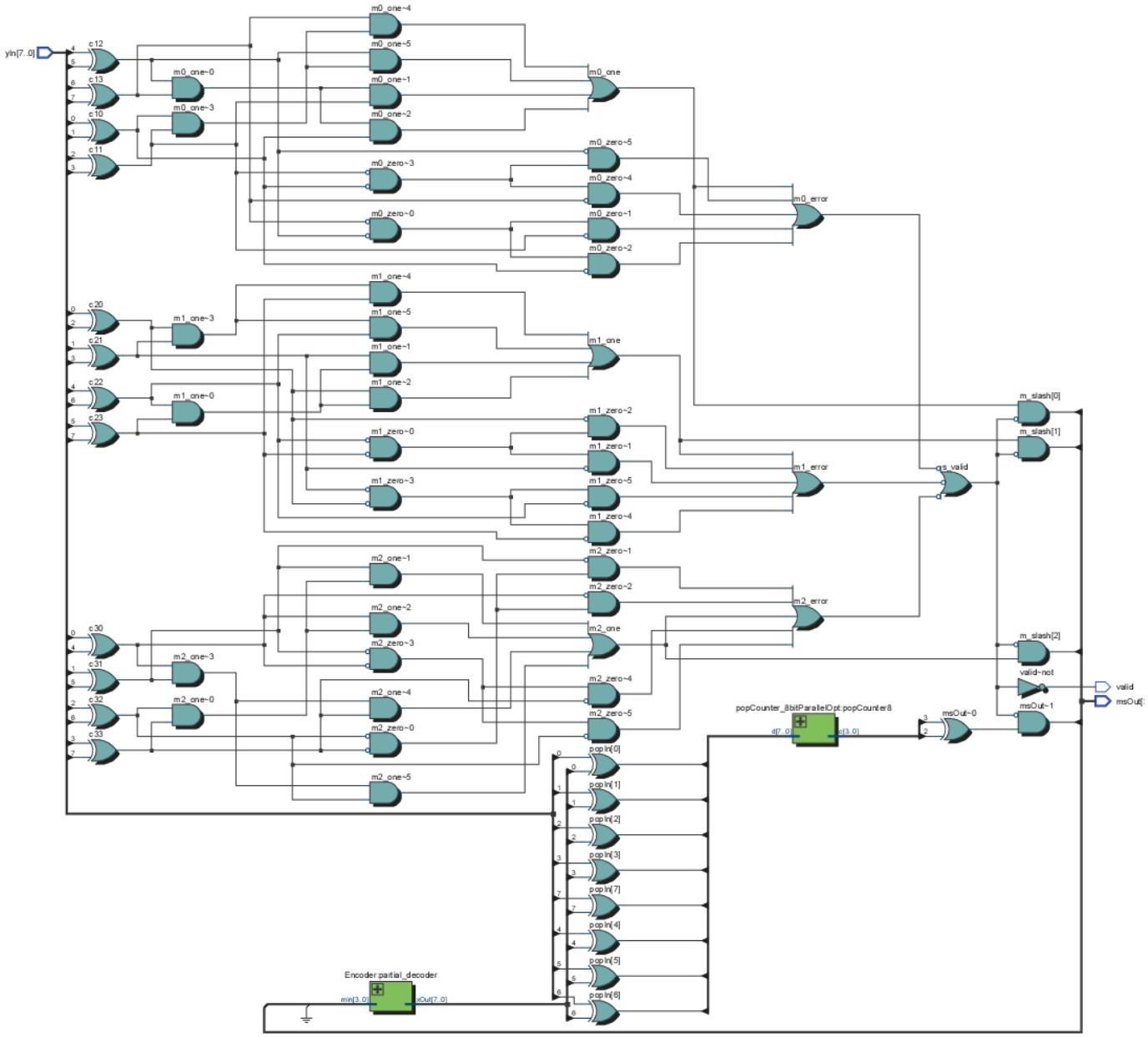
14 AND gates, 8 XOR gates, 4 NOT gates and 17 D Flip-Flop PET.

1.4. Quartus project and operation simulation:



2. Parallel input decoder:

2.1 Circuit interface and schematics of the internal organization:



2.2. Implementation cost:

20 XOR, 40 AND, 23 OR, 29 NOT and 1 8-bit POPCounter.

8-bit POPCounter =

4x(1XOR + 1AND) +
2x[(1XOR + 1AND) + (2XOR + 1AND)] +
(1XOR + 1AND) + (2XOR + 2AND + 1OR) + (2XOR + 1AND) =
= 15XOR + 12AND + 1OR

8-bit POPCounter Propagation Delay =

Stage 0: 1XOR gate

Stage 1: 2XOR gates

Stage 2: 2XOR gates + 1AND gate + 1OR gate

Total: 5XOR gates + 1AND gate + 1OR gate

TOTAL COST = 35XOR, 52AND, 24OR, 29NOT

Total Propagation Delay =

m'3 path :

Stage 0: 1XOR gate

Stage 1: 5XOR gates + 1AND gate + 1OR gate (8-bit POPCounter)

Stage 2: 1XOR gates + 1AND gate

Total: 7XOR gates + 2AND gates + 1OR gate

m'0, m'1 and m'2 path worst case:

Stage 0: 1XOR gate + 1AND gate

Stage 1: 1NOT gate + 1AND gate (inverted input AND gate)

Stage 2: 1NOT gate + 1AND gate (inverted input AND gate)

Stage 3: 1OR gate

Stage 4: 1NOT gate + 1OR gate (inverted input OR gate)

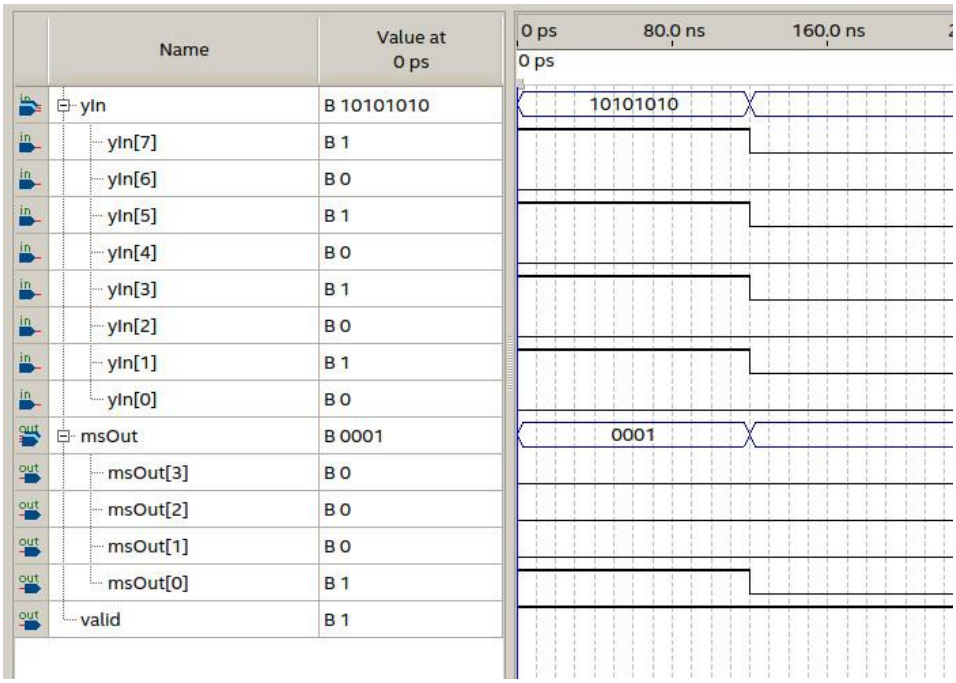
Stage 5: 1NOT gate + 1AND gate (inverted input AND gate)

Total: 4NOT gates + 1XOR gate + 4AND gates + 2OR gates

2.3. Quartus project and operation simulation:

Simulation1

Simulation2


Name
Value at
0 ps
yIn
B 10101010
yIn[7]
B 1
yIn[6]
B 0
yIn[5]
B 1
yIn[4]
B 0
yIn[3]
B 1
yIn[2]
B 0
yIn[1]
B 1
yIn[0]
B 0
msOut
B 0001
msOut[3]
B 0
msOut[2]
B 0
msOut[1]
B 0
msOut[0]
B 1
valid
B 1
0 ps
80.0 ns
160.0 ns
0 ps
10101010
0001