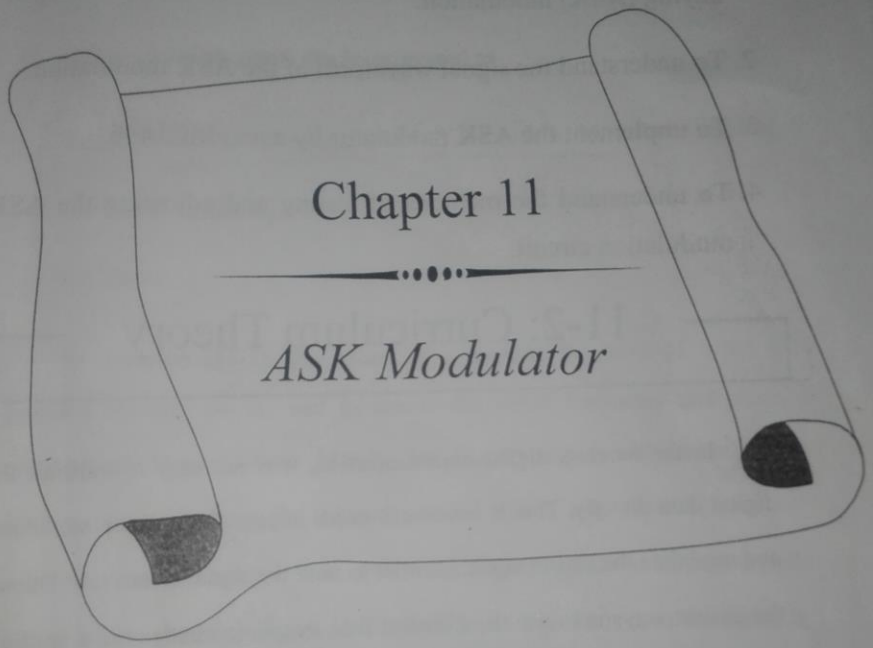


Chapter 11

ASK Modulator

11-1: Curriculum Objectives

1. To understand the operation theory of the amplitude shift keying (ASK) modulation.
2. To understand the signal waveform of the ASK modulation.
3. To implement the ASK modulator by using MC1496.
4. To understand the methods of testing and adjusting the ASK modulation circuit.

11-2: Curriculum Theory

In the wireless digital communication, it is not easy to transmit the digital data directly. This is because it needs to pass through the modulator and modulate the carrier signal in order to send the signal effectively. One of the easiest ways is to use the different data stream to change the amplitude of carrier, this kind of modulation is called amplitude modulation, and we call it as amplitude shift keying (ASK) modulation in digital communication.

Figure 11-1 is the basic circuit diagram of ASK modulator. Let the input data be 5 V, when the signal pass through the buffer, the switch S1 will

switch to point A, at this time the ASK output waveform is f_1. When the input data is 0 V, when the signal pass through the buffer, the switch S1 will switch to point B, at this time the ASK output waveform is DC 0 V. The above-mentioned is the basic theory of ASK modulation.

ASK modulation signal can be expressed as

$$x_{ASK}(t) = A_i \cos(\omega_c t + \phi_0); \quad 0 \le t \le T, i = 1, 2, \cdots, M \qquad (11\text{-}1)$$

ω_c: Cutoff frequency.

ϕ_0: Phase

In equation (11-1), the values of amplitude A_i have M types of possible change, the ω_c and ϕ_0 denote the cutoff frequency and phase, respectively. If we choose $M = 2$, the $x_{ASK}(t)$ signal will transmit the binary signal, therefore, the values of A are $A_1 = 0$ and $A_2 = A$, A is the arbitrary constant so we can obtain the binary ASK modulated signal waveform as shown in figure 11-2. When input logic is 1, then the signal is transmitted out; when the input logic is 0, then no signal is transmitted, so this also called on-off keying (OOK), this type of method is used in the past time.

In this chapter, we utilize 2206 IC waveform generator and MC1496 multiplier to produce the modulated ASK signal. First of all lets introduce

the characteristics of 2206 IC. 2206 IC is a waveform generator, which is similar to 8038 IC. Figure 11-3 is the circuit diagram of the ASK modulator by using 2206 IC. In figure 11-3, resistors R_2, R_5 comprise a voltage divided circuit. The main function of the voltage divided circuit is to let the negative voltage waveform of the 2206 IC operates normally. The oscillation frequency of 2206 IC is determined by resistor R_1 and the resistor located at pin 8. Its oscillation frequencies are $f_1 = 1/2\pi R_1 C$, $f_2 = 1/2\pi RC$ where R is the resistor at pin 8. If $R = \infty$, then frequency f_2 equal to zero. There is an internal comparator in 2206 IC. Assume that when the input is 5 V, the output frequency is f_1, and when the input is 0 V, the output frequency is f_2. We can utilize the TTL signal at pin 9 to control the output frequency to be f_1 or f_2. This type of structure is similar to the structure in figure 11-1. Therefore, by using the characteristic of this structure, we can achieve ASK modulation easily.

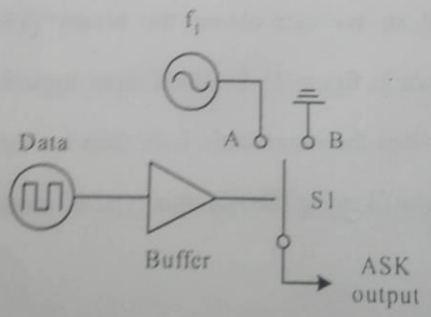


Figure 11-1 Basic circuit diagram of ASK modulator.

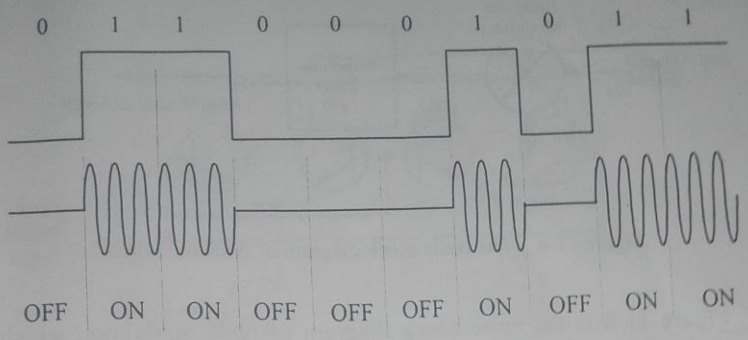


Figure 11-2 ASK modulation signal waveform.

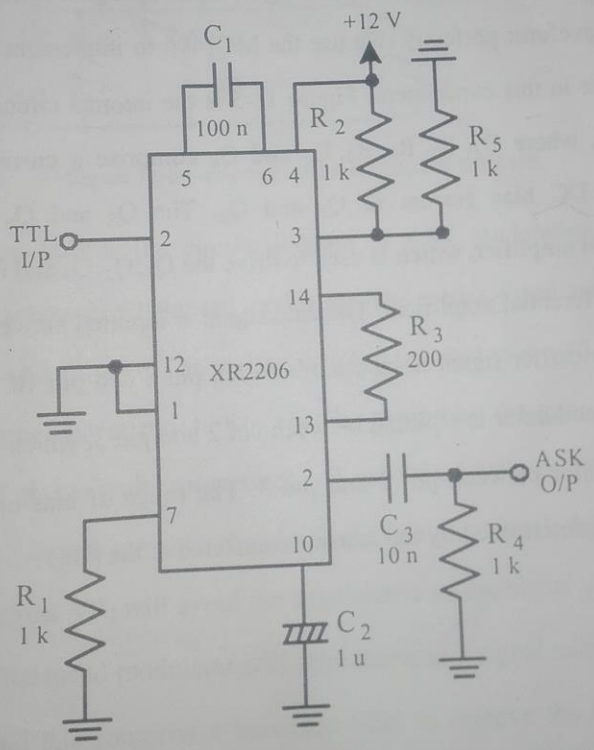


Figure 11-3 Circuit diagram of ASK modulator by using 2206 IC.

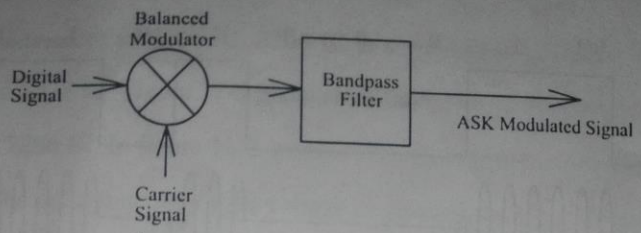


Figure 11-4 The basic block diagram of ASK modulator.

Figure 11-4 is the basic block diagram of ASK modulator, which the balanced modulator can meet the objectives of amplitude modulation, and the bandpass filter will remove the high frequency signal to make the ASK signal waveform perfectly. We use the MC1496 to implement the balanced modulator in this experiment. Figure 11-5 is the internal circuit diagram of MC1496, where D_1, R_1, R_2, R_3, Q_7 and Q_8 comprise a current source, it provides DC bias current to Q_5 and Q_6. The Q_5 and Q_6 comprise a differential amplifier, which is used to drive the Q_1, Q_2, Q_3 and Q_4 to become double differential amplifiers. The data signal is inputted between pin 1 and pin 4. The carrier signal is inputted between pin 8 and pin 10. The gain of balanced modulator is inputted between pin 2 and pin 3, which is controlled by the resistor between pin 2 and pin 3. The range of bias current of the amplifier is determined by the resistor connected at the pin 5.

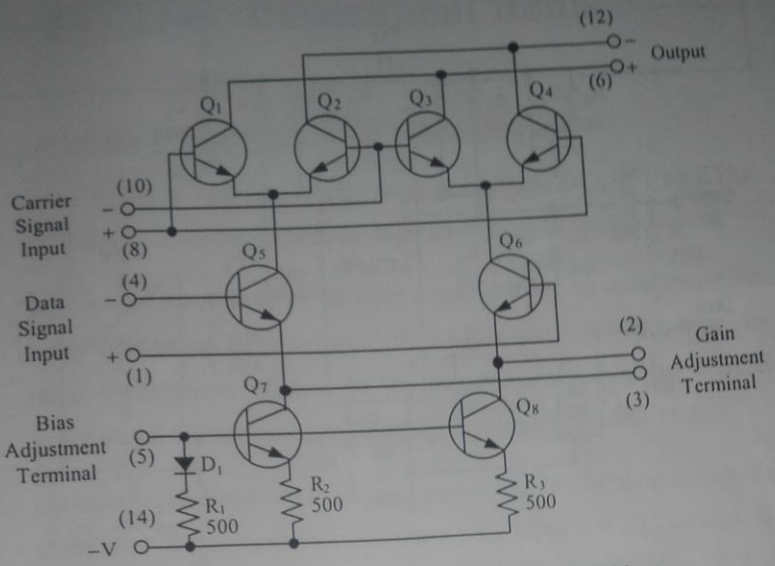


Figure 11-3 Internal circuit diagram of MC1496.

Figure 11-6 is the circuit diagram of ASK modulation, which the MC1496 comprises a balanced modulator. The carrier signal and data signal are single-ended input. The carrier signal is inputted at pin 10 and the data signal is inputted at pin 1. R_{13} and R_{14} determine the gain and the bias current of this circuit, respectively. If we adjust VR_1 or the data signal amplitude, it can prevent the ASK modulation signal from distortion. Slightly adjust VR_2 will avoid the asymmetric of the signal waveform. The pin 12 of balanced modulator will send the output signal to uA741. The C_3, R_{17}, R_{18} and R_{19} comprise a bandpass filter to remove the high frequency signal, so that the ASK signal waveform will become more perfect.

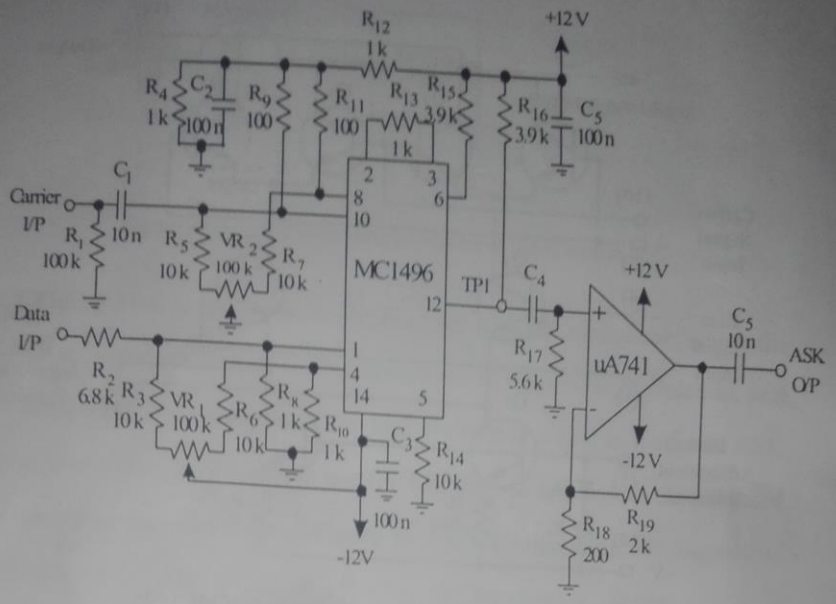


Figure 11-6 Circuit diagram of ASK modulator by using MC1496.

11-3: Experiment Items

Experiment 1: XR 2206 ASK modulator

1. Refer to figure 11-3, R_1 = 1 kΩ or refer to figure DCS11-1 on ETEK DCS-6000-06 module. Let J2 be short circuit and J3 be open circuit.
2. Let the two terminal of I/P be short circuit and JP1 be open circuit, i.e. at the data signal input terminal (Data I/P), input 0 V DC voltage. By using oscilloscope, observe on the output signal waveform of ASK signal (ASK O/P), then record the measured results in table 11-1.
3. Let the two terminal of I/P be open circuit and JP1 be short circuit, i.e. at the data signal input terminal (Data I/P), input 5 V DC voltage. By using oscilloscope, observe on the output signal waveform of ASK signal (ASK O/P), then record the measured results in table 11-1.
4. At the data signal input terminal (Data I/P), input 5 V amplitude, 100 Hz TTL signal. By using oscilloscope, observe on the output signal waveform of ASK signal (ASK O/P), then record the measured results in table 11-1.
5. According to the input signal in table 11-1, repeat step 4 and record the measured results in table 11-1.
6. Refer to figure 11-3, R_1 = 510 Ω or refer to figure DCS11-1 on ETEK DCS-6000-06 module. Let J2 be open circuit and J3 be short circuit.
7. According to the input signal in table 11-2, repeat step 2 to step 4 and record the measured results in table 11-2.

Experiment 2: MC 1496 ASK modulator

1. Refer to figure 11-6 or refer to figure DCS11-2 on ETEK DCS-6000-06 module.
2. At the data signal input terminal (Data I/P), input 5 V amplitude, 500 Hz TTL signal. Then at the carrier signal input terminal (Carrier I/P), input 400 mV amplitude and 20 kHz sine wave frequency.
3. By using oscilloscope, observe on the output signal waveform of the modulated ASK signal (ASK O/P). Adjust VR_1 until the signal does not occur distortion. Then adjust VR_2 to avoid the asymmetry of the signal. Finally record the output signal waveform of the balanced modulator (TP1) and the ASK O/P in table 11-3.
4. According to the input signal in table 11-3, repeat step 2 to step 3 and record the measured results in table 11-3.
5. At the data signal input terminal (Data I/P), input 5 V amplitude, 1 kHz TTL signal. Then at the carrier signal input terminal (Carrier I/P), input 400 mV amplitude and 20 kHz sine wave frequency.
6. Follow the adjustment in step 3, then record the output signal waveform of the balanced modulator (TP1) and the ASK O/P in table 11-4.
7. According to the input signal in table 11-4, repeat step 5 to step 6 and record the measured results in table 11-4.
8. At the data signal input terminal (Data I/P), input 5 V amplitude, 1 kHz TTL signal. Then at the carrier signal input terminal (Carrier I/P), input 400 mV amplitude and 100 kHz sine wave frequency.

9. Follow the adjustment in step 3, then record the output signal waveform of the balanced modulator (TP1) and the ASK O/P in table 11-5.

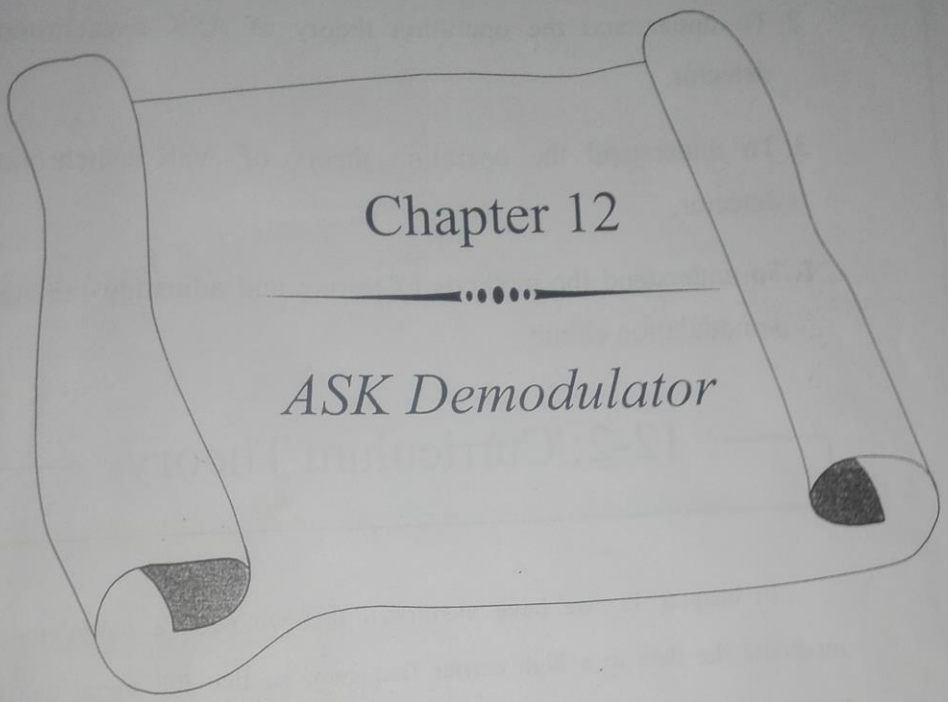
10. According to the input signal in table 11-5, repeat step 5 to step 6 and record the measured results in table 11-5.

11-5: Problems Discussion

1. In figure 11-6, what are the functions of μA741, C_3, R_{17}, R_{18} and R_{19}?

2. In figure 11-6, what are the purposes of VR_1 and VR_2?

3. In figure 11-6, what are the purposes of R_{13} and R_{14}?



Chapter 12

ASK Demodulator

12-1: Curriculum Objectives

1. To understand the operation theory of ASK demodulation.
2. To understand the operation theory of ASK asynchronous detector.
3. To understand the operation theory of ASK synchronous detector.
4. To understand the methods of testing and adjusting the ASK demodulation circuit.

12-2: Curriculum Theory

In chapter 11, we have mentioned that we need a modulator to modulate the data to a high carrier frequency, so that the signal can be transmitted effectively. Therefore, for receiver, we must convert the digital signal back to the modulating signal. Figure 12-1 shows the theoretical diagram of ASK demodulation. There are two methods to design the ASK demodulator, which are asynchronous detector and synchronous detector. We will discuss these two types of ASK demodulator in this chapter.

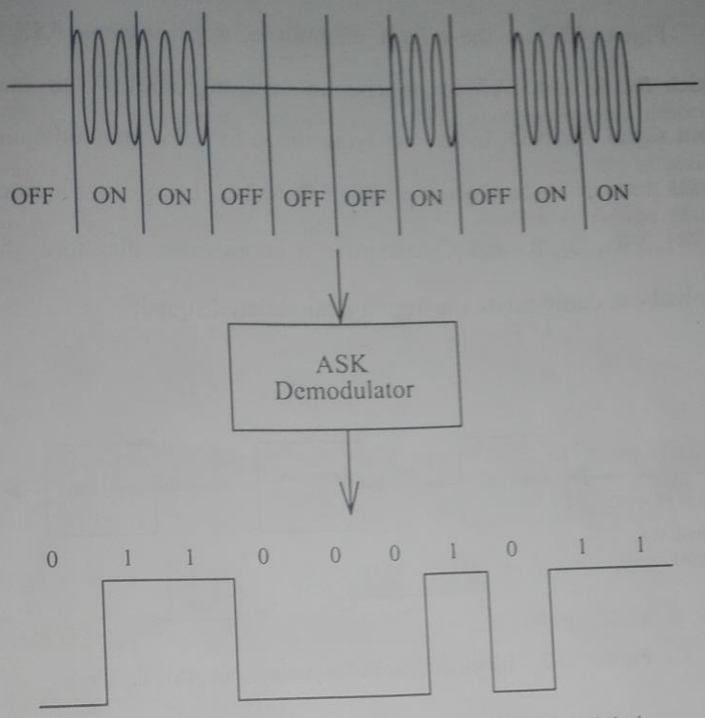


Figure 12-1 Theoretical diagram of ASK demodulation.

1. Asynchronous ASK Detector.

Figure 12-2 is the block diagram of asynchronous ASK detector. This structure is a typical asynchronous ASK detector. When the ASK signal pass through the rectifier, we can obtain the positive half wave signal. After that the signal will pass through a low-pass filter and obtain an envelop detection. Then get rid of the DC signal, the digital signal will be recurred.

Figure 12-3 is the circuit diagram of asynchronous ASK detector, which R_1, R_2 and μA741 comprise an inverting amplifier to amplify the input signal. Then D_1 is the rectifying diode to make the modulation signal passes through D_1 half wave rectifier. R_3 and C_1 comprise a low-pass filter. μA741, VR_1, D_2, R_4 and C_2 comprise a comparator, therefore, the output terminal can demodulate the digital demodulated signal.

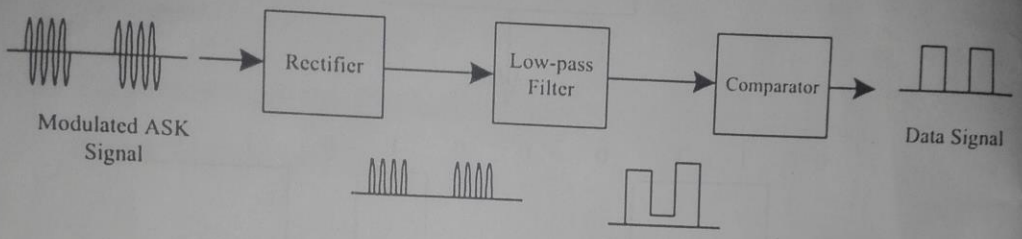


Figure 12-2 Block diagram of asynchronous ASK detector.

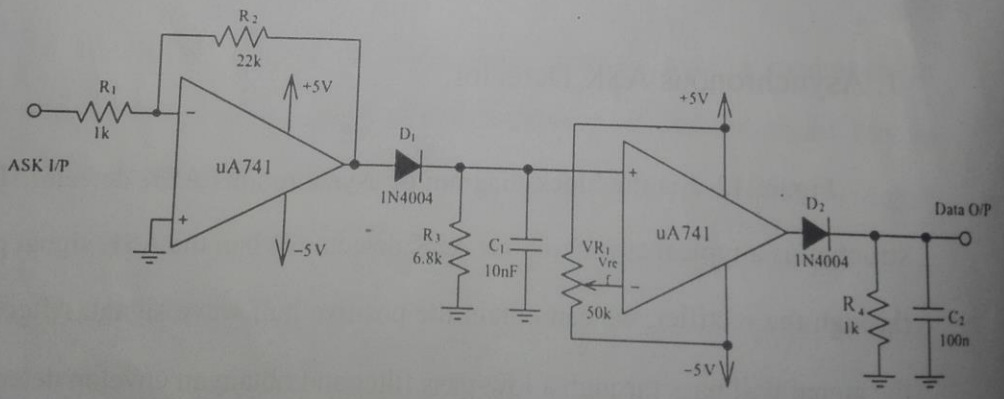


Figure 12-3 Circuit diagram of ASK asynchronous detector.

2. Synchronous ASK Detector

We have mentioned before that we can use synchronous detector to design the ASK demodulation. This experiment utilizes the structure of square-law detector and the block diagram is shown in figure 12-4. Let $x_{ASK}(t)$ be the ASK modulated signal, which is

$$x_{ASK}(t) = A_i \cos(\omega_c t + \phi_0); \quad 0 \le t \le T, \quad i = 1, 2, \cdots, M \qquad (12\text{-}1)$$

In equation (12-1), the values of amplitude A_i have M types of possible change, the ω_c and ϕ_0 denote the cutoff frequency and phase constant, respectively. When we input the ASK modulated signal to the two input terminals of balance modulator, then the output signal of balanced modulator can be expressed as

$$\begin{aligned} x_{out}(t) &= k x_{ASK}(t)\, x_{ASK}(t) \\ &= k A_i^2 \cos^2(\omega_C + \phi_0) \\ &= \frac{kA_i^2}{2} + \frac{kA_i^2}{2}\cos(2\omega_C t + 2\phi_0) \end{aligned} \qquad (12\text{-}2)$$

where $0 \le t \le T$, $i = 1, 2, \cdots, M$

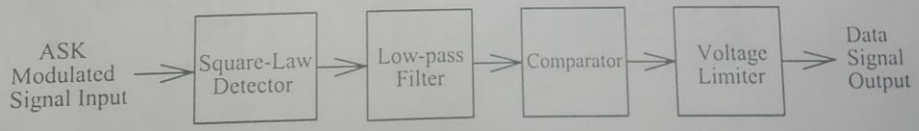


Figure 12-4 Basic block diagram of ASK demodulator.

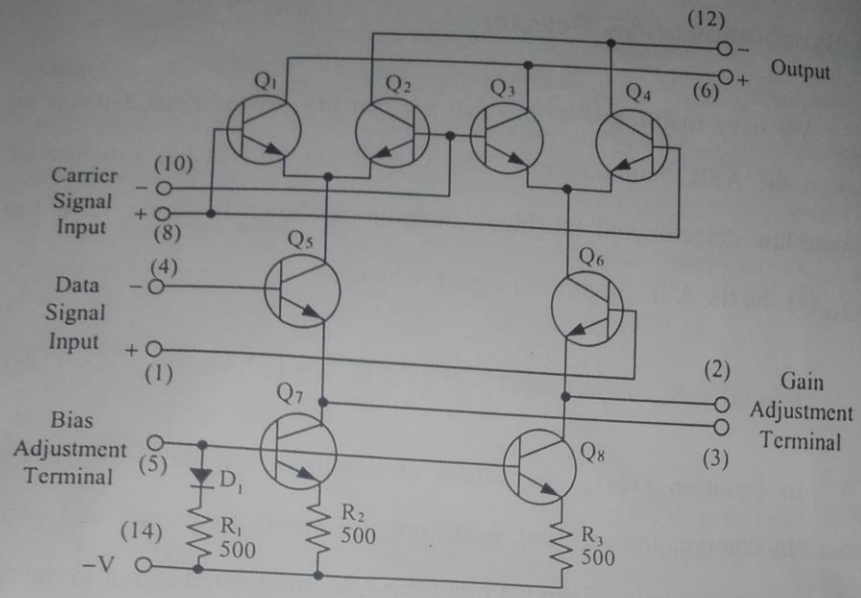


Figure 12-5 Internal circuit diagram of MC1496 balanced modulator.

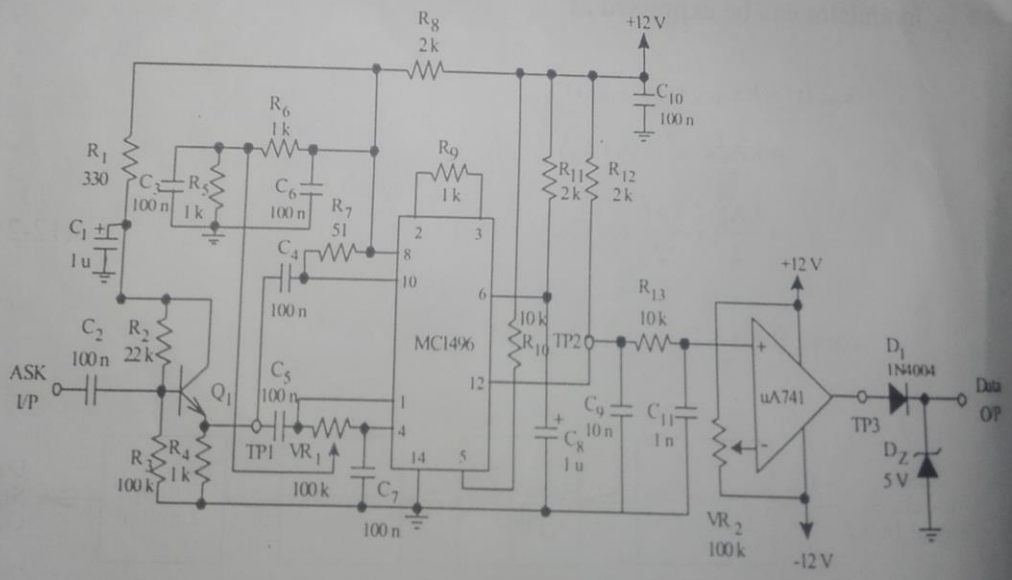


Figure 12-6 Circuit diagram of ASK synchronous detector.

where k represents the gain of balanced modulator. The first term of equation (12-2) is the data signal amplitude and the second term is the 2^{nd} harmonic of the modulated signal. From the output signal $x_{out}(t)$, if the first data signal amplitude receives the demodulated ASK signal, this means that the data signal can be recovered correctly.

In this chapter, we utilize MC1496 balanced modulator to design the square-law detector as shown in figure 12-5. Figure 12-5 is the internal circuit diagram of MC1496 balanced modulator (Readers may refer to the circuit diagram in chapter 11).

Figure 12-6 is the circuit diagram of synchronous ASK detector. In figure 12-6, Q_1, C_1, C_2, R_2, R_3 and R_4 comprise an emitter follower. VR_1 controls the input ranges of modulated ASK signal and the output signal of MC1496 (pin 12) is shown in equation (12-2). The C_9, C_{11} and R_{13} comprise a low-pass filter, which the objective is to remove the 2^{nd} harmonic of modulated ASK signal as shown in the second term in equation (12-2). The first term in the equation (12-2) is the data signal amplitude part, which can be recovered by using the comparator and voltage limiter comprised by μA741, VR_2, D_1 and D_Z.

12-3: Experiment Items

Experiment 1: Asynchronous ASK detector (XR 2206)

1. Use the ASK modulator in chapter 11 with R_1 = 1 kΩ (as shown in figure 11-3) or refer to figure DCS11-1 on ETEK DCS-6000-06 module to produce the amplitude modulated signal as the modulated ASK signal input. Let J2 be short circuit and J3 be open circuit.
2. At the data signal input terminal (Data I/P) in figure DCS11-1, input 5 V amplitude and 100 Hz TTL signal.
3. Connect the ASK signal output terminal (ASK O/P) in figure DCS11-1 to the signal input terminal of the asynchronous ASK detector (ASK I/P) in figure DCS12-1.
4. Adjust the variable resistor VR_1 in figure DCS12-1 to obtain the optimum reference level of the comparator. By using oscilloscope, observe on the output signal waveforms of the negative feedback amplifier (TP1), demodulated signal output port (TP2), comparator reference level (TP3) and the digital signal output port (Data O/P). Finally, record the measured results in table 12-1.
5. According to the input signal in table 12-1, repeat step 2 to step 4 and record the measured results in table 12-1.
6. Use the ASK modulator in chapter 11 with R_1 = 510 Ω (as shown in figure 11-3) or refer to figure DCS11-1 on ETEK DCS-6000-06 module to produce the amplitude modulated signal as the modulated ASK signal input. Let J2 be open circuit and J3 be short circuit.

7. According to the input signal in table 12-2, repeat step 2 to step 4 and record the measured results in table 12-2.

Experiment 2: Asynchronous ASK detector (MC 1496)

1. Use the ASK modulator in chapter 11 (as shown in figure 11-6) or refer to figure DCS11-2 on ETEK DCS-6000-06 module to produce the amplitude modulated signal as the modulated ASK signal input.

2. At the data signal input terminal (Data I/P) in figure DCS11-2, input 5 V amplitude and 100 Hz TTL signal. At the carrier signal input terminal (Carrier I/P), input 400 mV amplitude and 20 kHz sine wave frequency.

3. Adjust VR_1 of ASK modulator in figure DCS11-2 and observe on the modulated ASK signal before the signal occurs distortion, then slightly adjust VR_2 to avoid the asymmetry of the signal to obtain the optimum output waveform of modulated ASK signal (ASK O/P).

4. Connect the ASK signal output terminal (ASK O/P) in figure DCS11-2 to the signal input terminal of the asynchronous ASK detector (ASK I/P) in figure DCS12-1.

5. Adjust the variable resistor VR_1 in figure DCS12-1 to obtain the optimum reference level of the comparator. By using oscilloscope, observe on the output signal waveforms of the negative feedback amplifier (TP1), demodulated signal output port (TP2), comparator reference level (TP3) and the digital signal output port (Data O/P). Finally, record the measured results in table 12-3.

6. According to the input signal in table 12-3, repeat step 3 to step 5 and record the measured results in table 12-3.

7. At the data signal input terminal (Data I/P) in figure DCS11-2, input 5 V amplitude and 100 Hz TTL signal. At the carrier signal input terminal (Carrier I/P), input 400 mV amplitude and 100 kHz sine wave frequency.

8. According to the input signal in table 12-4, repeat step 3 to step 5 and record the measured results in table 12-4.

Experiment 3: Synchronous ASK detector

1. Use the ASK modulator in chapter 11 (as shown in figure 11-6) or refer to figure DCS11-2 on ETEK DCS-6000-06 module to produce the amplitude modulated signal as the modulated ASK signal input.

2. At the data signal input terminal (Data I/P) in figure DCS11-2, input 5 V amplitude and 1 kHz TTL signal. At the carrier signal input terminal (Carrier I/P), input 400 mV amplitude and 100 kHz sine wave frequency.

3. Adjust VR_1 of ASK modulator in figure DCS11-2 and observe on the modulated ASK signal before the signal occurs distortion, then slightly adjust VR_2 to avoid the asymmetry of the signal to obtain the optimum output waveform of modulated ASK signal (ASK O/P).

4. Connect the ASK signal output terminal (ASK O/P) in figure DCS11-2 to the signal input terminal of the asynchronous ASK detector (ASK I/P) in figure DCS12-2.

5. By using oscilloscope and switching to DC channel, then adjust VR_2 of figure DCS12-2 to obtain the optimum comparator reference voltage. Then observe on the output signal waveforms of the emitter follower (TP1), balanced modulator (TP2), comparator (TP3) and data signal output port (Data O/P). Finally, record the measured results in table 12-5. If the signal output waveform occurs distortion, then slightly adjust VR_1.

6. According to the input signal in table 12-5, repeat step 3 to step 5 and record the measured results in table 12-5.

7. At the data signal input terminal (Data I/P) in figure DCS11-2, input 5 V amplitude and 1 kHz TTL signal. At the carrier signal input terminal (Carrier I/P), input 400 mV amplitude and 40 kHz sine wave frequency.

8. According to the input signal in table 12-6, repeat step 3 to step 5 and record the measured results in table 12-6.

12-5: Problems Discussion

1. In figure 12-3, if we neglect the μA741 op-amp and connect the ASK modulator to the diode detector, then what are the results?

2. What are the purposes of the comparators in figure 12-3 and figure 12-6?

3. In figure 12-6, what are the objectives of R_{13}, C_9 and C_{11}?

4. In figure 12-6, what are the objectives of D_1 and D_Z?