



13-1: Curriculum Objectives

1. To understand the operation theory of FSK modulator.
2. To understand the FSK modulation by using the theory of mathematical.
3. To design and implement the FSK modulator by using VCO.

13-2: Curriculum Theory

In digital signal transmission, the repeater is used to recover the data signal, this will enhance the immunity to noise. So the coding technique can be used to detect, correct and encrypt the signal. During long haul transmission, the high frequency part of the digital signal will easily attenuate and cause distortion. Therefore, the signal has to be modulated before transmission, and one of the methods is the frequency-shift keying (FSK) modulation. FSK technique is to modulate the data signal to two different frequencies to achieve effective transmission. At the receiver, the data signal will be recovered based on the two different frequencies of the received signal.

The relation of FSK signal and data signal is shown in figure 13-1.

When the data signal is 5 V, after the signal pass through the buffer, the switch S1 will OFF, then the frequency of FSK signal is f_1 . When the data signal is 0 V, after the signal pass through the buffer, the switch S2 will OFF, the frequency of FSK signal is f_2 . Normally, the difference between frequencies f_1 and f_2 has to be as large as possible. This is because the correlation of both signals is low, therefore, the effect of transmitting and receiving will be better. However, the required bandwidth must be increased.

Figure 13-2 is the signal waveforms of FSK modulation.

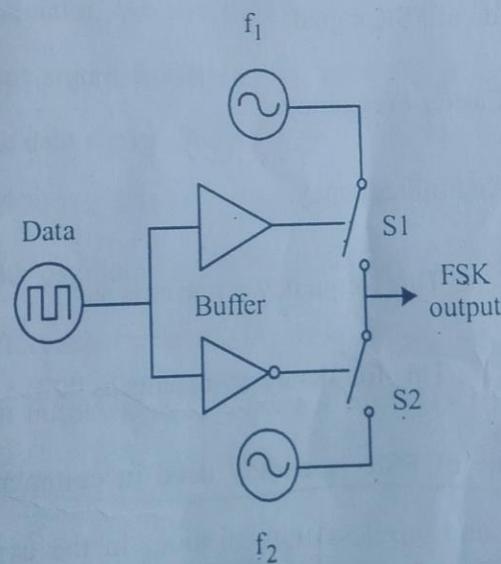


Figure 13-1 Structure diagram of FSK modulator.

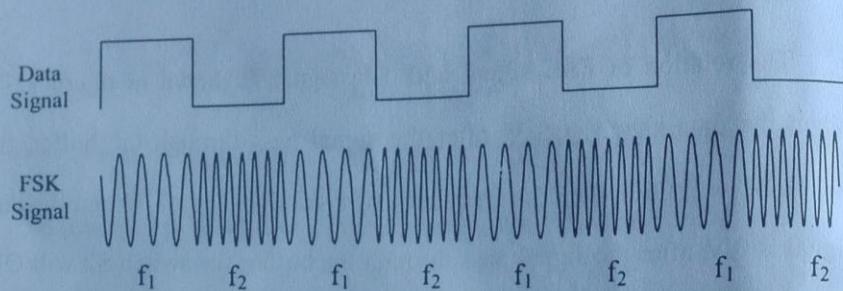


Figure 13-2 Relation diagram between data signal and FSK signal.

In this section, we utilize the theory of mathematic to solve the FSK modulation as shown in equation (13-1). The expression are as follow

$$\begin{aligned} V_{FSK} &= A \cos(\omega_C)t \times \cos(\omega_D)t \\ &= \frac{A}{2} [\cos(\omega_C + \omega_D)t + \cos(\omega_C - \omega_D)t] \end{aligned} \quad (13-1)$$

A: Magnitude of FSK signal.

$\cos(\omega_C)t$: Carrier Frequency.

$\cos(\omega_D)t$: Audio Frequency.

$\cos(\omega_C + \omega_D)t$: This frequency represents as "1".

$\cos(\omega_C - \omega_D)t$: This frequency represents as "0".

The technique of FSK is widely used in commercial and industrial wire transmission and wireless transmission. In the experiments, we will discuss how to produce FSK signal. In certain applications, the FSK signal is fixed. For example, for wireless transmission, the mark signal is 2124 Hz

and space signal is 2975 Hz. For wire transmission such as telephone, the frequencies are as follow

$$\text{Space} = 1370 \text{ Hz}$$

$$\text{Mark} = 870 \text{ Hz}$$

or

$$\text{Space} = 2225 \text{ Hz}$$

$$\text{Mark} = 2025 \text{ Hz}$$

From the above mentioned, we notice that the frequency gap of FSK is 500 Hz.

In FSK modulator, we use data signal (square wave) as the signal source. The output signal frequency of modulator is based on the square wave levels of the data signal. In this chapter, the frequencies of the carriers are 870 Hz and 1370 Hz. These two frequencies can be produced by using a voltage controlled oscillator, (VCO). The output signal frequencies are varied by the difference levels of the input pulse to produce two different frequencies. Each output signal frequency corresponds to an input voltage level (i.e. "0" or "1").

In this chapter, we utilize 2206 IC waveform generator and LM 566 voltage controlled oscillator to produce the modulated FSK signal. First of all lets introduce the characteristics of 2206 IC. 2206 IC is a waveform



generator, which is similar to 8038 IC. Figure 13-3 is the circuit diagram of the FSK modulator by using 2206 IC. In figure 13-3, resistors R₃, R₄ comprise a voltage divided circuit. The main function of the voltage divided circuit is to let the negative voltage waveform of the 2206 IC operates normally. The oscillation frequency of 2206 IC is determined by resistors R₁ and R₅. Its oscillation frequencies are $f_1 = 1/2\pi R_1 C$, $f_2 = 1/2\pi R_5 C$. There is an internal comparator in 2206 IC. Assume that when the input is 5 V, the output frequency is f₁, and when the input is 0 V, the output frequency is f₂. We can utilize the TTL signal at pin 9 to control the output frequency to be f₁ or f₂. This type of structure is similar to the structure in figure 13-1. Therefore, by using the characteristic of this structure, we can achieve FSK modulation easily.

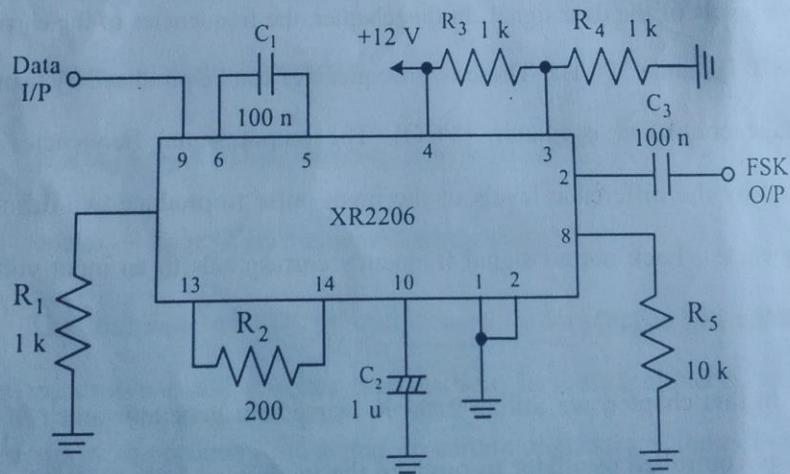


Figure 13-3 Circuit diagram of FSK modulator by using 2206 IC.

Next, we use LM566 voltage control oscillator to implement the FSK modulator. First of all, we will discuss the varactor diode. Varactor diode or tuning diode is mainly used for changing the capacitance value of oscillator. The objective is to let the output frequency of oscillator can be adjusted or tunable, therefore varactor diode dominates the tunable range of the whole voltage controlled oscillator.

Varactor diode is a diode, which its capacitance can be varied by adding a reverse bias to pn junction. When reverse bias increases, the depletion region become wide, this will cause the capacitance value decreases; nevertheless when reverse bias decreases, the depletion region will be reduced, this will cause the capacitance value increases. Varactor diode also can be varied from the amplitude of AC signal.

Figure 13-4 is the capacitance analog diagram of varactor diode. When a varactor diode without bias, the concentration will be differed from minor carriers at pn junction. Then these carriers will diffuse and become depletion region. The p type depletion region carries electron positive ions, then the n type depletion region carries negative ions. We can use parallel plate capacitor to obtain the expression as shown as follow:

$$C = \frac{\epsilon A}{d} \quad (13-2)$$

where

$$\epsilon = 11.8 \epsilon_0 \text{ (dielectric constant of Silicon)}$$

$$\epsilon_0 = 8.85 \times 10^{-12}$$

A: the cross section area of capacitor.

d: the width of depletion region.

When reverse bias increases, the width of depletion region d will increase but the cross section area A remains, therefore the capacitance value would be reduced. On the other hand, the capacitance value will increase when reverse bias decreases.

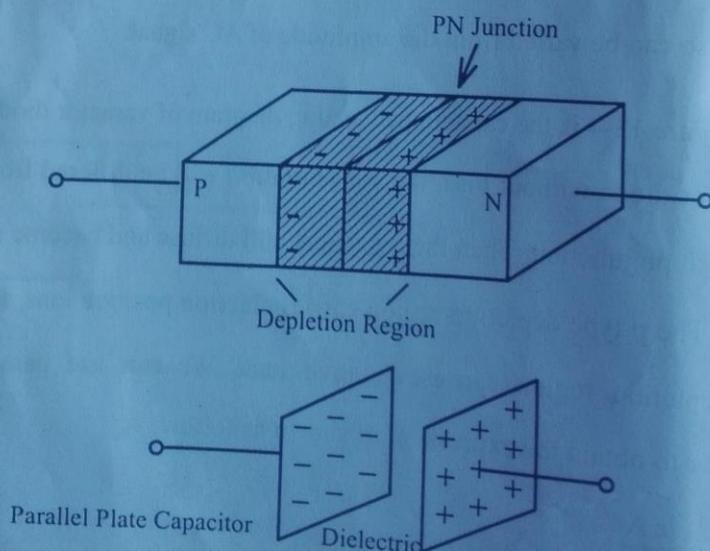


Figure 13-4 Capacitance analog diagram of varactor diode.

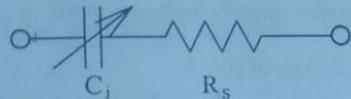


Figure 13-5 Equivalent circuit diagram varactor diode.

Varactor diode can be equivalent to a capacitor series a resistor as shown in figure 13-5. From figure 13-5, C_j is the junction capacitor of semiconductor, which only exists in pn junction. R_s is the sum of bulk resistance and contact resistance of semiconductor material, which is related to the quality of varactor diode (generally below a few ohm).

Tuning ratio, TR is the ratio of capacitance value under two different biases for varactor diode. The expression is shown as follow:

$$TR = \frac{C_{V_2}}{C_{V_1}} \quad (13-3)$$

where

TR: tuning ratio.

C_{V_1} : capacitance value of varactor diode at V_1 .

C_{V_2} : capacitance value of varactor diode at V_2 .

The oscillation frequency of LM566 is

$$f_0 = \frac{2}{R_{10}C_5} \left(\frac{V_{cc} - V_{in}}{V_{cc}} \right) \quad (13-4)$$

Where V_{cc} is the power supply voltage input at pin 8 of LM566. V_{in} is the input voltage of LM566 at pin 5.

If V_{cc} is fixed, then with proper R_{10} , C_5 and V_{in} , the output signal frequencies (f_o) of LM566 will be 1072 Hz and 1272 Hz. The conditions for using LM566 VCO are as follow

$$2 \text{ k}\Omega \leq R_{10} \leq 20 \text{ k}\Omega$$

$$0.75 \leq V_{in} \leq V_{cc}$$

$$f_o \leq 500 \text{ kHz}$$

$$10 \text{ V} \leq V_{cc} \leq 24 \text{ V}$$

Figure 13-6 is the circuit diagram of FSK modulator. The operation theory is to convert the voltage level of data signal (TTL levels) to appropriate voltage level. This voltage will input to the input terminal of LM566 VCO. Then, the VCO will produce two frequencies with respect to the input voltage levels (870Hz and 1370Hz). The Q_1 , Q_2 , R_1 , R_2 , R_3 , VR_1 and VR_2 comprise a voltage converter. In the circuit, Q_1 will operate as NOT gate. When the input signal of the base of Q_1 is high, then Q_1 will switch on. At this moment, the output signal of the collector will be low (around 0.2 V), so Q_2 will switch off. When input signal of the base of Q_1 is low (0 V), Q_1 will switch off. At this moment, the output signal of collector of Q_1 is high

(5 V), so, Q_2 will switch on. When Q_2 switch off, the input voltage of VCO is

$$V_1 = \frac{VR_2}{VR_2 + R_6} V_{cc} \quad (13-5)$$

The VCO output signal frequency is f_1 . When Q_2 switches on, the input voltage of VCO is (assume the resistance of Q_2 is only a few ohm)

$$V_2 = \frac{VR_1 // VR_2}{(VR_1 // VR_2) + R_6} V_{cc} \quad (13-6)$$

At this moment, the output signal frequency of VCO is f_2 . So, we just need to adjust VR_1 and VR_2 , then the output signal frequencies of VCO will become f_1 and f_2 which are 1370 Hz and 870 Hz, respectively. In figure 13-6, the two μ A741, R_5 , R_6 , R_7 , R_8 , R_9 , R_{10} , C_3 , C_4 , C_5 and C_6 comprise a 4th order low-pass filter. The objective is to remove the unwanted signal from the LM566 VCO output (TP2), so that we can obtain the sinusoidal waveform signal.

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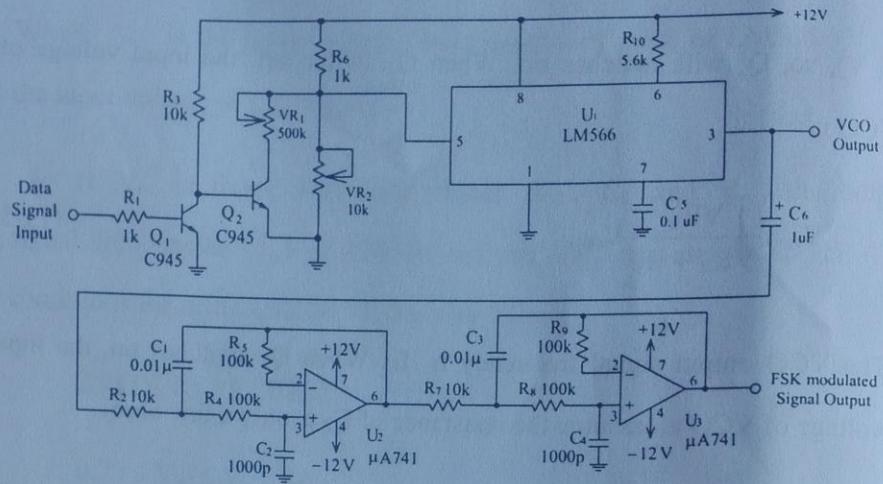


Figure 13-6 Circuit diagram of FSK modulator.

13-3: Experiment Items

Experiment 1: XR 2206 FSK modulator

1. Refer to figure 13-3 with $R_1 = 1 \text{ k}\Omega$ and $R_S = 10 \text{ k}\Omega$ or refer to figure DCS13-1 on ETEK DCS-6000-07 module. Let J2 and J4 be short circuit, J3 and J5 be open circuit.
2. From figure DCS13-1, let the two terminal of I/P be short circuit and JP1 be open circuit, i.e. at the data signal input terminal (Data I/P), input 0 V DC voltage. By using oscilloscope, observe on the output signal waveform of FSK signal (FSK O/P), then record the measured results in table 13-1.
3. From figure DCS13-1, let the two terminal of I/P be open circuit and JP1 be short circuit, i.e. at the data signal input terminal (Data I/P), input 5 V DC voltage. By using oscilloscope, observe on the output signal waveform of FSK signal (FSK O/P), then record the measured results in table 13-1.
4. At the data signal input terminal (Data I/P), input 5 V amplitude, 100 Hz TTL signal. By using oscilloscope, observe on the output signal waveform of FSK signal (FSK O/P), then record the measured results in table 13-1.
5. According to the input signal in table 13-1, repeat step 4 and record the measured results in table 13-1.



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6. Refer to figure 13-3 with $R_1 = 7.5 \text{ k}\Omega$ and $R_5 = 15 \text{ k}\Omega$ or refer to figure DCS13-1 on ETEK DCS-6000-07 module. Let J2 and J4 be open circuit, J3 and J5 be short circuit.
7. According to the input signal in table 13-2, repeat step 2 to step 4 and record the measured results in table 13-2.

Experiment 2: LM566 FSK modulator

1. Refer to the circuit diagram in figure 13-6 or figure DCS13-2 on ETEK DCS-6000-07 module.
2. From figure DCS13-2, let the two terminal of I/P be short circuit and JP1 be open circuit, i.e. at the data signal input terminal (Data I/P), input 0 V DC voltage. By using oscilloscope, observe on the output signal waveform of the VCO output port (TP2) of LM 566. Slightly adjust VR₂ so that the frequency of TP2 is 1370 Hz. Again observe on the output signal waveforms of the charge and discharge test point (TP1), second order low-pass filter (TP3) and FSK signal output port (FSK O/P). Finally, record the measured results in table 13-3.
3. From figure DCS13-2, let the two terminal of I/P be open circuit and JP1 be short circuit, i.e. at the data signal input terminal (Data I/P), input 5 V DC voltage. By using oscilloscope, observe on the output signal waveform of the VCO output port (TP2) of LM 566. Slightly adjust VR₂ so that the frequency of TP2 is 870 Hz. Again observe on TP1, TP3 and FSK O/P. Finally, record the measured results in table 13-3.
4. At the data signal input terminal (Data I/P), input 5V amplitude and 200 Hz TTL signal. By using oscilloscope, observe on the output signal waveforms of Data I/P, TP1, TP2, TP3, and FSK O/P. Finally, record the measured results in table 13-4.
5. According to the input signal in table 13-4, repeat step 4 and record the measured results in table 13-4.



13-5: Problems Discussion

1. In figure 13-6, what are the functions of Q_1 , Q_2 and LM566?
2. In figure 13-6, what are the functions of variable resistors VR_1 and VR_2 ?
3. In figure 13-6, if the input signal is larger than the FSK frequency, will this circuit operate properly? (i.e. compare the 200 Hz and 900 Hz input signals in table 13-3)

Chapter 14

FSK Demodulator

14-1: Curriculum Objectives

1. To understand the operation theory of FSK demodulator.
2. To implement the FSK detector circuit by using PLL.
3. To understand the operation theory of comparator by using operational amplifier as voltage level converter.

14-2: Curriculum Theory

In chapter 13 we use FSK modulator for long distance communication, which the voltage level of digital signal has been converted to frequency. Therefore, at the receiver, we have to recover the FSK signal to digital signal, that means the frequency should be converted back to voltage. We use phase locked loop (PLL) as FSK demodulator. PLL is a kind of automatic tracking system, which is able to detect the input signal frequency and phase. PLL is widely used in wireless applications, such as AM demodulator, FM demodulator, frequency selector and so on. In the digital communications, various types of digital PLLs are developed. Digital PLL is very useful in carrier synchronization, bit synchronization and digital demodulation.

1. Asynchronous FSK detector

The block diagram of asynchronous FSK detector is shown in figure 14-1. In figure 14-1, we can see that at the receiver parts, there are two low-pass filters, which their center frequencies are $\omega_C + \omega_D$ and $\omega_C - \omega_D$, respectively. By using the characteristics of the filter, we can obtain the $\omega_C + \omega_D$ (digital signal represents as 1) and $\omega_C - \omega_D$ (digital signal represent as 0): Then combine the digital signal after demodulation, finally, the original digital signal can be obtain at the output terminal. Since the fixed frequency deviation of the carrier signal (ω_C) is quite small, therefore, the usage of sharp filter is its disadvantage.

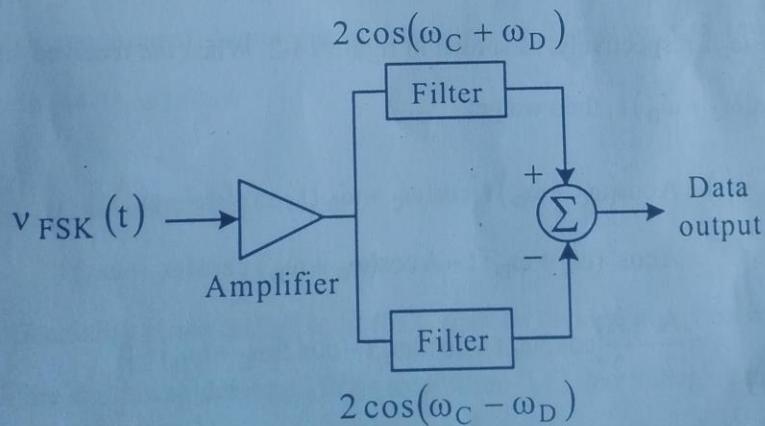


Figure 14-1 Block diagram of asynchronous FSK detector.

2. Synchronous FSK Detector

Let the received data signal $v_{FSK}(t)$ multiply by local oscillation (LO) signals $\cos(\omega_C + \omega_D)t$ or $\cos(\omega_C - \omega_D)t$ as shown in equations (14-1) and (14-3). Then we can obtain $\cos[2(\omega_C + \omega_D)]t$, which the digital signal frequency is represented as 1 or $\cos[2(\omega_C - \omega_D)]t$, which the digital signal frequency is represented as 0. After that by using the filter to remove the second order harmonics and DC voltage, then we can obtain the original digital signal as shown in figure 14-2.

In this section, we utilize the theory of mathematic to solve the FSK demodulation as shown in equation (14-1). The synchronous FSK detector needs two LO oscillators, which the LO frequencies are $\omega_C - \omega_D$ and $\omega_C + \omega_D$, respectively, as shown in figure 14-2. When the received signal is $A \cos(\omega_C + \omega_D)t$, then we get

$$\begin{aligned}
 v(t) &= A \cos(\omega_C + \omega_D)t [\cos(\omega_C + \omega_D)t - \cos(\omega_C - \omega_D)t] \\
 &= A \cos^2(\omega_C + \omega_D)t - A \cos(\omega_C + \omega_D)t \cos(\omega_C - \omega_D)t \\
 &= \frac{A}{2} - \frac{A}{2} [\cos 2\omega_C t + \cos 2\omega_D t - \cos 2(\omega_C + \omega_D)t]
 \end{aligned} \tag{14-1}$$

By using a filter to remove all the unwanted signal in equation (14-1), then the represented output signal frequency is 1 and we can rewritten equation (14-1) as follow

$$v_1(t) = \frac{A}{2} \cos[2(\omega_C + \omega_D)t] \quad (14-2)$$

ω_C : Carrier frequency.

ω_D : Signal frequency.

When the received signal is $A \cos(\omega_C - \omega_D)t$, then we get

$$\begin{aligned} v(t) &= A \cos(\omega_C + \omega_D)t [-\cos(\omega_C + \omega_D)t + \cos(\omega_C - \omega_D)t] \\ &= -A \cos^2(\omega_C + \omega_D)t + A \cos(\omega_C + \omega_D)t \cos(\omega_C - \omega_D)t \\ &= -\frac{A}{2} + \frac{A}{2} [\cos 2\omega_C t + \cos 2\omega_D t - \cos 2(\omega_C + \omega_D)t] \end{aligned} \quad (14-3)$$

By using a filter to remove all the unwanted signal in equation (14-3), then the represented output signal frequency is 0 and we can rewritten equation (14-1) as follow

$$v_2(t) = \frac{A}{2} \cos[2(\omega_C - \omega_D)t] \quad (14-4)$$

Generally, phase locked loop (PLL) can be divided into 3 main parts, which are the phase detector (PD), loop filter (LF) and voltage controlled oscillator (VCO). The block diagram of PLL is shown in figure 14-3.

In figure 14-3, when the input signal frequency changes, the output signal of the phase detector will change and so as well as the output

voltage. We can use this characteristic to design the FSK demodulator. Let the FSK signal frequencies as f_1 and f_2 . Then these signals are inputted to the input terminal of figure 14-3. When the signal frequency is f_1 , the output voltage will be V_1 . When the input signal frequency is f_2 , the output voltage is V_2 . At this moment, we have converted the frequency to voltage. If we add a comparator at the output terminal of PLL, the reference voltage will lie between V_1 and V_2 , then at the output terminal of comparator, we are able to obtain the digital signal, which is the demodulated FSK signal.

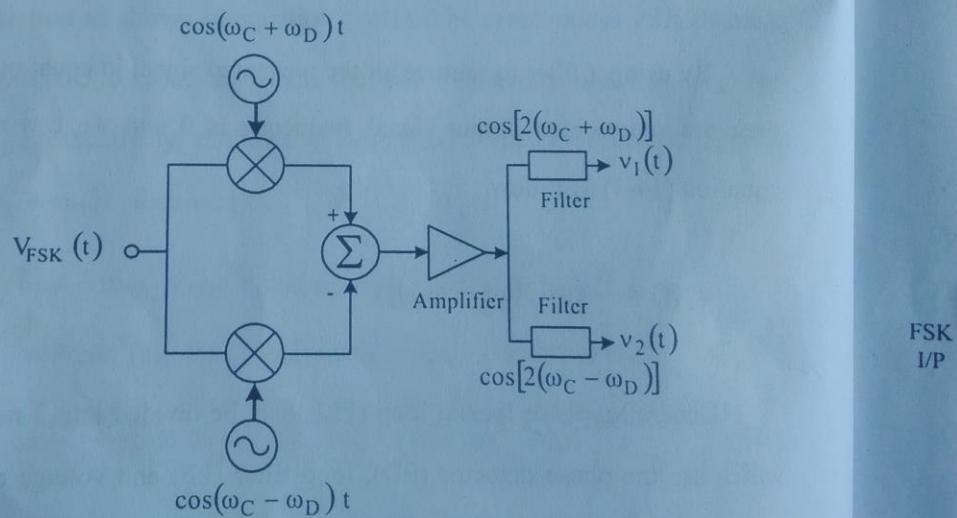


Figure 14-2 Block diagram of synchronous FSK detector.

In this experiment, we implement the FSK demodulator by using LM565 PLL as shown in figure 14-4. The operation frequency of LM565 PLL is below 500 kHz and the internal circuit diagram is shown in figure 14-4. It includes phase detector, voltage controlled oscillator and amplifier. The phase detector is a double-balanced modulator type circuit and the VCO is integrated Schmitt circuit.

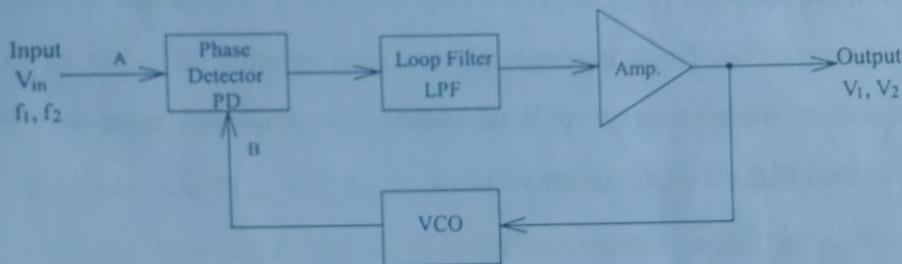


Figure 14-3 Block diagram of PLL.

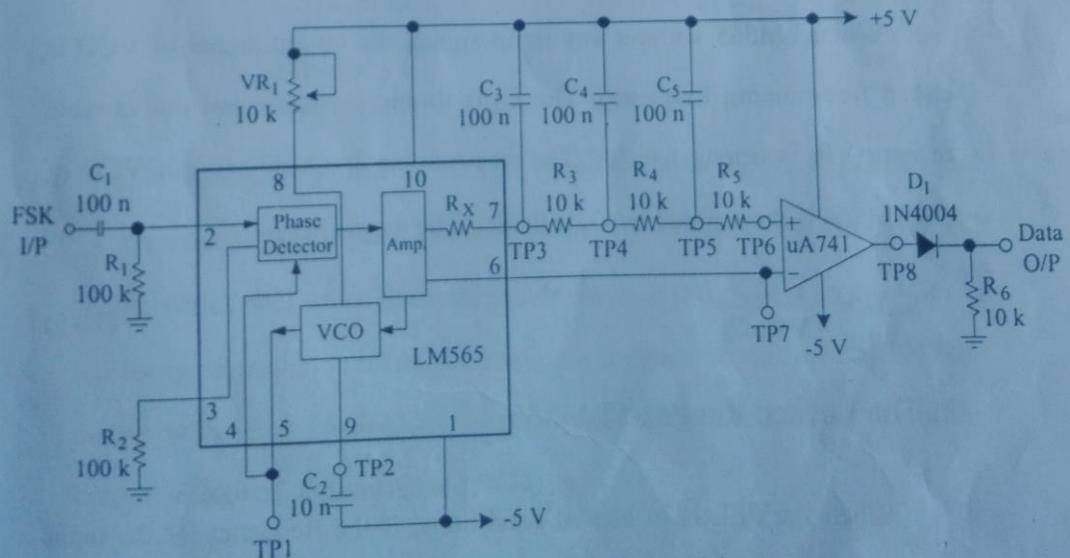


Figure 14-4 Circuit diagram of FSK demodulator.

Pin 1 is connected to negative voltage supply, -5 V. Pins 2 and 3 are connected to the input signals, but normally pin 3 will connect to ground. If pins 4 and 5 are connected to frequency multiplier, then various multiplications of frequencies can be obtained. In this experiment, we need not use the frequency multiplier, therefore, these two pins are shorted. Pin 6 is the reference voltage output. The internal resistor (R_x) of pin 7 and the external capacitor (C_3) comprise a loop filter. Pin 8 is connected to timing resistor (VR_1). Pin 9 is connected to timing capacitor (C_2). Pin 10 the positive voltage supply +5 V of LM565. The important parameters of LM565 PLL circuit design are as below

1) The Free-Running Frequency of LM565

When LM565 without any input signal, the output signal of VCO is called free-running frequency. The C_2 is timing capacitor and the variable resistor VR_1 is timing resistor. The free-running frequency (f_o) of VCO of the LM565 is determined by C_2 and VR_1 . The expression is

$$f_o \approx \frac{1.2}{4 VR_1 C_2} \quad (14-5)$$

2) The Locked Range of LM565

When the PLL is in locked conditions, if the frequency of the input signal (f_i) deviates from f_o , then the PLL will remain in the locked

condition. When f_i reaches a certain frequency, which the PLL is not able to lock, then the difference between f_i and f_o is called the locked range.

The locked range of LM565 can be expressed as

$$f_L = \frac{8f_o}{V_c} = \frac{8f_o}{V_{cc} - V_{EE}} \quad (14-6)$$

3) The Captured Range of LM565

The initial mode of PLL is in unlocked condition, then the frequency of the input signal (f_i) will come near to f_o . When f_i reaches a certain frequency, the PLL will be in locked condition. At this moment, the difference between f_i and f_o is called the captured range. The captured range of LM565 can be expressed as

$$f_C = \frac{1}{2\pi} \sqrt{\frac{2\pi \times f_L}{3.6 \times 10^3 \times C_2}} \quad (14-7)$$

In figure 14-4, pin 7 of LM565 is connected to R_3 , R_4 , R_5 , C_3 , C_4 and C_5 to comprise a low-pass filter. The objective is to remove the unwanted signal, which will cause the comparator produce incorrect action. $\mu A741$ is the comparator and its reference voltage is inputted at pin 6 of LM565. The output voltage of LM565 will pass through $\mu A741$ and D_1 to obtain the output voltage of digital signal of TTL level.



14-3: Experiment Items

5.

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Experiment 1: XR2206 FSK demodulator

1. Refer to the circuit diagram in figure 14-4 or figure DCS14-1 on ETEK DCS-6000-07 module. Without adding any signal at the input terminal (FSK I/P), then by using oscilloscope, observe on the VCO output (TP1) of LM565, adjust variable resistor VR_1 so that the free-running frequency of LM565 operates at 1170 Hz.
2. At the input terminal (FSK I/P) of figure DCS14-1, input 4 V amplitude and 870 Hz sine wave frequency. By using oscilloscope and switching to DC channel, then observe on the output signal waveform of FSK I/P, TP1, charge and discharge test point (TP2), low-pass loop circuit 1 (TP3), low-pass loop circuit 2 (TP4), low-pass loop circuit 3 (TP5), low-pass loop circuit 4 (TP6), reference voltage of the comparator (TP7), output terminal of the comparator (TP8) and data signal output port (Data O/P). Finally, record the measured results in table 14-1.
3. At the input terminal (FSK I/P) of figure DCS14-1, input 4 V amplitude and 1370 Hz sine wave frequency. Repeat step 2 and record the measured results in table 14-2.
4. Refer to figure 13-3 with $R_1 = 7.5 \text{ k}\Omega$ and $R_5 = 15 \text{ k}\Omega$ or refer to figure DCS13-1 on ETEK DCS-6000-07 module. Let J2 and J4 be open circuit, J3 and J5 be short circuit.

5. Without adding any signal at the input terminal (FSK I/P) of figure DCS14-1, then by using oscilloscope, observe on the VCO output (TP1) of LM565, adjust variable resistor VR₁ so that the free-running frequency of LM565 operates at 1170 Hz.
6. At the data signal input terminal (Data I/P) of figure DCS13-1, input 5 V amplitude, 150 Hz TTL signal.
7. Connect the modulated FSK signal (FSK O/P) of figure DCS13-1 to the input terminal (FSK I/P) of figure DCS14-1. By using oscilloscope, observe on the output signal waveforms of TP1, TP2, TP3, TP4, TP5, TP6 and Data O/P. Finally record the measured results in table 14-3.
8. According to the input signal in table 14-3, repeat step 6 to step 7 and record the measured results in table 14-3.

Experiment 2: LM 565 FSK demodulator

1. Refer to the circuit diagram in figure 13-6 or figure DCS13-2 on ETEK DCS-6000-07 module.
2. From figure DCS13-2, let the data signal input terminal (Data I/P) be short circuit and J1 be open circuit, i.e. input 0 V DC voltage to the data signal input terminal (Data I/P). By using oscilloscope, observe on the output signal waveform of the VCO output port (TP1) of LM 566. Slightly adjust VR₁ so that the output frequency of TP1 is 1370 Hz. Again let the data signal input terminal (Data I/P) be open circuit and J1 be short circuit, i.e. input 5 V DC voltage to the data signal input terminal (Data I/P). By using oscilloscope, observe on the output signal waveform of the VCO output port (TP1) of LM 566. Slightly adjust VR₁ so that the output frequency of TP1 is 870 Hz.
3. Without adding any signal at the input terminal (FSK I/P) of figure DCS14-1, then by using oscilloscope, observe on the VCO output (TP1) of LM565, adjust variable resistor VR₁ so that the free-running frequency of LM565 operates at 1170 Hz.
4. At the data signal input terminal (Data I/P) of figure DCS13-1, input 5 V amplitude, 150 Hz TTL signal. Connect the modulated FSK signal (FSK O/P) of figure DCS13-2 to the input terminal (FSK I/P) of figure DCS14-1. By using oscilloscope and switching to DC channel, observe on the output signal waveforms of FSK I/P, TP1, TP2, TP3, TP4, TP5, TP6 and Data O/P. Finally record the measured results in table 14-4.
5. According to the input signal in table 14-4, repeat step 4 and record the measured results in table 14-4.

14-5: Problems Discussion

1. In figure 14-4, what are the factors that determine the free-running frequency of LM565 PLL?
2. In figure 14-4, what are the purposes of μ A741?
3. In figure 14-4, what are the functions of pin 6 of LM565?
4. Why the output signal of LM565 must pass through the multi-stages low-pass filter, and then connects to comparator?