I2C-BUS / Summary

Two bus lines: **SDA** (serial data) and **SCL** (serial clock); Low is dominant

Data detection

Data on SDA must be stable during SCL==HIGH. This defines the bit value. During SCL==LOW, SDA may change (Abbildung 1).

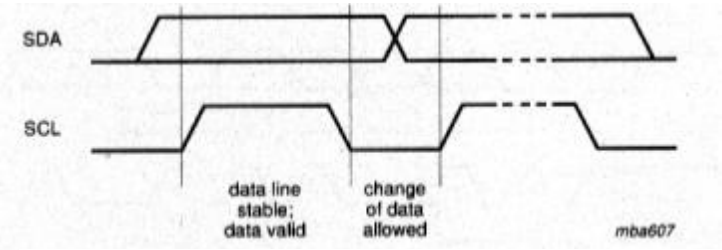


Abbildung 1: Data detection

START / STOP conditions

START condition: SCL==HIGH and SDA HIGH → LOW

STOP condition: SCL==HIGH and SDA LOW → HIGH

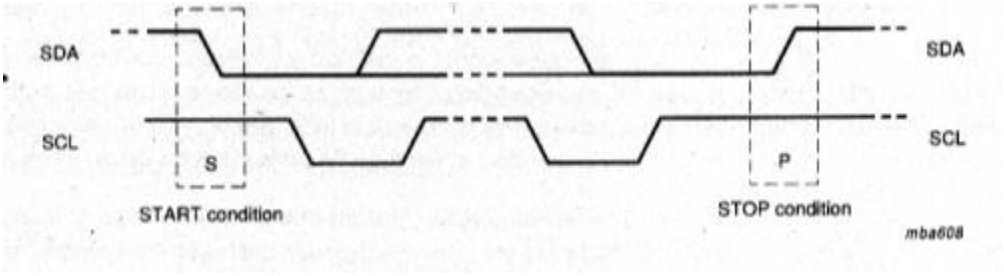


Abbildung 2: START / STOP conditions

Data transfer diagram

The diagram in Abbildung 3 shows the signal in both lines during data transfer

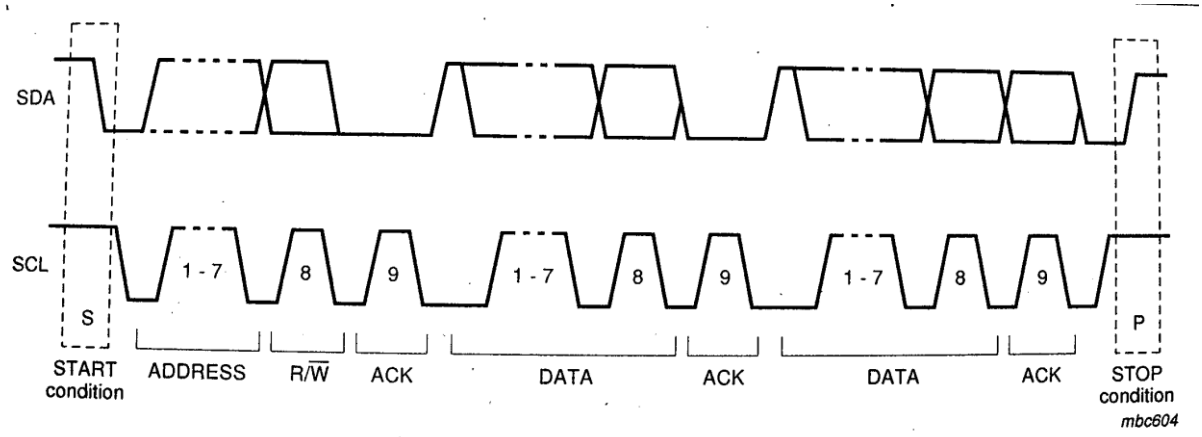
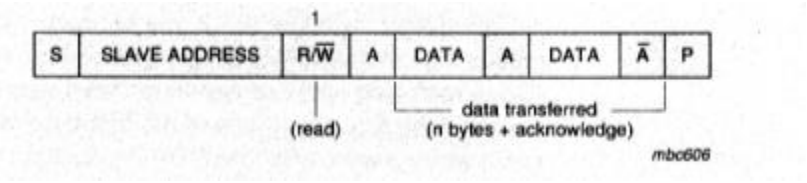


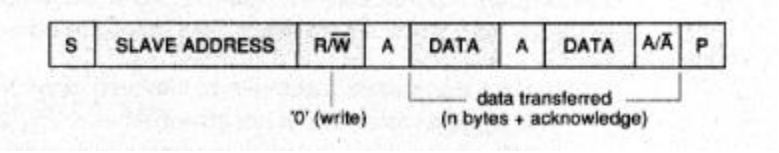
Abbildung 3: Data transfer

Possibilities of data transfer

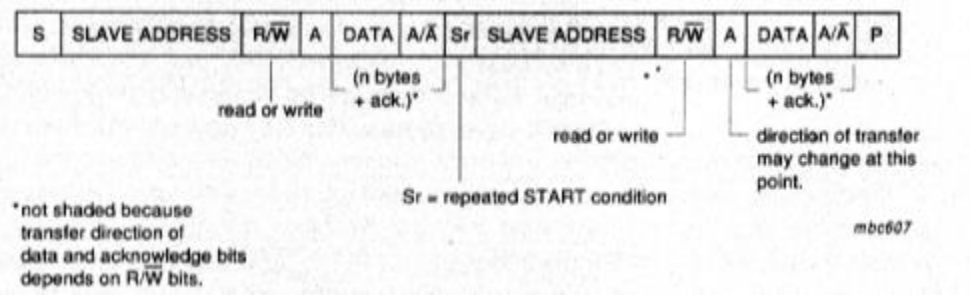
1. Master addressing slave and sending to slave



2. Master addressing slave and reading from slave



3. Combination of both by a "repeated start condition" instead of a stop + start



Master read or write continuously from Slave until STOP conditions is set.