I2C-BUS / Summary

Two bus lines: **SDA** (serial data) and **SCL** (serial clock); Low is dominant

Data detection

Data on SDA must be stable during SCL==HIGH. This defines the bit value. During SCL==LOW, SDA may change (Abbildung 1).

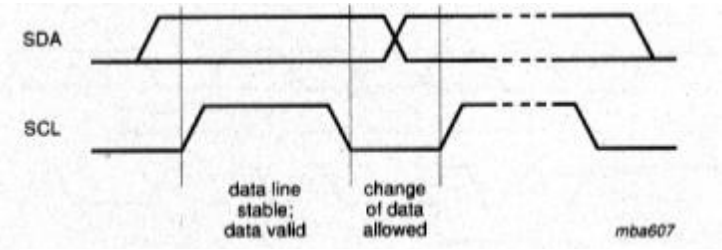


Abbildung 1: Data detection

START / STOP conditions

START condition: SCL==HIGH and SDA HIGH → LOW

STOP condition: SCL==HIGH and SDA LOW → HIGH

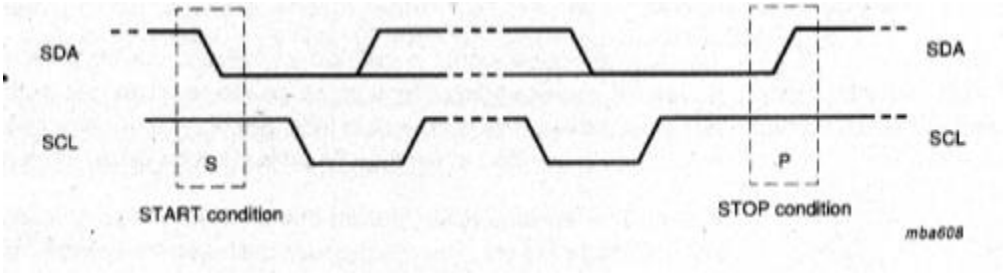
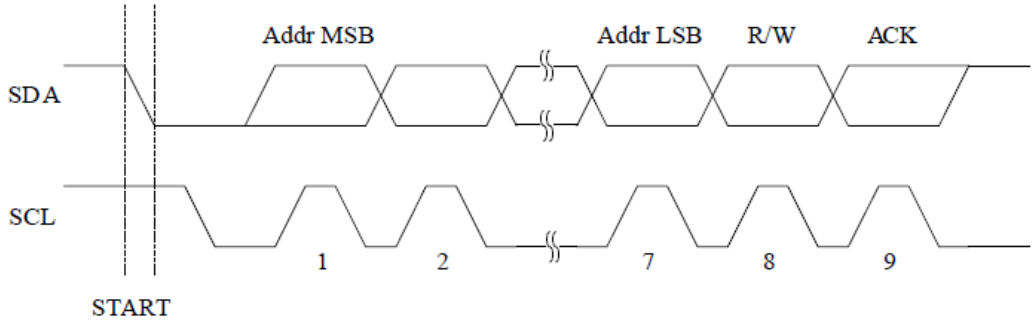


Abbildung 2: START / STOP conditions

Address Packet Format

All address packets transmitted on the TWI bus are 9 bits long, consisting of 7 address bits, one READ/WRITE control bit and an acknowledge bit. When a Slave recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

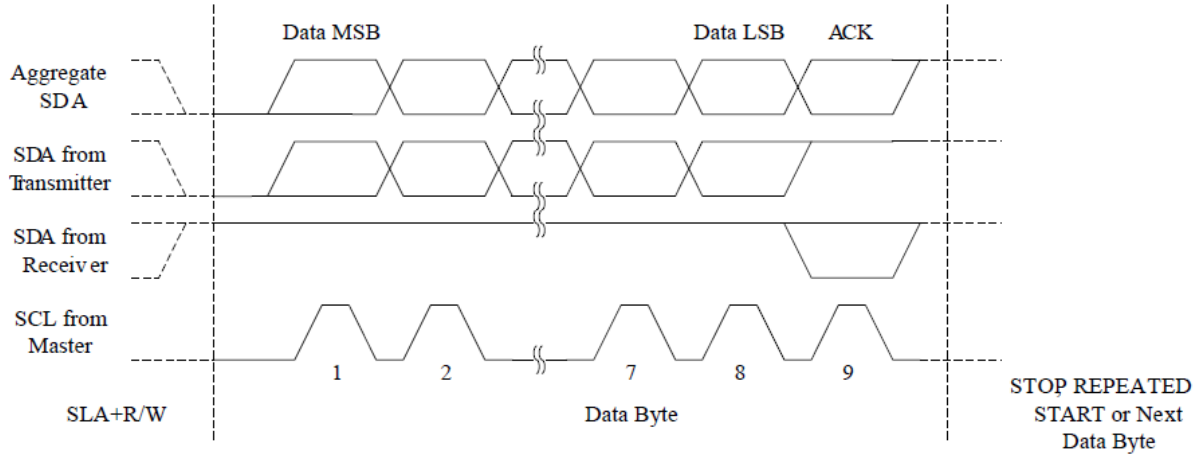
Figure 26-4. Address Packet Format



Data Packet Format

All data packets transmitted on the TWI bus are nine bits long, consisting of one data byte and an acknowledge bit. During a data transfer, the Master generates the clock and the START and STOP conditions, while the Receiver is responsible for acknowledging the reception. An Acknowledge (ACK) is signalled by the Receiver pulling the SDA line low during the ninth SCL cycle.

Figure 26-5. Data Packet Format



Data transfer diagram

The diagram in Abbildung 3 shows the signal in both lines during data transfer

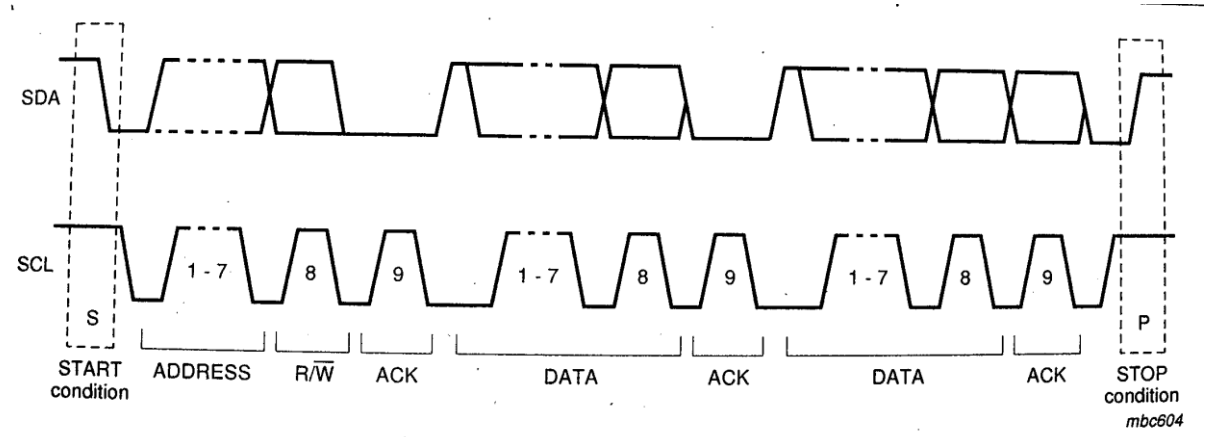
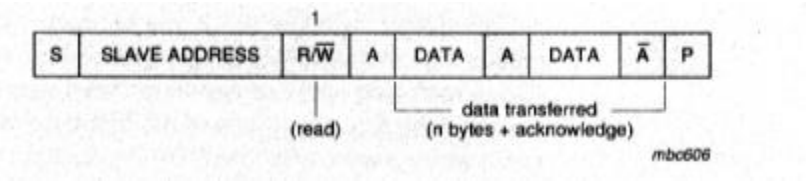


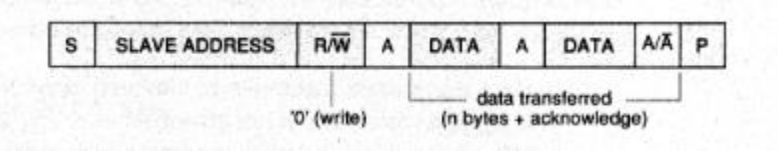
Abbildung 3: Data transfer

Possibilities of data transfer

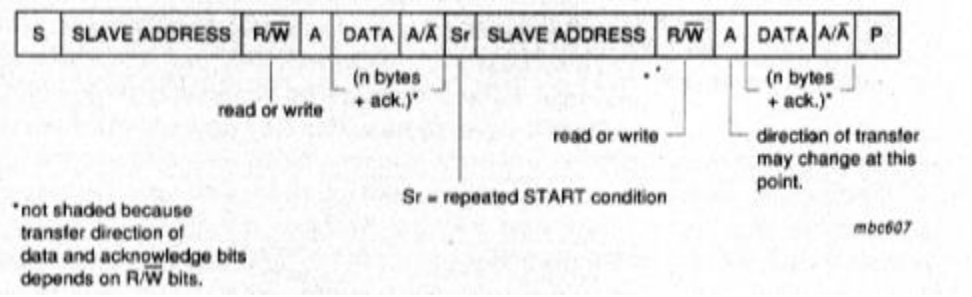
1. Master addressing slave and sending to slave



2. Master addressing slave and reading from slave



3. Combination of both by a "repeated start condition" instead of a stop + start



Master read or write continuously from Slave until STOP conditions is set.