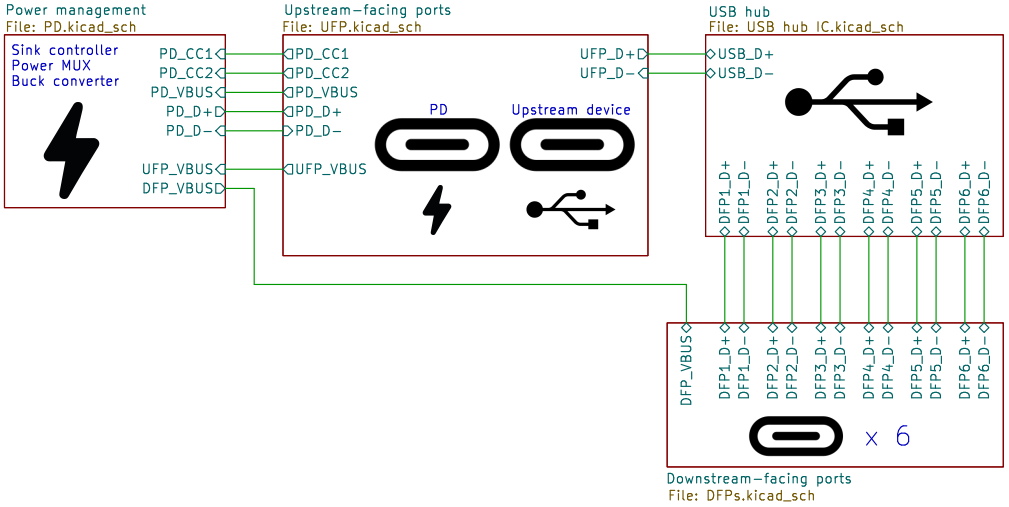

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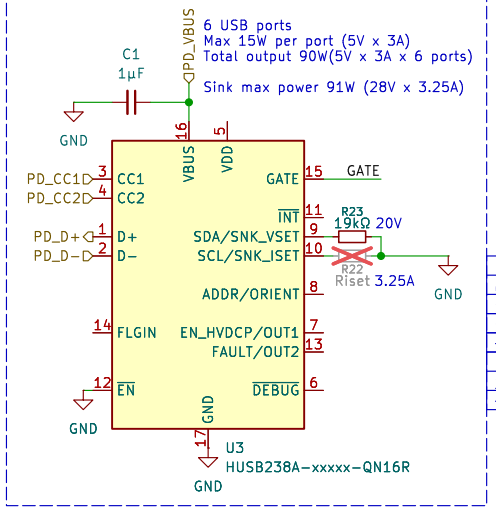
Sheet: /
File: Multiport USB−C 2.0 hub.kicad_sch

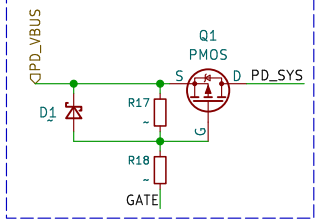
Title: Multiport USB−C 2.0 hub

Size: A4	Date: 2025−12−10	**Rev: R1**
KiCad E.D.A. 9.0.3		Id: 1/5

PD Sink Controller

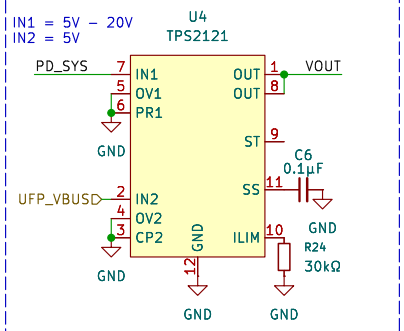


PD VBUS Switching



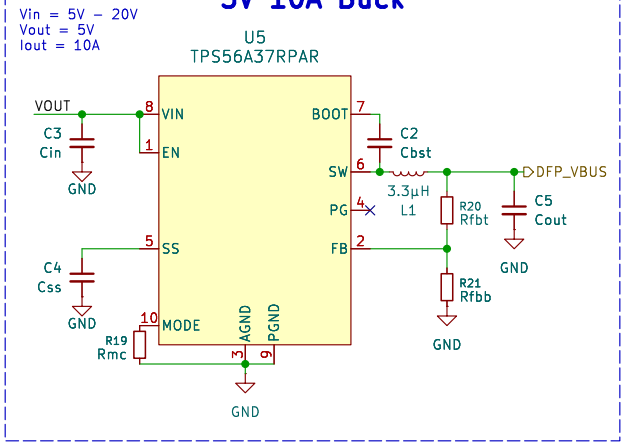
R_VSET kΩ	Voltage
6	12V
11	15V
19	20V
float	28V
R_ISET kΩ	**Amperage**
21	3A
float	3.25A

Power MUX



TODO:
confirm ILIM value (3.25A)
confirm priority
confirm OVP

5V 10A Buck



TYPICAL APPLICATION CIRCUITS

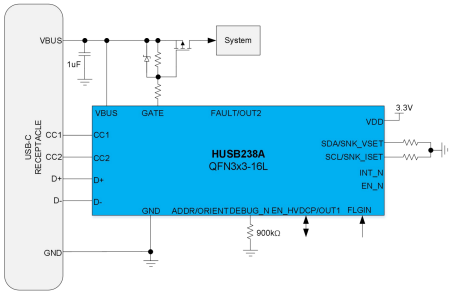
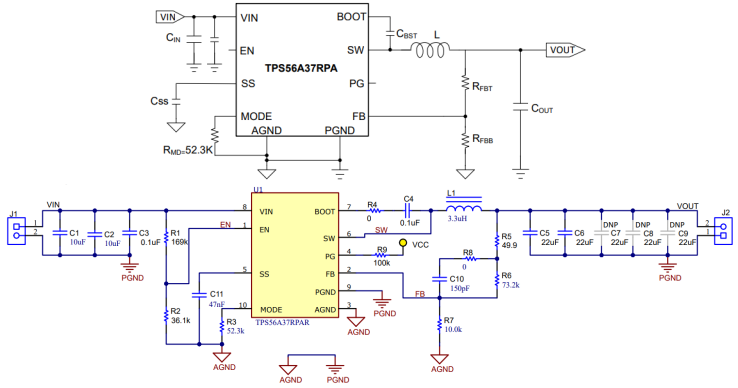


Figure 4. HUSB238A configured as GPIO mode (Maximum 28V)



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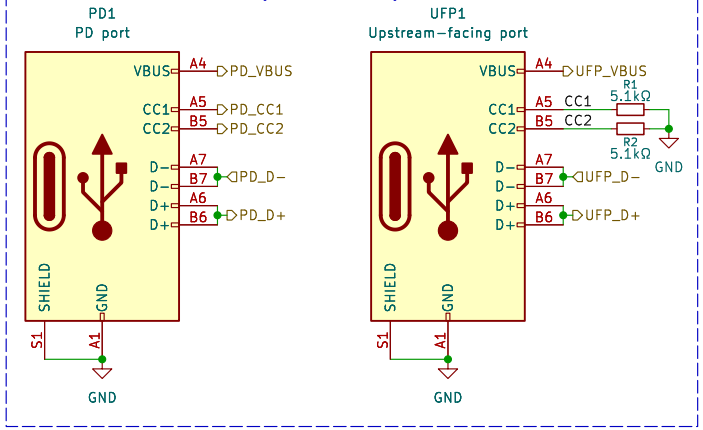
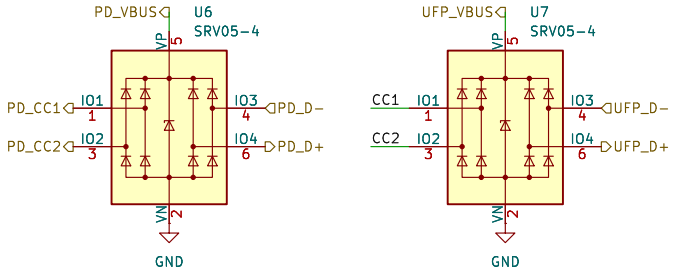
Sheet: /Power management/
File: PD.kicad_sch
Title: Power delivery components
Size: A4 | Date: 2025-12-10 | **Rev: R1**
KiCad E.D.A. 9.0.3 | Id: 3/5

Upstream ports



TVS diodes



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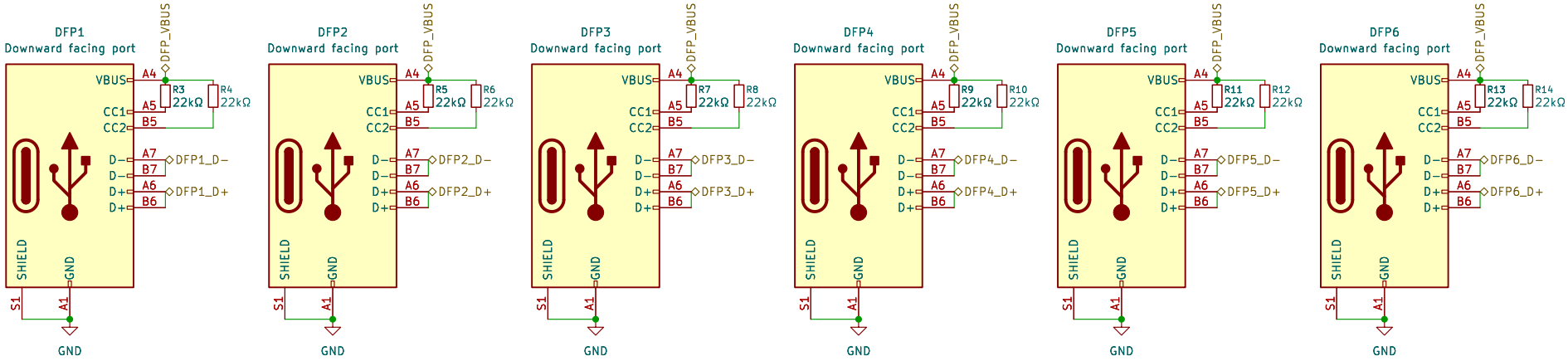
Sheet: /Upstream−facing ports/
File: UFP.kicad_sch

Title: Upstream−facing ports

Size: A4	Date: 2025−12−10	**Rev: R1**
KiCad E.D.A. 9.0.3		Id: 2/5



CC value	Current
56kΩ	500mA
22kΩ	1.5A
10kΩ	3A

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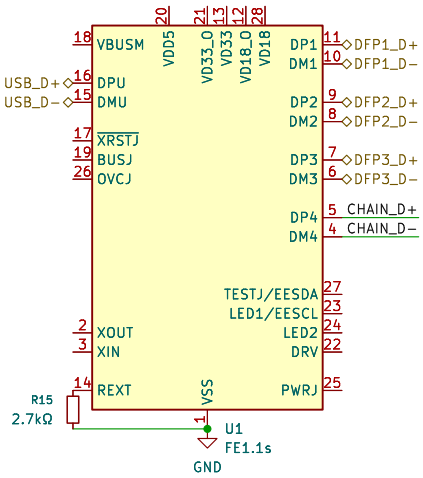
Sheet: /Downstream-facing ports/
File: DFPs.kicad_sch

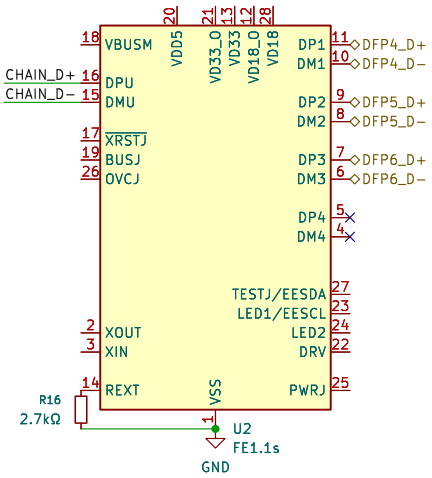
Title: Downstream-facing ports

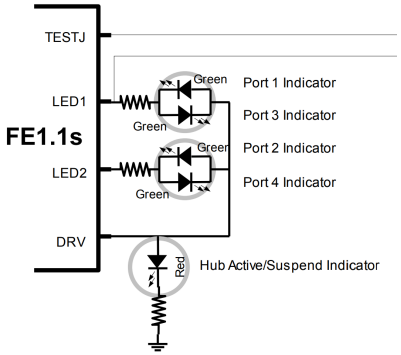
Size: A4	Date: 2025-12-10	**Rev: R1**
KiCad E.D.A. 9.0.3		Id: 5/5

Pin Description Table

Pin Name	LQFP Pin No.	SSOP Pin No.	Type	Function	Note
VSS	10	1	P	Ground.	
XOUT	11	2	OSC	12 MHz Crystal Oscillator output	
XIN	12	3	OSC	12 MHz Crystal Oscillator input.	
DM4	14	4	UT	The D- pin of the 4th Downstream Facing Port.	
DP4	15	5	UT	The D+ pin of the 4th Downstream Facing Port.	
DM3	17	6	UT	The D- pin of the 3rd Downstream Facing Port.	
DP3	18	7	UT	The D+ pin of the 3rd Downstream Facing Port.	
DM2	20	8	UT	The D- pin of the 2nd Downstream Facing Port.	
DP2	21	9	UT	The D+ pin of the 2nd Downstream Facing Port.	
DM1	23	10	UT	The D- pin of the 1st Downstream Facing Port.	
DP1	24	11	UT	The D+ pin of the 1st Downstream Facing Port.	
VD18_O	26	12	P	1.8V power output from 3.3V→1.8V integrated regulator – a 10μF decoupling capacitor is required.	
VD33	27	13	P	3.3V power input for 3.3V→1.8V integrated regulator.	
REXT	28	14		A 2.7KΩ (± 1%) resister should be connected to VSS to provide internal bias reference.	
DMU	30	25	UT	The D- pin of the Upstream Facing Port.	
DPU	31	16	UT	The D+ pin of the Upstream Facing Port.	
XRSTJ	34	17	I	External Reset, active low, is an optional source of chip reset signal, beside the build-in Power-On-Reset. The minimum low pulse width is 10 μs.	
VBUSM	35	18	I	The V_{BUS} Monitor of upstream facing port.	
BUSJ	36	19	I	Bus power indicator: 0 – Bus Powered; 1 – Self Powered.	
VDD5	38	20	P	5V power input for integrated 5V→3.3V regulator.	
VD33_O	39	21	P	3.3V power output from 5V→3.3V integrated regulator – a 10μF decoupling capacitor is required.	
TEST	40	———	I	Test Mode Enable – should be tied to ground for normal operation.	
DRV	42	22	I/O	LED Drive Control	1
LED1/ EESCL	43	23	I/O	Port 1 and Port 3 Enabled Indicator (LED) Control, and external Serial EEPROM Clock.	1
LED2	44	24	I/O	Port 2 and Port 4 Enabled Indicator (LED) Control	1
PWRJ	47	25	O	Downstream Device Power Enable, active low, for *Ganged Power Switching*.	
OVCJ	48	26	I	Over Current Indicator, active low, for *Global Over-Current Protection.*	
TESTJ/ EESDA	2	27	I/O	Test Mode Enable, active low with internal pull-up, and external Serial EEPROM Data/Address.	1
VD18	9	28	P	1.8V power input.	







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Sheet: /USB hub/
File: USB hub IC.kicad_sch

Title: USB 2.0 hub controllers + LEDs

Size: A4	Date: 2025-12-10	Rev: R1
KiCad E.D.A. 9.0.3		Id: 4/5