Piratach Yoovidhya

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Education

Carnegie Mellon University • Pittsburgh, PA

M.S. in Computer Science, Research Thesis (GPA: 4.0) *August 2024*

B.S. in Computer Science, Concentration in Computer Systems *May 2022*

Selected Coursework:

15-740, Computer Architecture
15-410, Operating Systems
15-451, Algorithm Design and Analysis
17-715, Hardware Security
15-852, Parallel and Concurrent Algorithms
15-744, Graduate Computer Networks

Work Experience

Apple Inc. • Graphics Modeling Engineer • *Cupertino, CA* ***(Aug 2024 - Present)***

- Performance modeling for GPU memory systems.

Google LLC • Software Engineer • *Sunnyvale, CA* ***(Aug 2022 - July 2023)***

- Worked within Google Cloud Storage, designing and implementing a load generator used to generate prod-representative traffic.
- This is used to ensure changes are robust, and will not cause any issues when rolled out to production.

KBTG • Data Science Intern • *Bangkok, Thailand* ***(Jun 2019 - Aug 2019)***

- Worked in the data science team to develop a feature that evaluated the price of a car (for collateral) from a photo to be used in K-Plus, Thailand's #1 mobile banking app
- Successfully developed a license plate and vehicle image recognition model using Keras, and connected it to a pipeline that would function as a part of the vehicle price evaluation program

Research Experience ***(at Carnegie Mellon University)***

Simulating Cache Coherence for Cache-Attached Accelerators ***(Aug 2023 - Aug 2024)***

- Builds on top of existing work on Kobold, through a **model** in the **gem5** simulator. (**C++**, **Python**)
- Designed and implemented a novel memory access predictor, novel replacement policies, and micro-benchmarks.
- In collaboration with Professor Nathan Beckmann and PhD student Jennifer Brana.

Microarchitectural Simulation of Polymorphic Cache Hierarchy ***(Jan 2022 - May 2022)***

- Simulated microarchitecture through a dataflow architecture on a CGRA in a **Zsim-based** simulator in **C++**.
- Allows for fine-grained instruction-level parallelism and flexibility over routing of inputs/outputs.
- In collaboration with Professor Nathan Beckmann and PhD students Brian Schwedock and Nikhil Agarwal.

täkō: a polymorphic cache hierarchy ***(Nov 2020 - May 2022)***

- Designed and implemented applications that show a significant speedup compared to the baseline cache.
- Identified potential problem in the system, where the callbacks would pollute the core's L2 with unused data. This is later addressed in Kobold.
- Best paper nominee at ISCA'22.
- Collaborated with Professor Nathan Beckmann and PhD student Brian Schwedock.

Notable Skills: C, C++, Python, CUDA, Modelling, Memory Systems, Accelerators, gem5, CPU Architecture, GPU Architecture, Low-power Computing, Cache Design