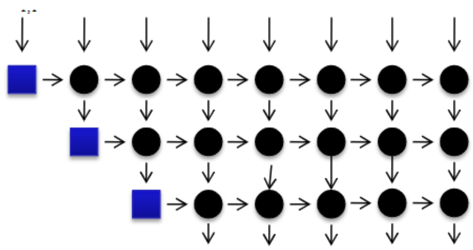
ELEC 522 Assignment 5

Student: Sixu Li (S01435077)

1. Description of QRD design architecture



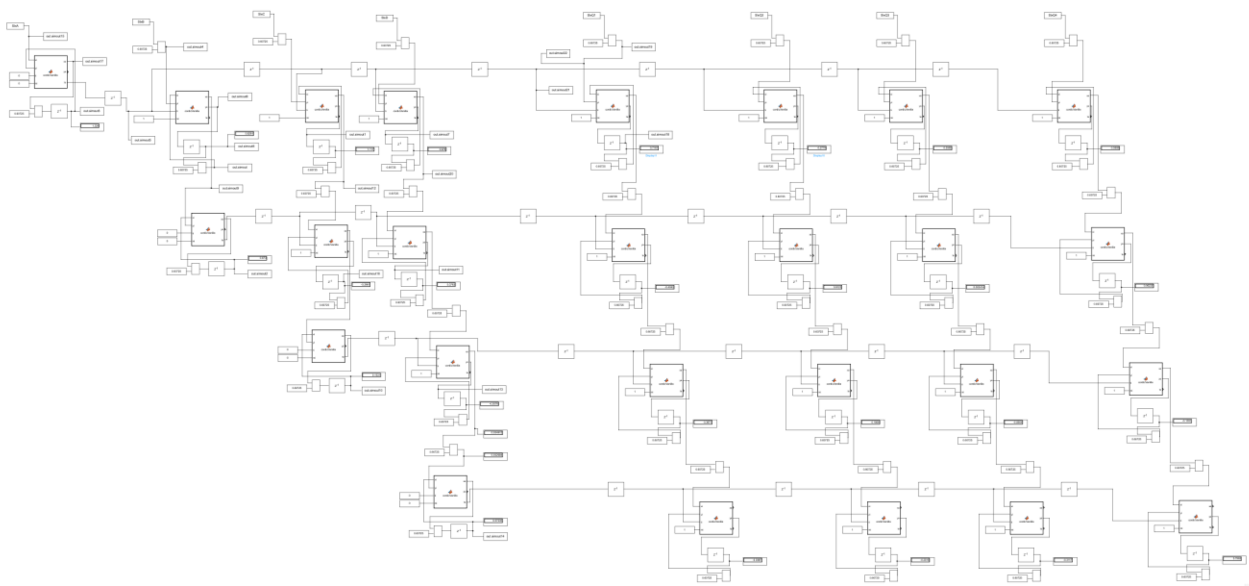
Here we adopted the design show in the slide. But with another row for easier control.

Each element can perform in either vectoring mode or rotating mode.

There will be additional unload input fed into the array for unloading.

2. Model Composer model using the Vitis HLS block and testing results.

The screenshot shows the architecture of the QRD Array.



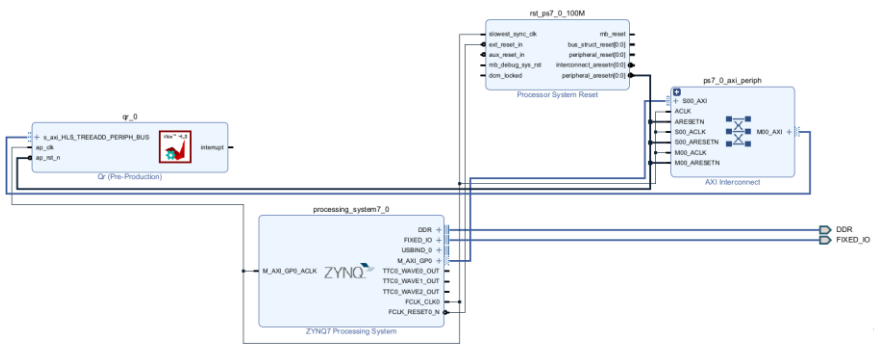
The following figure shows the test result on the example matrix. We can see that the result from the Simulink modules matched with theoretical results.

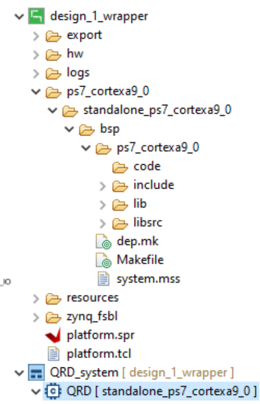
```
>> simQ

simQ =

    0.7163   -0.4033    0.4011    0.4041
    0.2767    0.9129    0.1902    0.2319
    0.3079    0.0051   -0.8882    0.3411
    0.5617    0.0618   -0.1184   -0.8165

>> Q_gt

Q_gt =

   -0.7162    0.4035    0.4008   -0.4044
   -0.2768   -0.9129    0.1900   -0.2322
   -0.3080   -0.0050   -0.8885   -0.3401
   -0.5617   -0.0618   -0.1175    0.8166
```

```
>> simR

simR =

    1.2285    0.8255    1.1174    0.6787
         0    0.6741   -0.2952    0.3774
         0         0    0.1523   -0.5098
         0         0         0   -0.1099

>> R_gt

R_gt =

   -1.2285   -0.8256   -1.1173   -0.6788
         0   -0.6740    0.2953   -0.3773
         0         0    0.1524   -0.5096
         0         0         0    0.1105
```

3. Generate IP block from Model Composer and integrate with ARM processor using Vivado. Generate hardware and XSA for Vitis

The following two figure shows the Block Design Diagram in Vivado, and the compiled XSA in Vitis.





4. Vitis C++ control of QRD Model Composer accelerator with testing results of at least 2 test matrices

Note that the Q output by the program is the Q Transpose, so the results are correct. And in QR decomposition, the sign (+ / -) of Q and R are not important considering one flip in one row will be flipped back in another row during rotation, so we only need to compare the absolute value.

The following 4 screenshots show two test cases. The latter one may have a bit larger error, but that is due to the CORDIC iteration number and the cost brought by fixed point. The error is larger in the last row of Q in test case 2 compared to others, that is cost by the last row of R, we can see that R[4,4] in test case 2 is 0.006, which is very small. The last row of Q is generated by the last row of R, so the error will be larger too.

Test Case 1

```
>> A1

A1 =

    0.8799    0.3194    0.9805    0.0850
    0.3401    0.8438    0.0687    0.4099
    0.3784    0.2577    0.2073    0.6262
    0.6900    0.5054    0.5914    0.5547

>> r1

r1 =

   -1.2285   -0.8256   -1.1173   -0.6788
         0   -0.6740    0.2953   -0.3773
         0         0    0.1524   -0.5096
         0         0         0    0.1105

>> q1

q1 =

   -0.7162   -0.2768   -0.3080   -0.5617
    0.4035   -0.9129   -0.0050   -0.0618
    0.4008    0.1900   -0.8885   -0.1175
   -0.4044   -0.2322   -0.3401    0.8166
```

```
--- Start of the Program ---

Current done: 2

------------------------------------------------------

Matrix R:

1.2285, 0.8260, 1.1166, 0.6788

0.0000, 0.6731, -0.2964, 0.3761

0.0000, 0.0000, 0.1530, -0.5087

0.0000, 0.0000, 0.0000, 0.1158

Matrix Q:

0.7159, 0.2778, 0.3084, 0.5608

-0.4046, 0.9121, 0.0033, 0.0622

0.3971, 0.1868, -0.8916, -0.1094

-0.4069, -0.2351, -0.3307, 0.8175

---------------

1.0000, 2.0000

--- End of the Program ---
```

Test Case 2

```
>> A2

A2 =

    0.7241    0.5470    0.2991    0.5388
    0.5470    0.4991    0.1706    0.4716
    0.2991    0.1706    0.1898    0.1337
    0.5388    0.4716    0.1337    0.5239

>> r2

r2 =

   -1.0969   -0.8881   -0.3999   -0.8846
         0   -0.1052    0.1045   -0.1363
         0         0   -0.0400    0.0628
         0         0         0    0.0006

>> q2

q2 =

   -0.6601   -0.4987   -0.2727   -0.4912
    0.3729   -0.5344    0.6800   -0.3362
    0.0966   -0.6751   -0.2424    0.6901
   -0.6449    0.1002    0.6360    0.4118
```

```
--- Start of the Program ---
Current done: 2

-----------------------------------------------------

Matrix R:

1.0970, 0.8877, 0.3997, 0.8842

0.0000, 0.1062, -0.1040, 0.1365

0.0000, 0.0000, 0.0412, -0.0630

0.0000, 0.0000, 0.0000, 0.0023

Matrix Q:

0.6594, 0.4973, 0.2738, 0.4921

-0.3667, 0.5385, -0.6842, 0.3275

-0.0667, 0.6664, 0.2215, -0.7081

0.5730, -0.1242, -0.5587, -0.3306

--------------

1.0000, 2.0000

--- End of the Program ---
```

5. Synthesis and place and route implementation report from Vivado.

The following two figures are the area & timing report after synthesis.

Name	Slice LUTs (53200)	Slice Registers (106400)	F7 Muxes (26600)	F8 Muxes (13300)	DSPs (220)	Bonded IOPADs (130)	BUFGCTRL (32)
design_1_wrapper	15361	13315	197	18	48	130	1
design_1_i (design_1)	15361	13315	197	18	48	0	1
processing_system7_	24	0	0	0	0	0	1
ps7_0_axi_periph (de	421	562	0	0	0	0	0
qr_0 (design_1_qr_0_	14897	12713	197	18	48	0	0
rst_ps7_0_100M (des	19	40	0	0	0	0	0

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.665 ns	Worst Hold Slack (WHS):	0.045 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	29777	Total Number of Endpoints:	29777	Total Number of Endpoints:	14075

All user specified timing constraints are met.

The following two figures are the area & timing report after P&R.

Hierarchy

Name	Slice LUTs (53200)	Slice Registers (106400)	F7 Muxes (26600)	F8 Muxes (13300)	Slice (13300)	LUT as Logic (53200)	LUT as Memory (17400)	DSPs (220)	Bonded IOPADs (130)	BUFGCTRL (32)
design_1_wrapper	14804	13196	197	18	5324	14107	697	48	130	1
design_1_i (design_1)	14804	13196	197	18	5324	14107	697	48	0	1
processing_system7_	0	0	0	0	0	0	0	0	0	1
ps7_0_axi_periph (de	373	450	0	0	169	322	51	0	0	0
qr_0 (design_1_qr_0_	14414	12713	197	18	5164	13769	645	48	0	0
rst_ps7_0_100M (des	17	33	0	0	12	16	1	0	0	0

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.535 ns	Worst Hold Slack (WHS):	0.008 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	29525	Total Number of Endpoints:	29525	Total Number of Endpoints:	13946

All user specified timing constraints are met.

6. Turning in files including Model Composer file, screen capture of Vivado block diagram, Vitis C++ file, and screen capture of Vitis terminal results

All the screenshots are attached in this report.

- A5V3FIX > Vitis HLS files
- A5V3_HDL > Vivado HDL project
- BareMetal > Vitis arm programs
- MATLAB > Model Composer files