ELEC 522 Assignment 3

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1. Describe how you changed your C code and the architecture constraints to optimize your design.

The basic function element of my hls block is Vector-Vector multiplication (VVM). VVM is the basic operation in Matrix-Vector Multiplication (MVM) and Matrix-Matrix Multiplication (MMM). The HLS block adopted a multiplication – adder tree.

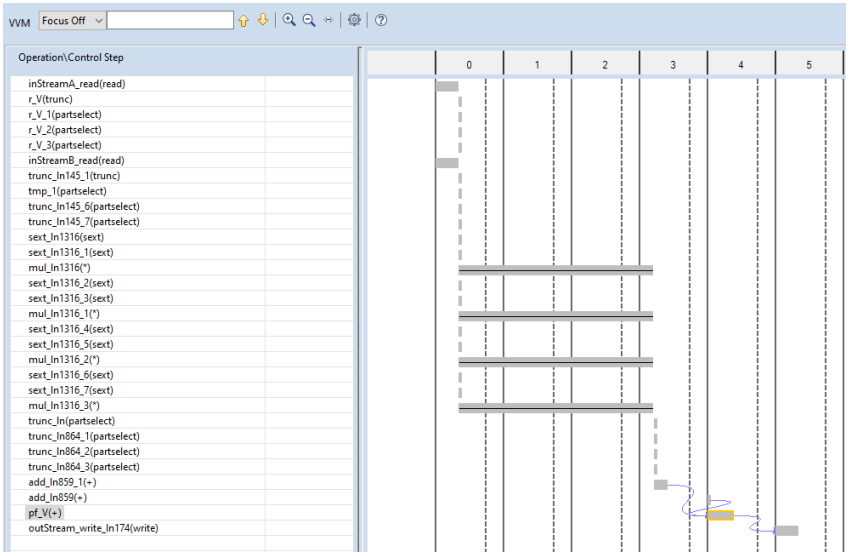
2.Write C testbench code to verify the function of your code and use Vitis HLS simulation tools to verify at this level.

Testbench is attached in the submitted zip file.

3. Describe your final choice of the constraint configurations and explain the advantages of your final design over the other trial designs that you made.

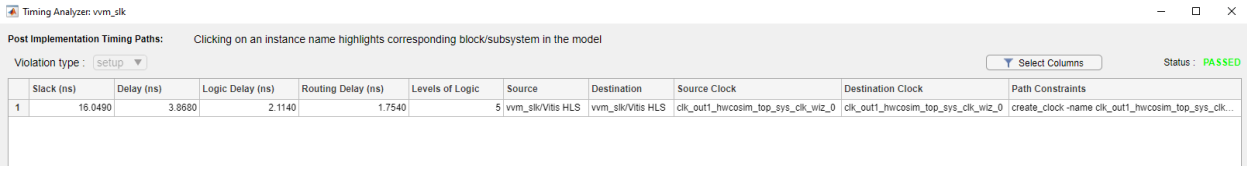
No additional constrains, by adopting vector data structure. The multiplication will be automatically computed in parallel.

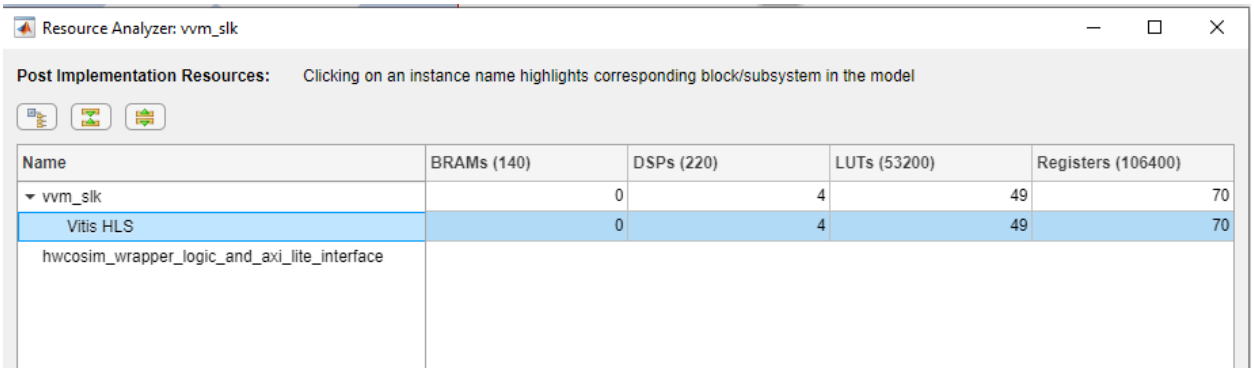
4. Include and explain the timing scheduling results from the Vitis HLS Gannt chart schedule graphics.



From the above figure, we can see that the vector is first multiplied in parallel. Then two addition is performed to get the partial sum. The final sum is then calculated and fed into the stream fifo.

5. Give the timing and resource information from the synthesis and place and route implementation report from HDL Netlist generation after integration into Model Composer.

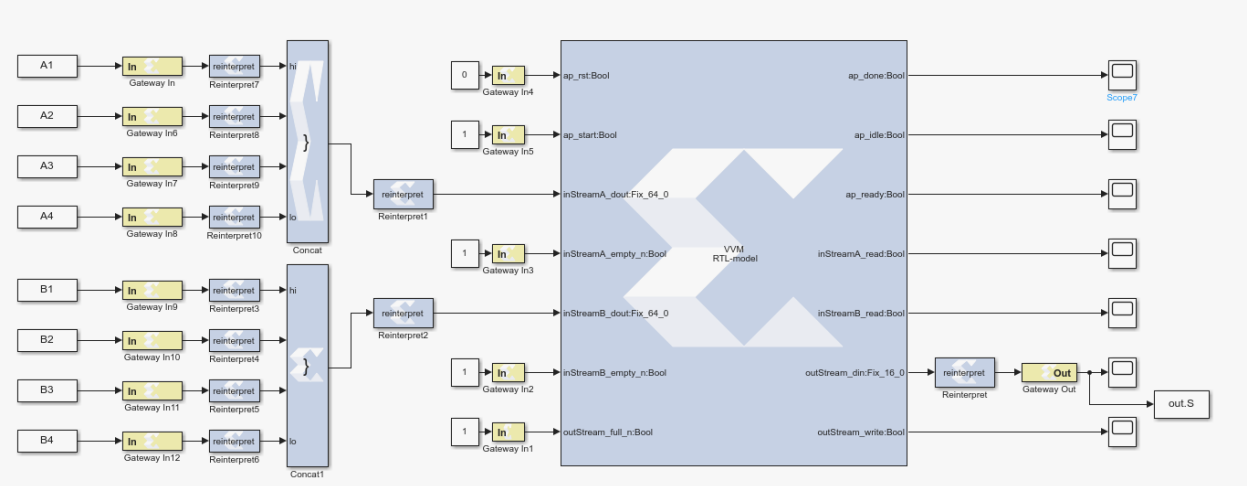




6. Calculate maximum throughput of your system.

This module can perform a vector-vector multiplication with 5 clocks. Which is 4 OPS / 5 clock. With 100MHz clock, the throughput is 80MOPS/s in 16bit.

7. Use Vitis HLS block to test the complete matrix multiplication in Model Composer as in Project 2. The design should support continuous matrix multiplication



8. Do hardware in the loop Co-Simulation to verify performance of Vitis HLS code on the ZedBoard in the lab.

Done.

9. Compare the results of this project with those from the Model Composer matrix multiplication project 2 and discuss the differences between the two design flows that possibly cause the different results.

The module in project 2 can perform the matrix multiplication within 16 clocks, the matrix multiplication contains 16*4 OPS. The throughput is 400MOPS/s in 16bit. The throughput in project 2 is significantly higher than the project 3. The main reason is that I do not know how to implement systolic array in HLS.

10. Turn in all project source files, .c, .m, .slx, and instructions on how to test.

All the files are included in the submitted zip file.