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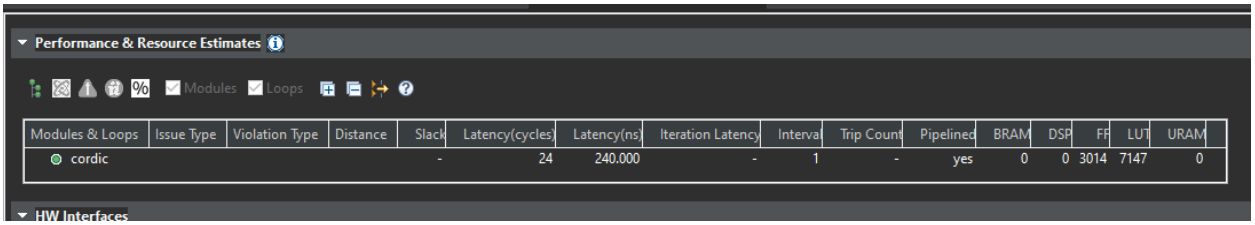
September 29th 2022

Elec 522

High Level Design

The purpose of this project is to find the QR decomposition of a Given 4 x 4 Matrix systolically initially in model composer and then use vitis to put into ARM Core.

Final Resource Usage from HLS



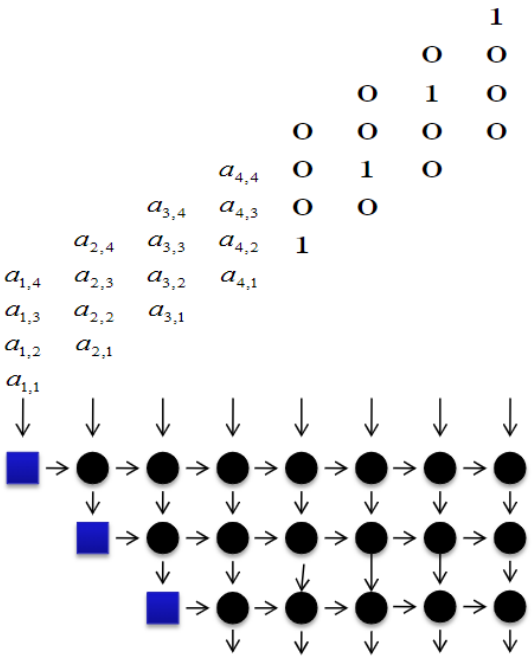
Notice no DSPs were used in this solution For the HLS portion.

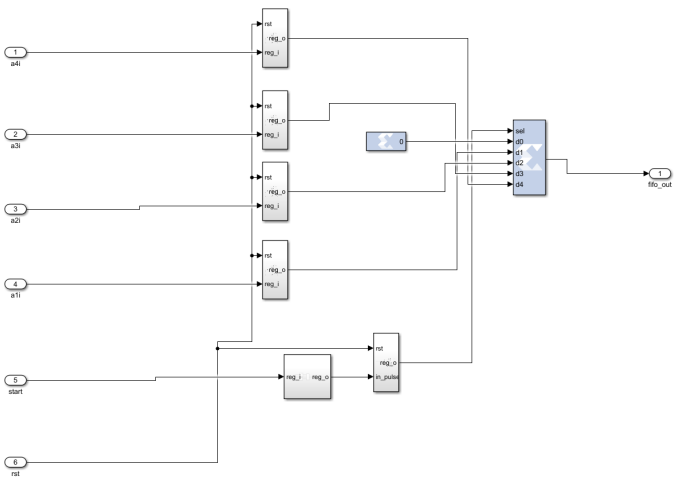
Model Composer Architecture:

Inputs:

- **Ai matrix** (16 elements, <16,3> Fixed T),
- **Reset signal** (Bool) which resets all registers and processes of leading and unloading variables, and
- **Start Signal** (bool) which is a signal set high when all variables are loaded properly and calculator can begin (for timing),

Each of the elements is latched to a register which then fed to a multiplexer awaiting the start signal such that a column can be fed into the rotation and arctan blocks ina systolic manner such as that of the figure to the right:

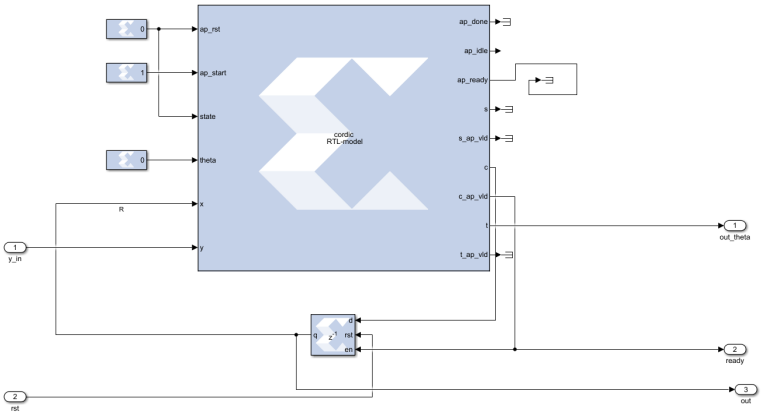




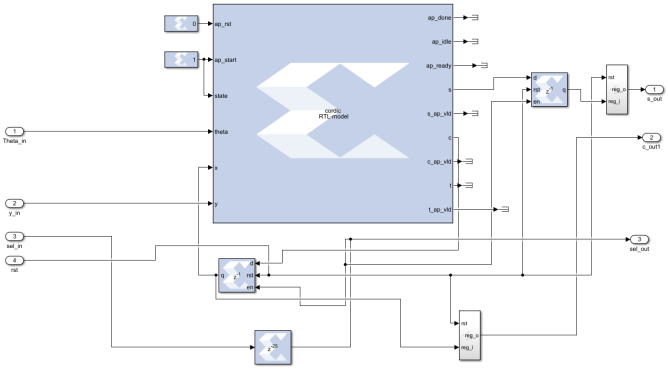
Calculations of elements

My design allows the variables to be loaded in a non-systolic way (the inputs can be placed into design all at once) and yet load the elements into the cordic blocks in a pipelined systolic manner. This Allows it to be easily used in vitis because it's harder to control inputs that are very cycle and time dependent.

Arctan block



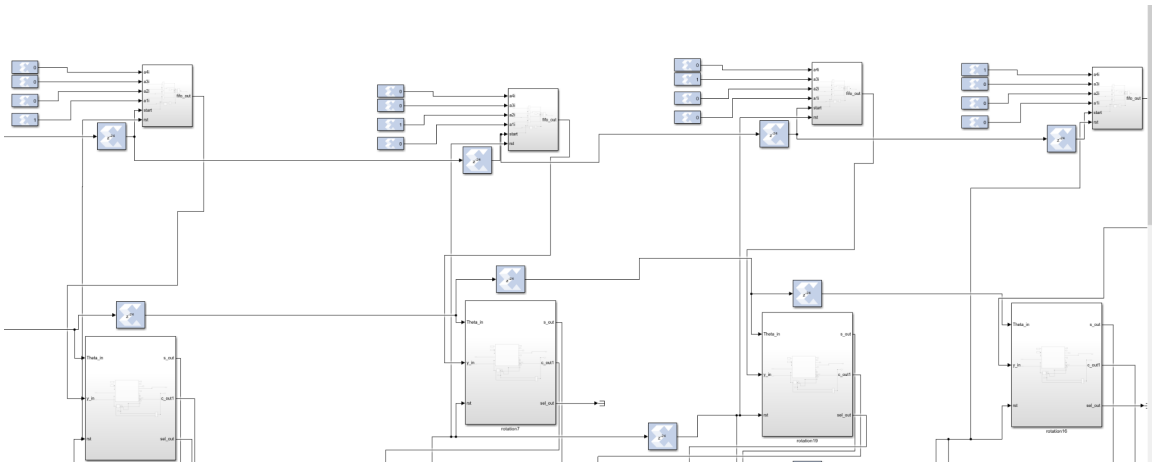
Rotation Block



Shown above is the Arctan block which feeds back the Cosine for the next theta and a_i_i value, the register saves that value for when it's done calculating that value and when it's time for a new matrix value, the register can be reset.

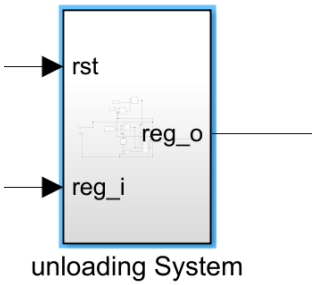
Also shown above is the rotation block which feeds back the Cosine for the next theta and a_i_j value, the register saves that value for when it's done calculating that value and when it's time for a new matrix value, the register can be reset. The registers feed into a latch such that the value is saved and reading the output at a certain cycle would not be necessary.

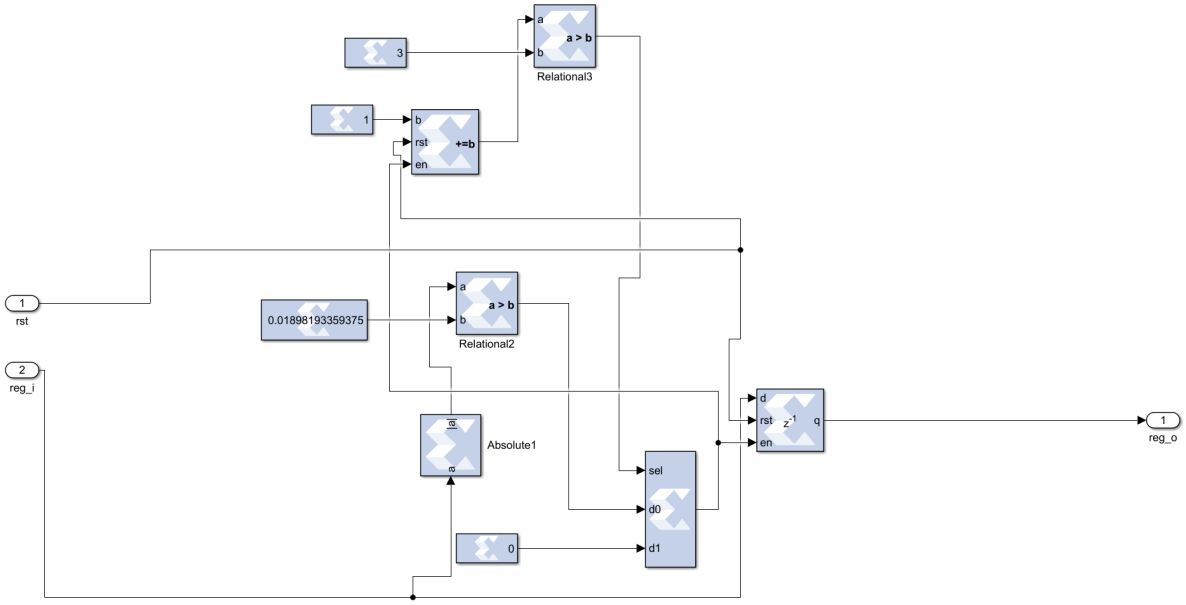
For the Q values, an identity matrix will be fed but since these values are constant as input registers, we don't have to have the identity matrix as a separate matrix input and instad make it built in

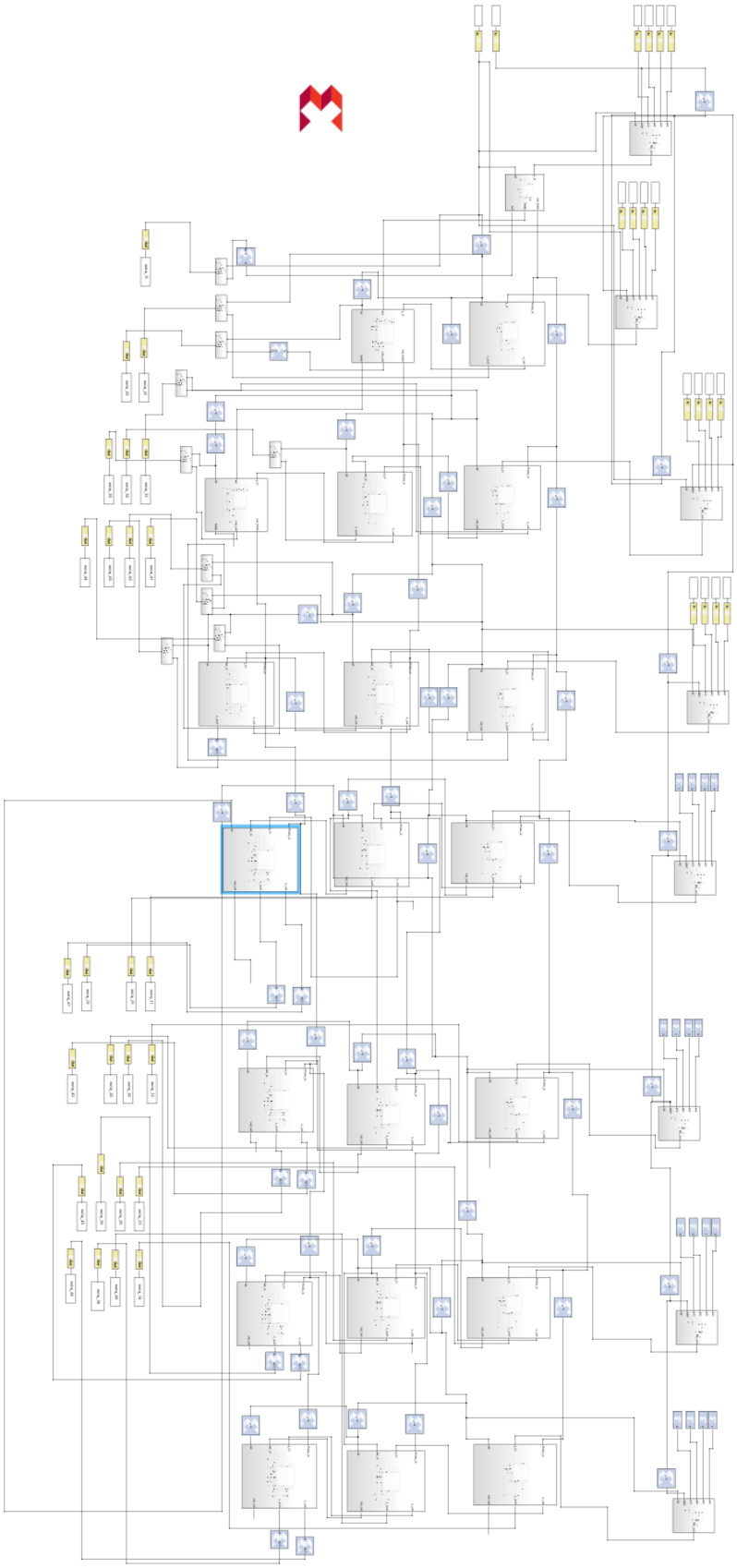


Unloading Variables:

Values coming out of the cordic blocks will be latched into the unloading subsystem which takes the input reg_i, which is the output of cordic. After a certain amount of changes of this value (for the case of values of R matrix is 4) the value will latch and only be reset after the REST signal is given. This ensures that the design can be read without having to be time / cycle dependent.

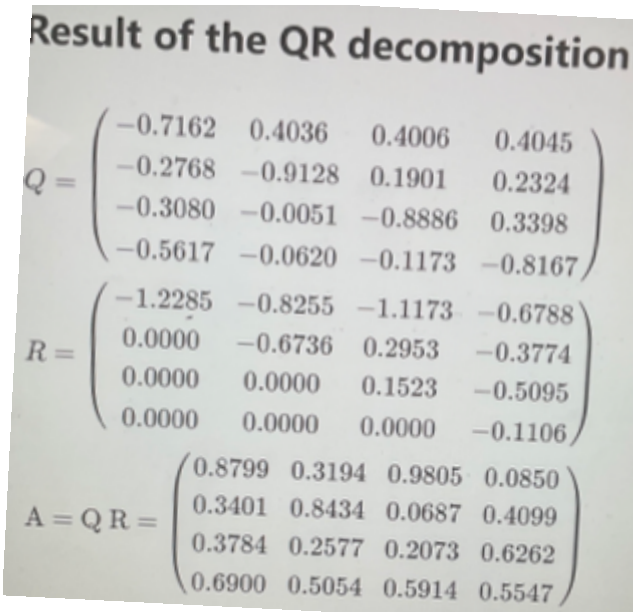




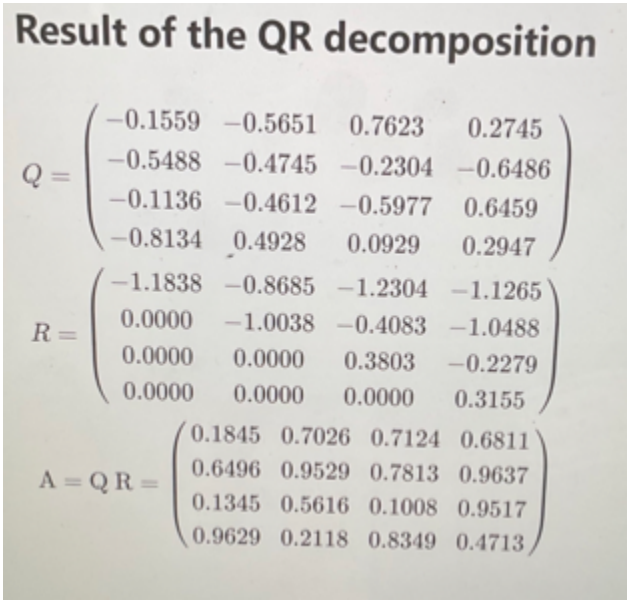


Testing in Model Composer:
These are two matrices that will be used to ensure design is correct

A1 Precalculation:



A2 Precalculation:

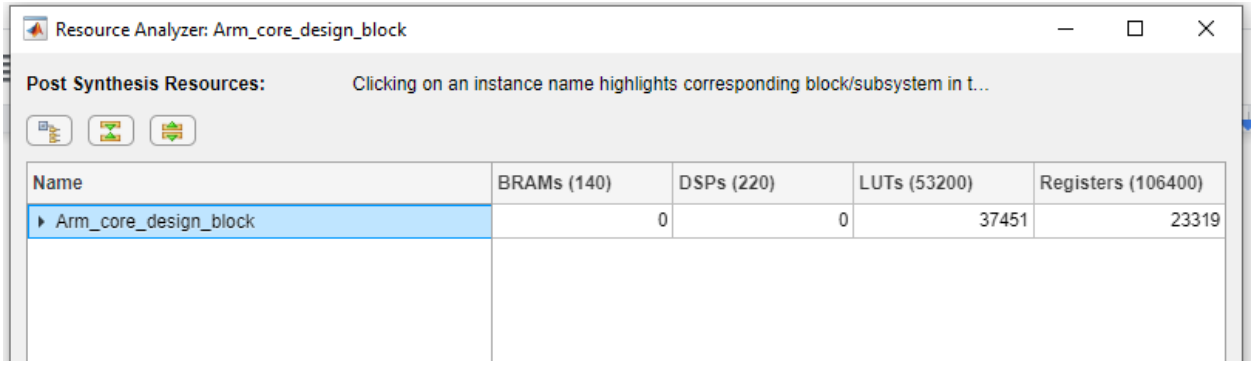


At first, before control for inputs and outputs were made, the design was fully systolic, meaning I was able to calculate the two matrix values of A1 and A2 one after the other. The outputs are below:

```
R1 =

   -1.2269   -0.8223   -1.1075   -0.6766
         0   -0.6707    0.2980   -0.3734
         0         0    0.1549   -0.5016
         0         0         0    0.1147


Q1 =

   -0.7069    0.4049    0.3906    0.4072
   -0.2737   -0.9027    0.1865    0.2371
   -0.3063   -0.0034   -0.8834    0.3298
   -0.5612   -0.0618   -0.1055   -0.8101


R2 =

   -1.1802   -0.8608   -1.2225   -1.1199
         0   -0.9979   -0.4034   -1.0466
         0         0    0.3802   -0.2363
         0         0         0    0.3119


Q2 =

   -0.1517   -0.5587    0.7502   -0.2754
   -0.5427   -0.4711   -0.2208    0.6490
   -0.1122   -0.4601   -0.6001   -0.6287
   -0.8130    0.4885    0.0883   -0.2913
```

Now for model composer, i tested the matrices separately after the handling of the inputs and outtputs. To test A1 you must run Final_design_inputs,m and A2 will be Final_design_inputsa2.m, to read a matrix after simulation is Final_design_disp,m

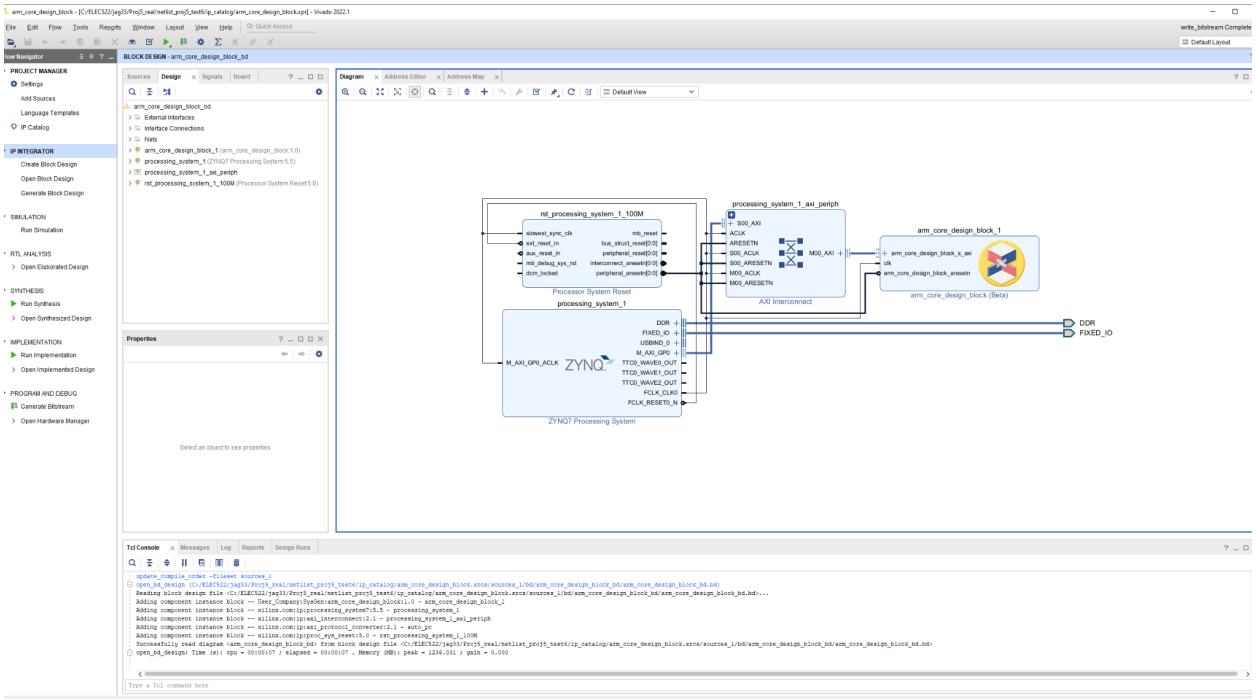
Resource Usage:



LUT: 37451
Reg: 23319

Vivado:

The workspace used for Vivado was Netlist_proj5_test6 which should have all that was included. The exported hardware is in vitis_test6_agan folder which has the vitis testbench



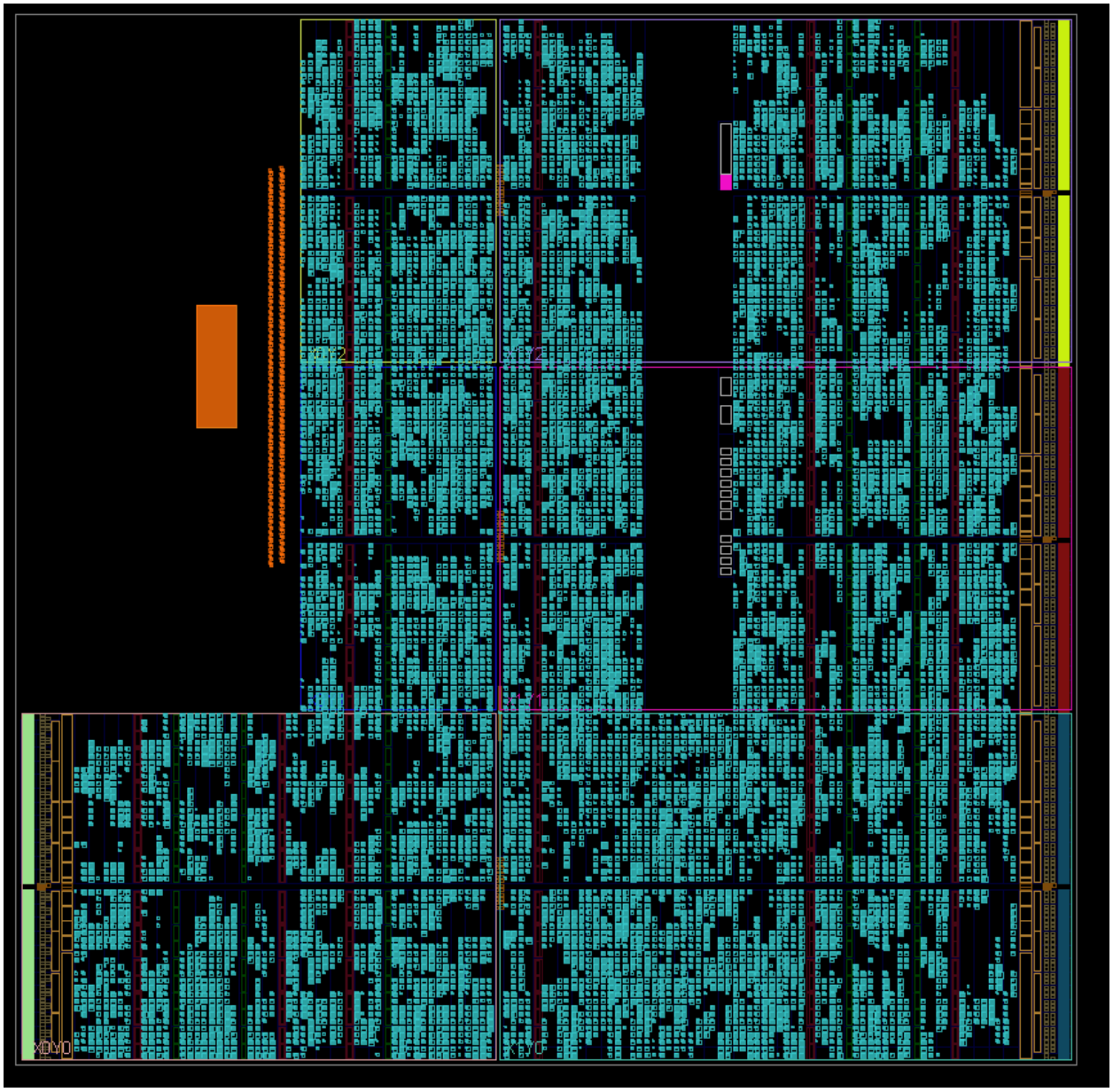
Arm Vitis Section:

In Vitis A test bench was created, where I tested Both matrix A1 and A2 one after the other which gave me accurate results to that of model composer:

```
----------Praying for it working MODE----------

----------A1----------

{0.879883, 0.340088, 0.378418, 0.689941},

{0.319458, 0.843384, 0.25769, 0.505371},

{0.980469, 0.0687256, 0.207275, 0.591431},

{0.0849609, 0.409912, 0.626221, 0.554688}}
----------R1----------

{-1.22693, -0.822266, -1.10754, -0.676636},

{0.00000,-0.669556, 0.298584, -0.371704},

{0.00000, 0.00000, 0.154663, -0.502686},

{0.00000, 0.00000, 0.00000, 0.114746}}
----------Q1----------

{-0.706909, 0.405396, 0.389771, 0.407227},

{-0.273682, -0.901001, 0.186401, 0.237061},

{-0.306274, -0.00341797, -0.883423, 0.329834},

{-0.556152, -0.0582275, -0.105469, -0.810059}}

----------*Next Matrix*----------

----------A2----------
```

```
----------*Next Matrix*----------

----------A2----------

{0.184448, 0.649658, 0.134521, 0.962891},

{0.702637, 0.962891, 0.561646, 0.211792},

{0.712402, 0.78125, 0.10083, 0.834961},

{0.681152, 0.963745, 0.95166, 0.471313}}

----------R2----------

{-1.18018, -0.866455, -1.22253, -1.11877},

{0.00000,-1.00171, -0.400757, -1.03723},

{0.00000, 0.00000, 0.381958, -0.227417},

{0.00000, 0.00000, 0.00000, 0.315552}}
----------Q2----------

{-0.151733, -0.552612, 0.752319, -0.273682},

{-0.542725, -0.474609, -0.22644, 0.643433},

{-0.112183, -0.456665, -0.593384, -0.637695},

{-0.806519, 0.492554, 0.0897217, -0.286865}}
```

Vivado Report



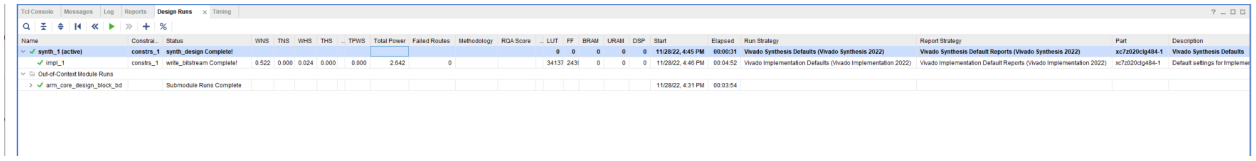
Tcl Console | Messages | Log | Reports | Design Runs | Timing

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Methodology Summary
- Check Timing (0)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.522 ns	Worst Hold Slack (WHS):	0.024 ns	Worst Pulse Width Slack (WPWS):	4.020 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	34362	Total Number of Endpoints:	34362	Total Number of Endpoints:	25546

All user specified timing constraints are met.



Tcl Console | Messages | Log | **Reports** | Design Runs | Timing

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		11/28/22, 4:46 PM	9.2 KB
synthesis_report			11/28/22, 4:46 PM	124.7 KB
Out-of-Context Module Runs				
arm_core_design_block_bd				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		11/28/22, 4:33 PM	8.2 KB
synthesis_report			11/28/22, 4:33 PM	204.1 KB
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		11/28/22, 4:34 PM	8.0 KB
synthesis_report			11/28/22, 4:34 PM	55.4 KB
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		11/28/22, 4:35 PM	7.6 KB
synthesis_report			11/28/22, 4:35 PM	38.1 KB
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		11/28/22, 4:35 PM	8.1 KB
synthesis_report			11/28/22, 4:35 PM	28.2 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc		11/28/22, 4:47 PM	1.5 KB
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io		11/28/22, 4:48 PM	146.6 KB
Utilization - Place Design	report_utilization		11/28/22, 4:48 PM	10.9 KB
Control Sets - Place Design	report_control_sets	verbose = true;	11/28/22, 4:48 PM	142.7 KB
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		

Report	Type	Options	Modified	Size
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc		11/28/22, 4:47 PM	1.5 KB
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io		11/28/22, 4:48 PM	146.6 KB
Utilization - Place Design	report_utilization		11/28/22, 4:48 PM	10.9 KB
Control Sets - Place Design	report_control_sets	verbose = true;	11/28/22, 4:48 PM	142.7 KB
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc		11/28/22, 4:50 PM	1.5 KB
Methodology - Route Design	report_methodology		11/28/22, 4:50 PM	1.6 KB
Power - Route Design	report_power		11/28/22, 4:50 PM	10.1 KB
Route Status - Route Design	report_route_status		11/28/22, 4:50 PM	0.6 KB
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;	11/28/22, 4:50 PM	184.5 KB
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization		11/28/22, 4:50 PM	20.3 KB
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;	11/28/22, 4:50 PM	1.1 KB
implementation_log			11/28/22, 4:51 PM	44.7 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log			11/28/22, 4:51 PM	44.7 KB

```
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+------+-----------------------------------------------------+----------+
|      |BlackBox name                                        |Instances |
+------+-----------------------------------------------------+----------+
|1     |arm_core_design_block_bd_auto_pc_0                   |         1|
|2     |arm_core_design_block_bd_arm_core_design_block_1_0   |         1|
|3     |arm_core_design_block_bd_processing_system_1_0       |         1|
|4     |arm_core_design_block_bd_rst_processing_system_1_100M_0 |         1|
+------+-----------------------------------------------------+----------+

Report Cell Usage:
+------+-----------------------------------------------------------+------+
|      |Cell                                                       |Count |
+------+-----------------------------------------------------------+------+
|1     |arm_core_design_block_bd_arm_core_design_block_1_0_bbox    |     1|
|2     |arm_core_design_block_bd_auto_pc_0_bbox                    |     1|
|3     |arm_core_design_block_bd_processing_system_1_0_bbox        |     1|
|4     |arm_core_design_block_bd_rst_processing_system_1_100M_0_bbox |     1|
+------+-----------------------------------------------------------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:21 . Memory (MB): peak = 1317.441 ; gain = 32.832
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 5 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed = 00:00:19 . Memory (MB): peak = 1317.441 ; gain = 32.832
Synthesis Optimization Complete : Time (s): cpu = 00:00:20 ; elapsed = 00:00:21 . Memory (MB): peak = 1317.441 ; gain = 32.832
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.010 . Memory (MB): peak = 1317.441 ; gain = 0.000
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1343.047 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete, checksum: ee581797
INFO: [Common 17-83] Releasing license: Synthesis
38 Infos, 14 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:24 ; elapsed = 00:00:25 . Memory (MB): peak = 1347.070 ; gain = 62.461
INFO: [Common 17-1381] The checkpoint 'C:/ELEC522/jag33/Proj5_real/netlist_proj5_test6/ip_catalog/arm_core_design_block.runs/synth_1/arm_core_design_block_bd_wrapper.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file arm_core_design_block_bd_wrapper_utilization_synth.rpt -pb arm_core_design_block_bd_wrapper_utilization_synth.pb
```

Conclusion

My design uses no multiplication with magnitude accurate results, My design has inputs and outputs which are not cycle depending on loading and unloading, however the calculations are done in a time dependent manner once the start signal is issued.