ELEC522 – Fall 2022

Project 2: Xilinx FPGA Model Composer Systolic for Matrix Multiplication

By

Hsuan-You (Shaun) Lin

Rice University, Houston, TX

Sep. 30, 2022

Supervised by

Dr. Joseph R. Cavallaro

Contents

List of Figures

Input:

Step 1: Input Matrix m-code

Run the “Input_Matrix.m” file. The program will add the Matrix to workspace as shown in *Figure 1*.

(a) Screen capture of input Matrix m-code

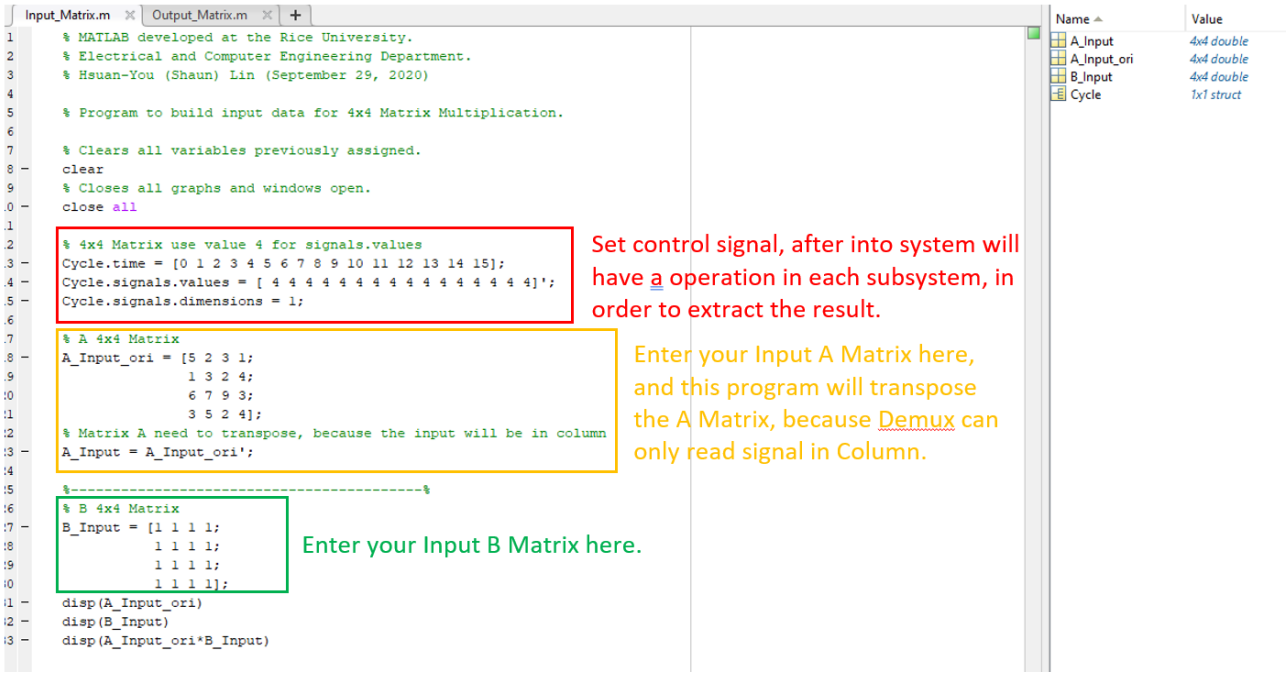


Figure 1.

(b) Screen capture of Command Window input result

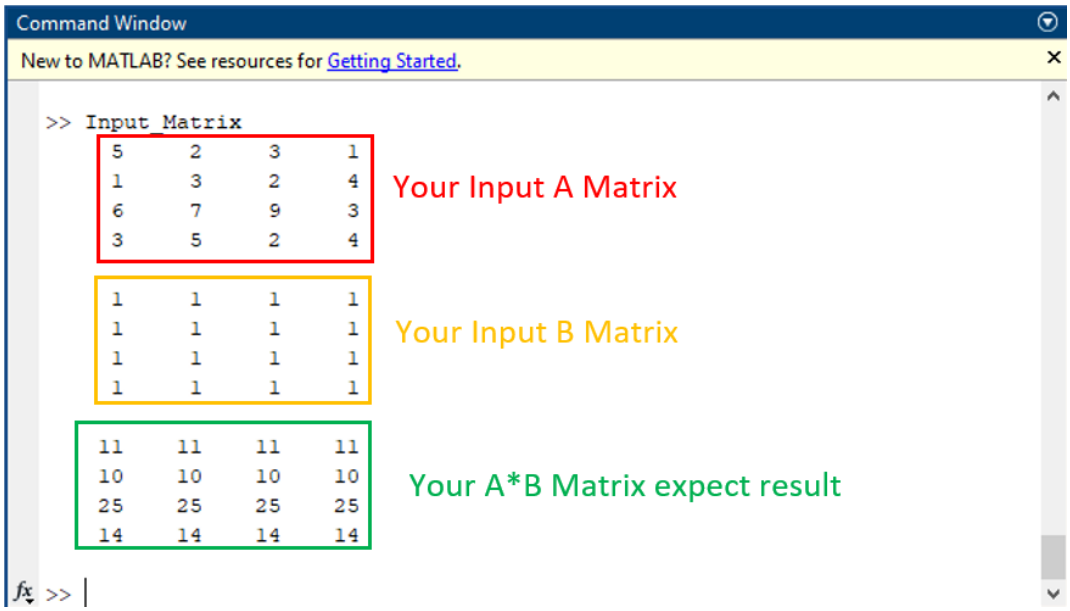


Figure 2.

Step 2: Input signal from workspace into the system

Input A matrix will be read in rows, as shown in *Figure 3*.

(b) Screen capture of A matrix input signal

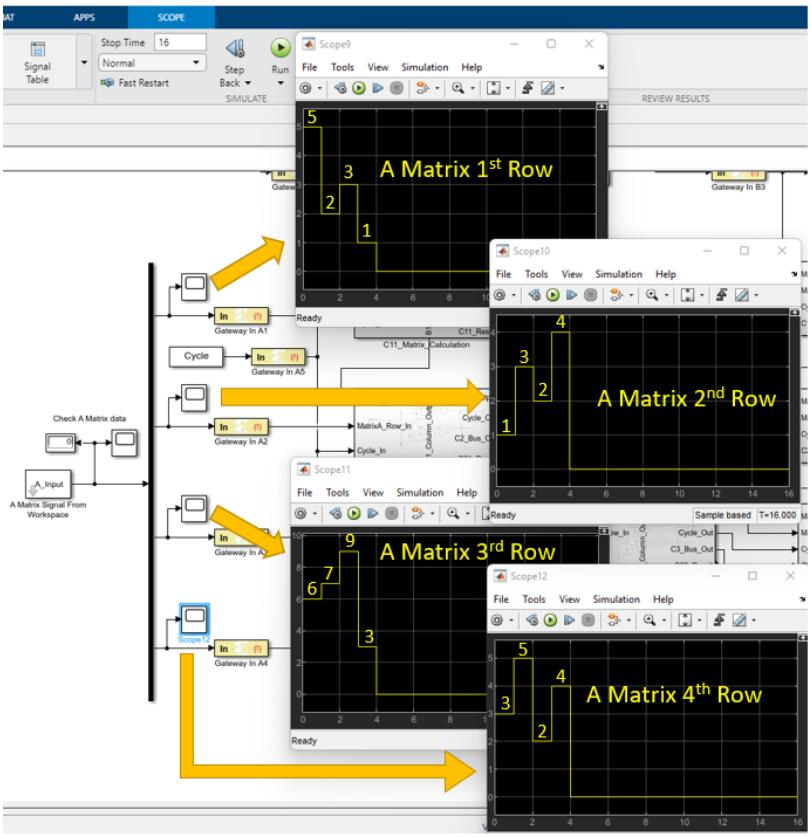


Figure 3.

Input B matrix will be read in columns, as shown in *Figure 4*.

(b) Screen capture of B matrix input signal

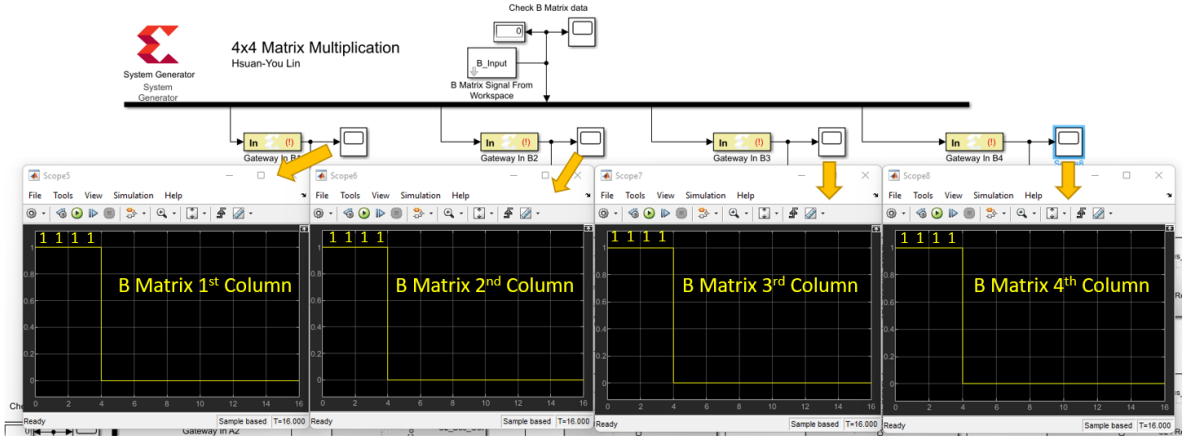


Figure 4.

Architecture:

Step 1: Systolic matrix multiplication system architecture in model composer

I designed this systolic matrix multiplication with 8 inputs, a cycle control signal and 4 output result as shown in *Figure 5*.

(a) Screen capture of my systolic matrix multiplication system architecture (model composer)

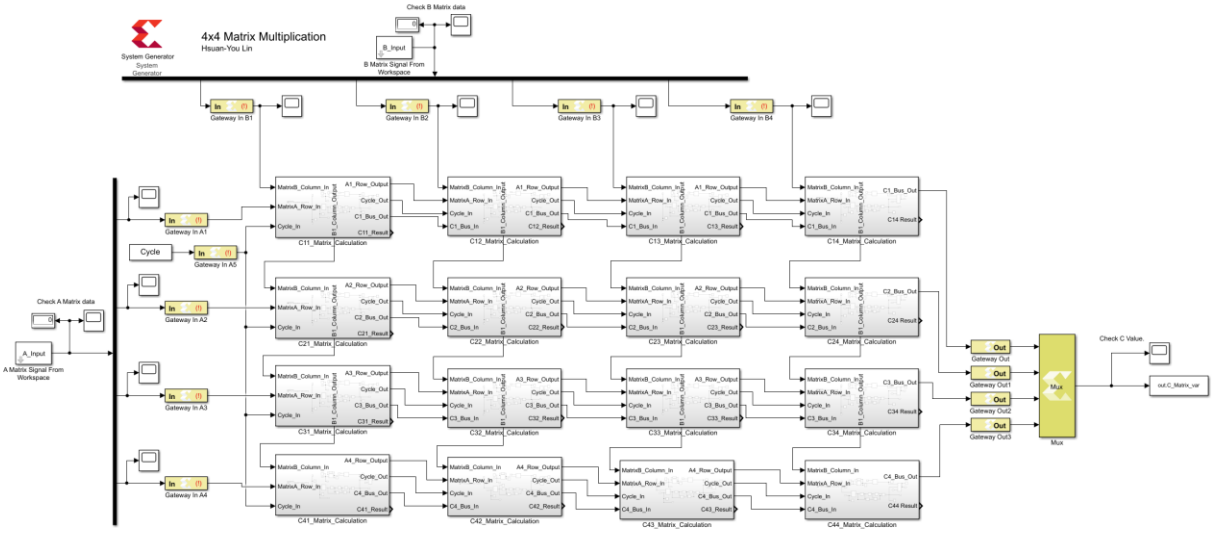


Figure 5.

Step 2: Subsystem architecture

The signal will complete the calculations in the subsystem as shown in *Figure 6*.

(b) Screen capture of my subsystem architecture

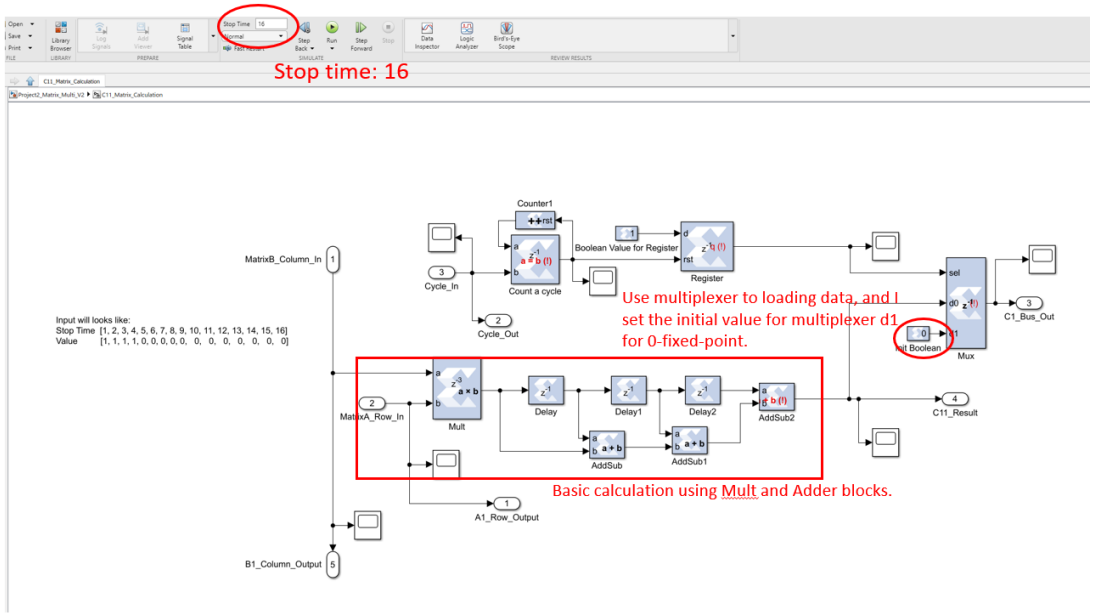


Figure 6.

Step 3: Subsystem calculation result

Using Mult and Adder to calculate A*B signal and use Counter and Register to do the control signal, then in the end of the subsystem use the Multiplexer to accumulate result signals as shown in *Figure 7*.

(c) Screen capture of 1st subsystem signal result

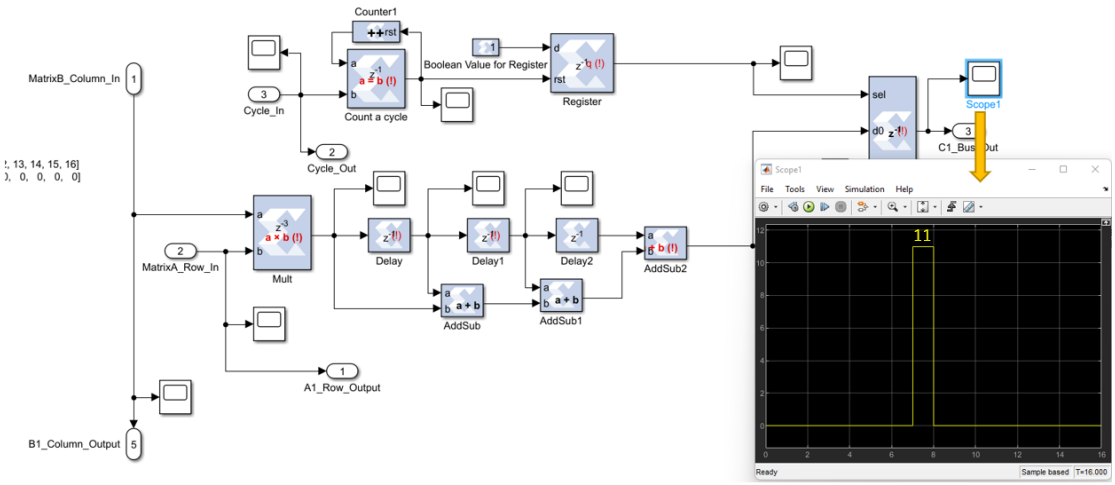


Figure 7.

(d) Screen capture of 16 subsystem signal result

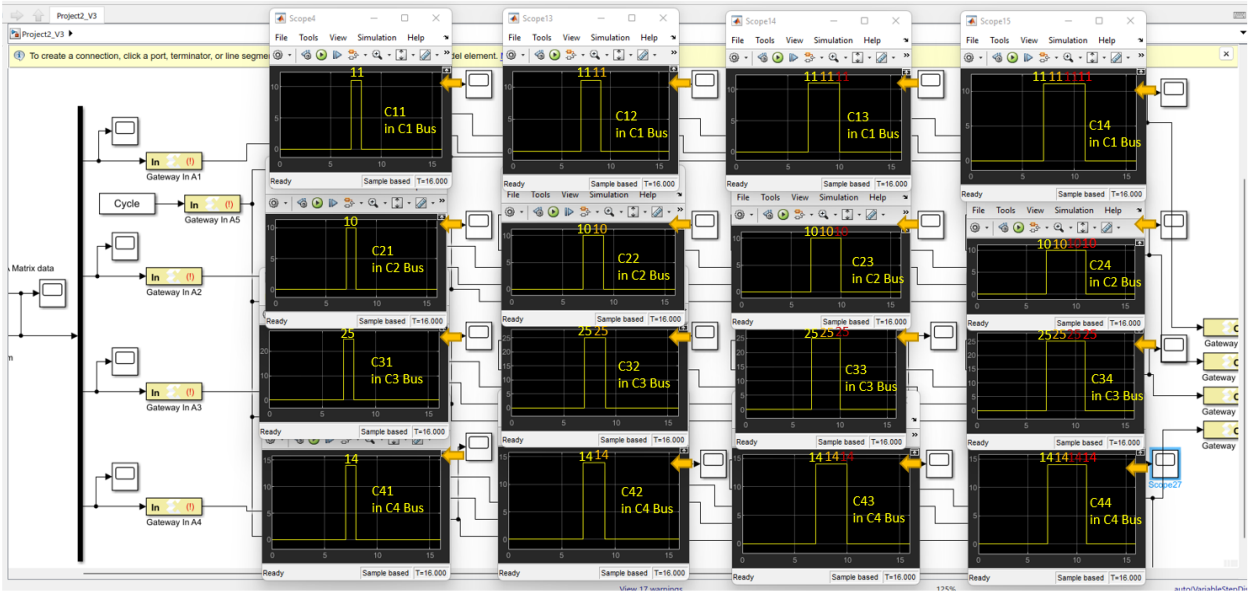


Figure 8.

Output:

Step 1: Output calculation result to workspace

After Systolic Matrix Multiplication, it will have 4 Bus signal use a Mux block to collect all signal to workspace as shown in *Figure 9*.

(a) Screen capture of systolic matrix multiplication system output results to workspace

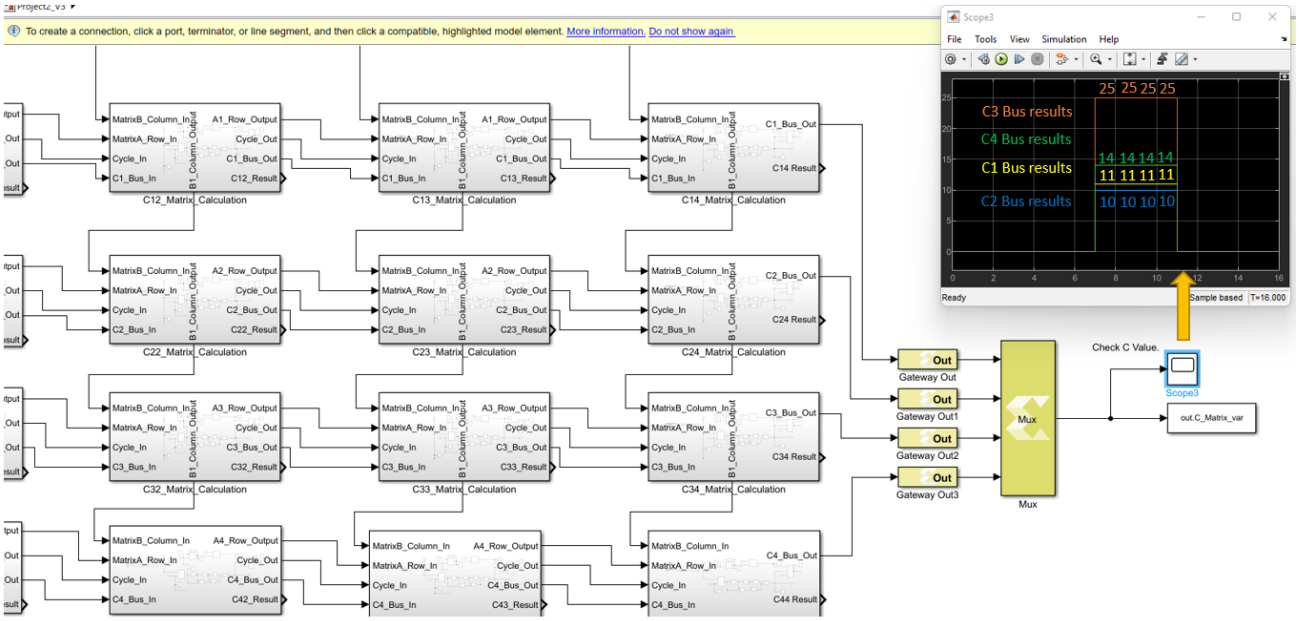


Figure 9.

Step 2: Output Matrix m-code

Run the "Output_Matrix.m" file. The program will read result Matrix from workspace as shown in *Figure 10*.

(b) Screen capture of output Matrix m-code

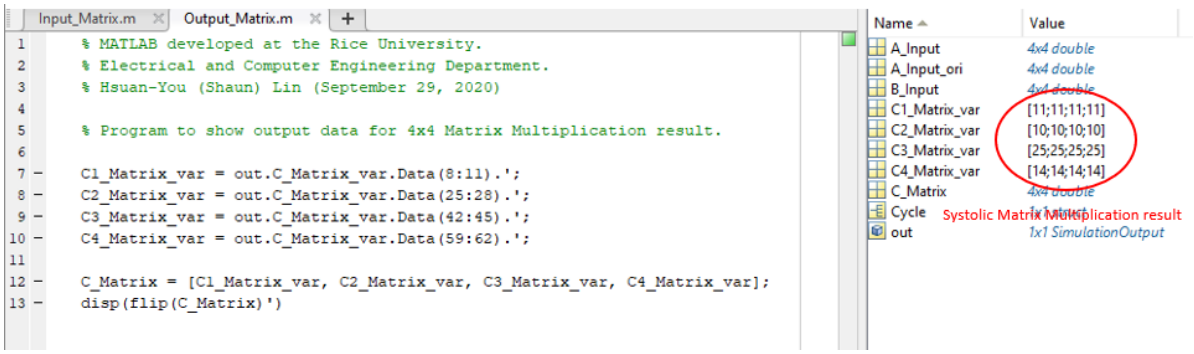


Figure 10.

(c) Screen capture of Command Window output result

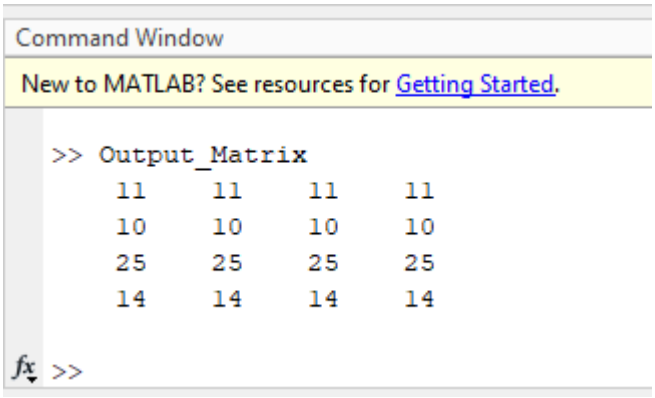


Figure 11.

Hardware co-simulation:

Step 1: Co-Simulation Systolic matrix multiplication system in model composer

After successfully generate the system in JTAG compilation mode, I connect the input and output into gray block system, to simulate the system in Zedboard as shown in *Figure 12*.

(a) Screen capture of co-simulation systolic matrix multiplication system architecture (model composer)

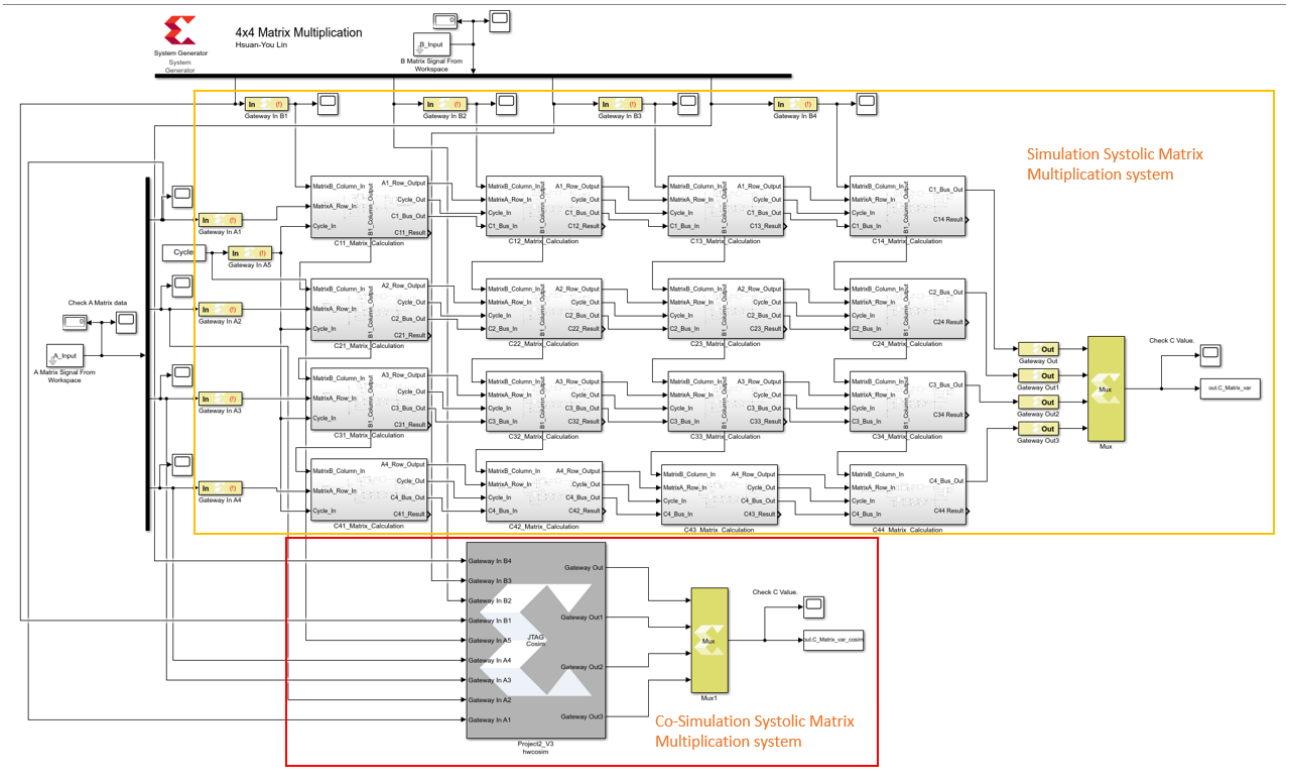


Figure 12.

Step 2:

Run the “Output_Matrix_cosim.m” file. The program will read cosim result Matrix from workspace as shown in *Figure 13*.

(b) Screen capture of cosim output Matrix m-code

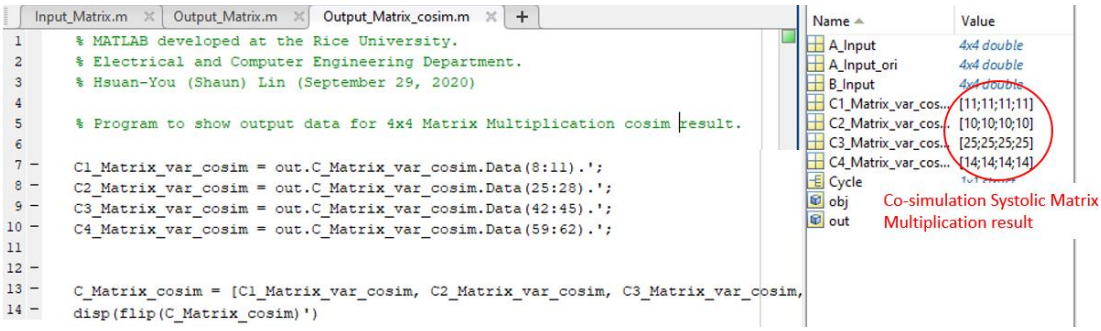


Figure 13.

(c) Screen capture of Command Window output cosim result

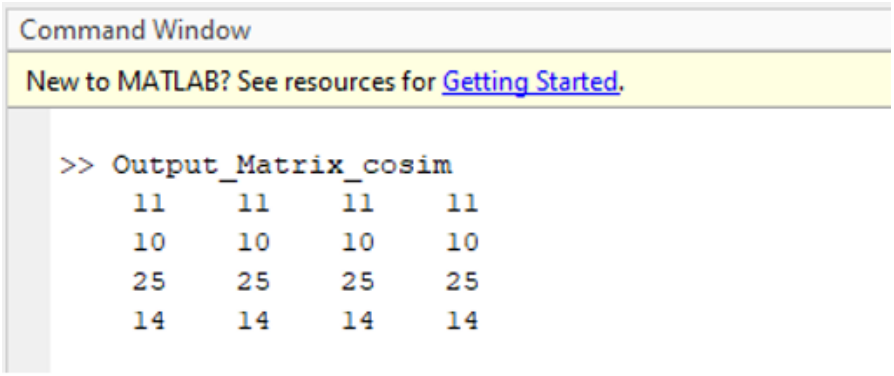


Figure 14.

Resource and Time Result:

Step 1: Resource Analyzer results

After set the Analyzer type to Resource, successfully generate the system, as you can see in *Figure 15*, this system used **16 DSPs, 2,100 LUTs and 2,224 Registers.**

(a) Screen capture of resource analyzer results

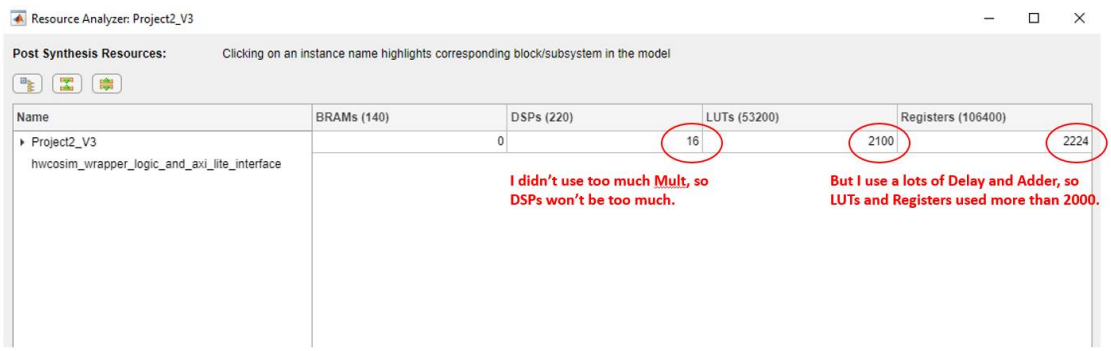
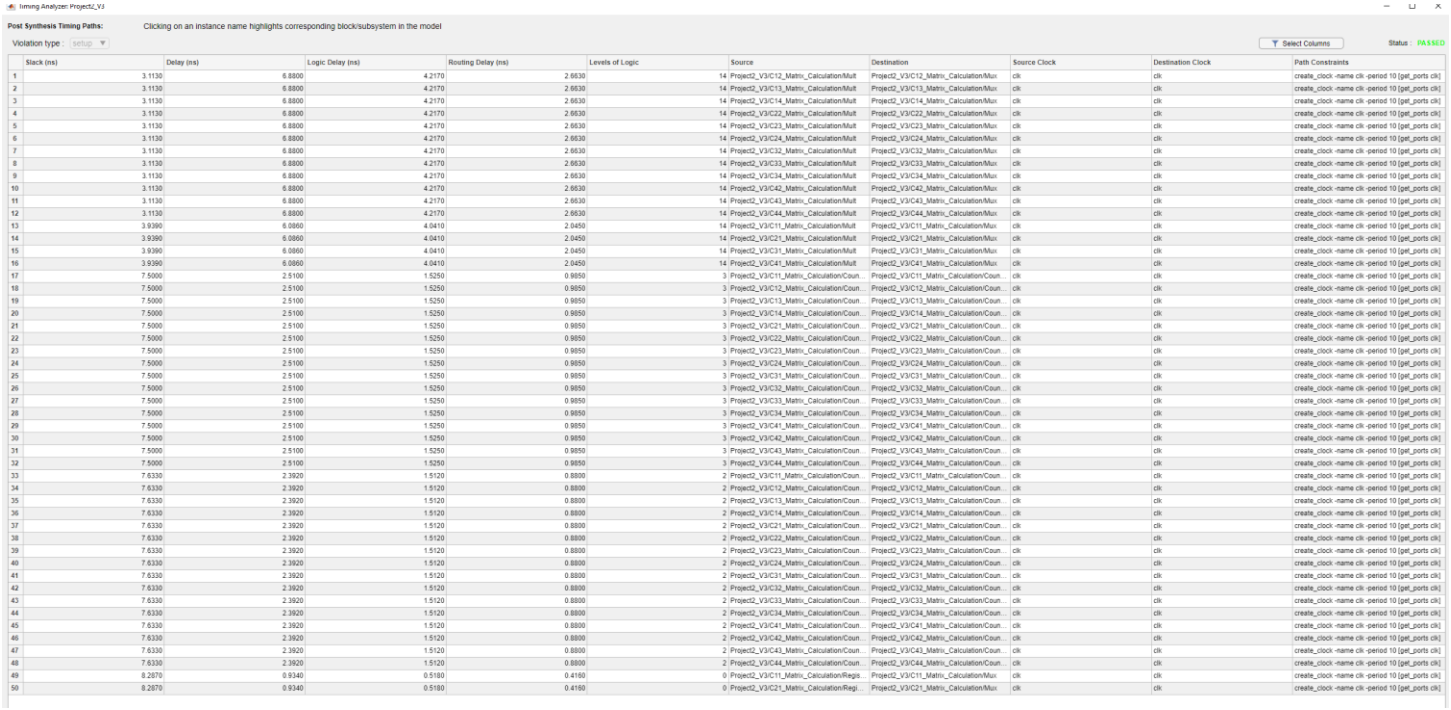


Figure 15.

Step 2: Timing Analyzer results

After set the Analyzer type to Timing, successfully generate the system, as shown in *Figure 16*.

(a) Screen capture of timing analyzer results – passing with 10ns



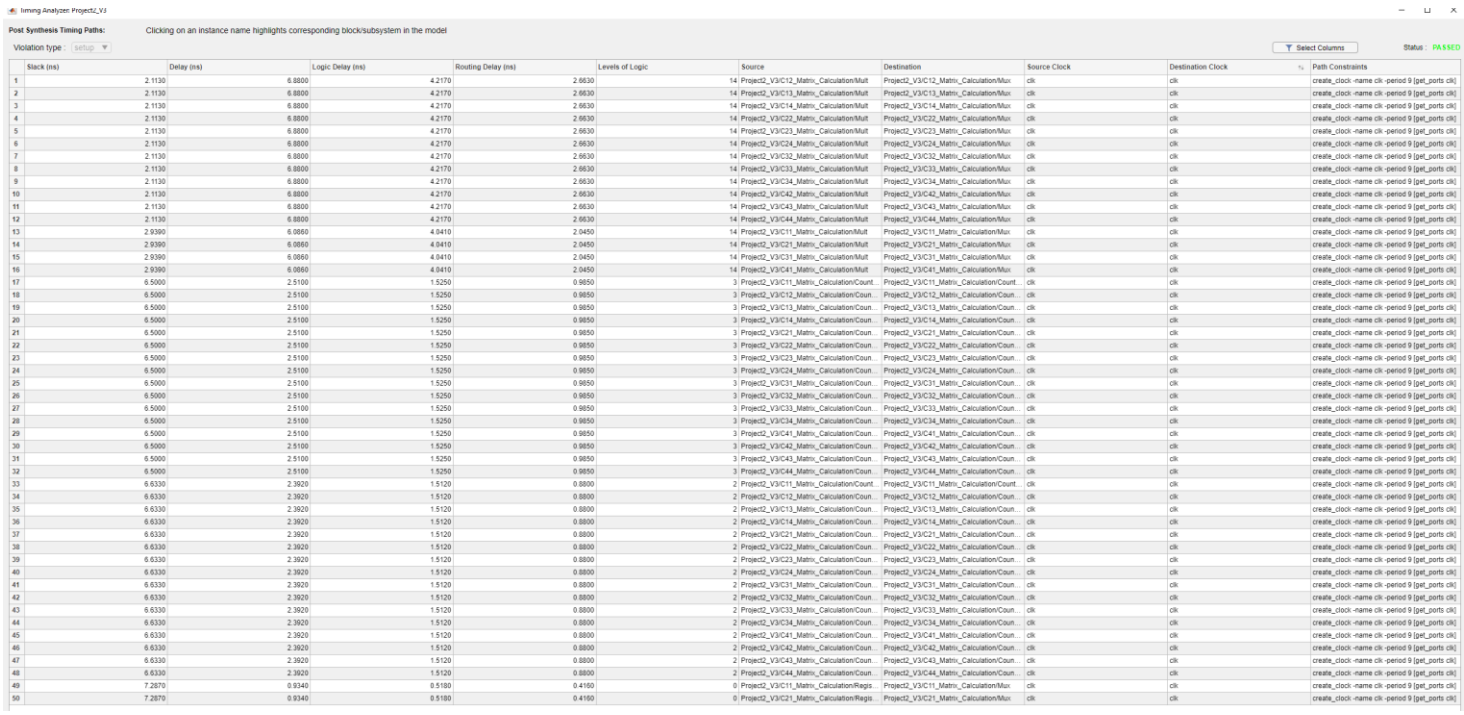
Post Synthesis Timing Paths: Clicking on an instance name highlights corresponding block/subsystem in the model

Violation type : setup | Select Columns | Status : PASSED

	Slack (ns)	Delay (ns)	Logic Delay (ns)	Routing Delay (ns)	Levels of Logic	Source	Destination	Source Clock	Destination Clock	Path Constraints
1	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C12_Matrix_Calculation/Mult	Project2_V3/C12_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
2	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C13_Matrix_Calculation/Mult	Project2_V3/C13_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
3	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C14_Matrix_Calculation/Mult	Project2_V3/C14_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
4	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C22_Matrix_Calculation/Mult	Project2_V3/C22_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
5	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C23_Matrix_Calculation/Mult	Project2_V3/C23_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
6	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C24_Matrix_Calculation/Mult	Project2_V3/C24_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
7	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C32_Matrix_Calculation/Mult	Project2_V3/C32_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
8	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C33_Matrix_Calculation/Mult	Project2_V3/C33_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
9	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C34_Matrix_Calculation/Mult	Project2_V3/C34_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
10	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C42_Matrix_Calculation/Mult	Project2_V3/C42_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
11	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C43_Matrix_Calculation/Mult	Project2_V3/C43_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
12	3.1130	6.8800	4.2170	2.6630	14	Project2_V3/C44_Matrix_Calculation/Mult	Project2_V3/C44_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
13	3.9390	6.0860	4.0410	2.0450	14	Project2_V3/C11_Matrix_Calculation/Mult	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
14	3.9390	6.0860	4.0410	2.0450	14	Project2_V3/C21_Matrix_Calculation/Mult	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
15	3.9390	6.0860	4.0410	2.0450	14	Project2_V3/C31_Matrix_Calculation/Mult	Project2_V3/C31_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
16	3.9390	6.0860	4.0410	2.0450	14	Project2_V3/C41_Matrix_Calculation/Mult	Project2_V3/C41_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
17	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C11_Matrix_Calculation/Coun...	Project2_V3/C11_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
18	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
19	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
20	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
21	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
22	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
23	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
24	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
25	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
26	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
27	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
28	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
29	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
30	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
31	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
32	7.5000	2.5100	1.5250	0.9850	3	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
33	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C11_Matrix_Calculation/Coun...	Project2_V3/C11_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
34	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
35	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
36	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
37	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
38	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
39	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
40	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
41	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
42	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
43	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
44	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
45	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
46	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
47	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
48	7.6330	2.3920	1.5120	0.8800	2	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 10 [get_ports clk]
49	8.2870	0.9340	0.5180	0.4160	0	Project2_V3/C11_Matrix_Calculation/Regis...	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]
50	8.2870	0.9340	0.5180	0.4160	0	Project2_V3/C21_Matrix_Calculation/Regi...	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 10 [get_ports clk]

Figure 16.

(b) Screen capture of timing analyzer results – passing with 9ns



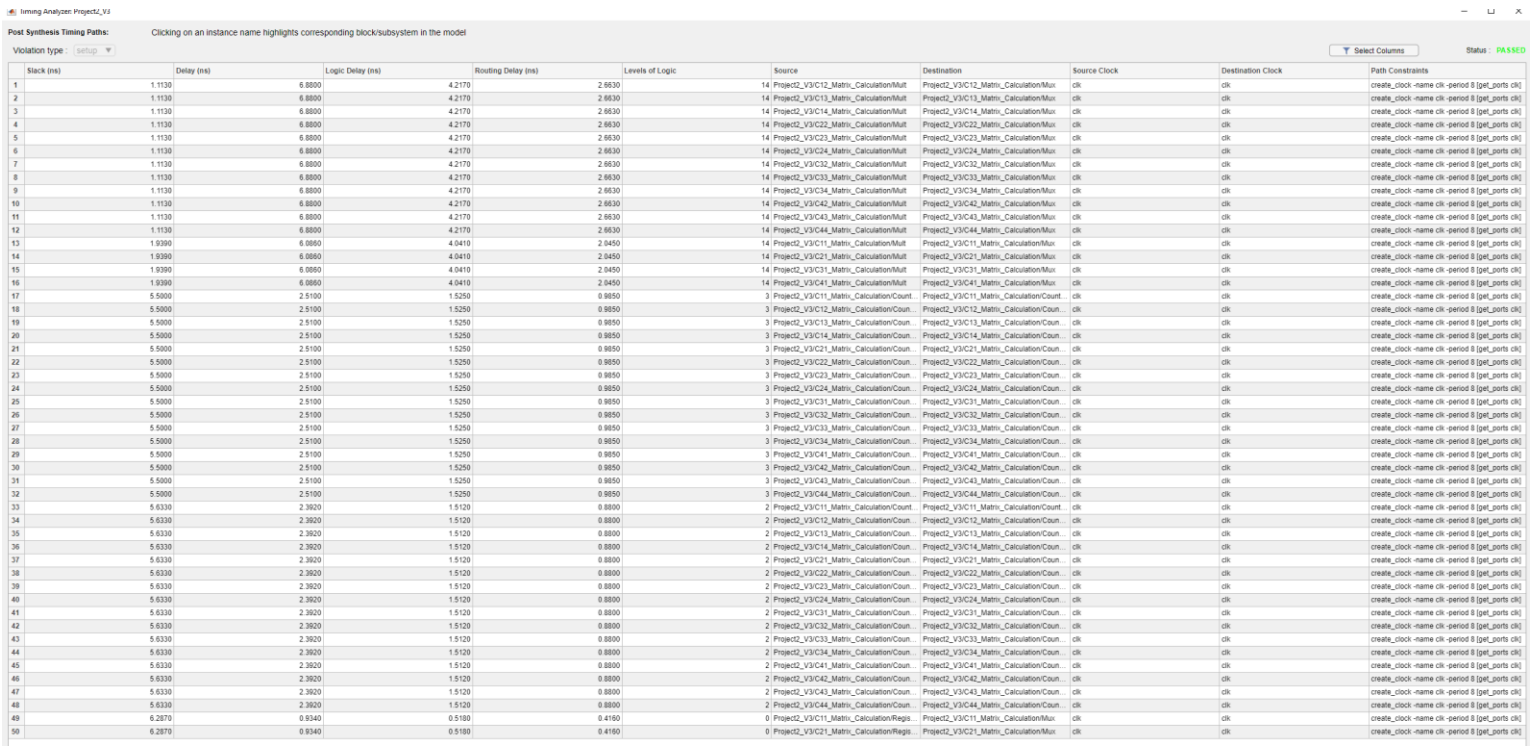
Post Synthesis Timing Paths: Clicking on an instance name highlights corresponding block/subsystem in the model

Violation type : setup | Select Columns | Status : PASSED

	Slack (ns)	Delay (ns)	Logic Delay (ns)	Routing Delay (ns)	Levels of Logic	Source	Destination	Source Clock	Destination Clock	Path Constraints
1	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C12_Matrix_Calculation/Mult	Project2_V3/C12_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
2	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C13_Matrix_Calculation/Mult	Project2_V3/C13_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
3	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C14_Matrix_Calculation/Mult	Project2_V3/C14_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
4	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C22_Matrix_Calculation/Mult	Project2_V3/C22_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
5	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C23_Matrix_Calculation/Mult	Project2_V3/C23_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
6	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C24_Matrix_Calculation/Mult	Project2_V3/C24_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
7	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C32_Matrix_Calculation/Mult	Project2_V3/C32_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
8	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C33_Matrix_Calculation/Mult	Project2_V3/C33_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
9	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C34_Matrix_Calculation/Mult	Project2_V3/C34_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
10	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C42_Matrix_Calculation/Mult	Project2_V3/C42_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
11	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C43_Matrix_Calculation/Mult	Project2_V3/C43_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
12	2.1130	6.8800	4.2170	2.6630	14	Project2_V3/C44_Matrix_Calculation/Mult	Project2_V3/C44_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
13	2.9390	6.0860	4.0410	2.0450	14	Project2_V3/C11_Matrix_Calculation/Mult	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
14	2.9390	6.0860	4.0410	2.0450	14	Project2_V3/C21_Matrix_Calculation/Mult	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
15	2.9390	6.0860	4.0410	2.0450	14	Project2_V3/C31_Matrix_Calculation/Mult	Project2_V3/C31_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
16	2.9390	6.0860	4.0410	2.0450	14	Project2_V3/C41_Matrix_Calculation/Mult	Project2_V3/C41_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
17	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
18	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
19	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
20	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
21	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
22	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
23	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
24	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
25	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
26	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
27	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
28	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
29	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
30	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
31	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
32	6.5000	2.5100	1.5250	0.9850	3	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
33	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
34	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
35	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
36	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
37	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
38	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
39	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
40	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
41	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
42	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
43	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
44	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
45	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
46	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
47	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
48	6.6330	2.3920	1.5120	0.8800	2	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 9 [get_ports clk]
49	7.2870	0.9340	0.5180	0.4160	0	Project2_V3/C11_Matrix_Calculation/Regis...	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]
50	7.2870	0.9340	0.5180	0.4160	0	Project2_V3/C21_Matrix_Calculation/Regis...	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 9 [get_ports clk]

Figure 17.

(c) Screen capture of timing analyzer results – passing with 8ns



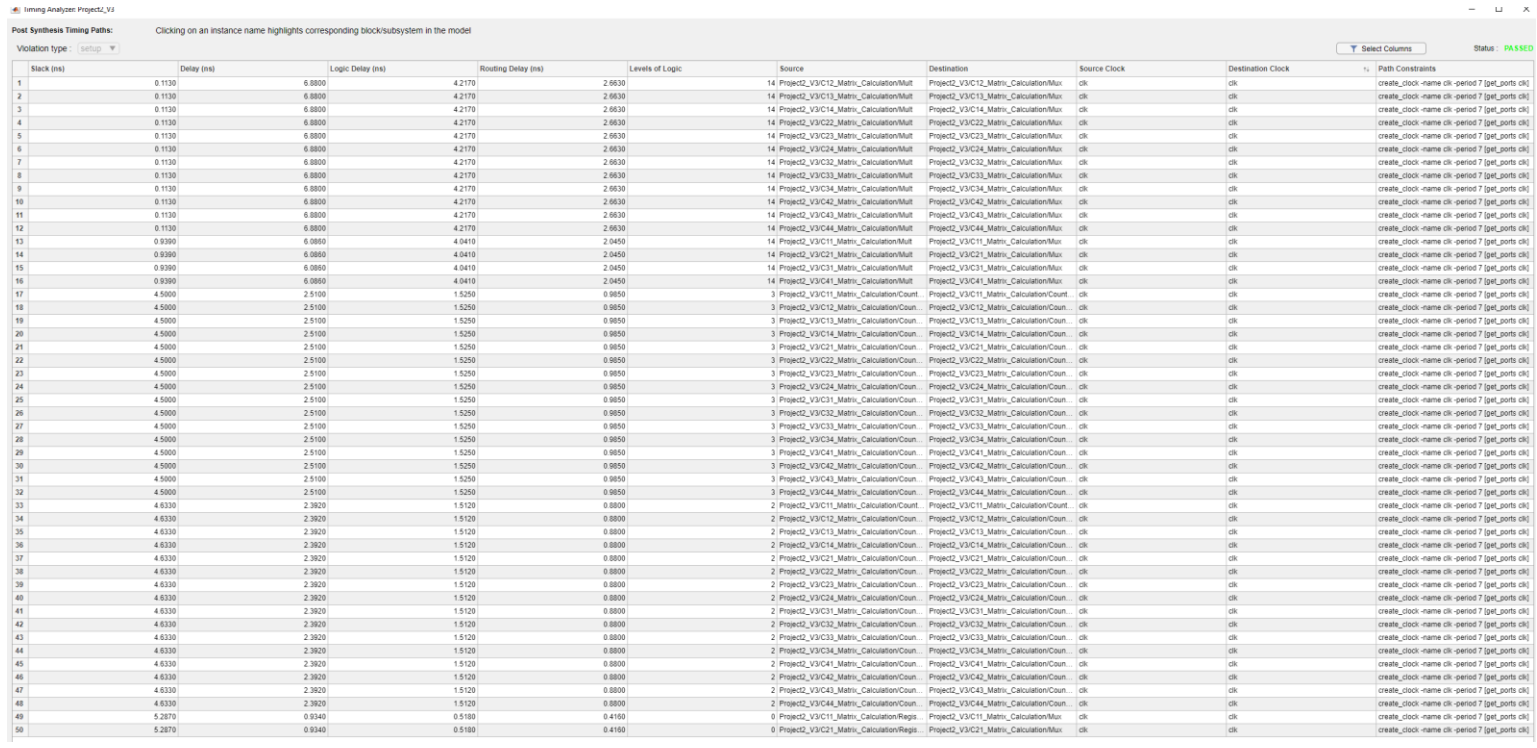
Post Synthesis Timing Paths: Clicking on an instance name highlights corresponding block/subsystem in the model

Violation type : setup — Select Columns — Status : PASSED

	Slack (ns)	Delay (ns)	Logic Delay (ns)	Routing Delay (ns)	Levels of Logic	Source	Destination	Source Clock	Destination Clock	Path Constraints
1	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C12_Matrix_Calculation/Mult	Project2_V3/C12_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
2	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C13_Matrix_Calculation/Mult	Project2_V3/C13_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
3	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C14_Matrix_Calculation/Mult	Project2_V3/C14_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
4	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C22_Matrix_Calculation/Mult	Project2_V3/C22_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
5	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C23_Matrix_Calculation/Mult	Project2_V3/C23_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
6	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C24_Matrix_Calculation/Mult	Project2_V3/C24_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
7	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C32_Matrix_Calculation/Mult	Project2_V3/C32_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
8	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C33_Matrix_Calculation/Mult	Project2_V3/C33_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
9	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C34_Matrix_Calculation/Mult	Project2_V3/C34_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
10	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C42_Matrix_Calculation/Mult	Project2_V3/C42_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
11	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C43_Matrix_Calculation/Mult	Project2_V3/C43_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
12	1.1130	6.8800	4.2170	2.6630	14	Project2_V3/C44_Matrix_Calculation/Mult	Project2_V3/C44_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
13	1.9390	6.0860	4.0410	2.0450	14	Project2_V3/C11_Matrix_Calculation/Mult	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
14	1.9390	6.0860	4.0410	2.0450	14	Project2_V3/C21_Matrix_Calculation/Mult	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
15	1.9390	6.0860	4.0410	2.0450	14	Project2_V3/C31_Matrix_Calculation/Mult	Project2_V3/C31_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
16	1.9390	6.0860	4.0410	2.0450	14	Project2_V3/C41_Matrix_Calculation/Mult	Project2_V3/C41_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
17	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
18	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
19	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
20	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
21	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
22	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
23	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
24	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
25	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
26	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
27	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
28	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
29	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
30	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
31	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
32	5.5000	2.5100	1.5250	0.9850	3	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
33	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
34	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
35	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
36	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
37	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
38	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
39	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
40	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
41	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
42	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
43	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
44	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
45	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
46	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
47	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
48	5.6330	2.3920	1.5120	0.8800	2	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 8 [get_ports clk]
49	6.2870	0.9340	0.5180	0.4160	0	Project2_V3/C11_Matrix_Calculation/Regis...	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]
50	6.2870	0.9340	0.5180	0.4160	0	Project2_V3/C21_Matrix_Calculation/Regis...	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 8 [get_ports clk]

Figure 18.

(d) Screen capture of timing analyzer results – passing with 7ns



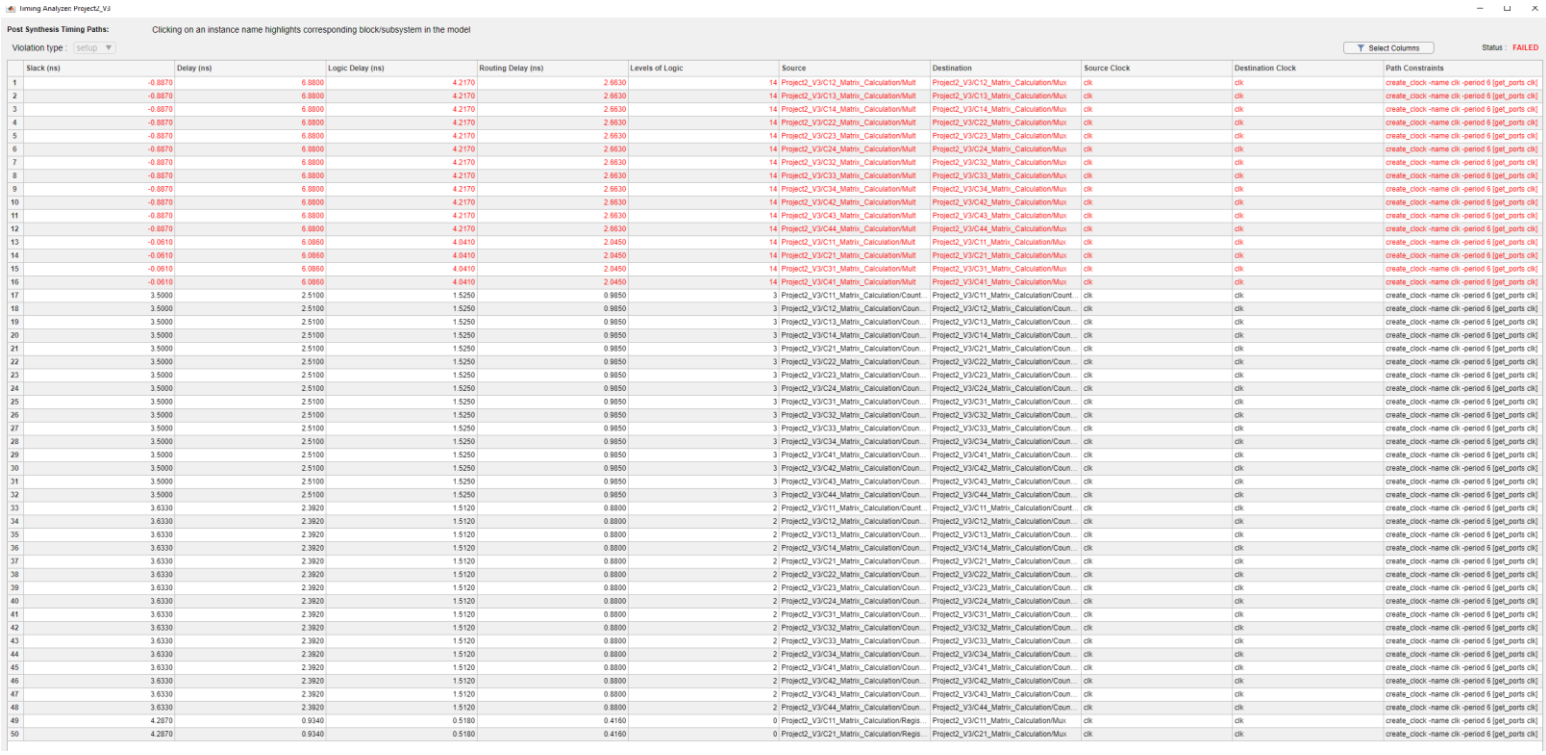
Post Synthesis Timing Paths: Clicking on an instance name highlights corresponding block/subsystem in the model

Violation type : setup — Select Columns — Status : PASSED

	Slack (ns)	Delay (ns)	Logic Delay (ns)	Routing Delay (ns)	Levels of Logic	Source	Destination	Source Clock	Destination Clock	Path Constraints
1	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C12_Matrix_Calculation/Mult	Project2_V3/C12_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
2	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C13_Matrix_Calculation/Mult	Project2_V3/C13_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
3	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C14_Matrix_Calculation/Mult	Project2_V3/C14_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
4	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C22_Matrix_Calculation/Mult	Project2_V3/C22_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
5	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C23_Matrix_Calculation/Mult	Project2_V3/C23_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
6	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C24_Matrix_Calculation/Mult	Project2_V3/C24_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
7	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C32_Matrix_Calculation/Mult	Project2_V3/C32_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
8	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C33_Matrix_Calculation/Mult	Project2_V3/C33_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
9	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C34_Matrix_Calculation/Mult	Project2_V3/C34_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
10	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C42_Matrix_Calculation/Mult	Project2_V3/C42_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
11	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C43_Matrix_Calculation/Mult	Project2_V3/C43_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
12	0.1130	6.8800	4.2170	2.6630	14	Project2_V3/C44_Matrix_Calculation/Mult	Project2_V3/C44_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
13	0.9390	6.0860	4.0410	2.0450	14	Project2_V3/C11_Matrix_Calculation/Mult	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
14	0.9390	6.0860	4.0410	2.0450	14	Project2_V3/C21_Matrix_Calculation/Mult	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
15	0.9390	6.0860	4.0410	2.0450	14	Project2_V3/C31_Matrix_Calculation/Mult	Project2_V3/C31_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
16	0.9390	6.0860	4.0410	2.0450	14	Project2_V3/C41_Matrix_Calculation/Mult	Project2_V3/C41_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
17	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
18	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
19	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
20	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
21	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
22	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
23	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
24	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
25	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
26	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
27	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
28	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
29	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
30	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
31	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
32	4.5000	2.5100	1.5250	0.9850	3	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
33	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
34	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
35	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
36	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
37	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
38	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
39	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
40	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
41	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
42	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
43	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
44	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
45	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
46	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
47	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
48	4.6330	2.3920	1.5120	0.8800	2	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 7 [get_ports clk]
49	5.2870	0.9340	0.5180	0.4160	0	Project2_V3/C11_Matrix_Calculation/Regis...	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]
50	5.2870	0.9340	0.5180	0.4160	0	Project2_V3/C21_Matrix_Calculation/Regis...	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 7 [get_ports clk]

Figure 19.

(e) Screen capture of timing analyzer results – failed with 6ns



	Slack (ns)	Delay (ns)	Logic Delay (ns)	Routing Delay (ns)	Levels of Logic	Source	Destination	Source Clock	Destination Clock	Path Constraints
1	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C12_Matrix_Calculation/Mult	Project2_V3/C12_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
2	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C13_Matrix_Calculation/Mult	Project2_V3/C13_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
3	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C14_Matrix_Calculation/Mult	Project2_V3/C14_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
4	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C22_Matrix_Calculation/Mult	Project2_V3/C22_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
5	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C23_Matrix_Calculation/Mult	Project2_V3/C23_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
6	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C24_Matrix_Calculation/Mult	Project2_V3/C24_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
7	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C32_Matrix_Calculation/Mult	Project2_V3/C32_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
8	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C33_Matrix_Calculation/Mult	Project2_V3/C33_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
9	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C34_Matrix_Calculation/Mult	Project2_V3/C34_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
10	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C42_Matrix_Calculation/Mult	Project2_V3/C42_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
11	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C43_Matrix_Calculation/Mult	Project2_V3/C43_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
12	-0.8870	6.8800	4.2170	2.6630	14	Project2_V3/C44_Matrix_Calculation/Mult	Project2_V3/C44_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
13	-0.0610	6.0860	4.0410	2.0450	14	Project2_V3/C11_Matrix_Calculation/Mult	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
14	-0.0610	6.0860	4.0410	2.0450	14	Project2_V3/C21_Matrix_Calculation/Mult	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
15	-0.0610	6.0860	4.0410	2.0450	14	Project2_V3/C31_Matrix_Calculation/Mult	Project2_V3/C31_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
16	-0.0610	6.0860	4.0410	2.0450	14	Project2_V3/C41_Matrix_Calculation/Mult	Project2_V3/C41_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
17	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
18	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
19	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
20	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
21	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
22	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
23	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
24	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
25	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
26	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
27	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
28	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
29	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
30	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
31	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
32	3.5000	2.5100	1.5250	0.9850	3	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
33	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C11_Matrix_Calculation/Count...	Project2_V3/C11_Matrix_Calculation/Count...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
34	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C12_Matrix_Calculation/Coun...	Project2_V3/C12_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
35	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C13_Matrix_Calculation/Coun...	Project2_V3/C13_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
36	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C14_Matrix_Calculation/Coun...	Project2_V3/C14_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
37	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C21_Matrix_Calculation/Coun...	Project2_V3/C21_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
38	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C22_Matrix_Calculation/Coun...	Project2_V3/C22_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
39	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C23_Matrix_Calculation/Coun...	Project2_V3/C23_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
40	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C24_Matrix_Calculation/Coun...	Project2_V3/C24_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
41	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C31_Matrix_Calculation/Coun...	Project2_V3/C31_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
42	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C32_Matrix_Calculation/Coun...	Project2_V3/C32_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
43	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C33_Matrix_Calculation/Coun...	Project2_V3/C33_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
44	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C34_Matrix_Calculation/Coun...	Project2_V3/C34_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
45	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C41_Matrix_Calculation/Coun...	Project2_V3/C41_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
46	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C42_Matrix_Calculation/Coun...	Project2_V3/C42_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
47	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C43_Matrix_Calculation/Coun...	Project2_V3/C43_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
48	3.6330	2.3920	1.5120	0.8800	2	Project2_V3/C44_Matrix_Calculation/Coun...	Project2_V3/C44_Matrix_Calculation/Coun...	clk	clk	create_clock -name clk -period 6 [get_ports clk]
49	4.2870	0.9340	0.5180	0.4160	0	Project2_V3/C11_Matrix_Calculation/Regis...	Project2_V3/C11_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]
50	4.2870	0.9340	0.5180	0.4160	0	Project2_V3/C21_Matrix_Calculation/Regis...	Project2_V3/C21_Matrix_Calculation/Mux	clk	clk	create_clock -name clk -period 6 [get_ports clk]

Figure 20.

Testing Methodology:

Step 1: Matrix multiplication testing

I also test other value into my system, and always get the correct results as shown in *Figure 21 and Figure 22*.

(a) Screen capture of different input results test 1

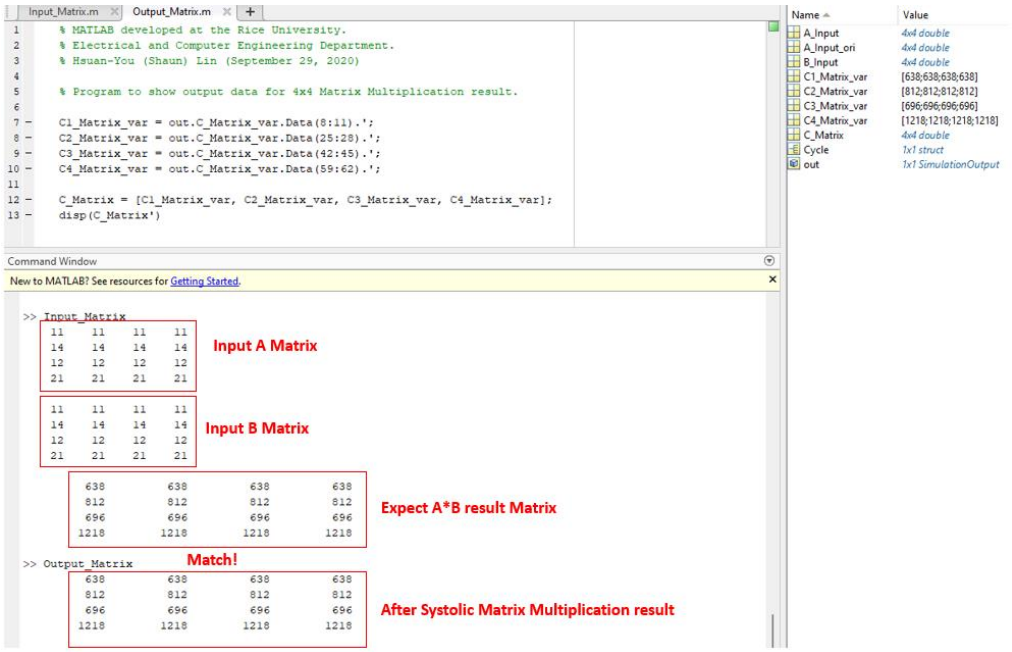


Figure 21.

(b) Screen capture of different input results test 2

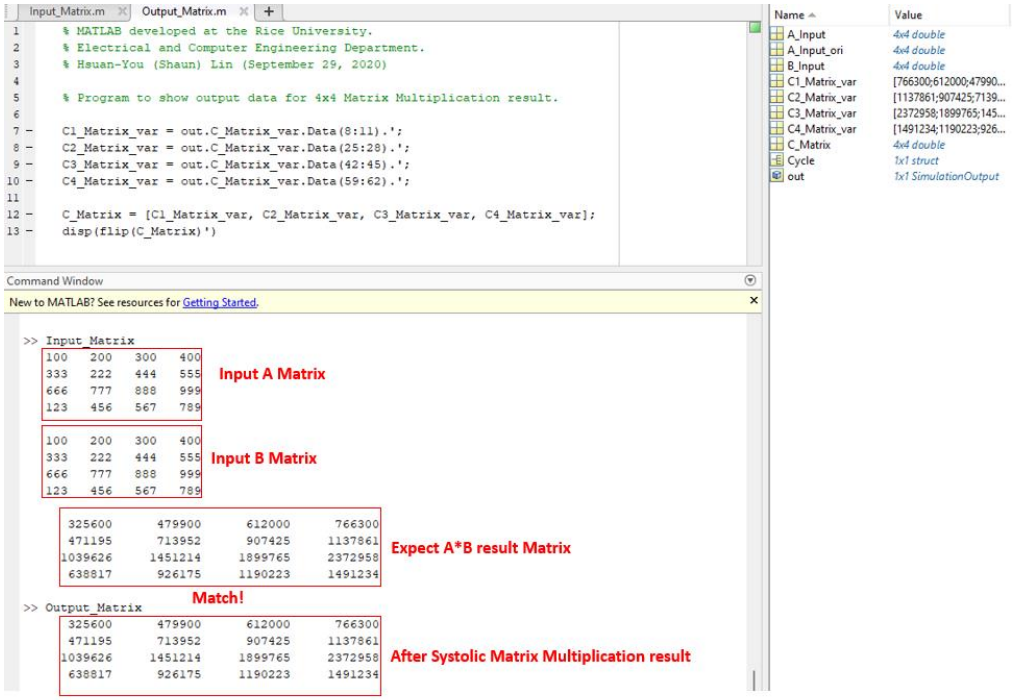


Figure 22.