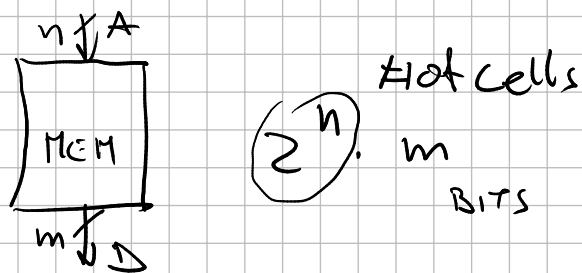
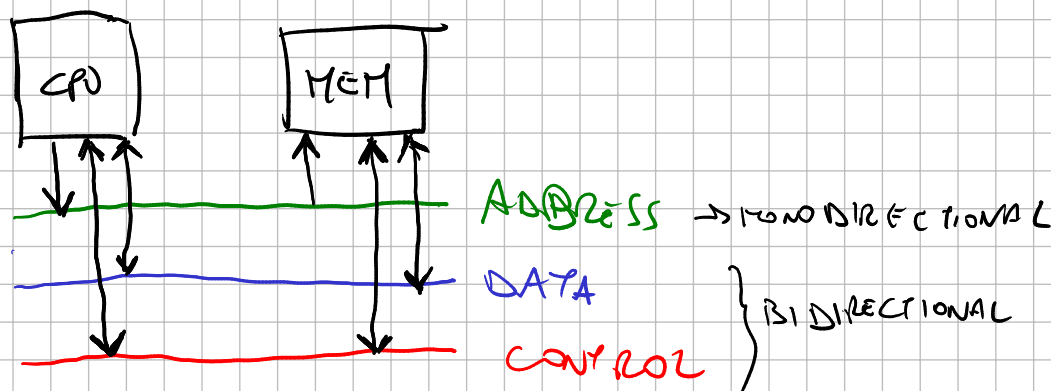
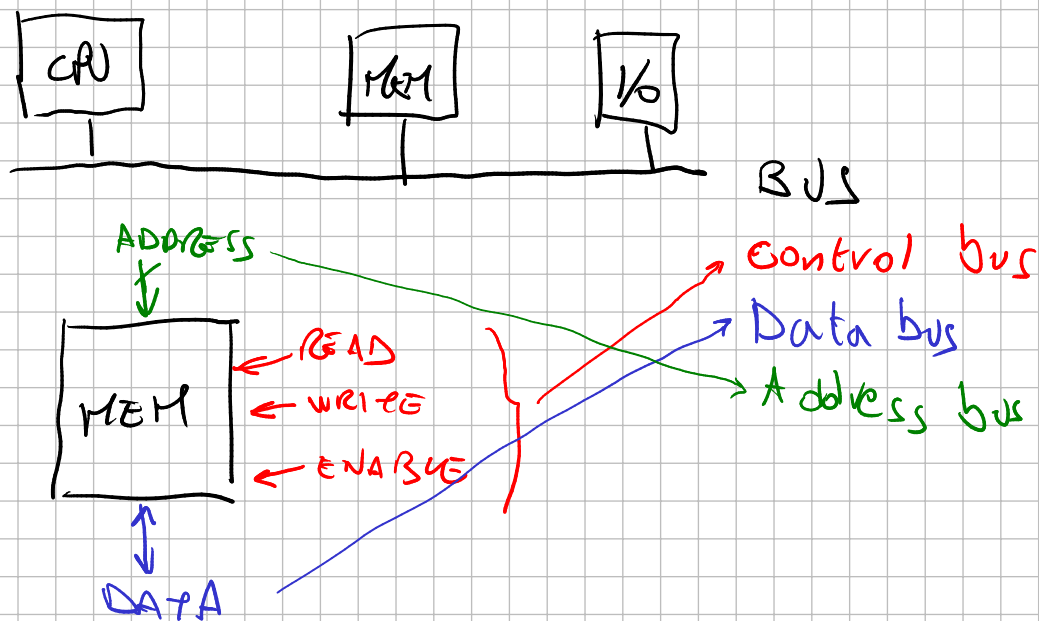


PARALLELISM



8086

A BUS 20 bits
D BUS 16 bits
SHARED based on time

t

8088

A BUS 20 bits

D BUS 8 bits \rightarrow compatible to older components

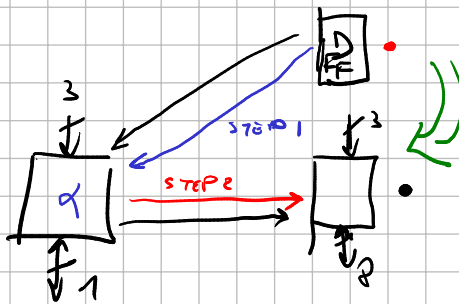
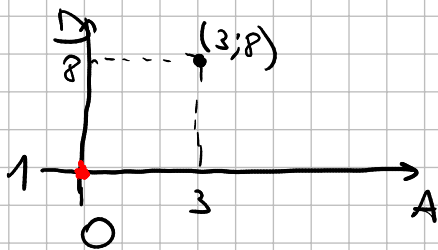
Parallelism \Leftrightarrow Computation!

8086 parallelism: 16 bits

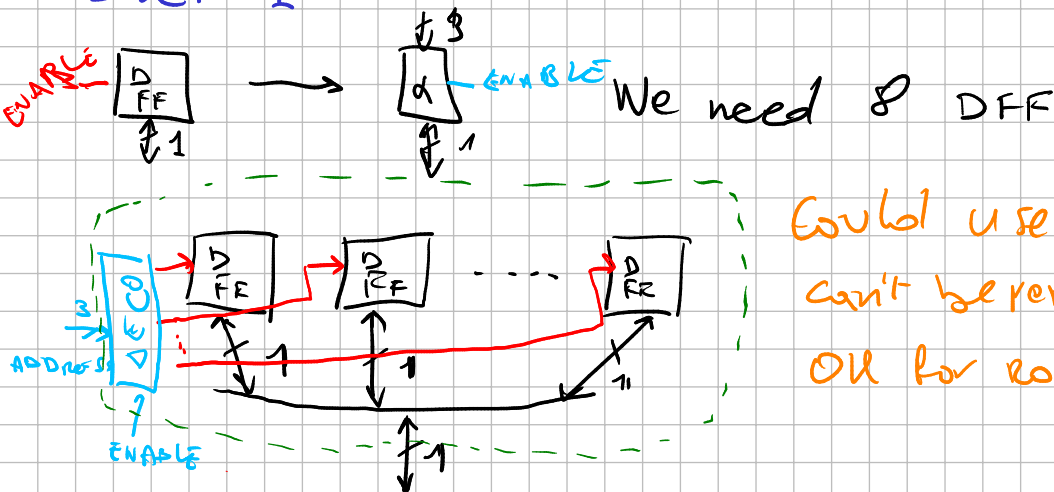
(P.C.) program counter
register

16 bits in 8086

STATIC MEMORY \rightarrow LARGE MEMORY DESIGN

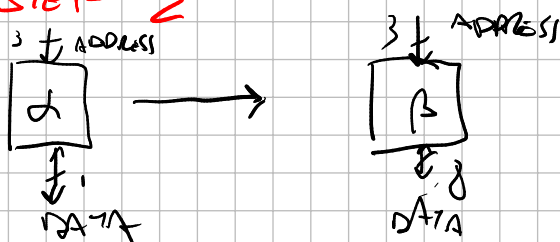


STEP 1

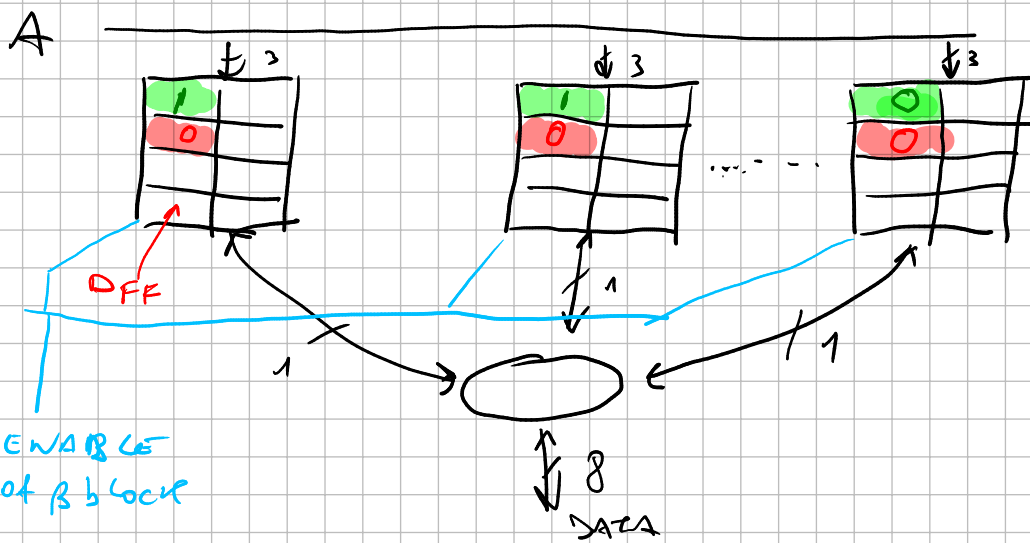
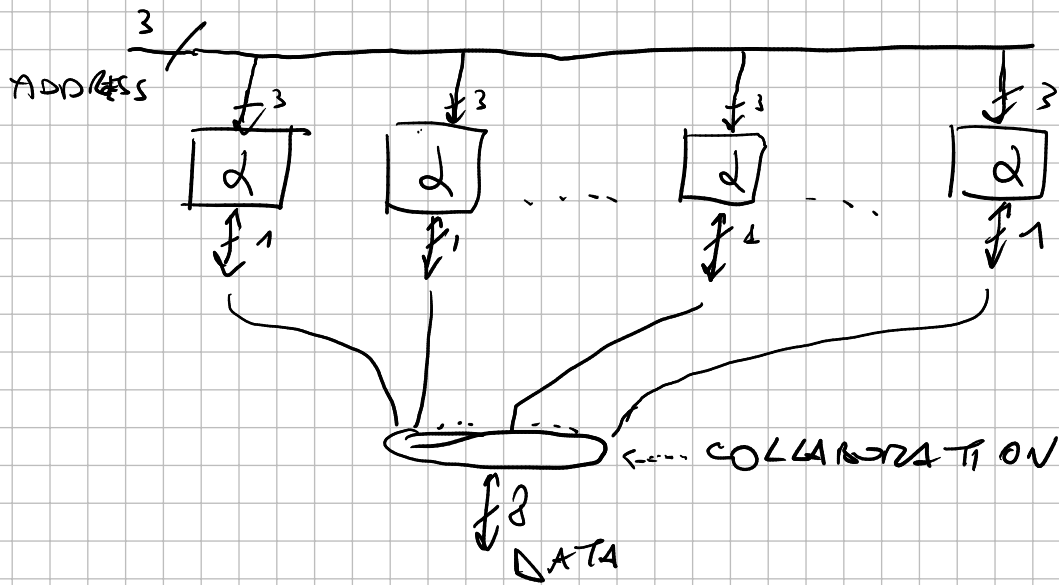


Could use a MUX but it
can't be reversed (not bi-directional)
OK for read, but not for write

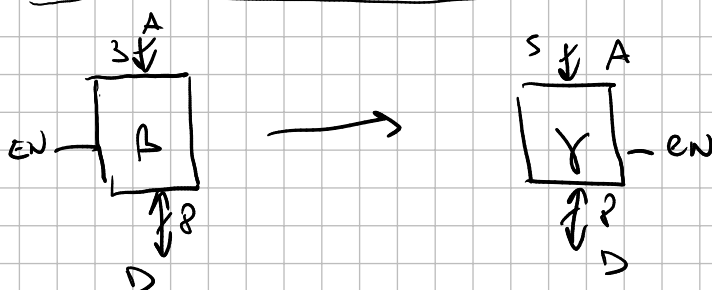
STEP 2

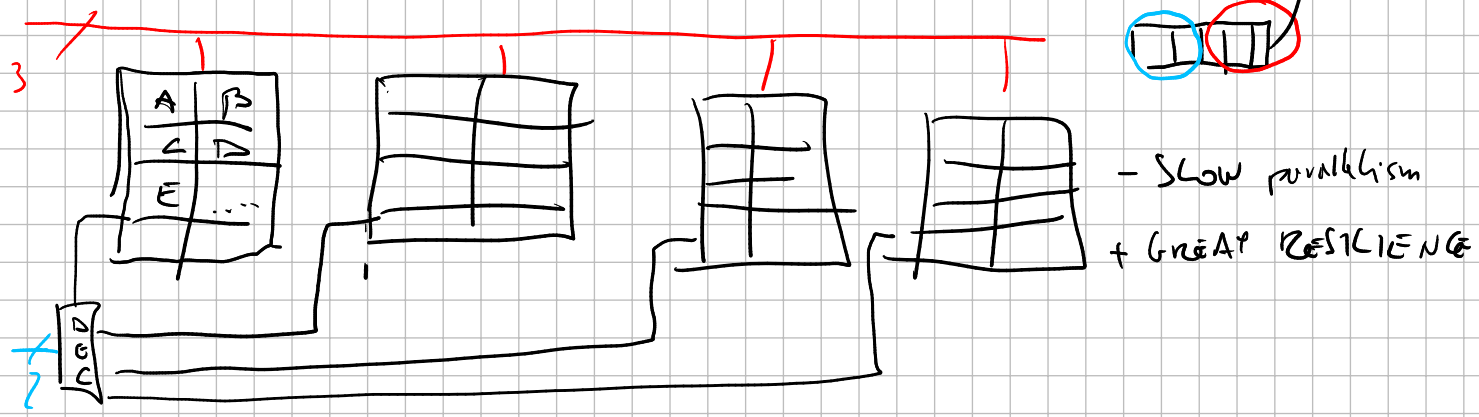
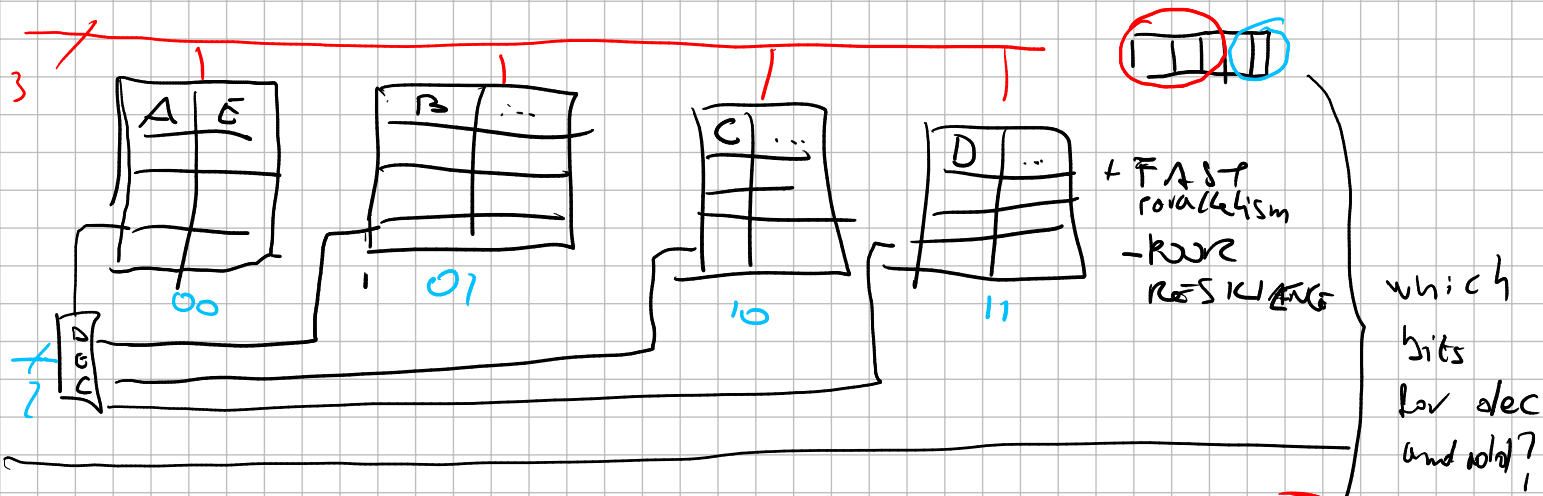
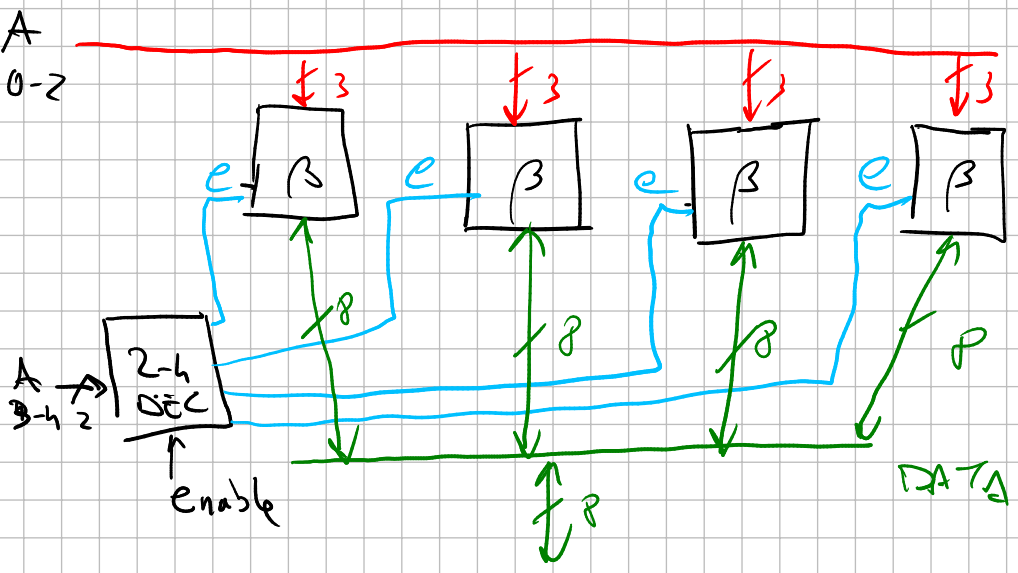


We need 8 blocks

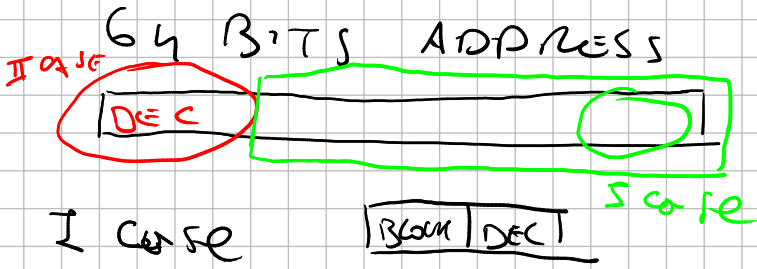


ADDR	8 BITS
0 0 0	1 1 0 0 . . . 0
0 0 1	0 1 . . . 1
0 1 0	0 0 . . . 0





00	0000	→	A
00	001	→	B
00	010	→	C
00	011	→	D
00	100	→	E
...	...	→	...



I case

BLOCK	DEC
-------	-----

II case

DEC	BLOCK
-----	-------



0	2	4	6	8	10
1	3	5	7	9	

ADDRESS DATA RATE