UNIVERSITY OF ENGINEERING & MANAGEMENT (UEM) KOLKATA

श्रद्धावान लभते ज्ञानम्
UEM

INDEX

LAB : Computer Organization & Architecture LAB (Hardware)

YEAR : 2nd SEMESTER 4th

EXPT. NO.	DATE	NAME OF THE EXPERIMENT	PAGE	REMARKS
1	2/2/23	Design Register Circuit-	1-6	BM 2/2
2	16/2/23	Adder-Subtractor Composite Circuit	7-9	
4	15/3/23	Design for a BCD adder	10-12	23/03/23.
5	30/3/23	A) Design Composite	13-15	06/04/23
		Logic Unit Using Multiplexer		
		B) Design Composite	16-20	
		Arithmetic Unit Using		
		multiplexer		
6	13/4/23	Memory Read/write	21-23	
		operation Using RAM IC		

Aim - Implementing SISO, SIPO and PIPO shift registers.

Component Required - IC4013, connecting wire, bread board, trainer kit.

Therory:

Register - A register is a collection of flip flop. A flip-flop is used to store single bit digital data. For storing a large number of bits, the storage capacity is increased by grouping more than one flipflop. If we want to store an n-bit word we have to use an n-bit register containing n number of flipflops.

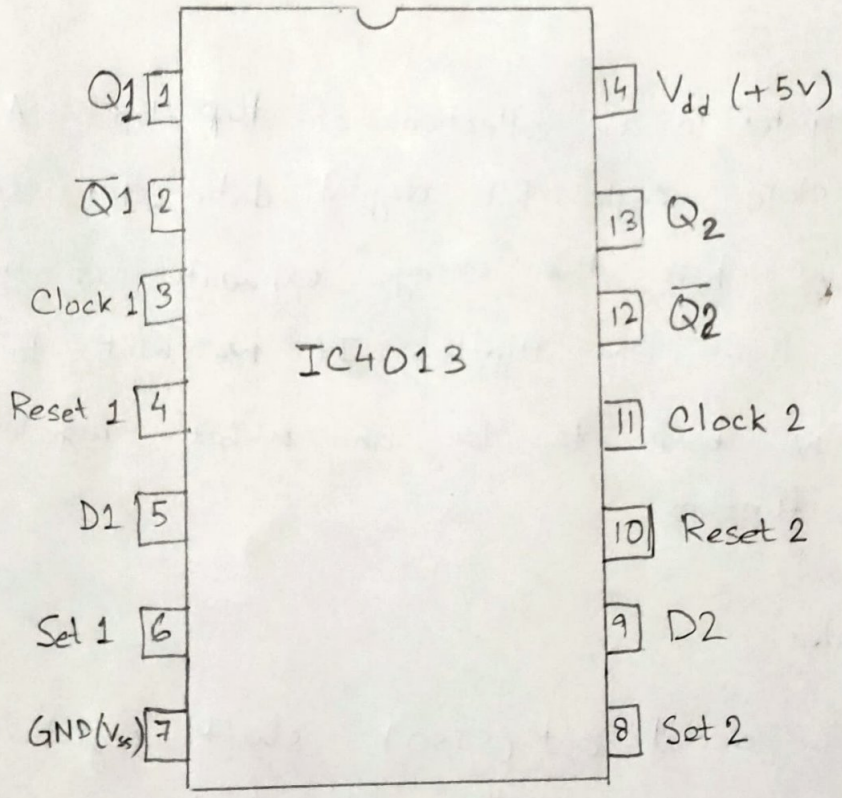
Types of Register -

SISO - Serial in serial out (SISO) shift register are kind of shift register where both data loading as well as data retrieval to / from shift register occurs in serial - mode.

SIPO - A serial in parallel out shift register is similar to the serial in, serial out shift register is that it shifts data into internal storage element and shifts data out at the serial out, data out, pin. It is different in that it makes all the internal stages available as output.

PIPO - The shift register which uses parallel input and generates parallel output is known as the parallel input parallel output (PIPO) shift register. The shift register include three connections only the PI (parallel I/P), PO (parallel O/P) & the clock signal.

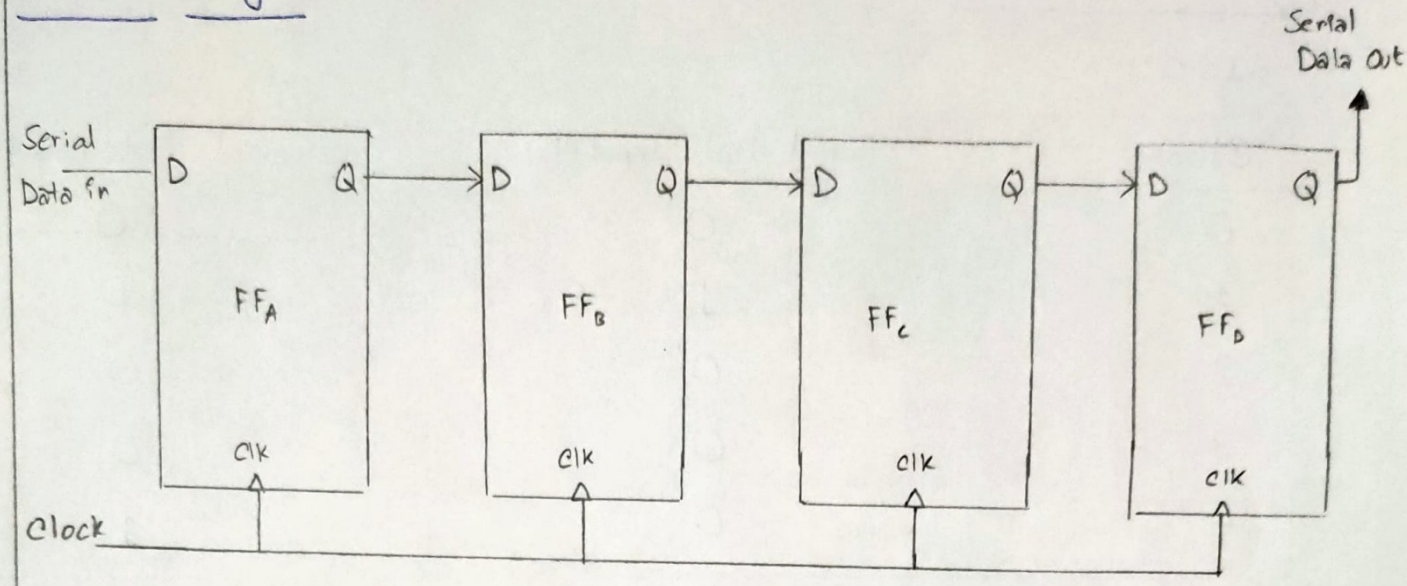
PIN DIAGRAM
(D Flipflop)



Dual D flipflop

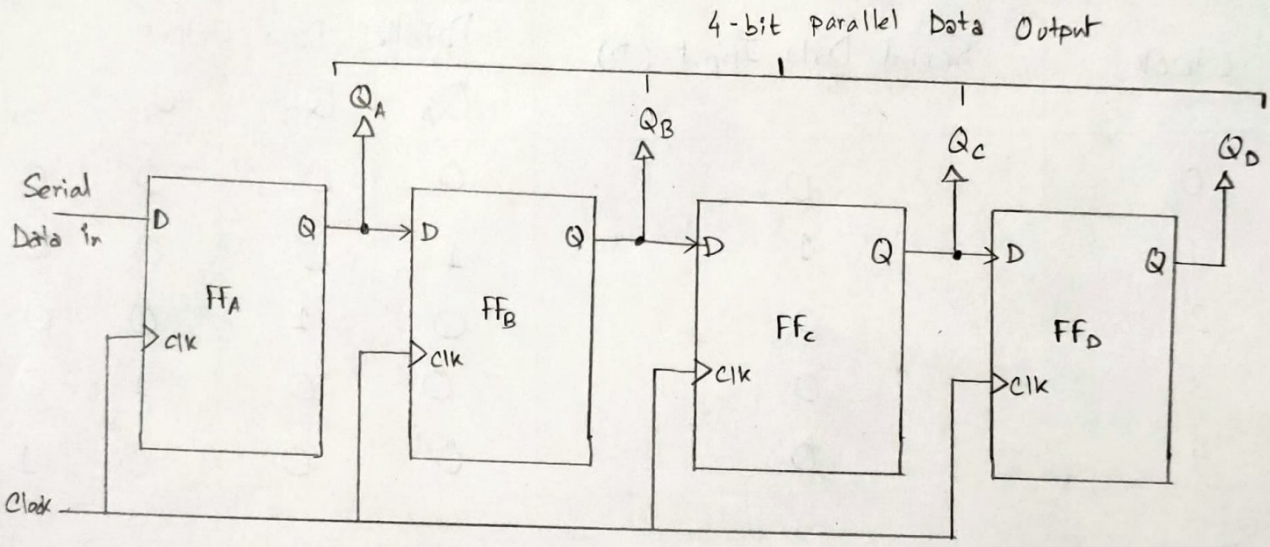
Circuit Diagram -

1)



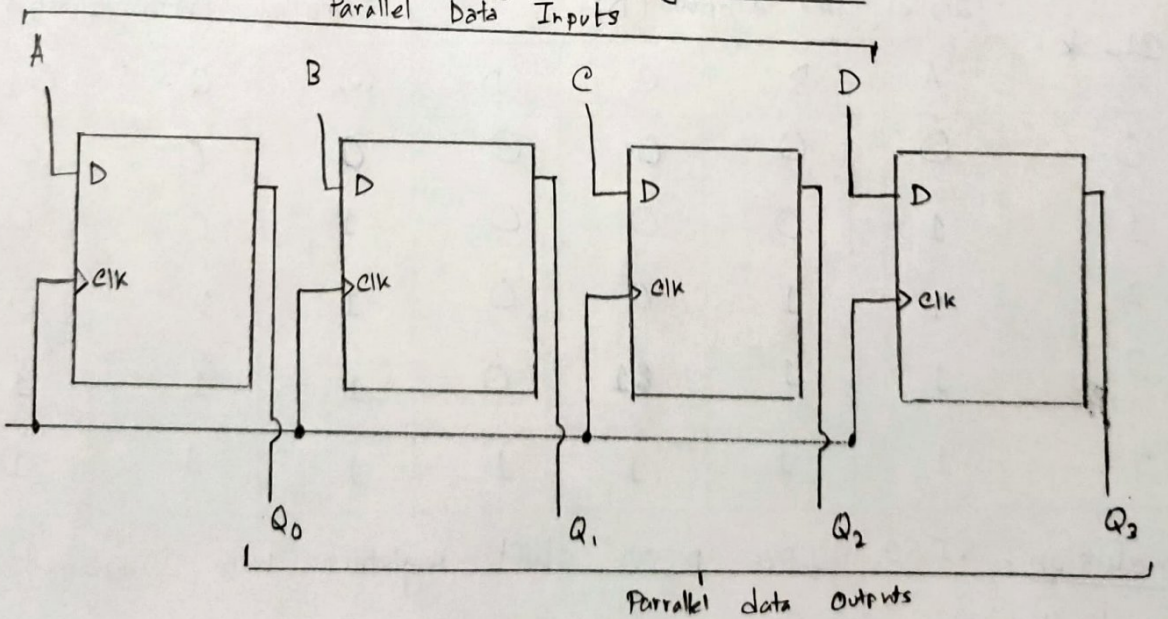
4 bit SISO register Using D - flipflop

2)



4 bit SIPO register Using D flipflop

3)



4 bit PIPO Register Using D flipflop

Observation Table:

SISO:

Clock	Serial Data Input (D)	Serial Data Output (Q)
0	0	0
1	1	0
2	0	0
3	0	0
4	0	1

SIPO:

Clock	Serial Data Input (D)	Parallel Data Output			
		Q_A	Q_B	Q_C	Q_D
0	0	0	0	0	0
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	0	0	0	0	1

PIPO:

Clock	Parallel Data Input (D)				Parallel Data Output (Q)			
	A	B	C	D	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	1	1	0	0	1	1	0	0
3	1	1	1	0	1	1	1	0
4	1	1	1	1	1	1	1	1

Conclusion: SISO, SIPO, PIPO shift registers were implemented and truth table is verified.

Objective:

To design the adder-subtractor composite circuit.

Theory:

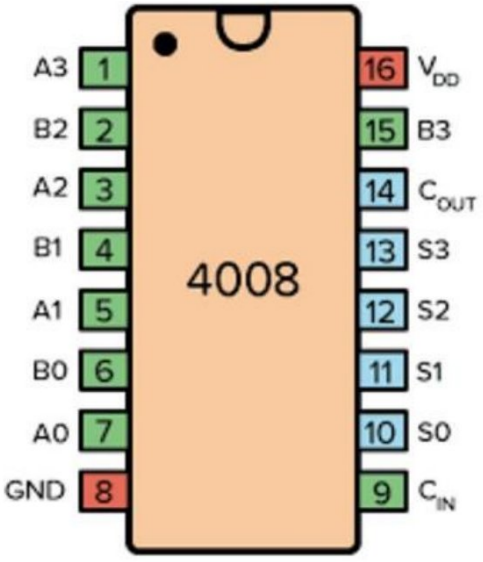
The 4-bit adder-subtractor composite circuit performs the operation of both addition and subtraction. It has two 4-bits inputs $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. The Mode Select line(M) is connected with the C_{in} of the least significant bit of the Full-adder, is used to perform the operation of addition and subtraction. The XOR gates are used as controlled inverter.

Adders are part of the arithmetic and logic unit (ALU).

Component Required:

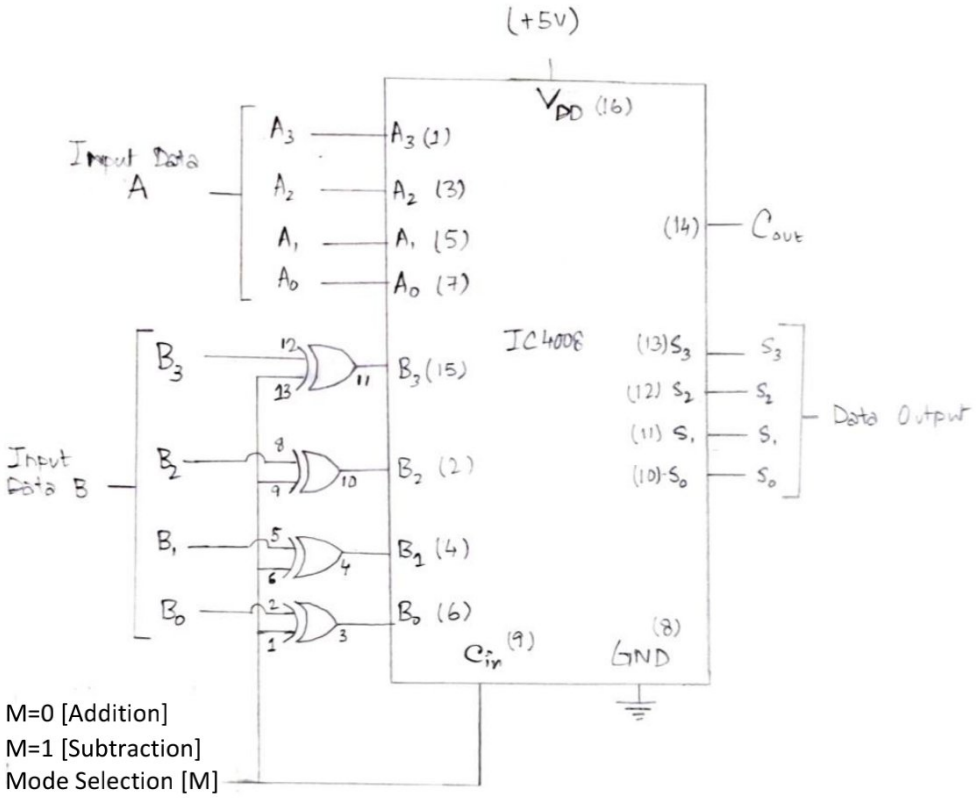
Sl No.	Item	Specification	Qty.
1	IC 4008	4-bit binary full adder	1
2	IC 4070	XOR Gate	1
3	Digital Trainer Kit	-	1
4	Breadboard	-	1
5	Wires	-	-

Pin Diagram:



Pin Diagram of 4-bit Binary Full Adder (IC4008)

Circuit Diagram:



Adder-subtractor composite circuit

Truth Table:

Mode Selection	Input (A)				Input (B)				Output (S)				
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	S_3	S_2	S_1	S_0
0	0	0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1	0	1	0	1	0	0
0	1	1	0	0	0	0	1	1	0	1	1	1	1
1	1	1	0	0	0	0	1	1	0	1	0	0	1
1	1	0	1	0	0	0	0	1	0	1	0	0	1
1	1	0	0	1	0	0	1	1	0	0	1	0	1

Conclusion:

4-bit adder and subtractor composite circuit was made and truth table was verified.

Experiment NO – CO – 04

TITLE: Design the circuit for a BCD adder

OBJECTIVE: To design the circuit for a BCD adder

THEORY:

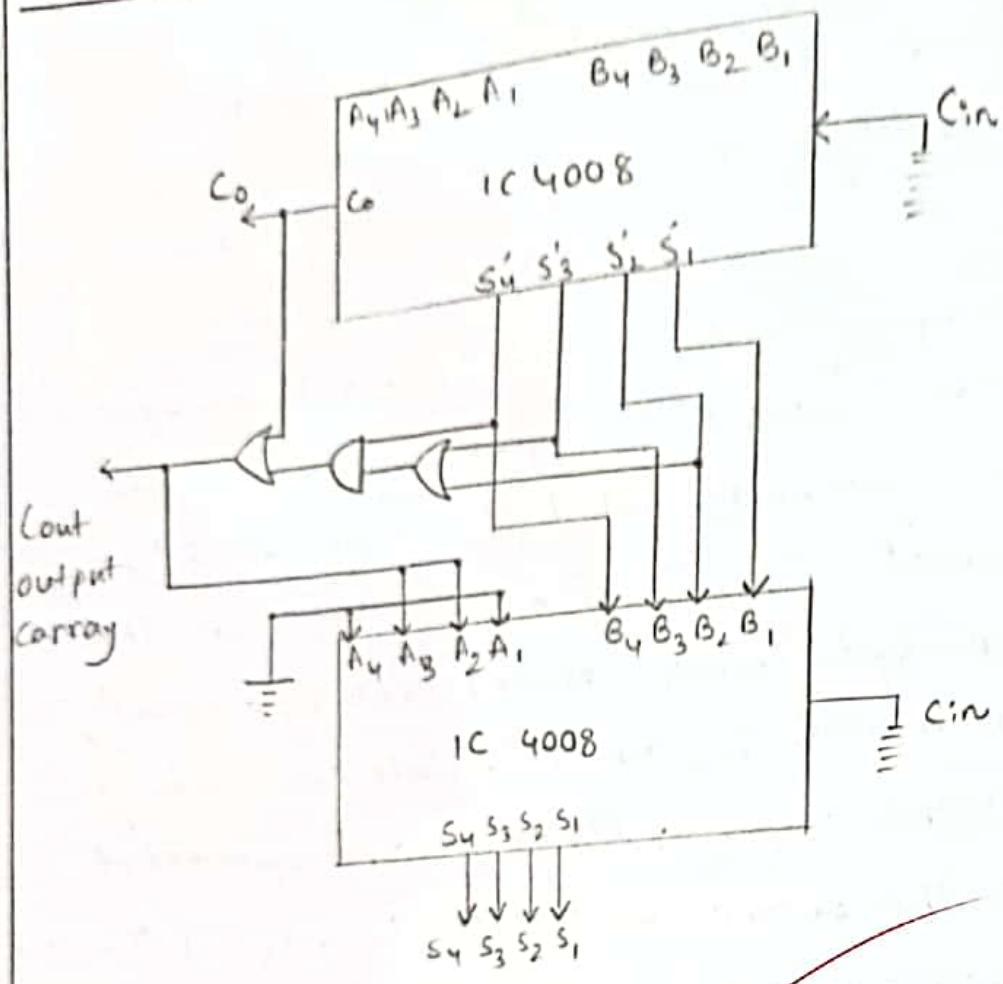
In computing and electronic systems, binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum digit which is also in BCD. This circuit includes correction logic. For sums > 9 the circuit need to add 2's compliment of 10_{10} $(0110)_2$ to the uncorrected result $(S_4\ S_3\ S_2\ S_1)$. Correction is also needed when carry out $(Cout_4)$ is generated (for numbers (16 – 19).

BCD was used in many early decimal computers.

PIN DIAGRAM

11

CIRCUIT DIAGRAM:



Truth Table:

Decimal number	Cout	S_4	S_3	S_2	S_1	Decimal number	Cout	S_4	S_3	S_2	S_1
0	0	0	0	0	0	10	1	0	0	0	0
1		0	0	0	1	11	1	0	0	0	1
2		0	0	1	0	12	1	0	0	1	0
3		0	0	1	1	13	1	0	0	1	1
4		0	1	0	0	14	1	0	1	0	0
5		0	1	0	1	15	1	0	1	0	1
6		0	1	1	0	16	1	0	1	1	0
7		0	1	1	1	17	1	0	1	1	1
8		1	0	0	0	18	1	1	0	0	0
9		1	0	0	1	19	1	1	0	0	1

K map for BCD adder:

S_3S_4 \ S_1S_2	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$$C_{out} = S_3S_4 + S_4S_2$$

INSTRUMENT & COMPONENT REQUIRED:

SL NO.	Item	Specification	Qty.
1	IC 4071	OR Gate	1
2	IC 4081	AND Gate	1
3	IC 4008	4bit binary full adder	2
4	Trainer kit	–	1
5	Breadboard	–	1
6	Wires	–	as required

VERIFICATION TABLE:

Serial no	Input (A)				Input (B)				Output (S)			
	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	S_4	S_3	S_2	S_1
1	0	0	0	0	1	0	0	1	1	0	0	1
2	0	1	1	1	0	1	0	0	0	0	0	1
3	0	0	0	1	0	0	0	0	0	0	0	1
4	0	0	0	1	0	0	0	1	0	0	1	0
5	0	1	0	1	0	0	1	1	1	0	0	0
6	1	0	0	0	0	1	0	1	0	0	1	1

Conclusion

By this experiment we are able to build the bcd adder.

Experiment NO - CO-05(A)

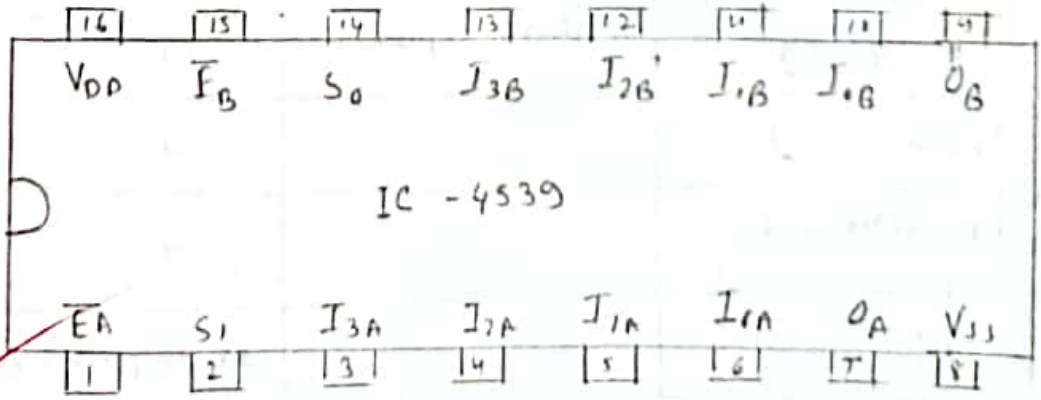
TITLE: Design a composite logic Unit using multiplexer.

OBJECTIVE: To design a composite logic Unit Using Multiplexer.

THEORY:

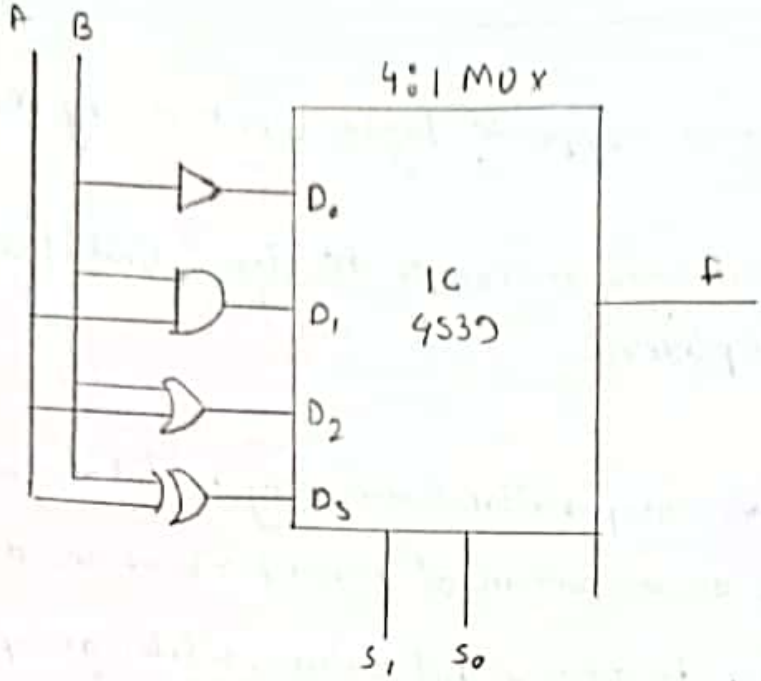
Logic microoperations are very useful for manipulating individual bits or a portion of a word stored in a register. They can be used to change bit values, delete group of bits, or insert new bit values into a register. these microperations require different logic gates to be inserted for each bit or pair of bits in the register to perform the required operation. Although there are several logic microoperations, most computers use only four. AND, OR, XOR, and NOT - from which all others can be derived.

PIN DIAGRAM



Dual 4-input multiplexer

CIRCUIT DIAGRAM:



INSTRUMENT & COMPONENT REQUIRED:

Sl no.	Item	Specification	qty
1	IC 4071	OR Gate	1
2	IC 4081	AND Gate	1
3	IC 4069	NOT Gate	1
4	IC 7486	XOR Gate	1
5	IC 4539	Dual multiplexer	1
6	Trainer kit	–	1
7	Breadboard	–	1
8	Wires	–	as required

VERIFICATION TABLE:

Select lines		Input		output (F:)	Operation
S_1	S_0	A	B		
0	0		1	0	NOT
0	1	0	0	0	OR
		0	1	1	
		1	0	1	
		1	1	1	
1	0	0	0	0	AND
		0	1	0	
		1	0	0	
		1	1	1	
1	1	0	0	0	XOR
		0	1	1	
		1	0	1	
		1	1	0	

CONCLUSION:

By this experiment we are now able to build logic unit using multiplexer.

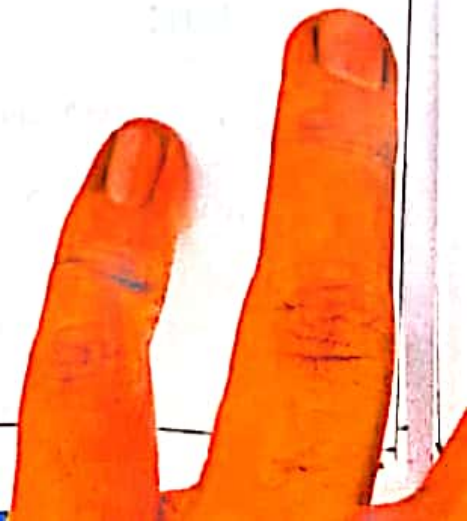
Experiment NO - CO-05(B)

TITLE: Design a Composite Arithmetic Unit Using multiplexer.

OBJECTIVE: To design a composite arithmetic Unit Using multiplexer.

THEORY:

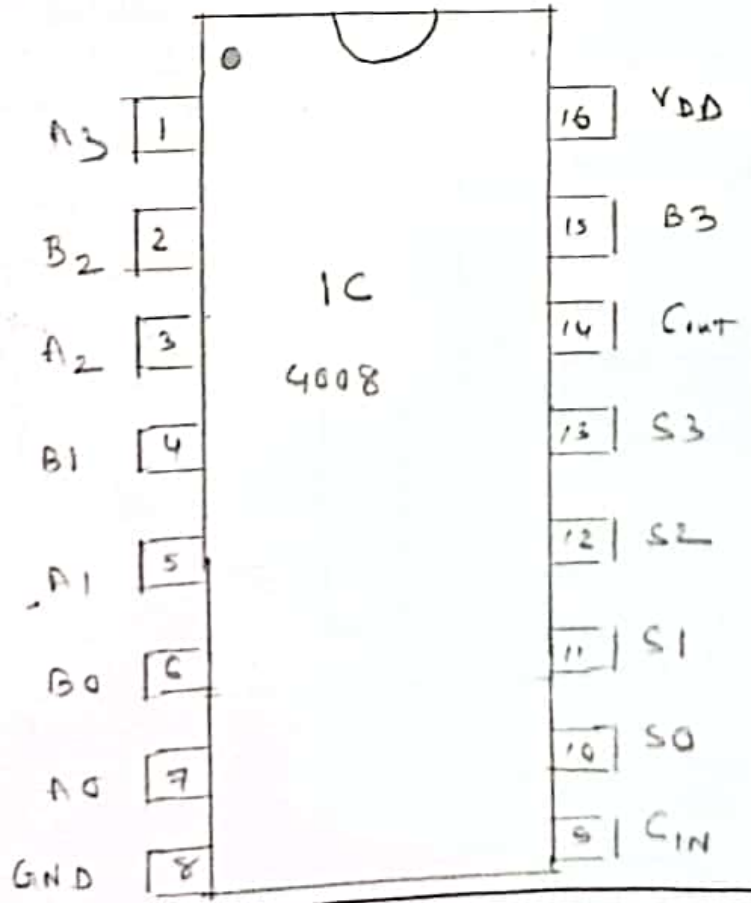
The Arithmetic Unit (AU) also called the Arithmetics Logic Unit (ALU), is a part of the Central processing Unit (CPU). It is often referred to as the Engine of the CPU because it allows the Computer to perform mathematical Calculation such as addition, subtraction etc. The AU comprised of many interconnected elements that are designed to perform specific task. the basic component of an AU is the parallel adder. By controlling the data inputs to the adder. It is possible to obtain different types of arithmetic operations.



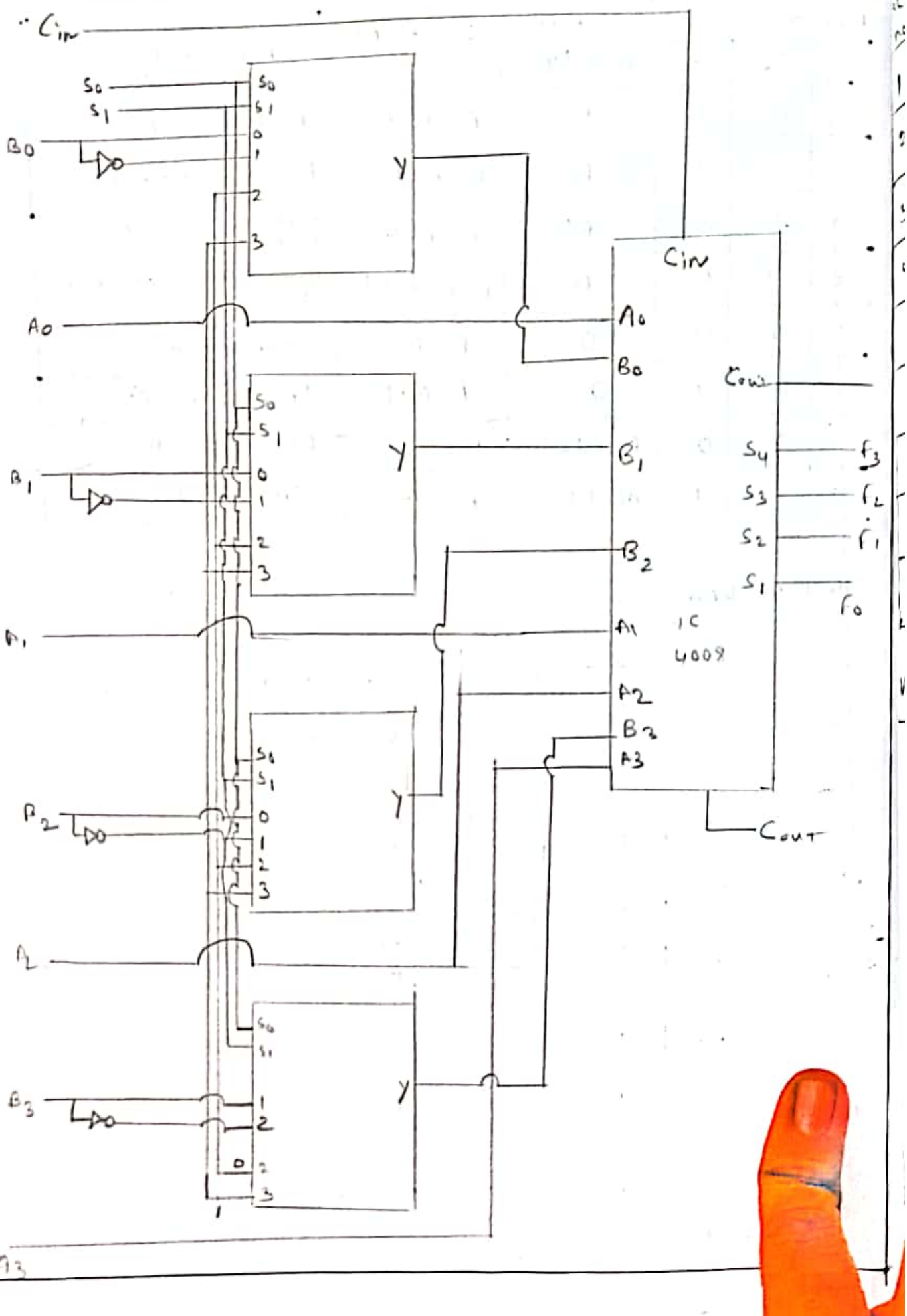
Function Table:

Function Selection			output of MUX (Y)	output (F)	Function Name
S_1	S_0	Cin			
0	0	0	B	F = A+B	Add B to A
0	0	1	B	F = A+B+1	Add B to A plus 1
0	1	0	B'	F = A+B'	Add 1's compliment of B to A
0	1	1	B'	F = A+B'+1	Add 2's compliment of B to A
1	0	0	0	F = A	Transfer A
1	0	1	0	F = A+1	Increment A
1	1	0	All 1's	F = A-1	Decrement A
1	1	1	All 1's	F = A	Transfer A

PIN DIAGRAM:



CIRCUIT DIAGRAM:



INSTRUMENT & COMPONENT REQUIRED:

Sl no.	Item	Specification	qty
1	OR Gate	IC 4071	4
2	AND Gate	IC 4081	4
3	NOT Gate	IC 4069	8
4	XOR Gate	IC 7486	4
5	Dual - 4bit mux	IC 4539	4
6		IC 4008	1
7	Trainer kit	-	1
8	Breadboard	-	1
9	wires	-	As per require

VERIFICATION TABLE:

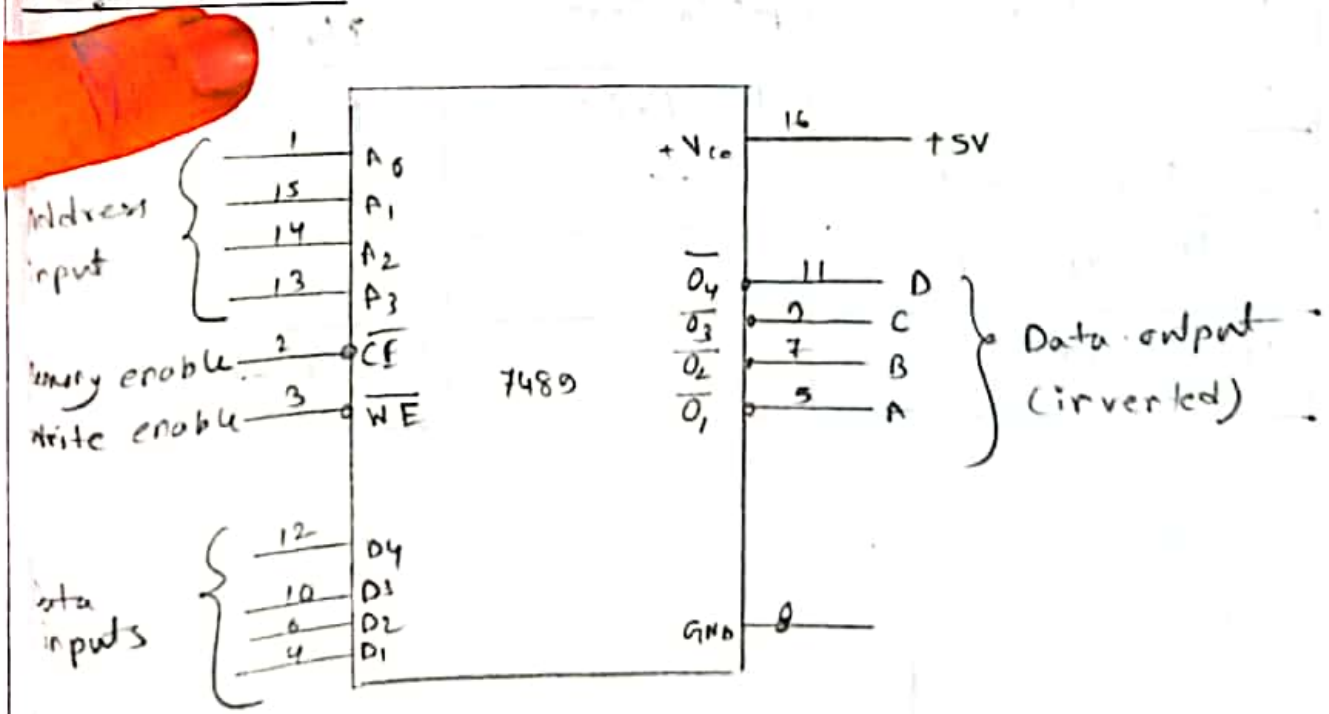
Experiment NO – CO - 06

TITLE: Memory Read/Write operation Using RAM IC

OBJECTIVE: To memory Read/write operation Using RAM IC

THEORY: Random Access Memory (RAM) is a volatile chip memory in which both read and write operation can be performed. Any random memory location can be accessed for information transfer to or from the memory. It is also called Read–Write Memory (RWM). The IC 7489 is arranged as 16 words of 4 bit each (16×4). It is a 64 bit memory.

PIN DIAGRAM



Function Table for RAM IC 7489:

Inputs		Operations	State of output
CE'	R/W'		
L	L	Write	Compliments of data inputs
L	H	Read	Complement of selected word
H	H	Inhibit entry	Undetermined
H	H	High	High

INSTRUMENT & COMPONENT REQUIRED:

SL NO	Item	Specification	Qty
1		IC 7489	1
2	Trainer kit	—	1
3	Breadboard	—	1
4	Wires	—	As required

ERIFICATION TABLE:

I/P	Memory Address				Data to be stored (W)				I/P	output (R)			
CE'	A_3	A_2	A_1	A_0	D_4	D_3	D_2	D_1	W'/R	O_3'	O_2'	O_1'	O_0'
0	0	0	0	1	0	0	1	0	0	–	–	–	–
0	0	0	0	1	–	–	–	–	1	1	0	0	1
0	0	0	1	0	0	0	1	1	0	–	–	–	–
0	0	0	1	0	–	–	–	–	1	1	1	0	0
0	0	0	1	0	0	1	0	1	0	–	–	–	–
0	0	0	1	0	–	–	–	–	1	1	0	1	0
0	0	1	1	0	–	–	–	–	1	–	–	–	–
0	1	1	0	0	1	0	0	1	0	–	–	–	–
0	1	1	0	0	–	–	–	–	1	0	1	1	0

Conclusion:

By the experiment we understand how the computer RAM store the data in address and perform the read/write operation.