Digital Design and Computer Organisation Laboratory

3rd Semester, Academic Year 2025

Date:19-08-2025

Name: Prajwal M	SRN:PES2UG24CS910	Section:C

Week Number: 3 Program Number: 3

TITLE:IMPLEMENTAION OF BCD ADDER

bcd_adder.v

```
1  module bcd_adder(
2      input [3:0] a,
3      input [3:0] b,
4      input cin,
5      output [3:0] sum,
6      output cout    "cout": Unknown word.
7  );
8      wire [3:0] temp_sum;
9      wire temp_cout;    "cout": Unknown word.
10     wire correction;
11     wire [3:0] correction_val;
12     wire [3:0] final_sum;
13     wire final_cout;    "cout": Unknown word.
14     ripple_carry_adder rca(.a(a), .b(b), .cin(cin), .sum(temp_sum), .cout(temp_cout));    "cout": Unknown word.
15     assign correction = temp_cout | (temp_sum[3] & (temp_sum[2] | temp_sum[1]));    "cout": Unknown word.
16     assign correction_val = correction ? 4'b0110 : 4'b0000;
17     ripple_carry_adder rca_correction(.a(temp_sum), .b(correction_val), .cin(1'b0), .sum(sum), .cout(cout));    "co
18 endmodule    "endmodule": Unknown word.
19
```

bcd_adder_tb.v

```v
module bcd_adder_tb;
    reg [3:0] a, b;
    reg cin;
    wire [3:0] sum;
    wire cout;    "cout": Unknown word.

    bcd_adder uut(
        .a(a),
        .b(b),
        .cin(cin),
        .sum(sum),
        .cout(cout)    "cout": Unknown word.
    );

    initial begin
        $dumpfile("bcd_adder_tb.vcd");    "dumpfile": Unknown word.
        $dumpvars(0, bcd_adder_tb);    "dumpvars": Unknown word.
        $display("Time | a | b | cin | sum | cout");    "cout": Unknown word.
        $monitor("%4d | %d | %d | %b | %d | %b", $time, a, b, cin, sum, cout);    "cout": Unknown word.
        a = 0; b = 0; cin = 0; #10;
        a = 0; b = 1; cin = 0; #10;
        a = 0; b = 2; cin = 0; #10;
        a = 0; b = 3; cin = 0; #10;
        a = 0; b = 4; cin = 0; #10;
        a = 0; b = 5; cin = 0; #10;
        a = 0; b = 6; cin = 0; #10;
        a = 0; b = 7; cin = 0; #10;
        a = 0; b = 8; cin = 0; #10;
        a = 0; b = 9; cin = 0; #10;
        a = 1; b = 0; cin = 0; #10;
        a = 1; b = 1; cin = 0; #10;
        a = 1; b = 2; cin = 0; #10;
        a = 1; b = 3; cin = 0; #10;
        a = 1; b = 4; cin = 0; #10;
        $finish;
    end
endmodule    "endmodule": Unknown word.
```

Windows PowerShell - gtkwa

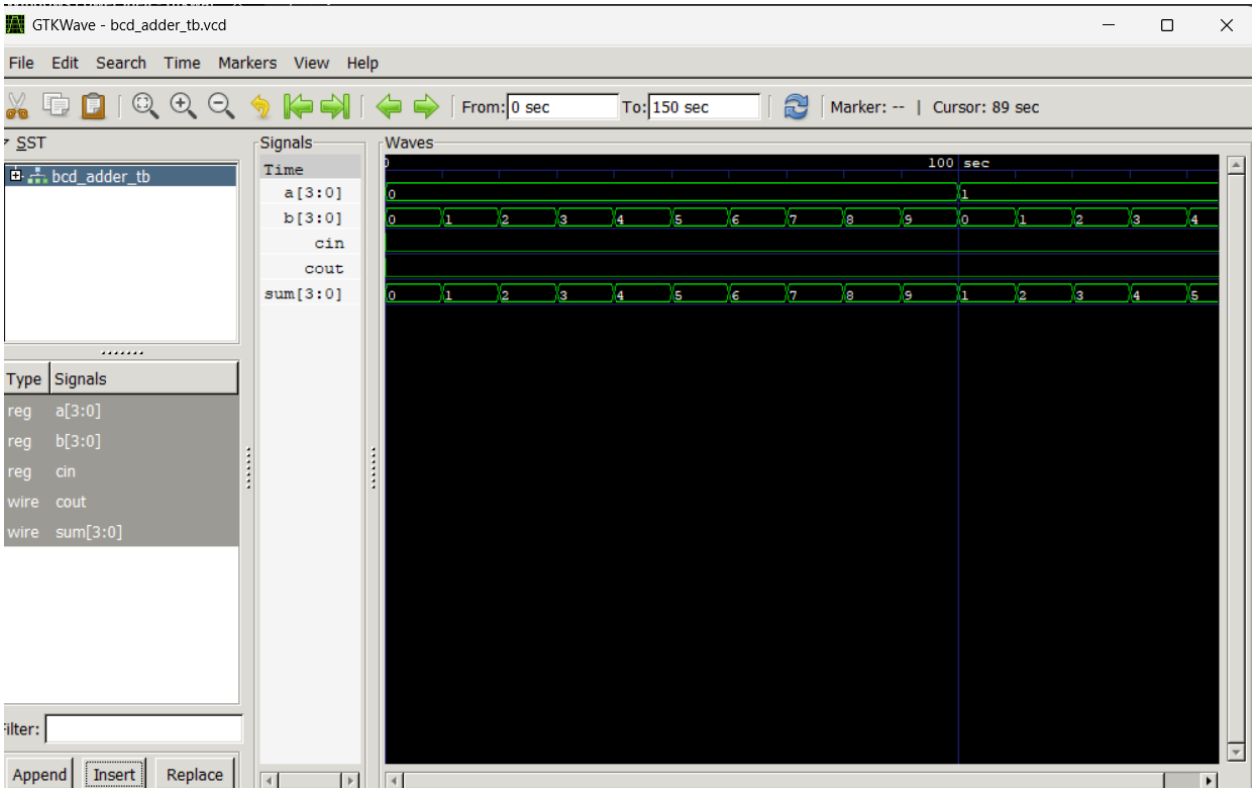
```
D:\iverilog lab\week 3>iverilog -o bcdadder bcd_adder.v ripple_carry_adder.v basic.v fulladder.v halfadd.v bcd_adder_tb.
v

D:\iverilog lab\week 3>vvp bcdadder
VCD info: dumpfile bcd_adder_tb.vcd opened for output.
Time|a|b|cin|sum|cout
   0| 0| 0|0| 0|0
  10| 0| 1|0| 1|0
  20| 0| 2|0| 2|0
  30| 0| 3|0| 3|0
  40| 0| 4|0| 4|0
  50| 0| 5|0| 5|0
  60| 0| 6|0| 6|0
  70| 0| 7|0| 7|0
  80| 0| 8|0| 8|0
  90| 0| 9|0| 9|0
 100| 1| 0|0| 1|0
 110| 1| 1|0| 2|0
 120| 1| 2|0| 3|0
 130| 1| 3|0| 4|0
 140| 1| 4|0| 5|0

D:\iverilog lab\week 3>gtkwave bcd_adder_tb.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[150] end time.
```


GTKWave - bcd_adder_tb.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 150 sec
Marker: -- | Cursor: 89 sec
SST
bcd_adder_tb
Type Signals
reg a[3:0]
reg b[3:0]
reg cin
wire cout
wire sum[3:0]
Filter:
Append Insert Replace
Signals
Time
a[3:0]
b[3:0]
cin
cout
sum[3:0]
Waves
100 sec