**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:19-08-2025

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|---|---|---|

Week Number: 3 Program Number: 3

TITLE:IMPLEMENTAION OF HALF,FULL,RIPPLE CARRY ADDER

## 1.HALF ADDER

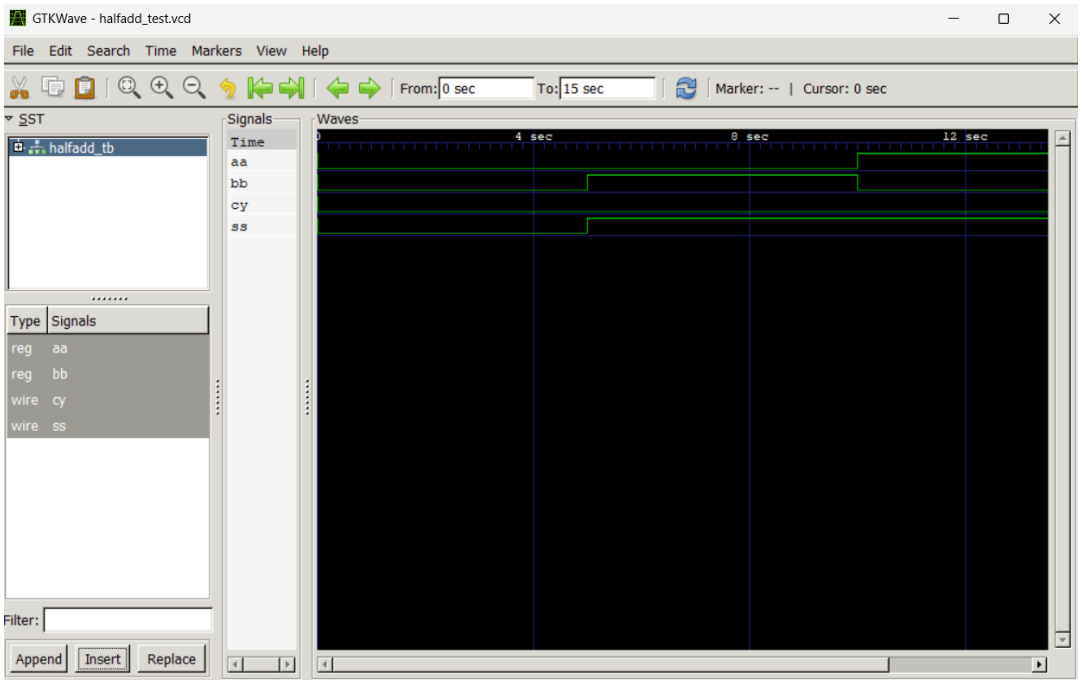
halfadd.v

```
1  module halfadd(a, b,sum, cout);    "halfadd": Unknown word.
2  input a, b;
3  output sum, cout;    "cout": Unknown word.
4   xor2 x0(a,b,sum);
5   and2 a0(a,b,cout);     "cout": Unknown word.
6  endmodule    "endmodule": Unknown word.
7
```

halfadder_tb.v

```
1  module halfadd_tb;    "halfadd": Unknown word.
2  reg aa,bb;
3  wire ss,cy;
4  halfadd add1(.a(aa), .b(bb),  .sum(ss), .cout(cy));    "halfadd": Unknow
5  initial
6  begin
7  $dumpfile("halfadd_test.vcd");    "dumpfile": Unknown word.
8  $dumpvars(0, halfadd_tb);    "dumpvars": Unknown word.
9  end
10
11 initial
12  begin
13 $monitor($time, "a=%b, b=%b, sum=%b, carry=%b", aa, bb, ss, cy);
14  aa = 1'b0;bb = 1'b0;
15 #5  aa = 1'b0;bb = 1'b1;
16 #5  aa = 1'b1;bb = 1'b0;
17 #5  aa = 1'b1;bb = 1'b1;
18 end
19 endmodule    "endmodule": Unknown word.
20
```

```
D:\iverilog lab\week 3>iverilog -o halfadd halfadd.v basic.v halfadder_tb.v

D:\iverilog lab\week 3>vvp halfadd
VCD info: dumpfile halfadd_test.vcd opened for output.
                   0a=0, b=0, sum=0, carry=0
                   5a=0, b=1, sum=1, carry=0
                  10a=1, b=0, sum=1, carry=0
                  15a=1, b=1, sum=0, carry=1

D:\iverilog lab\week 3>
```



# 2.FULL ADDER

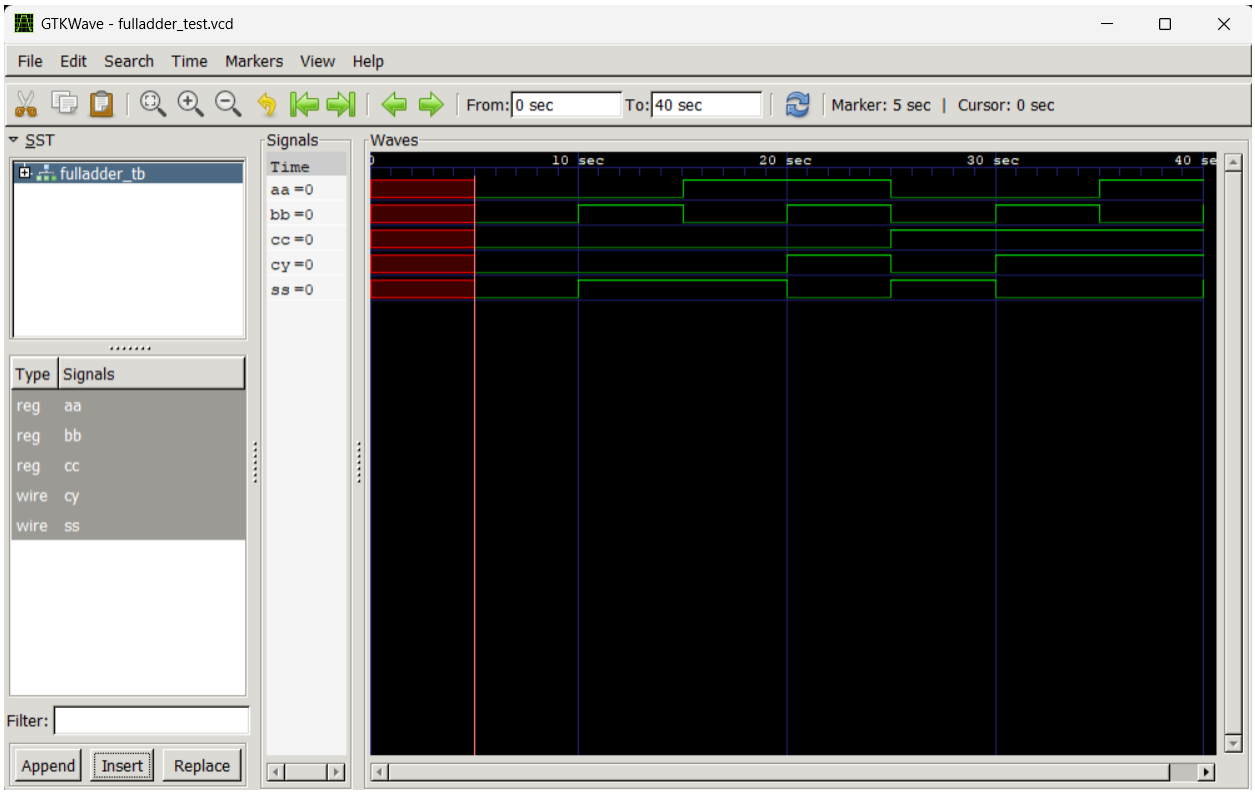
fulladder.v

```v
module fulladder(a, b, cin, sum, cout);    "fulladder": Unknown word.
    input a, b, cin;
    output sum, cout;    "cout": Unknown word.
    wire w1, w2, w3, w4, w5;

    xor2 x1(a, b, w1);
    xor2 x2(w1, cin, sum);

    and2 a1(a, b, w2);
    and2 a2(b, cin, w3);
    and2 a3(a, cin, w4);
    or2 o1(w2, w3, w5);
    or2 o2(w5, w4, cout);    "cout": Unknown word.
endmodule    "endmodule": Unknown word.

```

fulladder_tb.v

```v
module fulladder_tb;    "fulladder": Unknown word.
    reg aa, bb, cc;
    wire ss, cy;

    fulladder uut(.a(aa),.b(bb),.cin(cc),.sum(ss),.cout(cy));    "fulladder": Unknown word.

    initial begin
        $dumpfile("fulladder_test.vcd");    "dumpfile": Unknown word.
        $dumpvars(0, fulladder_tb);    "dumpvars": Unknown word.
    end

    initial begin
        $monitor($time, "a=%b, b=%b, cin=%b, sum=%b, cout=%b", aa, bb, cc, ss, cy);    "cout": Unknown word.
        #5 aa=1'b0; bb=1'b0; cc=1'b0;
        #5 aa=1'b0; bb=1'b1; cc=1'b0;
        #5 aa=1'b1; bb=1'b0; cc=1'b0;
        #5 aa=1'b1; bb=1'b1; cc=1'b0;
        #5 aa=1'b0; bb=1'b0; cc=1'b1;
        #5 aa=1'b0; bb=1'b1; cc=1'b1;
        #5 aa=1'b1; bb=1'b0; cc=1'b1;
        #5 aa=1'b1; bb=1'b1; cc=1'b1;
        $finish;
    end
endmodule    "endmodule": Unknown word.

```

```
D:\iverilog lab\week 3>iverilog -o fulladd fulladder.v basic.v halfadd.v fulladder_tb.v

D:\iverilog lab\week 3>vvp fulladd
VCD info: dumpfile fulladder_test.vcd opened for output.
                   0a=x, b=x, cin=x, sum=x, cout=x
                   5a=0, b=0, cin=0, sum=0, cout=0
                  10a=0, b=1, cin=0, sum=1, cout=0
                  15a=1, b=0, cin=0, sum=1, cout=0
                  20a=1, b=1, cin=0, sum=0, cout=1
                  25a=0, b=0, cin=1, sum=1, cout=0
                  30a=0, b=1, cin=1, sum=0, cout=1
                  35a=1, b=0, cin=1, sum=0, cout=1
                  40a=1, b=1, cin=1, sum=1, cout=1

D:\iverilog lab\week 3>
```




# 3.RIPPLE CARRY ADDER

ripple_carry_adder.v

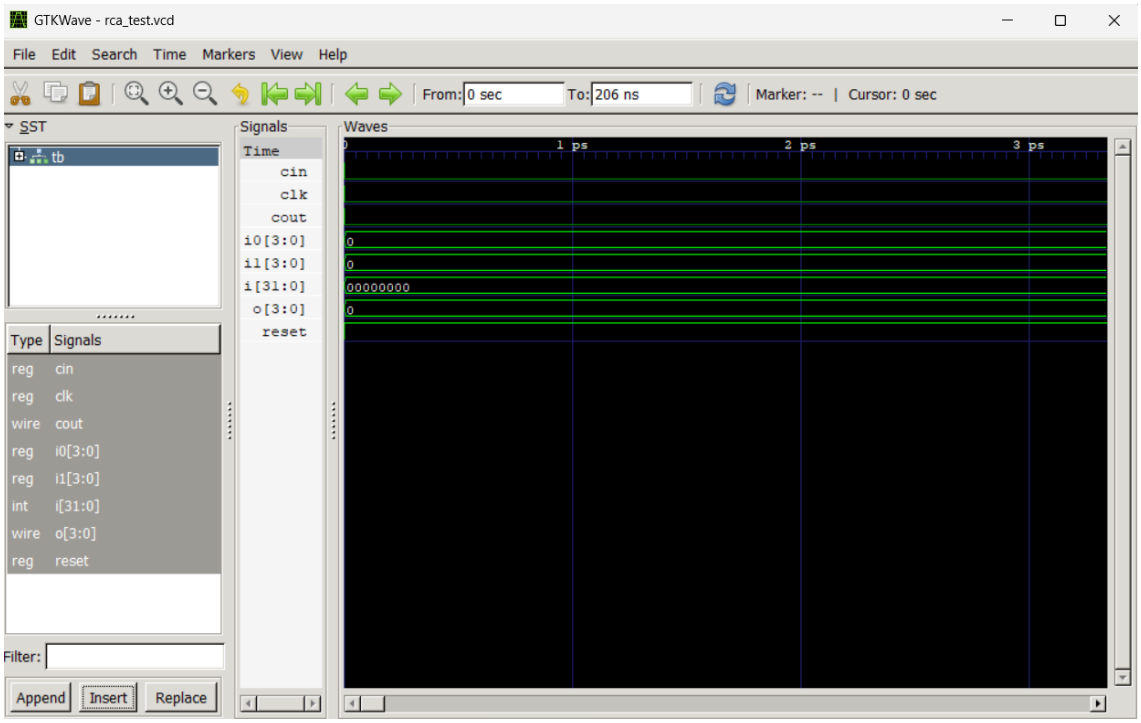
```
1  module ripple_carry_adder(input wire [3:0] a, b, input wire cin, output wire [3:0] sum, output wire cout);    "cout": Unknow
2      wire [2:0] c;
3      fulladder u0 (.a(a[0]), .b(b[0]), .cin(cin), .sum(sum[0]), .cout(c[0]));    "fulladder": Unknown word.
4      fulladder u1 (.a(a[1]), .b(b[1]), .cin(c[0]), .sum(sum[1]), .cout(c[1]));    "fulladder": Unknown word.
5      fulladder u2 (.a(a[2]), .b(b[2]), .cin(c[1]), .sum(sum[2]), .cout(c[2]));    "fulladder": Unknown word.
6      fulladder u3 (.a(a[3]), .b(b[3]), .cin(c[2]), .sum(sum[3]), .cout(cout));    "fulladder": Unknown word.
7  endmodule    "endmodule": Unknown word.
8
```

ripple_carry_adder_tb.v

```
1  `timescale 1 ns / 100 ps
2  `define TESTVECS 10    "TESTVECS": Unknown word.
3  module tb;
4  reg clk, reset;
5   reg [3:0] i0, i1;
6   reg cin;
7  wire [3:0] o;
8  wire cout;     "cout": Unknown word.
9   reg [8:0] test_vecs [0:(`TESTVECS-1)];     "vecs": Unknown word.
10 integer i;
11 initial
12 begin
13 $dumpfile("rca_test.vcd");     "dumpfile": Unknown word.
14 $dumpvars(0,tb);     "dumpvars": Unknown word.
15  end
16
17 initial
18 begin
19  reset = 1'b1; #12.5 reset = 1'b0; end  initial clk = 1'b0; always #5 clk =~ clk;
20   initial begin
21  test_vecs[0] = 9'b000000000;     "vecs": Unknown word.
22  test_vecs[1] = 9'b000000001;     "vecs": Unknown word.
23 test_vecs[2] = 9'b000100010;     "vecs": Unknown word.
24   test_vecs[3] = 9'b000100011;     "vecs": Unknown word.
25 test_vecs[4] = 9'b001000100;     "vecs": Unknown word.
26   test_vecs[5] = 9'b001000101;     "vecs": Unknown word.
27   test_vecs[6] = 9'b101010110;     "vecs": Unknown word.
28    test_vecs[7] = 9'b101010111;     "vecs": Unknown word.
29 test_vecs[8] = 9'b111011110;     "vecs": Unknown word.
30 test_vecs[9] = 9'b111011111;     "vecs": Unknown word.
31   end
32
33
34 initial {i0, i1, cin, i} = 0;
35  ripple_carry_adder u0 (i0, i1, cin, o, cout);     "cout": Unknown word.
36 initial begin    #6
37 for(i=0;i<`TESTVECS;i=i+1)     "TESTVECS": Unknown word.
38    begin #10 {i0, i1, cin}=test_vecs[i];     "vecs": Unknown word.
39 end     #100 $finish;  end
40 always@(i0 or i1 or cin)
41 $monitor("At time = %t, i0=%b, i1=%b,cin=%b,Sum = %b,Carry %b", $time,i0,i1,cin,o,cout);     "cout": Unknown word.
42 endmodule    "endmodule": Unknown word.
43
```

Windows PowerShell

```
D:\iverilog lab\week 3>iverilog -o rippadd fulladder.v basic.v ripple_carry_adder.v ripple_carry_adder_tb.v

D:\iverilog lab\week 3>vvp rippadd
VCD info: dumpfile rca_test.vcd opened for output.
At time =                    0, i0=0000, i1=0000,cin=0,Sum = 0000,Carry 0
At time =                  260, i0=0000, i1=0000,cin=1,Sum = 0001,Carry 0
At time =                  360, i0=0001, i1=0001,cin=0,Sum = 0010,Carry 0
At time =                  460, i0=0001, i1=0001,cin=1,Sum = 0011,Carry 0
At time =                  560, i0=0010, i1=0010,cin=0,Sum = 0100,Carry 0
At time =                  660, i0=0010, i1=0010,cin=1,Sum = 0101,Carry 0
At time =                  760, i0=1010, i1=1011,cin=0,Sum = 0101,Carry 1
At time =                  860, i0=1010, i1=1011,cin=1,Sum = 0110,Carry 1
At time =                  960, i0=1110, i1=1111,cin=0,Sum = 1101,Carry 1
At time =                 1060, i0=1110, i1=1111,cin=1,Sum = 1110,Carry 1

D:\iverilog lab\week 3>
```


GTKWave - rca_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 206 ns
Marker: -- | Cursor: 0 sec
SST
tb
Type Signals
reg cin
reg clk
wire cout
reg i0[3:0]
reg i1[3:0]
int i[31:0]
wire o[3:0]
reg reset
Filter:
Append Insert Replace
Signals
Time
cin
clk
cout
i0[3:0]
i1[3:0]
i[31:0]
o[3:0]
reset
Waves
1 ps
2 ps
3 ps
0
0
00000000
0