Digital Design and Computer Organisation Laboratory

3rd Semester, Academic Year 2025

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Week Number: 5 Program Number: 5

TITLE:IMPLEMENTAION OF 2:4 Decoder and 4:2 encoder

1. 4:2-Encoder

encoder4.v

```
module encoder4x2(input wire i0,input wire i1,input wire i2,input wire i3,output wire y0,output wire y1);
assign y0=i1|i3;
assign y1=i2|i3;
endmodule    "endmodule": Unknown word.

```

encoder4_tb.v

```
module TB;
reg i0,i1,i2,i3;
wire y0,y1;
encoder4x2 uut(.i0(i0),.i1(i1),.i2(i2),.i3(i3),.y0(y0),.y1(y1));
initial begin
$dumpfile("encoder4x2_test.vcd");    "dumpfile": Unknown word.
$dumpvars(0,TB);    "dumpvars": Unknown word.
end
initial begin
i0=1;i1=0;i2=0;i3=0;
#5 i0=0;i1=1;i2=0;i3=0;
#5 i0=0;i1=0;i2=1;i3=0;
#5 i0=0;i1=0;i2=0;i3=1;
end
initial begin
$monitor("At time %t, i0=%b, i1=%b, i2=%b, i3=%b, y0=%b, y1=%b", $time,i0,i1,i2,i3,y0,y1);
end
endmodule    "endmodule": Unknown word.

```

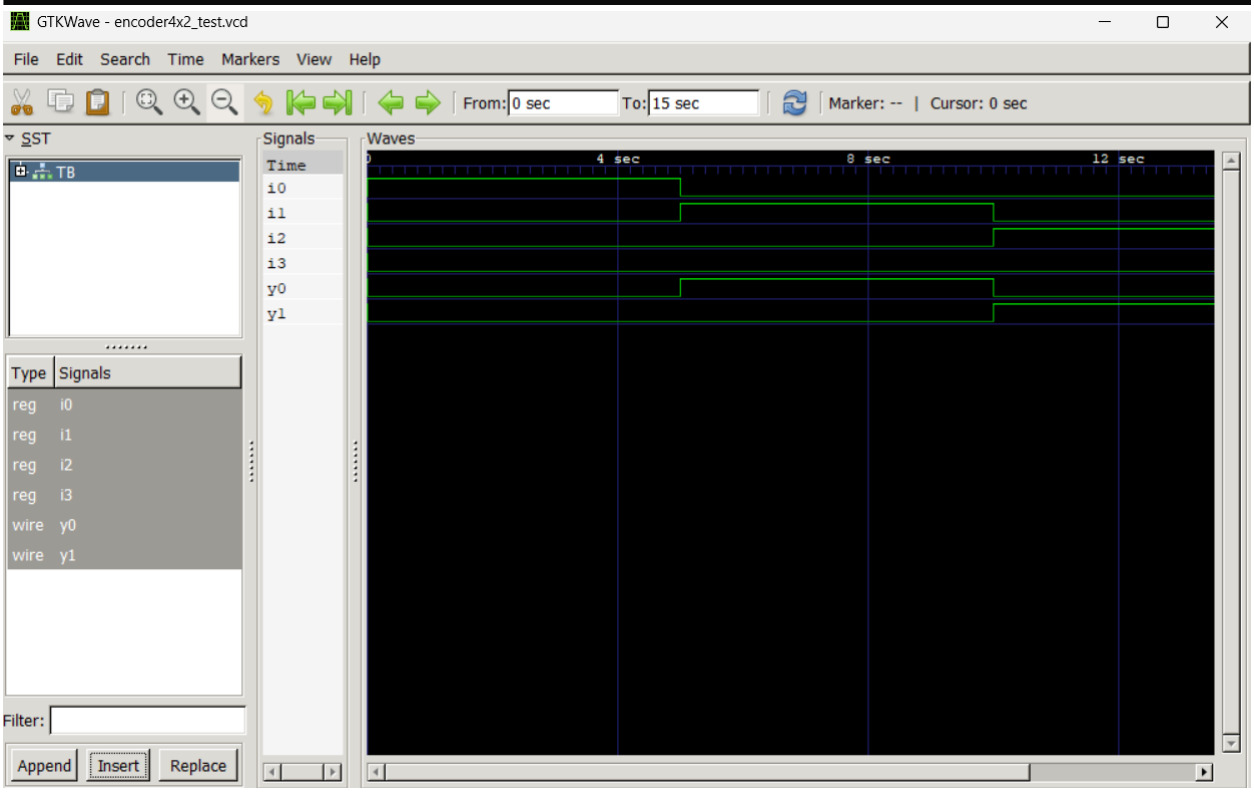
```
D:\iverilog lab\week 4>iverilog -o encoder encoder4.v encoder4_tb.v

D:\iverilog lab\week 4>vvp encoder
VCD info: dumpfile encoder4x2_test.vcd opened for output.
At time                    0, i0=1, i1=0, i2=0, i3=0, y0=0, y1=0
At time                    5, i0=0, i1=1, i2=0, i3=0, y0=1, y1=0
At time                   10, i0=0, i1=0, i2=1, i3=0, y0=0, y1=1
At time                   15, i0=0, i1=0, i2=0, i3=1, y0=1, y1=1

D:\iverilog lab\week 4>gtkwave encoder4x2_test.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[15] end time.
```



2. 2:4 Decoder

decoder2.v

```
1  module decoder2x4(input wire a,input wire b,output wire y0,output wire y1,output wire y2,output wire y3);
2  assign y0=~a&~b;
3  assign y1=~a&b;
4  assign y2=a&~b;
5  assign y3=a&b;
6  endmodule    "endmodule": Unknown word.
7
```

decoder2_tb.v

```
1   module decoder_TB;
2   reg a,b;
3   wire y0,y1,y2,y3;
4   decoder2x4 uut(.a(a),.b(b),.y0(y0),.y1(y1),.y2(y2),.y3(y3));
5   initial begin
6   $dumpfile("decoder2_test.vcd");    "dumpfile": Unknown word.
7   $dumpvars(0,TB);    "dumpvars": Unknown word.
8   end
9   initial begin
10  a=0;b=0;
11  #5 a=0;b=1;
12  #5 a=1;b=0;
13  #5 a=1;b=1;
14  end
15  initial begin
16  $monitor("At time %t, a=%b, b=%b, y0=%b, y1=%b, y2=%b, y3=%b", $time,a,b,y0,y1,y2,y3);
17  end
18  endmodule    "endmodule": Unknown word.
19
```

```
D:\iverilog lab\week 4>iverilog -o decoder decoder2.v decoder2_tb.v

D:\iverilog lab\week 4>vvp decoder
VCD info: dumpfile decoder2x4_test.vcd opened for output.
At time                    0, a=0, b=0, y0=1, y1=0, y2=0, y3=0
At time                    5, a=0, b=1, y0=0, y1=1, y2=0, y3=0
At time                   10, a=1, b=0, y0=0, y1=0, y2=1, y3=0
At time                   15, a=1, b=1, y0=0, y1=0, y2=0, y3=1

D:\iverilog lab\week 4>gtkwave decoder2x4_test.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[15] end time.
```