

# Digital Design and Computer Organisation Laboratory

3rd Semester, Academic Year 2025

Date:25-08-2025

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Week Number: 4

Program Number: 4

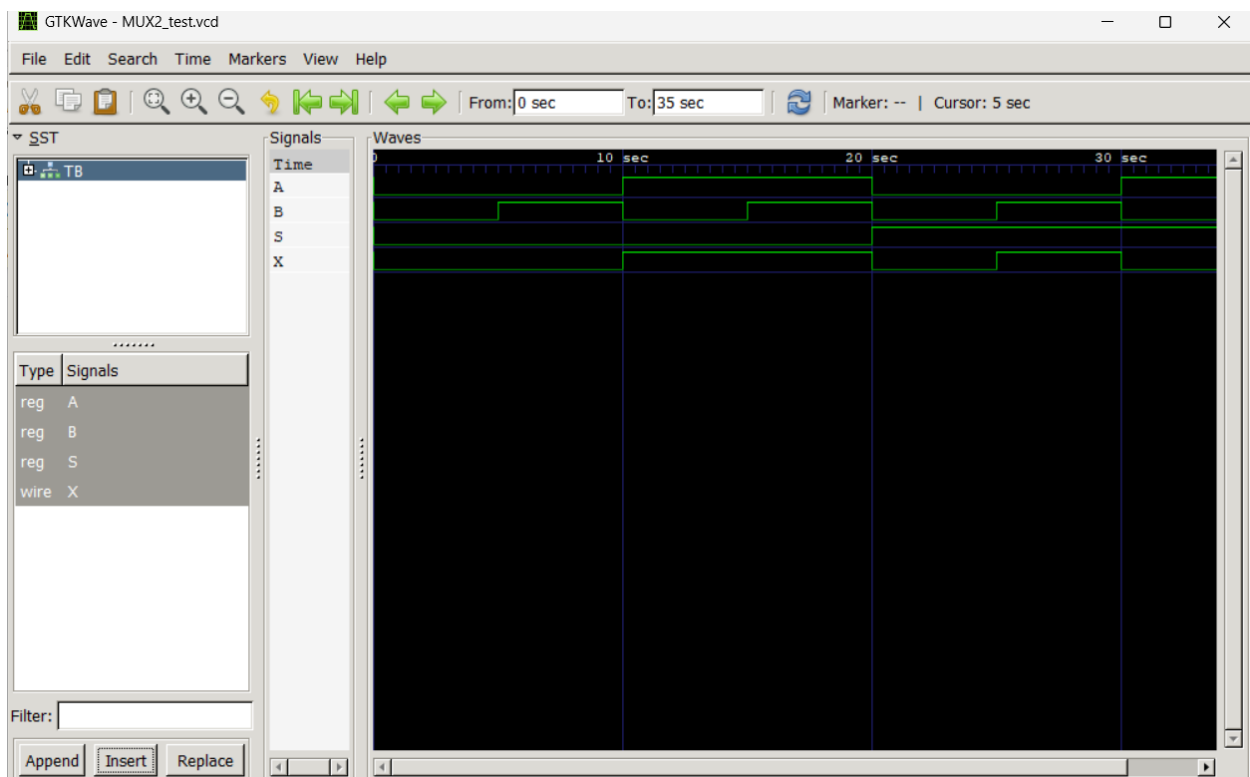
TITLE:IMPLEMENTAION OF MUX2 , MUX4 ,DEMUX2

## 1.MUX-2

```
1 mux2.v
2 module mux2 (input wire i0, i1, j, output wire o);
3   assign o = j ? i1 : i0;
4 endmodule
```

```
1 mux2_tb.v
2 module TB;
3   reg A,B,S;
4   wire X;
5   initial
6   begin
7     $dumpfile("MUX2_test.vcd");
8     $dumpvars(0,TB);
9     mux2 newMUX(.i0(A), .i1(B), .j(S), .o(X));
10    initial
11    begin
12      S = 1'b0; A = 1'b0; B = 1'b0;
13      #5 S = 1'b0; A = 1'b0; B = 1'b1;
14      #5 S = 1'b0; A = 1'b1; B = 1'b0;
15      #5 S = 1'b0; A = 1'b1; B = 1'b1;
16      #5 S = 1'b1; A = 1'b0; B = 1'b0;
17      #5 S = 1'b1; A = 1'b0; B = 1'b1;
18      #5 S = 1'b1; A = 1'b1; B = 1'b0;
19      #5 S = 1'b1; A = 1'b1; B = 1'b1;
20    end
21    initial
22    begin
23      $monitor("At time %t, S = %b, A = %b, B = %b, X = %b", $time, S, A, B, X);
24    end
25  endmodule
```

```
Windows PowerShell - gtkwa x + v
D:\iverilog lab\week 4>iverilog -o mux2 mux2.v mux2_tb.v
D:\iverilog lab\week 4>vvp mux2
VCD info: dumpfile MUX2_test.vcd opened for output.
At time      0, S = 0, A = 0, B = 0, X = 0
At time      5, S = 0, A = 0, B = 1, X = 0
At time     10, S = 0, A = 1, B = 0, X = 1
At time     15, S = 0, A = 1, B = 1, X = 1
At time     20, S = 1, A = 0, B = 0, X = 0
At time     25, S = 1, A = 0, B = 1, X = 1
At time     30, S = 1, A = 1, B = 0, X = 0
At time     35, S = 1, A = 1, B = 1, X = 1
D:\iverilog lab\week 4>gtkwave MUX2_test.vcd
GTKWave Analyzer v3.3.48 (w)1999-2013 BSI
[0] start time.
[35] end time.
```



## 2.MUX-4

```
mux4.v
1 module mux4 (input wire [3:0] i, input wire j1, j0, output wire o);
2 wire t0, t1;
3 mux2 mux2_0 (.i0(i[0]), .i1(i[1]), .j(j0), .o(t0));
4 mux2 mux2_1 (.i0(i[2]), .i1(i[3]), .j(j0), .o(t1));
5 mux2 mux2_2 (.i0(t0), .i1(t1), .j(j1), .o(o));
6 endmodule "endmodule": Unknown word.
```

```
mux4_tb.v
1 module TB;
2 reg [3:0] ii;
3 reg s0;
4 reg s1;
5 wire yy;
6 initial begin
7     $dumpfile("MUX4_test.vcd"); "dumpfile": Unknown word.
8     $dumpvars(0, TB); "dumpvars": Unknown word.
9 end
10 mux4 newMUX(.i(ii), .j0(s0), .j1(s1), .o(yy));
11 initial begin
12     ii = 4'b0000; s0 = 1'b0; s1 = 1'b0;
13     #5 ii = 4'b1000; s0 = 1'b0; s1 = 1'b0;
14     #5 ii = 4'b0000; s0 = 1'b0; s1 = 1'b1;
15     #5 ii = 4'b0100; s0 = 1'b0; s1 = 1'b1;
16     #5 ii = 4'b0000; s0 = 1'b1; s1 = 1'b0;
17     #5 ii = 4'b0010; s0 = 1'b1; s1 = 1'b0;
18     #5 ii = 4'b0000; s0 = 1'b1; s1 = 1'b1;
19     #5 ii = 4'b0001; s0 = 1'b1; s1 = 1'b1;
20 end
21 initial begin
22     $monitor("At time %t, s1 = %b, s0 = %b, ii = %b, yy = %b", $time, s1, s0, ii, yy);
23 end
24 endmodule "endmodule": Unknown word.
25
```

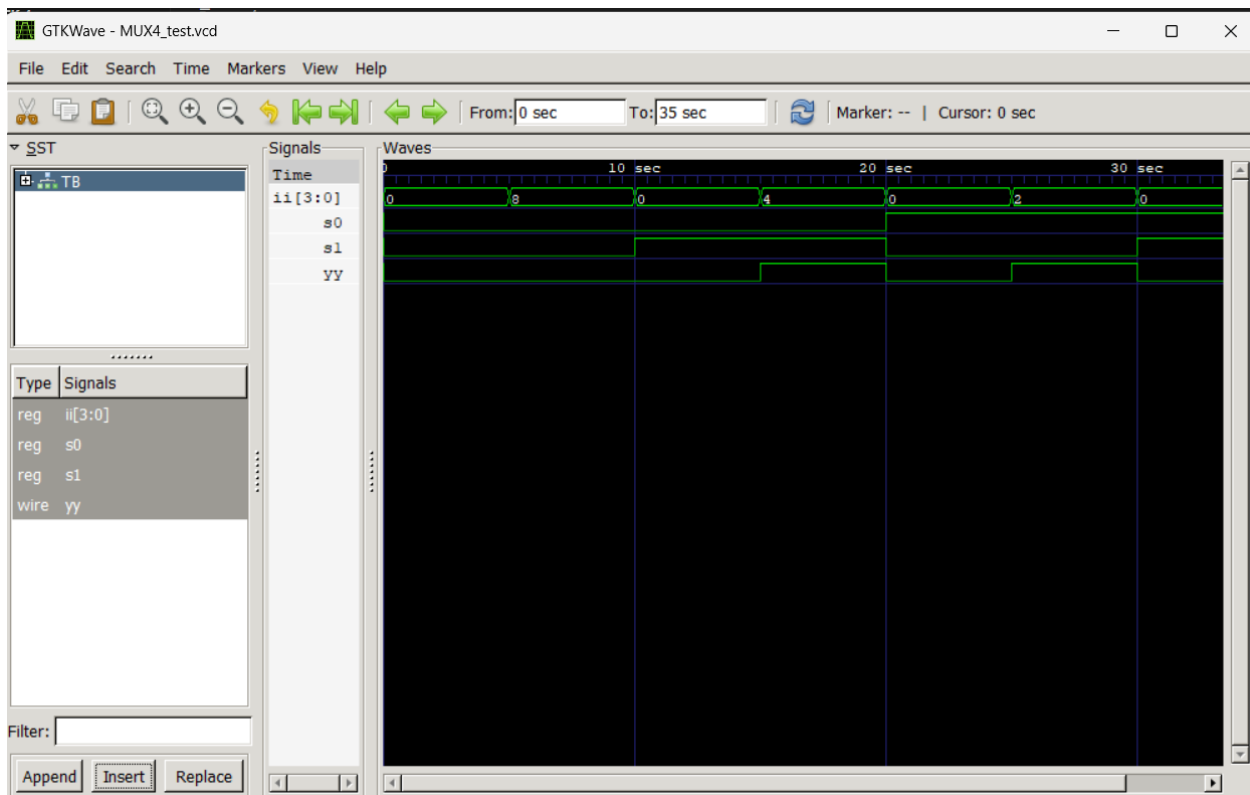
```
Windows PowerShell - gtkwai
D:\iverilog lab\week 4>iverilog -o mux4 mux2.v mux4.v mux4_tb.v

D:\iverilog lab\week 4>vvp mux4
VCD info: dumpfile MUX4_test.vcd opened for output.
At time      0, s1 = 0, s0 = 0, ii = 0000, yy = 0
At time      5, s1 = 0, s0 = 0, ii = 1000, yy = 0
At time     10, s1 = 1, s0 = 0, ii = 0000, yy = 0
At time     15, s1 = 1, s0 = 0, ii = 0100, yy = 1
At time     20, s1 = 0, s0 = 1, ii = 0000, yy = 0
At time     25, s1 = 0, s0 = 1, ii = 0010, yy = 1
At time     30, s1 = 1, s0 = 1, ii = 0000, yy = 0
At time     35, s1 = 1, s0 = 1, ii = 0001, yy = 0

D:\iverilog lab\week 4>gtkwave MUX4_test.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[35] end time.
```



## DEMUX-2

```

1 module demux2(input wire s,input wire d,output wire y0,output wire y1);    "demux": Unknown word.
2 assign y0=~s?d:1'b0;
3 assign y1=s?d:1'b0;
4 endmodule    "endmodule": Unknown word.
5

```

```

1 module TB;
2 reg s, d;
3 wire y0, y1;
4 demux2 uut(.s(s), .d(d), .y0(y0), .y1(y1));    "demux": Unknown word.
5 initial begin
6 s=0;d=0;
7 #5 s=0;d=1;
8 #5 s=1;d=0;
9 #5 s=1;d=1;
10 end
11 initial begin
12 $dumpfile("demux2_test.vcd");    "dumpfile": Unknown word.
13 $dumpvars(0,TB);    "dumpvars": Unknown word.
14 $monitor("At time %t, s = %b, d = %b, y0 = %b, y1 = %b", $time, s, d, y0, y1);
15 end
16 endmodule    "endmodule": Unknown word.
17
18

```

```
D:\iverilog lab\week 4>iverilog -o demux2 demux2.v demux2_tb.v

D:\iverilog lab\week 4>vvp demux2
VCD info: dumpfile demux2_test.vcd opened for output.
At time      0, s = 0, d = 0, y0 = 0, y1 = 0
At time      5, s = 0, d = 1, y0 = 1, y1 = 0
At time     10, s = 1, d = 0, y0 = 0, y1 = 0
At time     15, s = 1, d = 1, y0 = 0, y1 = 1

D:\iverilog lab\week 4>gtkwave demux2_test.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[15] end time.
```

