Digital Design and Computer Organisation Laboratory

3rd Semester, Academic Year 2025

Date:12-08-2025

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Week Number: 2 Program Number: 2

TITLE:IMPLEMENTAION OF BASIC GATES IN IVERILOG

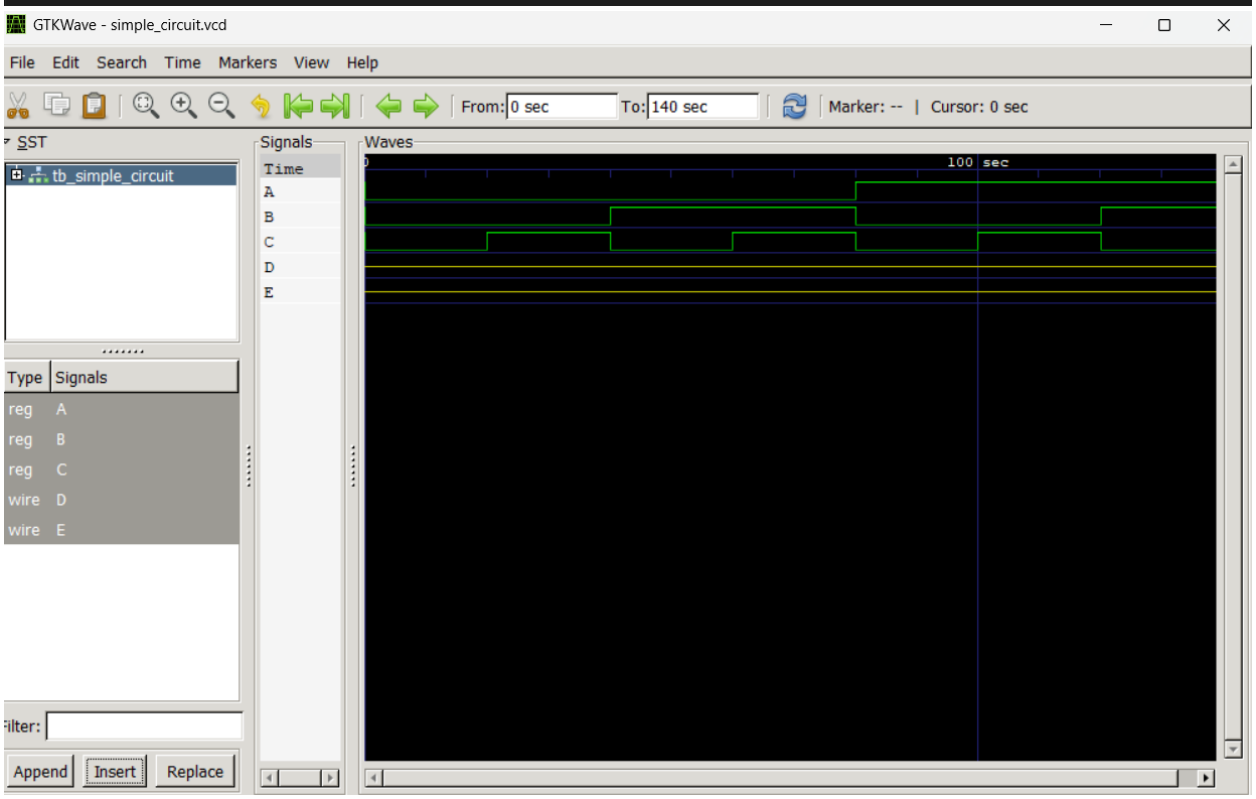
1.

simple_circuit.v

```
1   module simple_circuit (A, B, C, D, E);
2       output D, E;
3       input A, B, C;
4       wire w1;
5
6       and G1(w1, A, B);
7       not G2(C, E);
8       or  G3(w1, E, D);
9   endmodule    "endmodule": Unknown word.
10
```

tb_simple_circuit.v

```
1   module tb_simple_circuit;
2
3   reg A,B,C;
4   wire D,E;
5
6   simple_circuit M1(A,B,C,D,E);
7
8   initial begin
9           #0 A=1'b0 ; B=1'b0 ; C=1'b0;
10          #20 A=1'b0 ; B=1'b0 ; C=1'b1;
11          #20 A=1'b0 ; B=1'b1 ; C=1'b0;
12          #20 A=1'b0 ; B=1'b1 ; C=1'b1;
13          #20 A=1'b1 ; B=1'b0 ; C=1'b0;
14          #20 A=1'b1 ; B=1'b0 ; C=1'b1;
15          #20 A=1'b1 ; B=1'b1 ; C=1'b0;
16          #20 A=1'b1 ; B=1'b1 ; C=1'b1;
17
18      end
19
20
21  initial begin
22  $monitor($time,"A=%b B=%b C=%b D=%b E=%b",A,B,C,D,E);
23  end
24
25  initial begin
26  $dumpfile("simple_circuit.vcd");    "dumpfile": Unknown word.
27  $dumpvars(0,tb_simple_circuit);    "dumpvars": Unknown word.
28  end
29  endmodule    "endmodule": Unknown word.
```



```
Windows PowerShell

D:\Iverlog>iverilog -o test simple_circuit.v tb_simple_circuit.v

D:\Iverlog>vvp test
VCD info: dumpfile simple_circuit.vcd opened for output.
                   0A=0 B=0 C=0 D=z E=z
                  20A=0 B=0 C=1 D=z E=z
                  40A=0 B=1 C=0 D=z E=z
                  60A=0 B=1 C=1 D=z E=z
                  80A=1 B=0 C=0 D=z E=z
                 100A=1 B=0 C=1 D=z E=z
                 120A=1 B=1 C=0 D=z E=z
                 140A=1 B=1 C=1 D=z E=z

D:\Iverlog>
```

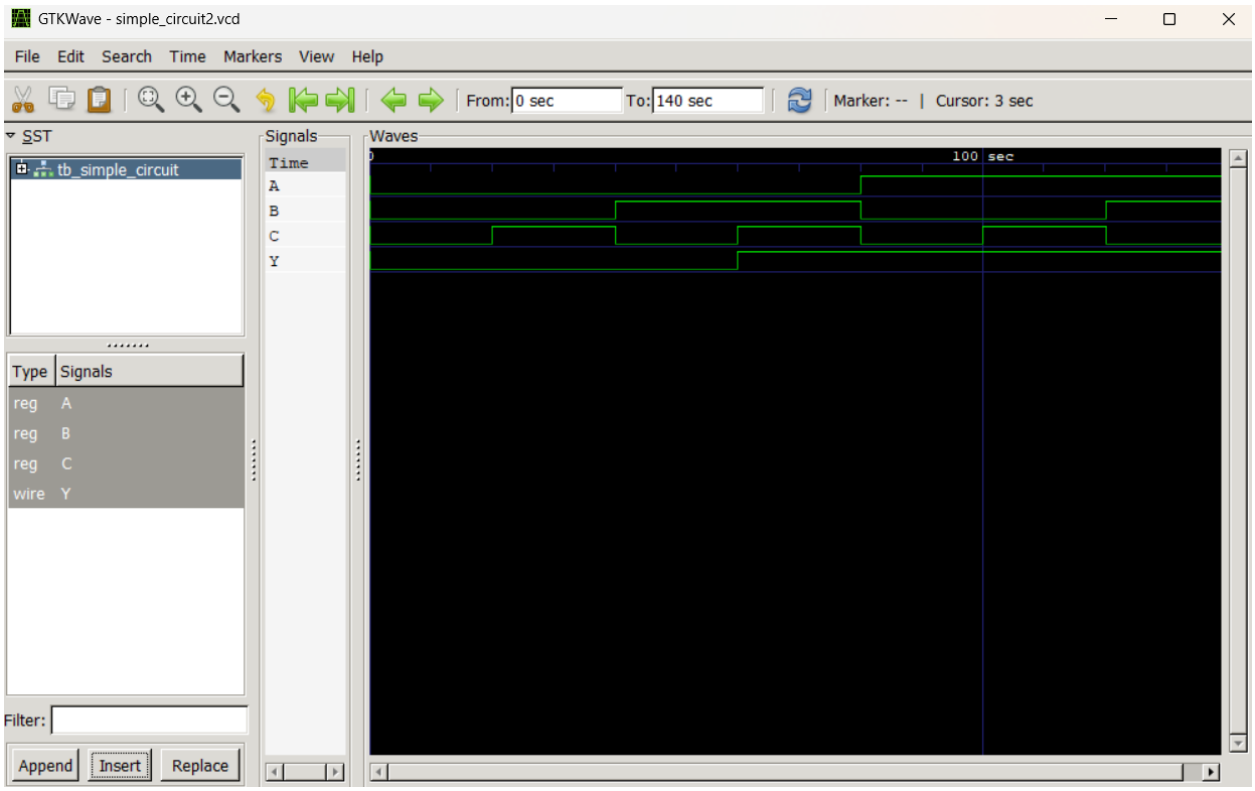
2.

and2.v

```
1   module and2(a, b, c);
2       input a, b;
3       output c;
4       assign c = a & b;
5   endmodule    "endmodule": Unknown word.
6
7   module or2(a, b, c);
8       input a, b;
9       output c;
10      assign c = a | b;
11  endmodule    "endmodule": Unknown word.
12  module simple_circuit2(A, B, C, Y);
13
14      input A, B, C;
15      output Y;
16      wire w1;
17
18      and2 and2_1(B,C,w1);
19      or2 or2_1(w1,A,Y);
20
21  endmodule    "endmodule": Unknown word.
```

tb_and2.v

```
1  module tb_simple_circuit;
2      reg A,B,C;
3      wire Y;
4      simple_circuit2 M1(A,B,C,Y);
5
6      initial begin
7          #0 A=1'b0 ; B=1'b0 ; C=1'b0;
8          #20 A=1'b0 ; B=1'b0 ; C=1'b1;
9          #20 A=1'b0 ; B=1'b1 ; C=1'b0;
10         #20 A=1'b0 ; B=1'b1 ; C=1'b1;
11         #20 A=1'b1 ; B=1'b0 ; C=1'b0;
12         #20 A=1'b1 ; B=1'b0 ; C=1'b1;
13         #20 A=1'b1 ; B=1'b1 ; C=1'b0;
14         #20 A=1'b1 ; B=1'b1 ; C=1'b1;
15
16     end
17
18     initial begin
19         $monitor($time,"A=%b B=%b C=%b Y=%b",A,B,C,Y);
20     end
21
22     initial begin
23         $dumpfile("simple_circuit2.vcd");    "dumpfile": Unknown word.
24         $dumpvars(0,tb_simple_circuit);    "dumpvars": Unknown word.
25     end
26 endmodule    "endmodule": Unknown word.
```



```
Windows PowerShell - gtkwav

D:\Iverlog>iverilog -o test and2.v tb_and2.v

D:\Iverlog>vvp test
VCD info: dumpfile simple_circuit2.vcd opened for output.
                   0A=0 B=0 C=0 Y=0
                  20A=0 B=0 C=1 Y=0
                  40A=0 B=1 C=0 Y=0
                  60A=0 B=1 C=1 Y=1
                  80A=1 B=0 C=0 Y=1
                 100A=1 B=0 C=1 Y=1
                 120A=1 B=1 C=0 Y=1
                 140A=1 B=1 C=1 Y=1

D:\Iverlog>gtkwave simple_circuit2.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[140] end time.
```

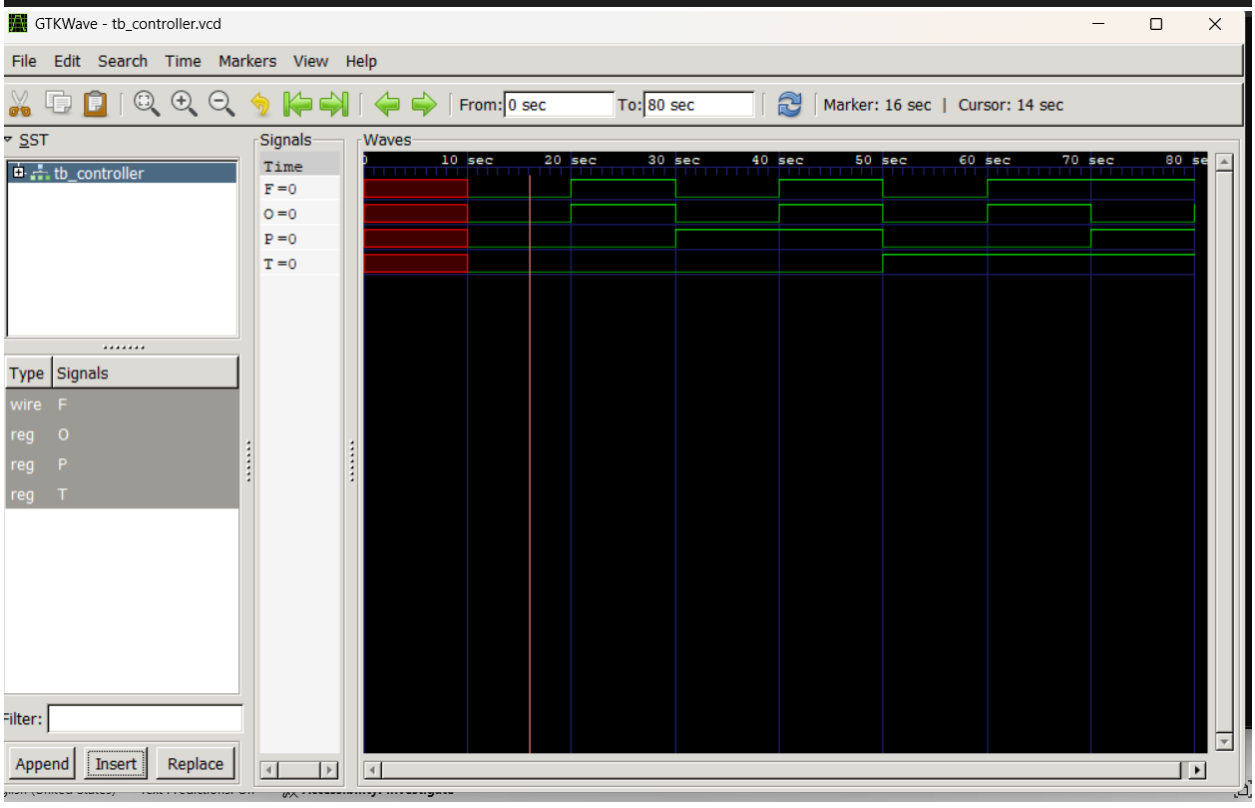
3.

tb_program3.v

```
1  module tb_controller;
2      reg T,P,O;
3      wire F;
4
       controller uut (T,P,O,F);
5      fan_controller uut (T,P,O,F);
6
7      initial begin
8
9          #10 T=0; P=0; O=0;
10         #10 T=0; P=0; O=1;
11         #10 T=0; P=1; O=0;
12         #10 T=0; P=1; O=1;
13         #10 T=1; P=0; O=0;
14         #10 T=1; P=0; O=1;
15         #10 T=1; P=1; O=0;
16         #10 T=1; P=1; O=1;
17     end
18
19 initial begin
20     $monitor($time,"T=%b P=%b O=%b F=%b",T,P,O,F);
21 end
22
23     initial begin
24         $dumpfile("tb_controller.vcd");    "dumpfile": Unknown word.
25         $dumpvars(0, tb_controller);    "dumpvars": Unknown word.
26     end
27
28 endmodule    "endmodule": Unknown word.
29
```

program3.v

```
1
2   module fan_controller(T, P, O, F);
3       input T,P,O;
4       output F;
5       wire TempPerson;
6
7       assign TempPerson=T&P;
8       assign F=TempPerson|O;
9
10  endmodule    "endmodule": Unknown word.
11
    module controller(T,P,O,F);
        input T,P,O;
12  module controller(T, P, O, F);
13      input T, P, O;
14      output F;
15
16      wire TempPerson;
17
18      and gate1(TempPerson, T, P);
19      or gate2(F, TempPerson, O);
20
21  endmodule    "endmodule": Unknown word.
22
23
```



```
D:\Iverlog>iverilog -o test program3.v tb_program3.v

D:\Iverlog>vvp test
VCD info: dumpfile tb_controller.vcd opened for output.
                   0T=x P=x O=x F=x
                  10T=0 P=0 O=0 F=0
                  20T=0 P=0 O=1 F=1
                  30T=0 P=1 O=0 F=0
                  40T=0 P=1 O=1 F=1
                  50T=1 P=0 O=0 F=0
                  60T=1 P=0 O=1 F=1
                  70T=1 P=1 O=0 F=1
                  80T=1 P=1 O=1 F=1
```