Review

Review on Short-Circuit Protection Methods for SiC MOSFETs

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Abstract: SiC MOSFETs have been a game-changer in the domain of power electronics, thanks to their exceptional electrical traits. They are endowed with a high breakdown voltage, reduced on-resistance, and superior thermal conductivity, which make them supremely suitable for high-power and resilient applications across aviation, automotive, and renewable energy sectors. Despite their intrinsic advantages, SiC MOSFETs also necessitate advanced safeguarding mechanisms to counteract the vulnerability to short-circuit conditions due to their lower short-circuit robustness. This review paper offers an in-depth analysis of the array of short-circuit protection (SCP) methods applied to SiC MOSFETs. This paper scrutinizes techniques such as desaturation detection, di/dt detection, gate charge characteristics monitoring, two-dimensional monitoring, Rogowski coil-based detection, and two-stage turn-off strategies. The paper meticulously explores the operational principles, merits, and limitations of each method, with an emphasis on their adaptability to various fault types, including hard switching faults and load-induced faults. This review acts as a thorough compendium, guiding the choice of pertinent SCP strategies, ensuring the secure and efficient functioning of SiC MOSFETs in demanding applications.

Keywords: silicon carbide (SiC) MOSFETs; short-circuit detection; short-circuit protection; desaturation method; di/dt detection; gate charge characteristics; Rogowski coil

1. Introduction

The rapid advancement in power electronics has led to the widespread adoption of silicon carbide (SiC) MOSFETs, especially in applications demanding high efficiency, high switching frequency, and superior thermal performance [1,2]. SiC metal–oxide–semiconductor field-effect transistors (MOSFETs), owing to their inherent material advantages over traditional silicon (Si) counterparts, have emerged as a pivotal component in modern power electronic systems; also, the integration of SiC MOSFETs with advanced transformer models, such as those operating in the ISM band, can potentially lead to more efficient and reliable power conversion systems [3]. These devices exhibit lower on-resistance, higher breakdown voltage, and significantly better thermal conductivity, making them ideal for high-voltage, high-temperature, and high-frequency applications [4–8].

One of the critical challenges associated with the deployment of SiC MOSFETs is ensuring reliable operation under fault conditions [9], particularly short-circuit (SC) events [10–14]. To lessen the negative impact of the subpar SiC/SiO_2 interface on the device's on-state resistance ($R_{ds,on}$), SiC MOSFETs have a shorter channel length and a thinner gate oxide layer [15,16]. Thus, SiC MOSFETs' maximum short-circuit current (I_{SC}) can exceed their rated current by up to 10 times [17–19]. Furthermore, SiC MOSFETs have a lower heat capacity and a higher short-circuit current density due to their smaller chip size when compared to Si insulated-gate bipolar transistor (IGBT) with identical voltage and current ratings [18]. As such, SiC MOSFETs have a poorer short-circuit tolerance capability than Si IGBTs, which causes SiC MOSFETs to break within a few microseconds as a result of gate failure or thermal runaway in a short-circuit event [11,20–22]. Therefore, short circuit protection (SCP) is essential to prevent catastrophic failures and enhance the longevity and

reliability of power systems incorporating SiC MOSFETs [23,24]. Traditional protection methods used for Si-based devices often fail when applied to SiC devices due to the distinct electrical and thermal characteristics of SiC [25,26]. As a result, SiC MOSFETs demand much faster reaction times due to their higher switching speeds and lower energy loss during switching events, making traditional, slower protection methods inadequate [9,27]. Additionally, SiC devices operate over a wider temperature range, typically from 200 K to 450 K, requiring more robust thermal management and protection strategies that traditional methods fail to provide [28]. Furthermore, in aerospace power systems, the complexity and reliability of the protection topology are crucial due to stringent requirements regarding electromagnetic interference (EMI) and power isolation [27]. Traditional methods often cannot meet these high-frequency operation conditions and stringent EMI standards without compromising reliability [25,26]. Therefore, specialized protection methods tailored to the unique characteristics of SiC devices are necessary to ensure their safe and efficient operation in advanced applications [29].

SCP for SiC MOSFETs is typically divided into two sections: SC detection and soft turn-off (STO), as shown in Figure 1. The detection phase involves identifying the occurrence of a short circuit as fast as possible, which is crucial for minimizing damage to the device and ensuring system reliability. Several SC detection methods have been proposed and implemented in recent years, as shown in Figure 1, each with its unique advantages and limitations. V_{GS} is the voltage between the gate and the source of the MOSFET, Q_G is the charge entering the gate, V_{DS} is a drain-to-source voltage, and I_{DS} is a drain-to-source current. These methods include desaturation detection [30], di/dt detection [31], gate charge (Q_G) monitoring [32], two-dimensional monitoring [33], power loss estimation [34], and the use of Rogowski coils [35], among others. Each method offers a different approach to detecting and mitigating short circuits, with varying degrees of effectiveness, complexity, and suitability for various applications. Once a short circuit is detected, the STO phase is initiated. Unlike abrupt turn-off methods, the STO process gradually reduces the gate voltage, allowing the MOSFET to transition smoothly from its conducting state to the non-conducting state [36]. This controlled reduction in current flow helps to minimize voltage overshoot and electromagnetic interference, reducing stress on the device and improving overall system stability. By combining effective detection mechanisms with an STO strategy, the short-circuit protection system ensures a robust response to fault conditions, safeguarding the device and enhancing its operational lifespan.

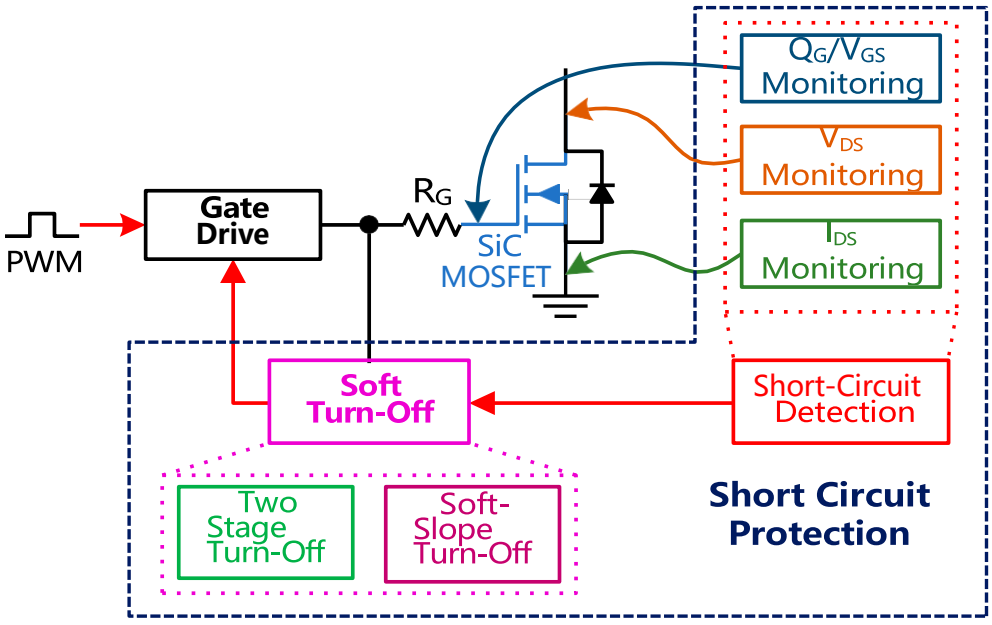

Figure 1. Short-circuit protection methods.

This paper provides a comprehensive review of the existing SCP methods for SiC MOSFETs. We analyze their working principles, advantages, and limitations, offering insights into their applicability in various power electronic systems. By understanding the strengths and weaknesses of these protection strategies, we aim to guide future research and development toward more robust and efficient SCP solutions for SiC MOSFETs. This review not only serves as a reference for engineers and researchers but also highlights the need for continued innovation in SCP technologies to fully harness the potential of SiC MOSFETs in next-generation power electronics.

2. Analysis of Short-Circuit Types

The following section cover the two main types of short circuits; hard-switching faults (HSFs) and faults under loads (FULs). HSF typically occurs during the rapid transition of a MOSFET from the off-state to the on-state. This situation is characterized by high levels of current flow while the voltage remains elevated, causing significant power dissipation. Such conditions are often caused by inadequate timing control or synchronization during the switching sequence, leading to premature activation of the MOSFET. Conversely, An FUL arises when a short circuit develops in the circuit while the MOSFET is already conducting load current. This can occur due to unexpected short circuits in the load, sudden increases in load demand that exceed the device's rated capacity, or failures in other components within the circuit, such as capacitors or inductors, which result in excessive currents. Figure 2a shows the schematic for test bench to simulate the HSF and FUL faults. Both fault conditions are discussed further in the following section.

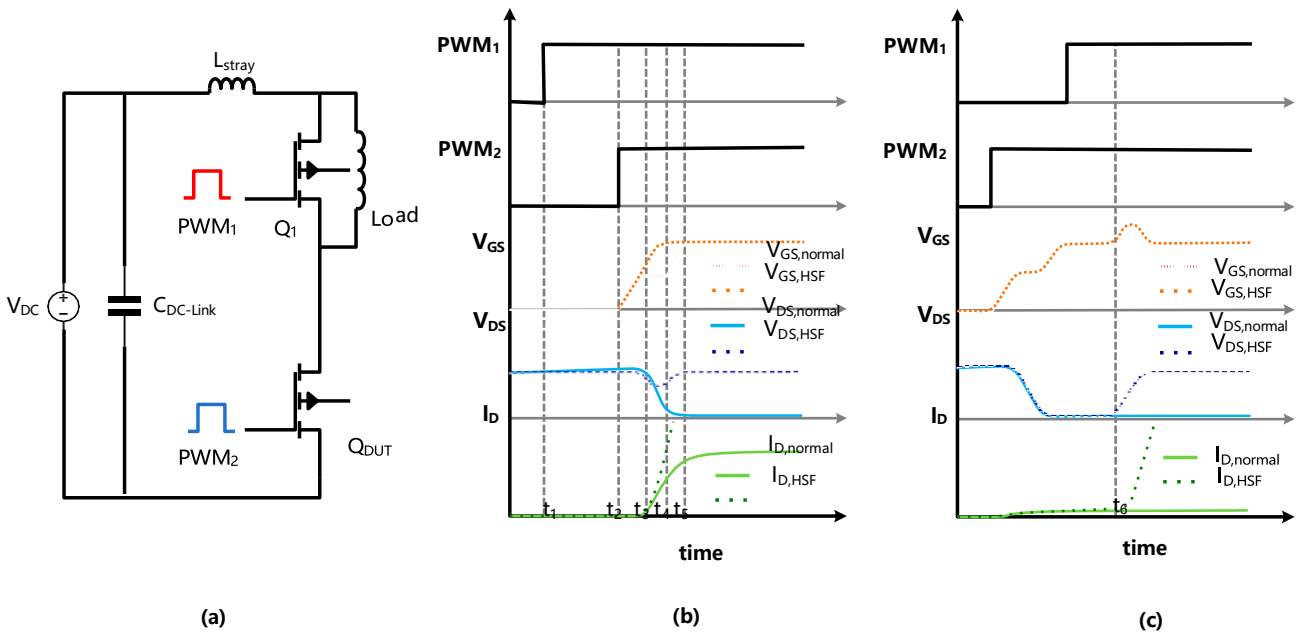

Figure 2. (**a**) Short circuit's test bench, (**b**) SiC MOSFET's parameters under an HSF and normal turn-on, and (**c**) SiC MOSFET's parameters under an FUL and normal turn-on.

2.1. HSF-Type Fault

An HSF occurs when a MOSFET is abruptly switched on into a short-circuit condition. From Figure 2a, when Q_1 (upper switch) is turned on, the current bypasses the load and flows through Q_1, where PWM_1 (pulse width modulation) and PWM_2 are gate signals for Q_1 and Q_{DUT} (device under test, i.e., the SiC MOSFET). By activating Q_1 before Q_{DUT} (device under test, i.e., the SiC MOSFET), an HSF is simulated, as a high short-circuit current will flow through the circuit when Q_{DUT} turns on. Figure 2b shows the behavior of the SiC MOSFET's different parameters under an HSF, which can be useful in detecting

fault conditions. This fault typically arises during the turn-on phase when the device is expected to conduct current but encounters a direct short circuit instead. An HSF is characterized by a high current spike upon turning on, leading to a very high peak current [37,38]. Simultaneously, V_{DS} drops rapidly to near zero as the MOSFET attempts to conduct the excessive current, resulting in a high rate of voltage change (dv/dt). This sudden transition subjects the device to significant thermal stress due to the instantaneous high-power dissipation. The protection challenge posed by HSFs necessitates extremely fast detection and response mechanisms to prevent device damage. Consequently, additional circuitry is typically required to quickly shut down the device upon fault detection, thereby protecting it from thermal and electrical overstress.

2.2. FUL-Type Fault

An FUL occurs when a MOSFET is already conducting current under normal operating conditions and then encounters a short-circuit fault. As shown in Figure 2a, the current path initially includes the load while Q_1 is off (and Q_{DUT} is on), indicating that the circuit is operating under normal load conditions. However, once Q_1 is turned on, the current bypasses the load and flows through Q_1 instead, simulating an FUL condition. The behavior of the various SiC MOSFET parameters under an FUL is shown in Figure 2c, which can help identify fault conditions. This type of fault can result from external factors such as load malfunction or a sudden short in the load path [39,40]. An FUL is characterized by a moderate rise in current, which increases to a high level but not as instantaneously as in an HSF, given that the device is already in the on-state and conducting current. The MOSFET may sustain this high current for a longer period, leading to gradual thermal stress buildup if the fault is not cleared promptly. Effective protection against FUL requires robust fault detection and protection mechanisms capable of managing a prolonged high current without immediate destruction. The protection scheme must also distinguish between normal load conditions and fault conditions to avoid false triggering and unnecessary interruptions.

Both HSF and FUL necessitate efficient short-circuit protection mechanisms to ensure the reliability and longevity of SiC MOSFETs. While an HSF demands ultrafast detection and response due to its abrupt nature, an FUL requires sustained current handling and reliable detection over an extended period. Advanced sensing techniques combined with rapid response circuitry are crucial for safeguarding SiC MOSFETs against these faults, particularly in high-performance applications such as aviation and other demanding environments.

3. SC Withstand Time Limits with the Usage of SiC MOSFETs

The short-circuit withstand time (SCWT) of SiC MOSFETs and Si IGBTs significantly differs due to their distinct material properties and device structures. SiC MOSFETs generally have a shorter SCWT compared to Si IGBTs. This discrepancy arises from the higher current density and smaller heat capacity of SiC MOSFETs, which result in faster thermal runaway during a short-circuit event [41].

Temperature and DC bus voltage also affect the SCWT of SiC MOSFETs [42]. According to [43], the SCWT for CREE 1st Generation (1G) SiC MOSFETs (1.2 kV) at 25 °C and 600 V DC bus voltage is 12 µs, decreasing to 11 µs at 200 °C, as described in Table 1. At 750 V and 200 °C, the SCWT further reduces to 7 µs. CREE 2nd Generation (2G) (1.2 kV) devices have an SCWT of 8 µs at 25 °C and 600 V, which decreases to 5 µs at 750 V and 200 °C. In contrast, 1.2 kV SiC MOSFETs from ROHMS exhibit a longer SCWT, i.e., 17 µs at 25 °C and 600 V, decreasing to 13 µs at 200 °C and 600 V, and further reducing to 11 µs at 200 °C and 750 V. These results indicate that the SCWT of SiC MOSFETs generally decreases with increasing temperature and DC bus voltage, underscoring the temperature-dependent nature of their short-circuit capability.

Table 1. Comparison of SCWT for CREE 1G, CREE 2G, and ROHM SiC MOSFETs at various temperatures and DC bus voltages.

SiC MOSFETs (1.2 kV)	Temperature/DC Bus Voltage	SCWT
CREE 1G	25 °C/600 V	12 µs
	200 °C/600 V	11 µs
	200 °C/750 V	7 µs
CREE 2G	25 °C/600 V	8 µs
	200 °C/600 V	8 µs
	200 °C/750 V	5 µs
ROHM	25 °C/600 V	17 µs
	200 °C/600 V	13 µs
	200 °C/750 V	11 µs

According to [44], the SCWT for the IKW25N120H3 IGBT (1.2 kV/25 A) is approximately 33 µs, with critical energy (*E*cr) values of 2772 mWs for HSFs and 2928 mWs for FULs at 25 °C, as shown in Figure 3. In comparison, the SCWT and *E*cr for the SiC MOSFET (C2M160120D) are around 10 µs and 400 mWs, respectively. Additionally, the SiC MOSFET (SCT2160KEC) has an SCWT of approximately 22 µs and an *E*cr of 900 mWs, as shown in Figure 3. The data reveal that SiC MOSFETs have a much shorter SCWT and lower *E*cr compared to IGBTs, meaning they can withstand a short circuit for a shorter duration and with less energy before failure occurs. This comparison is critical for understanding the trade-offs between SiC MOSFETs and IGBTs in high-power applications.

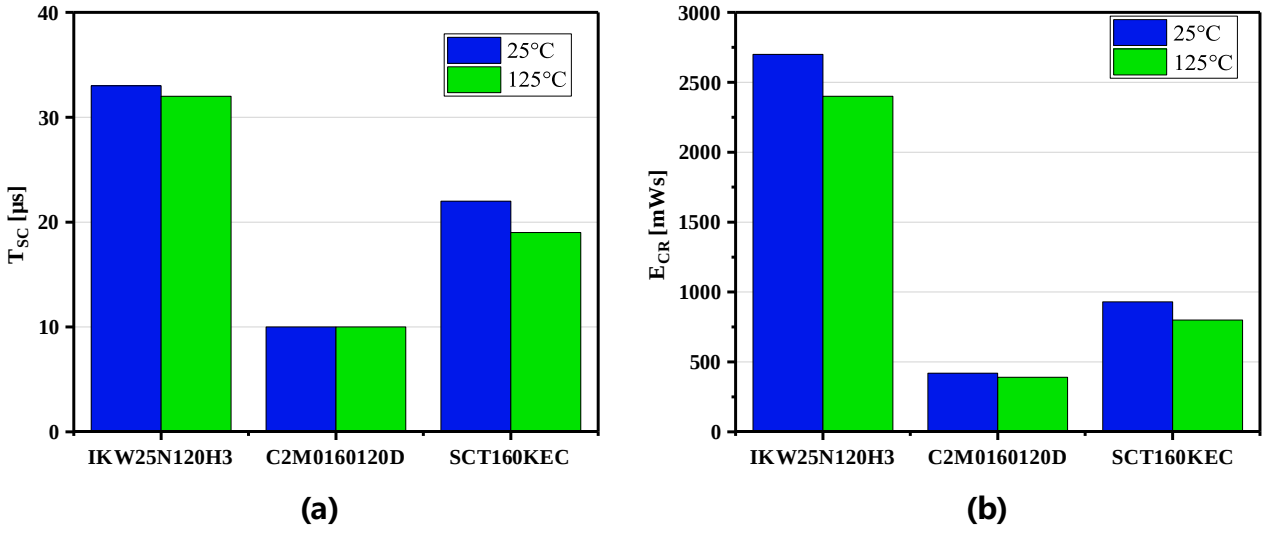

Figure 3. Analysis of short-circuit tolerance: Comparison of SiC MOSFET vs. Si IGBT in terms of (**a**) SCWT and (**b**) *E*cr.

4. Challenges in Short-Circuit Protection of SiC MOSFETs

In order to have a deeper comprehension of the obstacles and requirements related to the short-circuit protection of SiC MOSFETs, the corresponding challenges are presented as follows.

4.1. Device Structure of SiC MOSFET

The device structure of SiC MOSFETs is carefully engineered to balance $R_{ds,on}$ and short-circuit withstand capability. SiC MOSFETs often feature shorter channel lengths and thinner gate oxide layers to mitigate the negative impact of the poor quality SiC/SiO_2 interface on the device's $R_{ds,on}$. This design choice, however, introduces a trade-off [45–47]. Figure 4 shows the trade-off between short-circuit withstand time and normalized $R_{ds,on}$ for

SiC MOSFET [48]. Thinner gate oxide layers make the gate more vulnerable to damage due to high electric fields and leakage currents during short-circuit events [11,45]. Additionally, shorter channels lead to a more pronounced drain-induced barrier-lowering (DIBL) effect compared to Si IGBTs, causing a drift in threshold voltage (V_{th}). As described in [49], V_{th} decreases with increased V_{DS}, and the saturation current (I_C) can be expressed as:

$$I_C = \frac{Z \cdot \mu_i \cdot C_x (V_{GS} - V_{th})}{2L_{ch}} \quad (1)$$

where L_{ch} is the channel length, C_x is the gate oxide capacitance, μ_i indicates the electron mobility in the inversion layer, and Z indicates the channel width. Because of Equation (1), a drop in V_{th} results in a larger saturation current [50,51].

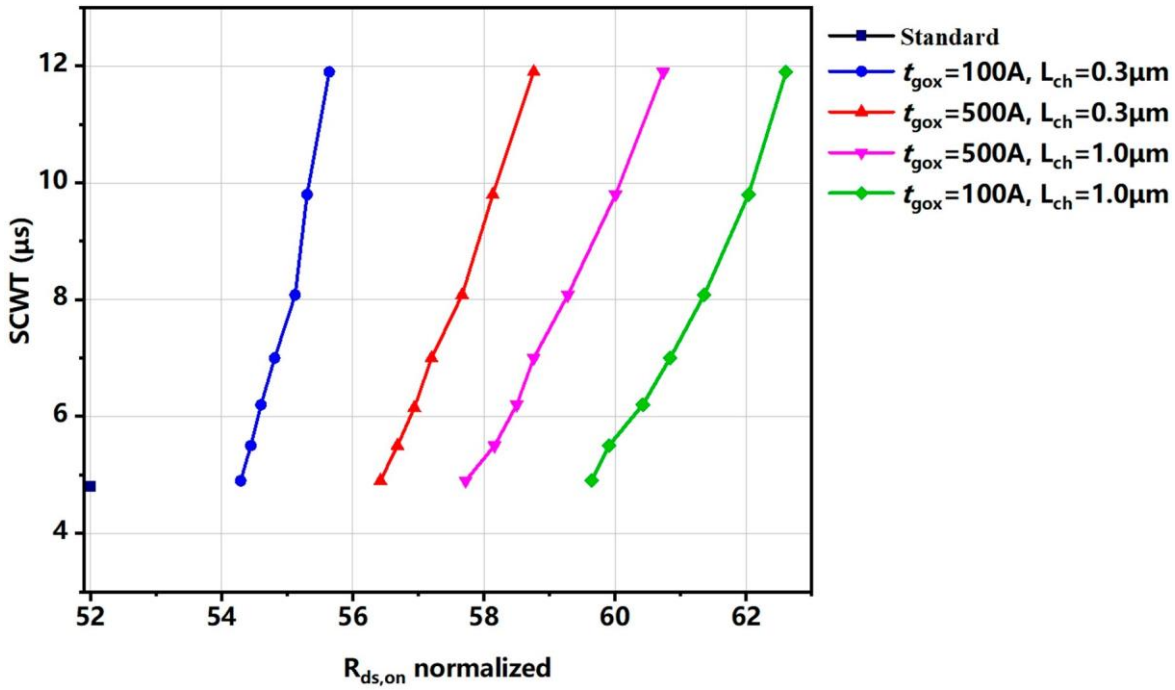

Figure 4. The trade-off curves between $R_{ds,on}$ and SCWT for the 1.2 kV SiC power MOSFET C2M0280120D with various Si GSS-DMM devices [48].

The channel resistance, which is a significant component of $R_{ds,on}$, contributes to the overall performance of SiC MOSFETs. To reduce $R_{ds,on}$, a thinner gate oxide layer and a shorter channel are designed, but these modifications can lower the short-circuit withstand capability. This structural vulnerability is further exacerbated by the DIBL effect, which affects the transconductance and causes the I_{DS} of SiC MOSFETs to vary widely with V_{DS}, as shown in Figure 5 [52]. This variation makes it challenging to detect short-circuit events based solely on the operating area.

Another critical aspect is the chip area, which is typically smaller in SiC MOSFETs compared to their Si counterparts, resulting in lower heat capacity [18]. During a short-circuit event, the relation between short-circuit energy (E_{SC}) and temperature variation (ΔT) is given by:

$$E_{SC} = cm\Delta T \quad (2)$$

where c is the heat capacity, m is mass, and ΔT represents temperature variation. Due to the smaller heat capacity, the junction temperature (T_j) of SiC MOSFETs rises more rapidly than that of Si IGBTs for the same short-circuit energy. Figure 6 shows the TCAD simulation of the SiC MOSFET's lattice temperature during short-circuit events showing that the

maximum lattice temperature can exceed 1000 K and reach the melting temperature of the aluminum electrode within microseconds [53].

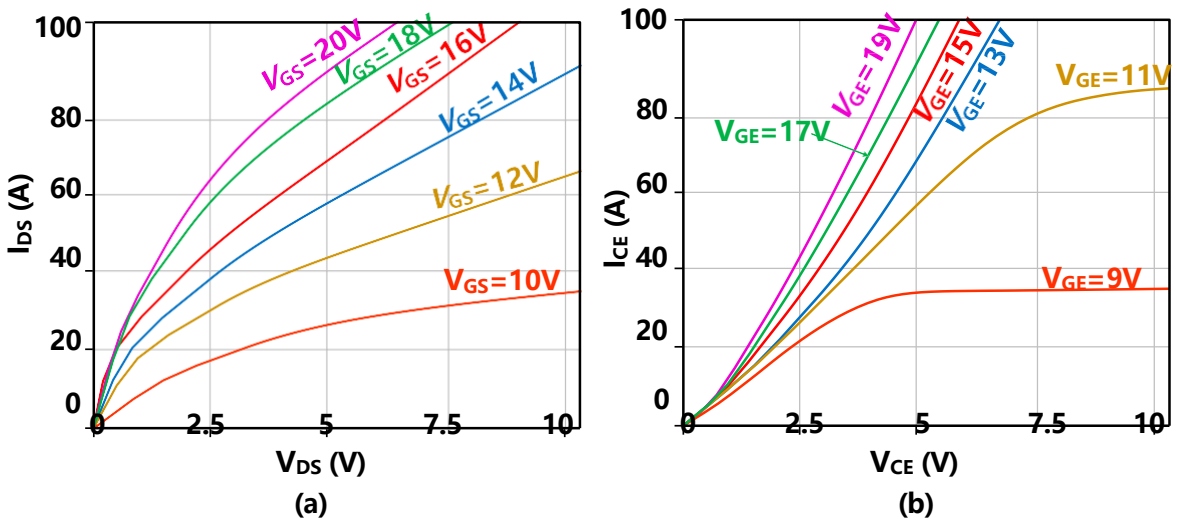

Figure 5. The output characteristics of a (**a**) SiC MOSFET and (**b**) a Si IGBT.

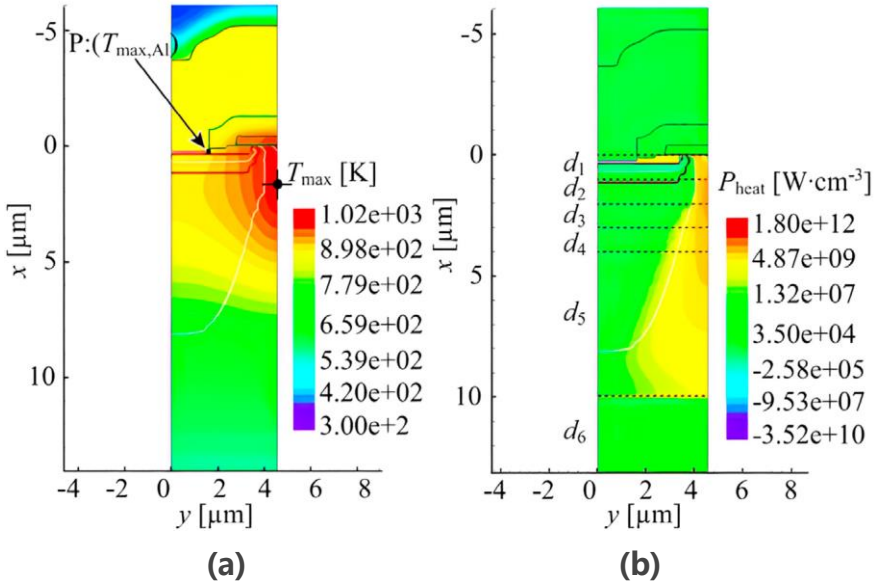

Figure 6. SC test verification: the 2D TCAD simulation (TCAD-SIMREF) of (**a**) the lattice temperature and (**b**) the volume heat distribution inside the power MOSFET structure at the end of the SC time (tsc = 11 μs) [53].

Under repetitive short-circuit conditions, the rapid rise in temperature within SiC MOSFETs can lead to severe consequences, particularly due to the thermal limits of the materials involved. As the junction temperature increases, especially near critical regions like the gate and drift regions, the heat can reach levels where aluminum, commonly used in the device's metallization, begins to melt. Aluminum has a melting point of approximately 660 °C, and if the localized temperature approaches this threshold, the integrity of the metal contacts can be compromised, potentially leading to catastrophic device failure [18].

Moreover, the elevated temperatures pose a significant risk to the insulation between the gate and drift regions, which is typically provided by a gate oxide layer made of silicon dioxide (SiO_2) [54]. This oxide layer is crucial for maintaining the electric field insulation between the gate and the underlying semiconductor material. However, excessive temperatures can degrade the gate oxide, resulting in several detrimental effects. First, the

insulating properties of the oxide may diminish, increasing the likelihood of gate leakage currents, which can cause the MOSFET to lose control and behave unpredictably. Second, if the thermal stress becomes too great, it can lead to electrical breakdown of the gate oxide, allowing current to flow directly between the gate and the drift region, effectively short-circuiting the device internally.

Furthermore, high temperatures can induce a shift in the threshold voltage (V_{th}) of the MOSFET, altering its switching behavior and reducing its efficiency. The combination of these factors, the melting of aluminum contacts, degradation of the gate oxide, and changes in electrical characteristics, significantly shortens the device's lifespan and reliability.

4.2. Switching Speed of SiC MOSFETs

SiC MOSFETs are known for their fast-switching speed, which is one of the primary advantages over their Si counterparts. This high-speed switching capability stems from several intrinsic properties of SiC as a material, as well as the design characteristics of SiC MOSFETs.

SiC has a wide bandgap of 3.26 eV, compared to Si's 1.12 eV [55]. This wide bandgap allows SiC devices to operate at higher temperatures and voltages with reduced leakage currents, facilitating faster switching transitions [56]. The higher critical electric field of SiC (approximately 10 times that of Si) enables the fabrication of devices with thinner drift regions and lower $R_{ds,on}$, contributing to the rapid switching performance.

Another significant factor is the low intrinsic carrier concentration in SiC, which reduces the charge storage in the device during switching [57]. This reduction minimizes the turn-off delay time and the total switching loss. The lower charge storage allows SiC MOSFETs to switch on and off more quickly, achieving higher frequencies with greater efficiency [58].

Furthermore, the fast-switching speed of SiC MOSFETs is advantageous in various applications, including power converters, motor drives, and high-frequency power supplies [59–62]. It allows for smaller passive components, reduced EMI, and higher efficiency in power conversion systems. The capability to operate at higher frequencies also leads to more compact and lightweight designs, which is particularly beneficial in applications like electric vehicles (EVs) and aerospace systems where size and weight are critical considerations.

Despite these benefits, the fast-switching speed of SiC MOSFETs poses some challenges. High dv/dt and di/dt associated with fast switching can induce significant EMI and noise in the system, which requires careful design and filtering to mitigate [63,64]. Additionally, the gate drive circuitry for SiC MOSFETs must be robust and capable of handling fast transients to ensure reliable operation.

5. Short-Circuit Detection Methods

SC detection for SiC MOSFETs is essential due to their unique electrical and thermal properties, which differ significantly from traditional Si-based devices. It usually consists of two parts, SC detection and STO.

SiC MOSFETs offer higher dv/dt and di/dt capabilities, faster-switching speeds, and higher operating temperatures, making conventional protection methods inadequate. To address these challenges, several innovative SC detection methods have been developed, each with specific advantages and limitations. These methods ensure the reliable operation of SiC MOSFETs, particularly in demanding applications like aerospace and automotive systems. The following sections explore these methods in detail, highlighting their working principles, benefits, and potential drawbacks. The current approaches for detecting short circuits can be classified into four groups based on the parameters being monitored V_{DS}-based detection, gate charge-based detection, I_{DS}-based detection, and combination detection method. These methods are listed in Table 2.

Table 2. Short-circuit detection methods for SiC MOSFET.

Parameters	Methods	Detectable Faults	Ref.
V_{DS}	V_{DS}	HSF and FUL	[30,65–67]
	dV_{DS}/dt	HSF	[68]
	$\int V_{DS}dt$	HSF and FUL	[69]
I_D	Rogowski coil	HSF and FUL	[35,70–78]
	dI_{DS}/dt	HSF and FUL	[30,79–84]
	TMR sensor	HSF and FUL	[73,85]
Gate	Q_G	HSF	[86–89]
	Gate leakage current	HSF and FUL	[32,86,90]
Combined	V_{GS} and dI_{DS}/dt	HSF and FUL	[33,91–93]
	V_{DS} and I_D	HSF and FUL	[34]

5.1. SC Detection Method Based on V_{DS} Monitoring

The desaturation method, as shown in Figure 7a, is a straightforward approach that monitors the V_{DS} to detect saturation, indicative of an SC [30,38,67,94–102]. When an SC occurs, V_{DS} quickly rises, triggering a shutdown. The desaturation detection circuit consists of a resistor, a blanking capacitor, and a diode, as shown in Figure 7a. When the device turns on, a current source charges the blanking capacitor and the diode starts conducting. During normal operation, the capacitor voltage is clamped at the forward voltage of the device. When an SC happens, the capacitor voltage is quickly charged to the threshold voltage, triggering the device shutdown. However, this method is very slow. As per [96], the desaturation method's SC detection time for a third-generation 10 kV SiC MOSFET under HSFs and FULs is approximately 1.5 µs.

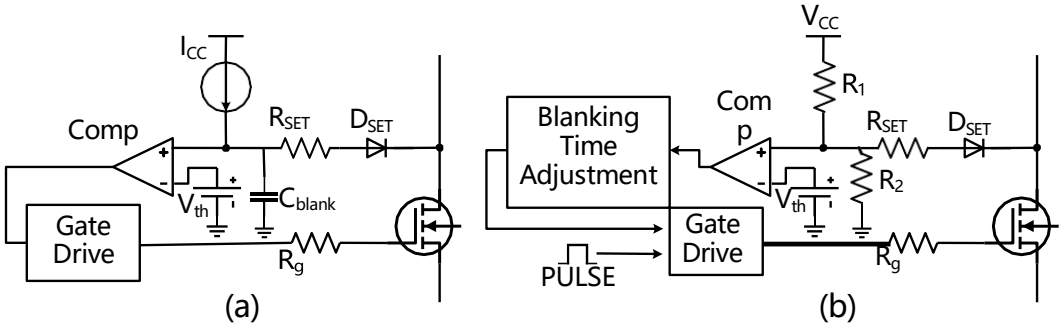

Figure 7. (**a**) Desaturation SCP circuit; (**b**) desaturation SCP with self-adjustive blanking time.

In [103], the blanking time for each switching period is adjusted by recording the V_{DS} fall time during each turn-on event and setting it as the blanking time for the next period, as shown in Figure 7b. This self-adjustive approach allows for a quick response to changes in the operating state without false triggering during normal switching transients. However, it introduces an adaptation delay ranging from several hundred nanoseconds to one microsecond. In [30], a Zener diode is added to block high-voltage pulses across blanking capacitor, and an extra diode is added across the resistor to fast discharge the capacitor during turn-off time, as shown in Figure 8a. Based on the short-circuit characteristic of SiC MOSFETs, where the short-circuit withstand time decreases as the DC bus voltage increases [104], the desaturation conduction voltage integral ($\int V_{DS}dt$)-based SC detection method was proposed in [69] and is shown in Figure 8b. This method's response speed for SC detection improves with the increase in DC bus voltage. The dv/dt detection method for SiC MOSFETs operates by monitoring the rate of change in V_{DS} [68]. During a short-circuit event, the V_{DS} increases rapidly, generating a significant dv/dt signal. This rapid change is detected by a dedicated circuit, which typically includes a high-speed comparator and a threshold-setting component, as shown in Figure 9.

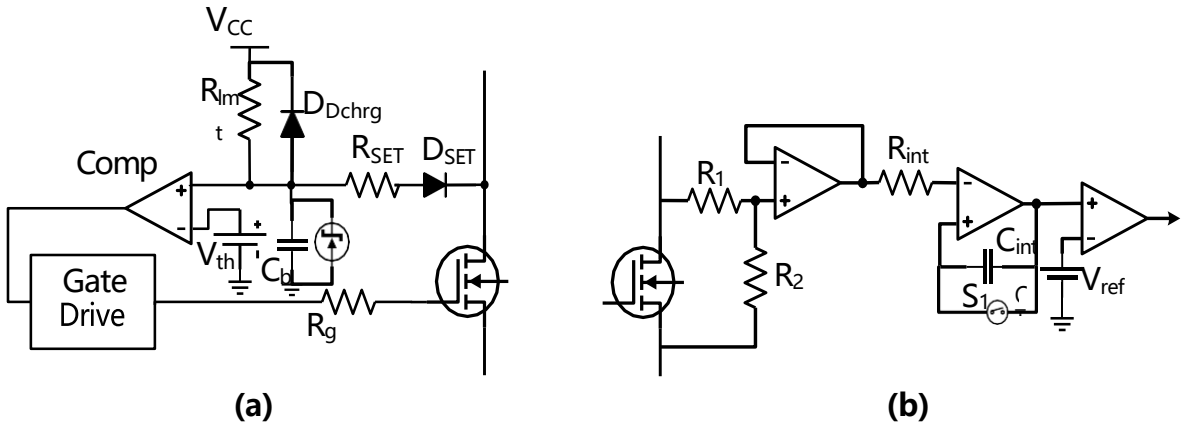

Figure 8. Desaturation methods: (**a**) with fast C_b discharging; (**b**) $\int V_{DS} dt$.

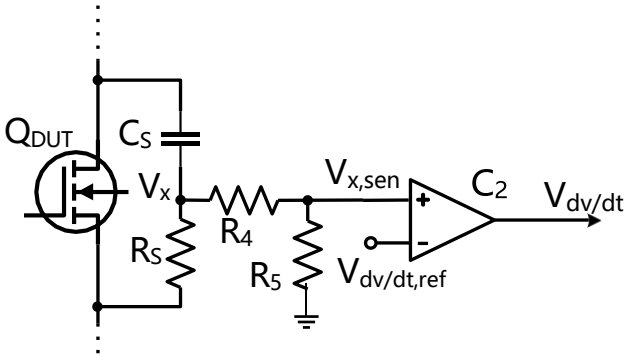

Figure 9. dv/dt detection method.

5.2. SC Detection Method Based on I_{DS} Monitoring

One of the direct I_S measurement methods is based on Rogowski coil for non-intrusive current sensing, providing a lightweight and non-intrusive design [35,70–78,90], as shown in Figure 10. The article in [35] introduces a PCB coil design based on a single interconnect trace for TO-247-4 L-packaged SiC MOSFETs. The interconnect, connecting the DC busbar to the SiC MOSFET terminal, generates flux linkages with a nearby PCB coil, achieving a mutual inductance of 0.175 nH per mm^3. This mutual inductance is significantly higher than that of a laminated busbar PCB coil design and attests to the efficacy of this design in extracting a high sensitivity with a compact coil size. The compact coil not only minimizes intrusion within the power loop but also yields a high natural frequency of 469 MHz. This high frequency enables a broad bandwidth for the current sensor, essential for implementing an ultrafast protection scheme. Additionally, the coil design, intricately linked to the interconnect trace length, allows control over mutual inductance and power-loop stray inductance by adjusting the trace length. Three-dimensional finite-element method simulations in COMSOL guide the selection of the interconnect trace length, minimizing power-loop stray inductance. This design methodology was applied to demonstrate a half-bridge circuit with PCB coils for current sensing of TO-packaged devices, showcasing a novel protection circuit with an impressive response time improvement from 86 ns to 25 ns compared to the existing state of the art. However, it comes with integration complexity, has a specific bandwidth, and is costly to produce.

A second I_{DS}-based detection method is Tunnel Magnetoresistance (TMR)-based SC detection method. These sensors are highly sensitive, respond quickly, and resist electromagnetic interference, making them ideal for SiC MOSFET applications. The TMR sensor detects changes in the magnetic field caused by a high current flow during a short circuit and promptly signals the protection circuit to shut down the MOSFET, preventing damage. A TMR current sensor, depicted in Figure 11, consists of a Wheatstone bridge

and a gain amplifier [73]. The TMR chip's output voltage (ΔV) is directly proportional to the magnetic flux density (B), which, according to Ampere's law, is proportional to the detected I_{DS}. Through linear amplification, the sensor's output voltage (v_m) maintains a proportional relationship with the current I_S.

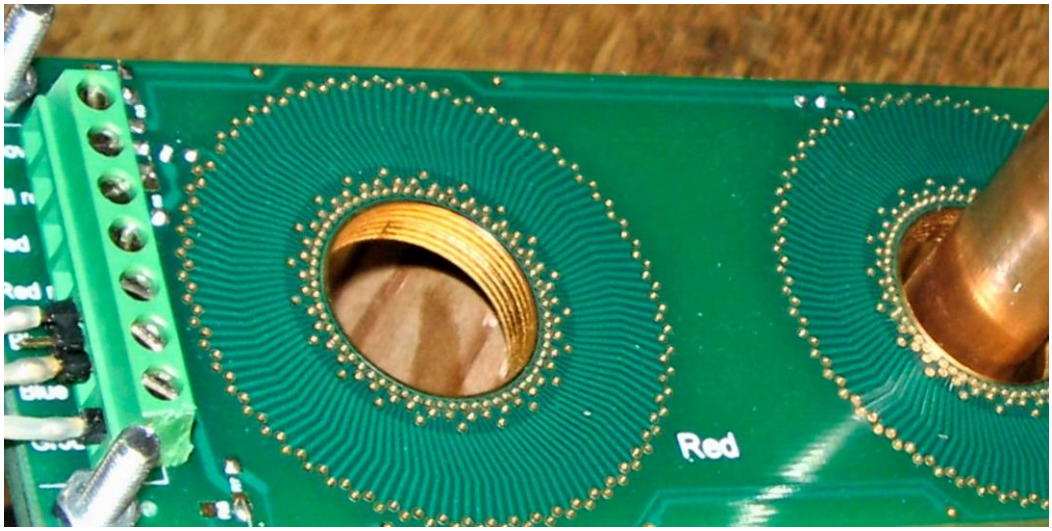

Figure 10. PCB-based Rogowski coil.

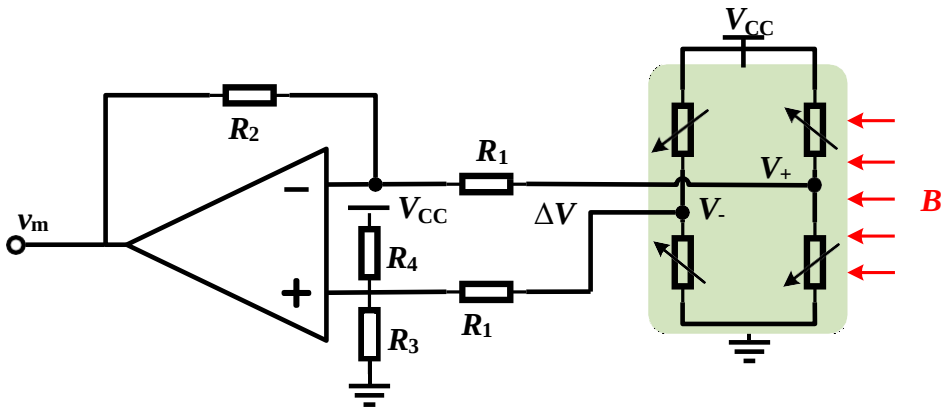

Figure 11. TMR Sensor [85].

A few more direct I_{DS}-based detection methods include Hall effect sensor, shunt, current transformer, on-chip sensor, etc. [105,106]. These current sensors can accurately monitor I_D, effectively preventing I_{SC} from rising to critical levels. However, many of these sensors have limitations when it comes to short-circuit detection applications.

Hall effect sensors detect the induced voltage generated by the measured current's magnetic field [107]. Hall effect sensors can measure current accurately, but they are expensive and susceptible to loop magnetic fields [108]. Although shunts are simple to install, they lead to increased switching loss and conduction loss [109]. Based on magnetoresistance effects, magneto-resistive current sensors are compact and exhibit a high sensitivity [106].

The indirect detection method is to detect the rate of change in current (di/dt) flowing through the parasitic inductance of the device [30,79–84], as shown in Figure 12a. This detected di/dt is then processed through a resistive–capacitive (RC) low-pass filter designed to restore the fast-changing current dynamics. The filtered di/dt is subsequently compared with a predefined threshold value, and if the calculated di/dt surpasses this threshold, indicative of a rapid change in current associated with an SC, the protective circuit is activated. However, under various fault scenarios, especially under FULs, it does not yield

consistent outcomes [31], leading to detection failure as C_S discharges after I_{DS} becomes steady after turn-on and rises again at the FUL. However, the rise in I_D under an FUL is less than under an HSF; thus, it requires two different thresholds for HSFs and FULs. Therefore, in [31], a different di/dt-RCD (RC + diode) protective circuit has been suggested to provide more precise and reliable results regardless of the fault types, as shown in Figure 12b, by adding a diode in series with R_S and L_{SS} to prevent C_S from discharging when the current is constant. While RC and RCD perform similarly for HSFs, i.e., the SCP time is around 100 ns, the RCD method demonstrates a faster detection time for FULs, achieving 72 ns compared to the RC method's 100 ns.

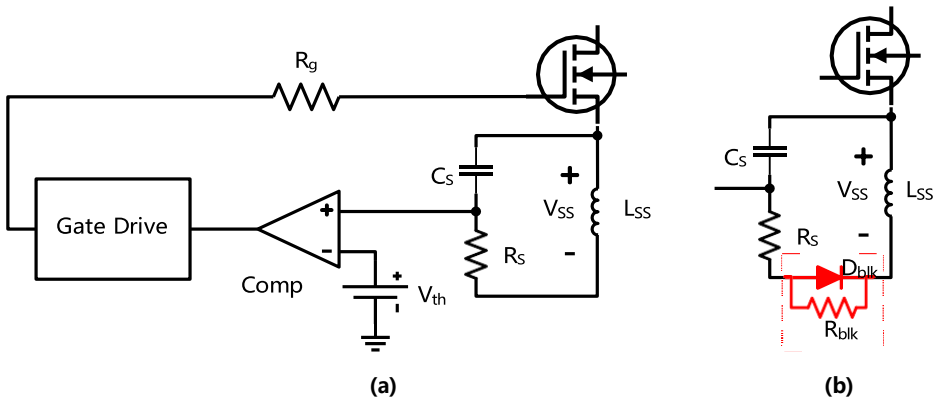

Figure 12. di/dt detection method: (**a**) RC integrator; (**b**) RCD integrator.

5.3. SC Detection Method Based on Gate Charge Monitoring

The gate charge-based SC detection method is a sophisticated approach used to identify and protect against short-circuit conditions in power semiconductor devices, such as SiC MOSFETs [32,86–89]. This method focuses on monitoring the gate charge dynamics to distinguish between normal operation and short-circuit events. In SiC MOSFETs, the total gate charge (Q_G) during the turn-on process consists of several stages: the initial charging of the gate-source capacitance (C_{GS}), the charging of the gate-drain capacitance (C_{GD}) during the Miller plateau, and the final charge saturation as the device reaches full conduction. As shown in Figure 13, under normal operating conditions, the presence of the Miller plateau results in a prolonged turn-on time, where both C_{GS} and C_{GD} charge gradually. During normal operation, the gate charge curve exhibits a clear Miller plateau characterized by simultaneous charging of C_{GS} and C_{GD} from the initial time to the Miller plateau, followed by a period dominated by the C_{GD} charge. The total gate charge (Q_{nor}) is the sum of charges during these intervals, resulting in a higher overall charge compared to fault conditions.

In contrast, during a short-circuit event like HSF, the V_{GS} rapidly reaches the preset level, quickly charging C_{GS} and C_{GD} without the typical delay caused by the Miller plateau. This results in a lower total gate charge (Q_{SC}) compared to normal operation, as the absence of a Miller plateau shortens the overall charging duration. The gate charge-based SC detection method leverages the difference in total gate charge between normal and fault conditions. As shown in Figure 14, by monitoring the V_{GS} and comparing the total gate charge to a reference threshold (Q_{ref}), the system can accurately detect short-circuit events. The protection mechanism is triggered when V_{GS} exceeds a predefined reference value, and the total gate charge remains below Q_{ref}, indicating an abnormal charging pattern indicative of a short circuit. This method offers precise detection of short-circuit events by focusing on the unique charging characteristics of the gate, allowing for rapid response times. It reduces false positives by analyzing the total gate charge alongside V_{GS}, distinguishing between normal switching transients and genuine fault conditions. Additionally, the gate charge-based method is particularly well suited for SiC MOSFETs, characterized by fast switching speeds and sensitive gate charge dynamics. Overall, the gate charge-based short-

circuit detection method provides a sophisticated and effective means of identifying and mitigating short-circuit events in power semiconductor devices, enhancing the reliability and safety of power electronic systems, especially those utilizing SiC MOSFETs.

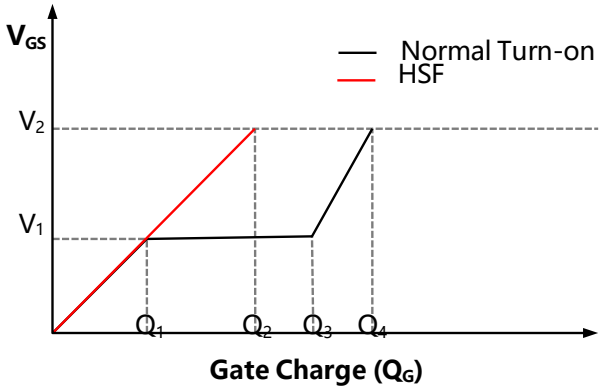

Figure 13. Q_G vs. V_{GS} response under an HSF and normal turn-on.

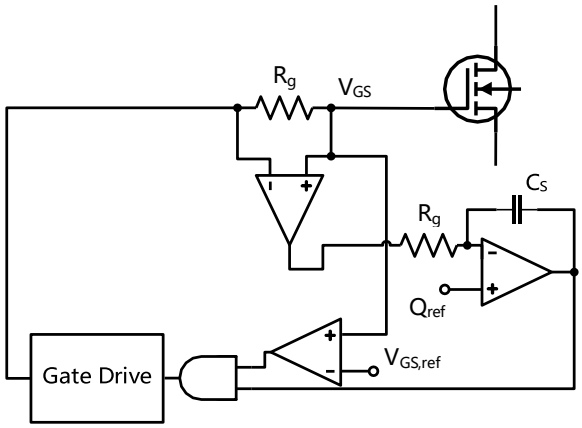

Figure 14. Gate charge characteristics method [89].

5.4. Two-Dimensional SC Detection Method

The two-dimensional method enhances fault detection by simultaneously monitoring both V_{GS} and I_{DS} [33,91–93]. As shown in Figure 15, it relies on the premise that specific fault conditions, such as SCs or abnormal load scenarios, induce distinctive changes in the V_{GS} and I_D characteristics. By analyzing the coordinated behavior of these parameters, the protection circuit distinguishes normal operation from potential fault conditions. The method involves establishing criteria for fault detection based on the relationship between V_{GS} and I_{DS}, allowing for a more comprehensive approach to identifying deviations from expected behavior. Monitored V_{GS} and I_D values are compared with predetermined threshold levels, and if deviations beyond these thresholds are detected, the protection mechanism is promptly activated. The response often entails the immediate shutdown of the SiC MOSFET to prevent further damage. While offering enhanced sensitivity and comprehensive fault detection capabilities, the method may introduce increased circuit complexity compared to single-parameter approaches, necessitating precise threshold calibration for accurate fault detection. The two-dimensional method finds applications in critical systems where a thorough understanding of both V_{GS} and I_D behavior is crucial for effective fault detection and rapid protective response. This versatility makes it suitable for various fault conditions, though it requires additional circuits, potentially introducing complexity.

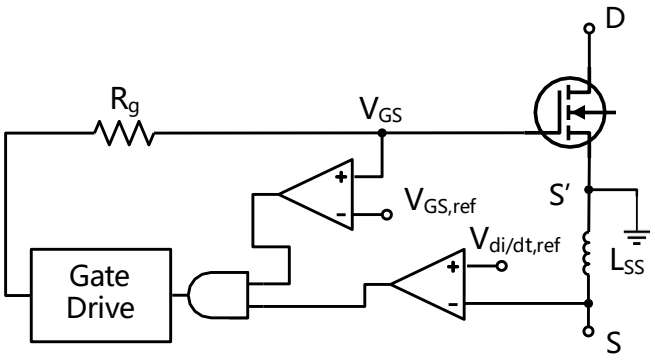

Figure 15. Two-dimensional protection method.

Another combined method is power loss estimation, which estimates the power loss of a SiC MOSFET by monitoring V_{DS} and I_D to identify abnormal conditions [34]. Inspired by the abovementioned method, an indirect power dissipation level short-circuit protection (IPDL-SCP) method is proposed in [34], while using as few components as possible. The method monitors the voltage oscillation of the source parasitic inductance (V_{SS}) combined with the V_{DS} of the SiC MOSFET, as shown in Figure 16. The protection is activated when both characteristics exceed safety values, indicating that the SiC MOSFET has already operated in overpowering conditions. While offering insights into power dissipation, this method demands accurate calibration and introduces additional losses. Table 3 summarizes all the conventional methods.

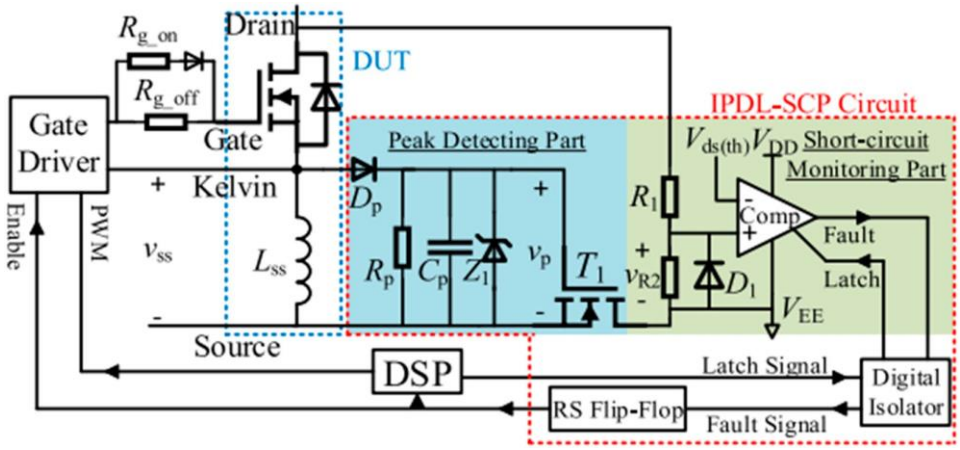

Figure 16. The indirect power dissipation SCP [34].

Table 3. Comparison between conventional SC detection methods.

Parameters	Methods	Noise Immunity	Temp. Effect	Cost/Complexity	Response Time		Ref.
					HSF	FUL	
V_{DS}	V_{DS}	Low	High	Low/simple	450 ns~1.5 µs	1.5 µs	[30,65–67]
	dV_{DS}/dt	Low	High	Low/moderate	250 ns	-	[68]
		Low	High	Low/moderate	700 ns	1.5 µs	[69]
I_D	Rogowski coil	High	Low	High/complex	<100 ns	<100 ns	[35,70–78,90]
	dI_{DS}/dt	Moderate	Low	Moderate/moderate	<100 ns	<100 ns	[30,79–84]
	TMR sensor	High	Low	High/complex	<100 ns	<100 ns	[73,85]
Gate	Q_G	Low	High	Moderate/moderate	173 ns	-	[86–88,110]
	Gate leakage current	Low	High	Moderate/complex	137 ns	86 ns	[90]
Combined	V_{GS} and dI_{DS}/dt	Moderate	Moderate	High/complex	<50 ns	<100 ns	[33,91–93]
	V_{DS} and I_D	Moderate	Low	High/complex	-	170 ns	[34]

6. Soft Turn-Off Strategy for SiC MOSFETs during SC

After detecting a short circuit, the next step is to initiate the turn-off process to prevent the device from overheating and potential damage. In case of a short circuit, a SiC MOSFET cannot be abruptly turned off due to the potential for dangerous voltage spikes in V_{DS}. Voltage spikes occur when the current flow is abruptly stopped due to the inductive elements present in the circuit, such as inductors, transformers, or even parasitic inductances within components and wiring. Inductive components store energy in their magnetic fields while current flows through them. When this current is suddenly interrupted, the stored energy has no gradual path for dissipation, resulting in a high voltage spike as the inductor attempts to maintain current flow. Instead of abruptly stopping current flow, which can cause high voltage spikes and potential damage, STO gradually reduces the current, minimizing excessive voltage transients and stress on both the device and surrounding circuitry. This gradual reduction also helps prevent high voltage spikes that could exceed the device's voltage ratings, thus avoiding breakdown or failure. Additionally, STO mitigates EMI by lowering the rate of change in current and voltage, which contributes to overall circuit stability. It also reduces thermal and electrical stress on the device, protecting it from damage and thermal runaway, which can lead to catastrophic failure. By smoothing the transition from the on to off state, STO improves the device's reliability and longevity, extending its operational life and enhancing overall system performance. Several STO methods are described below, including the soft slope turn-off, two-step turn-off, and multi-step turn-off methods [36,67].

STO significantly influences the junction temperature and lifecycle of SiC MOSFETs during short-circuit conditions. By gradually reducing the current flow rather than abruptly stopping it, STO helps control the rate of thermal rise within the device, effectively managing the junction temperature. This gradual decrease in current minimizes sudden heat generation, reducing thermal stress and preventing rapid temperature spikes. As a result, the junction temperature remains within safer limits, reducing the risk of thermal runaway and damage. Additionally, STO extends the operational lifespan of SiC MOSFETs by mitigating high thermal and electrical stresses that could otherwise lead to premature degradation of the device. Improved thermal management and reduced mechanical stress contribute to enhanced reliability and performance, ensuring that the device remains intact and functional over a longer period. Several STO methods are described below, including the soft slope turn-off, two-step turn-off, and multi-step turn-off (MSTO) methods [36,67].

6.1. Soft Slope Turn-Off Method

The soft slope turn-off method gradually reduces the gate voltage, allowing for a controlled decrease in drain current, as shown in Figure 17. This approach uses an adjustable STO current determined by a resistor (R_{soft}), which makes it relatively easy to implement on-chip. However, it requires customization for different SiC MOSFETs due to input capacitance (C_{GS}) variations across devices. The STO time must be optimized for various SiC MOSFET sizes and current capacities, often necessitating additional circuitry for proper adjustment.

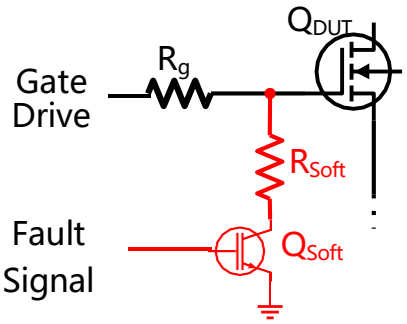

Figure 17. Soft slope turn-off.

6.2. *Two-Step Turn-Off Method*

In contrast, the two-step turn-off method employs a two-stage approach using a Zener diode and a sinking MOSFET, as shown in Figure 18. Initially, it clamps the V_{GS} to an intermediate level, allowing for a gradual decrease in drain current, followed by a complete turn-off by the main driver [36]. This method provides a more consistent STO time regardless of the SiC MOSFET's current capacity, making it easier to implement across different devices without extensive customization. However, it may produce two V_{DS} spikes during the two-stage clamping operation. Both methods aim to reduce stress on the SiC MOSFET during turn-off under short-circuit conditions, offering different trade-offs regarding implementation complexity and performance across various device specifications.

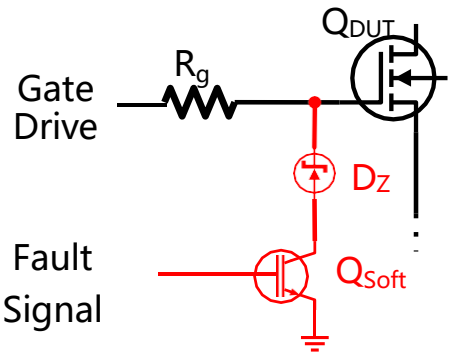

Figure 18. Two-step turn-off.

6.3. *Multi-Step Turn-Off Method*

In multi-step STO as shown in Figure 19, a MOSFET array controlled by an 8-bit digit is integrated in the gate driver [111]. After an overcurrent signal is generated, the MSTO circuit begins to sense V_{DS} by connecting with the external capacitor, to control the MOSFET array according to the VDS variation. An external capacitor is applied, coupling V_{DS} with V_{CPL}. In addition, the MSTO controller has a delay of ~15 ns, including a settling time of V_{CPL} after connecting to the external capacitor, propagation, and comparison delay of the controller. The V_{CPL} voltage is converted to an 8-bit thermometer code through the flash ADC in real time. The 8-bit codes determine the number of on/off MOSFETs required in the MOSFET array. This allows for real-time control of the number of MOSFETs turned off. This adjustment helps manage the sinking current and reduces VDS overshoot, enhancing the reliability of SiC devices in high-voltage applications. A comparison of different STO techniques is presented in Table 4.

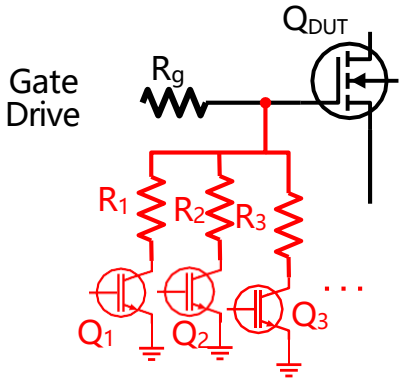

Figure 19. Multi-step STO.

Table 4. Comparison between different STO methods.

STO Methods	Advantages	Disadvantages	Delay Time
SOFT-SLOPE STO	- Reduced voltage spikes - Improved EMI performance - Enhanced device reliability - Simple design	- Slower response time - Increased switching losses	- 900 ns [36]
TWO-STEP STO	- Optimized trade-off between switching speed and voltage spikes - Reduced EMI - Moderate circuit design	- Potential VDS peak - Moderate switching losses - Potential for intermediate stress	- 500 ns [36]
MULTI-STEP STO	- Enhanced control over switching - Minimized voltage spikes and EMI - Superior protection	- Highest complexity - Implementation challenges - Increased overall losses	- 166 ns~1642 ns [111]

7. Conclusions

This article offered a detailed overview of the latest research on short-circuit protection for SiC MOSFETs. It began by outlining the challenges related to the device structure and the consequences of faster switching speeds. The paper then categorized and described advanced short-circuit detection methods into four key types: V_{DS}-based detection, gate charge-based detection, I_{DS}-based detection, and two-dimensional (2D) detection methods. Each method's principles, advantages, and limitations were thoroughly examined. The article also reviewed STO techniques used in short-circuit situations. Advancing SiC MOSFET protection will support broader use in high-power applications, driving innovation and efficiency in power electronics. This review provides a foundation for future research, aiming for more reliable and efficient power systems across industries.

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References

1. Wang, J.; Jiang, X. Review and Analysis of SiC MOSFETs' Ruggedness and Reliability. *IET Power Electron.* **2020**, *13*, 445–455. [CrossRef]
2. Tawfik, M.A.; Ehab, M.; Ahmed, A.; Park, J.H. Single-Stage Isolated DC/AC Converter with Continuous Dynamic Model and Controller Design. *IEEE Trans. Ind. Electron.* **2023**, *70*, 5971–5981. [CrossRef]
3. Ehab, M.; Tawfik, M.A.; Munir, M.U.; Ahmed, A.; Park, J.H. ISM-Band Frequency Transformer Modeling for Isolated High-Power Conversions. *IEEE Trans. Instrum. Meas.* **2023**, *72*, 8002111. [CrossRef]
4. Umegami, H.; Harada, T.; Nakahara, K. Performance Comparison of Si IGBT and SiC MOSFET Power Module Driving IPMSM or IM under WLTC. *World Electr. Veh. J.* **2023**, *14*, 112. [CrossRef]
5. Fuentes, C.D.; Müller, M.; Bernet, S.; Kouro, S. SiC-Mosfet or Si-IGBT: Comparison of Design and Key Characteristics of a 690 V Grid-Tied Industrial Two-Level Voltage Source Converter. *Energies* **2021**, *14*, 3054. [CrossRef]
6. Sun, J.; Yang, S.; Xu, H.; Zhang, L.; Wu, X.; Sheng, K.; Chen, K.J. High-Temperature Characterization of a 1.2-KV SiC MOSFET Using Dynamic Short-Circuit Measurement Technique. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 215–222. [CrossRef]
7. Maheri, H.M.; Babaei, E.; Sabahi, M.; Hosseini, S.H. High Step-Up DC-DC Converter with Minimum Output Voltage Ripple. *IEEE Trans. Ind. Electron.* **2017**, *64*, 3568–3575. [CrossRef]

8. Tawfik, M.A.; Munir, M.U.; Fayyaz, S.; Ahmed, A.; Park, J.H. Design, Optimization, and Control of an Isolated Single-Stage Fixed-Frequency Resonant DC/AC Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2024**, *12*, 2500–2516. [CrossRef]
9. Shi, B.; Ramones, A.I.; Liu, Y.; Wang, H.; Li, Y.; Pischinger, S.; Andert, J. A Review of Silicon Carbide MOSFETs in Electrified Vehicles: Application, Challenges, and Future Development. *IET Power Electron.* **2023**, *16*, 2103–2120. [CrossRef]
10. Wu, Y.; Li, C.; Zheng, Z.; Wang, L.; Zhao, W.; Zou, Q. A Behavior Model of SiC DMOSFET Considering Thermal-Runaway Failures in Short-Circuit and Avalanche Breakdown Faults. *Electronics* **2024**, *13*, 996. [CrossRef]
11. Unger, C.; Pfost, M. Particularities of the Short-Circuit Operation and Failure Modes of SiC-MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 6432–6440. [CrossRef]
12. Zhou, Y.; Liu, H.; Mu, S.; Chen, Z.; Wang, B. Short-Circuit Failure Model of SiC MOSFET Including the Interface Trapped Charges. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 90–98. [CrossRef]
13. Barazi, Y.; Richardeau, F.; Jouha, W.; Reynes, J.M. Vds and Vgs Depolarization Effect on Sic Mosfet Short-Circuit Withstand Capability Considering Partial Safe Failure-Mode. *Energies* **2021**, *14*, 7960. [CrossRef]
14. Wu, R.; Mendy, S.; Agbo, N.; Gonzalez, J.O.; Jahdi, S.; Alatise, O. Performance of Parallel Connected Sic Mosfets under Short Circuits Conditions. *Energies* **2021**, *14*, 6834. [CrossRef]
15. IEEE Power Electronics Society; IEEE Electron Devices Society; Power Sources Manufacturers Association; Institute of Electrical and Electronics Engineers. Isolated active-clamped SEPIC PFC converter based on SiC devices and integrated magnetics. In Proceedings of the WiPDA 2019: 7th Annual IEEE Workshop, Wide Bandgap Power Devices & Applications, Raleigh, NC, USA, 29–31 October 2019; ISBN 9781728137612.
16. Agarwal, A.; Baliga, B.J. Performance Enhancement of 2.3 KV 4H-SiC Planar-Gate MOSFETs Using Reduced Gate Oxide Thickness. *IEEE Trans. Electron. Devices* **2021**, *68*, 5029–5033. [CrossRef]
17. Romano, G.; Fayyaz, A.; Riccio, M.; Maresca, L.; Breglio, G.; Castellazzi, A.; Irace, A. A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 978–987. [CrossRef]
18. Reigosa, P.D.; Iannuzzo, F.; Luo, H.; Blaabjerg, F. A Short-Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules. *IEEE Trans. Ind. Appl.* **2017**, *53*, 2880–2887. [CrossRef]
19. Qu, X.; Wang, H.; Zhan, X.; Blaabjerg, F.; Chung, H.S.H. A Lifetime Prediction Method for LEDs Considering Mission Profiles. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; IEEE: Piscataway, NJ, USA, 2016. ISBN 9781467395502.
20. IEEE Power Electronics Society; IEEE Electron Devices Society; Power Sources Manufacturers Association; Institute of Electrical and Electronics Engineers. Loss Characterization and Analysis of High Voltage E-mode GaN HEMT in Soft-switching Application. In Proceedings of the WiPDA 2018: 6th Annual IEEE Workshop on Wide Bandgap Power Devices & Applications, Atlanta, Georgia, 31 October–2 November 2018; ISBN 9781538659090.
21. Institute of Electrical and Electronics Engineers; IEEE Electron Devices Society; IEEE Industry Applications Society; IEEE Power Electronics Society. Artificial Neural Network-Based (ANN) Approach for Characteristics Modeling and Prediction in GaN-on-Si Power Devices. In Proceedings of the 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Virtual, 13–18 September 2020; ISBN 9781728148366.
22. Unger, C.; Pfost, M. Thermal Stability of SiC-MOSFETs at High Temperatures. *IEEE Trans. Electron. Devices* **2019**, *66*, 4666–4672. [CrossRef]
23. Yu, R.; Jahdi, S.; Alatise, O.; Ortiz-Gonzalez, J.; Munagala, S.P.; Simpson, N.; Mellor, P. Measurements and Review of Failure Mechanisms and Reliability Constraints of 4H-SiC Power MOSFETs Under Short Circuit Events. *IEEE Trans. Device Mater. Reliab.* **2023**, *23*, 544–563. [CrossRef]
24. Chen, X.; Chen, H.; Shi, B.; Wang, Y.; Li, X.; Zhou, C.; Li, C.; Deng, X.; Luo, H.; Wu, Y.; et al. Investigation on Short-Circuit Characterization and Optimization of 3.3-KV SiC MOSFETs. *IEEE Trans. Electron. Devices* **2021**, *68*, 184–191. [CrossRef]
25. Li, F.; Jennings, M. Main Differences in Processing Si and SiC Devices. In *Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications*; InTech: Rijeka, Croatia, 2018.
26. Cui, H.; Li, B.; Kong, H.; Yang, F.; Wang, F.; Wang, L.; Gao, K. Understanding the Thermal Characteristics of SiC Power MOSFET Device for Power Modules Design. In Proceedings of the PEDG 2023–2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems, Shanghai, China, 9–12 June 2023; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2023; pp. 1088–1095.
27. Xu, Y. Applications and Challenges of Silicon Carbide (SiC) MOSFET Technology in Electric Vehicle Propulsion Systems: A Review. *Appl. Comput. Eng.* **2024**, *40*, 180–186. [CrossRef]
28. Wileman, A.J.; Aslam, S.; Perinpanayagam, S. A Road Map for Reliable Power Electronics for More Electric Aircraft. *Prog. Aerosp. Sci.* **2021**, *127*, 100739. [CrossRef]
29. Shoji, T.; Kuwahara, M.; Usui, M. Dependence of Short-Circuit Withstand Capability of SiC MOSFETs on Short-Circuit Failure Time. *IEEE Trans. Power Electron.* **2021**, *36*, 11739–11747. [CrossRef]
30. Awwad, A.E.; Dieckerhoff, S. Short-Circuit Evaluation and Overcurrent Protection for SiC Power MOSFETs. In Proceedings of the 2015 17th European Conference on Power Electronics and Applications, Geneva, Switzerland, 8–10 September 2015.
31. Xue, J.; Xin, Z.; Wang, H.; Loh, P.C.; Blaabjerg, F. An Improved Di/Dt-RCD Detection for Short-Circuit Protection of SiC Mosfet. *IEEE Trans. Power Electron.* **2021**, *36*, 12–17. [CrossRef]

32. Barazi, Y.; Boige, F.; Rouger, N.C.; Blaquiere, J.-M.; Richardeau, F.; Rouger, N.; Richardeau, F. "ig,Vgs" Monitoring for Fast and Robust SiC MOSFET Short-Circuit Protection with High Integration Capability Monitoring for Fast and Robust SiC MOSFET Short-Circuit Protection with High Integration Capability "Ig,Vgs" Monitoring for Fast and Robust SiC MOSFET Short-Circuit Protection with High Integration Capability Acknowledgements. In Proceedings of the 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 7–11 September 2020; p. 10. [CrossRef]
33. Hofstetter, P.; Bakran, M.M. The Two-Dimensional Short-Circuit Detection Protection for SiC MOSFETs in Urban Rail Transit Application. *IEEE Trans. Power Electron.* **2020**, *35*, 5692–5701. [CrossRef]
34. Ouyang, W.; Sun, P.; Xie, M.; Luo, Q.; Du, X. A Fast Short-Circuit Protection Method for SiC MOSFET Based on Indirect Power Dissipation Level. *IEEE Trans. Power Electron.* **2022**, *37*, 8825–8829. [CrossRef]
35. Rafiq, A.; Pramanick, S. Ultrafast Protection of Discrete SiC MOSFETs with PCB Coil-Based Current Sensors. *IEEE Trans. Power Electron.* **2023**, *38*, 1860–1870. [CrossRef]
36. Zhang, J.; Wu, H.; Zhang, Y.; Zhao, J. Turn-off Modes of Silicon Carbide MOSFETs for Short-Circuit Fault Protection. *J. Power Electron.* **2021**, *21*, 475–482. [CrossRef]
37. Dhanasekaran, S.; Miryala, V.K.; Hatua, K. Adaptive Digital Technique Assisted Hard Switching Fault Detection for SiC MOSFETs. In Proceedings of the IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia, WiPDA Asia 2021, Wuhan, China, 25–27 August 2021; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2021; pp. 338–343.
38. Wang, Q.; Zhang, J.; Iannuzzo, F.; Jiang, Y.; Zhang, W.; He, F. Short-Circuit Fault Adaptive Analysis and Protection for SiC MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2023**, *11*, 4867–4881. [CrossRef]
39. Cui, M.; Li, J.; Du, Y.; Zhao, Z. Behavior of SiC MOSFET under Short-Circuit during the On-State. *IOP Conf. Ser. Mater. Sci. Eng.* **2018**, *439*, 022026. [CrossRef]
40. Liao, X.; Shen, Q.; Hu, Y.; Yang, C.; Chen, X.; Li, H. Fault Protection for a SiC MOSFET Based on Gate Voltage Subjected to Short Circuit Type II. *Microelectron. Reliab.* **2020**, *107*, 113624. [CrossRef]
41. Reigosa, D.; Fernandez, D.; Gonzalez, C.; Lee, S.B.; Briz, F. Permanent magnet synchronous machine drive control using analog hall-effect sensors. In Proceedings of the ECCE: 2017 IEEE Energy Conversion Congress and Exposition, Cincinnati, OH, USA, 1–5 October 2017; IEEE: Piscataway, NJ, USA, 2017. ISBN 9781509029983.
42. Liu, Y.; Peng, F.Z. A four-level modular multilevel converter with self voltage balancing and extremely small DC capacitor. In Proceedings of the APEC 2019: Thirty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 17–21 March 2019; IEEE: Piscataway, NJ, USA, 2019. ISBN 9781538683309.
43. Wang, Z.; Shi, X.; Tolbert, L.M.; Wang, F.; Liang, Z.; Costinett, D.; Blalock, B.J. Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs. *IEEE Trans. Power Electron.* **2016**, *31*, 1555–1566. [CrossRef]
44. Verband der Elektrotechnik Elektronik Informationstechnik; Institute of Electrical and Electronics Engineers. *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of: Date 19–20 May 2015*; IEEE: Piscataway, NJ, USA, 2015; ISBN 9783800739240.
45. Li, H.; Wang, J.; Ren, N.; Xu, H.; Sheng, K. Investigation of 1200 V SiC MOSFETs' Surge Reliability. *Micromachines* **2019**, *10*, 485. [CrossRef] [PubMed]
46. Liu, H.; Wei, J.; Wei, Z.; Liu, S.; Shi, L. Experimental Comparison of a New 1.2 KV 4H-SiC Split-Gate MOSFET with Conventional SiC MOSFETs in Terms of Reliability Robustness. *Electronics* **2023**, *12*, 2551. [CrossRef]
47. Xu, H.; Wang, B.; Ren, N.; Long, H.; Huang, K.; Sheng, K. Influence of JFET Width on Short-Circuit Robustness of 1200 V SiC Power MOSFETs. *Electronics* **2023**, *12*, 4849. [CrossRef]
48. Kanale, A.; Baliga, B.J. Theoretical Optimization of the Si GSS-DMM Device in the BaSIC Topology for SiC Power MOSFET Short-Circuit Capability Improvement. *IEEE Access* **2021**, *9*, 70039–70047. [CrossRef]
49. Uhnevionak, V.; Burenkov, A.; Strenger, C.; Ortiz, G.; Bedel-Pereira, E.; Mortet, V.; Cristiano, F.; Bauer, A.J.; Pichler, P. Comprehensive Study of the Electron Scattering Mechanisms in 4H-SiC MOSFETs. *IEEE Trans. Electron. Devices* **2015**, *62*, 2562–2570. [CrossRef]
50. Noborio, M.; Kanzaki, Y.; Suda, J.; Kimoto, T. Experimental and Theoretical Investigations on Short-Channel Effects in 4H-SiC MOSFETs. *IEEE Trans. Electron. Devices* **2005**, *52*, 1954–1962. [CrossRef]
51. Tachiki, K.; Ono, T.; Kobayashi, T.; Kimoto, T. Short-Channel Effects in SiC MOSFETs Based on Analyses of Saturation Drain Current. *IEEE Trans. Electron. Devices* **2021**, *68*, 1382–1384. [CrossRef]
52. Available online: https://assets.wolfspeed.com/uploads/2024/01/Wolfspeed_C2M0040120D_data_sheet.pdf (accessed on 7 August 2024).
53. Tsibizov, A.; Kovacˇevic-Badstübner, I.; Kakarla, B.; Grossner, U. Accurate Temperature Estimation of SiC Power Mosfets under Extreme Operating Conditions. *IEEE Trans. Power Electron.* **2019**, *35*, 1855–1865. [CrossRef]
54. Ding, X.; Peng, L.; Zhao, Y.; Yang, K.; Cui, H.; Shan, Z.; Yang, Y.; Lyu, G. Short-Circuit Characteristics of Asymmetry Trench (AT) MOSFET and Associative Failure Mechanisms over Wide Ambient Temperature. In Proceedings of the International Symposium on Power Semiconductor Devices and ICs, Bremen, Germany, 2–6 June 2024; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2024; pp. 216–219.
55. Kumar, A.; Moradpour, M.; Losito, M.; Franke, W.T.; Ramasamy, S.; Baccoli, R.; Gatto, G. Wide Band Gap Devices and Their Application in Power Electronics. *Energies* **2022**, *15*, 9172. [CrossRef]

56. Wang, Y.; Ding, Y.; Yin, Y. Reliability of Wide Band Gap Power Electronic Semiconductor and Packaging: A Review. *Energies* **2022**, *15*, 6670. [CrossRef]
57. Fiorenza, P.; Giannazzo, F.; Roccaforte, F. Characterization of SiO_2/4H-SiC Interfaces in 4H-SiC MOSFETs: A Review. *Energies* **2019**, *12*, 2310. [CrossRef]
58. Tan, J.; Zhou, Z. An Optimized Switching Strategy Based on Gate Drivers with Variable Voltage to Improve the Switching Performance of SiC MOSFET Modules. *Energies* **2023**, *16*, 5984. [CrossRef]
59. Prado, E.O.; Bolsi, P.C.; Sartori, H.C.; Pinheiro, J.R. An Overview about Si, Superjunction, SiC and GaN Power MOSFET Technologies in Power Electronics Applications. *Energies* **2022**, *15*, 5244. [CrossRef]
60. Cha, K.; Kim, K. Asymmetric Split-Gate 4H-SiC MOSFET with Embedded Schottky Barrier Diode for High-Frequency Applications. *Energies* **2021**, *14*, 7305. [CrossRef]
61. Barbagallo, C.; Agatino Rizzo, S.; Scelba, G.; Scarcella, G.; Cacciato, M. On the lifetime estimation of SiC power MOSFETs for motor drive applications. *Electronics* **2021**, *10*, 324. [CrossRef]
62. La Via, F.; Alquier, D.; Giannazzo, F.; Kimoto, T.; Neudeck, P.; Ou, H.; Roncaglia, A.; Saddow, S.E.; Tudisco, S. Emerging SiC Applications beyond Power Electronic Devices. *Micromachines* **2023**, *14*, 1200. [CrossRef]
63. Chen, J.; Du, X.; Luo, Q.; Zhang, X.; Sun, P.; Zhou, L. A Review of Switching Oscillations of Wide Bandgap Semiconductor Devices. *IEEE Trans. Power Electron.* **2020**, *35*, 13182–13199. [CrossRef]
64. Wang, J.; Chung, H.S.H.; Li, R.T.H. Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance. *IEEE Trans. Power Electron.* **2013**, *28*, 573–590. [CrossRef]
65. Zhou, B.; Han, D.; Peng, F.Z.; Dwari, S. Improved De-Saturation Protection Circuits for Silicon Carbide MOSFET Gate Drivers. In Proceedings of the 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 14–17 June 2021; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2021; pp. 2544–2548.
66. Verband der Elektrotechnik Elektronik Informationstechnik; Institute of Electrical and Electronics Engineers. *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management: 16–18 May 2017*; IEEE: Piscataway, NJ, USA, 2017; ISBN 9783800744244.
67. Mesago Messe Frankfurt GmbH; Institute of Electrical and Electronics Engineers. *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management: 5–7 June 2018*; IEEE: Piscataway, NJ, USA, 2018; ISBN 9783800746460.
68. Guo, Z.; Li, H. Dv/Dt Sensing-Based Short-Circuit Protection for Medium-Voltage SiC Mosfets. *IEEE Trans. Power Electron.* **2023**, *38*, 10554–10558. [CrossRef]
69. Li, H.; Wang, Y.; Qiu, Z.; Wang, Z.; Hu, X.; Zhao, J. Short-Circuit Protection Circuit of SiC MOSFET Based on Drain-Source Voltage Integral. In Proceedings of the IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia, WiPDA Asia 2021, Wuhan, China, 25–27 August 2021; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2021; pp. 344–349.
70. IEEE Power Electronics Society; IEEE Industry Applications Society; Institute of Electrical and Electronics Engineers. *ECCE 2016: IEEE Energy Conversion Congress & Expo: Proceedings: Milwaukee, WI, USA, 18–22 September 2016*; IEEE: Piscataway, NJ, USA, 2016; ISBN 9781509007370.
71. Xu, Y.; Bu, X.; Hao, Y.; Xiang, P.; Li, W.; Hao, R. A Novel Short-Circuit Protect Method for SiC MOSFET Module Based on Simplified Rogowski Coil Current Sensor. In Proceedings of the 2019 4th IEEE Workshop on the Electronic Grid (eGRID), Xiamen, China, 11–14 November 2019.
72. Lee, J.A.; Ann, S.; Sim, D.H.; Lee, B.K. Design Guideline and Practical Solution of PCB-Type Rogowski Current Sensor for SiC MOSFET Short-Circuit Protection Based on Frequency Analysis. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 19–23 March 2023; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2022; pp. 1352–1357.
73. Feng, Y.; Shao, S.; Du, J.; Chen, Q.; Zhang, J.; Wu, X. Short-Circuit and Over-Current Fault Detection for SiC MOSFET Modules Based on Tunnel Magnetoresistance with Predictive Capabilities. *IEEE Trans. Power Electron.* **2022**, *37*, 3719–3723. [CrossRef]
74. Du, H.; Bayarsaikhan, Y.; Omura, I. Short-Circuit Protection Scheme with Efficient Soft Turn-off for Power Modules. *Microelectron. Reliab.* **2023**, *150*, 115078. [CrossRef]
75. Tsukuda, M.; Koga, M.; Nakashima, K.; Omura, I. Micro PCB Rogowski Coil for Current Monitoring and Protection of High Voltage Power Modules. *Microelectron. Reliab.* **2016**, *64*, 479–483. [CrossRef]
76. Stecca, M.; Tiftikidis, P.; Soeiro, T.B.; Bauer, P. Gate Driver Design for 1.2 KV SiC Module with PCB Integrated Rogowski Coil Protection Circuit. In Proceedings of the 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 10–14 October 2021; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2021; pp. 5723–5728.
77. Sharifi, S.; Kamel, T.; Tricoli, P. Investigating the best topology for Traction Power Substations (TPSs) in a Medium Voltage DC (MVDC) railway electrification system. In Proceedings of the2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, 6–10 September 2021; IEEE: Piscataway, NJ, USA, 2021; ISBN 9789075815375.
78. Runninger, A.; Granger, M. Design and Testing of a Hard-Fault Protection Circuit for a 1 KV SiC MOSFET Inverter. In Proceedings of the 2023 IEEE Energy Conversion Congress and Exposition (ECCE 2023), Nashville, TN, USA, 29 October–2 November 2023; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2023; pp. 5716–5719.

79. Acuna, J.; Walter, J.; Kallfass, I. Very Fast Short Circuit Protection for Gallium-Nitride Power Transistors Based on Printed Circuit Board Integrated Current Sensor. In Proceedings of the 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, Latvia, 17–21 September 2018.
80. Karakaya, F.; Alemdar, O.S.; Keysan, O. Layout-Based Ultrafast Short-Circuit Protection Technique for Parallel-Connected GaN HEMTs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 6385–6395. [CrossRef]
81. Lee, S.; Kim, K.; Shim, M.; Nam, I. A Digital Signal Processing Based Detection Circuit for Short-Circuit Protection of SiC MOSFET. *IEEE Trans Power. Electron.* **2021**, *36*, 13379–13382. [CrossRef]
82. Sun, K.; Wang, J.; Burgos, R.; Boroyevich, D. Design, Analysis, and Discussion of Short Circuit and Overload Gate-Driver Dual-Protection Scheme for 1.2-KV, 400-A SiC MOSFET Modules. *IEEE Trans. Power Electron.* **2020**, *35*, 3054–3068. [CrossRef]
83. Suzuki, H.; Funaki, T. Fast Short-Circuit Protection under Current Imbalance Condition for Multi-Paralleled SiC-MOSFETs. *Electr. Eng. Jpn.* **2023**, *216*, 35–45. [CrossRef]
84. Li, Q.; Yang, Y.; Wen, Y.; Tian, X.; Li, Y.; Xiang, W. A Fast Overcurrent Protection IC for SiC MOSFET Based on Current Detection. *IEEE Trans. Power Electron.* **2024**, *39*, 4986–4990. [CrossRef]
85. Du, J.; Feng, Y.; Chen, Q.; Shao, S. Tunnel Magnetoresistance-Based Short-Circuit Protection for SiC MOSFET in HybridPACK™ Drive Package. In Proceedings of the IECON 2022–48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 17–20 October 2022; IEEE Computer Society: Piscataway, NJ, USA, 2022.
86. Ke, Z.; Wang, J.; Hu, B.; Song, X.; Peng, Z.; Dai, Y.; Shen, Z.J. An Ultrafast Universal Short-Circuit Protection Technique Based on Gate Current Detection for SiC MOSFET. *IEEE Trans. Power Electron.* **2024**, *39*, 11931–11936. [CrossRef]
87. Picot-Digoix, M.; Richardeau, F.; Blaquiere, J.M.; Vinnac, S.; Azzopardi, S.; Le, T.L. Quasi-Flying Gate Concept Used for Short-Circuit Detection on SiC Power MOSFETs Based on a Dual-Port Gate Driver. *IEEE Trans. Power Electron.* **2023**, *38*, 6934–6938. [CrossRef]
88. Verband der Elektrotechnik Elektronik Informationstechnik; Institute of Electrical and Electronics Engineers. *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*; IEEE: Piscataway, NJ, USA, 2019; ISBN 9783800749386.
89. Horiguchi, T.; Kinouchi, S.; Nakayama, Y.; Akagi, H. A Fast Short-Circuit Protection Method Using Gate Charge Characteristics of SiC MOSFETs. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015; IEEE: Piscataway, NJ, USA, 2015; pp. 4759–4764. [CrossRef]
90. Hu, B.; Ke, Z.; He, M.; Zhang, C.; Liu, Z.; Wang, J. A Gate Current Detection for Short-Circuit Protection of SiC MOSFET. In Proceedings of the 2023 IEEE 4th China International Youth Conference on Electrical Engineering (CIYCEE 2023), Chengdu, China, 8–10 December 2023; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2023.
91. Xing, D.; Lyu, X.; Liu, J.; Xie, C.; Agarwal, A.; Wang, J. 3300-V SiC MOSFET Short-Circuit Reliability and Protection. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Virtual, 14–17 June 2021; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2021; pp. 1262–1266.
92. Li, Z.; Wei, J.; Chen, H. An Augmented Short Circuit Detection Method for SiC MOSFETs. In Proceedings of the 11th International Conference on Power Electronics, Machines and Drives (PEMD 2022), Newcastle, UK, 21–23 June 2022.
93. Mesago Messe Frankfurt GmbH; Institute of Electrical and Electronics Engineers. *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management: Date, 10–12 May 2016*; IEEE: Piscataway, NJ, USA, 2016; ISBN 9783800741861.
94. Sadik, D.P.; Colmenares, J.; Tolstoy, G.; Peftitsis, D.; Bakowski, M.; Rabkowski, J.; Nee, H.P. Short-Circuit Protection Circuits for Silicon-Carbide Power Transistors. *IEEE Trans. Ind. Electron.* **2016**, *63*, 1995–2004. [CrossRef]
95. Lyu, X.; Li, H.; Abdullah, Y.; Wang, K.; Hu, B.; Yang, Z.; Liu, J.; Wang, J.; Liu, L.; Bala, S. A Reliable Ultrafast Short-Circuit Protection Method for E-Mode GaN HEMT. *IEEE Trans. Power Electron.* **2020**, *35*, 8926–8933. [CrossRef]
96. Ji, S.; Laitinen, M.; Huang, X.; Sun, J.; Giewont, W.; Wang, F.; Tolbert, L.M. Short-Circuit Characterization and Protection of 10-KV SiC Mosfet. *IEEE Trans. Power Electron.* **2019**, *34*, 1755–1764. [CrossRef]
97. IEEE Power Electronics Society; IEEE Microwave Theory and Techniques Society; Institute of Electrical and Electronics Engineers; Wireless Power Week. In Proceedings of the 2020 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (Wow): 15–19 November 2020, Seoul, Republic of Korea; IEEE: Piscataway, NJ, USA, 2020; ISBN 9781728137469.
98. Yin, S.; Wu, Y.; Liu, Y.; Pan, X. Comparative Design of Gate Drivers with Short-Circuit Protection Scheme for SiC MOSFET and Si IGBT. *Energies* **2019**, *12*, 4546. [CrossRef]
99. Liu, C.; Zhang, Z.; Liu, Y.; Si, Y.; Wang, M.; Lei, Q. A Comprehensive Short-Circuit Protection Scheme for Series-Connected SiC MOSFETs. *IEEE Open J. Power Electron.* **2022**, *3*, 115–130. [CrossRef]
100. IEEE Industry Applications Society; Institute of Electrical and Electronics Engineers. In Proceedings of the 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), Harbin, China, 11–14 August 2019; IEEE: Piscataway, NJ, USA, 2019; ISBN 9781728133980.
101. Qin, H.; Yang, Y.; Xie, S.; Peng, J.; Hu, H.; Bu, F. Analysis of Short-Circuit Characteristics and the Design of a Novel Protection Circuit for SiC MOSFETs. In Proceedings of the 2022 International Conference on Power Energy Systems and Applications (ICoPESA 2022), Virtual, 25–27 February 2022; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2022; pp. 60–67.

102. Liu, J.; Wang, H. A Robust Design Method of Desaturation Protection Circuit for Silicon Carbide Power MOSFETs. In Proceedings of the 2023 IEEE Energy Conversion Congress and Exposition (ECCE 2023), Nashville, TN, USA, 29 October–2 November 2023; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2023; pp. 5433–5440.
103. Liu, T.; Quan, Y.; Zhou, X.; Tian, Y.; Cheng, X.; Huang, X. A Short Circuit Protection Circuit for SiC MOSFET with Self-Adjustive Blanking Time. *IEICE Electron. Express* **2021**, *18*, 20210345. [CrossRef]
104. Yu, H.; Shi, L.; Bhattacharya, M.; Jin, M.; Qian, J.; Agarwal, A.K. SiC Trench MOSFET with Depletion-Mode PMOS for Enhanced Short-Circuit Capability and Switching Performance. *Electronics* **2023**, *12*, 4764. [CrossRef]
105. Xin, Z.; Li, H.; Liu, Q.; Loh, P.C. A Review of Megahertz Current Sensors for Megahertz Power Converters. *IEEE Trans. Power Electron.* **2022**, *37*, 6720–6738. [CrossRef]
106. Ziegler, S.; Woodward, R.C.; Iu, H.H.C.; Borle, L.J. Current Sensing Techniques: A Review. *IEEE Sens. J.* **2009**, *9*, 354–376. [CrossRef]
107. Patel, A.; Ferdowsi, M. Current Sensing for Automotive Electronics—A Survey. *IEEE Trans. Veh. Technol.* **2009**, *58*, 4108–4119. [CrossRef]
108. Crescentini, M.; Syeda, S.F.; Gibiino, G.P. Hall-Effect Current Sensors: Principles of Operation and Implementation Techniques. *IEEE Sens. J.* **2022**, *22*, 10137–10151. [CrossRef]
109. Ferreira, J.A.; Cronje, W.A.; Relihan, W.A. Integration of High Frequency Current Shunts in Power Electronic Circuits. *IEEE Trans. Power Electron.* **1995**, *10*, 32–37. [CrossRef]
110. IEEE Power Electronics Society; IEEE Industry Applications Society; Institute of Electrical and Electronics Engineers. *ECCE 2015: IEEE Energy Conversion Congress & Expo: Montreal, Canada, 20–24 September 2015*; IEEE: Piscataway, NJ, USA, 2015; ISBN 9781467371513.
111. Shim, M.; Lee, K.; Kim, J.; Kim, K. Multistep Soft Turn-Off Time Control to Suppress the Overvoltage of SiC MOSFETs in Short-Circuit State. *IEEE Access* **2022**, *10*, 46408–46417. [CrossRef]