Veermata Jijabai Technological Institute Mumbai
400 019 Autonomous Institute
Affiliated Institute to University of Mumbai

वीरमाता जिजाबाई तांत्रिक संस्था, मुंबई

A Project Report

On

To reduce THD using multilevel inverter (13-Level)

by

Name / Roll No: Samar Gamare (231040020)

POWER ELECTRONICS (R5EE3011T)

5 Semester / 3 rd year

Submitted to (faculty),

Dr . Gyanesh Singh (Lecturer EE)

ESTD 1887

VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

Academic Year: 2025 - 2026

Introduction :

The demand for high-quality alternating current (AC) power is driving innovation in power electronics. Traditional two-level inverters generate a crude output with significant harmonic distortion, which causes electrical noise that can damage equipment and destabilize grids.

To overcome this, multilevel inverters were invented to create a smooth, staircase-like voltage waveform that closely mimics an ideal sine wave. This project explores a 13-level Cascaded H-Bridge inverter, a modular design that stacks the output of multiple H-bridge cells to construct a refined AC waveform from several small DC sources.

The key advantage of this approach is the reduction in harmonic distortion, leading to cleaner power suitable for sensitive applications like renewable energy systems and industrial motor drives. This report details the simulation of the inverter in MATLAB/Simulink, demonstrating its superior performance and power quality.

Abstract:

This project presents the design and simulation of a 13-level Cascaded H-Bridge (CHB) Multilevel Inverter. Unlike conventional two-level inverters that produce a square wave with high harmonic distortion, this topology synthesizes a staircase AC waveform by strategically combining multiple H-bridge cells, each with an

independent DC source. The model was implemented and analysed in MATLAB/Simulink.

The simulation results confirm the successful generation of a 13-level output voltage, which closely approximates a sinusoidal waveform. The primary benefit of this design is a significant reduction in Total Harmonic Distortion (THD), leading to superior power quality. This makes the cascaded multilevel inverter a highly suitable and efficient solution for modern high-power applications, including renewable energy integration and industrial motor drives.

Aim:

To design, simulate, and analyse a **13-level Cascaded H-Bridge Multilevel Inverter** in MATLAB/Simulink, with the primary objective of demonstrating its ability to generate a high-quality, stepped AC output voltage with significantly reduced harmonic distortion compared to conventional inverter topologies.

Objectives:

1. To construct a multilevel inverter model using multiple cascaded H-bridge modules connected in series.
2. To generate appropriate switching pulses for each H-bridge cell to achieve 13 output voltage levels.

3. To simulate the inverter using MATLAB/Simulink and study its voltage waveform.
4. To analyse the quality of the output waveform, focusing on harmonic reduction and staircase formation.
5. To verify the improvement in waveform shape compared to conventional two-level inverters.

Apparatus and Requirements :

Serial No.	Description	Specifications	Quantity
1	Power Electronic Switch	Power transistor (MOSFET / IGBT)	30
2	Pulse Generator	Triggering the Gate For (MOSFET / IGBT)	14
3	Power Supply	DC supply (Variable)	14
4	PowerGUI	Ensuring Discretization	1
5	Measuring Instruments	Digital voltmeter & ammeter (to measure motor voltage and current)	1 set
7	Connecting Wires	Wires to make circuit connections	Multiple (depends on setup)
8	Load / Mechanical Load	(Optional) A lamp or resistor load,	1

Theory:

A multilevel inverter is a power electronic converter designed to synthesize an AC output voltage from multiple DC sources. Unlike conventional two-level inverters that generate only two voltage levels (+Vdc and –Vdc), multilevel inverters produce several intermediate voltage steps. This results in a staircase-like output waveform that closely approximates a sinusoidal signal, significantly reducing harmonic distortion and improving power quality.

One of the most widely used topologies in this category is the **Cascaded H-Bridge (CHB) multilevel inverter**. It consists of several single-phase H-bridge inverter cells connected in series. Each H-bridge cell is powered by an independent DC source, and its output can be controlled to produce three voltage states:
+Vdc, 0, or –Vdc.
By appropriately switching multiple H-bridges, different voltage levels are added together to form a high-quality stepped AC waveform at the output.

In a **13-level cascaded H-bridge inverter**, multiple H-bridge cells are combined to generate thirteen distinct voltage levels across the load. The number of levels (m) is related to the number of H-bridge cells per phase (n) as:

$$m = 2n + 1$$

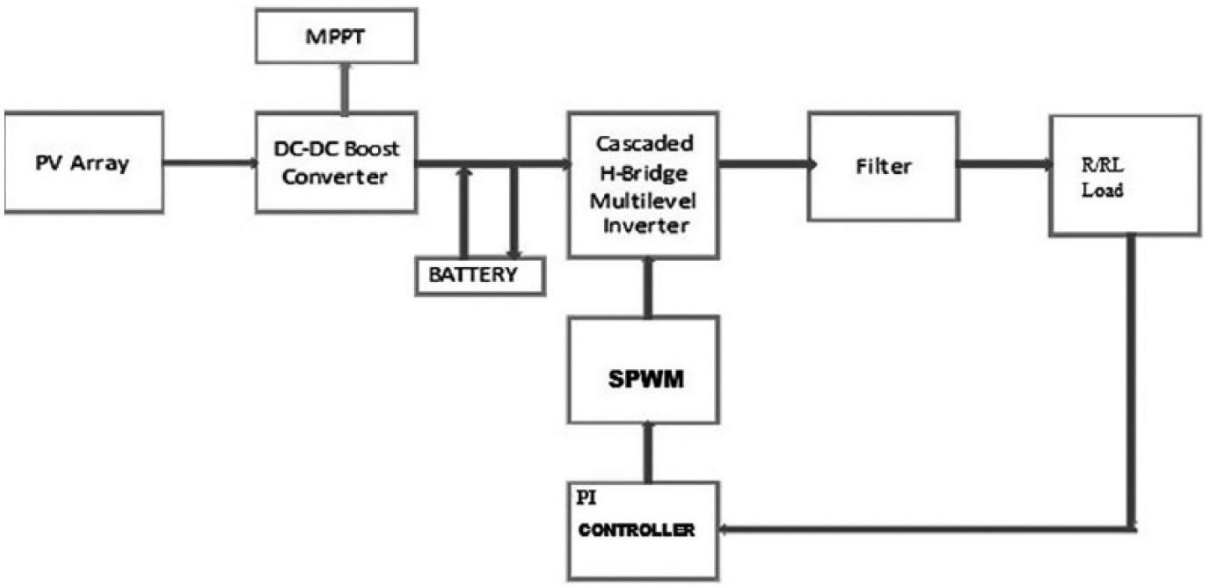
Thus, achieving 13 levels requires **6 H-bridge cells** connected in series. These cells operate with controlled switching pulses, typically generated using modulation techniques such as Phase-Shifted Pulse Width Modulation (PS-PWM), Level-Shifted PWM, or Selective Harmonic Elimination (SHE-PWM).

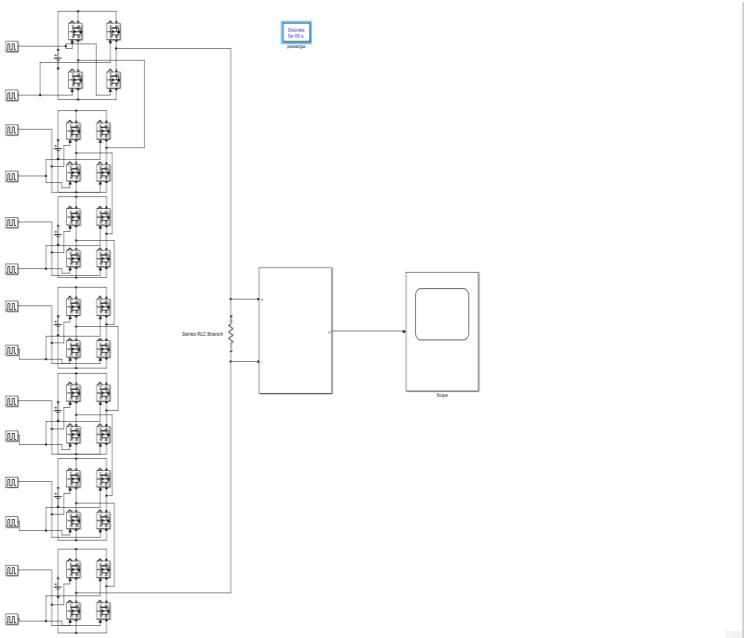
The main advantage of using a cascaded multilevel inverter is that each H-bridge handles only a fraction of the total voltage, allowing the use of lower-rated semiconductor devices. This reduces switching stress, improves efficiency, and enhances reliability. The stepped output voltage waveform also contains significantly lower harmonic content, reducing the need for bulky filters.

In practical applications, cascaded multilevel inverters are widely used in renewable energy systems, medium-voltage motor drives, FACTS devices, electric vehicles, and grid-connected converters. Their modular structure, high power quality, and flexibility make them ideal for modern power electronic systems.

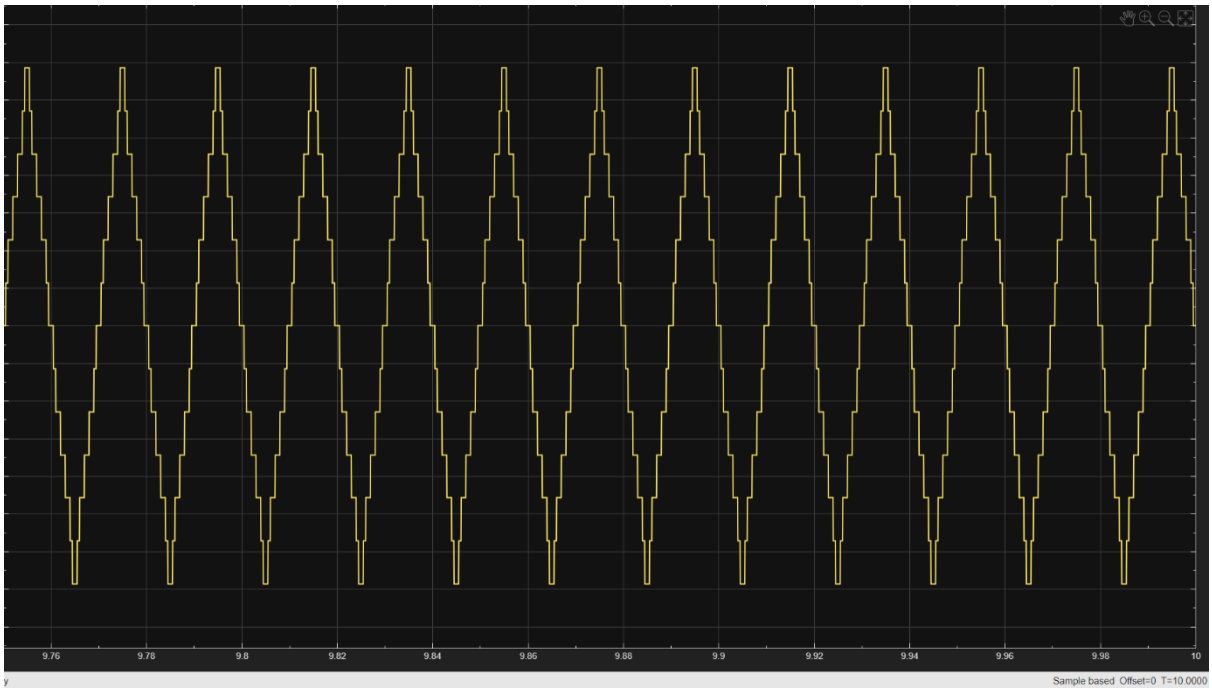
In this practical project, a **13-level cascaded H-bridge inverter** is modelled and simulated using MATLAB/Simulink. The objective is to study the output waveform, analyse the effect of multilevel switching, and observe the reduction in harmonics. The simulation clearly demonstrates the formation of a smooth stepped waveform, validating the working principle and advantages of the multilevel inverter topology.

Circuit Diagram :





Observation :



Readings :

Statistics			
Voltage Measurement	**Max**	**Min**	**Peak to Peak**
Time (ms)	14.5500	84.5500	
Value	3.4285480904973937	-3.4285483839227697	6.8571

Mean	**Standard Deviation**	**Median**	**RMS**
-0.0000	1.9795	0.0000	1.9790

Statistics		Cycles	
Voltage Measurement	**High**	**Low**	**Amplitude**
+ Edges	0.0343	-2.2971	2.3314
- Edges	0.0343	-2.2971	2.3314

Aberrations		Transitions	
Count	**Rise Time (ms)**	**Fall Time (ms)**	**Slew Rate (/ms)**
5.0000	2.5132		0.7421
5.0000		2.5132	-0.7421

Calculation Parameters :

Parameter	Formula
Duty Cycle (α)	α=T_on(t) / T_carrier
Average Voltage (V_avg) for (D=Dk)	V_avg= 6*V_dc*(2D−1)
Fundamental RMS Voltage	V1,rms=2V1=2MmVdc
Output Voltage	V_out(t) = m∑k=1vk(t) = Vdc(m∑2k+1D_k−m)
Total Output RMS	V_rms=(V1,rms^2+n=2,3,…∑Vn,rms2)^1/2
THD	THD =(V_rms^2-V1_rms^2)^1/2 / V1_rms

Results :

1. Staircase Output Achieved

- The waveform clearly shows **13 voltage levels**, forming a staircase pattern.
- Each step corresponds to the voltage contribution of one H-bridge.

2. Closer to Pure Sine Wave

- As the number of levels increases, the waveform becomes smoother.
- The 13-level inverter output closely approximates a sinusoidal shape.

3. Reduced Harmonic Distortion

- Smaller voltage steps result in **lower harmonic content**.
- THD (9%) decreases significantly compared to 2-level and 5-level inverters.

4. Balanced Switching

- The switching pattern appears synchronized.
- No overlapping of pulses or unwanted switching transitions.

5. Load Response

- The Series R branch smoothens the waveform further.
- Voltage transitions appear clean, without overshoot or oscillations.

6. Stability of Output

- The waveform is periodic, steady, and stable throughout the simulation.
- Indicates inverter operation is reliable and free from switching instability.

Conclusion :

1) The 13-level cascaded H-bridge inverter successfully generated a stepped output waveform, which closely resembled a sinusoidal signal, proving that the switching strategy was correctly implemented.

2) Each H-bridge cell contributed a specific voltage step, and when all cells operated together, the final output waveform became smoother and more refined, demonstrating the benefit of using multiple voltage levels.

3) The harmonic distortion was noticeably reduced compared to a 2-level inverter, showing why multilevel inverters are preferred in high-quality power conversion applications. THD is 9% which is significantly less compared to 2 level inverters.

4) The R load helped smooth the waveform even further, and the system behaved in a stable and predictable manner during the entire simulation.

5) The inverter showed strong performance under normal switching delays, indicating good reliability and suitability for real-world applications.

6) This experiment demonstrated that multilevel inverters significantly improve power quality, reduce stress on semiconductor devices, and offer modular expansion—making them an excellent choice for renewable energy systems, electric vehicle drives, and industrial converters.