Lab 6 - Building a Memory Hierarchy

Part 2 – Data cache

For this part 32 byte Data cache had been added. (i.e.containing 8 nos. of 4 byte blocks)

It allows us fast memory accessing when we use instructions like swd,swi,lwd,lwi by making the common case fast .Comparing with the part 1 which always used direct memory accessing)

Since every time these memory accessing instructions called CPU has to be stalled for 5 clock cycles which is inefficient. But using the cache in the best case

we can execute those instructions without stalling the CPU

Write hit ---> update only the cache (let it be inconsistent with memory)

Read -miss -->if old block is "dirty" old data should be read from memory before fetching that new block and Old-block should be written into memory - takes 41 CPU clock cycle

Write-miss --> write-back the old block to memory only if it's dirty , fetch new block and update the cache(only) – takes 41 CPU clock cycle
if it's not dirty , takes 21 CPU clock cycle

More efficient specially when rate of write accesses are high and it Reduces write traffic

When we call the same data then it will not stall the CPU

Instruction set used

00001001 00000000 00000000 00000000 //loadi 0 0x9

00000001 00000000 00000001 00000000 //loadi 1 0x1

00000001 00000000 00000000 00001010 //swd 0 1

00000000 00000001 00000000 00001011 //swi 1 0x00

00000001 00000000 00000010 00001000 //lwd 2 1

00000001 00000000 00000011 00001000 //lwd 3 1

00000001 00000000 00000100 00000011 //sub 4 0 1

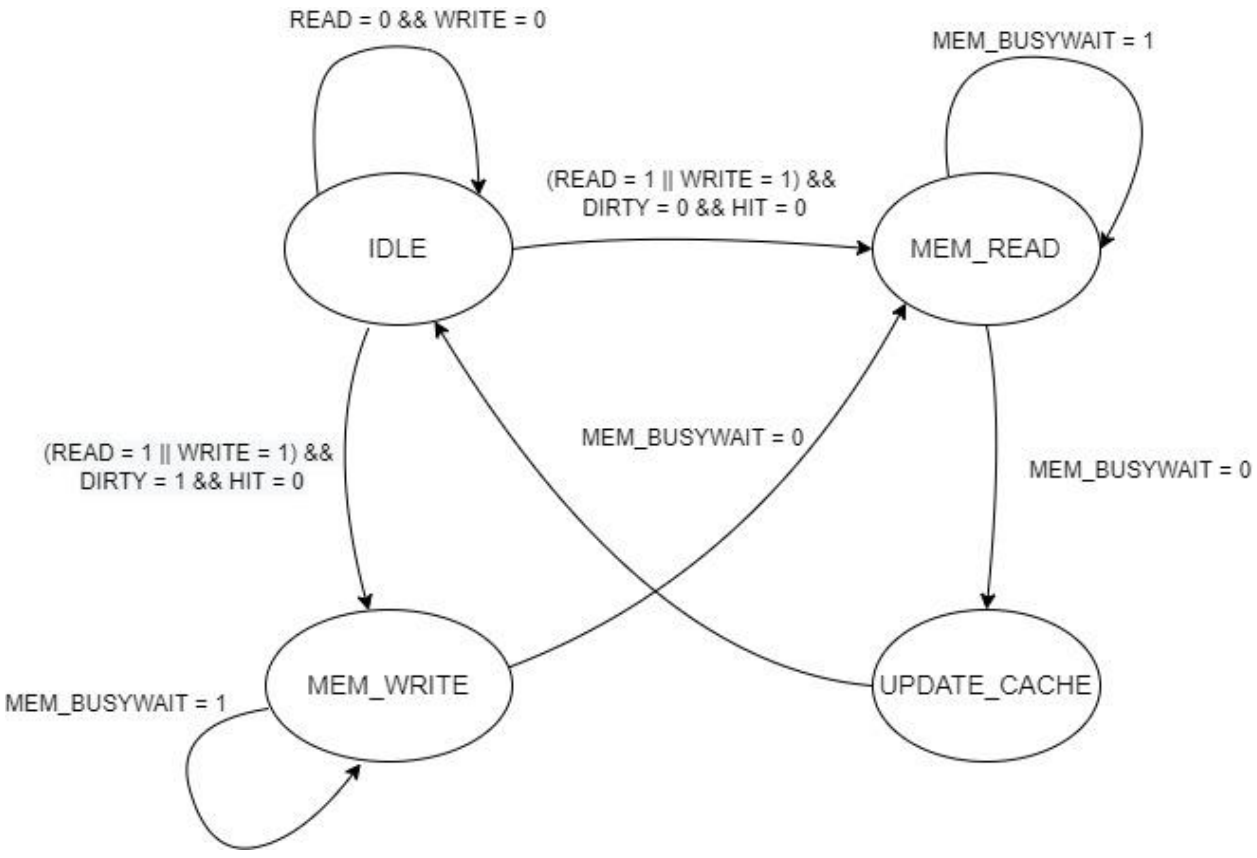
00000111 00000100 00000000 00001011 //swi 4 0x07

00000111 00000000 00000101 00001001 //lwi 5 0x07

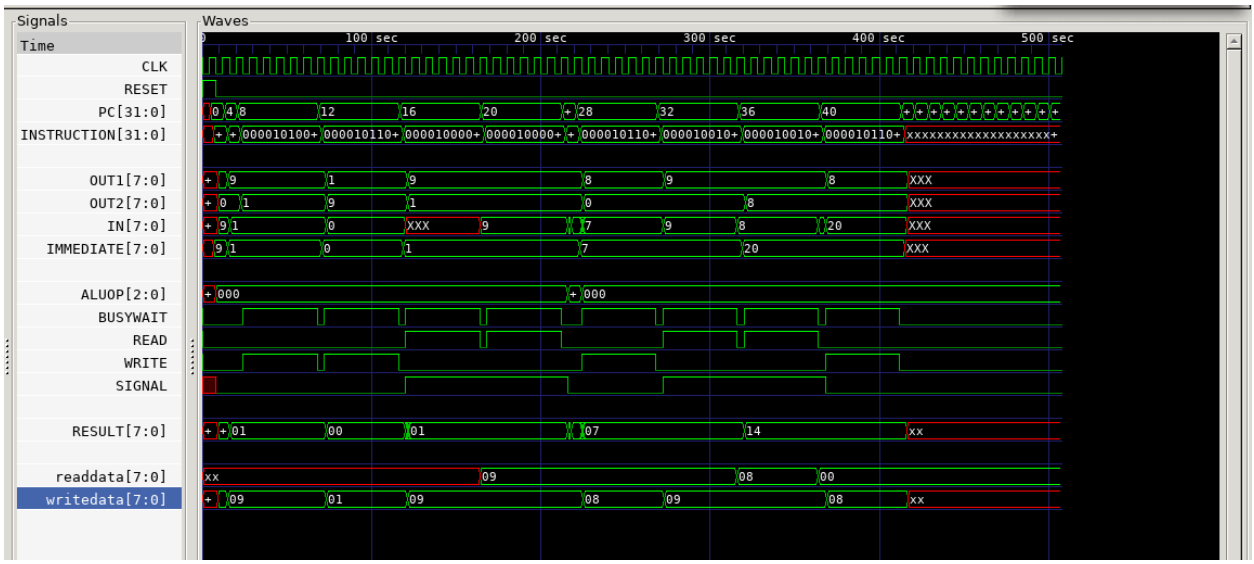
00010100 00000000 00000110 00001001 //lwi 6 0x20

00010100 00000100 00000000 00001011 //swi 4 0x20

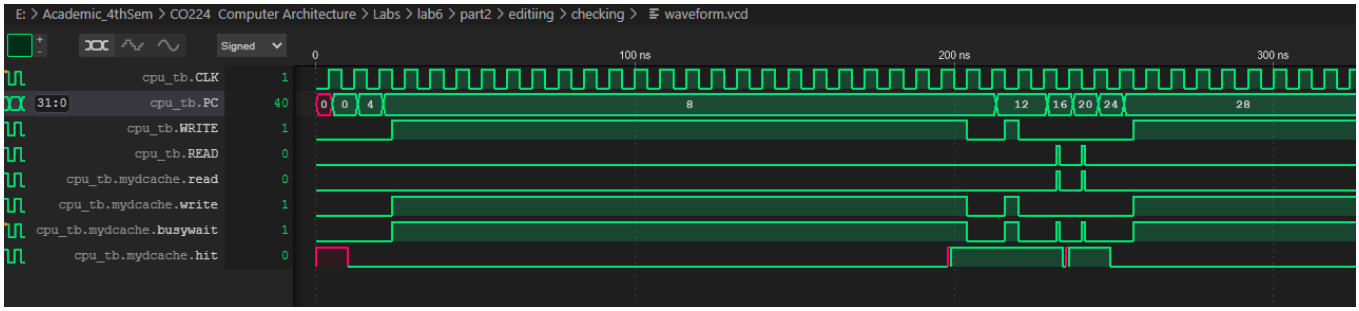
State diagram



Timing diagram of cpu without the cache



Timing diagram of the cpu with cache



Comparisons

- We can see more time is taken by the cpu with the cache than the cpu without the cache.This happens because in a miss it takes 21 clock cycles to get the data back to the cache.And 42 clock cycles to get the data back to cache if the dirty bit is 1 while it is a miss.
- But when a hit occurs, it takes less time to get the data to the cpu decreasing the average memory access time.
- And in part 1 we have accessed words but in part 2 we have accessed blocks therefore it reduces the memory access time as a whole set of data is fetched at a time.