Hardware Assignment 1 Report

Our goal was to design and implement a circuit that takes a 4-digit decimal/hexadecimal number from switches in the Basys3 board and displays it on the 4-seven segment displays on the board. We had to use an on-board clock and create a timing circuit to drive all the displays.

We started by creating a 'led_to_bcd.vhd' file which converts a 4-bit binary input(using any 4 switches) to a hexadecimal number (on the seven segment display). Since initially all the anode switches are on, the same number is displayed on all the 4-seven segment displays. Truth table for 4 bit input signal and seven bit cathode output is :
(A,B,C,D are bits of the input digit, and a to g is the cathode output.)

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	0	0	1	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

Below are the karnaugh maps used for the simplification of signals.

K-MAP FOR a :

SIMPLIFIED EXPRESSION : A’B’C’D+A’BC’D’+AB’CD+ABC’D

	$\overline{C}.\overline{D}$	$\overline{C}.D$	C.D	C.$\overline{D}$
$\overline{A}.\overline{B}$	0	1	0	0
$\overline{A}$.B	1	0	0	0
A.B	0	1	0	0
A.$\overline{B}$	0	0	1	0

K-MAP FOR b :

SIMPLIFIED EXPRESSION : BCD’+ACD+ABD’+A’BC’D

	$\overline{C}.\overline{D}$	$\overline{C}.D$	C.D	C.$\overline{D}$
$\overline{A}.\overline{B}$	0	0	0	0
$\overline{A}$.B	0	1	0	1
A.B	1	0	1	1
A.$\overline{B}$	0	0	1	0

K-MAP FOR c :

SIMPLIFIED EXPRESSION : ABD' + ABC + A'B'CD'

	$\overline{C}.\overline{D}$	$\overline{C}.D$	C.D	C.$\overline{D}$
$\overline{A}.\overline{B}$	0	0	0	1
$\overline{A}$.B	0	0	0	0
A.B	1	0	1	1
A.$\overline{B}$	0	0	0	0

K-MAP FOR d :

SIMPLIFIED EXPRESSION : BCD + A'B'C'D + A'BC'D'

	$\overline{C}.\overline{D}$	$\overline{C}.D$	C.D	C.$\overline{D}$
$\overline{A}.\overline{B}$	0	1	0	0
$\overline{A}$.B	1	0	1	0
A.B	0	0	1	0
A.$\overline{B}$	0	0	0	0

K-MAP FOR e :

SIMPLIFIED EXPRESSION : A'D + B'C'D + A'BC'

	$\overline{C}.\overline{D}$	$\overline{C}.D$	C.D	C.$\overline{D}$
$\overline{A}.\overline{B}$	0	1	1	0
$\overline{A}$.B	1	1	1	0
A.B	0	0	0	0
A.$\overline{B}$	0	1	0	0

K-MAP FOR f :

SIMPLIFIED EXPRESSION : A'B'D + B'CD' + A'CD + ABC'D

	$\overline{C}.\overline{D}$	$\overline{C}.D$	C.D	C.$\overline{D}$
$\overline{A}.\overline{B}$	0	1	1	1
$\overline{A}$.B	0	0	1	0
A.B	0	1	0	0
A.$\overline{B}$	0	0	0	1

K-MAP FOR g:

SIMPLIFIED EXPRESSION : A'B'D + B'CD' + A'CD + ABC'D

	$\overline{C}.\overline{D}$	$\overline{C}.D$	C.D	C.$\overline{D}$
$\overline{A}.\overline{B}$	1	1	0	0
$\overline{A}$.B	0	0	1	0
A.B	1	0	0	0
A.$\overline{B}$	0	0	0	0

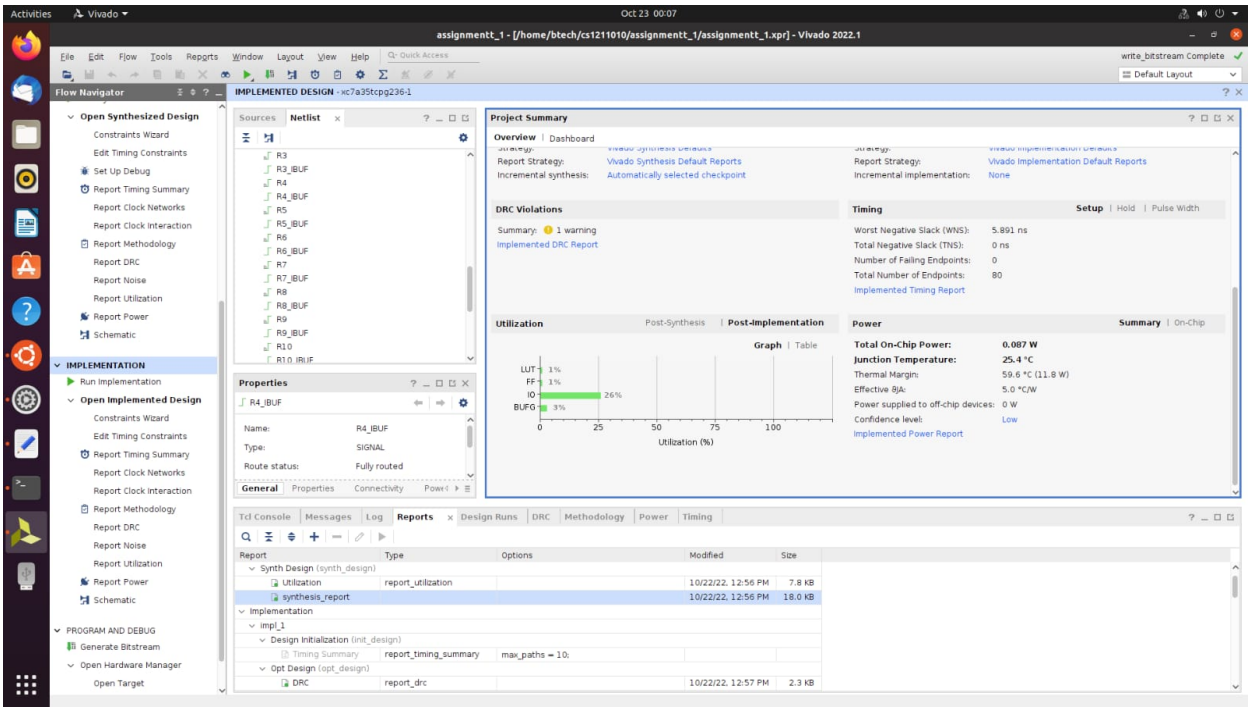
Then we created a file ‘mux_gate.vhd’ which uses all 16 switches on the basys board. We give 4-four bit binary inputs using the switches and use a multiplexer circuit on them. On the Basys3 board only one display can be activated at a given time. So, to display a separate digit on each LED display, the corresponding anode signal must be activated in a cyclic manner, and to avoid flickering, the refresh rate should vary between 1kHz - 60Hz (1-16 ms).

Another file ‘tim_ckt.vhd’ creates a timing circuit which helps to drive the different led displays. Frequency of the clock made was 1kHz. We defined two variables as counters, namely, ‘*clk_inpt*’ which is an integer that counts the number of cycles(frequency), and ‘*refresh*’ which is a 20-bit binary number whose last two bits are assigned to a variable called anode_activate which is used for activating the respective anodes.

We combined the utilities (behavioural) of all the above 3 files in a single file ‘display.vhd’ to get the desired circuit as per the specifications.

Utilisation reports

Graph form



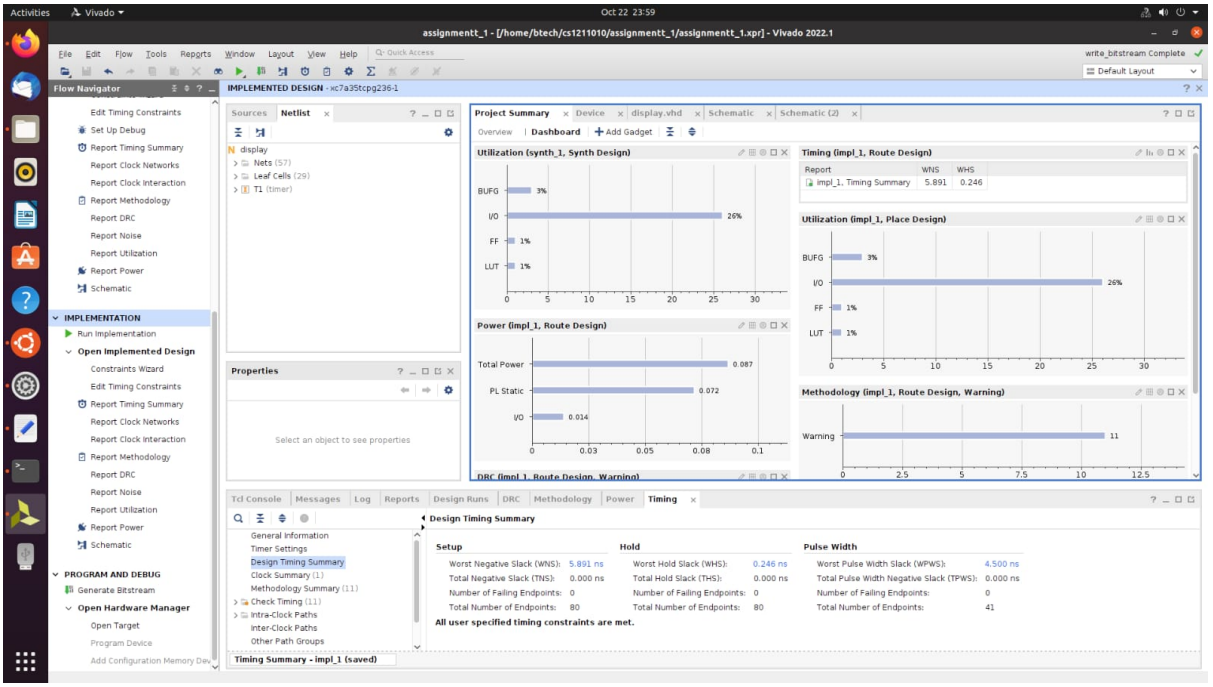
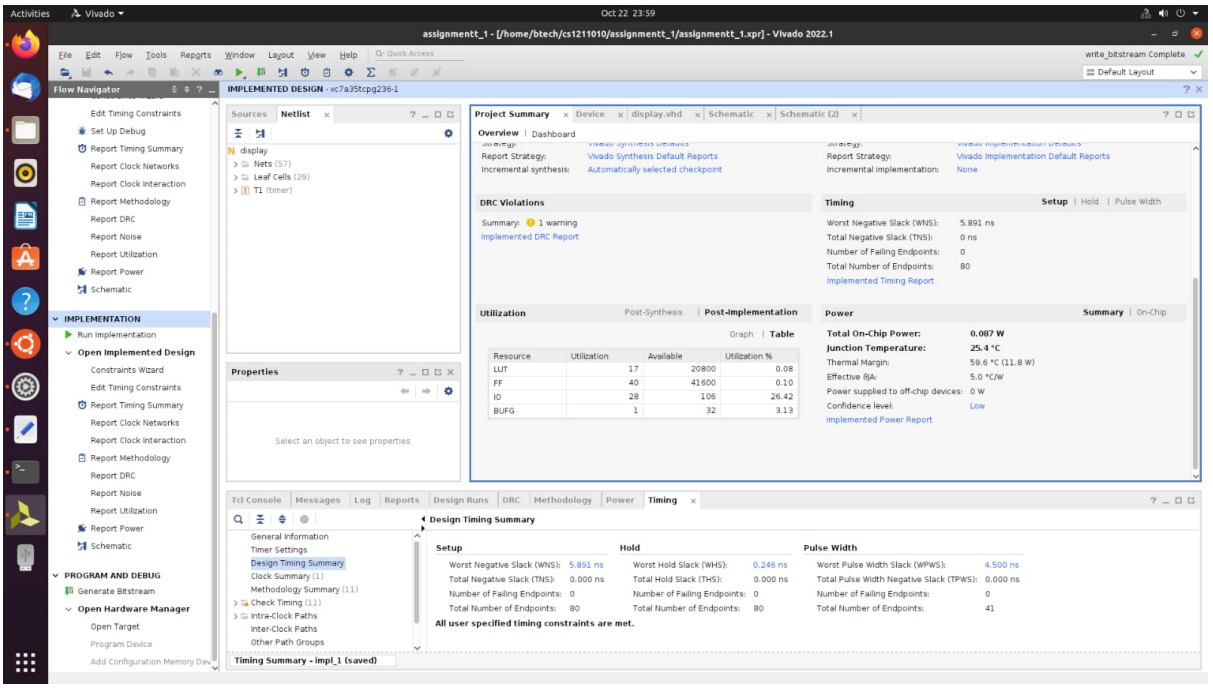

Activities
Vivado
Oct 22 23:59
assignmentt_1 - [/home/btech/cs1211010/assignmentt_1/assignmentt_1.xpr] - Vivado 2022.1
File Edit Flow Tools Reports Window Layout View Help
write_bitstream Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Sources Netlist
display
Nets (57)
Leaf Cells (29)
T1 (timer)
Properties
Select an object to see properties
Project Summary Device display.vhd Schematic Schematic (2)
Overview Dashboard Add Gadget
Utilization (synth_1, Synth Design)
BUFG 3%
I/O 26%
FF 1%
LUT 1%
Timing (impl_1, Route Design)
Report WNS WHS
impl_1, Timing Summary 5.891 0.246
Utilization (impl_1, Place Design)
Power (impl_1, Route Design)
Total Power 0.087
PL Static 0.072
I/O 0.014
Methodology (impl_1, Route Design, Warning)
Warning 11
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Methodology Summary (11)
Check Timing (11)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Setup
Worst Negative Slack (WNS): 5.891 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 80
Hold
Worst Hold Slack (WHS): 0.246 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 80
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 41
All user specified timing constraints are met.
Timing Summary - impl_1 (saved)
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Dev
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic

table form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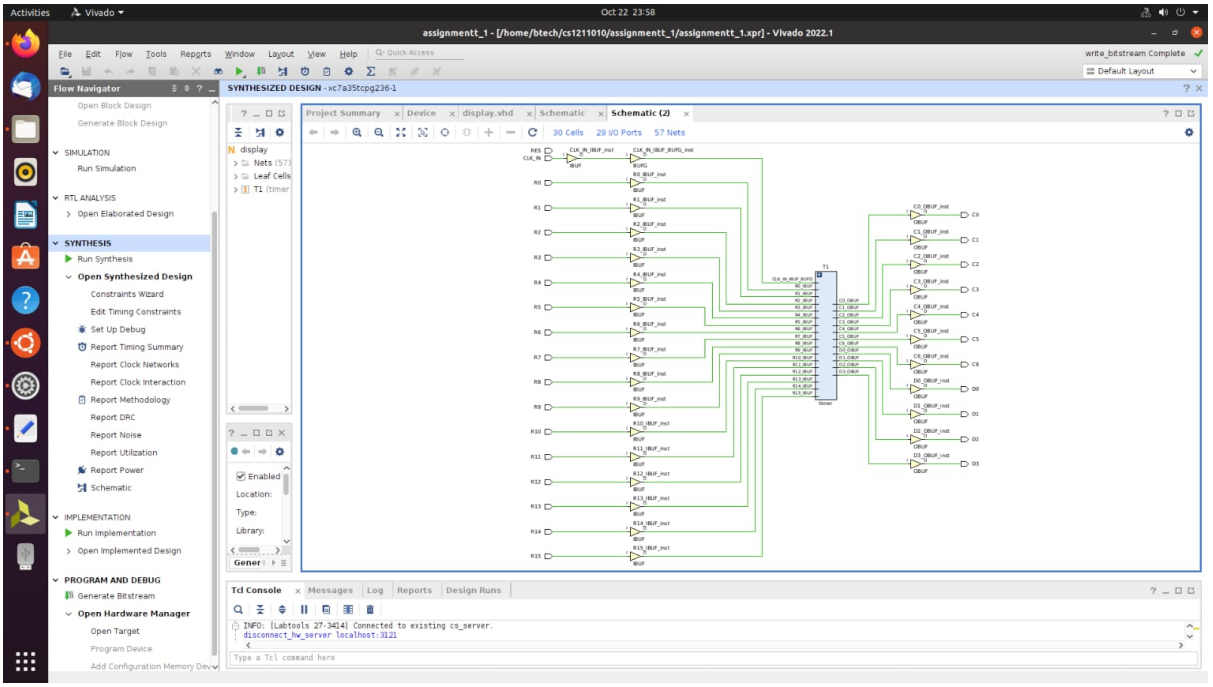
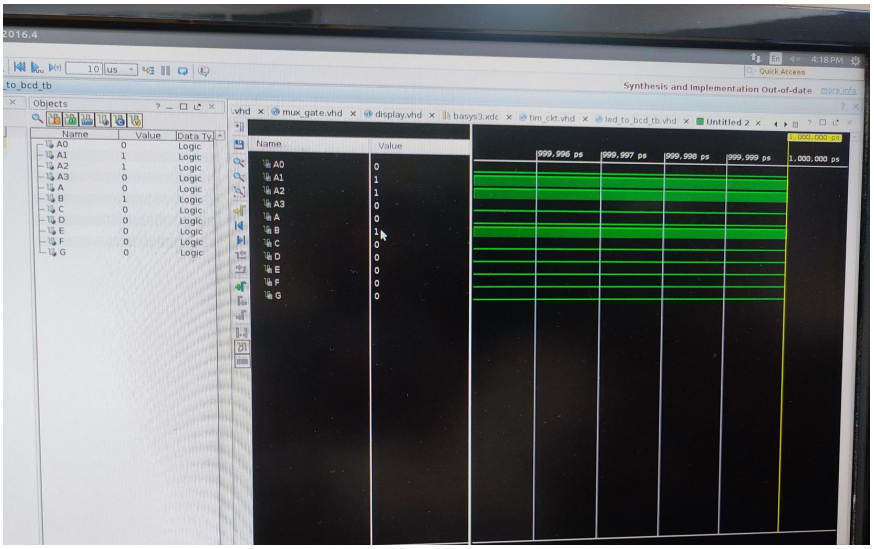
assignmentt_1 - [/home/btech/cs1211010/assignmentt_1/assignmentt_1.xpr] - Vivado 2022.1
File Edit Flow Tools Reports Window Layout View Help
write_bitstream Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Sources Netlist
display
Nets (57)
Leaf Cells (29)
T1 (timer)
Properties
Select an object to see properties
Project Summary Device display.vhd Schematic Schematic (2)
Overview Dashboard
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: Automatically selected checkpoint
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup Hold Pulse Width
Worst Negative Slack (WNS): 5.891 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 80
Implemented Timing Report
Utilization
Post-Synthesis Post-Implementation
Graph Table
Resource Utilization Available Utilization %
LUT 17 20800 0.08
FF 40 41600 0.10
IO 28 106 26.42
BUFG 1 32 3.13
Power
Summary On-Chip
Total On-Chip Power: 0.087 W
Junction Temperature: 25.4 °C
Thermal Margin: 59.6 °C (11.8 W)
Effective θJA: 5.0 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Methodology Summary (11)
Check Timing (11)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Setup
Worst Negative Slack (WNS): 5.891 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 80
Hold
Worst Hold Slack (WHS): 0.246 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 80
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 41
All user specified timing constraints are met.
Timing Summary - impl_1 (saved)
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Dev
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic

Synthesised design

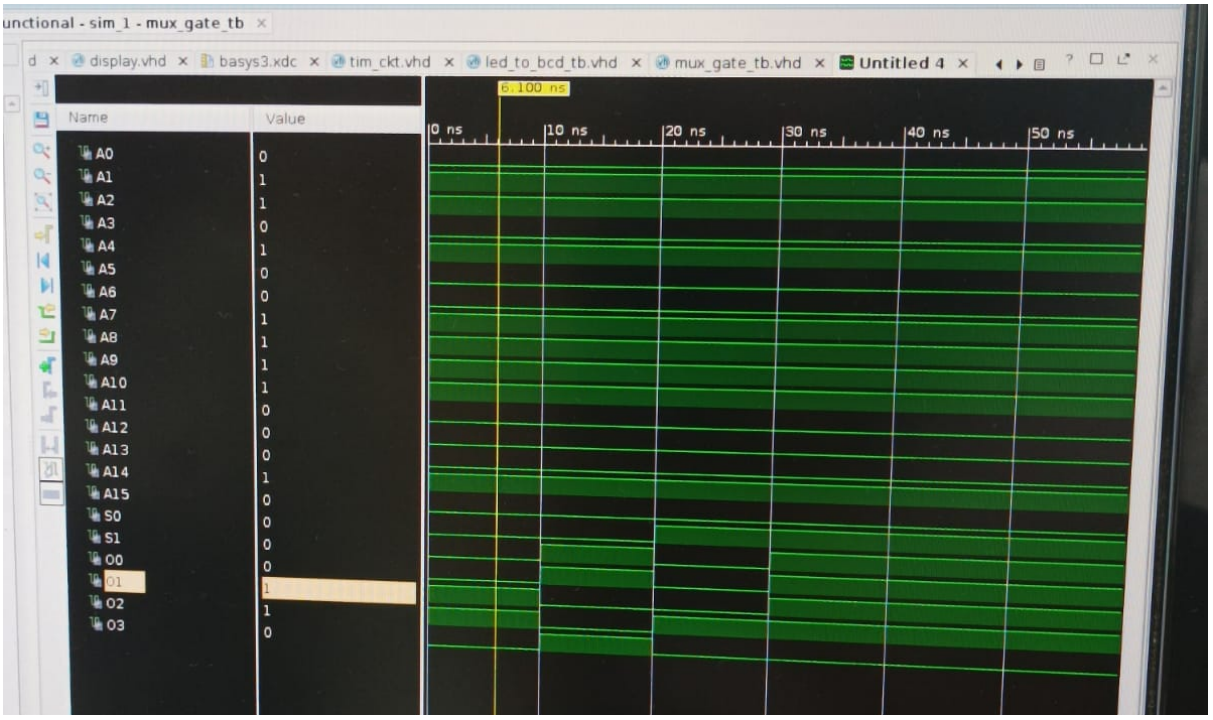


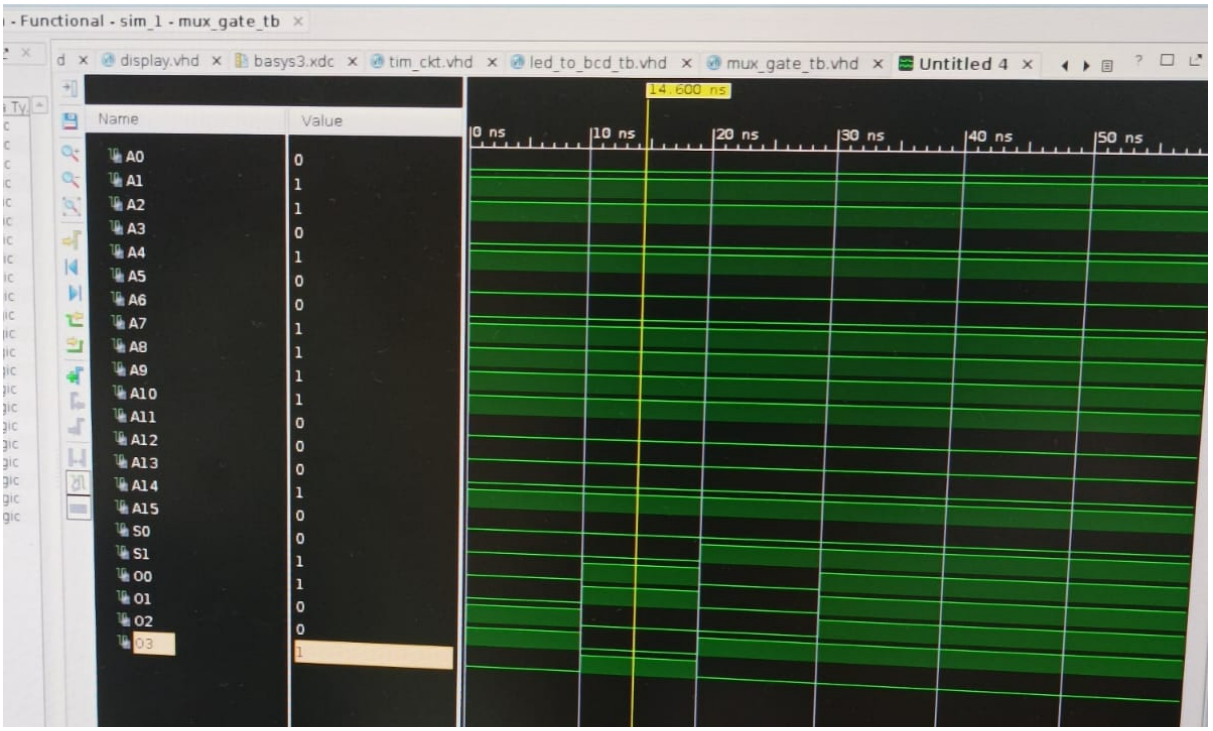
SYNTHESIS SNAPSHOTS

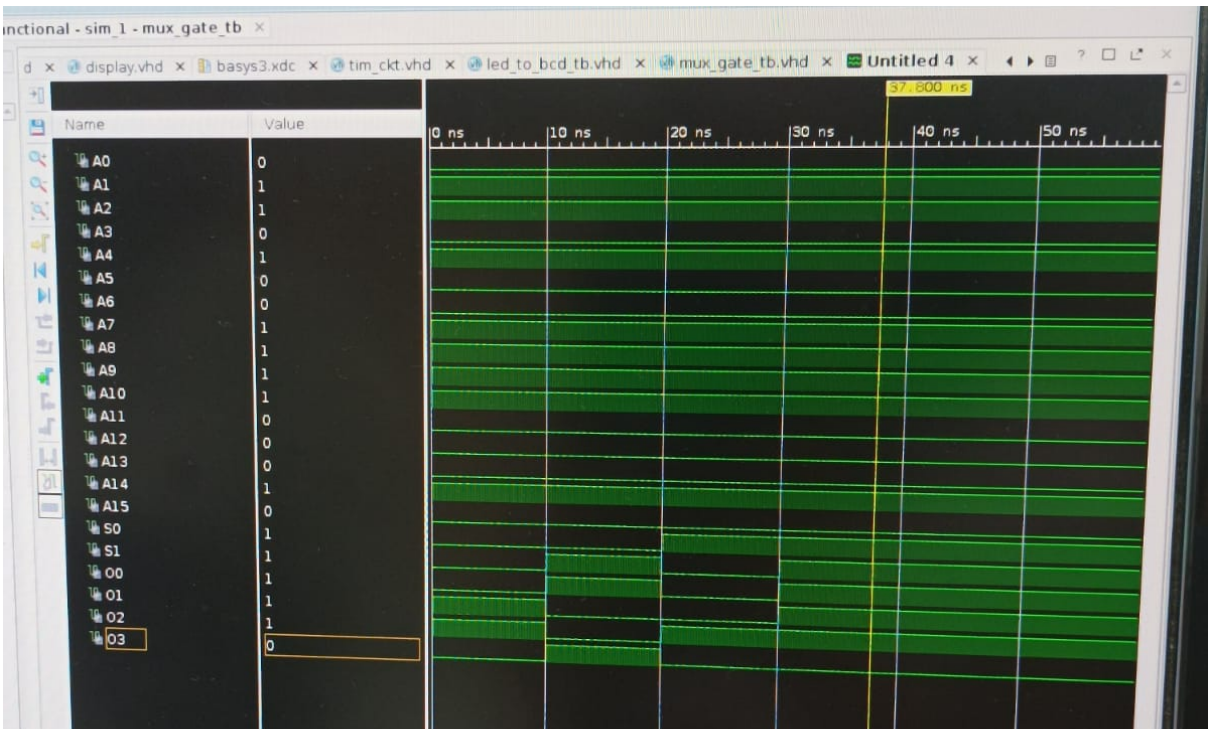
1)LED_TO_BCD(decoder synthesis)

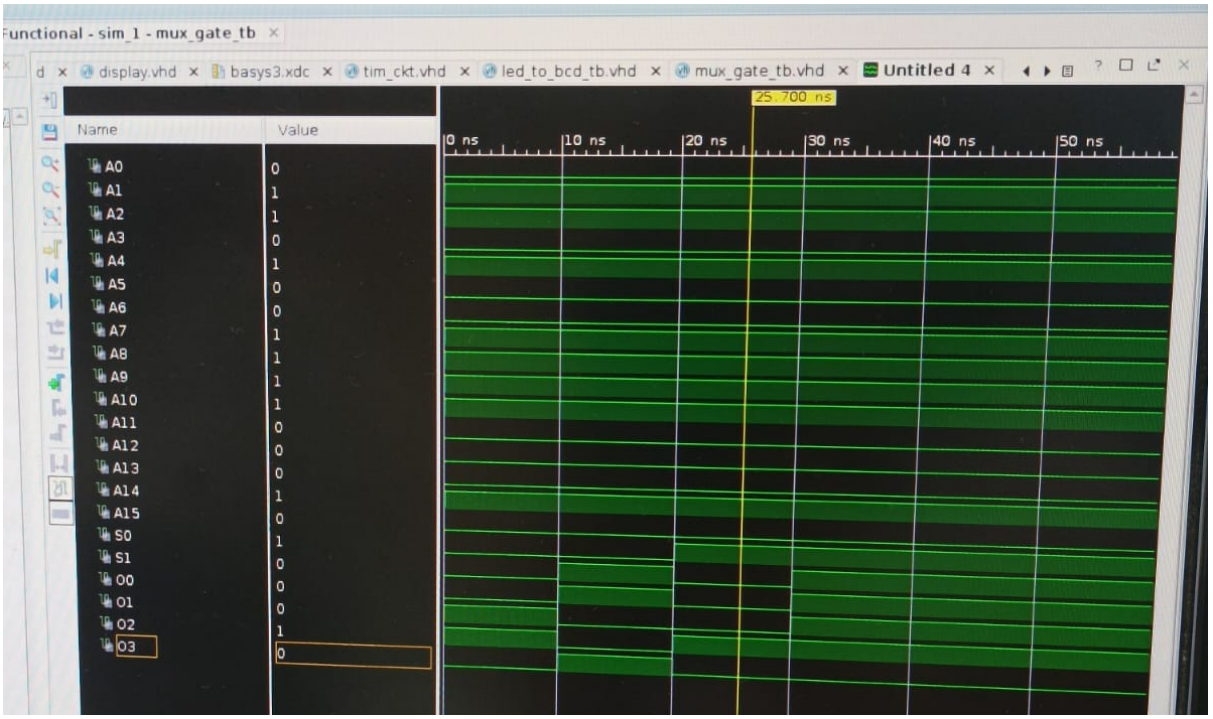


2)MUX GATE SYNTHESIS

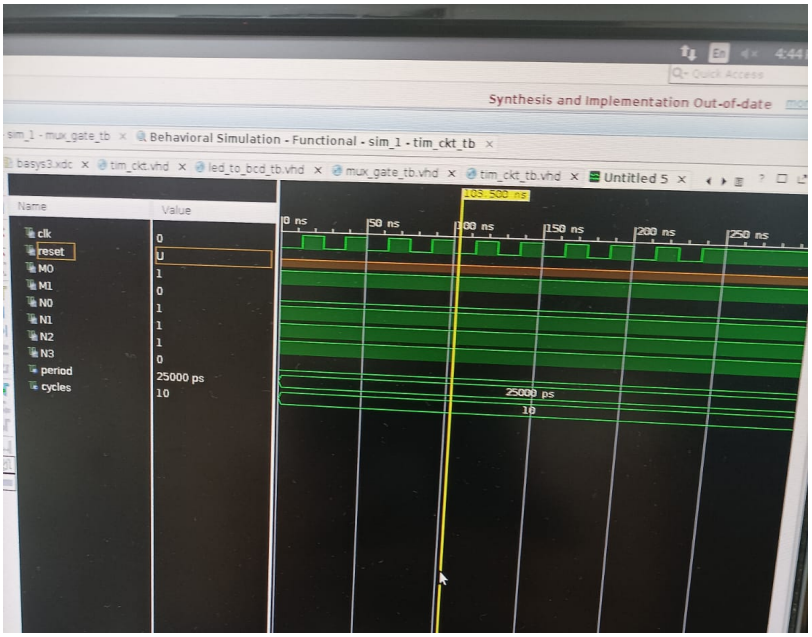




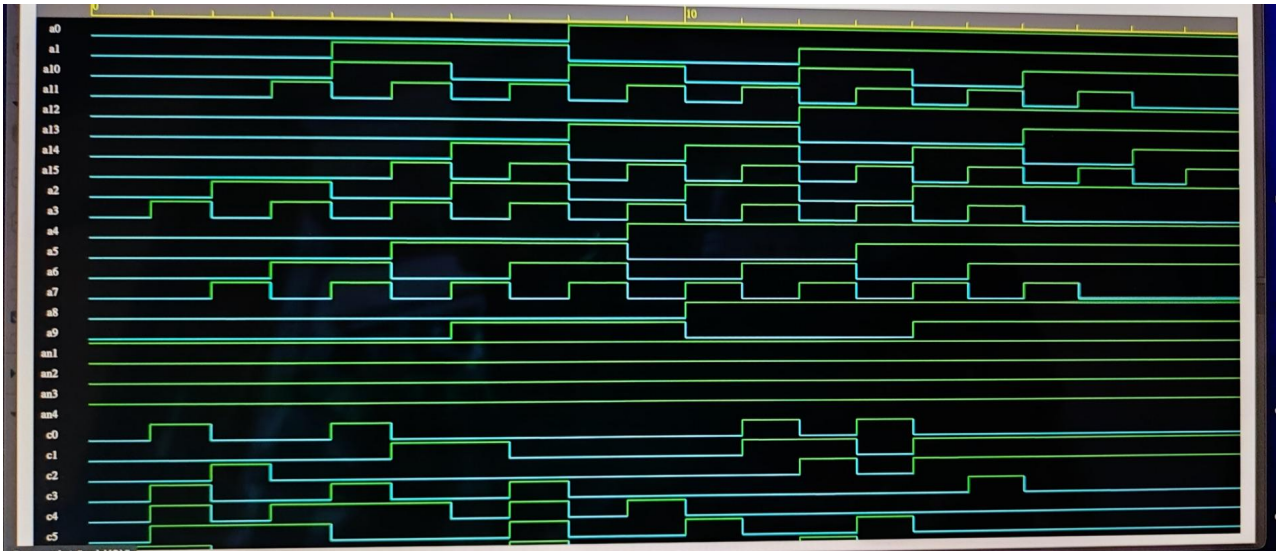

nctional - sim_1 - mux_gate_tb
display.vhd
basys3.xdc
tim_ckt.vhd
led_to_bcd_tb.vhd
mux_gate_tb.vhd
Untitled 4
37.800 ns
Name
Value
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
A0 0
A1 1
A2 1
A3 0
A4 1
A5 0
A6 0
A7 1
A8 1
A9 1
A10 1
A11 0
A12 0
A13 0
A14 1
A15 0
S0 1
S1 1
O0 1
O1 1
O2 1
O3 0


Functional - sim_1 - mux_gate_tb
display.vhd
basys3.xdc
tim_ckt.vhd
led_to_bcd_tb.vhd
mux_gate_tb.vhd
Untitled 4
25.700 ns
Name
Value
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
A0 0
A1 1
A2 1
A3 0
A4 1
A5 0
A6 0
A7 1
A8 1
A9 1
A10 1
A11 0
A12 0
A13 0
A14 1
A15 0
S0 1
S1 0
O0 0
O1 0
O2 1
O3 0

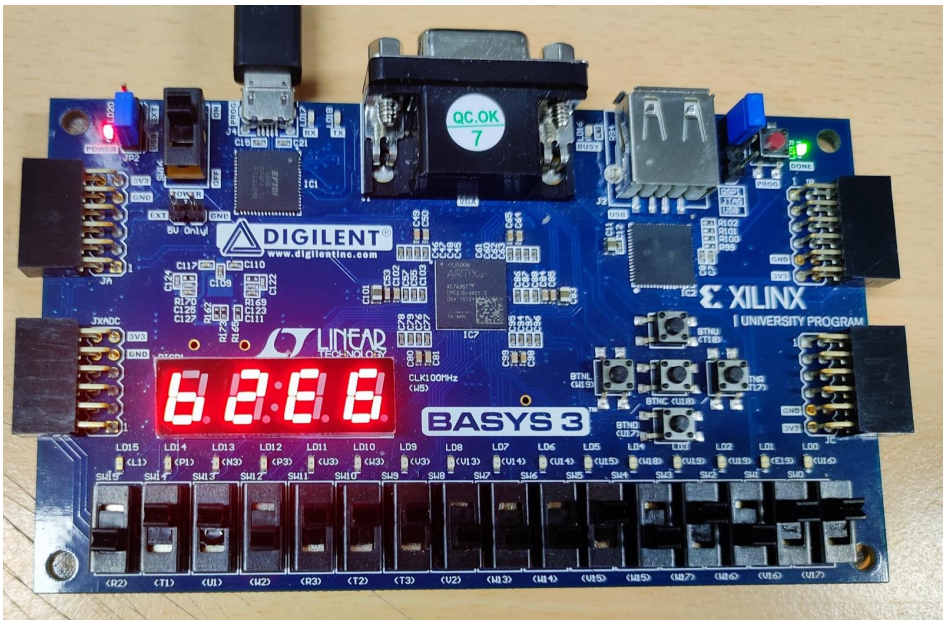
3)TIMER CIRCUIT SYNTHESIS



4) DESIGN (FINAL CIRCUIT)



Working code on hardware(input on switch 0110 1110 0010 1011)



By :
Kanishka Gajbhiye
Entry no:2021CS50131
Piyush Chauhan
Entry no: 2021CS11010