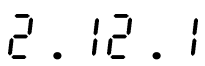
COL215 - Hardware Assignment 2

Stopwatch

Submission Deadline: 30 October 2022

1 Introduction

In this assignment, you will construct a stopwatch using the 7-segment displays and switches on the Basys 3 board.



2 Problem Description

Display format of the clock will be (M:SS:T): minutes (M) on one LED display, seconds (SS) on two LED displays and tenth of second (T) on one LED display. Refer to the format above. The task is to design and implement the following modules:

1. Use the 4-digit seven segment display created in the last assignment as a component (modify incrementally if required)
2. Create a stopwatch and display it on the board

2.1 stopwatch

Based on the display format for the stopwatch, you need a counter that keeps counting at every tenth of a second (10Hz) and then use logic to display the counter value in the above format of a stopwatch (i.e. display minutes, tens of seconds, unit of seconds and tenths of seconds).

The output from these counters will drive the 7-segment display module designed in the last assignment.

The inputs taken will be *enable_watch* (for starting the counting of time) and *reset_watch* (reset watch to 0:00.0).

You need to design a circuit to divide clock 100 Mhz to 10 Hz, this can be done using another modulo N counter where N = 10^7.

In addition to this, the watch will be controlled via four switches on the board:

- start: When start switch moves from $0 \rightarrow 1$, then *enable_watch* should be set to HIGH.
- pause: When pause switch moves from $0 \rightarrow 1$, then *enable_watch* is set to LOW.
- continue: When continue switch moves from $0 \rightarrow 1$, then *enable_watch* should be set to HIGH again. Note, continue state should only come after pause.
- reset: On reset from $0 \rightarrow 1$, *reset_watch* should be set to HIGH and the stopwatch counter should be reset to 0:00:0.

Please note that the switch inputs need to create a positive edge for changing the stopwatch inputs.

3 Submission and Demo Instructions

1. Demo should be given in the assigned lab slot.
2. You are required to submit zip file containing the following on Gradescope:
   - VHDL files for all the designed modules.
   - A short report (1-2 pages) explaining your approach. Include block diagram depicting the modules in the stopwatch. Include simulation waveforms and synthesis report.

3. Form groups of 2 students for the assignment.
    - Groups will remain the same for subsequent assignments; no changes allowed.
    - Only one submission is needed per group via Gradescope. Gradescope help link: `https://help.gradescope.com/article/m5qz2xsnjy-student-add-group-members`
4. Post your doubts in Assignment 2 thread on Piazza.
5. It is advisable that you should be ready with your design before the lab session, and during the session, perform validation of the design by downloading it into the FPGA board

4 Resources references

- IEEE document: `https://ieeexplore.ieee.org/document/8938196`
- Basys 3 board reference manual: `https://digilent.com/reference/_media/basys3:basys3_rm.pdf`
- Online VHDL simulator: `https://www.edaplayground.com/x/A4`