5th Semester Regular / Back Examination: 2021-22
OPERATING SYSTEMS
Branch: CSE, CST, ELECTRICAL & C.E,
ELECTRONICS & C.E, IT
Max Marks: 100
me: 3 Hours
Code: OF320

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part- I

Q1 Only Short Answer Type Questions (Answer All-10) (02×10)
a) What is Process Control Block (PCB)? (2)
b) What is meant by Context Switch? (2)
c) Distinguish between demand-paging and pre-paging? (2)
d) What are necessary conditions which can lead to a deadlock situation in a system? (2)
e) State the main difference between logical from physical address space. (2)
f) Explain Belady's Anomaly? (2)
g) What is a binary semaphore? What is its use? (2)
h) Define latency, transfer, and seek time with respect to disk I/O. (2)
i) What is the difference between Hard and Soft real-time systems? (2)
j) What is DRAM? In which form does it store data? (2)

Part- II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (06×08)
a) Explain briefly about, processor, assembler, compiler, loader, linker, and the functions executed by them. (6)
b) Explain Memory Partitioning, Paging, Segmentation. (6)
c) Differentiate between multi-tasking, multi programming and multi-threading? (6)
d) Explain Readers-Writers problem using semaphores. (6)
e) Name the three types of schedulers and give functions of each. (6)
f) When does race condition take place? What are the three requirements that must be satisfied by any possible solution to a critical section problem? (6)
g) Assume we have a demand-paged memory. The page table is held in registers. It takes 8 milliseconds to service a page fault if an empty page is available or the replaced page is not modified, and 20 milliseconds if the replaced page is modified. Memory access time is 100 nanoseconds. Assume that the page to be replaced is modified 70 percent of the time. What is the maximum acceptable page-fault rate for an effective access time of no more than 200 nanoseconds? (6)
h) State at least five differences between static linking and dynamic linking. (6)
i) A snapshot of the resource information of a system is given below for processes. (6)

Process ID	Allocation				Max				Available			
	A	B	C	D	A	B	C	D	A	B	C	D
P0	0	0	1	2	0	0	1	2	1	5	2	0
P1	1	0	0	0	1	7	5	0				
P2	1	3	5	4	2	3	5	6				
P3	0	6	3	2	0	6	5	2				
P4	0	0	1	4	0	6	5	6				

If a request from process P1 arrives for (0, 4, 2, 0), can the request be granted immediately?

j) Consider the two-dimensional array A: (6)

int A[ ][ ] = new int [8] [8];

where A[0][0] is at location 8 in a paged memory system with pages of size 8. A small process that manipulates the matrix resides in page 0 (location 0 to 7). Thus, every instruction fetch will be from page 0. For three page frames, how many page faults are generated by the following array-initialization loops, using LRU replacement and assuming that page 1 contains the process and the other two are initially empty?

(i)   for (int j=0; j<8; j++)
         for(int i=0; i<8; i++)
              A [i] [j] = 0;

(ii)   for (int i 0; i 8; i++)
          for(int j 0; j 8; j++)
               A [i] [j] 0;   **(6)**

Disk request comes to the disk driver for cylinder 10, 22, 20, 2, 40, 6 and 38 in the same order. A seek takes 6ms per cylinder move. How much seek time is needed, if following disk scheduling

k)   algorithm is taken. In each case the disk head is parked at cylinder 20.

i) C-LOOK (initially moving towards last cylinder)

ii) Closest Cylinder Next

Assume we have a demand-paged memory. The page table is held in registers. It takes 8 milliseconds to service a page fault if an empty page is available or the replaced page is not   **(6)**

l)   modified, and 20 milliseconds if the replaced page is modified. Memory access time is 100 nanoseconds. Assume that the page to be replaced is modified 70 percent of the time. What is the maximum acceptable page-fault rate for an effective access time of no more than 200 nanoseconds?

Only Long Answer Type Questions (Answer Any Two out of Four)   **(02×16)**

Q3   When does race condition take place? What are the three requirements that must be satisfied by any possible solution to a critical section problem? Describe Peterson's solution for critical section problem and show that this solution meets the above requirement. Also mention the limitation of Peterson's solution.   **(16)**

Q4   Assume, we have the workload as shown below. All 5 processes arrive at time 0, in the order given below. The length of the CPU burst time is given in milliseconds https://www.bputonline.com   **(16)**

Process: P1   P2   P3   P4   P5
Burst time: 10   29   3   7   12

Considering the FCFS, SJF and RR (q=10 ms) scheduling algorithms. Prepare the Gantt-chart and find out which algorithm would give the minimum average turnaround time.

Q5   Define distributed system. List and explain the characteristics of distributed system? What are the Advantages of Distributed Systems? Mention the challenges in distributed system.   **(16)**

Q6   A processor uses 2-level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns. Assuming that no page faults occur, compute the average time taken to access a virtual address approximately (to the nearest 0.5 ns).   **(16)**