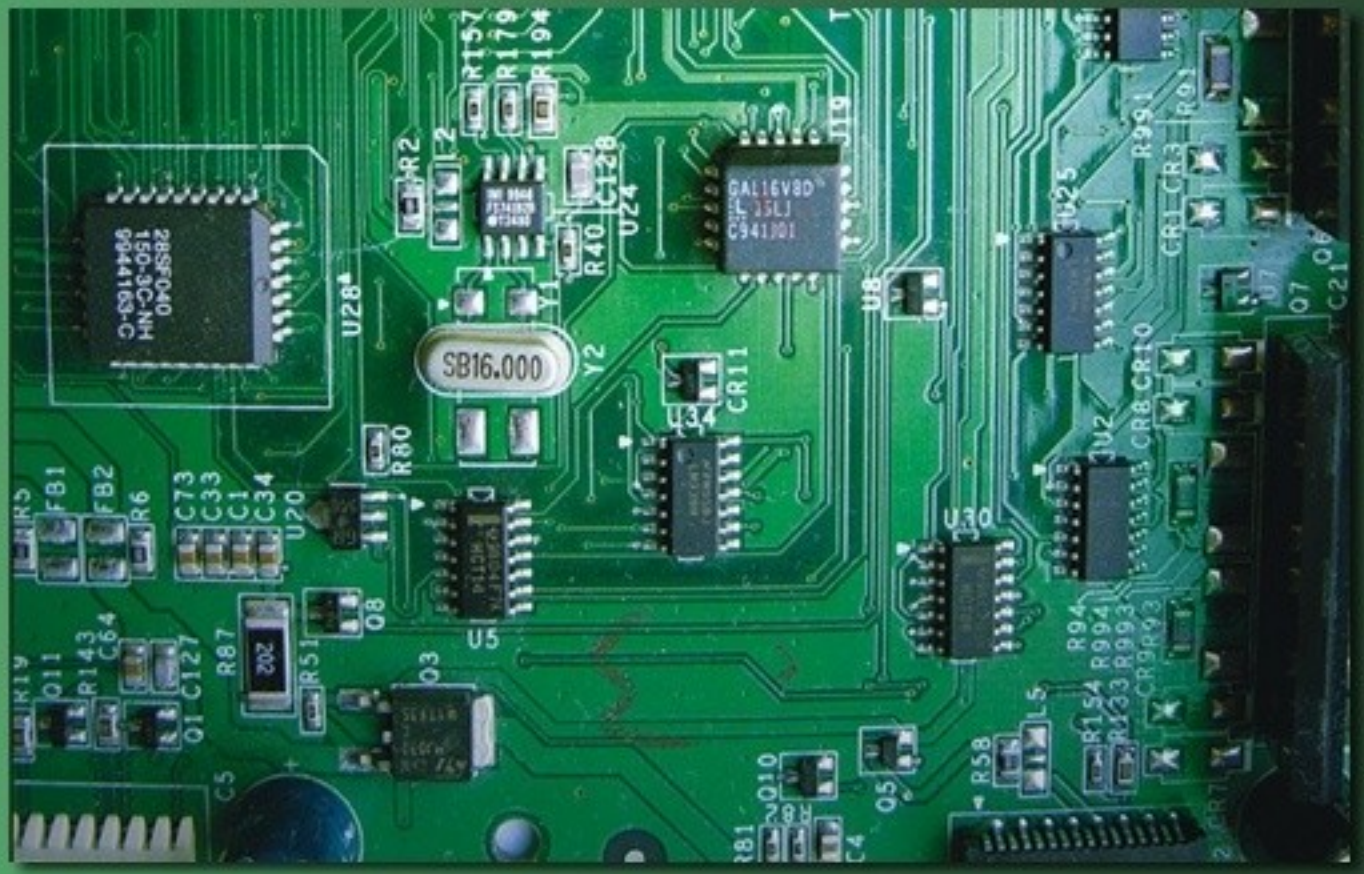
The Intel Microprocessors

8086/8088, 80186/80188, 80286, 80386, 80486 Pentium, Pentium Pro Processor, Pentium II, Pentium 4, and Core2 with 64-bit Extensions

Architecture, Programming, and Interfacing



EIGHTH EDITION

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Chapter 9: 8086/8088 Hardware Specifications

Introduction

- In this chapter, the pin functions of both the 8086 and 8088 microprocessors are detailed and information is provided on the following hardware topics: clock generation, bus buffering, bus latching, timing, wait states, and minimum mode operation versus maximum mode operation.
- These simple microprocessors are explained as an introduction to the Intel microprocessor family.

Chapter Objectives

Upon completion of this chapter, you will be able to:

- Describe function of each 8086 & 8088 pin.
- Understand the microprocessor's DC characteristics and indicate its fan-out to common logic families.
- Use the clock generator chip (8284A) to provide the clock for the microprocessor.
- Connect buffers and latches to the buses.

Chapter Objectives (*cont.*)

Upon completion of this chapter, you will be able to:

- Interpret the timing diagrams.
- Describe wait states and connect the circuitry required to cause various numbers of waits.
- Explain the difference between minimum and maximum mode operation.

9–1 PIN-OUTS AND THE PIN FUNCTIONS

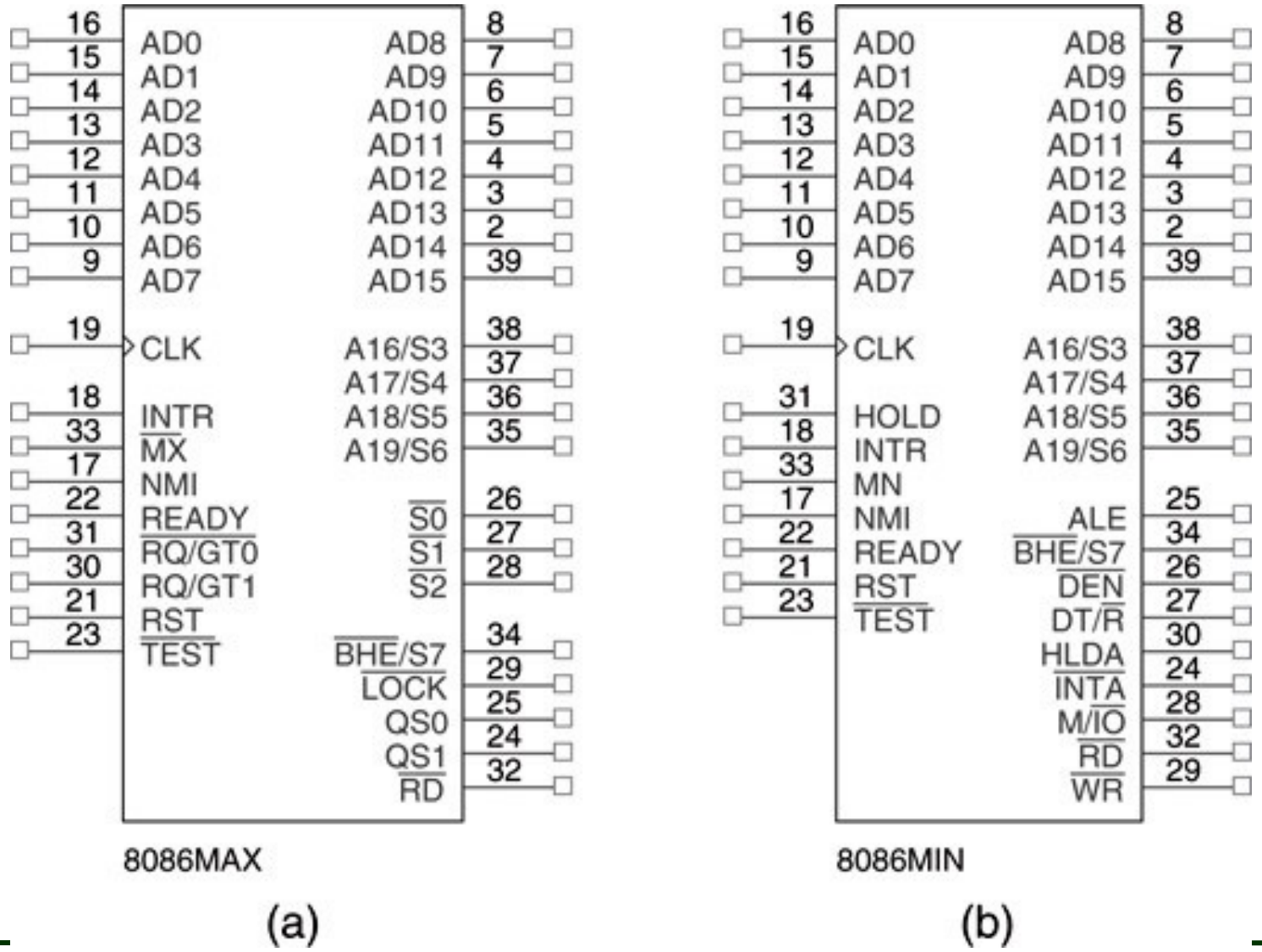
- In this section, we explain the function and the multiple functions of each of the microprocessor's pins.
- In addition, we discuss the DC characteristics to provide a basis for understanding the later sections on buffering and latching.

The Pin-Out

- Figure 9–1 illustrates pin-outs of 8086 & 8088.
  - both are packaged in 40-pin **dual in-line** packages (DIPs)
- 8086 is a 16-bit microprocessor with a 16-bit data bus; 8088 has an 8-bit data bus.
  - 8086 has pin connections AD_0–AD_{15}
  - 8088 has pin connections AD_0–AD_7
- Data bus width is the only major difference.
  - thus 8086 transfers 16-bit data more efficiently

- There is, however, a minor difference in one of the control signals. The 8086 has an M/$\overline{IO}$ pin, and the 8088 has an IO/$\overline{M}$ pin.
- The only other hardware difference appears on Pin 34 of both integrated circuits: on the 8088, it is an SS0 pin, whereas on the 8086, it is a $\overline{BHE}$/S7 pin.

Figure 9–1 (a) The pin-out of the 8086 in maximum mode; (b) the pin-out of the 8086 in minimum mode.



Power Supply Requirements

- Both microprocessors require **+5.0 V** with a supply voltage tolerance of ±10 percent.
  - 8086 uses a maximum supply current of 360 mA
  - 8088 draws a maximum of 340 mA
- Both microprocessors operate in ambient temperatures of between 32° F and 180° F.
- 80C88 and 80C86 are CMOS versions that require only 10 mA of power supply current.
  - and function in temperature extremes of –40° F through +225° F

DC Characteristics

- It is impossible to connect anything to a microprocessor without knowing input current requirement for an input pin.
  - and the output current drive capability for an output pin
- This knowledge allows hardware designers to select proper interface components for use with the microprocessor
  - without the fear of damaging anything

Input Characteristics

- Input characteristics of these microprocessors are compatible with all the standard logic components available today.
- Table 9–1 depicts input voltage levels and the input current requirements for any input pin on either microprocessor.

Logic Level	Voltage	Current
0	0.8 V maximum	±10 μA maximum
1	2.0 V minimum	±10 μA maximum

Output Characteristics

- Table 9–2 illustrates output characteristics of all the output pins of these microprocessors.
- The logic 1 voltage level of the 8086/8088 is compatible with most standard logic families.
  - logic 0 level is not
- Standard logic circuits have a maximum logic 0 voltage of 0.4 V; 8086/8088 has a maximum of 0.45 V.
  - a difference of 0.05 V

- This difference reduces the noise immunity from 400 mV (0.8 V – 0.45 V) to 350 mV.
  - noise immunity is the difference between logic 0 output voltage and logic 0 input voltage levels
- Reduction in noise immunity may result in problems with long wire connections or too many loads.
- No more than 10 loads of any type should be connected to an output pin without buffering
  - if this factor is exceeded, noise will begin to take its toll in timing problems

Pin Connections AD_7 - AD_0

- 8088 **address/data bus** lines are multiplexed
  - and contain the rightmost 8 bits of the memory address or I/O port number whenever ALE is active (logic 1)
  - or data whenever ALE is inactive (logic 0)
- These pins are at their high-impedance state during a hold acknowledge.

Pin Connections A_{15} - A_8

- 8088 **address bus** provides the upper-half memory address bits that are present throughout a bus cycle.
- These address connections go to their high-impedance state during a hold acknowledge.

Pin Connections AD_{15} - AD_8

- 8086 **address/data bus** lines compose upper multiplexed address/data bus on the 8086.
- These lines contain address bits A_{15}–A_8 whenever ALE is a logic 1, and data bus connections D_{15}–D_8 when ALE is a logic 0.
- These pins enter a high-impedance state when a hold acknowledge occurs.

Pin Connections A_{19}/S_6 - A_{16}/S_3

- **Address/status bus** bits are multiplexed to provide address signals A_{19}–A_{16} and status bits S_6–S_3.
  - high-impedance state during hold acknowledge
  - status bit S_6 is always **logic 0**,
  - bit S_5 indicates the condition of the **IF flag bit**
- S_4 and S_3 show which segment is accessed during the current bus cycle.
  - these status bits can address four separate 1M byte memory banks by decoding as A_{21} and A_{20}

TABLE 9–4 Function of status bits S_3 and S_4.

S_4	S_3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

Pin Connections $\overline{RD}$

- When **read signal** is logic 0, the data bus is receptive to data from memory or I/O devices
  - pin floats high-impedance state during a hold acknowledge

Ready

- Inserts wait states into the timing.
  - if placed at a logic 0, the microprocessor enters into wait states and remains idle
  - if logic 1, no effect on the operation

Pin Connections INTR

- **Interrupt request** is used to request a hardware interrupt.
  - If INTR is held high when IF = 1, 8086/8088 enters an interrupt acknowledge cycle after the current instruction has completed execution

NMI

- The **non-maskable interrupt** input is similar to INTR.
  - does not check IF flag bit for logic 1
  - if activated, uses interrupt vector 2

Pin Connections $\overline{\text{TEST}}$

- The **Test** pin is an input that is tested by the WAIT instruction.
- If **$\overline{\text{TEST}}$** is a logic 0, the WAIT instruction functions as an NOP.
- If **$\overline{\text{TEST}}$** is a logic 1, the WAIT instruction waits for **$\overline{\text{TEST}}$** to become a logic 0.
- The **$\overline{\text{TEST}}$** pin is most often connected to the 8087 numeric coprocessor.

Pin Connections RESET

- Causes the microprocessor to reset itself if held high for a minimum of four clocking periods.
  - when 8086/8088 is reset, it executes instructions at memory location FFFFOH (CS = FFFFH, and IP = 0000H, so PA will be FFFF0H)
  - also disables future interrupts by clearing IF flag

CLK

- The **clock** pin provides the basic timing signal.
  - must have a duty cycle of 33 % (high for one third of clocking period, low for two thirds) to provide proper internal timing

Pin Connections VCC

- This **power supply** input provides a +5.0 V, ±10 % signal to the microprocessor.

GND

- The **ground** connection is the return for the power supply.
  - 8086/8088 microprocessors have two pins labeled GND—both must be connected to ground for proper operation

Pin Connections MN/$\overline{MX}$

- **Minimum/maximum** mode pin selects either minimum or maximum mode operation.
  - if minimum mode selected, the MN/$\overline{MX}$ pin must be connected directly to +5.0 V

BHE S_7

- The **bus high enable** pin is used in 8086 to enable the most-significant data bus bits (D_{15}–D_8) during a read or a write operation.
- The state of S_7 is always a logic 1.

Minimum Mode Pins

- Minimum mode operation is obtained by connecting the MN/$\overline{\text{MX}}$ pin directly to +5.0 V.
  - do not connect to +5.0 V through a pull-up register; it will not function correctly

IO/$\overline{\text{M}}$ or M/$\overline{\text{IO}}$

- The **IO/$\overline{\text{M}}$** (8088) or **M/$\overline{\text{IO}}$** (8086) pin selects memory or I/O.
  - indicates the address bus contains either a memory address or an I/O port address.
  - high-impedance state during hold acknowledge

Minimum Mode Pins $\overline{\text{WR}}$

- **Write line** indicates 8086/8088 is outputting data to a memory or I/O device.
  - during the time $\overline{\text{WR}}$ is a logic 0, the data bus contains valid data for memory or I/O
  - high-impedance during a hold acknowledge

$\overline{\text{INTA}}$

- The **interrupt acknowledge** signal is a response to the INTR input pin.
  - normally used to gate the interrupt vector number onto the data bus in response to an interrupt request.

Minimum Mode Pins ALE

- **Address latch enable** shows the 8086/8088 address/data bus contains an address.
  - can be a memory address or an I/O port number
  - ALE signal doesn't float during hold acknowledge

DT/$\overline{R}$

- The **data transmit/receive** signal shows that the microprocessor data bus is transmitting (**DT/$\overline{R}$ = 1**) or receiving (**DT/$\overline{R}$ = 0**) data.
  - used to enable external data bus buffers

Minimum Mode Pins DEN

- **Data bus enable** activates external data bus buffers.

HOLD

- **Hold input** requests a direct memory access (DMA).
  - if HOLD signal is a logic 1, the microprocessor stops executing software and places address, data, and control bus at high-impedance
  - if a logic 0, software executes normally

Minimum Mode Pins HLDA

- **Hold acknowledge** indicates the 8086/8088 has entered the hold state.

$\overline{SS0}$

- The $\overline{SS0}$ status line is equivalent to the S_0 pin in maximum mode operation.
- Signal is combined with **IO/$\overline{M}$** and **DT/$\overline{R}$** to decode the function of the current bus cycle.

TABLE 9–5 Bus cycle status (8088) using $\overline{SS0}$.

$IO/\overline{M}$	$DT/\overline{R}$	$\overline{SS0}$	*Function*
0	0	0	Interrupt acknowledge
0	0	1	Memory read
0	1	0	Memory write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	Passive

Maximum Mode Pins

- In order to achieve maximum mode for use with external coprocessors, connect the MN/$\overline{\text{MX}}$ pin to ground.

$\overline{\text{S2}}$, $\overline{\text{S1}}$, and $\overline{\text{S0}}$

- **Status bits** indicate function of the current bus cycle.
  - normally decoded by the 8288 bus controller

TABLE 9–6 Bus control function generated by the bus controller (8288).

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

Maximum Mode Pins $\overline{\text{RQ}}$/$\overline{\text{GT1}}$

- The **request/grant** pins request direct memory accesses (DMA) during maximum mode operation.
  - bidirectional; used to request and grant a DMA operation

$\overline{\text{LOCK}}$

- The **lock** output is used to lock peripherals off the system. This pin is activated by using the LOCK: prefix on any instruction.

Maximum Mode Pins QS_1 and QS_0

- The **queue status** bits show the status of the internal instruction queue.
  - provided for access by the 8087 numeric coprocessor

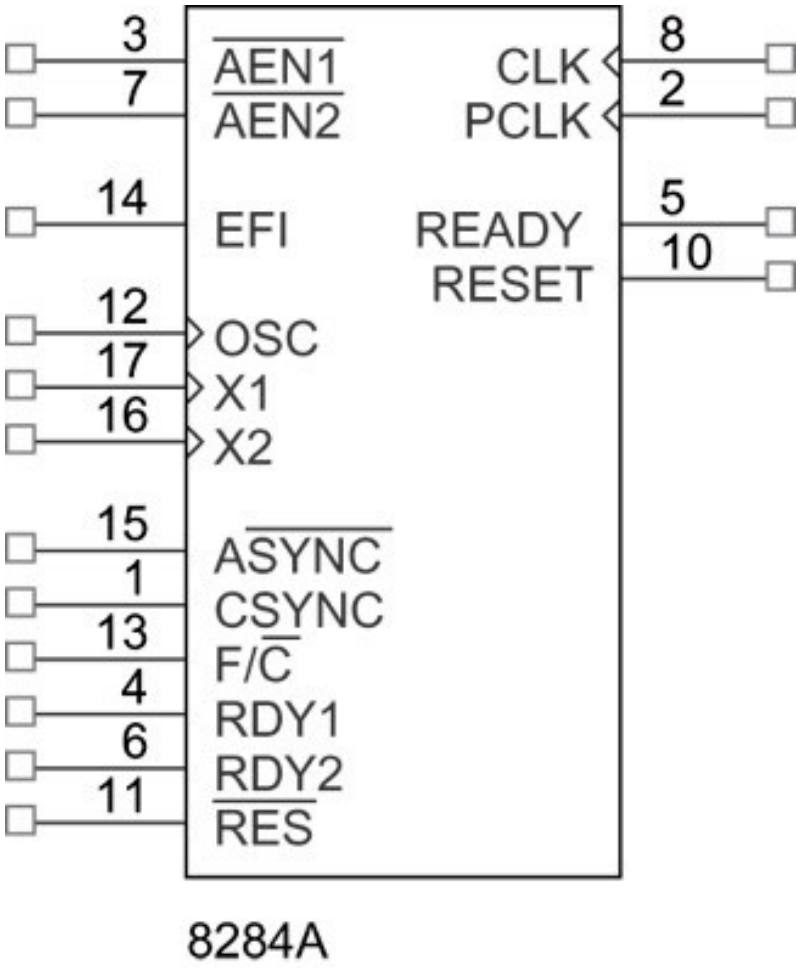
TABLE 9–7 Queue status bits.

QS_1	QS_0	*Function*
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

9–2 CLOCK GENERATOR (8284A)

- This section describes the 8484A clock generator and the RESET signal.
  - also introduces the READY signal for 8086/8088
- With no clock generator, many circuits would be required to generate the clock (CLK).
- 8284A provides the following basic functions:
  - clock generation; RESET & READY synch;
  - TTL-level peripheral clock signal
- Figure 9–2 shows pin-outs of the 8284A

Figure 9–2 The pin-out of the 8284A clock generator.



8284A *Pin Functions*

- 8284A is an 18-pin integrated circuit designed specifically for use 8086/8088.

$\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$

- The **address enable** pins are provided to qualify bus ready signals, RDY1 and RDY2.
  - used to cause wait states
- Wait states are generated by the READY pin of 8086/8088 controlled by these two inputs.

Pin Functions RDY_1 and RDY_2

- The **bus ready** inputs are provided, in conjunction with the $\overline{AEN1}$ & $\overline{AEN2}$ pins, to cause wait states in 8086/8088.

$\overline{ASYNC}$

- The **ready synchronization** selection input selects either one or two stages of synchronization for the RDY_1 and RDY_2 inputs.

Pin Functions READY

- **8284 Ready** is an output pin that connects to the 8086/8088 READY input.
  - synchronized with the RDY_1 and RDY_2 inputs

X_1 and X_2

- The **crystal oscillator** pins connect to an external crystal used as the timing source for the clock generator and all its functions

Pin Functions F/$\overline{C}$

- The **frequency/crystal** select input chooses the clocking source for the 8284A.
  - if held high, an external clock is provided to the EFI input pin
  - if held low, the internal crystal oscillator provides the timing signal
- The external frequency input is used when the **F/$\overline{C}$** pin is pulled high.
- EFI supplies timing when the **F/$\overline{C}$** pin is high.

Pin Functions CLK

- The **clock output** pin provides the CLK input signal to 8086/8088 and other components.
  - output signal is one third of the crystal or EFI input frequency
  - 33% duty cycle required by the 8086/8088

PCLK

- The **peripheral clock** signal is one sixth the crystal or EFI input frequency.
  - PCLK output provides a clock signal to the peripheral equipment in the system

Pin Functions OSC

- **Oscillator output** is a TTL-level signal at the same frequency as crystal or EFI input.
  - OSC output provides EFI input to other 8284A clock generators in multiple-processor systems

$\overline{\text{RES}}$

- **Reset input** is an active-low input to 8284A.
  - often connected to an RC network that provides power-on resetting

Pin Functions RESET

- **Reset output** is connected to the 8086/8088 RESET input pin.

CSYNCH

- The **clock synchronization** pin is used when the EFI input provides synchronization in systems with multiple processors.
  - if internal crystal oscillator is used, this pin must be grounded

Pin Functions GND

- The **ground pin** connects to ground.

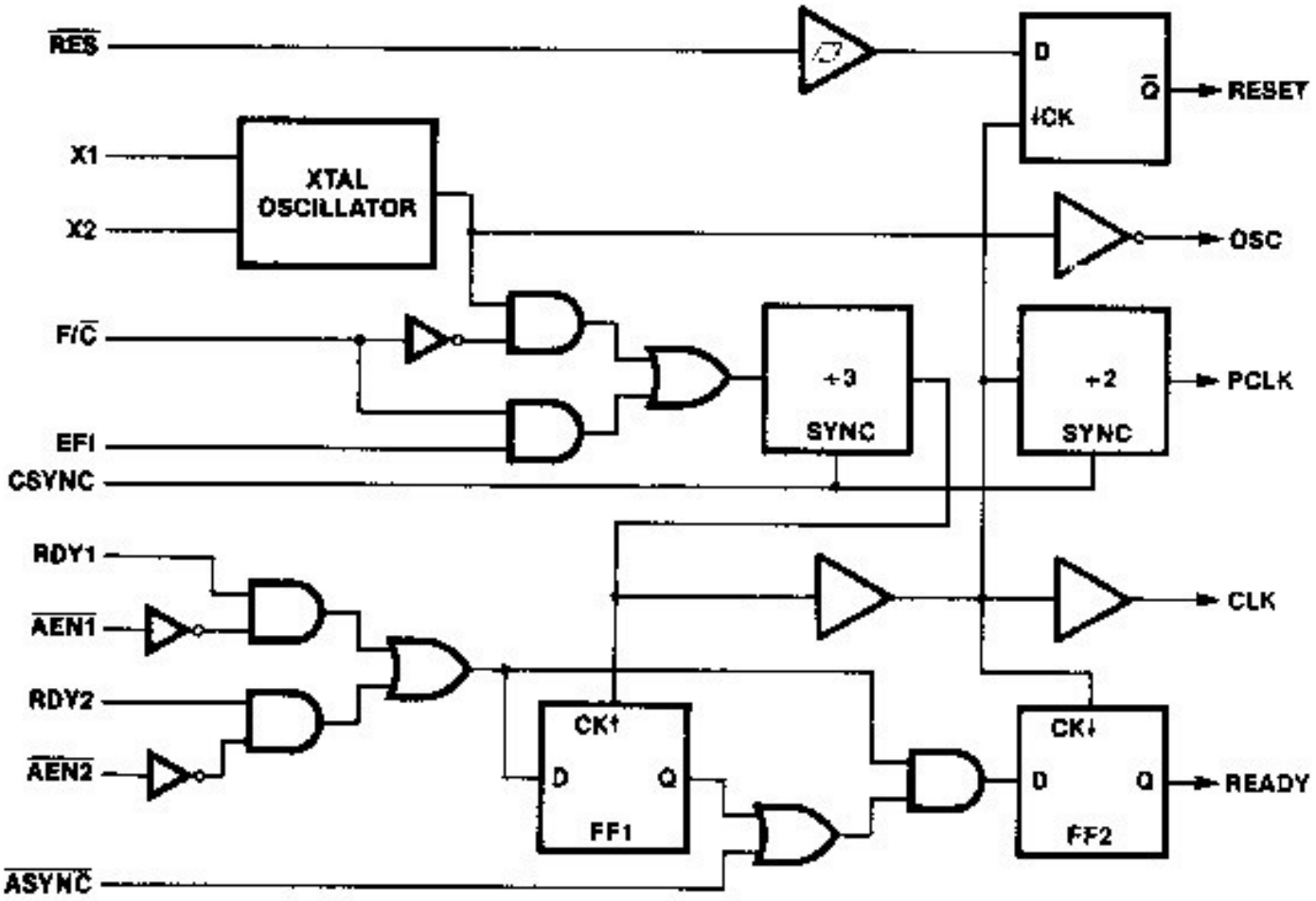
VCC

- This **power supply** pin connects to +5.0 V with a tolerance of ±10%.

Operation of the 8284A

- The 8284A is a relatively easy component to understand.
- Figure 9–3 illustrates the internal timing diagram of the 8284A clock generator.
- The top half of the logic diagram represents the clock and synchronization section of the 8284A clock generator.

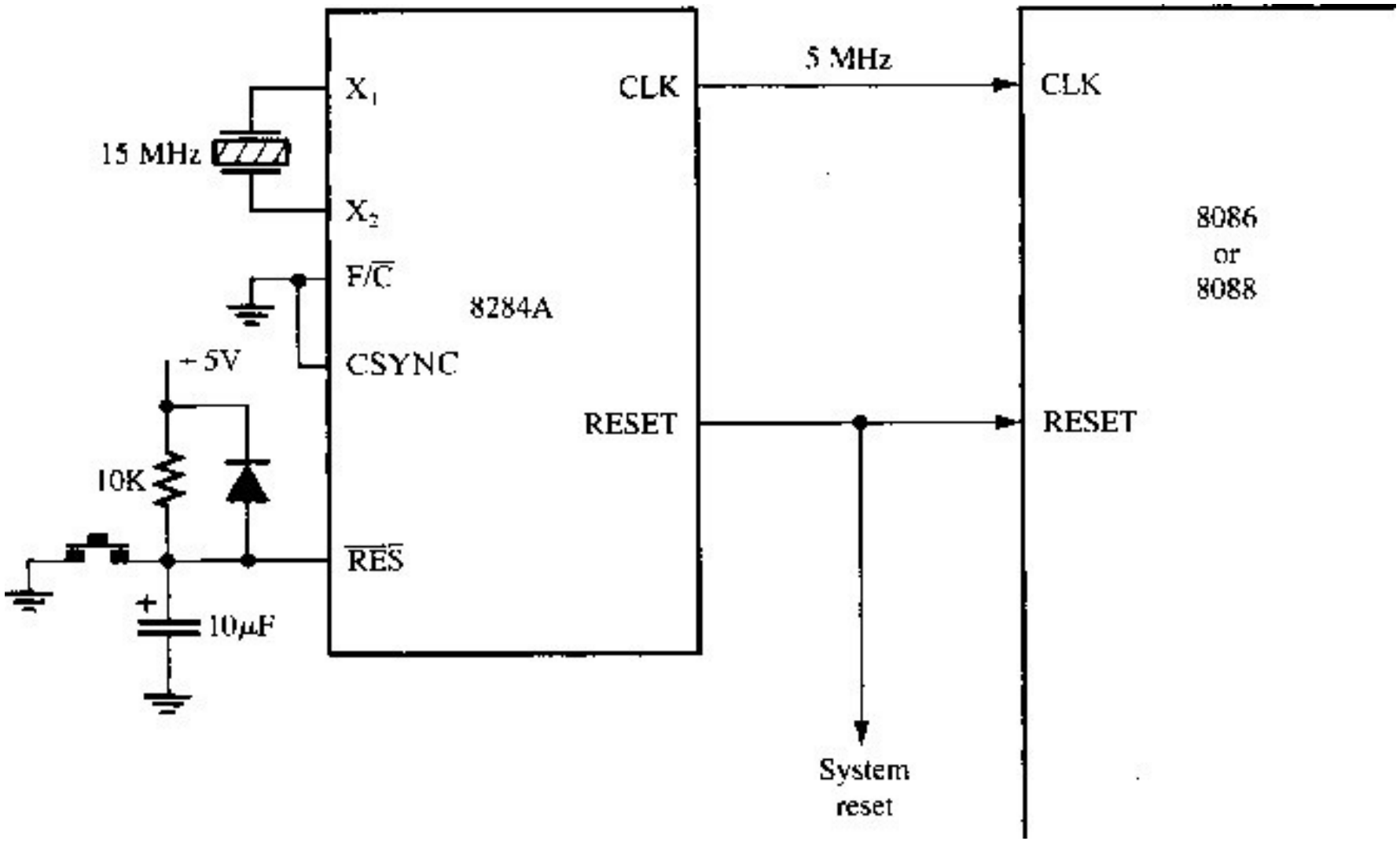
Figure 9–3 The internal block diagram of the 8284A clock generator.



Operation of the Clock Section

- Crystal oscillator has two inputs: X_1 and X_2.
  - if a crystal is attached to X_1 and X_2, the oscillator generates a square-wave signal at the same frequency as the crystal
- The square-wave is fed to an AND gate & an inverting buffer to provide an OSC output.
- The OSC signal is sometimes used as an EFI input to other 8284A circuits in a system.
- Figure 9–4 shows how an 8284A is connected to the 8086/8088.

Figure 9–4 The clock generator (8284A) and the 8086 and 8088 microprocessors illustrating the connection for the clock and reset signals. A 15 MHz crystal provides the 5 MHz clock for the microprocessor.



Operation of the Reset Section

- The reset section of 8284A consists of a Schmitt trigger buffer and a D-type flip-flop.
  - the D-type flip-flop ensures timing requirements of 8086/8088 RESET input are met
- This circuit applies the RESET signal on the negative edge (1-to-0 transition) of each clock.
- 8086/8088 microprocessors sample RESET at the positive edge (0-to-1 transition) clocks.
  - thus, this circuit meets 8086/8088 timing requirements

9–3 BUS BUFFERING AND LATCHING

- Before 8086/8088 can be used with memory or I/O interfaces, their multiplexed buses must be demultiplexed.
- This section provides detail required to demultiplex the buses and illustrates how the buses are buffered for very large systems.
  - because the maximum fan-out is 10, the system must be buffered if it contains more than 10 other components

Demultiplexing the Buses

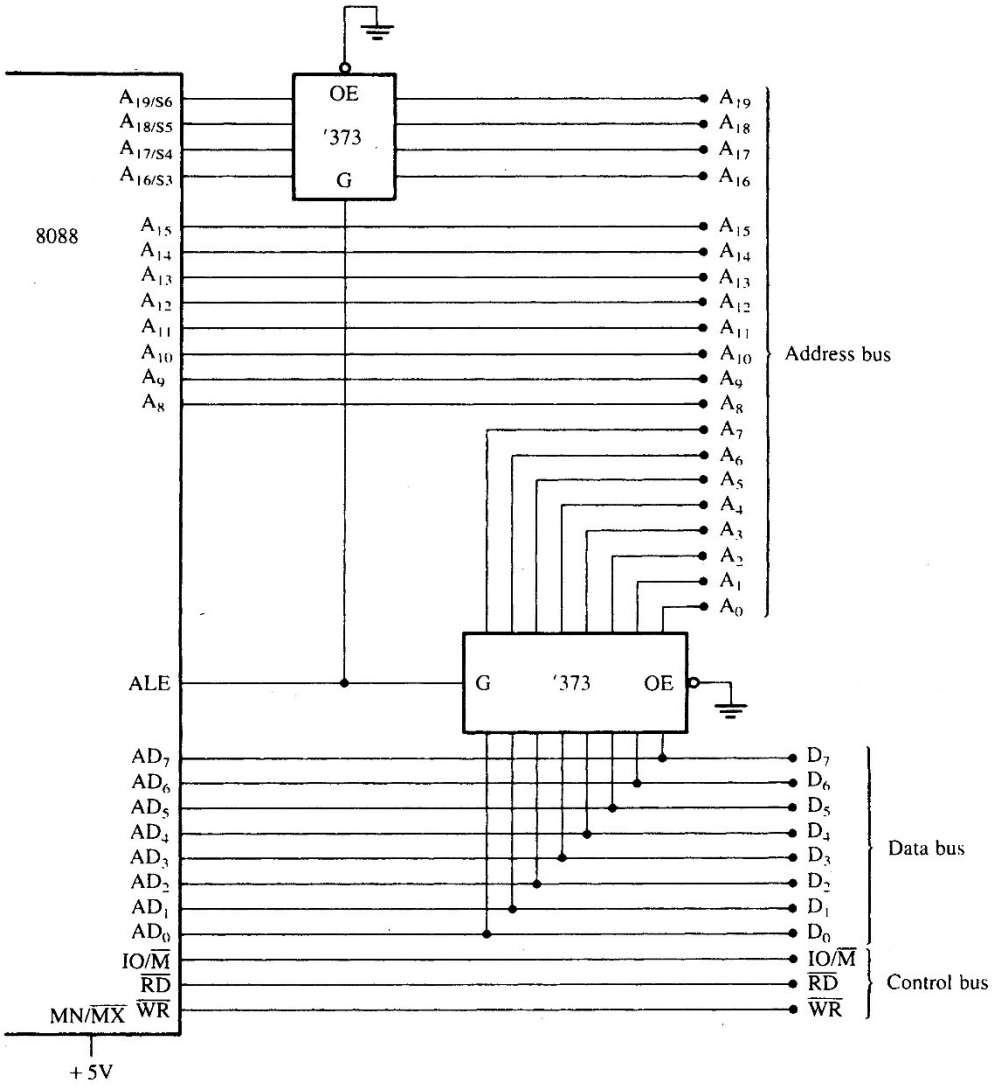
- The address/data bus of the 8086/8088 is multiplexed (shared) to reduce the number of pins required for the integrated circuit
  - the hardware designer must extract or demultiplex information from these pins
- Memory & I/O require the address remain valid and stable throughout a read/write cycle.
- If buses are multiplexed, the address changes at the memory and I/O, causing them to read or write data in the wrong locations

- All computer systems have three buses:
  - an address bus that provides memory and I/O with the memory address or the I/O port number
  - a data bus that transfers data between the microprocessor and the memory and I/O
  - a control bus that provides control signals to the memory and I/O
- These buses must be present in order to interface to memory and I/O.

Demultiplexing the 8088

- Figure 9–5 illustrates components required to demultiplex 8088 buses.
  - two 74LS373 or 74LS573 transparent latches are used to demultiplex the address/data bus connections AD_7–AD_0
  - and address/status connections A_{19}/S_6–A_{16}/S_3
- The latches, which are like wires whenever the address latch enable pin (ALE) becomes a logic 1, pass the inputs to the outputs.

Figure 9–5 The 8088 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8088-based systems.

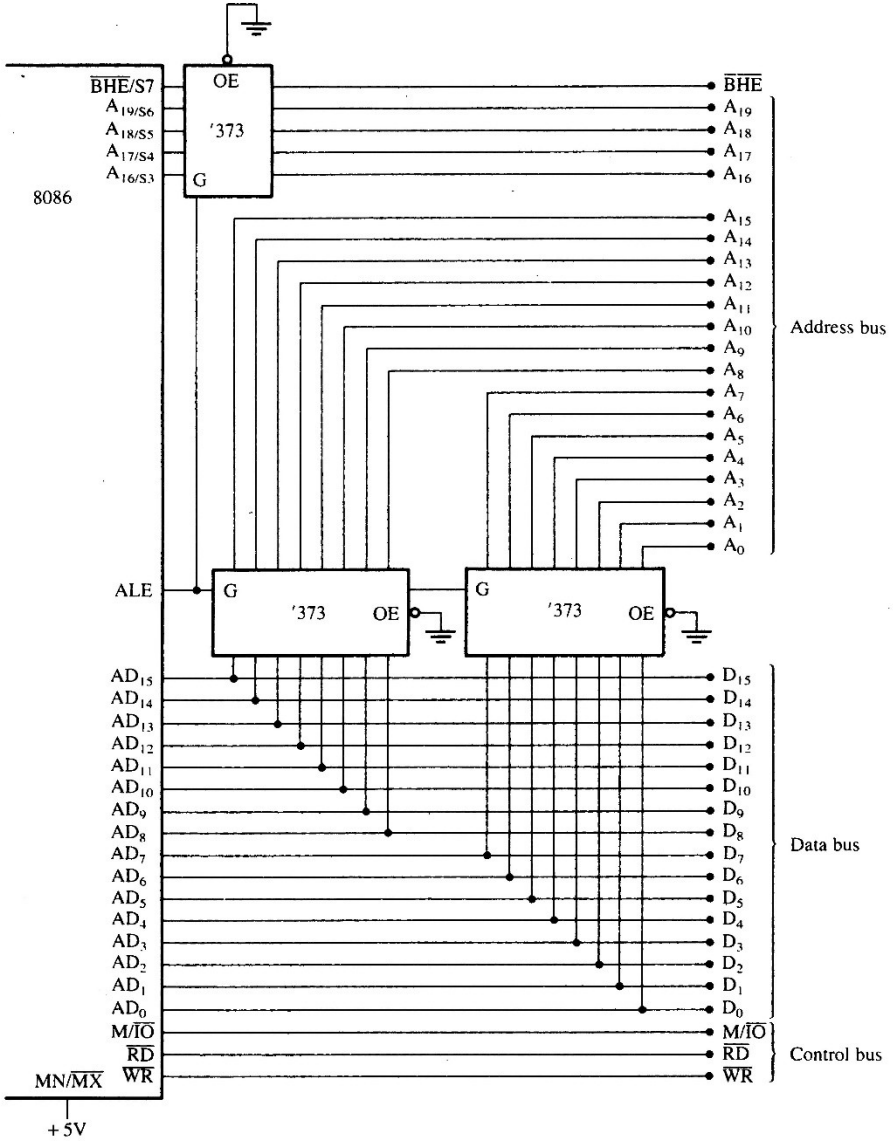


- After a short time, ALE returns to logic 0 causing the latches to remember inputs at the time of the change to a logic 0.
- This yields a separate address bus with connections A_{19}–A_0.
  - these allow 8088 to address 1Mb of memory
- The separate data bus allows it to be connected to any 8-bit peripheral device or memory component.

Demultiplexing the 8086

- Fig 9–6 illustrates a demultiplexed 8086 with all three buses:
- address (A_{19}–A_0 and $\overline{BHE}$)
- data (D_{15}–D_0),
- control (M/$\overline{IO}$,$\overline{RD}$, and $\overline{WR}$)
- Here, the memory and I/O system see the 8086 as a device with:
  - a 20-bit address bus;16-bit data bus
  - and a three-line control bus

Figure 9–6 The 8086 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8086-based systems.



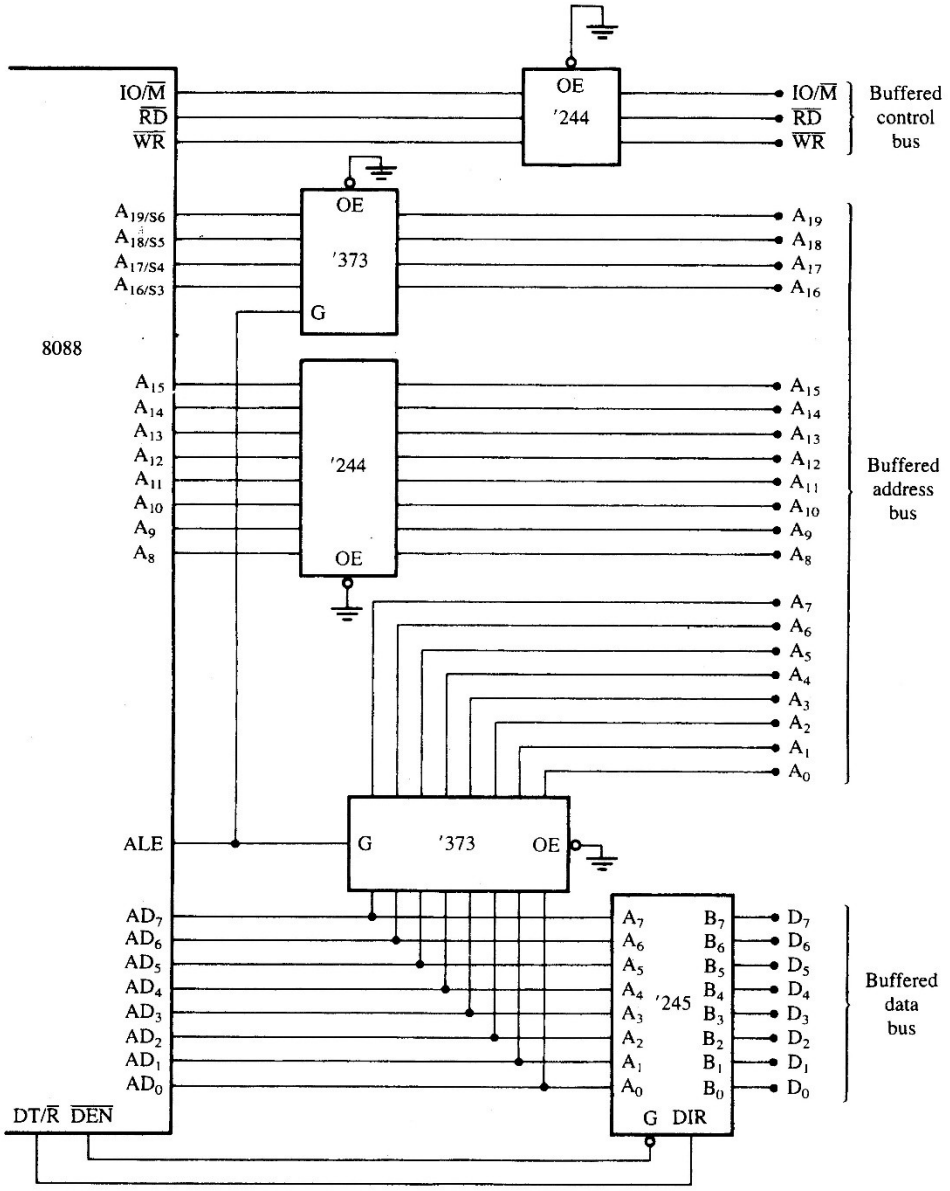
The Buffered System

- If more than 10 unit loads are attached to any bus pin, the entire system must be buffered.
- Buffer output currents have been increased so that more TTL unit loads may be driven.
- A fully buffered signal will introduce a timing delay to the system.
- No difficulty unless memory or I/O devices are used which function at near maximum bus speed.

The Fully Buffered 8088

- Figure 9–7 depicts a fully buffered 8088 microprocessor.
  - a fully buffered 8088 system requires two 74LS244s, one 74LS245, and two 74LS373s
- Direction of the 74LS245 is controlled by the $\overline{DT/R}$ signal.
  - enabled and disabled by the $\overline{DEN}$ signal

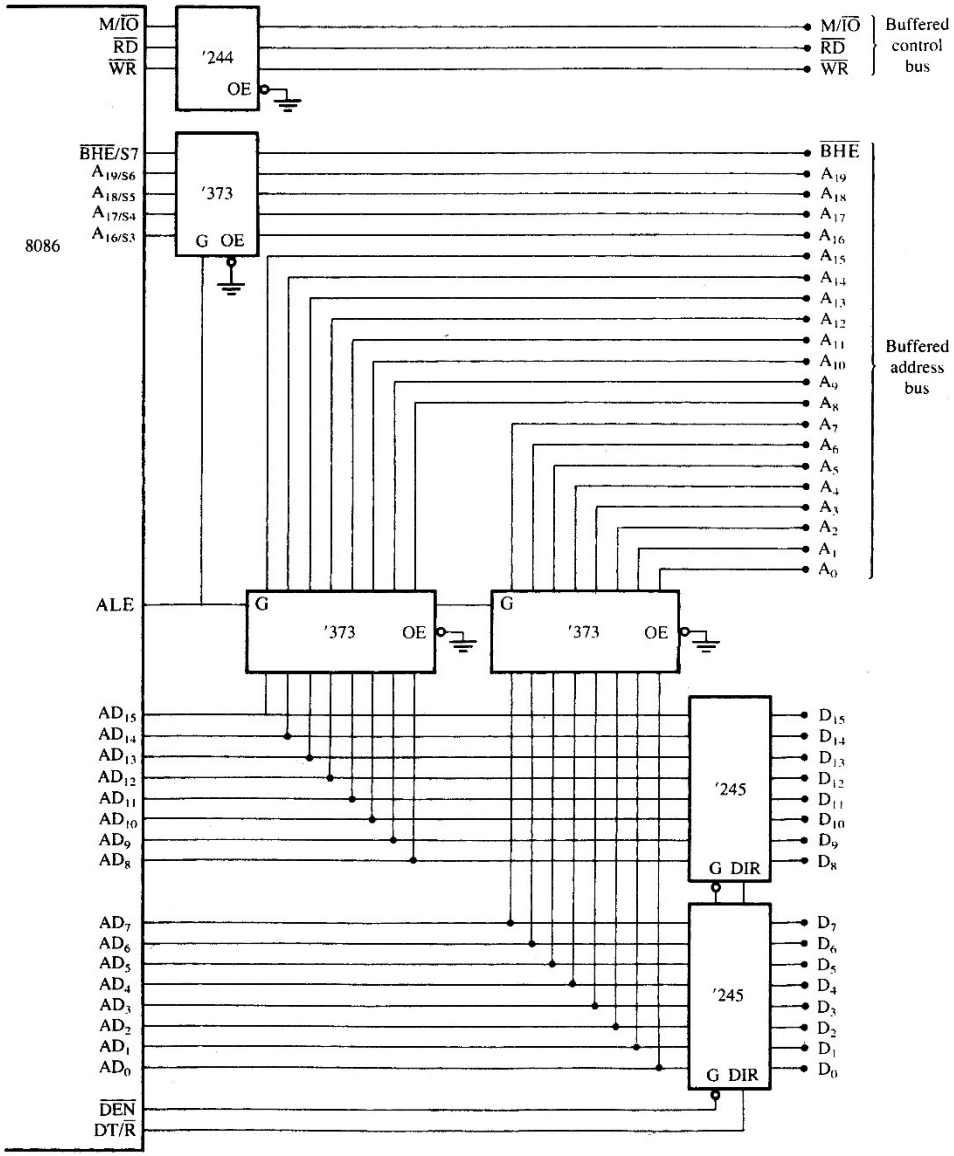
Figure 9–7 A fully buffered 8088 microprocessor.



The Fully Buffered 8086

- Figure 9–8 illustrates a fully buffered 8086.
  - a fully buffered 8086 system requires one 74LS244, two 74LS245s, and three 74LS373s
- 8086 requires one more buffer than 8088 because of the extra eight data bus connections, D_{15}–D_8.
- It also has a BHE signal that is buffered for memory-bank selection.

Figure 9–8 A fully buffered 8086 microprocessor.



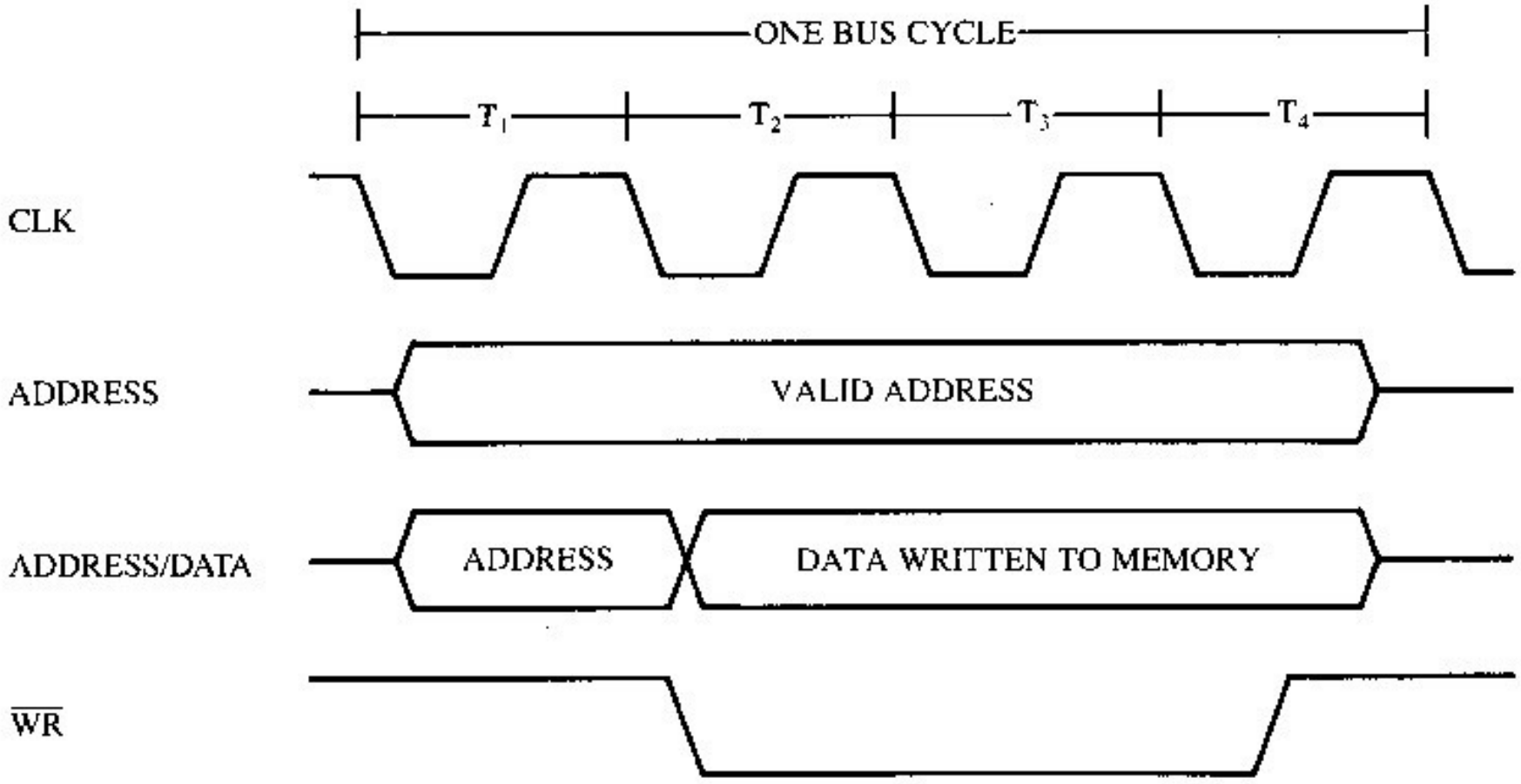
9–4 BUS TIMING

- It is essential to understand system bus timing before choosing memory or I/O devices for interfacing to 8086 or 8088 microprocessors.
- This section provides insight into operation of the bus signals and the basic read/write timing of the 8086/8088.
- *Bus cycle is the time required to make a single read or write operation between microprocessor and memory/IO device.*
  - Each bus cycle equals four system-clocking periods (T states)

Basic Bus Operation

- The three buses of 8086/8088 function the same way as any other microprocessor.
- If data are written to memory the processor:
  - outputs the memory address on the address bus
  - outputs the data to be written on the data bus
  - issues a write ($\overline{WR}$) to memory
  - and IO/$\overline{M}$= 0 for 8088 and M/$\overline{IO}$ = 1 for 8086
- See simplified timing for write in Fig 9–9.

Figure 9–9 Simplified 8086/8088 write bus cycle.



- During the first clocking period (T1) in a bus cycle many things happen:
  - The address of memory or I/O location is sent out via the address bus and the address/data bus connections.
  - Control signals ALE, DT/$\overline{R}$, and IO/$\overline{M}$ (8088) or M/$\overline{IO}$ (8086) are also output.
  - The IO/$\overline{M}$ or M/$\overline{IO}$ signal indicates whether the address bus contains a memory address or an I/O device(port) number.

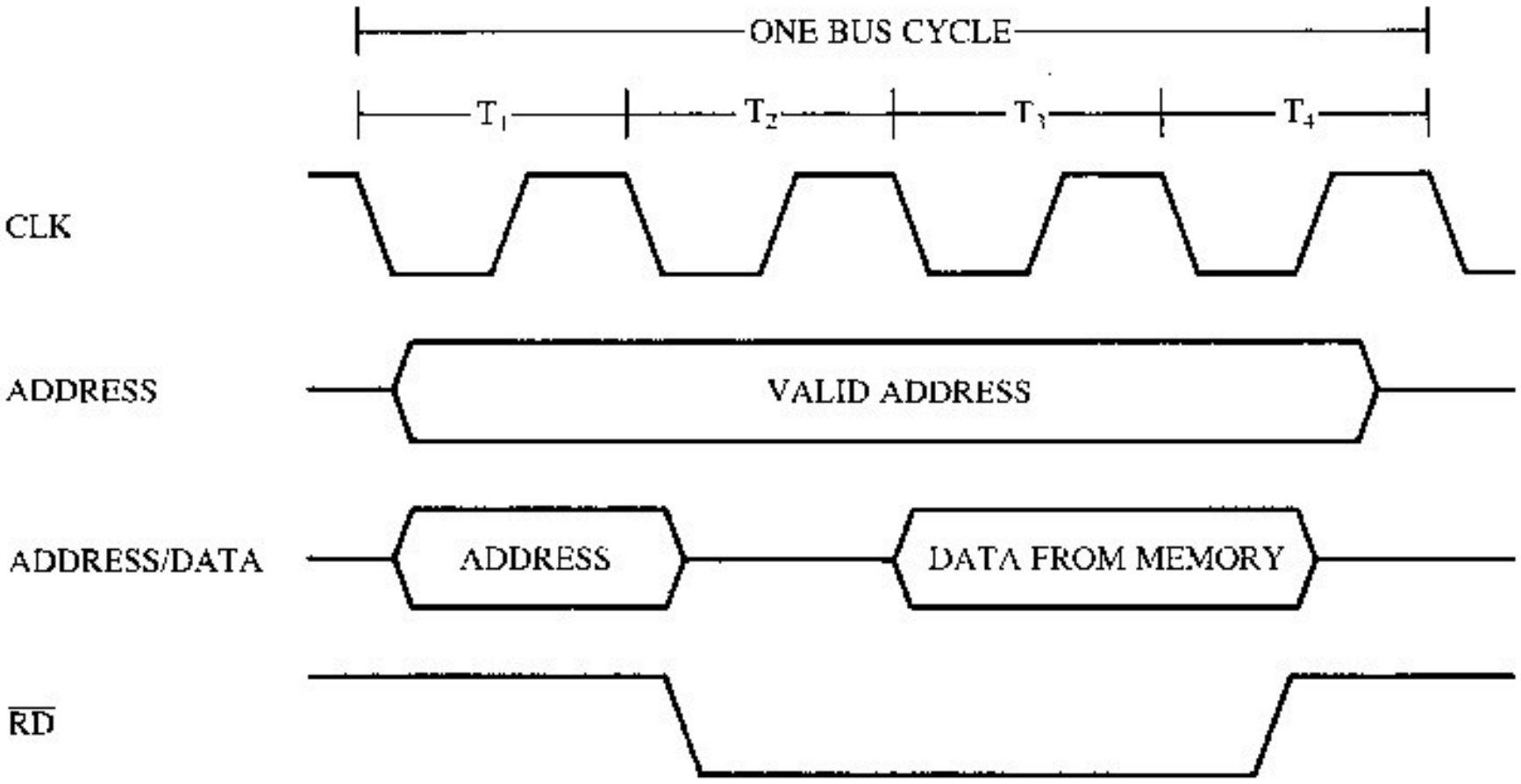
- During the second clocking period (T2):
  - The 8088/8086 microprocessor issue the $\overline{RD}$ or $\overline{WR}$ singnal, $\overline{DEN}$, and in the case of write, the data to be written appear on the data bus.
    - The $\overline{DEN}$ signal turns on the data bus buffers, if they are present in the system
  - These events cause the memory or I/O device to begin to perform a read or a write.

- During the third clocking period (T3):
  - READY is sampled at the end of T_2
    - If READY is low at this time, T_3 becomes a wait state.
  - This clocking period is provided to allow the memory time to access data.
  - If the bus cycle happens to be a read bus cycle, the data bus is sampled at the end of T_3

- During the fourth clocking period (T4):
  - All bus signals are deactivated in preparation for the next bus cycle.
  - Microprocessor samples the data bus connections for data that are read from memory or I/O.
  - Microprocessor transfers data to the memory or I/O

- If data are read from the memory the microprocessor:
  - outputs the memory address on the address bus
  - issues a read memory signal ($\overline{RD}$)
  - and accepts the data via the data bus
- See simplified timing for read in Fig 9–10.

Figure 9–10 Simplified 8086/8088 read bus cycle.



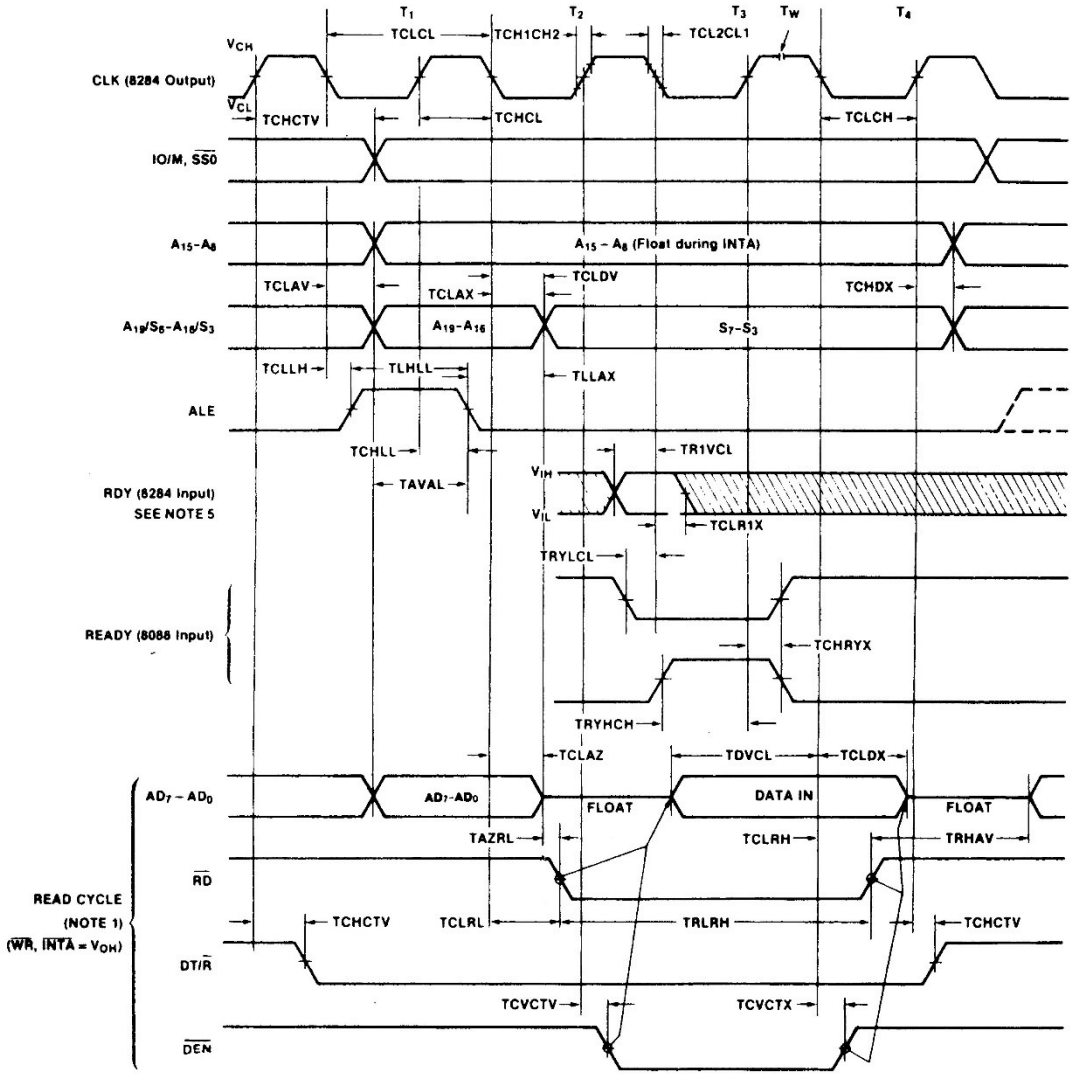
Timing in General

- 8086/8088 use memory and I/O in periods called bus cycles.
- Each cycle equals four system-clocking periods (T states).
  - newer microprocessors divide the bus cycle into as few as two clocking periods
- If the clock is operated at 5 MHz, one 8086/8088 bus cycle is complete in 800 ns.
  - basic operating frequency for these processors

- During the first clocking period in a bus cycle, called T1, many things happen:
  - the address of the memory or I/O location is sent out via the address bus and the address/data bus connections.
- During TI, control signals are also output.
  - indicating whether the address bus contains a memory address or an I/O device (port) number
- During T2, the processors issue the $\overline{RD}$ or $\overline{WR}$ signal, DEN, and in the case of a write, the data to be written appear on the data bus.

- These events cause the memory or I/O device to begin to perform a read or a write.
- READY is sampled at the end of T_2.
  - if low at this time, T_3 becomes a wait state (T_w)
  - this clocking period is provided to allow the memory time to access data
- If a read bus cycle, the data bus is sampled at the end of T_3.
- Illustrated in Figure 9–11.

Figure 9–11 Minimum mode 8088 bus timing for a read operation.



- In T_4, all bus signals are deactivated in preparation for the next bus cycle
- data bus connections are sampled for data read from memory or I/O

Read Timing

- Figure 9–11 also depicts 8088 read timing.
  - 8086 has 16 rather than eight data bus bits
- Important item in the read timing diagram is time allowed for memory & I/O to read data.
- Memory is chosen by its access time.
  - the fixed amount of time the microprocessor allows it to access data for the read operation
- It is extremely important that memory chosen complies with the limitations of the system.

- The microprocessor timing diagram does not provide a listing for memory access time.
  - necessary to combine several times to arrive at the access time
- Memory access time starts when the address appears on the memory address bus and continues until the microprocessor samples the memory data at T_3.
  - about three T states elapse between these times
- The address does not appear until T_{CLAV} time (110 ns if a 5 MHz clock) after the start of T_1.

- T_{CLAV} time must be subtracted from the three clocking states (600 ns) separating the appearance of the address (T_1) and the sampling of the data (T_3).
- The data setup time (T_{DVCL}), which occurs before T_3 must also be subtracted.
- Memory access time is thus three clocking states minus the sum of T_{CLAV} and T_{DVCL}.
- Because T_{DVCL} is 30 ns with a 5 MHz clock, the allowed memory access time is only 460 ns (access time = 600 ns –110 ns – 30 ns).

Figure 9–12 8088 AC characteristics.

A.C. CHARACTERISTICS (8088: T_A = 0°C to 70°C, V_{CC} = 5V ±10%)* (8088-2: T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

		8088		8088-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	118		68		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

- To find memory access time in this diagram:
  - locate the point in T_3 when data are sampled
  - you will notice a line that extends from the end of T_3 down to the data bus
  - at the end of T_3, the microprocessor samples the data bus.

- Memory devices chosen for connection to the 8086/8088 operating at 5 MHz must be able to access data in less than 460 ns.
  - because of the time delay introduced by the address decoders and buffers in the system
  - a 30- or 40-ns margin should exist for the operation of these circuits
- The memory speed should be no slower than about 420 ns to operate correctly with the 8086/8088 microprocessors.

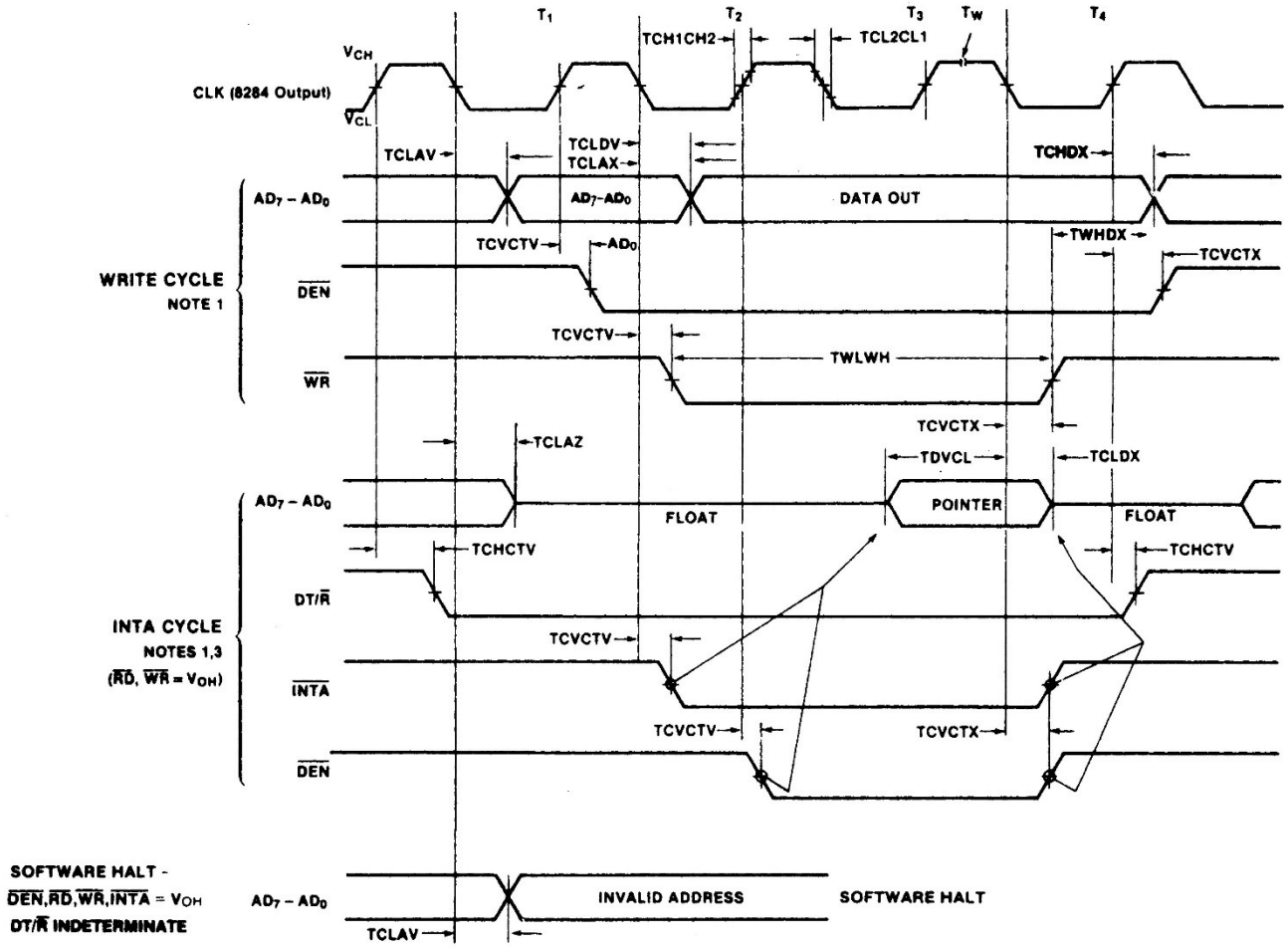
Strobe Width

- The other timing factor to affect memory operation is the width of the $\overline{RD}$ strobe.
- On the timing diagram, the read strobe is given as T_{RLRH}.
- The time for this strobe at a 5 MHz clock rate is 325 ns.
- This is wide enough for almost all memory devices manufactured with an access time of 400 ns or less.

Write Timing

- Figure 9–13 illustrates 8088 write-timing.
  - 8086 is nearly identical
- The $\overline{RD}$ strobe is replaced by the $\overline{WR}$ strobe,
  - the data bus contains information *for* the memory rather than information *from* the memory,
  - D$\overline{T}$/R remains a logic 1 instead of a logic 0 throughout the bus cycle
- When interfacing some devices, timing may be critical between when $\overline{WR}$ becomes logic 1 and the data are removed from the data bus.

Figure 9–13 Minimum mode 8088 write bus timing.



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED

- Memory data are written at the trailing edge of the $\overline{WR}$ strobe.
- On the diagram, this critical period is T_{WHDX} or 88 ns when 8088 on a 5 MHz clock.
- Hold time is often less than this.
  - in fact often 0 ns for memory devices
- The width of the WR strobe is T_{WLWH} or 340 ns with a 5 MHz clock.
- This rate is compatible with most memory devices with access time of 400 ns or less.

SUMMARY

- Both 8086 and 8088 require a single +5.0 V power supply with a tolerance of ±10%.
- The 8086/8088 microprocessors are TTL-compatible if the noise immunity is derated to 350 mV from the customary 400 mV.
- The 8086/8088 microprocessors can drive one 74XX, five 74LSXX, one 74SXX, ten 74ALSXX, and ten 74HCXX unit loads.

SUMMARY (*cont.*)

- The 8284A clock generator provides the system clock (CLK), READY and RESET synchronization.
- The standard 5 MHz 8086/8088 operating frequency is obtained by attaching a 15 MHz crystal to the 8284A clock generator.
- The PCLK output contains a TTL-compatible signal at one half the CLK frequency.

SUMMARY (*cont.*)

- Whenever the 8086/8088 microprocessors are reset, they begin executing software at memory location FFFF0H (FFFF:0000) with the interrupt request pin disabled.
- Because the 8086/8088 buses are multiplexed and most memory and I/O devices aren't, the system must be demultiplexed before interfacing with memory or I/O.

SUMMARY (*cont.*)

- Demultiplexing is accomplished by an 8-bit latch whose clock pulse is obtained from the ALE signal.
- In a large system, the buses must be buffered because the 8086/8088 microprocessors are capable of driving only 10 unit loads, and large systems often have many more.

SUMMARY (*cont.*)

- Bus timing is very important to the remaining chapters in the text. A bus cycle that consists of four clocking periods acts as the basic system timing.
- Each bus cycle is able to read or write data between the microprocessor and the memory or I/O system.

SUMMARY (*cont.*)

- The 8086/8088 microprocessors allow the memory and I/O 460 ns to access data when they are operated with a 5 MHz clock.
- Wait states (Tw) stretch the bus cycle by one or more clocking periods to allow the memory and I/O additional access time.
- Wait states are inserted by control-ling the READY input to the 8086/8088. READY is sampled at the end of T2 and during Tw.

SUMMARY (*cont.*)

- Minimum mode operation is similar to that of the Intel 8085A microprocessor, whereas maximum mode operation is new and specifically designed for the operation of the 8087 arithmetic coprocessor.
- The 8288 bus controller must be used in the maximum mode to provide the control bus signals to the memory and I/O.

SUMMARY

- This is because the maximum mode operation of the 8086/8088 removes some of the system's control signal lines in favor of control signals for the coprocessors.
- The 8288 bus controller reconstructs these removed control signals.

Pin Functions

The following list provides a description of each pin of the 8288 bus controller.

S_2, S_1, and S_0	**Status inputs** are connected to the status output pins on the 8086/8088 microprocessor. These three signals are decoded to generate the timing signals for the system.
CLK	The **clock** input provides internal timing and must be connected to the CLK output pin of the 8284A clock generator.
ALE	The **address latch enable** output is used to demultiplex the address/data bus.
DEN	The **data bus enable** pin controls the bidirectional data bus buffers in the system. Note that this is an active high output pin that is the opposite polarity from the $\overline{\text{DEN}}$ signal found on the microprocessor when operated in the minimum mode.
DT/$\overline{\text{R}}$	The **data transmit/receive** signal is output by the 8288 to control the direction of the bidirectional data bus buffers.
$\overline{\text{AEN}}$	The **address enable** input causes the 8288 to enable the memory control signals.
CEN	The **control enable** input enables the command output pins on the 8288.
IOB	The **I/O bus mode** input selects either the I/O bus mode or system bus mode operation.
$\overline{\text{AIOWC}}$	The **advanced I/O write** is a command output used to provide I/O with an advanced I/O write control signal.
$\overline{\text{IORC}}$	The **I/O read command** output provides I/O with its read control signal.
$\overline{\text{IOWC}}$	The **I/O write command** output provides I/O with its main write signal.
$\overline{\text{AMWT}}$	The **advanced memory write** control pin provides memory with an early or advanced write signal.
$\overline{\text{MWTC}}$	The **memory write** control pin provides memory with its normal write control signal.
$\overline{\text{MRDC}}$	The **memory read** control pin provides memory with a read control signal.
$\overline{\text{INTA}}$	The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.
MCE/$\overline{\text{PDEN}}$	The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.