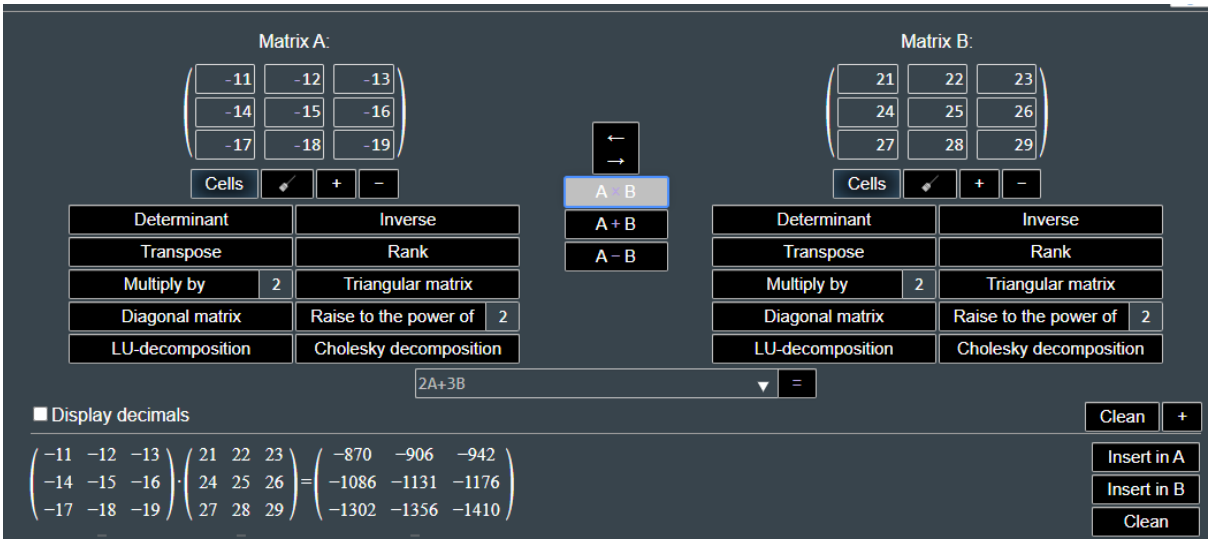
HDL Lab 5 Patrik Vahala 515733

Task 5.1

```c
int main(int argc, char **argv)
{
    mat_a_t in_mat_a[3][3] = {
        {-11, -12, -13},
        {-14, -15, -16},
        {-17, -18, -19}
    };
    mat_b_t in_mat_b[3][3] = {
        {21, 22, 23},
        {24, 25, 26},
        {27, 28, 29}
    };
```

I changed the matrix a's values to be negative. Using matrix calculator I calculated the correct solution:



First I initialized the result, instead of calculating it like so:

```
        result_t sw_result[3][3] = {
                {-870, -906, -942},
                {-1086, -1131, -1176},
                {-1302, -1356, -1410}
        };
       result_t hw_result[3][3];//, sw_result[3][3];
       int err_cnt = 0;

       // Generate the expected result
       // Iterate over the rows of the A matrix
       for(int i = 0; i < MAT_A_ROWS; i++) {
        //  for(int j = 0; j < MAT_B_COLS; j++) {
              // Iterate over the columns of the B matrix
          //   sw_result[i][j] = 0;
             // Do the inner product of a row of A and col of B
            // for(int k = 0; k < MAT_B_ROWS; k++) {
              //  sw_result[i][j] += in_mat_a[i][k] * in_mat_b[k][j];
            // }
          // }
       }
```

Test passing after initializing the result:

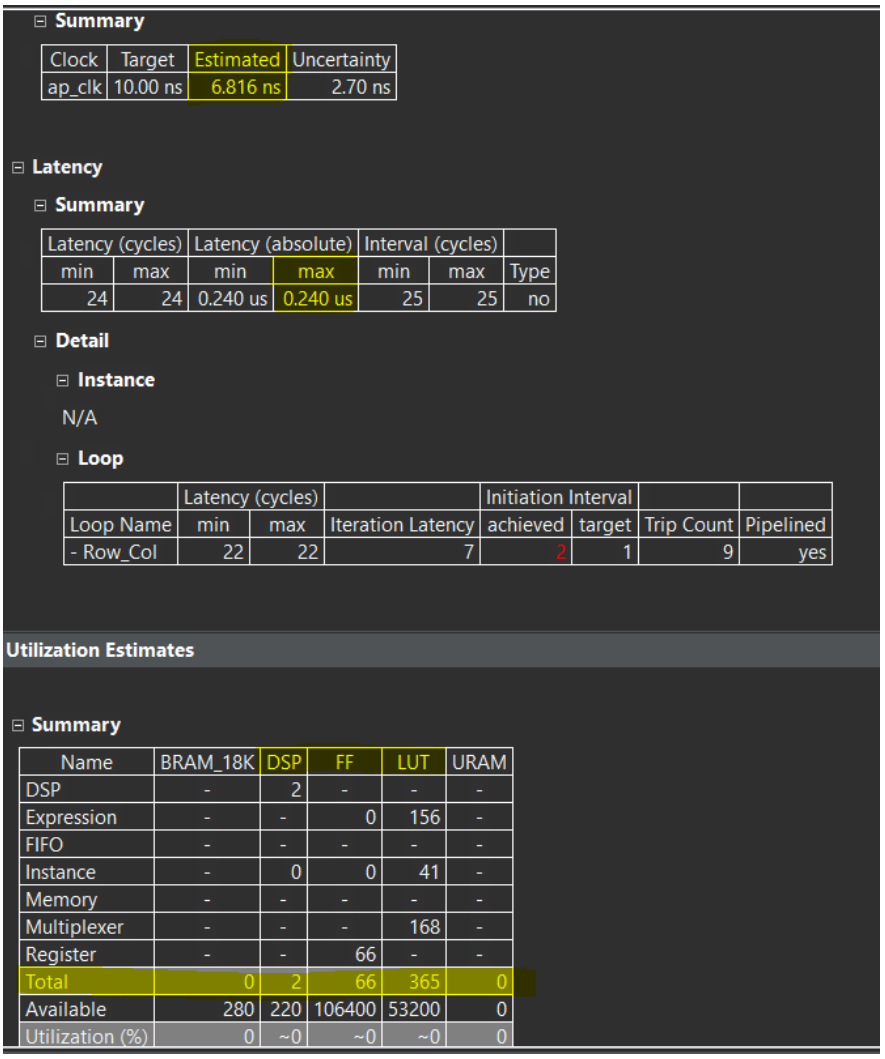
```
Vahala_Patrik_lab5.Debug [C/C++ Application]
{
{-870},{-906},{-942},
{-1086},{-1131},{-1176},
{-1302},{-1356},{-1410},
}
Test passes.
```

Test passing with one error mismatch:

```
<terminated> (exit value: 1) Vahala_Patrik_lab5.Debug [C/C++ Application] csim.exe
ERROR: 1 mismatches detected!
{-870},{-906},{-942},
{-1086},{-1131},{-1176},
{-1302},{-1356},{-1410},
}
Test passes.
```

Task 5.2

✓ Estimated clock period: 6.816ns
✓ Worst case latency: 0.240 us
✓ Number of DSP48E utilized in the implementation: 2
✓ Number of FFs utilized in the implementation: 66
✓ Number of LUTs utilized in the implementation: 365



Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.816 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
24	24	0.240 us	0.240 us	25	25	no

Detail

Instance

N/A

Loop

	Latency (cycles)			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Row_Col	22	22	7	2	1	9	yes

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	2	-	-	-
Expression	-	-	0	156	-
FIFO	-	-	-	-	-
Instance	-	0	0	41	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	168	-
Register	-	-	66	-	-
Total	0	2	66	365	0
Available	280	220	106400	53200	0
Utilization (%)	0	~0	~0	~0	0

Task 5.3

Benefit of working with FPGAs writing code in VHDL is that it allows me to model and simulate the system before it is transferred into a real hardware thus saving time(?) and preventing problems. Drawbacks include i.e. the time it takes to model and simulate instead of just going to work on the hardware straight away. I also realized that I can better understand what's happening with real hardware (leds, switches, etc.) instead of the summary that Vivado gives in waves and states. Automatic VHDL code in Vitis HLS is O.K. readability wise.