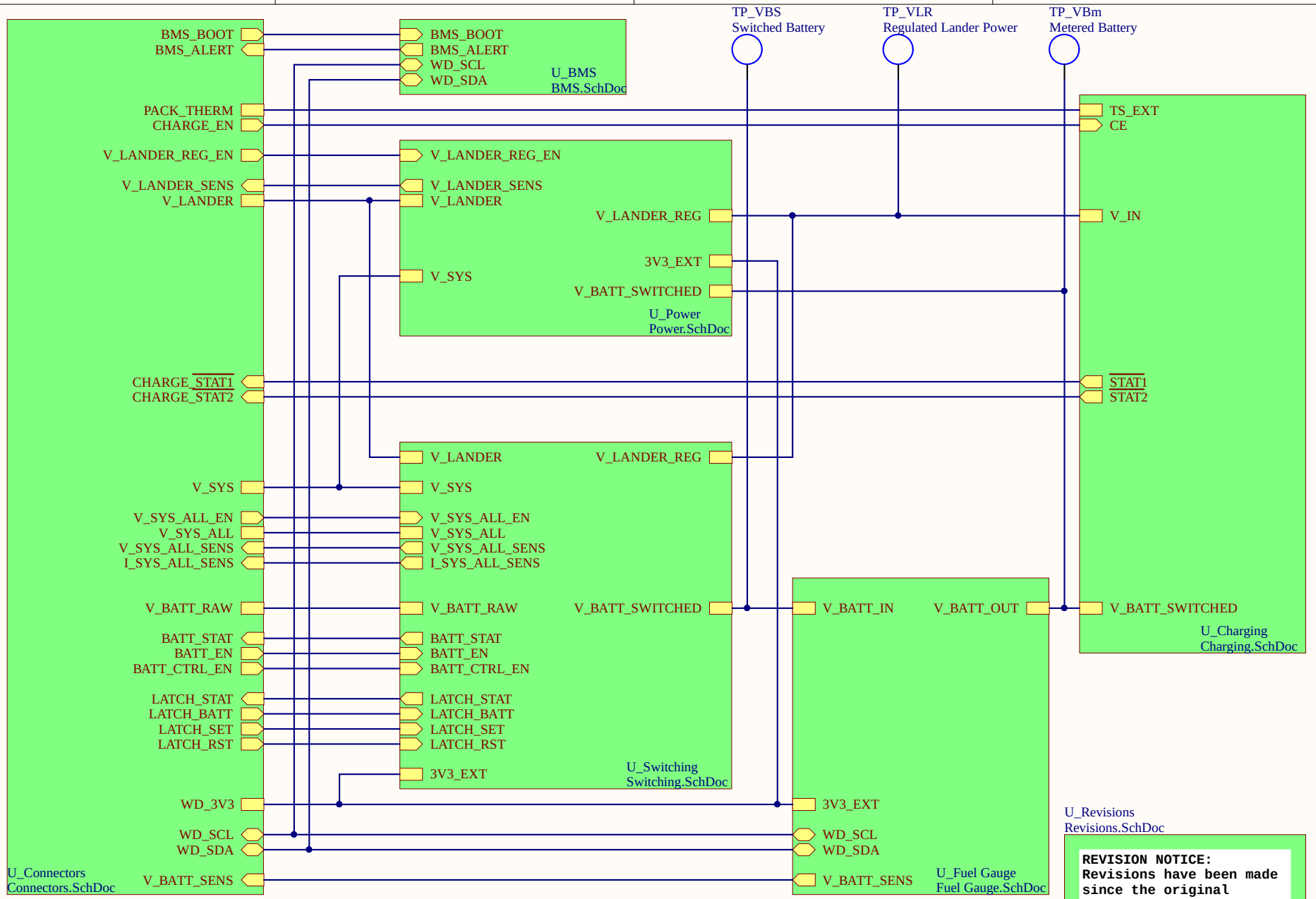
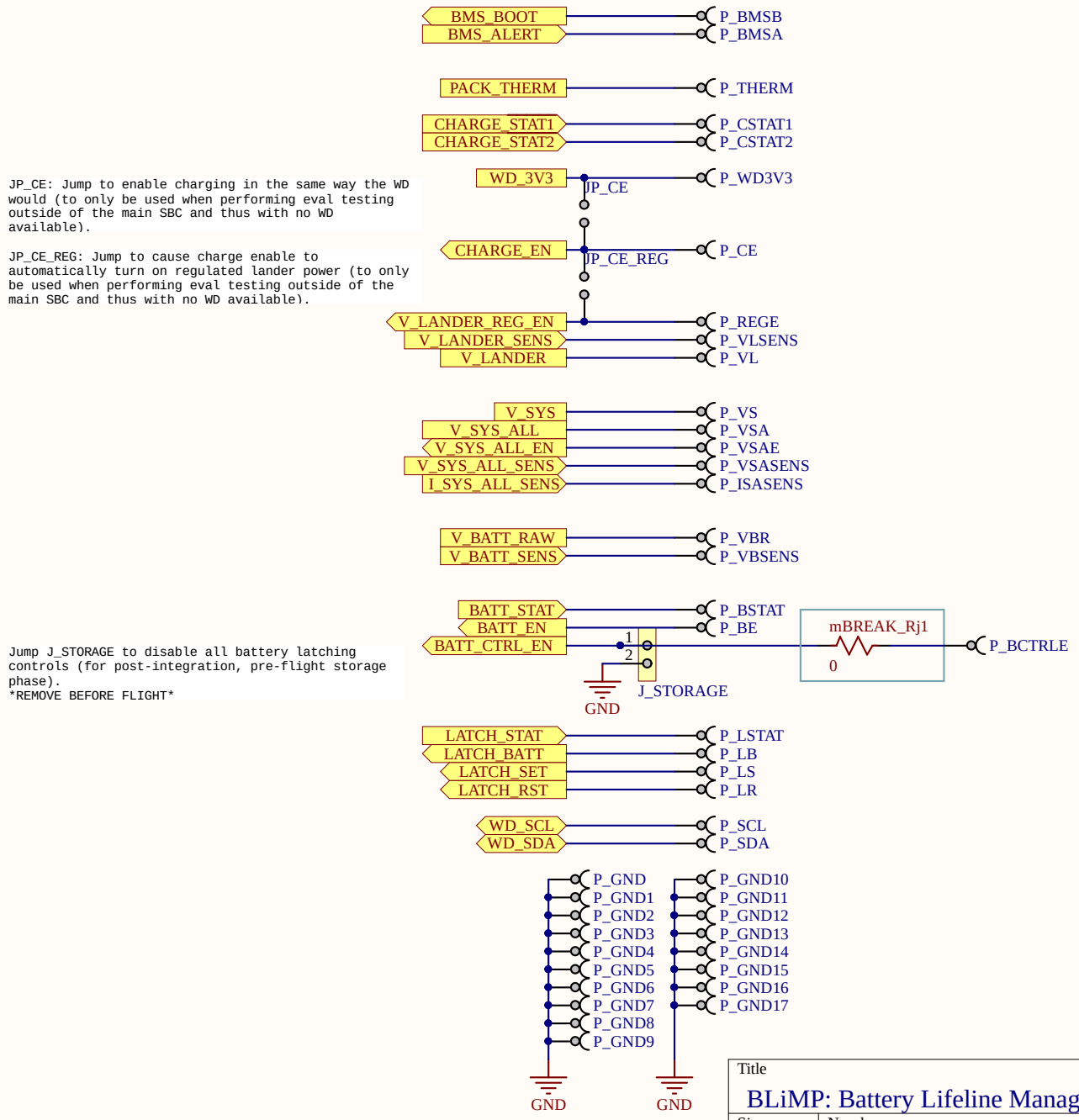



```
A NOTE ON DESIGN PHILOSOPHY:

Since this version of the board will have to:
> Survive launch -possibly with excessive impacts of vibration due to being on a somewhat massive castellated board
> Work in both cislunar space and on the surface of the Moon
All with:
> Possibly with less than ideal amounts of testing on Earth
> Definitely no option for revision

A large number of redundancies and fail safes were included in the design. Specifically, circuits which contribute directly to
the rover's ability to power the board, especially during transit, or latch the batteries were implemented in such a way that
no failure of a single IC - due to radiation or even cracking or separation under launch vibration - could cause the circuit to
fail.
```

Title	BLiMP: Battery Lifeline Management PCB	
Size: A	Number: 1	Revision: 1.0.2f - Manual Mod
Date: 10/28/2021	Sheet 1 of 10	
File: C:\Users\..\Main.SchDoc	Drawn By: Connor W. Colombo	



Title	BLiMP: Battery Lifeline Management PCB – Connectors	
Size: A	Number: 1	Revision: 1.0.2f - Manual Mod
Date: 10/28/2021	Sheet 2 of 10	
File: C:\Users\..\Connectors.SchDoc	Drawn By: Connor W. Colombo	

System Output Power

V_BATT_SWITCHED
Dp5 PDS1040Q
Dp4 PDS1040Q
V_LANDER
Rp29 2M, 1%
Rp28 232k, 0.1%
GND
V_LANDER_SENS

V_LANDER_SENS helps determine if we're attached to the lander and powered.
Full voltage sense range (max rated lander voltage is 1.1*28=30.8V):
3.3 * (232k+2000k)/232k = 31.7V

NOTE:
> This VIN + VBATT -> VSYS architecture comes from the tested charging reference circuit; so any components which mirror those in the reference circuit use the Xc? namespace instead of Xp? like all other components in this sheet in order to be able to be easily cross-referenced with the reference circuit during testing.

V_SYS
V_SYS
Cp18 10uF, 50V, 10%
GND

Charger Power Switching

See Power Note [P0] for SSR resistor selection calculations.

3V3_EXT
This SSR is VERY important (rover dies without warning or knowledge if it dies); so, it has been doubled up for redundancy.

Up1 CS128
Rp2 68k
Rp3 487R, 1%
Qp1A BCR135S
Up3 CS128
Rp4 68k
Rp5 487R, 1%
Qp1B BCR135S
GND
TP_VLS Switched Lander Power

V_LANDER_REG_EN
Note: V_LANDER_REG_EN can safely be tied to CHARGE_EN but should be done so off-board so that the two aren't *required* to be identical.
mCp1 100nF, C0G
GND

Charger Input Regulation

See Power Note [P4] for rationale for V_LANDER_REG regulator.

Bypass Resistor
Bypass resistor to be populated instead of regulator (and supporting components) in the event of an implementation failure with the regulator.
Rp1 [DNP] 0
V_LANDER_REG

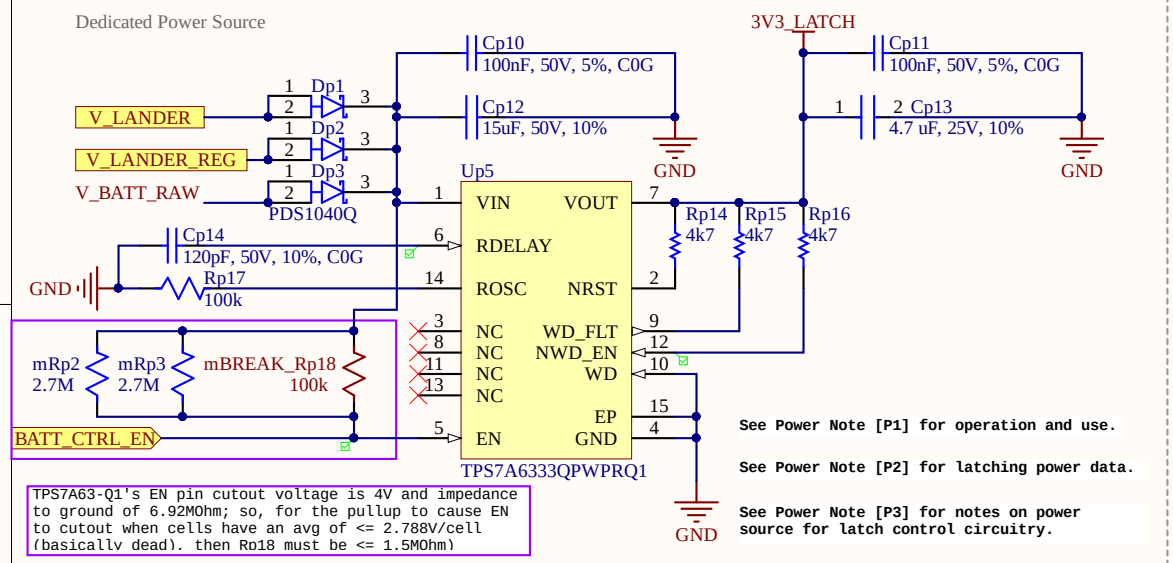
Power Regulator
See Power Note [P5] for inductor criteria.
Lp1 10uH, 37m6Ohm, 10.6A (sat)
Cp1 68nF, 50V, C0G
Cp2 68nF, 50V, C0G
Place near VIN.
Cp3 100nF, 50V, 5%, C0G
Place near PVIN.
Cp4 15uF, 50V, 10%
Up4
BST1 SW1 SW2 BST2
VIN PVIN RUN
PVOUT LDO PLDO
PROG MODE GND PGND PGND FB VC
LTC3114HDHC-1
Cp5 15uF, 50V, 10%
2 Cp6 4.7 uF, 25V, 10%
Place near PLDO.
Rp6 0
2 Cp7 33nF, 50V, C0G
Rp8 27k, 5%
Rp7 2M, 1%, 0805
Cp8 10nF, 50V, 5%, C0G
Rp9 75k, 1%
Cp9 10pF, 50V, 5%, C0G
Rp13 45k3, 1%
Rp10 0
Rp11 [DNP] 0
Rp12 [DNP] 0
3V3_EXT
GND

See Power Note [P6] for IC configuration info.

Title: BLiMP: Battery Lifeline Management PCB – Power		
Size: A	Number: 1	Revision: 1.0.2f - Manual Mod
Date: 10/28/2021		Sheet 3 of 10
File: C:\Users\..\Power.SchDoc		Drawn By: Connor W. Colombo

Battery Switching and Latching

Dedicated Power Source



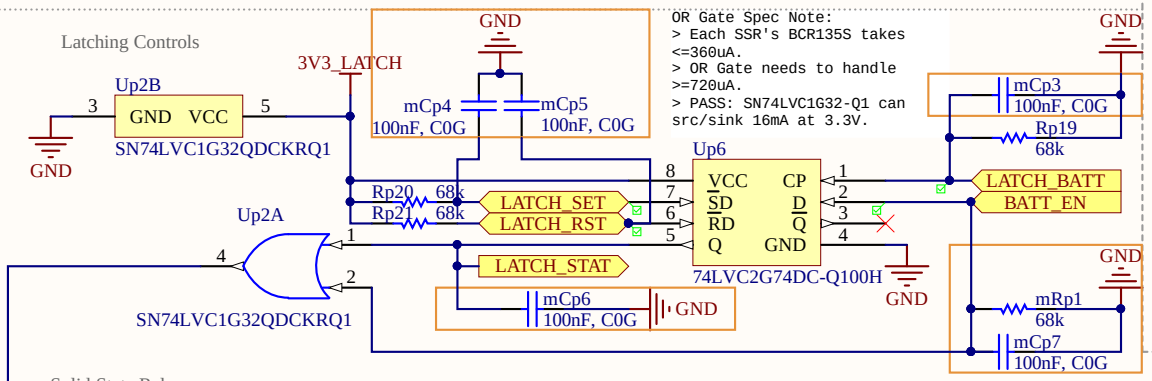
TPS7A63-Q1's EN pin cutout voltage is 4V and impedance to ground of 6.92MOhm; so, for the pullup to cause EN to cutout when cells have an avg of <= 2.788V/cell (basically dead), then Rp18 must be <= 1.5MOhm)

See Power Note [P1] for operation and use.

See Power Note [P2] for latching power data.

See Power Note [P3] for notes on power source for latch control circuitry.

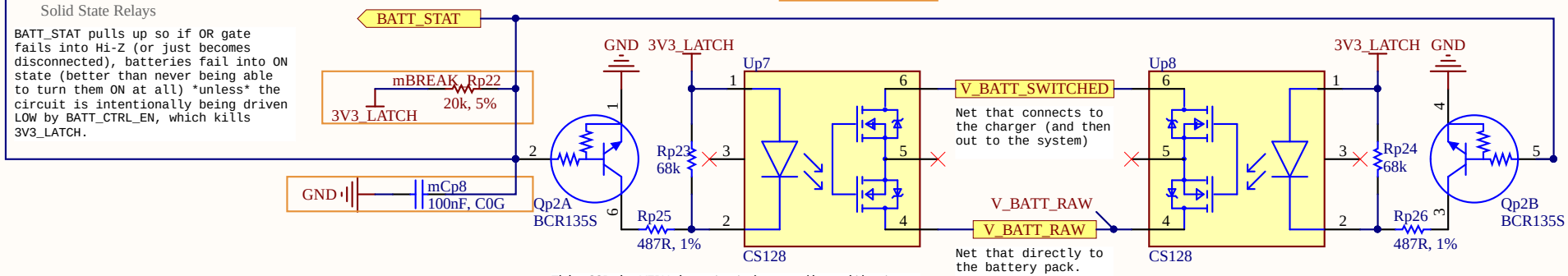
Latching Controls



OR Gate Spec Note:
> Each SSR's BCR135S takes <=360uA.
> OR Gate needs to handle >=720uA.
> PASS: SN74LVC1G32-Q1 can src/sink 16mA at 3.3V.

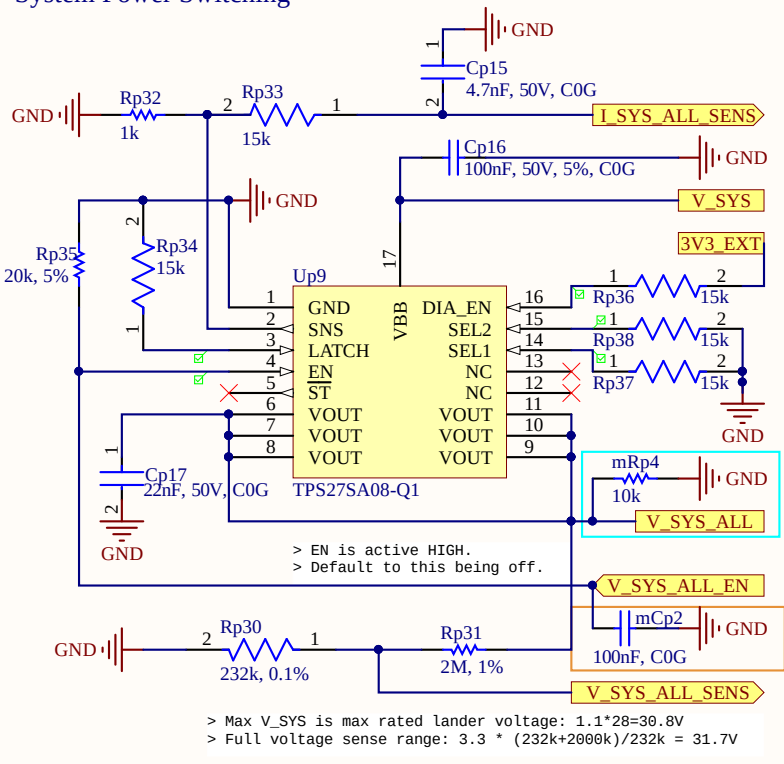
Solid State Relays

BATT_STAT pulls up so if OR gate fails into Hi-Z (or just becomes disconnected), batteries fail into ON state (better than never being able to turn them ON at all) *unless* the circuit is intentionally being driven LOW by BATT_CTRL_EN, which kills 3V3_LATCH.



This SSR is VERY important (rover dies without warning or knowledge if it dies); so, it has been doubled up for redundancy. Also allows for higher nominal current draw. Backup part: AQV252G2SX

System Power Switching



> EN is active HIGH.
> Default to this being off.

> Max V_SYS is max rated lander voltage: 1.1*28=30.8V
> Full voltage sense range: 3.3 * (232k+2000k)/232k = 31.7V

NOTE:
I_SYS_ALL_SENS reflects output current during nominal operations but also serves to as a fault indicator. See datasheet for specifics.

Configuration Note:
(from Table 9-2 in datasheet)
DIA_EN = H & SEL1 = L & SEL2 = L
-> ST = HiZ & SNS = Load Current

Title: BLiMP: Battery Lifeline Management PCB– Power (Switching)		
Size: A	Number: 1	Revision: 1.0.2f - Manual Mod
Date: 10/28/2021	Sheet 4 of 10	
File: C:\Users\..\Switching.SchDoc	Drawn By: Connor W. Colombo	

[P0] SOLID STATE RELAY RESISTOR SELECTION:

3V3_MIN = 3.267V
3V3_MAX = 3.333V

> CS128:
IF_ON_MAX = 3.0mA
IF_MAX_RATED = 50mA
VF_MIN = 1.0V
VF_MAX = 1.5V

> BCR135: VCE(sat) = 0.3V

> LED Resistor Selection:
R_LED = (V_LANDER_MIN - VCE - VF_MAX)/IF_ON_MAX = 489Ohm
-round-down-to-E96-> R = 487Ohm

> Maximum LED Current:
I_NOM = (V_LANDER_MAX - VF_MIN)/R_LED = 4.8mA
PASS: I_NOM < I_MAX_RATED

[P1] BATTERY CONTROL:

> Make sure BATT_CTRL_EN is HiZ or HIGH to enable the battery controller circuit (3V3_LATCH). Note: this line has an external HW pull up to the regulator's V_IN so HiZ is preferred.

> Set EN_BATT high to connect batteries.

> To latch batteries (and make state persistent even in the event of a WD fault), set EN_BATT to the desired state then wait for 1/fmax_min = 1/175MHz = 6ns then pulse LATCH_BATT high for 1/fmax_min = 6ns then low to save the state. Note: default (e.g. init) state of LATCH_BATT should be LOW or Hi-Z (since it has a HW pull-down).

> The latch power is secured by its own small high efficiency 3V3 regulator which ensures latch is always powered invariant to the state of the rest of the system.

> Note: For safety reasons (so the WD doesn't accidentally reset it on the surface if there's a persistent memory fault), WD should *always* boot with BATT_CTRL_EN as Hi-Z and only set it LOW (to reduce power draw from lander) by a command and *not* save this state persistently. Any time WD reboots, BATT_CTRL_EN should go Hi-Z or HIGH.

> Note: To charge batteries, BATT_CTRL_EN and EN_BATT should both be HIGH.

> Note: For redundancy, latch output (LATCH_STAT) and standard enable signal (EN_BATT) are OR-gated so even if there's a latch fault, the batteries can still be connected, they'll just no longer stay connected in the even of a WD reset which lasts longer than its supply's discharge time.

> Note: The power-up latch state is indeterminate; so, the WD must check LATCH_STAT and make sure its OFF upon booting into KeepAlive UNLESS it's already deployed (in which case it should make sure the LATCH is enabled). Persistent memory in the WD should be used to determine whether the rover has been deployed.

> Note: LATCH_SET and LATCH_RST are used to force LATCH_STAT HIGH or LOW respectively. These are manual overrides for use in case there is an issue with the normal data/clock latching. In nominal operation, these should remain unused (and pulled HIGH)

[P2] BATTERY CONTROL (LATCHING CIRCUIT) POWER DRAW:

3V3_LATCH Power Draw ON State:
> 2x BCR135S + SSR LED Drive Max Current: 5.4511mA
> D Latch Quiescent Current: 4uA
> D Latch Current Draw per High Input (DICC): 4*500uA
> D Latch Input Leakage: 4 * 1uA
> OR Gate Sink + OFF Current (ICCmax): 10uA + 2*5uA
> OR Gate Current Draw per High Input (DICC): 2*500uA
> LE Pull-down Max: 3V3_MAX/68k=49uA
> nOE Pull-down Max: 3V3_MAX/68k=49uA
> BATT_STAT Pull-up Max (OFF): 3V3_MAX/19k=167uA

> Min. Required 3V3_LATCH Supply Current: 14.1952mA

3V3_LATCH Max Power Draw OFF State:
> 2x BCR135S + SSR LED Leakage Current: 67nA
> D Latch Quiescent Current: 4uA
> D Latch Current Draw per High Input (DICC): 2*500uA
> D Latch Input Leakage: 2 * 1uA
> OR Gate Sink + OFF Current (ICCmax): 10uA + 2*5uA
> OR Gate Current Draw per High Input (DICC): 0*500uA
> LE Pull-down Max: 3V3_MAX/68k=49uA
> nOE Pull-down Max: 3V3_MAX/68k=49uA
> BATT_STAT Pull-up Max (OFF): 3V3_MAX/19k=167uA

> Total OFF State Current Draw: I_OFF = 1.2911mA
> 3V3_LATCH Reg. Input Quiescent Current Power:
I_Q_MAX = f_therm * I_Q_MAX_NOM = <1.2*<271uA = <326uA
P_Q = V_BATT_MAX * I_Q_MAX = 25.2V * 326uA = <8.2152mW
> 3V3_LATCH Regulator Efficiency:
eff_min = I_OUT/(I_OUT+I_Q) * 3V3_MAX/V_BATT_MAX
eff_min = 0.126
> Total OFF State Power Draw from 3V3:
P_3V3_OFF = 1/eff_min * 3V3_MAX * I_OFF + P_Q = 42.7mW
* Note: this is a gross overestimate (maximum upperbound) due to the uncertainties in the actual value of DICC. As such, this should be measured once a BLiMP is fabricated.

Total STORAGE State Battery Drain:
> This is with the J_STORAGE jumper installed, putting the 3V3_LATCH regulator into sleep mode
> 3V3_LATCH Regulator Sleep Current: I_SLEEP_IN <= 3uA
> 2x SSR Output Leakage Current: I_L_SSR_OUT = <1uA

> Expected STORAGE State Battery Current:
I_BATT_STORE = I_SLEEP_IN + 2 * I_L_SSR_OUT = 5uA
> Total OFF State Power Draw from Batteries:
P_BATT_STORE_MAX = I_BATT_STORE * V_BATT_MAX = 129uW
> Min. Battery Life in STORAGE State (post-integration, pre-launch):
T_L_STORAGE_MIN = C_BATT_MIN / I_BATT_STORE
-> T_L_STORAGE_MIN = 3400mAh / 5uA = 680khrs = 77yrs
> PASS: T_L_STORAGE_MIN > 2*T_STORAGE_MAX = 2yrs

Total OFF State Battery Drain (with 3V3_LATCH powered by lander):
> 2x SSR Output Leakage Current: I_L_SSR_OUT = <1uA

> Expected OFF State Battery Current:
I_BATT_OFF = 2 * I_L_SSR_OUT = 2uA
> Total OFF State Power Draw from Batteries:
P_BATT_OFF_MAX = I_BATT_OFF * V_BATT_MAX = 51.6uW
> Min. Battery Life in OFF State (Transit):
T_L_TRANSIT_MIN = f_therm * C_BATT_MIN / I_BATT_OFF
-> T_L_TRANSIT_MIN = 0.7 * 3400mAh / 2uA = 1.19Mhrs = 135yrs
> PASS: T_L_TRANSIT_MIN > 2*T_TRANSIT_MAX = 72days

NOTE: BCR135S + SSR LED Current Draw Sim:
https://www.multisim.com/content/t3mSdGk5SAxd7oeVEhDnKQ/ssr-current-draw/open/

[P3] POWER SOURCES FOR 3V3_LATCH:

Three power sources are connected to the 3V3_LATCH regulator via Schottky diodes because:

> After deployment the latching hardware needs to be powered directly by the battery pack (V_BATT_RAW).

> To avoid draining the batteries during transit, V_LANDER is attached.

> But, since V_LANDER can hypothetically drop 10% to 25.2V, current could still be drawn from the batteries; so, V_LANDER_REG (28V) is attached.

> V_LANDER is still used in addition to V_LANDER_REG (instead of *just* using V_LANDER_REG and V_BATT_RAW) so that we'll still be able to latch the batteries in the event of a 28V regulator failure.

NOTE:
> This setup is used to make the rover's battery control circuitry as fault-tolerant as possible.

> The P_3V3_OFF<<=42.7mW this requires from the lander will allow the rover to safely keep the batteries completely detached during transit.

> The implication of this setup is that even if the batteries are latched off, P_3V3_OFF<<=42.7mW will be drawn from whichever of these power sources has the highest voltage. In transit, that will be the lander; however, it should be noted that, in the pre-flight STORAGE phase, if the lander is not supplying power, P_3V3_OFF will be draw from the batteries by default, meaning the rover will have a default pre-flight storage lifetime of:
T_L_STORAGE = E_BATT / P_3V3_OFF = 77Wh / 42.7mW = 1800hrs = 75days.
* Note: because P_3V3_OFF is a gross overestimate, this is very much a minimum lifetime.

>> Since battery control is not needed during pre-flight storage, this level of drain from the batteries during STORAGE can be prevented by adding a "REMOVE BEFORE FLIGHT" storage jumper (J_STORAGE) which should be routed to the outside of the rover chassis and removed at the last possible moment before flight.

>> To prevent even P_3V3_OFF<<=42.7mW from being drawn from the lander during transit (in the event that all possible power must be diverted to heaters), BATT_CTRL_EN can be driven LOW to disable all battery latch controls (just completely disconnect the batteries). In this case, only I_BATT_STORE=4uA will drawn from the lander, equalling <=5uA*30.8V=154uW.

[P4] NEED FOR INPUT POWER REGULATOR:

> Lander power is 28V +- 10% = [25.2V, 30.8V]

> Charging IC enters CV phase at VBAT = 25.2V +- 0.202V

> Charging IC will go into sleep mode if its VCC (lander power) is < 150mV greater than the V_BAT (i.e. if VCC-VBAT < 150mV).

> So, V_LANDER always needs to be 150mV > than V_BATT in order to allow the CV phase to happen. So, the upper bound for the min required lander voltage is VBAT + dVBATp + 0.150V = 25.55V.

> So, the window for the possible supplied lander voltages dips down to 25.2V, 0.35V below the highest possible value for the charging IC's minimum required voltage to charge (25.5V), meaning the charger might enter sleep mode due to low supply voltage before it gets to enter the final (CV) charging step.

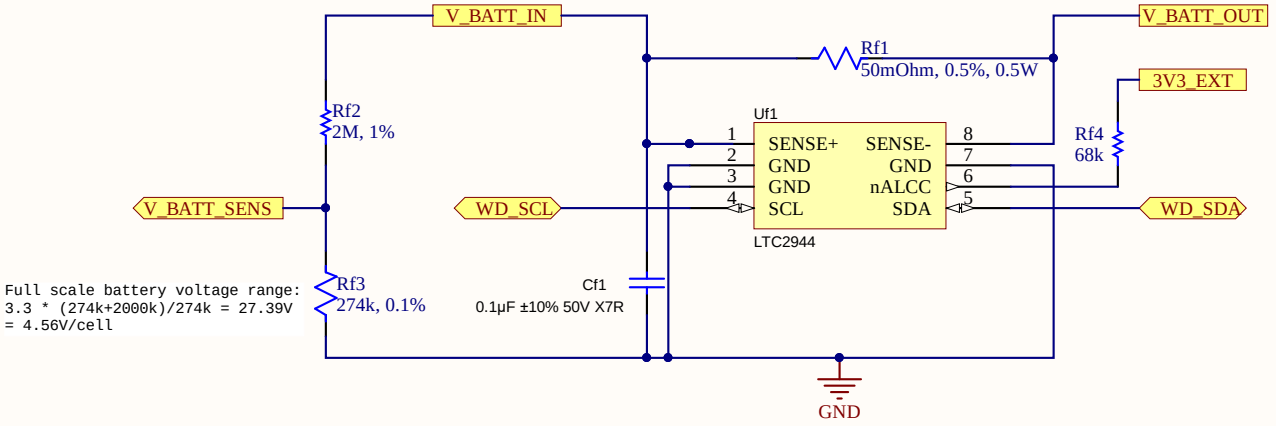
> Also, V_LANDER_MAX = 30.8V and, although the absolute maximum rating (in air) for VCC on the charging IC is 33V, the recommended maximum is 28V. It's likely that above this 28V recommended maximum increased power loss and heating in the IC will occur.

[P5] CHARGER INPUT REGULATION INDUCTOR SELECTION:
> Must have low DCR.
> 10uH was chosen since this circuit will operate as both a shallow boost and shallow buck converter. 10uH is in the middle of the 4.7uH-15uH range given in the datasheet where boost circuits favor the lower end and buck circuits favor the higher end.
> Peak-to-peak ripple current:
DIPP_BUCK = VOUT/L * (VIN_MAX-VOUT)/VIN_MAX * (1/1.2MHz-0.05us)
-> DIPP_BUCK = 28V/10uH * (30.8V-28V)/30.8V * 0.7833us = 0.199A
DIPP_BST = VIN_MIN/L * (VOUT-VIN_MIN)/VOUT * (1/1.2MHz-0.05us)
-> DIPP_BST = 25.2V/10uH * (28-25.2)/28 * 0.7833us = 0.197A
> Inductor Saturation Current for I_SRC_MAX = 3W/28V = 0.107A:
I_SAT > I_SRC_MAX + 1/2*max(DIPP_BUCK,DIPP_BST) = 207mA

[P6] CHARGER INPUT REGULATION IC CONFIGURATION:

> MODE = GND -> High eff. mode switching from burst to PWM mode. Connect to 3V3 to keep in PWM.
> RUN = VIN -> Keep on. Connect to GND to disable.
> C_OUT = 15uF (already specced and >10uF).
> R_VC_Z = (0.42/3)*29kHz*VOUT*2*pi*C_OUT/(1.97A/V*120uS)=45.3k
> R_PROG: I_LIM_TARG = 0.9A = 25000*1V/R_PROG_TARG
-> R_PROG_TARG = 27.7k -common-> R_PROG=27k -> I_LIM=0.93A.
> R_LOAD_EQ_MIN = VOUT/I_LIM = 30.10hm
> C_VC_P1 = R_LOAD_EQ_MIN*C_OUT/R_VC_Z = 9.96nF -> 10nF
> C_VC_P2 = 10pF (standard)
> C_PROG >= 3*C_VC_P1 -> 33nF
> R_FP_TOP = 2MOhm (arbitrary)
> R_FP_BOT = R_FP_TOP * 1V / (VOUT - 1V) = 74.1k -> 75k
> Therefore, VOUT = 1V*(R_FP_TOP+R_FP_BOT)/R_FP_BOT = 27.67V

Title	BLiMP: Battery Lifeline Management PCB – Power Notes	
Size: A	Number: 1	Revision: 1.0.2f - Manual Mod
Date: 10/28/2021	Sheet 5 of 10	
File: C:\Users\..\Power_Notes.SchDoc	Drawn By: Connor W. Colombo	



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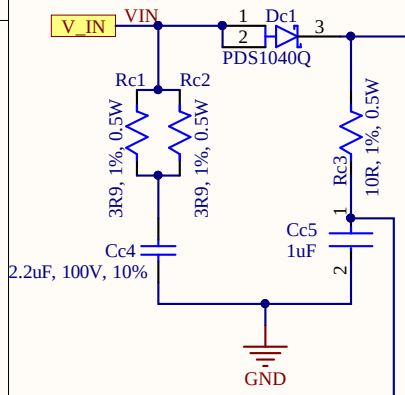
Size: A	Number: 1	Revision: 1.0.2f - Manual Mod	
Date: 10/28/2021		Sheet 6 of 10	
File: C:\Users\..\Fuel Gauge.SchDoc		Drawn By: Connor W. Colombo	

Input Power

Input Filter (Damping RC Network)

This input filter is to prevent voltage spikes caused by parasitic inductance and capacitance upon boot up, which is unlikely since we're using a regulator; however, we're including the option to bypass that, so this filter should remain in place.

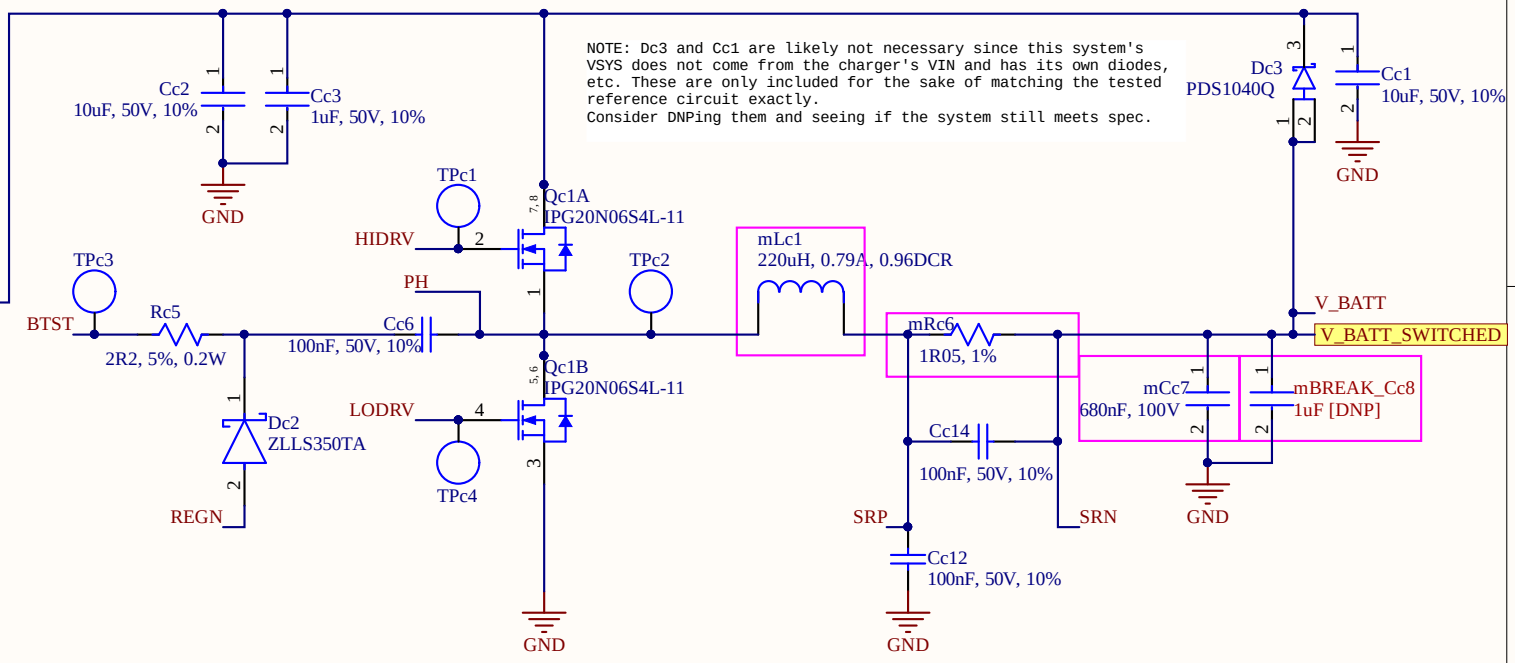
Place close to charging IC's VCC.



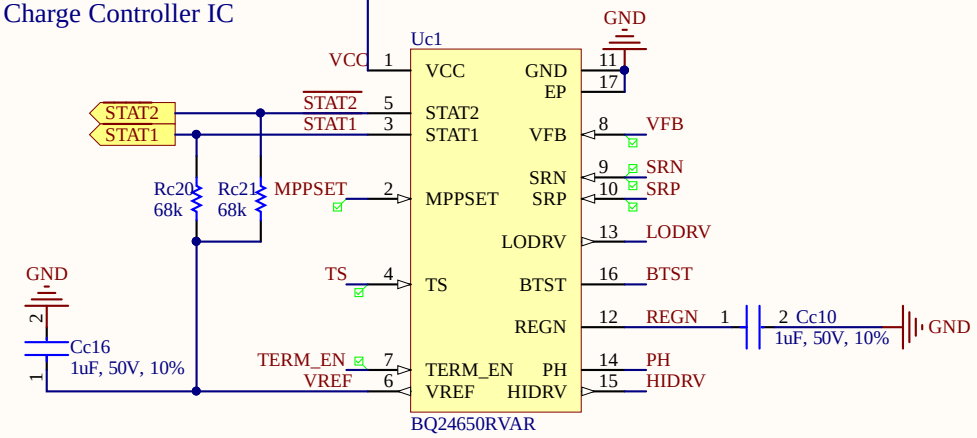
Charging Pathway

See General Notes [N2] and [N3] for important notices about DNP (red boxed) components.

NOTE: Dc3 and Cc1 are likely not necessary since this system's VSYS does not come from the charger's VIN and has its own diodes, etc. These are only included for the sake of matching the tested reference circuit exactly.
Consider DNPing them and seeing if the system still meets spec.

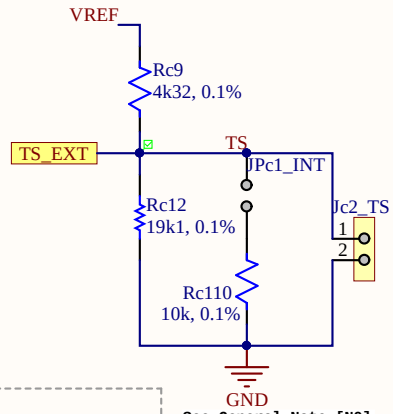


Charge Controller IC



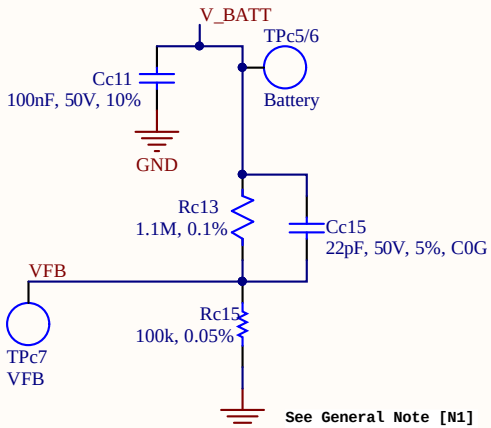
State Sensing

Battery Pack Temperature



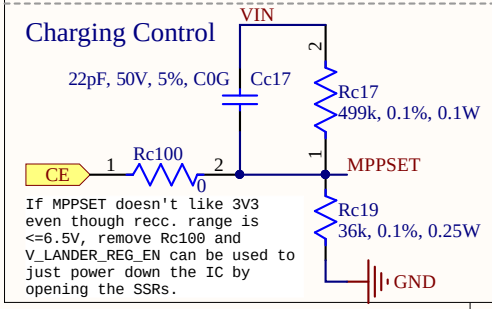
See General Note [N0] for thermisitor input resistor calculations.

Output (Pack) Voltage



See General Note [N1] for VFB input resistor calculations.

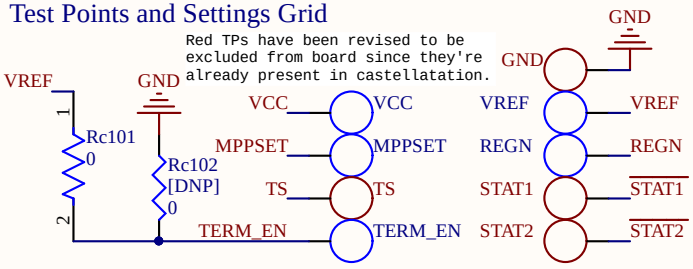
Charging Control



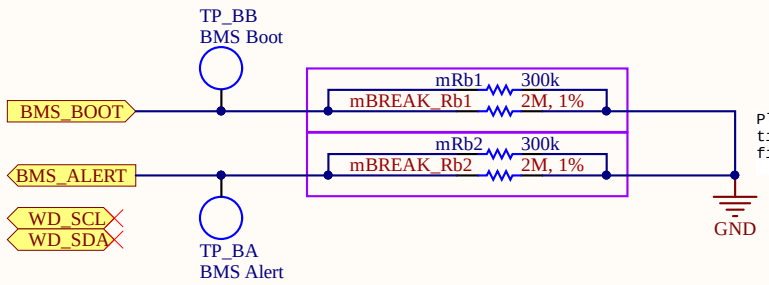
If MPPSET doesn't like 3V3 even though recc. range is <=6.5V, remove Rc100 and V_LANDER_REG_EN can be used to just power down the IC by opening the SSRs.

Test Points and Settings Grid

Red TPs have been revised to be excluded from board since they're already present in castellatation.



Title	BLiMP: Battery Lifeline Management PCB – Charging		
Size: A	Number: 1	Revision: 1.0.2f - Manual Mod	
Date: 10/28/2021		Sheet 7 of 10	
File: C:\Users\..\Charging.SchDoc		Drawn By: Connor W. Colombo	



Placeholder pins. Real BMS circuit will be added if time permits. Board footprint and pinout needed to be finalized before this could be decided.

Title	BLiMP: Battery Lifeline Management PCB – BMS		
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[N0] THERMISTOR DIVIDER SELECTION:

From Battery Cell Datasheet:
> Min Charging Temp: TCMIN = 0℃
> Max Charging Temp: TCMAX = 45℃

From BQ24650 Charging IC Datasheet:
> On-board Reference Voltage:
V_VREF = 3.267V : 3.3V : 3.333V
> Low Temperature Rising Threshold:
V_LTF = V_VREF*(72.5%:73.5%:74.5%) = 2.37V : 2.43V : 2.48V
> Cut-Off Temperature Threshold:
V_TCO = V_VREF*(44.3%:45%:45.7%) = 1.45V : 1.49V : 1.52V

Thermistor Data (B57863S0103F040)
> Nominal Resistance (at 25C): R_TH_NOM = R25 = 10.000k
> No. of R/T Characteristic: 8016
> B(25/100) = ln(R25/R100)/(1/(25+273) - 1/(100+273)) = 3988K
> Temperature Tolerance (code: F): ±0.2K

> R_TH_COLD = R_TH(TCMIN):
>> RT/R25(TCMIN=0℃) = 3.265
>> ∝(TCMIN=0℃) 1/R[∂R/∂T] = 5.1 %/K
>> -> R_TH_COLD = R_TH(TCMIN) = 32.65k

> R_TH_HOT = R_TH(TCMAX):
>> RT/R25(TCMAX=45℃) = 0.4369
>> ∝(TCMIN=45℃) 1/R[∂R/∂T] = 3.9 %/K
>> -> R_TH_HOT = R_TH(TCMAX) = 4.369k

TS Voltage Divider:
> Rc12 = R_BOT = V_VREF*R_TH_COLD*R_TH_HOT*(1/V_LTF-1/V_TCO) / (R_TH_HOT*(V_VREF/V_TCO-1) - R_TH_COLD*(V_VREF/V_LTF-1))
-> Rc12 = 18.18k : 19.11k : 20.16k
> Rc9 = R_TOP = (V_VREF/V_LTF-1)/(1/R_BOT + 1/R_TH_COLD)
-> Rc9 = 4.429k : 4.346k : 4.267k

Choose:
> Rc12 = R_BOT = 19.1k +- 0.1%
> Rc9 = R_TOP = 4.32k +- 0.1%

Forward Calculate Real Range:
> Cold threshold:
>> R_TH_COLD = -(R_TOP*R_BOT*V_LTF)/(R_TOP*V_LTF + R_BOT*V_LTF - R_BOT*V_VREF)
-> R_TH_COLD = 28.21k : 32.15k : 37.21k
>> R_TH_COLD/R25 = 2.821 : 3.215 : 3.721
>> T_COLD = 3.057℃ : 0.3437℃ : -2.357℃

> Hot threshold:
>> R_TH_HOT = -(R_TOP*R_BOT*V_TCO)/(R_TOP*V_TCO + R_BOT*V_TCO - R_BOT*V_VREF)
-> R_TH_HOT = 4.190k : 4.337k : 4.491k
>> R_TH_HOT/R25 = 0.4189 : 0.4337 : 0.4491
>> T_HOT = 46.17℃ : 45.21℃ : 44.37℃

[N1] VFB BATTERY VOLTAGE DIVIDER SELECTION:

6 cells/pack
> BMS Balance: VBAL = 4.125V/cell
> BMS Overcharge: VOC = 4.25±0.025V/cell
> Overvoltage Shutoff: VOV = 1.04*VBAT
> Charge Regulation: VREG = 2.1V
> Charge Accuracy (-40C to 125C): rVC = ±0.7%

Target:
> Cell voltage: VC = 4.2V/cell
> Pack voltage: VBAT = 6*VC = 25.2V
> Pack voltage tolerance:
6*(4.25V-0.0125V-4.2V) = dVBAT = ± 0.2022V

Actual:
> Pack voltage: VBAT = 2.1*(1+R13/R15) = 25.2V
> Cell voltage: VC = VBAT/6 = 4.2V/cell
> Pack voltage tolerance:
dVBAT_div = sqrt(VREG^2*R13^2/R15^4*dR15^2 + VREG^2/R15^2*dR13^2) = 0.0258V
dVBAT = +[(1+rVC)*(VBAT + dVBAT_div) - VBAT]
- [VBAT - (1-rVC)*(VBAT + dVBAT_div)]
-> dVBAT = +0.2024V/-0.2020V
(good out to 1mV)

> Max. Battery Output Capacitance:
CMAX = 2 * 6mA * 1s / (1+R13R15) = 1000uF

[N2] CHARGING CIRCUIT DNP NOTICE:
> Lc1, Rc6, Cc7, Cc8 (and possibly Cc5) are marked DNP and boxed in red because they either contribute to detemining or are determined by the charging current, which is TBD at the time of drawing.
> DNP in this context means that the PCBA fab *should not* populate these components and they will instead be populated in the test lab after fabrication.
> An array of these components of varying values will be ordered after this board for later population.
> Note: In application, this circuit should only source around 1W -> 50mA max. but has been designed to handle up to 1A.

[N3] IMPORTANT NOTE ON CHARGING CIRCUIT DNP COMPONENT VALUES:
> Values given are those for these components are those which were used in the TI BQ24650EVM eval board, which charges at 2A. They are provided for the purposes of cross-referencing only.
> DO NOT UNDER ANY CIRCUMSTANCE populate the board with these reference values since they will cause the circuit to draw up to 2A from the regulated supply which only sources 1.2A max.

NOTE:
Optimal values for these components can be determined using a BQ24650 calculator provided by TI in SLUC175D, available at:
https://www.ti.com/product/BQ24650#tech-docs
(make sure to navigate to the proper "bq24650" sheet in the downloaded SLUC175D excel file).

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v1.0.2b REVISION NOTICE:
This revision (v1.0.2b) represents a change with respect to v1.0.2 which was fabricated. All changes in v1.0.2b must therefore be manually added to the board. All such components which must be added manually have their designators prefixed with a lower-case 'm'. Likewise, any net breaks (open jumpers) which must be added or components which must be removed are prefixed with 'mBREAK' and any new connections which must be made are to be added using a 0-Ohm resistor prefixed with 'mPATCH'. All changes are boxed in orange.

v1.0.2c REVISION NOTICE:
Revision 1.0.2c is a change with respect to v1.0.2b described above. A new component value was changed (Rp18) as indicated by a component removal (mBREAK_...) and addition (m...). Also two components (Rb1 and Rb2) had minor (inconsequential) value changes. All changes are boxed in purple.

v1.0.2d REVISION NOTICE:
Revision 1.0.2d is a change with respect to v1.0.2c described above. A new component was added to prevent VSA from floating when switched off. All component changes are boxed in cyan. Also V_BATT ports were renamed to V_BATT_SWITCHED to clarify their function.

v1.0.2e REVISION NOTICE:
Revision 1.0.2e is a change with respect to v1.0.2d described above. Originally unpopulated configuration components for the charging IC have been specified and added. These are the components that have been boxed in red in previous revisions and are now boxed in pink. See "Power Analysis and BLiMP Charger Calculations" in Avionics/SBC/Iris Rev I in the Iris Team Google Drive for the supporting calculations for the changes. These changes configure the board to target a charging current of 0.039A into the batteries. Testing indicates this requires 3.9W from the lander supply at 28V during charging.

v1.0.2f REVISION NOTICE:
Revision 1.0.2f is a change with respect to v1.0.2e described above. A safety modification (line break) was made to prevent VIN on the 3V3_LATCH supply from being connected via Rp18 to the Watchdog's BCTRLE pin via 1.35MOhm resistance when the pin is in a High-Z state as an input or when the WD is simply unpowered.

Alternatively the WD BCTRLE pin can be connected to the BLiMP BCTRLE pin via a 383kOhm resistor in series with a 155kOhm (+- 10kOhm) pull down resistor on the WD side to keep the two connected while also protecting the WD from voltages above 3.3V and allowing the EN pin on the 3V3_LATCH regulator to stay above its ON threshold of 4V when WD BCTRLE is High-Z. The only problem with this approach is that setting the WD pin to LOW won't turn off BCTRLE until after the VIN voltage drops below 18.87V (i.e. no lander voltage input and batteries depleted to 3.14V/cell). So, not very useful.

Title	BLiMP: Battery Lifeline Management PCB – Revision Log		
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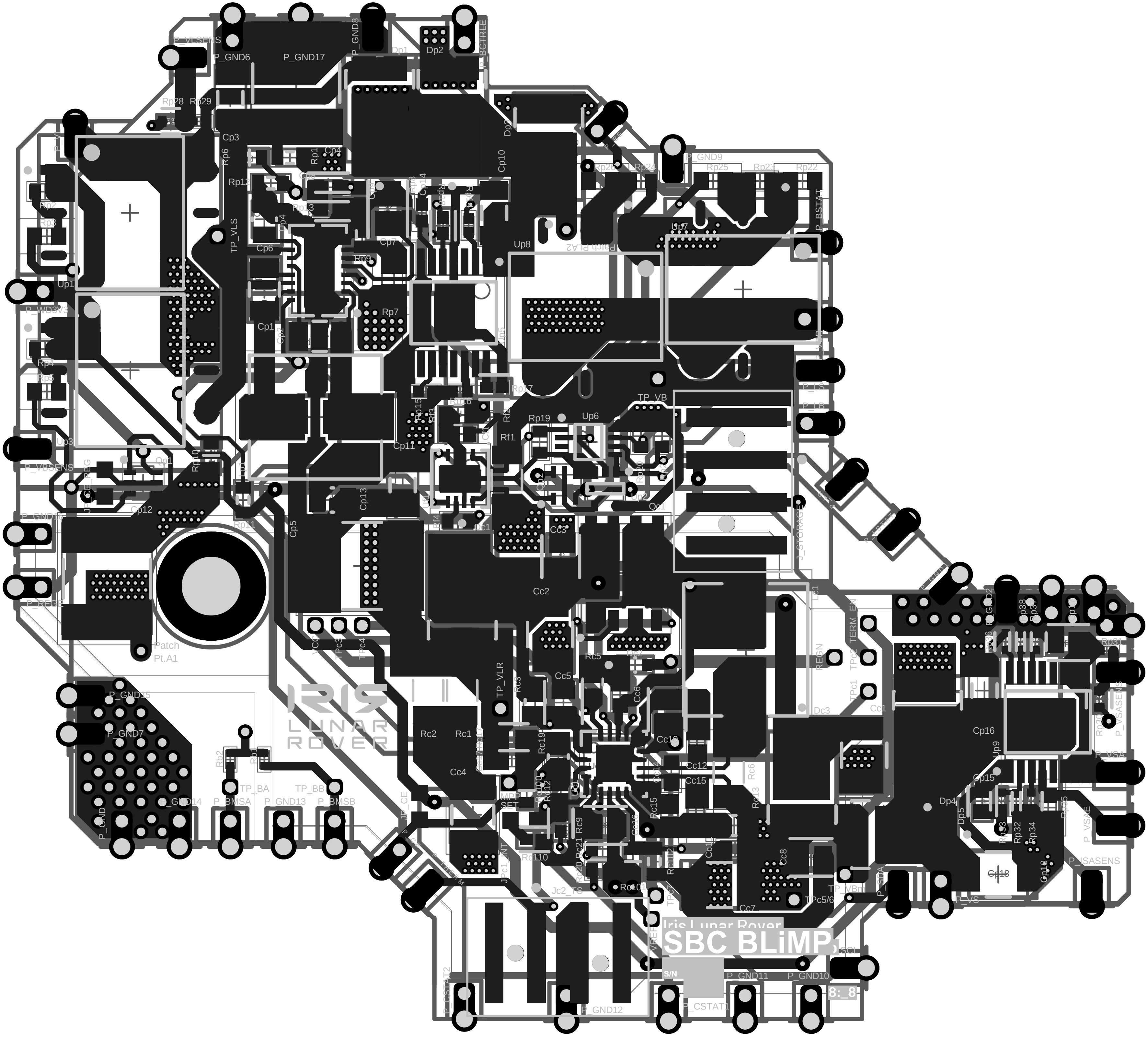
File: C:\Users\..\Revisions.SchDoc		Drawn By: Connor W. Colombo	


IRIS
LUNAR
ROVER
Iris Lunar Rover
SBC BLiMP