BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
INSTRUCTION DIVISION
SECOND SEMESTER 2015 - 2016
COURSE HANDOUT (PART II)

Date: 15 / 01 / 2016

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No :**CS G524**
Course Title **:Advanced Computer Architecture**
Instructor-in-charge : S Mohan

1. Scope and Objective:

The course aims at familiarizing students with advanced computer architectures suitable for high-performance computing. The advanced concepts in uniprocessor and the issues in designing & using high performance parallel computers will also be covered. System resources such as memory technology and I/O subsystems needed to achieve proportional increase in performance will be discussed along with the software support required for these systems.

2. Text Book:
Computer Architecture: A Quantitative Approach, by J.L. Hennessy & D.A. Patterson, Morgan Kaufmann., 5th Ed, 2012.

3. Reference Books:
(R1) Modern Processor Design, John P Shen & Mikko H. Lipasti., Tata McGraw Hill, 2006.
(R2) Advanced Computer Architecture, Kai Hwang, McGraw Hill, 1993.
(R3) Computer Organisation & Design Patterson, David A & J L Hennenssy, Elsevier, 4th Ed. 2009.

4. Course Plan:

Lecture No.	Topics to be covered	Reference
01	Introduction	Ch. 1
02, 03	CISC & RISC, Performance	Ch. 1
04, 05	Review of Pipelining Concepts	**Appendix-A**
06, 07	Pipeline Implementation – Design	**Appendix-A**
08, 09, 10	Static Scheduling	Ch. 3
11, 12	Dynamic Scheduling	Ch. 3
13	Case Study	----
14, 15, 16	Exploiting ILP: SMT Approach	Ch. 3
17	Memory Organisation- Introduction	**Appendix-C**
18, 19	Memory Organisation – Cache Memory	Ch. 2
20, 21	Memory Organisation – Main Memory	Ch. 2
22, 23, 24	Virtual Memory & Virtual Machines	
25	Storage Systems	**Appendix-D**
26, 27	Storage Systems- RAID	**Appendix-D**
28	Case study	**Appendix-D**
29	Parallel Processing – Introduction	Ch. 5
30,31	Shared Memory Multiprocessors	Ch. 5
32, 33	Diistributed Shared Memory	Ch. 5

	Multiprocessor	
34, 35	Cache Coherency, Memory Consistency Models	Ch. 5
36, 37	Multithreading & Multithreded Processors	Ch. 5
38, 39	VLIW & EPIC	**Appendix-H**
40, 41	Recent Trends	**-----**

6. Evaluation Scheme:

EC No.	Evaluation Component	Duration (min)	Weightage (%)	Date & Time	Nature of Component
1	Mid Sem Test	90	40	15/3 11:00 - 12:30 PM	Closed Book
2	Assignment and Project*	-----	15		Open Book
3	Comprehensive	180	45	5/5 AN	Partly Open

* Details of the assignments and project will be announced later.

8. Chamber Consultation Hours: *Tuesday 3PM to 4 PM*

9. Make-up Policy:

Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

10. Notices: Notices regarding the course will be put up on the course web page and major notices will be displayed on the IPC notice board.

Instructor - in - charge
CS G524