Course Handout (Part II)

Date: 10.01.2016

In addition to Part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : MEL G641
Course Title : CAD for IC Design
Instructor-in-charge : ABHIJIT ASATI (Pilani Campus)
Other Instructors : Mr. Gavax Joshi (Goa Campus), email: gbjoshi@goa.bits-pilani.ac.in

1. Scope and Objective of the course:

To teach the basic concepts of CAD tools used for IC/VLSI Design process. To be conversant with the use of existing CAD tools and algorithms for all the stages of the design cycle of a VLSI chip design and to study the design issues involved in the development of CAD tools. Current trends in CAD tools for IC/VLSI design.

2. Text Book:

(i) An Introduction to CAD for VLSI
Author: Stephen M. Trimberger

Publisher, Year: Kluwer Academic Press 1987.

(ii) Algorithm for VLSI Physical Automation, 3rd Edition

Author: Naveed Sherwani

Publisher, Year: Kluwer Academic Press, 1998

3. Reference Books

(i) VLSI Physical Design Automation: Theory and practice

Author: Sadiq M Sait and Habib Youssef

Publisher, Year: World Scientific Press, 1999

(ii) Computer Aids for VLSI Design

Author: Steven M. Rubin

Publisher, Year: Addison Wesley, 1987

(iii) Simulation in the Design of Digital systems

Author: John B. Gosling

Publisher, Year: Cambridge University Press (CUP), 1993

(iv) Introduction to VLSI Systems

Author: Carver Mead and Lynn Conway

Publisher, Year: Addison-Wesley,1980

(v) A VHDL Primer, 3rd Edition,

Author: J. Bhaskar

Publisher, Year: Pearson /Prentice-Hall, 1999

(vi) Verilog HDL

Author: Samir Palnitkar

Publisher, Year: Pearson Education Asia, 2007

(vii) Synthesis and Optimization of Digital Circuits

Author: Giovanni De Micheli

Publisher, Year: Tata McGraw-Hill, 1994

4. Course Plan

Topics	**Lectures**
An introduction to electronic system design and CAD for IC Design	2
CAD: A general overview	2
IC Design Flows and CAD Tools	6
HDLs (VHDL/Verilog Modeling)	11
Schematic, Layout and Stick Editors	5
Overview of CIF	1
Partitioning, Floor-planning and Assignment	4
Placement and Routing	5
High Level and logic Synthesis	2
Simulation (Behavioral , Functional, Logic, Mixed mode, and Fault simulation)	1
Current trends in CAD tools	1
TOTAL	40

5. Evaluation schedule:

EC No.	Components	Duration	Weightage (%)	Date & Time	Remarks
1.	Test-1	50 min.	20	TBA	Closed Book
2.	Test-2	50 min.	20	TBA	Open Book
3.	Comprehensive Examination	3 Hrs	40	7/5 AN	Closed Book
4.	Project/Seminar/Lab Assignments	Regular	20	TBA	Open Book

6. Chamber consultation hour: Will be declared later

7. Notices: All notices related to the course will be put on the **EEE** Notice board.

(Instructor-in-charge)

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