BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
FIRST SEMESTER 2015 - 2016
COURSE HANDOUT (PART II)

Date: 3 / 08 / 2015

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : **MEL G624**
Course Title : **Advanced VLSI Architecture**
Instructor-in-charge : K.R.Anupama (anupkr@goa.bits-pilani.ac.in)
Instructors : Vineet Kumar, S.K.Sahoo

1. Scope and Objective:

The course aims at familiarizing students with advanced parallel processing architectures suitable for high-performance computing. It deals with three levels of parallelism – Instruction-Level, Data Level and Thread Level.

2. Text Book:

T1. *Computer Architecture: A Quantitative Approach,* by J.L. Hennessy & D.A. Patterson, Morgan Kaufmann., 3rd Ed, 2006.
T2. Modern Processor Design: Fundamentals of Superscalar Processors, John Paul Shen & Mikko.H.Lipasti , Tata McGraw Hill,2011.
T3. DSP Processor Fundamentals, Phil Lapesly , Jeff Bier, Amit Shoham, Edward.A.Lee, Wiley India Edition,2011.

3. Reference Books:

(R1) Parallel Computer Architecture: A Hardware / Software Approach, David E Culler & Jaswinder Pal Singh., Morgan Kauffmann / Harcourt India, 2002.
(R2) Computer Architecture Pipelined& Parallel Processor Design, M.J.Flynn, Narosa Publishing House, 2006
(R3) Advanced Computer Architecture: A Design Space Approach, Sima, Fountain,Kacsuk, Pearson, 2012.
(R3) Journals & Conference Proceedings

*** It is assumed that students have a working knowledge of MIPS Architecture**
4. Course Plan:

No.	Topics to be covered	Reference
01	Introduction to Parallel Processing	Class Notes
02-04	Introduction to ILP	T1- Ch-3, T2 – Ch1
05-11	Pipeline architectures	T2-Ch2
12	VLIW architectures	Class Notes
11-19	Superscalar Architectures	T2-Ch4, 5
20-21	DSP Architectures	T3

	Case Studies -1	Self -Study
23	Instruction level Data parallel Architecture- Introduction	Class Notes
24-26	SIMD Architectures	Class Notes
27-29	Vector Processors	Class Notes
	Case Studies-2	Self-Study
30	Thread & Process Level Parallel Architectures- Introduction	Ch 6
31-34	Multi-threaded architectures	Class Notes
35-37	Distributed Memory MIMD Architectures	Class Notes
38-40	Shared Memory MIMD Architecture	Class Notes
	Case Studies -3	Self Study

The material in the text will be supplemented with papers from Journals. Class Notes will include journal papers, e-material

5. Evaluation Scheme:

EC No.	Evaluation Component	Duration (min)	Weightage (200)	Date, Time & Venue	Nature of Component
1	Test I	60	45	9/10 10:00 - 11:30 AM	Closed Book
2	Test II	60	45		Closed Book
3	Case Studies, Class Room Interactions	….	30		
4	Comprehensive	180	80	10/12 AN	Closed/Open Book

* Details of the assignments will be announced later.

6. Chamber Consultation Hours: *To be Announced*

7. Make-up Policy:

Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

9. Notices: Notices regarding the course will be displayed on moodle.

Instructor - in - charge