Birla Institute of Technology and Science, Pilani
Instruction Division
First Semester 2015-16
Course Handout (Part-II)

Date:03/08/2015

In addition to Part I (General Handout for all the courses appended to the time table), this portion gives further specific details regarding the course.

Course No.	**CS F215/EEE F215/INSTR F215**
Course Title	**Digital Design**
Instructor-in-charge	S.MOHAN
Team of Instructors	
(i) For Lecture	S. Gurunarayanan, S.Mohan, Arnab Hazra
(ii) For Tutorial	Srinivas Reddy, Vineet Kumar, SnehLata, Arnab Hazra, Devesh S., Nitin Chaturvedi, Anantha Krishna C.
(ii) For Practical	Lucky Sharan, Priya Gupta, Mahesh Angira, Prachi Sharma, Jitendra, Meenakshi S., J. Bhardwaj, Ravinder Kumar, Nitin Chaturvedi, Prashant Upadhyay.
Course Description	This course covers the topics on logic circuits and minimization, Combinational and sequential logic circuits, Programmable Logic devices, State table and state diagrams, Digital ICs, Arithmetic operations and algorithms, Introduction to Computer organization, Algorithmic State Machines, RTL level realization of Digital systems
Scope and Objective	The objective of the course is to impart knowledge of the basic tools for the design of digital circuits and to provide methods and procedures suitable for a variety of digital design applications. The course also introduces fundamental concepts of computer organization. Laboratory exercises on Combination and Sequential logic design will be given as a part of the course.

Text Books :

T1: M.Moris Mano and Michael D. Ciletti "Digital Design", PHI, 5th Edition, 2013

T2: G Raghurama. S Gurunarayanan, Sudeept Mohan, Karthik, "Laboratory Manual", EDD notes 2007.

Reference Books:

R1: Donald D.Givonne, "Digital Principles and Design" TMH, 2003

R2: W. Stallings, "Computer Organization and Architecture" PHE, 9th Edition, 2012

Course Plan

Lect. No.	Learning Objectives	Topics to be covered	Reference to Text Book
1	Introduction to Digital Systems and Characteristics of Digital ICs.	Digital Systems, Digital ICs	1.1; 1.9; 2.3, 10.1,2
2-3	Simplification of Boolean functions	K-Maps (4,5 variables), QM Method	3.1 to 3.4, 3.5 to 3.8
4-6	Combinational Logic, Arithmetic circuits	Adders, Subtracters Multipliers	4.1 - 4-7
7	Simulation and synthesis basics using HDL	Hardware Description Languages	3.11
8-9	Sequential Logic	Flip-Flops & Characteristic tables, Latches.	5.1 to 5.4
10-13	Digital Integrated Circuits	TTL, MOS Logic families and their characteristics	10.3, 10.5, 10.7 to 10.9
14-16	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	4.8 to 4.11
17	Simulation of Combinational Logic Functions.	HDL for Combinational Logic	4.12
18-20	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction	5.5, 5.7
21	Simulation of Sequential	HDL for Sequential Logic	5.6

	Logic Functions.		
22-24	Memory and PLDs	RAM, ROM, PLA, PAL	7.1, 7.5 to 7.7
25-28	Registers & Counters	Shift registers, Synchronous & Asynchronous counters, clock skew & Clock Jitter	6.1 to 6.5
29	Analysis of arithmetic units	Multiplication & Division algorithms	R2
30-31	Design of Digital Systems	Algorithmic State Machines	R1. Chapter 8
32-3**8**	Modular approach for CPU Design	RTL, HDL description	8.1,8.2, 8.4 to 8.8
39-40	Memory Organization	Memory Hierarchy & different types of memories	R2

Evaluation Scheme:

Component	**Duration**	**Maximum Marks**	**Date & Time**	**Venue**	**Remarks**
MID SEMESTER TEST	90 mins	90	8/10 2:00 - 3:30 PM	To be announced	CB
Assignments/Tutorials	To be announced	45	Continuous	To be announced	-
Comprehensive Examination	3 Hrs	120	9/12 FN	To be announced	CB/OB
Practical: Regularity, Lab reports & Viva		20	Regular lab sessions		
Lab test		25	To be announced		

(b) Practicals

S.No.	**Name of experiment**
1.	BOOLEAN FUNCTIONS IMPLEMENTATION
2.	DESIGN OF ARITHMATIC CIRCUITS
3.	IMPLEMENTATION OF BCD ADDER
4.	DECODERS, MULTIPLEXERS AND DEMULTIPLEXERS
5.	LATCHES & FLIP-FLOPS
6.	OPERATION OF A 4-BIT COUNTER
7.	COMPARATORS & ARITHMETIC LOGIC UNIT
8.	COUNTER DESIGN
9.	SHIFT REGISTERS
10.	DESIGN OF SEQUENCE DETECTOR
11.	MEMORIES AND FPGAS

Assignments: Assignment sheets will be given in tutorial classes. There will be evaluation based on these assignments in the tutorial classes. There will also be Simulation based assignments, which will be given as take home assignments.

Chamber Consultation Hour: To be announced in class

Notices: All notices will be displayed on the CS, LTC and EEE notice boards