**Date: 02/08/2016**

In addition to Part-I (General Handout) for all courses appended to the time table), this portion gives further specific details regarding the course.

*Course No* : EEE G594
*Course Title* : Advanced VLSI Devices
*Instructor-in-charge* : **Arnab Hazra**

## 1. Scope of the course:

The present course will basically deal with the Physics, Analysis, and Design of Novel and Advanced VLSI Device (Mostly in Nano-scale dimensions) Structures. The main topics for this course center around Nano FETs (Field-Effect Devices) the most promising VLSI Device till date.

## 2. Objective of the course:

At the end of the course, one will be able to:

- Make projections about CMOS device scaling and how it affects circuit/system performance.
- Recognize the relevant device physics that underlies CMOS device design.
- Go to a conference or read a journal article about CMOS devices and use the knowledge obtained in this course to understand the material.
- Develop an intuitive feel in addition to solving equations.
- Obtain necessary skills to explore the research space of state-of-the-art VLSI technology.

## 3. Course Description:

This course examines the device physics of and engineering of advanced transistors and the way such devices enter into the development of new technologies. Focus is given on the review of metal oxide semiconductor (MOS) fundamentals along with quasi-ballistic and ballistic transport. Short-channel effects (SCEs) in sub-micron (towards nanometer regime) metal oxide semiconductor field-effect transistors (MOSFETs) including device scaling considerations are also included. Device physics and engineering issues of sub 100 nm MOSFETs (towards nanometer regime) are the primary objectives. Limits of the state-of-the-art silicon device technology and key issues in the miniaturization of devices are also integrated here. Alternative device structures (non-conventional MOSFETs) and transport in novel nano-devices are also part of this course.

## 4. Pre-requisite:

Students, want to go through the course, only should have a little background of Electron Devices [EEE/INSTR F214], and Physics & Modeling of Microelectronics Devices [MEL G631] (but may not be too stringent !!)

## 5. Related Books:

[1] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Third Edition, Wiley, 2006.
[2] S. M. Sze, *Semiconductor Devices : Physics and Technology*, Second Edition, Wiley, 2002
[3] Sima Dimitrijev, *Principles of Semiconductor Devices*, Second edition, Oxford University Press, 2013
[4] J. Singh, *Electronic and Optoelectronic Properties of Semiconductor Structures*, CUP, 2007
[5] S. D. Brotherton, *Introduction to Thin Film Transistors:Physics and Technology of TFTs*, Springer,2013
[6] Cherie R. Kagan, Paul Andry, *Thin Film Transistors*, Marcel Dekker, Inc., 2016
[7] Charles P. Poole, Frank J. Owens, *Introduction to Nanotechnology*, Wiley, 2011

**6. Course Plan:**

| Lect. No. | Topic | Learning Objective | References |
|---|---|---|---|
| **Part I: Review of long channel MOSFETs** | | | |
| 1-2 | MOS Capacitor Device Physics | Review the basic concepts of MOS Device Physics. | *Study Materials will be provided* |
| 3-4 | Fundamental of MOSFETs | Review the basic concepts of MOSFET device structure, operation, I-V characteristics, device modelling etc. | |
| 5-8 | MOSFET Scaling: Short Channel Effects (SCEs), Mobility reduction, Subthreshold Current, Channel Length Modulation, Drain Induced Barrier Lowering (DIBL) and Finite Output Resistance. | To realize the significance of Second Order Effects on the device operation and other performance limitations of conventional MOSFET due to the device scaling. | |
| **Part II: Nanoscale MOSFETs** | | | |
| 9 | Challenges of Nanoscale MOSFETs | Down Scaling benefits and rules. | *Study Materials will be provided* |
| 10-12 | Limitations of Nanoscale MOSFETs: Subthreshold Leakage, Threshold Voltage Variation, Mobility Degradation, Hot Carrier Effects, Source Drain Tunnelling, Parasitic Resistance and Capacitance, Reverse Biased Junction Leakage Current etc. | To realize the overall limitations of Nanoscale MOSFETs considering the Channel, Gate, Drain/Source and Substrate related issues individually. | |
| **Part III: Advanced MOSFETs (Reduction of Short Channel Effects and Performance Enhancement Techniques)** | | | |
| 13-18 | Silicon-on-Insulator (SOI) MOSFETs: Fully Depleted (FD) SOI, Partially Depleted (PD) SOI, Junction Less SOI. | To gain the idea about Silicon-on-Insulator (SOI) devices and its structures, manufacturing materials, operations, characterizations, modelling and applications to control of short channel effects. | *Study Materials will be provided* |
| 19-24 | Other Multigate SOI-MOSFETs: Double Gate, FinFET, π Gate, Ω Gate, Gate-All-Around (GAA) or surrounding gate, Silicon on Nothing (SON), Nanowire FET | Study the advanced MOSFETs structures and device characteristics to realize the advantages, drawbacks to propose the possible solutions. | |

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| 25-30 | (i)Channel Engineering: Retrograde Substrate and Halo Doping profiles;<br>(ii)Gate Engineering: High-k gate dielectrics, Metal Gate-Stack;<br>(iii) Sorce/Drain (S/D) Engineering: S/D Engineering of nanoscale double gate SOI MOSFETs, Schottky-barrier S/D Technology;<br>(iv) Material Engineering: high mobility materials (e.g. Ge, GaAs/InGaAs etc.) for channel of FET; | Study the complete device engineering towards more advanced MOSFET device structures. | |
| **Part IV: Promising Nanodevices Beyond CMOS** | | | |
| 31-33 | Thin Film Transistors (TFT): Hydrogenated amorphous silicon (a-Si:H) TFT | Study the a-Si:H material, a-Si:H TFT architecture, fabrication process, layout, performance and characterizations. | *Study Materials will be provided* |
| 34-37 | Single Electron Transistors (SETs): Single Electron Box, Quantum dot, Charge quantization, Coulomb Blockade. | Development of fundamental concepts on Single Electron Transistors (SETs). | |
| 38-40 | Impact-Ionization MOSFETs (IMOSFETs); Tunnel FETs (TFETs); Schottky-Barrier FETs (SBTFETs); Cabron Nanotube-FETs (CNTFET) | Development of fundamental concepts on IMOSFETs, TFETs, SBTFETs, and CNTFET. | |

7. **Other Home and Reading Assignments:** These will be specified from time to time.

8. **Evaluation Scheme:**

| Component | Duration | Marks | Date and Time | Remarks |
|---|---|---|---|---|
| Mid Sem Test | 90 Mints. | 70 | 3/10 4:00 - 5:30 PM | Open Book |
| Assignment (Laboratory Computer Simulation /Device Modeling ) | | 20 | To be announced | Demo / test |
| Comprehensive | 3 hrs | 110 | **2/12 AN** | Closed Book |
| **TOTAL** | | **200** | | |

9. **Chamber Consultation Hour**: To be announced in Class (arnab.hazra@pilani.bits-pilani.ac.in)
10. **Make-up Policy**: Make-up will be given on extremely genuine grounds only. Prior application should be made for seeking the make-up examination.
11. **Notices**: Notices, if any, concerning the course will be put up on EEE Notice Board.

**Instructor In Charge**
**EEE G594**