BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
FIRST SEMESTER 2015 - 2016
COURSE HANDOUT (PART II)

Date: 03 / 08 / 2016

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No	: **MEL G624**
Course Title	: **Advanced VLSI Architecture**
Instructor—Goa	: K.R.Anupama (anupkr@goa.bits-pilani.ac.in)
Instructor–Hyd	:J.Sowmya (soumyaj@hyderabad.bits-pilani.ac.in)
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	: Vineet Kumar (vineet@pilani.bits-pilani.ac.in)

1. Scope and Objective:

The course aims at familiarizing students with advanced parallel processing architectures suitable for high-performance computing. It deals with three levels of parallelism – Instruction-Level, Data Level and Thread Level.

2. Text Book:

T1. *Computer Architecture: A Quantitative Approach,* by J.L. Hennessy & D.A. Patterson, Morgan Kaufmann., 3rd Ed, 2006.
T2. Modern Processor Design: Fundamentals of Superscalar Processors, John Paul Shen &Mikko.H.Lipasti , Tata McGraw Hill,2011.
T3. Advanced Computer Architecture: A Design Space Approach, Sima, Fountain,Kacsuk, Pearson, 2012.

3. Reference Books:

(R1) Parallel Computer Architecture: A Hardware / Software Approach, David E Culler & Jaswinder Pal Singh., Morgan Kauffmann / Harcourt India, 2002.
(R2) Computer Architecture Pipelined& Parallel Processor Design, M.J.Flynn, Narosa Publishing House, 2006
(R3) DSP Processor Fundamentals, Phil Lapesly , Jeff Bier, Amit Shoham, Edward.A.Lee, Wiley India Edition,2011.
(R3) Journals & Conference Proceedings

*** It is assumed that students have a working knowledge of MIPS Architecture**

4. Course Plan:

No.	Topics to be covered		Reference
01	Introduction to Parallel Processing		Class Notes
	Reading Assignment 1- CPU Architecture Introduction (At the end of 1st week of course work)		T1 Ch1 (1.3 -1.13)
02-04	Introduction to ILP	Pipeline Dependencies	T1- Ch-3, T2 – Ch1
		Arithmetic & Architectural Pipelines	
		Pipeline Idealism	
05-07	Pipeline architectures – Design of RISC Pipeline	Typical RISC Pipeline Design	T2-Ch2
		CISC Pipeline	
		Pipeline Examples	
	Reading Assignment 2 – Memory Design (At the end of 3rd week of course)		T2 Ch2
08-11	Superscalar Architectures -Pipeline Design – Data Path	Widening of Pipeline	T2-Ch4, 5
		Parallel Fetch & Decode	
		Instruction Dispatch & Issue	
		Register Renaming &Tomsulo	
		ROB	
		Superscalar Pipeline Operation - Examples	
	Reading Assignment 3 – VLIW Architectures (At the end of 6th week of course work)		Ch1 – Appendix H
12-16	Superscalar Architectures – Branch Prediction	Basic Branch Prediction Schemes	T2- Ch 9, Ch 10
		BTA &Misprediction Penalty & Recovery	
		Advanced Branch Prediction – Correlated Branch Prediction	
		Advanced Branch Prediction – Hybrid	
		Advanced Branch Prediction – Tournament Predictors	
		Value Prediction - Introduction	
	Reading Assignment 5- A Comparative Study of Advanced Branch Predictors (At the end of 9th week of course work)		Relevant Journal & Conference Papers
	Reading Assignment 6 – Value Prediction (At the end of 11th week of course work)		T2 – Ch 10

17	Instruction level Data Parallel Architecture- Introduction		
18-20	SIMD Architectures	Fine Grained Parallel SIMD	T1-Ch4 & Class Notes
		Coarse Grained SIMD	
		Examples of SIMD operation	
21-22	Vector Processors	VMIPS Architecture	T1-Ch4
		Multi-Lane Systems	
		Performance Analysis of vector Systems	
23-24	GPU	SIMD Extensions	T1-Ch4
		NVIDIA GPU Architectures - SIMT	
	Reading Assignment 7 – CUDA (At the end of 13th week of course work)		
25	Thread & Process Level Parallel Architectures- Introduction		T1-Ch5
26	Multi-threaded architectures	Shared Memory & Distributed Memory Architecture	T1-Ch5, T2 Ch-11
		Cache in TLP	
27-29	Cache Architectures	Snoopy Cache Protocols	T1-Ch5
		MSI, MESI	
		MESIF, MOSIF	
		4C of Cache	
		Directory based Cache	
30	Multi-Threaded Architectures	Explicit Multi-Threading	T2 – Ch11
		Implicit Multi-Threading	
	Reading Assignment 8- Interconnection Network in Multi-core Processors (At the end of penultimate week of course)		T1- Appendix F + Relevant Papers
31	CPU vs ASIC : qualitative analysis of performance (speed) and energy consumption of functions		Class Notes + Relevant Papers
32	CPU vs ASIC : quantitative modeling of speed and energy consumption of functions		Class Notes + Relevant Papers
33	Application Specific Instruction-set Processor (ASIP) - the via media between CPU and ASIC.		Class Notes + Relevant Papers
34-35	Techniques for identifying Application Specific instructions.		Class Notes + Relevant Papers
36-40	Design approaches for ASIPs - examples and cases		Class Notes + Relevant Papers

Note:

- *The material in the text will be supplemented with papers from Journals. Class Notes will include journal papers, e-material.*
- *Reading Assignments will be evaluated based on Activity in On-line Discussion Forum on EdX – based on Reading Assignment Topics of Discussion / Open Ended problems will be put up.*
- *All students will have to do Reading Assignment 1.*
- *Students can pick 3 out of the remaining Reading Assignments. Maximum number of students/ reading assignment will be decided based on Class Strength.*

5. Evaluation Scheme:

EC No	Evaluation Component	Duration (min)	Weightage (200)	Date, Time	Nature of Component
1	Test I	60	25	TBA	Closed Book
2	Test II	60	25	TBA	Closed Book
3	Class Room & Online Interactions	….	80	15	Open Book
	4- Reading Assignments			20	
	GEM5 Assignment Problems			45	
4	Comprehensive	180	70	5/12 FN	Closed/Open Book (25+45)

6. Chamber Consultation Hours:*To be Announced for Goa Campus. For students of Pilani &Hyd Campus – I will be usually available on-line on EdX forum or via Mail.*

7. Make-up Policy: Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

8. Plagiarism & Copying: Plagiarism and copying will be dealt with severity. Any student who Plagiarizes or copies will automatically be given 0 for all assignment and class room interaction components.

9. Notices: Notices regarding the course will be displayed onEdX site.

Instructor - in - charge