BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, Pilani
Pilani Campus

INSTRUCTION DIVISION
FIRST SEMESTER 2016-2017
Course Handout Part II

Dated : Aug 2016

In addition to part I (General Handout for all courses appended to the time-table) this portion gives further specific details regarding the course.

Course No. **: MEL G623**
Course Title **: ADVANCED VLSI DESIGN**
Instructor-in-charge **: ANU GUPTA**

1. Scope and Objective of the Course:

The field of Digital very large-scale integrated circuits has gone through dramatic evolutions and changes. With minimum feature size approaching 60 nm, the complexity of the designs and interconnection parasitics has increased dramatically. This has led to new design methodologies and implementations strategies. This course is intended to give a detailed knowledge and experience in design of advanced VLSI circuits and chips in today's and future nano-scale CMOS technologies. Major VLSI design challenges will be studied, followed by careful treatment of several versatile digital, and mixed analog-digital circuit building blocks frequently utilized in VLSI chips The deep submicron devices behave differently, and bring to the forefront a number of issues that influence reliability, cost, performance, and power dissipation of the digital IC. With communication systems getting more and more complex, there is an ever increasing need for a VLSI designer to understand these issues and new design methodologies. Importance of research papers, and CAD tools in IC design process is also emphasized.

2. Text Book :

J. M. Rabaey, A. Chandrakasan, "Digital integrated Circuits-A design perspective", Second Edition, Prentice Hall Electronics and VLSI Series

Reference Books :

1. IEEE journals
2. William J Dally, John W Poulton, " Digital Systems Engineering"; Cambridge University Press
3. A. Bellaour, M. Elmasry, "Low power digital VLSI design-circuits and systems" , Second Edition, Kluwer academic publishers,
4. R. Best, "Phase Locked Loop",McGraw Hill Publishers.
5. S. S. Rofail, K. S. Yeo, "Low voltage, Low power Digital BiCMOS Circuits", Prentice Hall Inc.
6. K. Roy, S.C. Prasad, "Low Power CMOS VLSI Circuit Design", Wiley Interscience Publication.
7. M. J. S. Smith, "Application Specific Integrated Circuits", Pearson Education (Singapore) Pte Ltd.
8. Bhaskhar Jayram, "AVHDL PRIMER", Prentice Hall.
9. IEEE Journals of solid state circuits, VLSI system.
10. Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman, " **Digital Systems testing and** testable design," September 1994, Wiley-IEEE Press
11. Martin. Ken, "Digital Integrated Circuit Design", Oxford University Press, Inc.
12. Michael. L. Bushnell, and Vishwani. D. Agrawal, "Essentials Of Electronic Testing For Digital, Memory And Mixed Signal VLSI Circuits. Kluwer Academic Publishers, Third Edition, 2004

13. Behrooz Parhami, "Computer Arithmetic-algorithms and Hardware design", Oxford University Press Inc , 2000
14. Sutherland. I., Harris. David, Sproull. Bob, " Logical Effort-Designing Fast CMOS Circuits", Morgan Kaufmann Publishers.

3. Course Plan :

No. of Lec. (approx.)	Topic To be Covered	Learning Objectives	Ref. to Text Book
1	General Introduction		
6	Timing issues in synchronous VLSI systems and system timing,	System design issues	Text book (ch. 7) / IEEE journals
5	Clock signals distribution and clock generation (All Digital phase locked loop design assignment)	Clock distribution networks Generation of clock using DLL and its design	Chapter -10 , Ref-3
9	High speed computer arithmetic – algorithms and design, ➢ Addition / subtraction -- Parallel prefix computation ➢ Multiplication / division ➢ Logical effort in circuit design,	Techniques for high speed computation	Chapter-11, Ref.-12, Ref. 13, IEEE papers
2	Input/output circuits design, ground bounce	Interfacing circuits	Ref-2
5	Low power VLSI circuit design techniques	Low power consuming circuit design techniques	Ref-2, 4,5, IEEE papers
4	Deep submicron device engineering,	Knowledge of mos device at submicron level	Chapter-I , IEEE papers
5	Asynchronous system design ASIC technology, FPGA technology (overview)	Request acknowledge protocols in design ASIC chip design issue (mostly covered through lab work), FPGA chip design issue	Text book (ch. 10) / IEEE journals Ref-7, IEEE journals
4	Wire design principles in nanometer region Memory and array structures (overview and self reading)	Driver circuits design techniques, signal integrity etc. Memory organization and design of memory cells	Ref-2, , IEEE papers Chapter-12, IEEE papers
Total Lectures No. (41)			

4. Evaluation Scheme :

Component	Duration	Marks	Date & Time	Venue	Remarks
Mid Semester Test	50 Mts.	25	-		CB/ OB
Assignments /project/ presentations	(Continuous)	40	Spread across the semester		OB
Comp. Exam	3 Hours	35	12/12 AN		CB
		100			

5. **Assignment :** Regular Assignments covering use of VERILOG, , and MENTOR GRAPHICS/ CADENCE TOOLS for Simulation of Advanced VLSI Circuits will be given.

7. **Make up Policy:** Make up will be given only on genuine reasons. Applications for make up should be given in advance and prior permission should be obtained for Scheduled tests.

8. **Chamber Consultation Hour/s :** 5 pm Mon-Thurs. / or fix a time prior to meeting

9. **Notices:** All notices related to the course will be put on EEE Notice Board.

Instructor-In-Charge
MEL G623