FIRST SEMESTER 2014-2015
Course Handout Part II

Dated: 03/08/2015

In addition to part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. **: MEL G626**
Course Title **: VLSI TEST & TESTABILITY**
Instructor-in-charge **: Abhijit Asati email: abhijit_asati@pilani.bits-pilani.ac.in**
Other Instructors : Mr. Gavax Joshi (Goa Campus), email: gbjoshi@goa.bits-pilani.ac.in

1. Scope and Objective of the Course:

The objective of this course is to deal with the study of VLSI design flow, Functional verification, verification flow, need of electronic testing, fault modeling, test generation for combinational circuits, test generation for sequential circuits, fault simulation, Built-In Self-Test (BIST), Memory testing, Design for Testability (DFT), SoC test, fault diagnosis, Analog/RF test.

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2. Text Book :

i) Michael. L. Bushnell, and Vishwani. D. Agrawal, "Essentials Of Electronic Testing For Digital, Memory And Mixed Signal VLSI Circuits" Kluwer Academic Publishers, Third Edition, 2004**.**

ii) B. Wile, John C. Goss and W. Rosner *" Comprehensive Functional Verification" Morgan Kaufmann, 2005*

3. Reference Books :

i) *M Abromovici, M A Breuer & A. D. Friedman "Digital Systems Testing and Testable Design ", Jaico Publications, Paperback Impression, 2001.*
ii) *H. Fujiwara, "Logic Testing and Design for testability" MIT Press, 1985.*
iii) *IEEE Transactions on Computers*
iv) *IEEE Transactions on VLSI Systems*

4. Course Plan:

S.No.	Topic	Lectures
1	Introduction + VLSI design flow	3
2	Functional verification and verification challenges	1
3	Simulation-based verification (SBV)	4
4	Introduction to system verilog	3
5	Formal verification (FV): BDD, Formal Boolean equivalence checking, property checking	4
6	Semi-formal verification	1

7	Electronic testing	1
8	Fault modeling: Stuck-at, bridge, delay, and cross-talk fault Models	3
9	Test generation for combinational circuits: ATPG algorithms (D-algorithm, PODEM, FAN)	5
10	Test generation for sequential circuits: Time frame expansion model	2
11	Built-In Self-Test (BIST)	3
12	Memory test	2
13	Delay test	2
14	Design for Testability (DFT)	2
15	System-on-a-Chip (SoC) test	1
16	Fault diagnosis, Analog/RF test, Test issues in nano-technology	1
	Total	38

5. Evaluation Scheme :

Component	Duration	Marks	Date & Time	Venue	Remarks
Test-1	50 Min	20	5/10 10:00 - 11:30 AM	TBA	CB/OB
Test-2	50 Min	20	TBA	TBA	CB/OB
Assignments	(Continuous)	20		(OB)	
Comp. Exam	3 Hours	40	1/12 AN	TBA	CB
		100			

6. Chamber Consultation Hours : To be announced in the class.

7.Notices: All notices related to the course will be put on EEE Notice Board.

Instructor-In-Charge
MEL G626