INSTRUCTION DIVISION
FIRST SEMESTER 2016 - 2017
COURSE HANDOUT (PART II)

Date: 02 / 08 / 2016

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : EEE G626
Course Title : Hardware/Software Codesign
Instructors/in-charge : ASHISH MISHRA.

1. Scope and Objective

The course provides advanced knowledge in the design of complex computer systems, in particular embedded systems. Models and methods are discussed that are fundamental for systems that consist of software and hardware components. Investigate topics ranging from system modeling to hardware-software implementation; explore analysis and optimization processes in support of algorithmic and architectural design decisions; and gain design experience with case studies using contemporary high-level methods and tools. The course emphasizes a top-down design methodology driven by bottom-up constraints.

2. Contents

The course covers the following subjects:

- Models for describing hardware and software components (specification)
- System design (hardware-software partitioning and design space exploration)
- Performance analysis and estimation techniques

3. Prerequisites

Prerequisites for the course is a basic knowledge in the following areas: computer architecture, digital design, software design, and embedded systems.

4. Text Book

1. Daniel D Gajski, Frank Vahid, Sanjay Narayan, Jie Gong, *Specification and Design of Embedded Systems*, Prentice Hall, 1994.
2. Patrick R. Schaumont, A practical Introduction to Hardware/Software Codesign. Springer, 2010.
3. Peter Marwedel, *Embedded System Design*, Springer 2003
4. Jorgen Staunstrup, Wayne Wolf, *Hardware / Software Co-Design: Principles and Practice*, Kluwer Academic, 1997.

5. Reference Book

1. G. DeMicheli, R. Ernst and W. Wolf, Readings in Hw/Sw Co-design, M. Kaufmann, 2002,
2. Hardware/Software Codesign. G. DeMicheli and M. Sami (eds.), NATO ASI Series E, Vol. 310, 1996.
3. Sanjaya Kumar, James H. Aylor, Barry W. Johnson, and Wm. A. Wulf. The Codesign of Embedded Systems. Kluwer, 1995
4. Tony Givargis, Frank Vahid, Embedded System Design : A Unified Hardware / Software.
5. Black David C. SystemC : From The Ground Up

6. V. Raghavan , Principles of compiler design, Tata Mcgraw Hill Publishing Co Ltd ,2010.
7. Journal papers and Conference publications

6. Course Plan

Lecture No.	Learning Objectives	Topics to be covered	References
01-02	Introduction	Introduction to Embedded System Design/High Level Design, Introduction to Hardware/Software Codesign, Dualism of Hardware and Software designs.	T3: CH-5
03-05	Case study	Digital Camera Design, Theora design	R4 : CH-7 and notes
06-14	Linux ,Profiling and Dot format	Profiling: gprof and cachegrind. Drawing graphs and Benchmarks.	Class notes
15-16	Specification and Modeling concepts	Concept of system modeling, Need for Concurrent Models.	T1 :CH-2
17-18	Modeling and implementation concepts	Analysis of Data Flow Graphs and Control Flow Graphs, Hardware Implementation and Software Implementation of Data Flow, Data and Control Edges of C Program, Translation of C to Hardware	R4:CH-3
19-22	High Level Synthesis	Introduction to compiler : Generating graphs in LLVM and using Vivado	Class notes, R6
23 -25	Specification Languages	Modeling with SystemC	R5
26	Co-simulation and Co-verification	Introduction to Co-simulation Environment	Class notes
27- 29	Hardware/Software Interfaces	Connecting Hardware and Software, On-Chip Bus Systems, Bus Transfers, Synchronization schemes, Memory-Mapped Interfaces, Coprocessor Interfaces, Custom Instruction Interfaces	CH-8,9
30,31	Mapping and Scheduling	Architecture mapping and scheduling	Class notes
32-35	System Partitioning	Partitioning Issues, Partitioning algorithms, Functional partitioning for Hardware, Hardware and Software Partitioning Algorithms	T1:CH-6
36-39	Power Management & Design Quality Estimation	Quality Metrics, Hardware Estimation, Software Estimation: DVS, DPM and software power	T3:CH-5,7
40	Estimation Techniques	Hardware and Software	T1:CH-9

7. Evaluation Scheme

EC No.	Evaluation Component	Duration (min)	Weightage (%)	Date & Time	Nature of Component
1.	MID semTest	90	30	4/10 4:00 - 5:30 PM	Closed Book
3.	Lab/Project/ Assignment/ Presentation	------	35	To be announced	Open Book
4.	Comprehensive	180	35	5/12 AN	Open/Closed Book

8. Lab

All the reading material will be provided to the students. This course has will have demo on various tools like vivado, compiler, operating system, device drivers and SystemC. Students are expected to take projects on these topics.

9. Chamber Consultation Hours

4 to 5 P.M From Monday to Friday

10. Notices

Notices regarding the course will be put up on the course web site only

11. Makeup

Make-up will be given on **genuine** grounds only. Prior application should be made for seeking the make- up examination.

Instructor - in - charge
EEE G626