BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, Pilani
Pilani Campus

INSTRUCTION DIVISION

FIRST SEMESTER 2015-2016

Course Handout Part II

Dated: 03/08/2015

In addition to part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. **: EEE F313/ INSTR F313**
Course Title **: ANALOG AND DIGITAL VLSI DESIGN**
Instructor-in-charge **: ANU GUPTA**

1. Scope and Objective of the Course:

The objective of this course is to deal with the study of the technology and building blocks of analog and digital integrated circuits. It is also included to deal with the salient features of digital circuits, structured systems and design automation in VLSI field. Scope of the course includes an introduction to practical considerations and fundamentals of integrated circuits and basic principles of design of digital and analog integrated circuits. Importance of CAD tools in IC design process is also envisaged.

2. Text Books :

(T1) Rabaey Jan M. , Chandrakasan Anantha and Nikolic Borivoje, " Digital Integrated Circuits", Pearson Education. McGraw Hill.

(T2) Behzad Razavi,"Design of Analog CMOS integrated circuits", TATA McGraw Hill.

Prime reference Books:

(R1) Kang. S.M and Leblebici Y., "CMOS Digital Integrated Circuits: Analysis and Design,

(R2) Johns. David A. and Martin K, "Analog Integrated Circuit Design," John Wily & Sons. Inc.

Reference Books :

1. *Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley Publishing Company.*
2. *Pucknell D.A. and Eshraghian K.,"Basic VLSI design", Prentice Hall of India Pvt. Ltd.*
3. *Allen Phillip and Holberg Douglas, "CMOS Analog Circuit Design", Oxford University Press.*
4. *Gregorian R., Temes G.C.,"Analog Mos integrated circuits for signal processing", Wiley Interscience Publication.*
5. *Sze S.M.,"VLSI Technology", Second edition, TATA McGraw Hill.*
6. *Randall A Geiger, Phillips E. allen, Noel R Strader, "VLSI Design techniques for analog and digital circuits," TATA McGraw Hill.*
7. *Bhaskhar Jayram, "A VHDL PRIMER", Prentice Hall.*
8. *Palnitkar Samir, "Verilog HDL" Pearson Education Asia.*
9. *IEEE Journals of solid state circuits, IEEE transactions on Very Large Scale Integration system.*

10. Martin. Ken, "Digital Integrated Circuit Design", Oxford University Press.

3. Course Plan :

Topic to be covered	Learning Objectives	No. of Lectures	Reference/Text Book
General Introduction			
1. Introduction to VLSI Design Methodologies	Knowledge of Existing Design Methods	2	Chapter-1 (T1) /(R1)
2. MOS Processing Technology, Design Rules, MOS Capacitances	Fabrication Technique Modeling of MOS for analysis	2	Chapter-2,3 (T1), (T2)
3. HDLs	VHDL/Verilog Modeling	2	Reference book-7 ,8
Digital Design			
1. MOS inverter- D.C and switching characteristics	Design of MOS Inverter.	5	Chapter- 3, 4, (T1), R1
2. Combinational MOS static logic circuits	Design of Complex digital circuits	5	Chapter-5,6 (T1), R1
3. Dynamic logic gates and flip flops	Design of Sequential circuits Design of Memory cells, decoders,	5	Chapter- 7,8,9 (T1), R1
4. Timing	pipeline	4	
5. Memory Circuits—selected portion	sense amplifiers	1	Chapter-10, 11 Chapter-10 (T1)+ (R1)
Analog Design			
6. Advanced current sources & sinks; Reference circuit	Design of biasing circuits	6	Chapter- 5,6 (T2), (R2)
7. Operational amplifiers architectures	Design of single & cascade amplifier Comparator design	6	Chapter-9 (T2), (R2)
8. Noise	Effect of noise on design	2	Chapter -7 (T2), (R2)
9. Comparators -overview		1	Reference 3

4. Evaluation Scheme :

Component	Duration	Marks	Date & Time	Venue	Remarks
Mid Sem. Test	50 Mts.	80	6/10 2:00 - 3:30 PM		CB/OB
Assignments	(Continuous)	60	Spread Across The Semester		OB
Weekly Tutorials	15-20 min.	60			OB
Comp. Exam	3 Hours	100	4/12 FN		CB/OB
		300			

5. **Assignment :**
Regular assignments covering use of VHDL/Verilog (modelsim simulator), cadence tools for design and simulation of VLSI circuits will be given.

6. **Makeup Policy:** Make up will be given only on genuine reasons. Applications for makeup should be given in advance and prior permission should be obtained for scheduled tests.

7. Chamber Consultation Hours : To be announced in the class.

8. **Notices:** All notices related to the course will be put on EEE Notice board.

Instructor-In-Charge