From: **Caleb Howington** howingtonc@gmail.com
Subject: ASC Paper Review Comments
Date: January 18, 2019 at 5:30 PM
To: Britton Plourde bplourde@syr.edu

CH

Dear Caleb Howington:

This message is to update you about the status of your manuscript, ASC2018-4EPo1A-03 titled "Interfacing superconducting qubits with cryogenic digital logic: Measurement", which has been submitted to the ASC 2018 Special Issue of the IEEE Transactions on Applied Superconductivity.

Based on the recommendations of reviewers, I am requesting that you make MAJOR REVISIONS to your manuscript. My comments and the reviewers' comments are included at the bottom of this message.

Please prepare a revised manuscript. To upload your revised manuscript, log into https://mc.manuscriptcentral.com/asc2018 and enter your Author Center from where you can submit the revision by clicking the "Manuscripts Awaiting Revision" queue or the "Click here to submit a revision" button. Your manuscript number has been given an appendix to denote a revision.

Also, please respond DIRECTLY to all comments enumerated by reviewers and editors. The upload form incorporates space to respond to comments. You can use this space to document any changes you make to the original manuscript. You can also incorporate responses into the cover letter or as a supplementary document. In order to expedite the processing of the revised manuscript, please be as specific as possible in your response to the reviewer(s) and editor.

It is highly recommended to use red text to indicate changes in the manuscript. Please note that, if the manuscript is accepted for publication, final files will be requested. These should not contain red text.

**NOTE: The revised manuscript is expected to improve. Lack of sufficient improvement may result in a reject decision.

DUE DATE FOR REVISION: 05-Feb-2019

Once again, thank you for submitting your manuscript to the ASC 2018 Special Issue of the IEEE Transactions on Applied Superconductivity and I look forward to receiving your revision.

Sent by ScholarOne Manuscripts https://mc.manuscriptcentral.com/asc2018 on behalf of:
Marcio de Andrade, Technical Editor
ASC 2018 Special Issue of the IEEE Transactions on Applied Superconductivity
marcio.deandrade@navy.mil

Technical Editor's Comments (if any) to Author:

Reviewer(s)' Comments to Author:

Reviewer: 1

Comments and suggestions for the author(s) (do not identify yourself or your institution).
The manuscript “Interfacing superconducting qubits with cryogenic digital logic: Measurement” by Howington shows the idea and numerical simulation of the qubit readout by using the SFQ circuits through the Josephson photomultiplier. Although I think it is interesting and valuable to publish from IEEE TAS, I have major comments as follows:

[M1] Regarding the scalability of the proposed readout scheme, the authors mention many qubits over 10^4 can be realized by using the cryogenic digital components in the abstract. On the other hand, in the main text, there is no clear estimation of the scalability of the consumption power for the proposed scheme. The author should describe this point, especially from the point of view of the possibility of the SFQ circuit implementation in the mK stage with the qubits.

[M2] The title of the manuscript seems confusing. I think it is better to replace asurement” with “Readout (or something)” because only simulation results are described in the present manuscript.

Minor comments are as follows:
[m1] QND should be defined as Quantum nondemolition in the main text

[m1] QND should be defined as Quantum nondemolition in the main text.
[m2] In the second paragraph of section II, “The Josephson Photomultiplier (JPM) is …” should be replace with “JPM is …” because JPM was already defined in section I.
[m3] It is better to change the order of Fig.2 and Fig.3.

Reviewer: 2

Comments and suggestions for the author(s) (do not identify yourself or your institution).
This paper is well organized and clearly written.
The authors present qubit readout scheme with a JPM coupled to a ballistic (un-shunted) JTL. This work is a continuation of the authors' previous series of works, and would be of interest to TAS readers.
If possible, would you clearly mention what is the new point you add in this paper compared to the previous works?
Some comments and request for addition.

1) In table 1, what is the unit?
2) In Fig 4, can you include any hint about "JPM reset" after qubit readout?
3) The power dissipation was well described in the previous literature,but if this paper is implicitly mentioning many qubits up to more than 10^4,then here are the questions.
- How much area is required to operate this circuit at mK, per readout, including the cooling?
- If the circuit gets densely packed, there would be a thermal gradient on chip in lateral dimension before the heat is dissipated to the substrate and the cold plate. What is the typical expected thermal length?
- Would you kindly add a paragraph about brief summary of power dissipation issue, including the power consumption, circuit footage, material and integration?
- Is the temperature you mentioned in line 55, page 2, "50 mK" for qubit operation, low enough?
I would suggest far lower temperature than 50 mK for proper coherence and fidelity of qubit operation.
Could you add any comments on that?
- Does your analysis of the heat load due to SFQ include the thermal budget for wiring? Or is it simply negligible?
Could you add a comment on that?
4) I think it would be better to present Fig 3 before Fig 2, as they are described in that order in the text.