Dear Marcio de Andrade,

We thank the reviewers for reading our manuscript and we are pleased that they both had a generally positive response. We have made revisions in response to the reviewer comments and we feel that this has strengthened our manuscript.

One of the reviewers suggested a change of title, which we have updated in the attached file. However, we leave this up to the discretion of the Editor, since the updated title will not match the ASC abstract it originated from.

The circuit diagrams in Figures 1 and 2 have also been replaced with higher quality versions.

Response to reviewers 1 and 2 are below:

Reviewer: 1

The manuscript “Interfacing superconducting qubits with cryogenic digital logic: Measurement” by Howington shows the idea and numerical simulation of the qubit readout by using the SFQ circuits through the Josephson photomultiplier. Although I think it is interesting and valuable to publish from IEEE TAS, I have major comments as follows:

[M1] Regarding the scalability of the proposed readout scheme, the authors mention many qubits over 10^4 can be realized by using the cryogenic digital components in the abstract. On the other hand, in the main text, there is no clear estimation of the scalability of the consumption power for the proposed scheme. The author should describe this point, especially from the point of view of the possibility of the SFQ circuit implementation in the mK stage with the qubits.

The text has been updated to not specify an exact number of potential qubits, as an exact analysis of the heat load of the proposed circuit is outside of the current scope of this paper. A related scheme for interfacing a JPM and SFQ circuitry was considered previously by some of us in Ref. [3], which contained a discussion of the associated heat load in a large qubit array. We have updated the text to refer more directly to Ref. [3].

[M2] The title of the manuscript seems confusing. I think it is better to replace “Measurement” with “Readout (or something)” because only simulation results are described in the present manuscript.

The title was initially proposed as the second part of sequential talks at ASC. We have taken the reviewer's suggestion and changed "Measurement" to "Readout", assuming this is permitted.

Minor comments are as follows:
[m1] QND should be defined as Quantum nondemolition in the main text.

QND is now defined before the first usage.

[m2] In the second paragraph of section II, “The Josephson Photomultiplier (JPM) is …” should be replace with “JPM is …” because JPM was already defined in section I.

Second JPM definition is removed

[m3] It is better to change the order of Fig.2 and Fig.3.

We agree with both reviewers here. Figure order has been updated.

Reviewer: 2

This paper is well organized and clearly written.
The authors present qubit readout scheme with a JPM coupled to a ballistic (un-shunted) JTL. This work is a continuation of the authors' previous series of works, and would be of interest to TAS readers.
If possible, would you clearly mention what is the new point you add in this paper compared to the previous works?

A sentence has been added to the introduction that better explains the scope of this paper.

Some comments and request for addition.

1) In table 1, what is the unit?

SFQ margins are usually reported as fractional variations. We have updated the Table to report all of the margins as percentages to remove any ambiguity.

2) In Fig 4, can you include any hint about "JPM reset" after qubit readout?

The JPM can be re-initialized into a single well once detected. A sentence has been added to Fig. 4, as well as a reference included to the full protocol.

3) The power dissipation was well described in the previous literature,but if this paper is implicitly mentioning many qubits up to more than 10^4,then here are the questions.
- How much area is required to operate this circuit at mK, per readout, including the cooling?
- If the circuit gets densely packed, there would be a thermal gradient on chip in lateral dimension
before the heat is dissipated to the substrate and the cold plate. What is the typical expected thermal length?
- Would you kindly add a paragraph about brief summary of power dissipation issue, including the power consumption, circuit footage, material and integration?
- Is the temperature you mentioned in line 55, page 2, "50 mK" for qubit operation, low enough?

I would suggest far lower temperature than 50 mK for proper coherence and fidelity of qubit operation.
Could you add any comments on that?
- Does your analysis of the heat load due to SFQ include the thermal budget for wiring? Or is it simply negligible?
Could you add a comment on that?

As we described in our response to Reviewer #1, we have removed the mention of >10^4 qubits. There is not sufficient space in the present manuscript to discuss the footprint, heat load, and wiring considerations, but we have now added references to our earlier work, Ref. [3], where these topics were addressed in the context of a related circuit.

4) I think it would be better to present Fig 3 before Fig 2, as they are described in that order in the text.

We agree with both reviewers here. Figure order has been updated.