



NIOBIUM INTEGRATED CIRCUIT FABRICATION

PROCESS #03-10-45

DESIGN RULES

REVISION #25, 12/12/2012

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Preface

HYPRES, Inc. has developed and sustains several fabrication processes for superconductor electronics. This document specifies the design rules of HYPRES fabrication process #03-10-45 for niobium-based superconducting integrated circuits. This information constitutes a self-contained guide to the physical layout of devices and circuits within the scope of the standard HYPRES fabrication process. Adherence to these rules will provide cost-effective, high yield designs.

1.0 General Description

- 1.1 This HYPRES IC fabrication process uses only refractory materials, with the exception of a Pd/Au metallization layer used primarily for contact pads and Copper used for wafer level bump layer. Niobium is used as the superconducting material due to its comparably high critical temperature, electrical and thermal stability, and ability to be thermally cycled many times without degradation. Aluminum/Niobium/Aluminum-Oxide/Niobium Josephson tunnel junctions are made by depositing an *in-situ* quad-layer across the entire wafer and subsequently defining junction areas by 1x photolithography and etching. This method yields good uniformity and reproducibility of junction parameters.
- 1.2 HYPRES currently offers three processes with three different critical current densities of Al/Nb/AlO_x/Nb quad-layer: 0.03 kA/cm² (0.3 μA/μm²), 1.0 kA/cm² (10 μA/μm²), and 4.5 kA/cm² (45 μA/μm²).
- 1.3 The Josephson junctions can be interconnected into circuit configurations using four superconducting layers (junction base electrode (layer M1), two Nb wiring layers (layers M2 and M3) and superconducting Nb ground plane (layer M0).
- 1.4 One normal metal layer is used to provide medium-value resistors, which can be used for shunting Josephson junctions, current distribution, *etc.* The sheet resistance of this layer is given in the table below for all three processes.

Process Jc	Sheet Resistance at 4.5K, Ohm/□	Material	Tc, K	Thickness, nm
0.03 kA/cm ²	2.0±0.20	Ti/AuPd/Ti	0.0	100±10
1.0 kA/cm ²	1.0±0.15	Mo	0.9	70±10
4.5 kA/cm ²	2.1±0.3	Mo	0.9	40±6

- 1.5 Silicon dioxide is deposited to provide insulation between the conducting layers. Anodization of the base electrode of quad-layer provides additional insulation to Josephson junctions.
- 1.6 Our standard fabrication process uses 6-inch (150 mm) diameter oxidized Si wafers.
- 1.7 HYPRES Niobium Process Flow Overview (next page)

#	Layer	GDS#	Mask polarity	Description
				Nb deposition
1	M0	30	-	M0 patterning (holes in niobium ground plane)
				SiO ₂ deposition
2	I0	31	-	Contact (via) between M1 and ground plane
				Al/Nb/Al, AlO _x /Nb quad-layer deposition (see 1.2)
3	I1A	2	+	Counter-electrode (junction area) definition for 0.03 or 1.0 kA/cm ² process.
3a	I1C	4	+	Counter-electrode (junction area) definition for 4.5 kA/cm ² process.
				Base electrode anodization
4	A1	5	+	Anodization layer patterning
5	M1	1	+	Quad-layer base electrode patterning
				SiO ₂ deposition
				Resistive layer deposition (see 1.4)
6	R2	9	+	Resistor patterning
				SiO ₂ deposition
7	I1B	3	-	Contact (via) between M2 and (I1A, R2, or M1)
				Nb deposition
8	M2A/M2	6	+	M2 layer patterning
				SiO ₂ deposition
9	I2	8	-	Contact (via) between M2 and M3
				Nb deposition
10	M3	10	+	M3 layer patterning
				SiO ₂ deposition (I3 - passivation layer)
	I3			Patterning (Contact pad between R3 and M3, using R3 – layer)
11	R3	11	+	R3-image reversal patterning for contact pad
				Diffusion stopping layer deposition,
				Pd/Au contact metallization evaporation
				R3, layer lift-off
12	BUMP	15	-	Wafer level bump patterning
				Copper evaporation
				BUMP layer lift-off
				DICE

2.0 Layout Design Rules

2.1 Minimal size and spacing for each layer is specified in the following table.

1	M0	Negative ⁽¹⁾	μm	6	R2	Positive	μm
	1.1	M0 spacing to M0	2.0		6.1	R2 spacing to R2	2.0
	1.2	M0 minimal size ⁽⁵⁾	2.0		6.2	R2 minimal size ⁽⁵⁾	3.0
	1.3	M0 spacing to I0	1.5		6.3	R2 surround I1B	1.5
	1.4	M0 spacing to M1	1.0		6.4	R2 spacing to M2	1.0 ⁽³⁾
	1.5	M0 spacing to R2	1.5 ⁽³⁾	7	I1B	Negative	
2	I0	Negative			7.1	I1B spacing to I1B	2.0
	2.1	I0 minimal size	2.5		7.2	I1B minimal size	2.0
	2.2	I0 spacing to I1C	1.5 ⁽²⁾		7.3	I1B surrounded by M2	1.5
	2.3	I0 surrounded by M1	1.5	8	M2	Positive	
	2.4	I0 spacing to R2	1.0		8.1	M2 spacing to M2	2.5
3	I1C ⁽⁴⁾	Positive			8.2	M2 minimal size ⁽⁵⁾	2.0
	3.1	I1C spacing to I1C	2.0		8.3	M2 surround I2	1.5
	3.2	I1C minimal size	1.5	9	I2	Negative	
	3.3	I1C surrounded by A1	1.0		9.1	I2 minimal size	3.0
	3.4	I1C spacing to M1	1.5		9.2	I2 surrounded by M3	1.5
	3.5	I1C spacing to R2	0.5	10	M3	Positive	
4	A1	Positive			10.1	M3 spacing to M3	2.5
	4.1	A1 spacing to A1	2.0		10.2	M3 minimal size ⁽⁵⁾	2.0
	4.2	A1 minimal size	2.0		10.3	M3 contact width with R3	3.0
	4.3	A1 surrounded by M1	0.5	11	R3	Positive	
	4.4	A1 spacing to R2	0.5		11.1	R3 spacing to R3	5.0
	4.5	A1 surround I1A or I1C	1.0		11.2	R3 minimal size ⁽⁵⁾	3.0
	4.5	A1 surround I1B	1.5	12	BUMP	Negative	
5	M1	Positive			12.1	BUMP spacing to BUMP	10.0
	5.1	M1 spacing to M1	2.5		12.2	BUMP minimal size ⁽⁵⁾	10.0
	5.2	M1 minimal size ⁽⁵⁾	2.5				
	5.3	M1 spacing to R2	1.0 ⁽³⁾				
	5.4	M1 surround I1B	1.5				

(1) “Negative” (dark-field) mask means, that the corresponding physical layer on the wafer will be removed from the design area. “Positive” (clear-field) mask means, that the physical layer will remain on the wafer in the design area.

(2) HYPRES cannot guaranty the quality (V_m , etc.) and the precise critical current (I_c) of junctions residing in I0 hole. I1A patterns may not overlap with I0 patterns.

(3) R2 patterns may not cover steps (M0, I0, or M1). We also recommend avoiding unnecessary crossings between M2 and R2 patterns.

(4) All rules for layer I1A are the same as for I1C.

(5) Minimal size is the minimal size of the real object (not mask), please see table 3.1 for bias value

3.0 Physical Layer Process Specifications

3.1 Since the fabrication process involves projection photolithography and etching, the size of structures on the wafer may differ somewhat from the design layout (*i.e.* feature size on the photomask). This change in size is called “bias”. In the table below, the bias is defined as the shift of the object’s border due to its enlargement/reduction relatively to its image on the mask. A positive bias means larger objects on the wafer than in the design.

Layer	Material	Bias (3.1), μ	Physical layer properties: Resistance, Capacitance, <i>etc.</i>	Thickness nm
M0	Nb	0.2±0.2	Nb, superconductor. Penetration depth $\lambda_L = 90$ nm	100±10
I0	SiO ₂	0.2±0.2	SiO ₂ , insulator. Capacitance: 0.28 fF/ $\mu\text{m}^2 \pm 20\%$	150±15
M1	Al/Nb	0.0±0.1	Quad-layer base electrode, superconductor. $\lambda_L = 90$ nm	135±10
I1A, I1C	AlO _x /Nb	0.0±0.1	Quad-layer counter electrode and tunnel barrier (see 3.2 and 3.3)	50±5
A1	Nb ₂ O ₅		Insulation on top of the base electrode surrounding I1A	40±5
	SiO ₂		SiO ₂ , insulator. Capacitance: 0.42 fF/ $\mu\text{m}^2 \pm 20\%$	100±10
R2		0.0 ± 0.2	(see table in 1.4)	
	SiO ₂		SiO ₂ insulator. Capacitance: 0.42 fF/ $\mu\text{m}^2 \pm 20\%$	100±10
I1B		- 0.1 ± 0.2	Contact hole through the above two SiO ₂ layers	
M2	Nb	- 0.2 ± 0.1	Nb, superconductor. Penetration depth $\lambda_L = 90$ nm $\pm 5\%$	300±20
	SiO ₂		SiO ₂ insulator. Capacitance: 0.08 fF/ $\mu\text{m}^2 \pm 20\%$	500±40
I2		0.1 ± 0.2	Contact hole through the above insulator	
M3	Nb	- 0.4 ± 0.2	Nb, superconductor. Penetration depth: $\lambda_L = 90$ nm $\pm 5\%$	600±50
	SiO ₂		SiO ₂ insulator.	200±20
I3			Contact hole through the above insulator, patterned by R3	
R3	Mo/Pd/Au	0.0 ± 1.0	Contact pads metallization	350±60
BUMP	Copper	0.0 ± 1.0	Wafer level Copper bump metallization	2000±200

3.2 We recommend using Josephson junctions of **circular** shape. The deviation of the radius of the circle in I1A (I1C) layer is within +/- 0.1 μm (see table 3.1). HYPRES **does not guarantee** high accuracy area for the small objects of other shapes in I1A or I1C layer.

3.3 The dependence of JJ specific capacitance vs. critical current density can be approximated by the following formula:

$$C_s = \frac{1.0}{24.7 - 2.0 \cdot \ln j_c} \quad (pF / \mu\text{m}^2)$$

here, C_s is specific capacitance in pF/ μm^2 and j_c is critical current density in $\mu\text{A}/\mu\text{m}^2$.

This gives us roughly 50 fF/ μm^2 at 10.0 $\mu\text{A}/\mu\text{m}^2$, 59 fF/ μm^2 at 45.0 $\mu\text{A}/\mu\text{m}^2$, and 37 fF/ μm^2 at 0.3 $\mu\text{A}/\mu\text{m}^2$. That is in a good agreement with the experimental data.

3.4 The critical current per micron width for Nb films is given in the following table

Nb Layer	M0	M1	M2	M3
I_c (mA/ μm)	20.0	30.0	50.0	70.0

If the wire crosses over steps, its I_c may drop by more than 50%. Please, see the minimal width of a wire in table 2.1 and the bias in table 3.0 before designing current transmitting lines.

4.0 Lithography features

4.1 Mask Grid Size

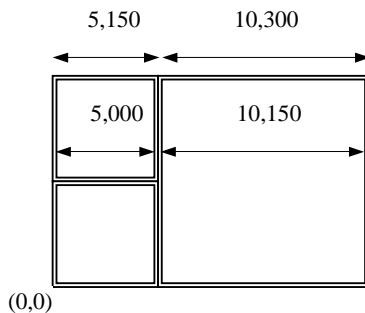
Mask	Layer	Grid Size [μm]
M0	Negative	0.5
I0	Negative	0.5
M1	Positive	0.5
I1A	Positive	0.1
I1C	Positive	0.1
A1	Positive	0.5
R2	Positive	0.5
I1B	Negative	0.1
M2	Positive	0.5
I2	Negative	0.5
M3	Positive	0.5
R3	Positive	0.5
BUMP	Negative	0.5

4.2 Layers I1A, I1C and I1B have a grid size of 0.1 μm . All remaining layers must use a grid size of 0.5 μm . Every vertex coordinates are being rounded up to a multiple of these numbers.

4.3 All layouts are **mirror imaged** when printed on wafers.

5.0 Designs Submission Formats

- 5.1 The layout file must be in GDS-II format.
- 5.2 Please submit designs to HYPRES through File Transfer Protocol (FTP) at <ftp://customer@ftp.hypres.com> or, if the size of the file is **less than 10 MB**, via E-mail to masoud@hypres.com.
- 5.3 The active chip area is limited by 5000 μm x 5000 μm and surrounded by 150- μm dicing channels. Dicing channels between chips are 150 μm wide. That means that 75 μm on each side of each die is consumed in dicing. No objects are allowed in the dicing channel.
- 5.4 It is also allowed to submit 1-cm chips. In this case, the die size is 10.3 mm x 10.3 mm and the actual size of the chip is 10.15 mm x 10.15 mm. All other sizes should be negotiated with HYPRES prior the submission.
- 5.5 When delivering layouts to HYPRES, send **only one file**, with all chips placed together in a single “supercell” with **5150- μm** grid. The “supercell” should be a cluster of chips (see example below), with the lower left corner of the cluster placed at (0, 0). The super cell area should therefore be exactly 5150 x 5150 x $N \times M$, where $N \times M$ is the number of chips.



- 5.6 **No cell name may exceed 60 characters.** Cell names will be truncated to this size automatically and might clobber other cells.

6.0 Cycle Time

- 6.1 One week is required to fabricate the photo masks.
- 6.2 Five weeks are required to process wafers.
- 6.3 Two days are required for dicing, Process Control Monitor testing, and packaging of chips.
- 6.4 Total cycle time is weeks and 2 days from mask release. Note: Cycle times may change depending upon customer requirements.
- 6.5 On average HYPRES has 8 mask releases per year. See www.hypres.com for up-to-date information and schedules.