



**Micro  
Technology  
Unlimited**

## **K-1012 SYSTEM BOARD**

**PROM-I/O-COMM.-PROGRAMMER  
FOR 6502 PROCESSORS**

**MAY 1979**

The K-1012 PROM/IO is a carefully engineered, manufactured, and tested product that should operate perfectly when handled and installed according to the following instructions. Note that the board is shipped in a black conductive plastic bag. Since MOS integrated circuits are used, damage from static discharge is possible. It is helpful to reduce static by working in an area with concrete floors and a reasonable humidity level. If this is impossible, at least avoid wearing rubber soled shoes and move slowly in the work area. When unpacking or handling the board, touch the screw sticking up in the middle of the heatsink first and release it last. Note that the preceding comments apply equally to the microcomputer board which of course contains MOS IC's also.

Connection to the microcomputer board should be as indicated in the accompanying chart. The easiest method of connection is with an MTU model K-1005 motherboard/cardfile. Alternatively the user may obtain two 2x22 pin printed circuit board edge connectors (.156" contact spacing) such as the one supplied with the processor and wire them together except for pins 3, 4, 16-20, and X. Wire length should not exceed 4 inches. Plug the processor expansion connector into one of the sockets, make any necessary connections to the application connector, and make any necessary power connections. The K-1012 may then be plugged into the other connector. Note that the K-1012 provides the DECODE ENABLE and VECTOR FETCH signals needed by the KIM-1 for expanded memory. They may be ignored with the SYM and AIM processors.

Note that as shipped the board requires an unregulated voltage between +7 and +12 volts to operate the logic and another unregulated voltage between +14 and +20 volts to operate the memory chips such as provided by the expansion outputs of an MTU K-1000 power supply. The on-board regulators may be bypassed by shorting the two outside pins of each regulator IC together if the user wishes to use a regulated power source. Use of the PROM programmer with a shorted 12 volt regulator is not recommended because the on-board voltage multiplier may not be able to supply the necessary programming power from the lower voltage. The various option jumpers on the board should not be reconfigured until the board is tested. The diagnostic program in the back of this manual assumes the standard jumper configuration which is already installed on assembled boards.

After connecting the processor, the K-1012, and the power supply, the system may be turned on. Pressing RESET on the processor should initiate normal operation. Assuming that one or more PROM's have been installed, look at some PROM addresses and verify that the contents are proper. No PROM's or blank PROM's should read FF. Look at addresses FE04-FE07 and FE08-FE0B which are the control and data registers of the PIA chips. The even addresses should read 00 and the least significant 6 bits of the odd addresses should also be zero. Look also at FE00 which should contain 00. This is the control register of the ACIA chip. The data register at FE01 may contain anything but it should be steady.

If all is well at this point the test program supplied with the K-1012 should be loaded through the keyboard and dumped to cassette tape. The entry point is 0200 and the program should return to the monitor shortly thereafter. If memory location 0000 contains 00, the diagnostic ran without error. Otherwise an error code has been stored and the program listing should be consulted to interpret the error. Then the troubleshooting guide elsewhere in this manual should be consulted for a possible solution.

The diagnostic checks the I/O registers on the two PIA chips and verifies that the ACIA transmits at the correct speed. Because of the nature of the board, a thorough diagnostic is not possible without considerable external fixturing. In our factory we install a set of test PROMS and a special loopback cable on the application connector. While the factory diagnostic is running, several critical signals are checked with an oscilloscope. The PROM programmer is also checked for proper voltage levels and the functionality of the failsafe circuit.

# OPTION STRAPPING AND JUMPER PLACEMENT

This board undoubtedly has more option jumpers than all of our other boards put together. This was done to accomodate the KIM/SYM/AIM processors, maximize flexibility, and minimize logic. However the board is shipped with all jumpers in a "standard" configuration which should suit the majority of KIM-1 users. Standard jumper tables for the SYM and AIM are shown below. Those jumpers that are most likely to be changed have been implemented as 16 pin DIP sockets. The contacts used in these sockets have adequate spring to withstand repeated insertion and withdrawal of #22 solid wire jumpers. The user may also utilize component carriers wired with jumpers or a standard 8 position DIP switch may be plugged into the socket.

The following summarizes the function of the major jumper options along with their standard settings in parentheses:

1. The address range of the MAIN group of 8 PROM's. (2000-3FFF)
  2. The address range of the AUXILIARY group of 4 PROM's and the exact mix of the 4 PROM's within the auxiliary block. (4000-5FFF, PROM's occupy 4000-4FFF) Fewer than 4 PROM's may be activated if desired, a deactivated PROM will not use up address space.
  3. The address of the I/O page (FE00)
  4. The base address of the I/O ports within the I/O page (00)
  5. The baud rate for the serial port (300 baud)
  6. Exchange of two of the modem control signals with two of the PIA handshake signals. (PIA handshake selection is standard)
  7. Allow or disallow interrupts from the PIA chips (disallow is standard) (The ACIA has its interrupt request permantly wired in)
  8. Selection between 2708 and TMS2716 PROM chips (need not be the same in main and auxiliary arrays) (2708 is standard, PC lines must be cut and jumpers soldered to the board to select TMS2716)
  9. Selection between 2708 and TMS2716 for the PROM programmer (2708 is standard, PC lines must be cut and jumpers soldered to the board to select TMS2716)
- M2708 [II-2 and II-15  
II-1 and II-16]*

## MAIN PROM ADDRESS STRAPPING (Using 2708 type PROM's)

ADDRESS RANGE	Jumper these pins together
0000 - 1FFF	U12-7 & U12-10      U12-5 & U12-12      U12-3 & U12-14
2000 - 3FFF	<i>16 RAM</i> U12-7 & U12-10      U12-5 & U12-12      U12-4 & U12-13 *
4000 - 5FFF	<i>16 RAM</i> U12-7 & U12-10      U12-6 & U12-11      U12-3 & U12-14
6000 - 7FFF	<i>16 RAM</i> U12-7 & U12-10      U12-6 & U12-11      U12-4 & U12-13
8000 - 9FFF	<i>16 RAM</i> U12-8 & U12-9      U12-5 & U12-12      U12-3 & U12-14
A000 - BFFF	<i>8 RAM</i> U12-8 & U12-9      U12-5 & U12-12      U12-4 & U12-13
C000 - DFFF	<i>4 ROM</i> U12-8 & U12-9      U12-6 & U12-11      U12-3 & U12-14
E000 - FFFF	<i>4 ROM</i> U12-8 & U12-9      U12-6 & U12-11      U12-4 & U12-13
NONE	<i>U12-8 &amp; U12-9</i> <i>U12-7 &amp; U12-11</i> <i>7+10 4 + 13</i>

ADDRESS RANGE	Jumper these pins together
0000 - 1FFF	U12-7 & U12-10      U12-5 & U12-12      U12-3 & U12-14
2000 - 3FFF	<i>16 RAM</i> U12-7 & U12-10      U12-5 & U12-12      U12-4 & U12-13 *
4000 - 5FFF	<i>16 RAM</i> U12-7 & U12-10      U12-6 & U12-11      U12-3 & U12-14
6000 - 7FFF	<i>16 RAM</i> U12-7 & U12-10      U12-6 & U12-11      U12-4 & U12-13
8000 - 9FFF	<i>16 RAM</i> U12-8 & U12-9      U12-5 & U12-12      U12-3 & U12-14
A000 - BFFF	<i>8 RAM</i> U12-8 & U12-9      U12-5 & U12-12      U12-4 & U12-13
C000 - DFFF	<i>4 ROM</i> U12-8 & U12-9      U12-6 & U12-11      U12-3 & U12-14
E000 - FFFF	<i>4 ROM</i> U12-8 & U12-9      U12-6 & U12-11      U12-4 & U12-13
NONE	<i>U12-8 &amp; U12-9</i> <i>U12-7 &amp; U12-11</i> <i>7+10 4 + 13</i>

## AUXILIARY PROM ADDRESS STRAPPING (Using 2708 type PROM's)

ADDRESS RANGE	Jumper these pins together
0000 - 1FFF	U15-7 & U15-10      U15-5 & U15-12      U15-3 & U15-14
2000 - 3FFF	U15-7 & U15-10      U15-5 & U15-12      U15-4 & U15-13
4000 - 5FFF	U15-7 & U15-10      U15-6 & U15-11      U15-3 & U15-14 *
6000 - 7FFF	U15-7 & U15-10      U15-6 & U15-11      U15-4 & U15-13
8000 - 9FFF	U15-8 & U15-9      U15-5 & U15-12      U15-3 & U15-14
A000 - BFFF	U15-8 & U15-9      U15-5 & U15-12      U15-4 & U15-13
C000 - DFFF	U15-8 & U15-9      U15-6 & U15-11      U15-3 & U15-14
E000 - FFFF	U15-8 & U15-9      U15-6 & U15-11      U15-4 & U15-13

ADDRESS RANGE	Jumper these pins together
0000 - 1FFF	U15-7 & U15-10      U15-5 & U15-12      U15-3 & U15-14
2000 - 3FFF	U15-7 & U15-10      U15-5 & U15-12      U15-4 & U15-13
4000 - 5FFF	U15-7 & U15-10      U15-6 & U15-11      U15-3 & U15-14 *
6000 - 7FFF	U15-7 & U15-10      U15-6 & U15-11      U15-4 & U15-13
8000 - 9FFF	U15-8 & U15-9      U15-5 & U15-12      U15-3 & U15-14
A000 - BFFF	U15-8 & U15-9      U15-5 & U15-12      U15-4 & U15-13
C000 - DFFF	U15-8 & U15-9      U15-6 & U15-11      U15-3 & U15-14
E000 - FFFF	U15-8 & U15-9      U15-6 & U15-11      U15-4 & U15-13

\* = STANDARD JUMPERING SUPPLIED WITH THE BOARD

## I/O PAGE ADDRESS STRAPPING

15

U11 6-14 U11 7-11

## PAGE NUMBER

Jumper these pins together

	A15	A14	A13	A12
OE	U11-4 & U11-13	U12-2 & U12-15	U15-2 & U15-15	U11-5 & U11-12
1E	16 U11-4 & U11-13	U12-2 & U12-15	U15-2 & U15-15	U11-6 & U11-11
2E	U11-4 & U11-13	U12-2 & U12-15	U15-1 & U15-16	U11-5 & U11-12
3E	U11-4 & U11-13	U12-2 & U12-15	U15-1 & U15-16	U11-6 & U11-11
4E	U11-4 & U11-13	U12-1 & U12-16	U15-2 & U15-15	U11-5 & U11-12
5E	U11-4 & U11-13	U12-1 & U12-16	U15-2 & U15-15	U11-6 & U11-11
6E	U11-4 & U11-13	U12-1 & U12-16	U15-1 & U15-16	U11-5 & U11-12
7E	U11-4 & U11-13	U12-1 & U12-16	U15-1 & U15-16	U11-6 & U11-11
8E	U11-3 & U11-14	U12-2 & U12-15	U15-2 & U15-15	U11-5 & U11-12
9E	U11-3 & U11-14	U12-2 & U12-15	U15-2 & U15-15	U11-6 & U11-11
AE	U11-3 & U11-14	U12-2 & U12-15	U15-1 & U15-16	U11-5 & U11-12
BE	U11-3 & U11-14	U12-2 & U12-15	U15-1 & U15-16	U11-6 & U11-11
CE	U11-3 & U11-14	U12-1 & U12-16	U15-2 & U15-15	U11-5 & U11-12
DE	U11-3 & U11-14	U12-1 & U12-16	U15-2 & U15-15	U11-6 & U11-11
EE	U11-3 & U11-14	U12-1 & U12-16	U15-1 & U15-16	U11-5 & U11-12
FE	U11-3 & U11-14	U12-1 & U12-16	U15-1 & U15-16	U11-6 & U11-11 *

U11-7 ?

## I/O BASE ADDRESS STRAPPING

## BASE ADDRESS

Jumper these pins together

→00	U10-1 & U10-16	U10-3 & U10-14	U10-5 & U10-12	U10-7 & U10-10 *
10	U10-1 & U10-16	U10-3 & U10-14	U10-5 & U10-12	U10-8 & U10-9
20	U10-1 & U10-16	U10-3 & U10-14	U10-6 & U10-11	U10-7 & U10-10
30	U10-1 & U10-16	U10-3 & U10-14	U10-6 & U10-11	U10-8 & U10-9
40	U10-1 & U10-16	U10-4 & U10-13	U10-5 & U10-12	U10-7 & U10-10
50	U10-1 & U10-16	U10-4 & U10-13	U10-5 & U10-12	U10-8 & U10-9
60	U10-1 & U10-16	U10-4 & U10-13	U10-6 & U10-11	U10-7 & U10-10
70	U10-1 & U10-16	U10-4 & U10-13	U10-6 & U10-11	U10-8 & U10-9
80	U10-2 & U10-15	U10-3 & U10-14	U10-5 & U10-12	U10-7 & U10-10
90	U10-2 & U10-15	U10-3 & U10-14	U10-5 & U10-12	U10-8 & U10-9
A0	U10-2 & U10-15	U10-3 & U10-14	U10-6 & U10-11	U10-7 & U10-10
B0	U10-2 & U10-15	U10-3 & U10-14	U10-6 & U10-11	U10-8 & U10-9
C0	U10-2 & U10-15	U10-4 & U10-13	U10-5 & U10-12	U10-7 & U10-10
D0	U10-2 & U10-15	U10-4 & U10-13	U10-5 & U10-12	U10-8 & U10-9
E0	U10-2 & U10-15	U10-4 & U10-13	U10-6 & U10-11	U10-7 & U10-10
F0	U10-2 & U10-15	U10-4 & U10-13	U10-6 & U10-11	U10-8 & U10-9

PIA 1 Enable IRQ A U36-5 & U36-12  
 Enable IRQ B U36-7 & U36-10  
 CB1 to A-21 U36-4 & U36-13 \*  
 CB2 to A-22 U36-2 & U36-15 \*

PIA 2 Enable IRQ A U36-6 & U36-11  
 " " B U36-8 & U36-9

ACIA Carrier Detect from A-21 U36-3 & U36-14  
 Clear To Send from A-22 U36-1 & U36-16

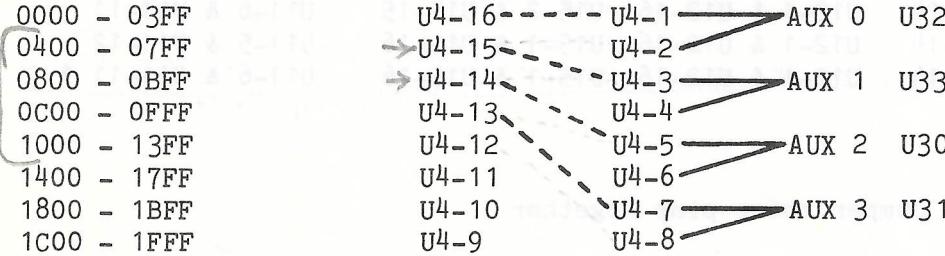
BAUD RATE (Be sure to select divide by 16 mode in ACIA)

75	U41-1 & U41-16	U41-3 & U41-14
110	U41-3 & U41-14	
150	U41-1 & U41-16	U41-4 & U41-13
300	U41-1 & U41-16	U41-8 & U41-9 *
600	U41-1 & U41-16	U41-7 & U41-10
1200	U41-1 & U41-16	U41-6 & U41-11
2400	U41-1 & U41-16	U41-5 & U41-12
4800	U41-1 & U41-16	U41-2 & U41-15

\* = Standard jumper supplied with assembled board.

The auxiliary PROM block was included to hold utility software such as I/O routines after the main PROM block is filled with BASIC or an assembler. It essentially works like the main PROM block except that only 4 PROM sockets are on the board. These 4 PROM's may be placed anywhere in the 8K block of addresses defined by the auxiliary PROM address jumpers listed on a previous page. In the table below, inserting a jumper will activate an auxiliary PROM socket and enable the bus drivers on the board to drive the bus when the socket is selected. If no jumpers are inserted, none of the auxiliary PROM sockets will be activated and the bus drivers will not be activated for any of the addresses in the auxiliary block. The standard jumper configuration assigns the 4 PROMS to the lower half of the 8K block defined by the auxiliary PROM address jumpers.

Address Range  
(Offset from AUX address) Standard jumpers shown



#### Conversion from 2708 PROMS to TMS-2716 (Multi-voltage type)

For the convenience of our customers and to insure a longer life for the product, the K-1012 offers the capability to use 16K EPROM's which hold 2K bytes each. Because of the wide availability and low cost of 2708 EPROM's however most users would want to use them. Thus the jumpers required for 2708 operation have been wired-in. Conversion to TMS2716 may be accomplished by cutting the 2708 traces and soldering in jumper wires as listed below. The main and auxiliary arrays may be independently converted but mixing of PROM's within the same array is not recommended. Note that when an array is converted that a 16K block of addresses is used and each PROM is worth 2K bytes.

#### To Convert the Main PROM Array to TMS2716

1. Remove jumper between U11-2 & U11-15
2. Solder in J6
3. Cut the following traces on the PCB: J8, J9, J12, J13, J16, J17, J20, J21, J32, J33, J36, J37, J40, J41, J44, J45
4. Solder in the following jumpers: J10, J11, J14, J15, J18, J19, J22, J23, J34, J35, J38, J39, J42, J43, J46, J47

#### To Convert the Auxiliary PROM Array to TMS2716

1. Remove jumper between U11-1 & U11-16
2. Solder in J7
3. If more than 4 TMS2716 are to be used, remove jumper from U12-13 or U12-14 and install a jumper from U12-14 to U12-11 or U12-12 whichever is open.
3. Cut the following traces on the PCB: J24, J25, J28, J29, J48, J49, J52, J53
4. Solder in the following jumpers: J26, J27, J30, J31, J50, J51, J54, J55

#### To Convert the PROM Programmer to TMS2716 (Be sure to read PROM programmer theory of operation after making this change)

1. Cut the following traces on the PCB: J1, J6
2. Solder in the following jumpers: J2, J3, J5

# SPECIFICATIONS

PROM Capacity - 12K using industry standard 2708, 24K using TMS2716 (multivoltage)  
 Parallel I/O - Four 8-bit ports and 8 handshaking lines, each bit of each port  
     may be programmed as an input or an output. Interrupt available  
     for each group of 8 bits. 6520 PIA chips are used.  
 Serial I/O - - Asynchronous, 5-8 data bits; even, odd, or no parity; 1 or 2 stop  
     bits. RTS, CTS, and CD modem control signals are provided. Baud  
     rates of 75, 110, 150, 300, 600, 1200, 2400, 4800 are provided  
     with an accuracy of .2% or better with a 1mHz system clock.  
     Serial data and modem signals are true RS-232 levels. A 6850 ACIA  
     chip is used.

PROM Programmer Can program standard 2708 EPROMS or with a jumper change, TMS2716  
 Access Time - - 550NS maximum as required by KIM-1 when using 450NS PROM's  
 Power Requirement - +7.5 volts unregulated .35 amp, +16 volts unregulated .25 amp.  
     +26 and -5 voltages required by the PROM's are generated on-board.  
 Addressing - - 8K of PROM must be contiguous on an 8K boundary, remaining 4K may  
     be scattered in a second 8K block. I/O requires 16 contiguous  
     addresses which can be placed anywhere in the next-to-last page of  
     any 4K block of addresses. IC sockets provided for all address  
     jumpers.  
 Buffering - - - Buffering for both address and data busses is provided. Maximum  
     bus load is 1 LS TTL gate input and one LS TTL tri-state output.  
 Physical Size - 7.5" X 11" exclusive of edge fingers. Two sets of 44 edge fingers  
     compatible with the KIM-1, SYM-1, or AIM-65 processors.

## PIN CONNECTIONS

EXPANSION CONNECTOR		APPLICATION CONNECTOR	
E-1	N.C.	E-A	GROUND
E-2	N.C.	E-B	ADDR BUS 0
E-3	N.C.	E-C	ADDR BUS 1
E-4	INT. REQ.	E-D	ADDR BUS 2
E-5	N.C.	E-E	ADDR BUS 3
E-6	N.C.	E-F	ADDR BUS 4
E-7	RESET	E-G	ADDR BUS 5
E-8	DATA BUS 7	E-H	ADDR BUS 6
E-9	DATA BUS 6	E-I	ADDR BUS 7
E-10	DATA BUS 5	E-J	ADDR BUS 8
E-11	DATA BUS 4	E-K	ADDR BUS 9
E-12	DATA BUS 3	E-L	ADDR BUS 10
E-13	DATA BUS 2	E-M	ADDR BUS 11
E-14	DATA BUS 1	E-N	ADDR BUS 12
E-15	DATA BUS 0	E-P	ADDR BUS 13
E-16	N.C.	E-Q	ADDR BUS 14
E-17	N.C.	E-R	ADDR BUS 15
E-18	+7.5 VOLTS IN	E-S	ADDR BUS 16
E-19	VECTOR FETCH	E-T	ADDR BUS 17
E-20	DECODE ENABLE	E-U	N.C.
E-21	N.C.	E-V	READ/WRITE
E-22	GROUND	E-W	N.C.
		E-X	+16 VOLTS IN
		E-Y	PHASE 2
		E-Z	N.C.
		A-1	EIA RTS
		A-2	PIA 2 CA1
		A-3	PIA 2 CA2
		A-4	PIA 1 PA0
		A-5	PIA 1 PA1
		A-6	PIA 1 PA2
		A-7	PIA 1 PA3
		A-8	PIA 1 PA4
		A-9	PIA 1 PA5
		A-10	PIA 1 PA6
		A-11	PIA 1 PA7
		A-12	PIA 1 PB0
		A-13	PIA 1 PB1
		A-14	PIA 1 PB2
		A-15	PIA 1 PB3
		A-16	PIA 1 PB4
		A-17	PIA 1 PB5
		A-18	PIA 1 PB6
		A-19	PIA 1 PB7
		A-20	(note 1)
		A-21	(note 2)
		A-22	PIA 2 CB1
			PIA 2 CB2
			A-Y
			A-Z

Note 1: A jumper selects between EIA CD and PIA 1 CB2      (PIA 1 CB2 is standard)  
 Note 2: A jumper selects between EIA CTS and PIA 1 CB1      (PIA 1 CB1 is standard)

## PROM PROGRAMMER OPERATION

The easiest way to use the PROM programmer on the K-1012 is to use the PROM programmer program listed in the back of this manual. The K-1012 is shipped with an ordinary but high quality 24 pin programming socket. If the board is to be used for extensive programming (over 100 PROM's), a zero-insertion-force socket (Textool or equivalent) wired to a short cable with 24 pin DIP plug and inserted into the programming socket is recommended.

1. Be sure the PROM is thoroughly erased. Germacidal or ozone lamps generally require 30 minutes (longer if the lamp is old) with the PROM placed 1 inch from the arc. New PROM's should be erased since their history is unknown.
2. Disconnect any peripheral devices connected to PIA 2 port A or bits 0-3 of port B that may be disturbed by random signals or which significantly load these lines.
3. Load the data to be programmed into RAM somewhere other than pages 0-3. Remember that all 1024 locations of the 2708 must be programmed at once; partial programming is not possible or safe for the PROM. Also note that the data need not reside at the same addresses that it will when the programmed PROM's are installed on the K-1012.
4. Load the PROM programmer program into RAM from the listing or optional cassette. If the 16 I/O addresses assigned to the K-1012 are not FE00 - FEOF, see the program listing for the necessary changes. The changes necessary for programming 2704's and TMS2716's are also shown in the listing.
5. With the program enable switch in the OFF position, insert the blank PROM into the programming socket. It is safe to do this with the power on. If the environment is dry, discharge your body to ground before plugging the PROM in.
6. Verify that the PROM is blank by executing NEWPRM (0200). Location 0000 will read FF if the PROM is indeed blank otherwise it will contain the contents of the non-blank cell and locations 0002 (L) and 0003 (H) will contain the PROM address of the non-blank location.
7. Set locations 0004 (L) and 0005 (H) to the RAM address containing the data to program.
8. Turn the program enable switch ON. DO NOT PRESS RESET WHILE THE SWITCH IS ON OR FALSE DATA MAY BE PROGRAMMED INTO THE PROM!
9. Execute PGMVFY (0203) to actually program the PROM. The program pulse LED should light during programming. Programming will require about 4 minutes after which the monitor should be re-entered. The PROM contents are compared against RAM after programming is complete. If this verify is successful, locations 0000 - 0003 will be 00. If not, location 0000 will contain the data actually in the PROM, location 0001 will contain the data that should have been in the PROM, and locations 0002 (low) and 0003 (high) will contain the RAM address of the data that did not program correctly.
10. Turn the program enable switch OFF. If the PROM verified, set aside for use later. If it did not verify write a question mark on it and restock unless it already has a question mark in which case it should be discarded or returned to the seller.

An unknown PROM may be compared against RAM contents by following steps 2-5 and 7 and then entering VERIFY (0206). This is the same routine that is executed after a programming cycle and it signals errors in the same manner.

A PROM may be copied by first reading it into RAM with READ (0209). Set up the RAM address in 0004 and 0005 and go to READ (0209). The original PROM may now be removed and a blank one installed. Follow the programming procedure outlined above to program the copy PROM. There is no danger of damaging the original PROM as long as the program enable switch is off.

## I/O PROGRAMMING TECHNIQUES

Both the parallel and the serial ports on the K-1012 use standard MOS interface chips. Full details about their operation and programming techniques is given in the manufacturer's specification sheets which are reproduced elsewhere in this manual. However several tips about their operation can be given here to get the user "up and running" quickly with a minimum of study.

### Parallel Ports

The two 6520 PIA chips provide 4 independent 8 bit ports plus 8 control lines. Each line of each port may be independently programmed for input or output although most applications would not mix functions on the same 8 bit port. Ports to be used as outputs must first be set up as outputs by writing all 1's into a special direction register. The 6520 does not address the direction register like the 6530 chips used on the KIM-1 or the 6522 chips used on the SYM-1 or AIM-65. Instead the direction registers share the same address as the data register. Selection between direction and data register addressing is controlled by bit 2 in the control register associated with each port. If bit 2 is a zero, the direction register is selected and if it is a one, the data register is selected. Thus initialization of a port for output would be accomplished by writing \$00 to the control register, writing \$FF to the direction/data register, and then writing \$04 to the control register. The port is now set up as an output and all of the extra functions of the 6520 are disabled. For inputs, it is only necessary to write \$04 to the control register; power up reset has already set the data direction register to zero. Like most MOS interface chips the contents of the data register may be read back thus allowing shifts and increment/decrement directly in the I/O register. However if the port A outputs are heavily loaded (such as by directly tying to transistor bases), the port cannot be read back accurately. Port B is buffered to prevent this problem.

The 6520 has many other functions available which allow very flexible control of the two control lines and interrupt request for each port. Consult the data sheet for detailed programming information.

FUNCTION	ADDRESS	FUNCTION	ADDRESS
PIA 1 port A data/direction	FE04	PIA 2 port A data/direction	FE08
PIA 1 port A control	FE05	PIA 2 port A control	FE09
PIA 1 port B data/direction	FE06	PIA 2 port B data/direction	FE0A
PIA 1 port B control	FE07	PIA 2 port B control	FE0B

(NOTE: PIA 2 drives the programmer)

### Serial Port

Full operation of the serial port is much simpler than the parallel ports. Only two addresses and 4 registers are involved. Address FE01 when written to is the transmit data register and when read is the receive data register. Address FE00 when written to is the control register and when read is the status register.

The first step in using the serial port is to set up the various transmission parameters. The standard setting is \$11 which gives 8 data bits, 2 stop bits, no parity, 16X clock, and interrupts disabled. Before writing this into the control register, a \$03 byte must be written to reset the chip. After configuration, bit 0 in the status register goes to a 1 when a data byte is received and goes back to zero when the receive data register is read. To transmit a byte it must be stored in the transmit data register. Bit 1 in the status register will then be set when the byte has been transmitted and another can be stored. The act of storing into the transmit data register will reset this bit.

The 6850 is also capable of numerous combinations of data bit count, parity generation/checking, 1X and 64X clock dividers, and independent receive and transmit interrupts. To use these functions effectively, consult the data sheet.

## APPLICATION INFORMATION

## INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

## REGISTER ADDRESSING

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RSO and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 - INTERNAL ADDRESSING

RS1	RS0	Control Register Bit		Location Selected
		CRA-2	CRB-2	
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

## CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 - CONTROL WORD FORMAT

CRA	7	6	5	4	3	2	1	0
	IRQA1	IRQA2	CA2 Control	DDRA	CA1 Control Access			
CRB	7	6	5	4	3	2	1	0
	IRQB1	IRQB2	CB2 Control	DDR B	CB1 Control Access			

## Data Direction Access Control Bit (CRA-2 and CRB-2)

– Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RSO and RS1.

## Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1)

– The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals IRQA and IRQB, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)		MPU Interrupt Request IRQA (IRQB)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled	– $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low	when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled	– $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low	when the interrupt flag bit CRA-7 (CRB-7) goes high

- NOTES:
1. ↑ indicates positive transition (low to high)
  2. ↓ indicates negative transition (high to low)
  3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
  4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, IRQA (IRQB) occurs on the positive transition of CRA-0 (CRB-0).

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an

interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS  
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)		MPU Interrupt Request IRQA (IRQB)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled	$\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low	when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled	$\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low	when the interrupt flag bit CRA-6 (CRB-6) goes high

- NOTES:
1. ↑ indicates positive transition (low to high)
  2. ↓ indicates negative transition (high to low)
  3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
  4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, IRQA (IRQB) occurs on the positive transition of CRA-3 (CRB-3).

**TABLE 5 – CONTROL OF CA2 AS AN OUTPUT  
CRA-5 is high**

CRA-5	CRA-4	CRA-3	CA2	
			Cleared	Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High on an active transition of the CA1 signal
1	0	1	Low immediately after an MPU Read "A" Data operation.	High on the negative edge of the next "E" pulse.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write in Control Register "A".	Always low as long as CRA-3 is low.
1	1	1	Always high as long as CRA-3 is high	High when CRA-3 goes high as a result of a Write in Control Register "A".

**TABLE 6 – CONTROL OF CB2 AS AN OUTPUT  
CRB-5 is high**

CRB-5	CRB-4	CRB-3	CB2	
			Cleared	Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal
1	0	1	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High on the positive transition of the next "E" pulse.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU write into control register "B".

**Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) –**  
The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Status lines when those lines are programmed to be interrupt inputs. These

bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

## APPLICATION INFORMATION

**INTERNAL REGISTERS**—The ACIA has four internal registers utilized for status, control, receiving data, and transmitting data. The register addressing by the R/W and RS lines and the bit definitions for each register are shown in Figure 4.

FIGURE 4 – DEFINITION OF ACIA REGISTERS

	BUFFER ADDRESS			
	RS • $\overline{R/W}$	RS • R/W	$\overline{RS} • \overline{R/W}$	$\overline{RS} • R/W$
Data Bus Line Number	Transmit Data Register	Receiver Data Register	Control Register	Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0*	Clk. Divide Sel. (CR0)	Rx Data Reg. Full (RDRF)
1	Data Bit 1	Data Bit 1	Clk. Divide Sel. (CR1)	Tx Data Reg. Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Sel. 1 (CR2)	Data Carrier Det. loss (DCD)
3	Data Bit 3	Data Bit 3	Word Sel. 2 (CR3)	Clear-to-Send (CTS)
4	Data Bit 4	Data Bit 4	Word Sel. 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Tx Control 1 (CR5)	Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Tx Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Rx Interrupt Enable (CR7)	Interrupt Request (IRQ)

## Notes:

- \* Leading bit = LSB = Bit 0
- \*\* Unused data bits in received character will be "0's."
- \*\*\* Unused data bits for transmission are "don't care's."

**ACIA STATUS REGISTER**—Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This Read Only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of: transmitting data register, the receiving data register and error status and the modem status inputs of the ACIA.

**Receiver Data Register Full (RDRF) [Bit 0]**—Receiver Data Register Full indicates that received data has been transferred to the Receiver Data Register. RDRF is cleared after an MPU read of the Receiver Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receiver Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

**Transmit Data Register Empty (TDRE) [Bit 1]**—The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

**Data Carrier Detect ( $\overline{DCD}$ ) [Bit 2]**—The Data Carrier Detect bit will be high when the  $\overline{DCD}$  input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated if the Receiver Interrupt Enable (RIE) is set. It remains high until the interrupt is cleared by reading the Status Register and the data register or a Master Reset occurs. If the  $\overline{DCD}$  input remains high after Read Status and Read Data or Master Reset have occurred, the  $\overline{DCD}$  Status bit remains high and will follow the  $\overline{DCD}$  input.

**Clear-to-Send ( $\overline{CTS}$ ) [Bit 3]**—The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low  $\overline{CTS}$  indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master Reset does not affect the Clear-to-Send status bit.

**Framing Error (FE) [Bit 4]**—Framing error indicates that the received character is improperly framed by the start and stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receiver data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

**Receiver Overrun (OVRN) [Bit 5]**—Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receiver Data Register

(RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until Overrun is reset. Character synchronization is maintained during the Overrun condition. The overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

**Parity Error (PE) [Bit 6]**—The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

**Interrupt Request ( $\overline{IRQ}$ ) [Bit 7]**—The IRQ bit indicates the state of the  $\overline{IRQ}$  output. Any interrupt that is set and enabled will be indicated in the status register. Any time the  $\overline{IRQ}$  output is low the IRQ bit will be high to indicate the interrupt or service request status.

**CONTROL REGISTER**—The ACIA control Register consists of eight bits of write only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send modem control output.

**Counter Divide Select Bits (CR0 and CR1)**—The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a Master Reset for the ACIA which clears the Status Register and initializes both the receiver and transmitter. Note that after a power-on or a power-fail restart, these bits must be set High to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	$\div 1$
→ 0	1	$\div 16$
1	0	$\div 64$
1	1	Master Reset

**Word Select Bits (CR2, CR3, and CR4)**—The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bit
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
→ 1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not double-buffered and therefore become effective immediately.

**Transmitter Control Bits (CR5 and CR6)**—Two Transmitter Control bits provide for the control of the Transmitter Buffer Empty interrupt output, the Request-to-Send output and the transmission of a BREAK level (space). The following encoding format is used:

CR6	CR5	Function
→ 0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmitting Interrupt Disabled and Transmits a BREAK level on the Transmit Data Output.

**Receiver Interrupt Enable Bit (RIE) (CR7)**—Interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts caused by the Receiver Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line are enabled or disabled by the Receiver Interrupt Enable Bit.

**TRANSMIT DATA REGISTER (TDR)**—Data is written in the Transmitter Data Register *during* the peripheral enable time (E) when the ACIA has been addressed and RS • R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the status register to go low. Data can then be transmitted. If the transmitter is idling and no

character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

**RECEIVE DATA REGISTER (RDR)**—Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receiver Data Register Full bit (RDRF) (in the status buffer) to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receiver Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receiver Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

## OPERATIONAL DESCRIPTION

From the MPU Bus interface the ACIA appears as two addressable RAM memory locations. Internally, there are four registers; two read-only and two write-only registers. The read-only registers are status and receive data, and the write only registers are control and transmit data. The serial interface consists of serial transmit and receive lines and three modem/peripheral control lines.

During a power-on sequence, the ACIA is internally latched in a reset condition to prevent erroneous output transitions. This power-on reset latch can only be released by the master reset function via the control register; bits b<sub>0</sub> and b<sub>1</sub> are set "high" for a master reset. After master resetting the ACIA, the programmable control register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none) and etc.

**TRANSMITTER**—A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmitter Data Register if the status read operation has indicated that the Transmitter Data

Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence continues until all the characters have been transmitted.

**RECEIVER**—Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an externally synchronized clock (to its data) while the divide by 16 and 64 ratios are provided for internal synchronization.

Bit synchronization in the divide by 16 and 64 modes is obtained by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

## PRINCIPLES OF OPERATION

Although the K-1012 PROM/IO board is large and has a lot of components, its design and operation are relatively simple. Looking at the block diagram the board is seen to consist of a bus buffer, address decoder, main PROM block, auxiliary PROM block, parallel I/O block, serial I/O block, on-board power supply, and PROM programmer.

The address and data busses are buffered by the bus buffer block. The address buffer is simple since it is unidirectional but the data buffer must be bidirectional. In particular the data out drivers must only be activated during read cycles to valid K-1012 addresses.

The address decoder establishes the range of memory addresses assigned to the two PROM blocks and the I/O blocks. Each of these three address ranges has its own independent address decoder. Another function of the address decoder is to provide the VECTOR FETCH and DECODE ENABLE signals needed by the KIM-1 when external memory is added. These signals serve no function with the SYM-1 and AIM-65 processors.

The main and auxiliary PROM blocks combined hold 12 PROMS; 8 in the main block and 4 in the auxiliary block. These blocks are independently enabled by their corresponding address decoder. The auxiliary PROM block, since it is not completely filled, feeds an enable signal back to the bus buffers only when a PROM actually responds to an address. Any addresses within the auxiliary block range that do not actually activate a PROM will not activate the data out drivers. Discrete circuitry within the two PROM blocks applies power to a PROM only when it is addressed thus drastically reducing power consumption.

The two I/O blocks are enabled by the address decoder when one of the 16 I/O addresses is referenced. Although there are only 10 unique I/O addresses, 16 are occupied (4 give undefined results and 2 are duplicated). The parallel I/O chips are just tied to the application edge fingers. The serial I/O chip's TTL levels are converted to/from EIA levels by discrete circuitry. All of the interrupt request signals from the I/O chips may be wire-ored together (via jumpers) and connected to the IRQ bus line. The baud rate generator for the serial port is implemented with a programmable counter driven by the system clock which is assumed to be crystal controlled at 1mHz.

The on-board power supply converts the +8 and +16 volt unregulated inputs to +5 and +12 volts regulated for the logic and PROM's. A charge pump circuit driven at the system clock frequency provides -5 volts regulated for the PROM's and an unregulated voltage of about 35 volts for the PROM programmer. The 35 volts is stored on a capacitor which then supplies the surge currents necessary during programming.

The PROM programmer is driven by part of the parallel I/O block. Eight bits are used to interface to the 8 data lines thus allowing the PROM to be read as well as programmed. Four additional bits are used to control the address counter and initiate program pulses. Although software determines the timing of the programming sequence, a fail-safe circuit protects the PROM from software crashes.

### Bus Buffers and Address Decoder

The majority of the bus interface circuitry is on page 2 of the detailed schematic drawings. Some of the 16 address lines are buffered by AND gates with the unused input tied high while those that must be available in true and complement form for the address decoder are run through two series inverters. All of these gates are low power Schottky to minimize bus loading without delaying the signals appreciably. U19, U21, and U22 are non-inverting tri-state buffers which are interconnected to form a bidirectional transceiver for the data bus. Because of U5-11, which is connected as an inverter, the transceiver is set to always receive bus data except when it is called upon to actually drive bus data. Again the LS version of these buffers is used to minimize bus loading and noise. The drive capability is fairly low which keeps switching noise down.

The mass of logic at the upper right of the diagram is the address decoder. U9-8 and U9-6 are the auxiliary and main PROM block decodes respectively. Since either block of addresses is 8K and must be on an 8K boundary, only A13 - A15 needs to be considered. Jumpers in the U15 and U12 area select the desired combination of true and complement A13 - A15 lines for the desired address block. If TMS-2716 PROMS are being used in the main array and it is desired to increase the block size to 16K, then the A13 jumper should be omitted and U9-3 should be jumpered to U9-5.

The block of 16 addresses used by the I/O circuitry is detected in two stages. The first stage is the detection of the I/O page address. It is assumed that the user desires to have I/O registers throughout the system (excluding those that are part of the processor board) all reside in the same memory page which is tucked away in a corner away from mainstream memory. U8 is used to detect this I/O page. The connections to A8 - A11 are fixed as E (hexadecimal) but jumpers select the connections to A12 - A15. Thus the I/O page may be set to XE where X is any hexadecimal digit. In KIM-1 systems X must be F if the VECTOR FETCH and DECODE ENABLE signals are to be used. In other systems X can be anything but the user must be careful to avoid interference with addresses on the processor board or other expansion boards or other portions of the K-1012 board. U7 implements the second stage of I/O address recognition. When enabled by U8 through inverter U5-3, it looks at A4 - A7 which can be jumpered in any combination of true and complement.

The DECODE ENABLE signal for the KIM-1 simply looks for A13 - A15 to be 000. When this combination is detected, the DECODE ENABLE line is driven low which then activates memory circuitry on-board the KIM-1. By convention VECTOR FETCH must be pulled low when one of the vector locations (FFFA-FFFF) is accessed by the processor. To simplify decoding circuitry, MTU boards broaden the range to include all addresses between FF00 to FFFF, i.e., page FF. Open-collector gate U2-3 in conjunction with the I/O page decoder detects page FF and pulls VECTOR FETCH down as required. For this to work properly, the I/O page must be set to FE. If the KIM-1 user desires the I/O page elsewhere, U2-3 must be disconnected from the bus and the system must have either another MTU board installed or the user must provide for the VECTOR FETCH function.

Further address decoding for the PROM's is accomplished on page 1 by decoders U1 and U3. Each decoder is activated by its respective PROM ARRAY ENABLE and looks at A10 - A12 to produce 8 mutually exclusive outputs which in turn enable particular PROM's. J6 and J7, which switches the decoder A input between A10 and A13, is used to convert between 2708 and TMS2716 PROM's. U4 is a jumper socket for the auxiliary PROM array. For every prom installed in this array, a jumper must be inserted to connect the PROM's chip enable to a decoder output.

Final address decoding for the two PIA chips and the ACIA chip is done with their multiple chip select inputs. The ACIA responds when A2 and A3 are both low thus it occupies the lowest 4 locations within the 16 I/O address block. PIA 1 responds when A2 is low and A3 is high and PIA 2 responds to the converse situation. Nothing responds when A2 and A3 are both high.

The function of U6 is to logical OR all of the enable signals generated by address decoding so that the data bus buffer is properly controlled. This OR function is then ANDed with read/write so that the bus buffer is turned around only during read cycles to an address on-board. Note that there is individual feedback from the auxiliary PROM block so that the bus is not driven when a non-existent auxiliary PROM is addressed.

Connection to the PROM's is quite straightforward. Essentially they are chip selected by the address decoder and look at A0 - A9 for final addressing. The power-down circuit is unique however. When chip select goes down on a PROM, the PNP transistor in series with its +12 lead is turned on by base drive through the series 1K resistor and 9.1V zener diode. The zener diode provides logic level shifting so that a 3 volt logic signal can drive the base at +12 potential. It is important when deselecting a PROM that chip select go high a couple of hundred NS before power is removed; if this is not done, the PROM will remain selected and drive its outputs for several milliseconds until internal nodes discharge. This delay is provided by the storage time of the PN/2N2907 transistors used. If a substitution is made, gold doped high speed switches must be avoided. The small amount of leakage that occurs with no resistor between base and emitter is of no consequence. The bleeder resistor shown between emitter and collector is not normally installed on the board. A resistor in the 1K to 3K range can be installed if the PROM's have unusually slow power-up characteristics or a short circuit will bypass power switching altogether. If the power down circuit is bypassed, only 8 PROM's can be used without overloading the power supply circuits.

#### Parallel I/O

The parallel I/O circuitry is a model of simplicity. The three chip select inputs on the 6520 (identical to the Motorola 6820) PIA chips are used as the final level of address decoding and A0 and A1 are used to select among the 4 internal addresses. For PIA 2, all 20 of the peripheral lines are routed straight to edge fingers. Only 18 from PIA 1 are wired directly but the other two (CB1 and CB2) may be jumpered to edge fingers if modem control signals on the serial port are not needed. The interrupt request outputs from the PIA chips may be individually jumpered onto the IRQ bus line. These jumpers are left out of factory assembled units to avoid possible confusion of inexperienced programmers.

Note that port A of PIA 2 is connected to the PROM programmer socket. However if no PROM is plugged in, there is no load on these lines. PB0 through PB3 also go into the programmer circuitry. PB2 and PB3 are not loaded since they drive CMOS. PB1 is loaded by 1LS TTL load which is about 1/5 of its drive capability. PB0 however is loaded such that 1-to-0 transitions after being in the 1 state for a long time are likely to be slow. In any case, when programming PROM's all external connections to these lines should be removed.

#### Serial I/O

Serial I/O capability is provided by a 6850 ACIA chip. It is addressed like the PIA chips but only A0 is looked at since there are only two internal registers to select. The chip however provides and accepts TTL logic levels while standard serial interfaces accept and provide EIA logic levels which swing between -5 and +5 volts minimum. The transistor circuits using Q22 - Q24 translate such input levels to TTL for the PIA chip. These inputs will withstand up to  $\pm 30$  volts but will also accept TTL level inputs. The 10K pullups on the carrier detect and clear-to-send inputs insure normal operation of the ACIA when these modem control signals are not used.

U39, which is a dual op-amp, provides very inexpensive and low power conversion from TTL levels to EIA levels. Essentially the op-amps are wired as comparators with a 2.5 volt threshold. The slew rate limit of the internally compensated amplifiers also provides a controlled rise and fall time of about 25 uS.

The baud rate generator consists of programmable counter U37 and post divider U38. U37 divides the 1mHz system clock by either 9 or 13 according to a jumper setting. In operation the counter is preset to 7 for divide by 9 or 3 for divide by 13. It then counts up at a 1mHz rate until it reaches 15. The next clock pulse will preset it again through the terminal count output and U44-11. U38 is a simple ripple counter and jumpers tap off various frequencies for the ACIA.

## Power Supply

The majority of the power supply is on page 2. Unregulated +8 and +16 volt inputs are regulated to +5 and +12 volts by VR3 and VR2 respectively. Each regulator has input capacitors to prevent oscillation and output capacitors to absorb large transient currents. The 1000uF input capacitor on the +16 volt line provides the additional filtering required when using our K-1000 series power supplies.

A charge pump circuit supplies negative and high positive voltages to the PROM's and PROM programmer. U2 and Q1 and Q2 provide a low impedance 12 volt square wave at the 1mHz system clock frequency. Pullup resistor R1 being returned to +16 volts insures adequate base drive to Q2 so that a full 12 volt swing is achieved even with heavy loads. D1, D2, C20, and C22 form a familiar half-wave voltage doubler circuit. The negative output voltage is achieved by returning D1's cathode to ground. C20 develops a charge of approximately -8 to -10 volts which then feeds VR1 to be regulated to -5 volts. C34 is a high frequency input bypass for VR1 which prevents oscillation.

On page 3 is another charge pump circuit configured as a parallel voltage quadrupler. Its operation is similar to the negative power supply except that "common" is returned to +12 volts and there are two complete doubler stages. In operation C28 accumulates a charge of +35 volts which is used by the PROM programmer.

## PROM Programmer

The PROM programmer is in the upper right corner of page 3. It consists of programming socket U34, address counter U35 and high voltage program pulse circuitry. The 8 data lines of U34 are tied directly to one of the parallel ports. Since the port may be set up for either input or output, the PROM may be both written and read without moving it out of the programming socket.

Address counter U35 provides sequential addressing of the 1024 locations in the PROM. The counter may be incremented and reset through 2 I/O port bits. This single chip CMOS counter saves considerable circuitry and tends to enforce sequential programming of the PROM in "passes" as recommended by the manufacturer.

The chip select input to the PROM requires special attention. For a 2708, +5 volts deselects the chip and ground selects it for reading. Positive 12 volts readies it for programming. Since the programming socket never needs to be deselected, this pin is driven between +12 and ground by U44-3. For a 2716, this pin is the 11<sup>th</sup> address pin so it is jumpered to the address counter instead. The write enable pin is the +5 supply to the chip. When reading, +5 volts is supplied by emitter follower Q16 which is saturated by the 12 volt drive of U44-3 and R37. When programming, this pin is solidly grounded by Q15, another emitter follower.

By far the most critical input to the PROM is the program pulse. This pulse must be +26 volts in amplitude to close tolerances and must be able to sink current when in the zero voltage state. Furthermore, the rise and fall times must be controlled and a current limit circuit should be included to prevent the PROM from drawing too much current during programming. The 5 transistor circuit using Q17 - Q22 has all of these properties. The Q17-Q18 combination is a current limited switch to the +35 volt power supply. A current limit threshold of about 20mA is reached when the voltage drop across R34 reaches .6 volts. Q19 and Q20 form a similar current limited switch to ground. When Q21 is off, which is the normal situation, current through R33, R32, and R35 turns Q20 on to ground the program pin. There is insufficient voltage drop across R33 in this situation to turn Q18 on. When Q21 is turned on for a program pulse, base current to Q20 is cut off and the three times greater current flow through R33 now turns Q18 on. C27 and the 20mA current limit provides a controlled voltage rise time of 1.2uS. The pulse amplitude is clamped at +26 volts by D15 and LED 1. Fall time is also controlled since Q20 is part of a current limited circuit. C29 and C30 limit how long Q21 can be continuously energized and therefore provide a fail-safe function.

## TROUBLESHOOTING

Factory assembled K-1012 boards have been carefully checked out and burned-in prior to shipment. However because of the scores of jumper options available, some of which involve PC trace cutting, it is impossible to test 100% of the board functions. Also since the customer supplies the PROM's, we have no control over their quality. If at all possible the customer should test the board as received with no jumper changes to avoid confusion.

In the event of trouble first give the board a thorough visual inspection. Unclipped excess component leads may have bent over and shorted during shipment. A poor solder connection might have opened during shipping vibration. Check that all of the standard jumpers are in place and not shorting against each other. It goes without saying that all connections between the processor board and the K-1012 should be checked. In particular a heavy ground lead (braid, large PC foil area, or #18 hookup wire) should be used and the bus wire lengths should not exceed 4 inches.

Following this the first area to check is the power supply. The incoming power should read a minimum of +8 and +15 volts with a voltmeter. If an oscilloscope is available, the negative peak of the ripple waveform must not drop below +7 and +14 volts. Next check the output of the positive regulators. If the heatsink is blazing hot and one of the regulated voltages is low or zero, suspect a short, possibly through a user supplied PROM. Check the -5 volt output. If it is low or zero and the regulator is even warm, suspect a short, again most likely through a user supplied PROM. If it is zero and the regulator is cold, the trouble is in the charge pump circuit. If the PROM programmer does not function, check the +35 volt programming supply. When not programming it should be at least +32 volts.

Addressing problems can be tracked down by noting which addresses the board does respond to. With most processors and monitors, a non-existent address will read back the page number of the non-existent address (this is due to the operation sequence of indirect addressing). If it responds to too many addresses (for example, I/O can be addressed at two different places), then either an address selection jumper is missing or a PC trace is open. This problem would most likely occur after the jumpers had been reconfigured by the user.

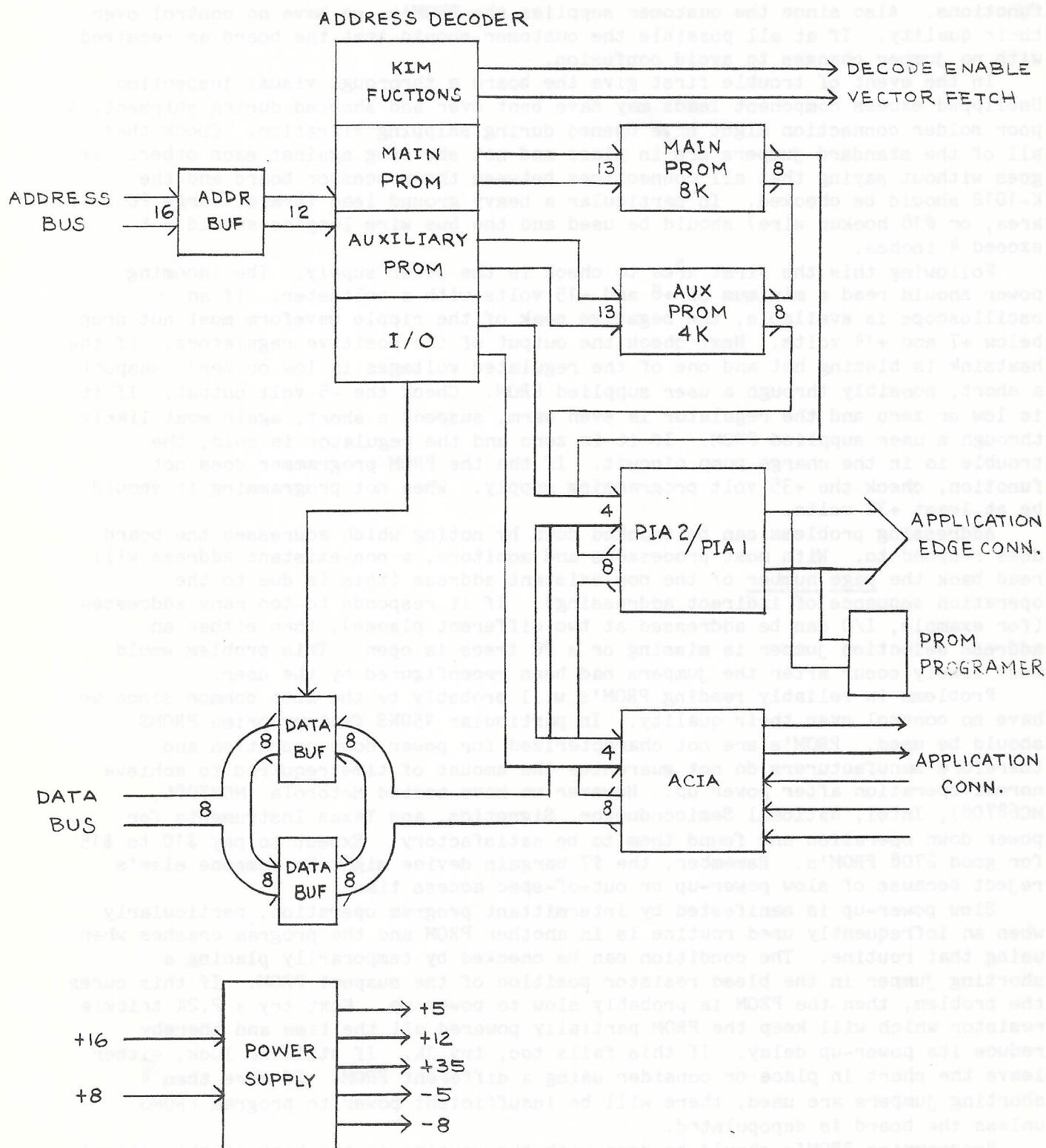
Problems in reliably reading PROM's will probably be the most common since we have no control over their quality. In particular 450NS factory prime PROMS should be used. PROM's are not characterized for power down operation and therefore manufacturers do not guarantee the amount of time required to achieve normal operation after power up. However we have tested Motorola (MC2708L, MC68708), Intel, National Semiconductor, Signetics, and Texas Instruments for power down operation and found them to be satisfactory. Expect to pay \$10 to \$15 for good 2708 PROM's. Remember, the \$7 bargain device might be someone else's reject because of slow power-up or out-of-spec access time.

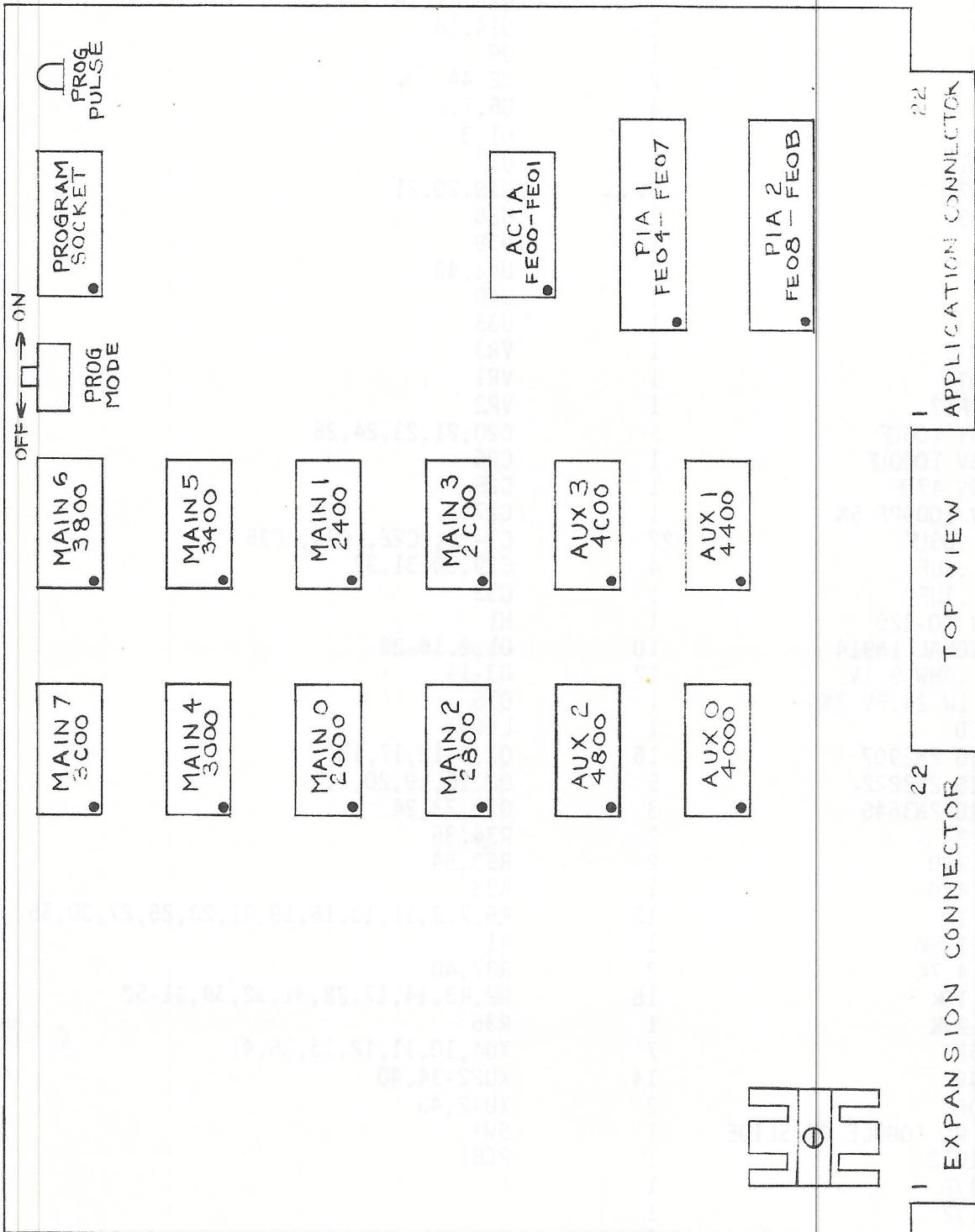
Slow power-up is manifested by intermittent program operation, particularly when an infrequently used routine is in another PROM and the program crashes when using that routine. The condition can be checked by temporarily placing a shorting jumper in the bleed resistor position of the suspect PROM. If this cures the problem, then the PROM is probably slow to power up. Next try a 2.2K trickle resistor which will keep the PROM partially powered all the time and thereby reduce its power-up delay. If this fails too, try 1K. If still no luck, either leave the short in place or consider using a different PROM. If more than 4 shorting jumpers are used, there will be insufficient power to program PROMS unless the board is depopulated.

Programming PROM's should be done with the routine in the back of this manual. This program conforms exactly to the manufacturer's specifications and should program the PROM's thoroughly. Most programming problems are caused by incomplete erasure. PROM's being erased should be rotated once during erasure to overcome the effects of possible shadows from scratches or bits of label on the window.

If the customer cannot find the problem or is unable to repair it, return the board to the factory for repair, preferably with the customer's PROM's in place.

## K-1012 BLOCK DIAGRAM





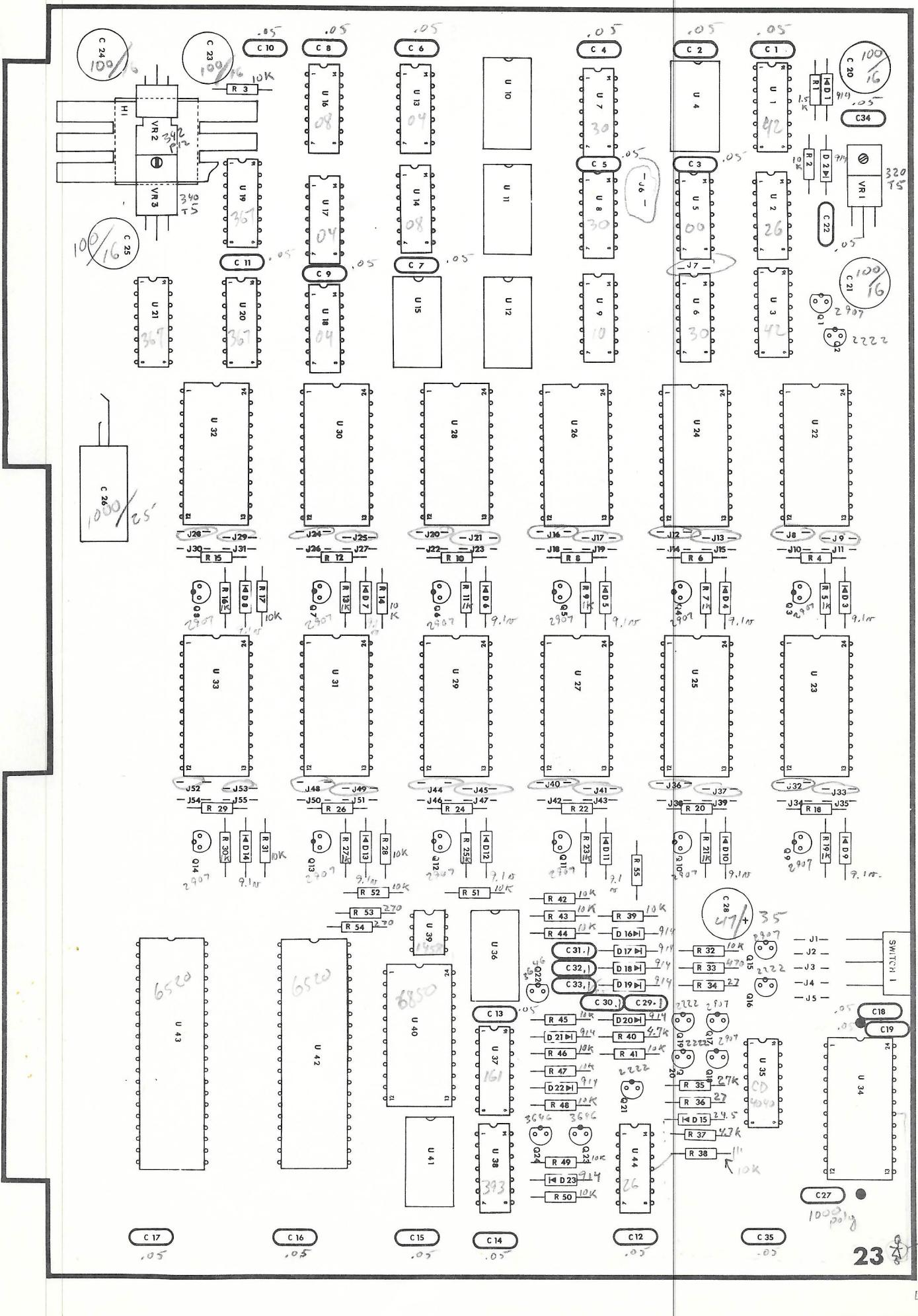
NOTE : ADDRESSES SHOWN ARE WITH THE STANDARD JUMPER CONFIGURATION

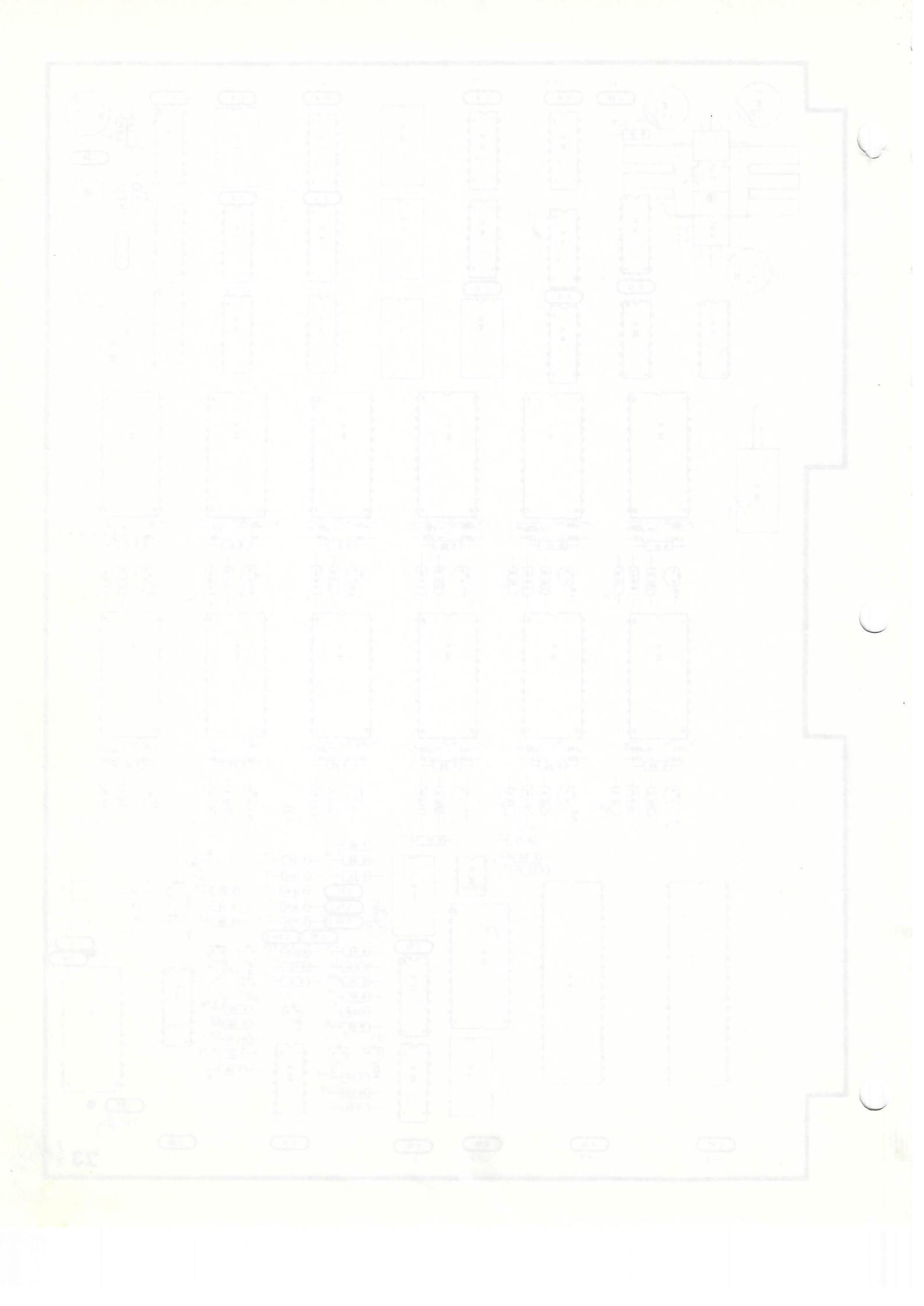
K-1012 PARTS LIST

PART DESCRIPTION	QUANTITY	DESIGNATORS
LOGIC 74LS00	1 ✓	U5
LOGIC 74LS04	3 ✓	U13, 17, 18
LOGIC 74LS08	2 ✓	U14, 16
LOGIC 74LS10	1	U9
LOGIC 74LS26	2 ✓✓	U2, 44
LOGIC 74LS30	3 ✓✓✓	U6, 7, 8
LOGIC 74LS42	2 ✓✓	U1, 3
LOGIC 74LS161	1	U37
LOGIC 74LS367	3 ✓✓✓	U19, 20, 21
LOGIC 74LS393	1	U38
LOGIC 1458	1	U39
LOGIC 6520	2	U42, 43
LOGIC 6850	1	U40
LOGIC CD4040	1	U35
VOLT REG 340T5	1	VR3
VOLT REG 320T5	1	VR1
VOLT REG 342P12	1	VR2
CAP ELECT 16V 100UF	5	C20, 21, 23, 24, 25
CAP ELECT 25V 1000UF	1	C26
CAP ELECT 35V 47UF	1	C28
CAP POLY 25V 1000PF 5%	1	C27
CAP Z5U 12V .05UF	22	C1-19, C22, C34, C35
CAP Z5U 12V .1UF	4	C29, 30, 31, 32
CAP Z5U 25V .1UF	1	C33
HEAT SINK 1W TO-220	1	H1
DIODE SIL SIGNAL 1N914	10	D1, 2, 16-23
DIODE ZENER .4MW 9.1V	12 ✓✓✓✓	D3-14
DIODE ZENER 1W 24.5V 2%	1 ✓	D15
DIODE LED RED	1	LED-1
TRANS PNP SIG 2N2907	16	Q1, 3-15, 17, 18
TRANS NPN SIG 2N2222	5	Q2, 16, 19, 20, 21
TRANS NPN SIG 2N3646	3	Q22, 23, 24
RES 1/4W 5% 27	2 ✓✓	R34, 36
RES 1/4W 5% 270	2 ✓✓	R53, 54
RES 1/4W 5% 470	1 ✓	R33
RES 1/4W 5% 1K	13 ✓	R5, 7, 9, 11, 13, 16, 19, 21, 23, 25, 27, 30, 55?
RES 1/4W 5% 1.5K	1 ✓	R1
RES 1/4W 5% 4.7K	2 ✓	R37, 40
RES 1/4W 5% 10K	18 ✓	R2, R3, 14, 17, 28, 31, 32, 39, 41-52
RES 1/4W 5% 27K	1 ✓	R35
SOCKET PC 16P	7 ✓	XU4, 10, 11, 12, 15, 36, 41
SOCKET PC 24P	14 ✓	XU22-34, 40
SOCKET PC 40P	2 ✓	XU42, 43
SWITCH SPST PC TOGGLE OR SLIDE	1	SW1
PC BOARD K-1012	1	PCB1
SCREW 4-40 3/8	1	
SCREW 4-40 1/2	1	
NUT 4-40	2	
WASHER, FIBRE 4-40	1	

TRICKLE RESISTORS ON PROMS  
IF NEEDED

R4, 6, 8, 10, 12, 15, 18, 20, 22, 24, 26, 29









# PROGRAMMING

Programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

## Absolute Maximum Ratings\*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
$V_{CC}$ With Respect to $V_{BB}$	+20V to -0.3V
$V_{DD}$ and $V_{SS}$ With Respect to $V_{BB}$	+15V to -0.3V
All Input or Output Voltages With Respect to $V_{BB}$ During Read	+15V to -0.3V
CS/WE Input With Respect to $V_{BB}$ During Programming	+20V to -0.3V
Program Input With Respect to $V_{BB}$	+35V to -0.3V
Power Dissipation	1.5W

### \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## READ OPERATION

### D.C. and Operating Characteristics

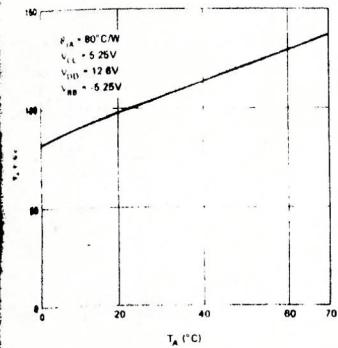
0°C to 70°C,  $V_{CC} = +5V \pm 5\%$ ,  $V_{DD} = +12V \pm 5\%$ ,  $V_{BB}^{[1]} = -5V \pm 5\%$ ,  $V_{SS} = 0V$ , unless otherwise noted.

Symbol	Parameter	Min.	Typ. <sup>[2]</sup>	Max.	Unit	Conditions
	Address and Chip Select Input Sink Current		1	10	µA	$V_{IN} = 5.25V$ or $V_{IN} = V_{IL}$
	Output Leakage Current		1	10	µA	$V_{OUT} = 5.5V$ , CS/WE = 5V
	$V_{DD}$ Supply Current	50	65	mA		Worst Case Supply Currents:
	$V_{CC}$ Supply Current	6	10	mA		All Inputs High
	$V_{BB}$ Supply Current	30	45	mA		CS/WE = 5V; $T_A = 0^\circ C$
	Input Low Voltage	$V_{SS}$	0.65	V		
	Input High Voltage	3.0	$V_{CC} + 1$	V		
	Output Low Voltage		0.45	V	$I_{OL}$	1.6mA
	$V_{OH1}$	3.7		V	$I_{OH1}$	100µA
	$V_{OH2}$	2.4		V	$I_{OH2}$	1mA
	Power Dissipation		800	mW		$T_A = 70^\circ C$

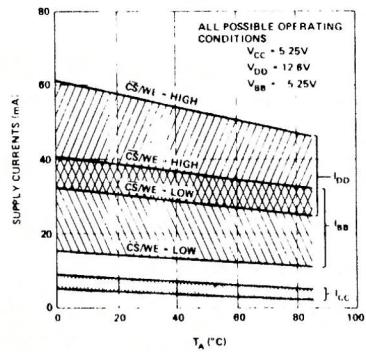
- NOTES. 1.  $V_{BB}$  must be applied prior to  $V_{CC}$  and  $V_{DD}$ .  $V_{BB}$  must also be the last power supply switched off.  
 2. Typical values are for  $T_A = 25^\circ C$  and nominal supply voltages.  
 3. The total power dissipation of the 2704/2708 is specified at 800 mW. It is not calculated by summing the various currents ( $I_{DD}$ ,  $I_{CC}$ , and  $I_{BB}$ ) multiplied by their respective voltages since current paths exist between the various power supplies and  $V_{SS}$ . The  $I_{DD}$ ,  $I_{CC}$ , and  $I_{BB}$  currents should be used to determine power supply capacity only.

### Typical Characteristics

MAXIMUM JUNCTION TEMPERATURE VS. AMBIENT TEMPERATURE



RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE

