CMSC 411 – Homework #2 – 2/10/2014

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[12 points] Acronyms

ALU	Arithmetic Logic Unit
CISC	Complex Instruction Set Computer
CPI	Cycles Per Instruction
CPU	Central Processing Unit
FP	Floating Point
MIPS	Million Instructions per Second
MFLOPS	Million floating point operations per second
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
SIMD	Single Instruction, Multiple Data
MOS	Metal Oxide Semiconductor
FET	Field Effect Transistor

[50 points] Definitions

Server

A computer used for running larger applications for multiple users, often simultaneously, and typically accessed only via a network.

Embedded Computer

A computer inside another device used for running one predetermined application or collection of software.

Supercomputers

A class of computer with the highest performance and cost; they are configured as servers and typically cost tens of hundreds of millions of dollars.

VHDL

Acronym for VHSIC (Very High Speed Integrated Circuit) Hardware Description Language. A high level language based off of Ada, that provides an abstract description of the hardware to simulate and debug the design.

Compiler

A program that takes a high level language as input and reduces it to some form that a computer or VM is able to interpret.

Assembler

A program that takes assembly language, and reduces it to binary or machine code.

Assembly Code

A symbolic language that can be translated into machine language. Easier to read, write

and debug than binary.

Machine Language

A binary representation understood by computers.

Application Software

Software that end-users use to do work, not including the operating system, or compiler.

Examples include word processors and text editors.

System Software

Software that provides services that are commonly useful, includng operating systems, compilers, loaders and assemblers.

[20 points] CPI/MIPS

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 950 MHz and M2 has a clock rate of 1200 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 – Cycles/Instruction Class	Machine M2 – Cycles/Instruction Class	Frequency
A	1	2	50%
B	2	1	35%
C	5	4	15%

(a) Calculate the average CPI for each machine, M1, and M2.

M1: 1 * 0.5 + 2 * 0.35 + 5 * 0.15 = 1.95 CPI
M2: 2 * 0.5 + 1 * 0.35 + 4 * 0.15 = 1.95 CPI

(b) Calculate the average MIPS ratings for each machine, M1 and M2.

M1: 950 MHz / 1.95 * 10^6 ~ 487 MIPS
M2: 1200 MHz / 1.95 * 10^6 ~ 615 MIPS

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[18 points] Pipelines
The design team for a simple, single-issue processor is choosing between two pipelined implementations. Here are some design parameters for the two possibilities:

	A	B
Clock Rate	700MHz	500 MHz
CPI for ALU instructions	1	1
CPI for Control instructions	3.1	1.5
CPI for Memory instructions	2.5	1.2

For a program with 20% ALU instructions, 15% control instructions and 65% memory instructions, which design will be faster? Give a quantitative CPI average for each case.

A: avg CPI = 1 * 0.2 + 3.1 * 0.15 + 2.5 * 0.65 = 2.29
MIPS = 700 MHz / 2.29 * 10^6 = 700 / 2.29 ~ 305

B: avg CPI = 1 * 0.2 + 1.5 * 0.15 + 1.2 * 0.65 = 1.205
MIPS = 500 MHz / 1.205 * 10^6 = 500 / 1.205 ~ 415

415 / 305 ~ 1.36 , so B is roughly 1.36 times faster than A.

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