Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (New) EXAMINATION – WINTER 2019

Subject Code: 3130704 Date: 3/12/2019

Subject Name: Digital Fundamentals

Time: 02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1*	**(a)**	Do as Directed 1. Given that $(16)_{10} = (100)_{x.}$ Find the value of x. 2. Add $(6E)_{16}$ and $(C5)_{16.}$ 3. $(1011011101101110)_2 = (\_\_\_\_\_)_8 = (\_\_\_\_\_)_{16}$.	**03**
	(b)	State and explain De Morgan's theorems with truth tables.	**04**
	(c)	Implement AND, OR, & EX-OR gates using NAND & NOR gates.	**07**
Q.2	**(a)**	Express the Boolean function F = A + B'C in a sum of minterms.	**03**
	(b)	Reduce the expression F = A [B + C' (AB + AC')']	**04**
	(c)	Simplify the following Boolean function by using the tabulation method. F (A, B, C, D) = Σ m (0, 1, 2, 8, 10, 11, 14, 15)	**07**
		OR	
	(c)	Using D & E as the MEV, Reduce F = A'B'C' + A'B'CD + A'BCE' + A'BC'E + AB'C + ABC + ABC'D'.	**07**
Q.3	**(a)**	Simplify the Boolean function F (w, x, y, z) = Σ m (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)	**03**
	(b)	Design 1 - bit Magnitude Comparator.	**04**
	(c)	Design a full adder and realize full adder using 3X8 Decoder and 2 OR gates.	**07**
		OR	
Q.3	**(a)**	Simplify the Boolean function F = A'B'C' + B'CD' + A'BCD' + AB'C'	**03**
	(b)	Explain 4 – bit parallel adder.	**04**
	(c)	Implement the following function using 8X1 MUX F (A, B, C, D) = Σ m (0, 1, 3, 4, 8, 9, 15)	**07**
Q.4	**(a)**	Explain SR flip-flop using characteristic table & characteristic equation.	**03**
	(b)	Explain the working of SISO shift register.	**04**
	(c)	Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use T – flip-flops.	**07**
		OR	
Q.4	**(a)**	What is the race around condition in JK flip-flop?	**03**
	(b)	Design 4-bit Ring counter using D flip-flip.	**04**
	(c)	Design JK flip-flip using D flip-flip.	**07**
Q.5	**(a)**	Explain the specification of D/A converter.	**03**
	(b)	Explain R-2R ladder type D/A converter,	**04**
	(c)	Explain Successive Approximation type A/D converter.	**07**
		OR	
Q.5	**(a)**	Explain classification of Memories.	**03**
	(b)	Explain the types of ROM.	**04**
	(c)	A combinational circuit is defined by the function F_1 (A, B, C,) = Σ m (4, 5, 7) F_2 (A, B, C,) = Σ m (3, 5, 7) Implement the circuit with a PLA having 3 inputs, 3 product term & 2 outputs.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2020

Subject Code:3130704 Date:05/03/2021

Subject Name:Digital Fundamentals

Time:10:30 AM TO 12:30 PM Total Marks:56

Instructions:

1. **Attempt any FOUR questions out of EIGHT questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Realize AND, OR and NOT gate using NAND gates only.	**03**
	(b)	State and prove De-Morgan's theorems using truth-tables.	**04**
	(c)	Do as directed: (a) $(1111.11)_2 = (\ ?\ )_8 = (\ ?\ )_{10}$ (b) 23 – 48 using 2's complement method (c) $(396)_{10} = (\ ?\ )_{BCD} = (\ ?\ )_{EX\text{-}3}$ (d) $(11111)_2 = (\ ?\ )_{Gray}$	**07**
Q.2	**(a)**	Define following: Figure of merit, Noise margin, and Power dissipation.	**03**
	(b)	Construct Hamming code for BCD 0110. Use even parity.	**04**
	(c)	Given a logic function: Z = ABC + BC'D + A'BC. (i) Make a truth table. (ii) Simplify using K-map. (iii)Realize simplified function using NAND gates only.	**07**
Q.3	**(a)**	Draw the logic diagram of 1-digit BCD adder.	**03**
	(b)	Minimize following Boolean function using K-map: $Y(A,B,C,D) = \Sigma\, m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$	**04**
	(c)	Write a brief note on race around condition and its solution. Draw & explain the logic diagram of master-slave JK flip-flop.	**07**
Q.4	**(a)**	Draw truth table of 2-bit digital comparator.	**03**
	(b)	Minimize following Boolean function using K-map: $F(A,B,C,D) = \Sigma\, m(1, 3, 7, 11, 15) + d(0, 2, 5)$	**04**
	(c)	Design a 4-bit synchronous down counter using T flip-flops.	**07**
Q.5	**(a)**	Design D FF using SR FF. Write truth table of D FF.	**03**
	(b)	Draw & explain in brief the logic diagram of 4-bit bidirectional shift register.	**04**
	(c)	List out various commonly used D/A converters. Draw & explain any one D/A converter.	**07**
Q.6	**(a)**	List out and explain any one application of the register.	**03**
	(b)	Design a 4-bit ripple up counter using JK flip-flops.	**04**
	(c)	List out various commonly used A/D converters. Draw & explain any one A/D converter.	**07**
Q.7	**(a)**	Draw internal organization of a 16 x 4 memory chip.	**03**
	(b)	Write a brief note on quantization and encoding.	**04**
	(c)	Write a detailed note on various types of memories.	**07**

Q.8	**(a)**	List out various characteristics of a D/A converter. Discuss any one.	**03**
	(b)	Obtain 2048 x 8 memory using 256 x 8 memory chips.	**04**
	(c)	Draw and explain in detail the block diagram of CPLD.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2021

Subject Code:3130704 Date:23-02-2022

Subject Name:Digital Fundamentals

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Implement EX-NOR using NAND gate.	**03**
	(b)	Convert the decimal number 225.225 to octal and hexadecimal.	**04**
	(c)	Give classification of logic families and compare CMOS and TTL.	**07**
Q.2	**(a)**	Convert F(A,B,C) = BC+A into standard minterm form.	**03**
	(b)	With logic diagram and truth table, explain the working of 3 line to 8 line decoder.	**04**
	(c)	Explain Successive Approximation A/D converter in detail.	**07**
		OR	
	(c)	A combinational logic is defined by functions: $F_1(A,B,C) = \sum m\,(3,5,6,7)$ $F_2(A,B,C) = \sum m\,(0,2,4,7)$ Implement the circuit with PLA having 3 inputs, 4 product terms & 2 outputs.	**07**
Q.3	**(a)**	Simplify the Boolean expression: $F(x,y,z) = \sum m\,(0,1,3,4,5,7)$	**03**
	(b)	Explain S-R clocked flip flop.	**04**
	(c)	Design full adder circuit using decoder and multiplexer.	**07**
		OR	
Q.3	**(a)**	Generate AND & EX-OR gates using NOR gate.	**03**
	(b)	Implement D flip flop using JK flip flop.	**04**
	(c)	Design a counter to generate the repetitive sequence 0,4,2,1,6.	**07**
Q.4	**(a)**	What is race around condition in JK flip flop.	**03**
	(b)	Construct a ring counter with five timing signals.	**04**
	(c)	Design BCD to Excess 3 code converter using minimum number of NAND gates.	**07**
		OR	
Q.4	**(a)**	Explain 2-bit comparator circuit.	**03**
	(b)	Write a short note on FPGA.	**04**
	(c)	What is Digital to Analog converter? Draw and Explain R-2R DAC.	**07**
Q.5	**(a)**	Perform following operation using 2's complement method. $(11010)_2 - (1000)_2$	**03**
	(b)	Write a short note on Read Only Memory (ROM).	**04**
	(c)	Explain the working of 4 bit binary ripple counter.	**07**
		OR	
Q.5	**(a)**	Obtain the truth table of the function: F = xy+yz+zx .	**03**
	(b)	Implement following functions using ROM. $F_1 = \sum m\,(1,3,4,6)$ and $F_2 = \sum m\,(0,1,5,7)$.	**04**
	(c)	Explain in detail Dual Slope A/D converter.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2021

Subject Code:3130704 Date:06/10/2021

Subject Name:Digital Fundamentals

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Solve the following Boolean functions by using K-Map. Implement the simplified function by using logic gates $F = (w,x,y,z) = \Sigma (0,1,4,5,6,8,9,10,12,14) + d(2,15)$	**03**
	(b)	Do as directed a. Convert 378.93_{10} to octal b. Add 27.5_8 and 74.4_8 c. Convert $5C7_{16}$ to decimal d. Multiply 1101_2 by 110_2	**04**
	(c)	With a neat block diagram explain the function of decoder. Design BCD to seven segment decoder	**07**
Q.2	**(a)**	Solve below function using 4 * 1 multiplexer $F(w,x,y) = \sum(1,2,4,7)$	**03**
	(b)	Compare CMOS and TTL Logic Family	**04**
	(c)	Design full adder and subtractor using mode control	**07**
		OR	
	(c)	Obtain the minimal expression for $f=\sum m(1,2,3,5,6,7,8,9,12,13,15)$ using the tabular method(Q McCluskey)	**07**
Q.3	**(a)**	Explain D flip flop with proper diagram	**03**
	(b)	Explain 4 bit Ring counter. What is the limitation in Ring counter?	**04**
	(c)	Design the Synchronous Mod – 6 counter using JK flip flop	**07**
		OR	
Q.3	**(a)**	Explain T flip flop with proper diagram	**03**
	(b)	Design 2 bit Ripple counter using –ve edge triggered JK flip flop	**04**
	(c)	Design 3 bit down Synchronous counter using T flip flop	**07**
Q.4	**(a)**	Explain below terms for DAC: a. Resolution b. Settling time	**03**
	(b)	Draw the logic diagram of Parallel in serial out shift register	**04**
	(c)	Draw and Explain R-2R ladder type DAC	**07**
		OR	
Q.4	**(a)**	Explain two input TTL Nand Gate	**03**
	(b)	Draw and Explain the successive approximation type ADC	**04**
	(c)	Draw and Explain 4 bit Universal Shift Register	**07**

Q.5	**(a)**	Explain below memory types a. MROM b. EEPROM	**03**
	(b)	Draw internal logic of a 32*8 ROM	**04**
	(c)	Draw PAL design to implement F1= a'bc+ab'c+ac' and F2=a'b'c'+bc	**07**

OR

Q.5	**(a)**	What are the advantages of PLD over the fixed function ICs	**03**
	(b)	Draw a structure of an unprogrammed PLA circuit	**04**
	(c)	Implement the following two Boolean functions with a PLA a. F1(A,B,C)=∑m(0,1,4) b. F2(A,B,C)=∑m(0,5,6,7)	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (NEW) EXAMINATION – SUMMER 2022

Subject Code:3130704 Date:18-07-2022

Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	List out various logic families. Also list characteristics of digital IC.	**03**
	(b)	What is signal? Explain different types of signal.	**04**
	(c)	Implement the following Boolean function using MUX a) $F(A,B,C) = \sum(1,3,6)$ b) $F(A,B,C) = \pi(2,3,5)$	**07**
Q.2	**(a)**	Perform the binary subtraction using 2's complement $(0111)_2 - (1101)_2$	**03**
	(b)	Convert the decimal Number 250.5 to base 4 and base 8.	**04**
	(c)	Design a Combinational circuit that convert 8- 4 -2 -1 code to BCD	**07**
		OR	
	(c)	Explain various logic gates.	**07**
Q.3	**(a)**	Compare Half adder and Full adder.	**03**
	(b)	Explain NAND gate as a Universal Gate.	**04**
	(c)	Implement 2-bit Magnitude comparator.	**07**
		OR	
Q.3	**(a)**	Simplify Boolean function using K-MAP F(A, B, C, D)=ABC'D' + ABC'D + ABCD' + AB'CD'	**03**
	(b)	Explain 4 bit Binary Parallel Adder.	**04**
	(c)	Explain Minterm and Maxterm.	**07**
Q.4	**(a)**	Give the difference between sequential circuit and combinational circuit.	**03**
	(b)	Explain Look-ahead Carry generator.	**04**
	(c)	Explain JK Flip-Flop.	**07**
		OR	
Q.4	**(a)**	Explain NAND SR Latch.	**03**
	(b)	Explain clock triggering mechanism.	**04**
	(c)	What is race around condition (racing)? How to solve it?	**07**
Q.5	**(a)**	Classify different types of digital to analog converters.	**03**
	(b)	Compare static RAM and dynamic RAM.	**04**
	(c)	List out different types of ROM. Also explain ROM.	**07**
		OR	
Q.5	**(a)**	Discuss the application of shift registers.	**03**
	(b)	Explain working of counter.	**04**
	(c)	Describe operation of D/A converter with binary-weighted resisters.	**07**

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