Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2020

Subject Code:3130907 Date:04/03/2021

Subject Name:Analog & Digital Electronics

Time:10:30 AM TO 12:30 PM Total Marks:56

Instructions:

1. **Attempt any FOUR questions out of EIGHT questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Define Slew Rate, CMRR, & Input Offset Voltage.	**03**
	(b)	Compare inverting and non-inverting op-amps.	**04**
	(c)	Draw & explain in detail the logic diagram & the truth table of clocked SR flip-flop.	**07**
Q.2	**(a)**	Draw block diagram of an op-amp.	**03**
	(b)	Draw and explain working of zero crossing detector.	**04**
	(c)	List out and discuss all the ideal characteristics of an op-amp.	**07**
Q.3	**(a)**	For an inverting amplifier, $V_1 = 1V$, $V_2 = 3V$, $V_3 = 2V$ with $R_1 = R_2 = R_3 = 2K\Omega$ and $R_F = 3K\Omega$. Determine the output voltage.	**03**
	(b)	Design an R-C phase shift oscillator to produce a sinusoidal output at 1KHz, using capacitor value 0.01 μF.	**04**
	(c)	Write a short note on instrumentation amplifier using op-amp.	**07**
Q.4	**(a)**	Explain the application of an op-amp as an integrator.	**03**
	(b)	Design full adder logic circuit using 3 x 8 decoder and OR gates.	**04**
	(c)	Explain the circuit diagram of op-amp as a Peak detector.	**07**
Q.5	**(a)**	Design D FF using SR FF. Write truth table of D FF.	**03**
	(b)	Minimize following Boolean function using K-map: $F(A,B,C,D) = \Pi\, M(1, 2, 3, 8, 9, 11, 14) \bullet d(7, 15)$	**04**
	(c)	Given a logic function: Z = ABC + BC'D + A'BC. a) Make a truth table. b) Simplify using K-map. c) Realize simplified function using NAND gates only.	**07**
Q.6	**(a)**	Minimize following Boolean function using K-map: $Y(A,B,C,D) = \Sigma\, m(0, 3, 5, 6, 9, 10, 12, 15)$	**03**
	(b)	Implement the following logic function using 8:1 multiplexer: $F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$	**04**
	(c)	Design a 4-bit synchronous down counter using T flip-flops.	**07**
Q.7	**(a)**	Compare combinational logic circuit with sequential logic circuit.	**03**
	(b)	Draw basic internal structure of 7490 ripple counter IC. Design BCD counter using 7490 IC.	**04**
	(c)	Draw & explain R-2R ladder D/A converter with necessary equations.	**07**

Q.8	**(a)**	Draw the logic diagram of 4-bit ripple up counter using JK FFs.	**03**
	(b)	Write a brief note on quantization and encoding.	**04**
	(c)	List out various commonly used A/D converters. Draw & explain Flash A/D converter with necessary decoding table. Also mention pros & cons of the same.	**07**

****

Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2021

Subject Code:3130907 Date:21-02-2022

Subject Name:Analog & Digital Electronics

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Define following a) CMRR b)PSRR c)Input Offset voltage	**03**
	(b)	What is cross over distortion in power amplifier?	**04**
	(c)	Draw and explain the equivalent circuit of OP-Amp.	**07**
Q.2	**(a)**	Define Slew Rate .Also mention about causes of slew rate.	**03**
	(b)	Draw the basic Integrator using OP-Amp. Derive the output equation of Integrator.	**04**
	(c)	Derive an expression for the output of a Inverting Summing amplifier with three input and Average amplifier.	**07**
		OR	
	(c)	Discuss the classification of active filter and explain the frequency response of each type.	**07**
Q.3	**(a)**	Simplify $\bar{A}BC\bar{D} + BC\bar{D} + B\bar{C}\bar{D} + B\bar{C}D$	**03**
	(b)	Realize expression using minimum NAND gates only $Y = A\bar{B} + A\bar{C} + C + AD + A\bar{B}C + ABC$	**04**
	(c)	For the following function implement the SOP and POS circuit $F(A,B,C,D) = \Sigma m(2,3,5,7,12) + \Sigma d(6,13,14,15)$	**07**
		OR	
Q.3	**(a)**	Simplify the Boolean function with K map $F(a, b, c, d) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$	**03**
	(b)	Implement the following function using 8:1 Multiplexer. $F(A,B,C,D) = \bar{A}B\bar{D} + ACD + \bar{B}CD + \bar{A}\bar{C}D$	**04**
	(c)	Explain Half Adder circuit .Explain Full adder circuit with the help of two Half adder.	**07**
Q.4	**(a)**	Compare RC phase shift and Wien bridge oscillator.	**03**
	(b)	Write a short note on Precision rectifier.	**04**
	(c)	Explain the working of Zero crossing Detector.	**07**
		OR	
Q.4	**(a)**	Define following a) Attenuation b) Pass Band c) Cut of frequency	**03**
	(b)	Draw the peak detector circuit using Op-amp and explain it's operation.	**04**
	(c)	Draw and explain the block diagram of basic three terminal IC Regulator.	**07**
Q.5	**(a)**	Explain the different types of triggering methods used for flip flops.	**03**
	(b)	Write a note on serial in parallel out operation of shift register.	**04**
	(c)	Explain the Binary Weighted register technique of D/A converter.	**07**
		OR	

Q.5	**(a)**	Define following specification of DAC a) Accuracy b) Resolution c) Setting time	**03**
	(b)	Which are the different methods for A/D conversion ?	**04**
	(c)	Draw and explain the working of 4 bit Ring counter.	**07**

.

****

Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2021

Subject Code:3130907 Date:11/09/2021

Subject Name:Analog & Digital Electronics

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Draw transistor C-E amplifier circuit. Draw its ac equivalent circuit.	**03**
	(b)	Sketch the block schematic of a typical operational amplifier and briefly explain the function of each block.	**04**
	(c)	Explain how Op-amp works as summing amplifier.	**07**
Q.2	**(a)**	List applications of instrumentation amplifier.	**03**
	(b)	Explain the following terms. (1) PSRR (2) Input bias current (3) Input offset Voltage (4) CMRR.	**04**
	(c)	Explain in detail voltage follower with its applications.	**07**
		OR	
	(c)	What do you mean by slew rate in an OP-AMP? Also mention about causes of slew rate and explain its significance in applications.	**07**
Q.3	**(a)**	What are the advantages of active filters over passive filters?	**03**
	(b)	Sketch Wein bridge oscillator. Explain working.	**04**
	(c)	Draw the circuit op-amp as differentiator and explain with necessary waveforms.	**07**
		OR	
Q.3	**(a)**	How to detect peak of waveform using OP-AMP?	**03**
	(b)	Compare: Comparator and Schmitt trigger.	**04**
	(c)	Draw and explain the use of op-amp as a zero crossing detector.	**07**
Q.4	**(a)**	Compare SOP and POS.	**03**
	(b)	Write short note on Gray code.	**04**
	(c)	Prove that NAND and NOR gates are universal gates.	**07**
		OR	
Q.4	**(a)**	Design half subtractor logic circuit.	**03**
	(b)	Explain Master-Slave J-K flip-flop configuration.	**04**
	(c)	Simplify the Boolean function F(A,B,C,D) = Σm (2,5,7,8,11,14,15), Σd=(0,3,6,10) using K-map method. Implement using basic logic gates.	**07**
Q.5	**(a)**	Sketch sample and hold circuit and explain its working.	**03**
	(b)	Explain resolution and quantization error in reference to ADC.	**04**
	(c)	Design 4-bit up/down ripple counter.	**07**
		OR	
Q.5	**(a)**	Compare EPROM with FLASH memory.	**03**
	(b)	Explain R-2R ladder DAC with necessary diagram.	**04**
	(c)	Draw 4-bit down counter; explain its working with timing diagram and truth table.	**07**

****

Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (NEW) EXAMINATION – SUMMER 2022

Subject Code:3130907 Date:15-07-2022

Subject Name:Analog & Digital Electronics

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Draw the symbol and write truth table of AND, OR, EX-OR gate	**03**
	(b)	Define combinational and sequential circuits with example	**04**
	(c)	Explain characteristics of an Ideal OPAMP	**07**
Q.2	**(a)**	Define gain band width product, input bias current and SVRR.	**03**
	(b)	Draw pin diagram of IC 741 and state function of each pin.	**04**
	(c)	Determine the output voltage in each of the following cases for the open loop differential amplifier (i) Vin1 = 5µV dc, Vin2 = -7µV dc (ii) Vin1 = 10mV rms, Vin2 = 20mV rms The OPAMP is a 741 with the following specifications: A = 200000, Ri = 2MΩ, Ro = 75Ω, +Vcc = +15V, -VEE = -15V and output voltage swing = ±14V. Also comment on the result with output waveforms.	**07**
		OR	
	(c)	Explain precision rectifier and peak detector with circuit diagram and waveforms.	**07**
Q.3	**(a)**	Derive the equation of CMRR in dB for the OPAMP connected in common mode configuration.	**03**
	(b)	Classify Active Filter and explain it's advantages	**04**
	(c)	Draw and explain differential instrumentation amplifier using transducer bridge.	**07**
		OR	
Q.3	**(a)**	Define scaling amplifier and derive output voltage equation of scaling amplifier.	**03**
	(b)	Explain working of sine wave to square wave converter with diagram and waveforms.	**04**
	(c)	Draw and explain PI controller using 4 OPAMPs.	**07**
Q.4	**(a)**	Show the logic arrangements for implementing 4 input NAND gate using 2 input AND gates and NOT gates.	**03**
	(b)	Write Minterm and Maxterm of three variables k-map	**04**
	(c)	Explain 4 to 1 multiplexer with logic diagram and truth table	**07**
		OR	
Q.4	**(a)**	Implement OR gate using NAND gates only with truth table and logic expressions.	**03**
	(b)	Explain sample and hold circuit relevant to D/A converter	**04**
	(c)	Explain 3 to 8 decoder with logic diagram and truth table	**07**

Q.5	**(a)**	Draw the block diagram of clocked S-R flip-flop and write its characteristics table.	**03**
	(b)	Explain quantization and encoding relevant to A/D converter.	**04**
	(c)	Explain 4 bit shift register with block diagram and timing diagram	**07**

OR

Q.5	**(a)**	Define setup time, hold time and propagation delay related to flip-flop.	**03**
	(b)	Explain dual slope A/D converter with block diagram.	**04**
	(c)	Explain 4 bit ring counter using D flip-flop with block diagram and timing diagram	**07**

****