Seat No.:	Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER-III (NEW) EXAMINATION – WINTER 2020

	•	Code:313090/	Date: 04/03/2	U Z 1
	•	Name: Analog & Digital Electronics		
		2:30 AM TO 12:30 PM	Total Mark	s:56
Inst	ructio			
	1. 2.	Attempt any FOUR questions out of EIGHT questions. Make suitable assumptions wherever necessary.		
	3.	Figures to the right indicate full marks.		
				MARKS
Q.1	(a)	Define Slew Rate, CMRR, & Input Offset Voltage.		03
	(b)	Compare inverting and non-inverting op-amps.		04
	(c)	Draw & explain in detail the logic diagram & the truth table flip-flop.	of clocked SR	07
Q.2	(a)	Draw block diagram of an op-amp.		03
	(b)	Draw and explain working of zero crossing detector.		04
	(c)	List out and discuss all the ideal characteristics of an op-amp.		07
Q.3	(a)	For an inverting amplifier, $V_1 = 1V$, $V_2 = 3V$, $V_3 = 2V$ with F $2K\Omega$ and $R_F = 3K\Omega$. Determine the output voltage.	$R_1 = R_2 = R_3 =$	03
	(b)	Design an R-C phase shift oscillator to produce a sinusoidal or	utput at 1KHz,	04
		using capacitor value 0.01 μF.		
	(c)	Write a short note on instrumentation amplifier using op-amp).	07
Q.4	(a)	Explain the application of an op-amp as an integrator.		03
2.1	(b)	Design full adder logic circuit using 3 x 8 decoder and OR ga	ites.	04
	(c)	Explain the circuit diagram of op-amp as a Peak detector.		07
Q.5	(a)	Design D FF using SR FF. Write truth table of D FF.		03
	(b)	Minimize following Boolean function using K-map: $F(A,B,C,D) = \prod M(1, 2, 3, 8, 9, 11, 14) \cdot d(7, 15)$		04
	(c)	Given a logic function: $Z = ABC + BC'D + A'BC$.		07
	(C)	a) Make a truth table.		07
		b) Simplify using K-map.		
		c) Realize simplified function using NAND gates only.		
Q.6	(a)	Minimize following Boolean function using K-map: $Y(A,B,C,D) = \sum m(0, 3, 5, 6, 9, 10, 12, 15)$		03
	(b)	Implement the following logic function using 8:1 multiplexer	·:	04
	(,-)	$F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$	•	-
	(c)	Design a 4-bit synchronous down counter using T flip-flops.		07
Q.7	(a)	Compare combinational logic circuit with sequential logic cir	cuit.	03
-	(b)	Draw basic internal structure of 7490 ripple counter IC. Design using 7490 IC.		04
	(c)	Draw & explain R-2R ladder D/A converter with necessary ea	quations.	07

Q.8	(a) (b)	Draw the logic diagram of 4-bit ripple up counter using JK FFs. Write a brief note on quantization and encoding.	03 04
	(c)	List out various commonly used A/D converters. Draw & explain Flash A/D converter with necessary decoding table. Also mention pros & cons of the same.	07

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-III (NEW) EXAMINATION - WINTER 2021

Subject Code:3130907	Date:21-02-2022
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Subject Name: Analog & Digital Electronics

Time:10:30 AM TO 01:00 PM	Total Marks:70
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Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.
- 4. Simple and non-programmable scientific calculators are allowed.

			MARKS
Q.1		Define following a) CMRR b)PSRR c)Input Offset voltage What is cross over distortion in power amplifier? Draw and explain the equivalent circuit of OP-Amp.	03 04 07
	(C)	Draw and explain the equivalent eneult of Or -Amp.	U7
Q.2	(a)	Define Slew Rate .Also mention about causes of slew rate.	03
	(b)	Draw the basic Integrator using OP-Amp. Derive the output equation of Integrator.	04
	(c)	Derive an expression for the output of a Inverting Summing amplifier with three input and Average amplifier. OR	07
	(c)	Discuss the classification of active filter and explain the frequency response of each type.	07
Q.3	(a)	Simplify $\overline{A}BC\overline{D} + BC\overline{D} + B\overline{C}\overline{D} + B\overline{C}D$	03
	` '	Realize expression using minimum NAND gates only $Y = A\overline{B} + A\overline{C} + C + AD + A\overline{B}C + ABC$	04
	(c)	For the following function implement the SOP and POS circuit $F(A,B,C,D) = \Sigma m (2,3,5,7,12) + \Sigma d (6,13,14,15)$	07
0.2	(-)	OR	02
Q.3	(a)	Simplify the Boolean function with K map $F(a, b, c, d) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$	03
	(b)		04
	(c)	Explain Half Adder circuit .Explain Full adder circuit with the help of two Half adder.	07
Q.4	(a)	Compare RC phase shift and Wien bridge oscillator.	03
~··	(b)	Write a short note on Precision rectifier.	04
	(c)	Explain the working of Zero crossing Detector. OR	07
0.4	(a)	Define following	03
	()	a) Attenuation b) Pass Band c) Cut of frequency	
	(b)	Draw the peak detector circuit using Op-amp and explain it's operation.	04
	(c)	Draw and explain the block diagram of basic three terminal IC Regulator.	07
Q.5	(a)	Explain the different types of triggering methods used for flip flops.	03
	(b)	Write a note on serial in parallel out operation of shift register.	04
	(c)	Explain the Binary Weighted register technique of D/A converter.	07

Q.5	(a)	Define following specification of DAC	03
		a) Accuracy b) Resolution c) Setting time	
	(b)	Which are the different methods for A/D conversion?	04
	(c)	Draw and explain the working of 4 bit Ring counter.	07

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-III (NEW) EXAMINATION - SUMMER 2021

Subject Code:3130907 Date:11/09/2021

Subject Name: Analog & Digital Electronics

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.
- 4. Simple and non-programmable scientific calculators are allowed.

			MARKS
Q.1	(a) (b)	Draw transistor C-E amplifier circuit. Draw its ac equivalent circuit. Sketch the block schematic of a typical operational amplifier and briefly explain the function of each block.	03 04
	(c)	Explain how Op-amp works as summing amplifier.	07
Q.2	(a)	List applications of instrumentation amplifier.	03
	(b)	Explain the following terms. (1) PSRR (2) Input bias current (3) Input offset Voltage (4) CMRR.	04
	(c)	Explain in detail voltage follower with its applications.	07
		OR	
	(c)	What do you mean by slew rate in an OP-AMP? Also mention about	07
		causes of slew rate and explain its significance in applications.	
Q.3	(a)	What are the advantages of active filters over passive filters?	03
	(b)	Sketch Wein bridge oscillator. Explain working.	04
	(c)	Draw the circuit op-amp as differentiator and explain with necessary	07
		waveforms.	
		OR	
Q.3	(a)	How to detect peak of waveform using OP-AMP?	03
	(b)	Compare: Comparator and Schmitt trigger.	04
	(c)	Draw and explain the use of op-amp as a zero crossing detector.	07
Q.4	(a)	Compare SOP and POS.	03
	(b)	Write short note on Gray code.	04
	(c)	Prove that NAND and NOR gates are universal gates.	07
		OR	
Q.4	(a)	Design half subtractor logic circuit.	03
	(b)	Explain Master-Slave J-K flip-flop configuration.	04
	(c)	Simplify the Boolean function $F(A,B,C,D) = \Sigma m$ (2,5,7,8,11,14,15), $\Sigma d=(0,3,6,10)$ using K-map method. Implement using basic logic gates.	07
Q.5	(a)	Sketch sample and hold circuit and explain its working.	03
Q.S	(b)	Explain resolution and quantization error in reference to ADC.	03
	(c)	Design 4-bit up/down ripple counter.	07
	(C)	OR	07
Q.5	(a)	Compare EPROM with FLASH memory.	03
V.	(a) (b)	Explain R-2R ladder DAC with necessary diagram.	03
	(c)	Draw 4-bit down counter; explain its working with timing diagram and	07
	(0)	truth table.	U/

Seat No.:	Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY BE - SEMESTER- III (NEW) EXAMINATION - SUMMER 2022

Subj	ect	Code:3130907 Date:15-0	07-2022
Subj	ect]	Name:Analog & Digital Electronics	
		:30 PM TO 05:00 PM Total Ma	arks:70
Instru			
	2. 3.	Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks. Simple and non-programmable scientific calculators are allowed.	
		Simple and non-programmable setemme calculators are anowed.	MARKS
Q.1	(a) (b)	•	03 04
	(c)	Explain characteristics of an Ideal OPAMP	07
Q.2	(a) (b) (c)		03 04 07
	(c)	<u> </u>	07
Q.3	(a)	Derive the equation of CMRR in dB for the OPAMP connected in common mode configuration.	03
	(b) (c)	Classify Active Filter and explain it's advantages Draw and explain differential instrumentation amplifier using transducer bridge.	04 07
Q.3	(a)	OR Define scaling amplifier and derive output voltage equation of scaling	03
Q.S	(a)	amplifier.	0.5
	(b)	and waveforms.	04
	(c)	Draw and explain PI controller using 4 OPAMPs.	07
Q.4	(a)	Show the logic arrangements for implementing 4 input NAND gate using 2 input AND gates and NOT gates.	03
	(b)	Write Minterm and Maxterm of three variables k-map	04
	(c)	Explain 4 to 1 multiplexer with logic diagram and truth table OR	07
Q.4	(a)	expressions.	03
	(b) (c)	Explain sample and hold circuit relevant to D/A converter Explain 3 to 8 decoder with logic diagram and truth table	04 07

Q.5	(a)	Draw the block diagram of clocked S-R flip-flop and write its	03
		characteristics table.	
	(b)	Explain quantization and encoding relevant to A/D converter.	04
	(c)	Explain 4 bit shift register with block diagram and timing diagram	07
		OR	
Q.5	(a)	Define setup time, hold time and propagation delay related to flip-flop.	03
	(b)	Explain dual slope A/D converter with block diagram.	04
	(c)	Explain 4 bit ring counter using D flip-flop with block diagram and	07
		timing diagram	