Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–IV (NEW) EXAMINATION – WINTER 2020

Subject Code:3140707 Date:15/02/2021

Subject Name:Computer Organization & Architecture

Time:02:30 PM TO 04:30 PM Total Marks:56

Instructions:

1. **Attempt any FOUR questions out of EIGHT questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	What is PSW? Explain each bit of it	**03**
	(b)	Write ALP for addition of 10 numbers	**04**
	(c)	List and explain Memory reference instructions in detail	**07**
Q.2	**(a)**	Design a digital circuit for 4-bit binary adder	**03**
	(b)	Explain 4 bit arithmetic circuit with suitable diagram.	**04**
	(c)	Draw and briefly explain flowchart for second pass of assembler.	**07**
Q.3	**(a)**	Explain any three register reference instruction in detail.	**03**
	(b)	Explain BCD adder in brief	**04**
	(c)	Draw and explain micro program sequencer circuit with diagram.	**07**
Q.4	**(a)**	State the differences between hardwired control and micro programmed control.	**03**
	(b)	Explain hardware implementation of common bus system using three-State buffers. Mention assumptions if required.	**04**
	(c)	Explain delay load and delay branch with respect to RISC pipeline.	**07**
Q.5	**(a)**	Draw and briefly explain flowchart for first pass of assembler	**03**
	(b)	State the major characteristics of RISC processor	**04**
	(c)	Elaborate 4-segment instruction pipeline with neat sketches.	**07**
Q.6	**(a)**	State the major characteristics of CISC processor	**03**
	(b)	List various types of addressing modes and explain any four of them.	**04**
	(c)	What is virtual memory? Explain relation between address space and memory space in virtual memory system.	**07**
Q.7	**(a)**	Briefly explain source initiated transfer using handshaking.	**03**
	(b)	Differentiate Programmed I/O and Interrupt initiated I/O	**04**
	(c)	Write a short note on associative memory.	**07**
Q.8	**(a)**	How main memory is useful in computer system? Explain the memory address map of RAM and ROM.	**03**
	(b)	Explain daisy chain priority interrupt	**04**
	(c)	Explain CPU-IOP communication with diagram.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – WINTER 2021

Subject Code:3140707 Date:03/01/2022

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Explain three state buffers.	**03**
	(b)	Describe BUN and BSA memory reference instructions in detail.	**04**
	(c)	What is interrupt? Describe interrupt cycle with neat diagram.	**07**
Q.2	**(a)**	Differentiate assembly language and machine language.	**03**
	(b)	What is the need of common bus? Draw common bus cycle.	**04**
	(c)	Write an assembly language program to find whether the given number is prime or not.	**07**
		OR	
	(c)	Write an assembly language program to find factorial of the given number.	
Q.3	**(a)**	Define followings: 1. Control Memory 2. Control Word 3. Control Address Register	**03**
	(b)	Draw the flowchart of first pass of the assembler and explain working of the same.	**04**
	(c)	What is the significance of pipelining in computer architecture? Write a note on instruction pipeline.	**07**
		OR	
Q.3	**(a)**	What is address sequencing? Explain.	**03**
	(b)	Construct a 4-bit adder-subtractor circuit.	**04**
	(c)	What addressing mode means? Explain any three addressing modes in detail with example.	**07**
Q.4	**(a)**	Enlist the characteristics of RISC.	**03**
	(b)	Write a program to evaluate X = (a*b)/c+d in two address and three address instruction formats.	**04**
	(c)	Draw neat and clean flowchart for divide operation. Explain with example.	**07**
		OR	
Q.4	**(a)**	Differentiate isolated I/O and memory mapped I/O.	**03**
	(b)	Describe pipeline conflicts.	**04**
	(c)	What is cache memory address mapping? Compare and contrast direct address mapping and set-associative address mapping.	**07**
Q.5	**(a)**	What is the importance of virtual memory?	**03**
	(b)	Explain multiport memory and crossbar switch with reference to interconnection structures in multiprocessors.	**04**

	(c)	Assume a computer system uses 5 bit (1 sign + 4 Magnitude) registers and 2's complement representation. Perform multiplication of number 10 with the smallest number in this system using booth algorithm. Show step-by-step multiplication process.	**07**

OR

Q.5	**(a)**	What is cache coherence? Describe.	**03**
	(b)	A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. How many bits for the will be required for TAG field?	**04**
	(c)	Which are the different ways to transfer data to and from peripheral devices? Explain any one of them in detail.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– IV EXAMINATION – SUMMER 2020

Subject Code: 3140707 Date:27/10/2020

Subject Name: Computer Organization & Architecture

Time: 10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			Marks
Q.1	**(a)**	Enlist register reference instructions and explain any one of them in detail.	**03**
	(b)	What is combinational circuit? Explain multiplexer in detail. How many NAND gates are needed to implement 4 x 1 MUX?	**04**
	(c)	Draw the flowchart for instruction cycle and explain.	**07**
Q.2	**(a)**	What is RAM and ROM?	**03**
	(b)	One hypothetical basic computer has the following specifications: Addressing Mods = 16 Total Instruction Types = 4 (IT1, IT2, IT3, IT4) Each of the instruction type has 16 different instructions. Total General-Purpose Register = 8 Size of Memory = 8192 X 8 bits Maximum number of clock cycles required to execute one instruction = 32 Each instruction of the basic computer has one memory operand and one register operand in addition to other required fields. a. Draw the instruction word format and indicate the number of bits in each part. b. Draw the block diagram of control unit.	**04**
	(c)	Write an assembly language program to find the Fibonacci series up to the given number.	**07**
		OR	
	(c)	Write an assembly language program to find average of 15 numbers stored at consecutive location in memory.	
Q.3	**(a)**	Which are different pipeline conflicts. Describe.	**03**
	(b)	What is assembler? Draw the flowchart of second pass of the assembler.	**04**
	(c)	Write a note on arithmetic pipeline.	**07**
		OR	
Q.3	**(a)**	What is address sequencing? Explain.	**03**
	(b)	Design a simple arithmetic circuit which should implement the following operations: Assume A and B are 3 bit registers. Add : A+B, Add with Carry: A+B+1, Subtract: A+B', Subtract with Borrow: A+B'+1, Increment A: A+1, Decrement A: A-1, Transfer A: A	**04**

	(c)	Explain how addition and subtraction of signed data is performed if a computer system uses signed magnitude representation.	**07**
Q.4	**(a)**	Enlist different status bit conditions.	**03**
	(b)	What is addressing mode? Explain direct and indirect addressing mode with example.	**04**
	(c)	What is cache memory address mapping? Which are the different memory mapping techniques? Explain any one of them in detail.	**07**
		OR	
Q.4	**(a)**	Differentiate isolated I/O and memory mapped I/O.	**03**
	(b)	Compare and contrast RISC and CISC.	**04**
	(c)	Explain booth's multiplication algorithm with example.	**07**
Q.5	**(a)**	What is associative memory? Explain.	**03**
	(b)	Differentiate between paging and segmentation techniques used in virtual memory.	**04**
	(c)	Write a note on asynchronous data transfer.	**07**
		OR	
Q.5	**(a)**	Write about Time-shared common bus interconnection structure.	**03**
	(b)	Explain the working of Direct Memory Access (DMA).	**04**
	(c)	Write a note on interprocess communication and synchronization.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – SUMMER 2021

Subject Code:3140707 Date:06/09/2021

Subject Name:Computer Organization & Architecture

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	State differences between hardwired control unit and microprogrammed control unit.	**03**
	(b)	Explain register stack and memory stack.	**04**
	(c)	Show the contents of registers E, AC, BR, QR and SC during the process of multiplying 11111 with 10101.	**07**
Q.2	**(a)**	Write down RTL statements for the fetch and decode operation of basic computer.	**03**
	(b)	Define pipelining. For arithmetic operation (Ai *Bi + Ci) with a stream of seven numbers (i=1 to 7). Specify a pipeline configuration to carry out this task.	**04**
	(c)	Write a program to evaluate the arithmetic statement: A*B+C*D+E i. Using an accumulator type computer. ii. Using a stack organized computer.	**07**
		OR	
	(c)	A non-pipeline system takes to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?	**07**
Q.3	**(a)**	List down six major characteristics of RISC processors.	**03**
	(b)	Explain how (r-1)'s complement is calculated. Calculate 9's complement of 546700.	**04**
	(c)	Elaborate CPU-IOP communication.	**07**
		OR	
Q.3	**(a)**	List and explain major instruction pipeline conflicts.	**03**
	(b)	Define RTL. Give block diagram and timing diagram of transfer of R1 to R2 when P=1.	**04**
	(c)	Elaborate content addressable memory (CAM).	**07**
Q.4	**(a)**	Explain memory hierarchy in brief.	**03**
	(b)	Draw and explain flowchart for first pass of assembler.	**04**
	(c)	Explain using a flowchart how address of control memory is selected in microprogrammed control unit.	**07**
		OR	
Q.4	**(a)**	Briefly explain DMA.	**03**
	(b)	Write assembly level program to subtract two given numbers.	**04**
	(c)	Write the symbolic microprogram routine for the BSA instruction. Use the microinstruction format of basic microprogrammed control unit.	**07**

Q.5	**(a)**	How many AND gates and Adders will be required to multiply a 5 bit number with a 3 bit number? Also say size of adder (bits). How many bits will be there in the result?	**03**
	(b)	What do you mean by cache memory? Justify the need of cache memory in computer systems.	**04**
	(c)	Discuss multistage switching network with neat diagrams.	**07**

OR

Q.5	**(a)**	Explain the non-restoring methods for dividing two numbers.	**03**
	(b)	Discuss source-initiated transfer using handshaking in asynchronous data transfer.	**04**
	(c)	Elaborate cache coherence problem with its solutions.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – SUMMER 2022

Subject Code:3140707 Date:29-06-2022

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	What is binary and decimal equivalent of F8 hexadecimal value?	**03**
	(b)	Write Steps for two n digit numbers subtraction in base r.	**04**
	(c)	List and explain Memory reference instructions in detail.	**07**
Q.2	**(a)**	What is arithmetic micro operation?	**03**
	(b)	What is RAM and ROM?	**04**
	(c)	Draw and explain working of 4 bit binary adder.	**07**
		OR	
	(c)	State and Explain any seven logic micro operation.	**07**
Q.3	**(a)**	List out Register for basic computer.	**03**
	(b)	Explain register reference instruction format.	**04**
	(c)	Explain register transfer using block diagram and timing diagram.	**07**
		OR	
Q.3	**(a)**	Draw and explain control unit diagram for basic computer.	**03**
	(b)	State various phases of instruction cycle.	**04**
	(c)	Explain any four input output reference instruction.	**07**
Q.4	**(a)**	Draw flowchart of first pass assembler.	**03**
	(b)	Write assembly language program to add two numbers.	**04**
	(c)	Write assembly language program to multiply two numbers.	**07**
		OR	
Q.4	**(a)**	What is address sequencing?	**03**
	(b)	Write assembly language program to subtract one number from other number.	**04**
	(c)	Explain booth's multiplication algorithm with example.	**07**
Q.5	**(a)**	Explain register stack.	**03**
	(b)	What is difference between two address and three address instructions?	**04**
	(c)	Write a note on asynchronous data transfer.	**07**
		OR	
Q.5	**(a)**	What is difference between direct and indirect addressing mode?	**03**
	(b)	Explain arithmetic pipeline.	**04**
	(c)	Write a short note on virtual memory.	**07**

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