

DESIGN OF VCO-BASED CONTINUOUS-TIME $\Delta\Sigma$ ADCS FOR
NEURAL RECORDING APPLICATIONS

BY

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ABSTRACT

Analog-to-digital converters for neural recording circuits require significant signal integrity constraints to measure action potentials. As technology for electrophysiology and brain-machine interfaces becomes more advanced, advances in analog-to-digital conversion circuits are needed. One particularly effective strategy for high-SNR ADCs is delta-sigma modulation to correct for errors induced by quantization noise. In this thesis, the fundamental theory and design constraints of delta-sigma modulation in neural-recording circuits will be explored as well as the implementation of a VCO-based quantizer to significantly reduce area and power constraints while maintaining high SNR. Preliminary simulations of a first-order loop filter followed by a VCO-based quantizer can achieve 92.9 dB of signal-to-quantization noise ratio (SQNR) at an oversampling ratio (OSR) of 500.

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CHAPTER 1

INTRODUCTION

Advances in brain-machine interfaces potentially can alleviate various neurological and psychiatric conditions and is an important tool in neuroscience. Outside of medical use cases, signals from neurons such as action potentials (APs) and local-field potentials (LFPs) can be filtered and interpreted for neuromodulation therapies, control of prosthetics, and advanced mixed-reality applications. Such development has lead to a proliferation of funding and research into advanced digital-signal processing and machine learning algorithms to decode and interpret neural activity. In order to provide an accurate training set for such applications however, better analog front-end circuitry are needed to achieve high signal integrity, minimal invasiveness, and low-cost [1]. Analog-to-digital conversion (ADC) techniques are performed to extract sensory data from a low-noise instrumentation amplifier that amplifies and filters spike recordings to allow for fast signal processing techniques. In particular, an ADC design used for a neural recording application must satisfy many requirements including low-bandwidth, low-power, and high signal-to-quantization-noise (SQNR).

Traditional architectures like successive-approximation registers (SAR) are commonly used in many ADC applications [2][3]. SAR ADCs traditionally have high linearity and can operate in a low-power state when not used but are generally used in high-speed applications and are better suited to wider bandwidths, not ideal for neural recording. In contrast, the delta-sigma ADC is known to have high resolutions at low-bandwidth signals as well as great power efficiency. Various delta-sigma ADC architectures have been designed with improvements to SQNR and power through increasing the number of stages in the ADC, increasing the number of levels in the quantizer, or changing the oversampling ratio (OSR) of the system. By exploring various architectures of delta-sigma ADCs and in particular, a VCO-based quantizer architectures, this research aims to design an ADC

optimal for neural recording applications.

This thesis will be organized as follows. Chapter 2 explains the design constraints and fundamentals behind the delta-sigma ADC. Chapter 3 explores the preliminary choices and designs at the start of the project. Chapter 4 lists the circuit design strategy of the integrator, quantizer, and DAC. Finally, chapter 5 concludes the thesis and the next steps.

CHAPTER 2

DELTA-SIGMA MODULATORS

This chapter introduces the fundamentals behind a delta-sigma modulator as well as the constraints that are applied to the application of neural recording and the VCO-based Quantizer.

2.1 Neural Recording

Action potentials, also known as spikes, are the target of recording for most neural recording applications. Spikes generate when channels and pumps along the axon of a neuron has a large update of ions such as Na^+ and K^+ which causes a $100\mu\text{V}$ voltage difference across the neuron and extracellular space. Due to a refractory period needed to return to the axons resting potential, the frequency of a spike occurs anywhere from 500-5 kHz. Common neural recording architectures typically have a low-noise instrumentation amplifier followed by an ADC that transmits the data via a link to a DSP processor for spike sorting and control. The LNA is assumed to have high common-mode rejection, management of DC input offsets, and high gain to combat noise from a recording electrode. It is evident that an ADC must be able to process low-signal bandwidths without much attenuation and that

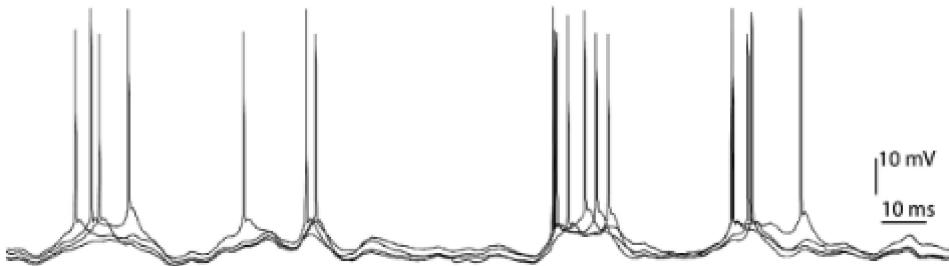


Figure 2.1: Spike train read from a neuron. Spikes have amplitudes on the order of $100\mu\text{V}$ and frequencies on the order of 500-5kHz

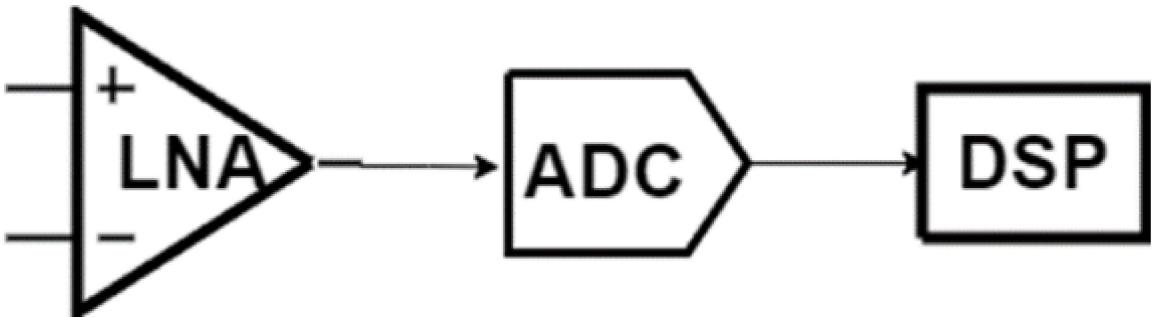


Figure 2.2: General model of a neural recording ASIC. Usually involves an analog-front end that amplifies and filters signals like a low-noise amplifier, an ADC, and a DSP processing block for further filtering or control

the speed of the ADC or its high frequency components is not particularly important. If the ADC is to be implanted alongside the LNA for minimum signal attenuation however, it is very important that the area is as small as possible to allow for scaling and the power is below $10 \mu\text{W}$ to prevent thermal ablation of surrounding tissue. However, due to the difficulty of achieving such a power constraint, it is beyond the scope of this thesis and the goal will be to minimize area and power as sufficiently as feasible.

Various implementations of a VCO-based ADC have been recently proposed for neural recording. Zhao et al.[8] proposed a hybrid-PLL type read out circuit that utilizes phase locking techniques to achieve an impressive 172 dB Schreier FoM at an area of $.025 \text{ mm}^2$ and $4.68 \mu\text{W}$ power consumption. Another implementation implemented by Pochet et al. that used a feedforward technique to linearize its VCOs managed to successfully implement a 179.6 dB Schreier FoM at 0.1 mm^2 area and $4.4 \mu\text{W}$ power consumption. Such FoMs are very difficult to achieve and meet the area and power consumption requirements of neural recording. This thesis aims to replicate the high SQNR and low area/power architectures that have been previously proposed.

2.2 ADC and Quantization Error Basics

The most fundamental analog-to-digital converter architecture is the quantizer. The quantizer breaks down an analog signal into a set of discrete levels that, aside from nonlinearities, have the same step size. The difference between the highest possible input and the lowest possible input of a step size

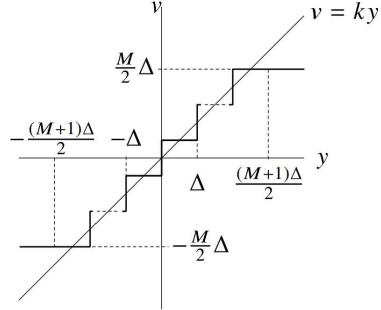


Figure 2.3: Figure from [5] detailing quantization. v indicates the input of the quantizer and y is the output. 2^*M is the number of steps in the quantizer

is known referred to as the full scale and the voltage needed to transition to another step is referred to as the the least significant bit (LSB, indicated by Δ).

Quantization errors are the differences between the quantized signal and the true input signal that are not described at the output. As shown from the Figure 2.3, the range of the quantization error is $(-\frac{\Delta}{2}, \frac{\Delta}{2})$.

Note that if the input voltage goes beyond the full scale of the quantizer, then the quantizer is said to be overloaded and can no longer output beyond the maximum inputs. From this, it is necessary to ensure that the quantizer is not overloaded and that the quantization steps are sufficiently small enough to encode as much information as possible. If the quantizer is continuously in use, then the noise of the quantizer can be approximated as a white noise and the noise power can be estimated as:

$$P_e = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} x^2 f(x) dx = \frac{1}{\Delta} \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} x^2 dx = \frac{\Delta^2}{12} \quad (2.1)$$

2.3 Oversampling

The need for high ENOBs and to prevent aliasing at frequencies close to the sampling frequency makes ADCs sampling at the rate of the Nyquist frequency infeasible. Therefore, it is necessary to oversample, that is sample at frequencies significantly higher than the Nyquist frequency. The oversam-

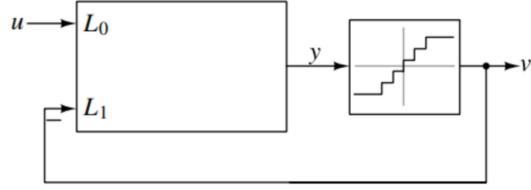


Figure 2.4: Figure from [5] detailing the Delta Sigma operation. u is the input of the system, y is the input of the quantizer, and v is the output of the system. The loop filter consists of two filters: L_0 handles the input and L_1 handles the feedback. In-band quantization noise that accumulates in the loop filter until it can be quantized where it is then subtracted from the input

pling ratio (OSR) is defined as:

$$OSR = \frac{f_s}{2f_B} \quad (2.2)$$

Due to the oversampling operation, the SQNR is significantly improved and the quantization noise is given as

$$P_e = \frac{1}{OSR} \frac{\Delta^2}{12} \quad (2.3)$$

2.4 Delta Sigma Operation and Noise Shaping

The delta sigma modulator is designed with three primary parts. A loop-filter, that restricts the bandwidth and achieves the appropriate full scale voltage for the quantizer; A quantizer; and a DAC that converts the quantized noise into a feedback input for the loop filter. The core of the loop-filter is an integrator that accumulates noise as the delta sigma modulator operates such that the noise can be quantized in a future time step, significantly reducing the amount of information lost from quantization.

The transfer functions will be split into a signal transfer function (STF) and a noise transfer function (NTF), the latter of which will be used to optimize the attenuation of the noise.

$$Y(z) = L_0(z)U(z) - L_1(z)V(z) \quad (2.4)$$

$$V(z) = Y(z) + E(z) \quad (2.5)$$

$$V(z) = STF(z)U(z) + NTF(z)E(z) \quad (2.6)$$

$$STF(z) = \frac{L_0(z)}{1 + L_1(z)} \quad (2.7)$$

$$NTF(z) = \frac{1}{1 + L_1(z)} \quad (2.8)$$

With all the components of the delta sigma modulator shown, there are three ways the SQNR of the signal can be significantly improved. (1) The oversampling ratio of the quantizer can be increased such that the sampling rate is much higher than the bandwidth of the signal. Such a strategy however requires higher power consumption to produce a higher frequency signal for the quantizer and has diminishing returns as the OSR gets much larger. (2) The levels of the quantizer can be increased with the step size as minimal as possible to improve the resolution. This however requires a larger quantizer block and more stringent circuit design to reduce the effects of nonlinearities. (3) Finally, the loop filter transfer function can be designed with more orders of integration, accumulating errors at a faster speed. This technique entails adding more integrators to the loop filter which creates additional design constraints for the circuit. However, the improvement of the SQNR is significant. As shown by Figure 2.5 for a 3-bit quantizer, the upper limit of the achievable SQNR increases for lower OSRs as the order of the loop filter increases.

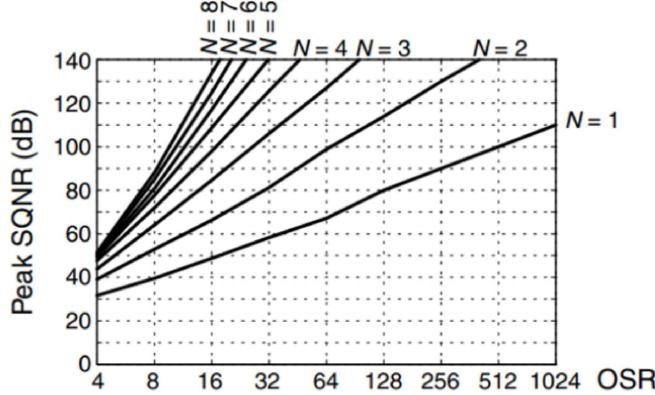


Figure 2.5: Figure from [5] showing the upper theoretical limits of SQNR as the order of a loop filter increases. Lower dynamic power consumption is desirable so ideally as low of an OSR as feasible is desired. However, increasing the order increases circuit complexity as well. Note that this plot shows Peak SQNR; the reality is very different depending on the signal and circuit properties.

2.5 Specifications

This table features a list of all the desired specifications for the ADC. Values such as SNDR, SFDR, and figure of merits (FoM) such as the Schreier FoM and Walden FoM are not included as these need to be experimentally derived and optimized for once a circuit is developed.

Specifications	Goal
SNQR	120 dB
DR	60-80 dB
Bandwidth	500Hz-5kHz
Quantizer Levels	32
Area	Minimal
Power	Minimal

2.6 CIFF Architecture

For systems that involve multiple integrators, the cascade of integrators with feedforward summation (CIFF) architectures appears to be the most ideal for neural recording applications as shown in Figure 2.6. The architecture's noise transfer function and diagram is given below and features multiple

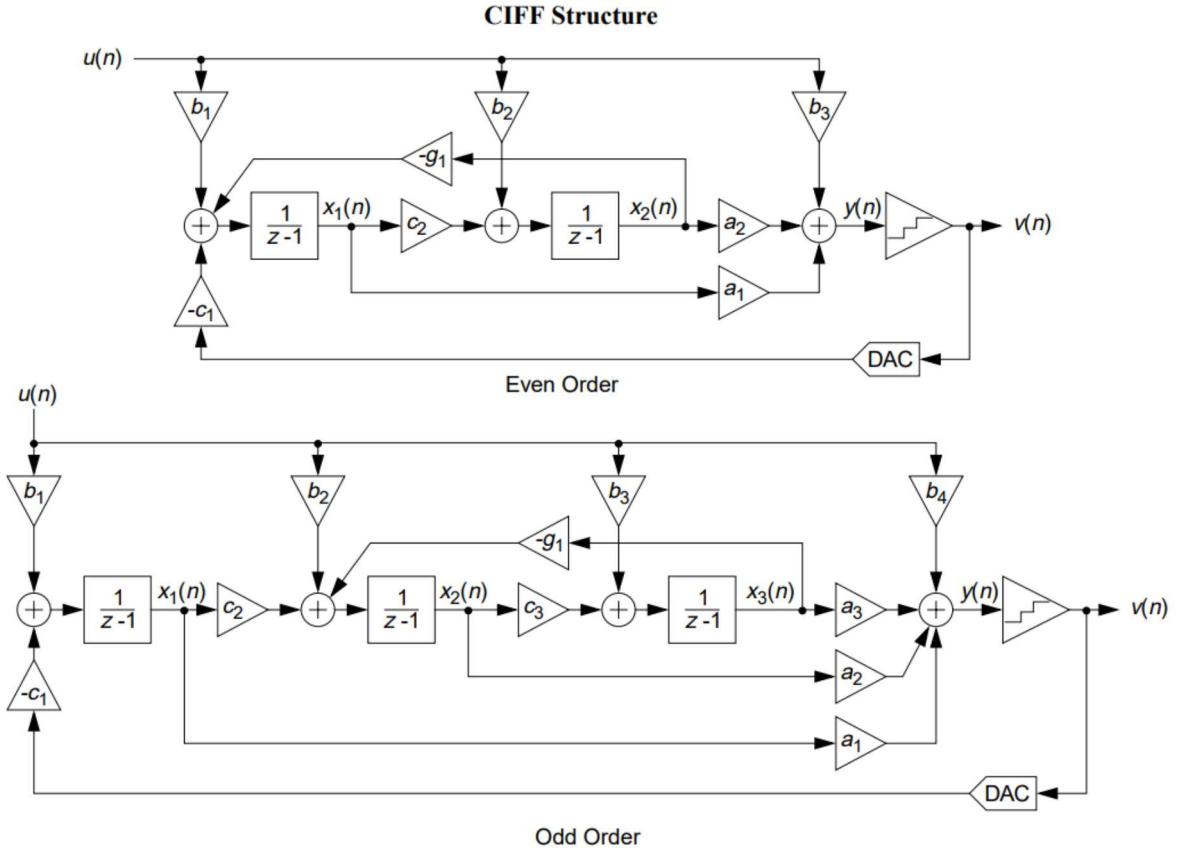


Figure 2.6: Models for a CIFF architecture from [6] depending on whether the loop filter has even or odd order. The most notable aspect of this architecture is the feedforward gains a that send the output of each integrator to the quantizer.

integrators in cascade with feedforward gains that sum at the quantizer. Unlike other higher-order delta-sigma architectures, this does not require the use of multiple DACs for feedback and does not introduce complex-valued zeros that would otherwise introduce oscillations making this the fastest and most power efficient architecture for neural recording applications.

2.7 VCO-Based ADC

Traditionally, quantizers would use an architecture based on ADCs such as FLASH or SAR ADCs. These architectures introduce large resistors and comparator circuits that introduce large thermal noise components into the

system. Clearly, another architecture needs to be used to meet the area, power, and noise constraints of neural recording. VCO-based ADCs rectify this problem by converting the input analog signal into a time-domain signal. VCOs or voltage-controlled oscillators use an input voltage signal to control the phase of an ongoing signal. Signals that are high voltage inputs will generate faster oscillations compared to signals with low voltage inputs, effectively converting the voltage-domain signal into the phase-domain. The phase can then be detected through digital components such as flip flops and XOR-gates. This technique comes with a few major advantages. 1) The entire quantizer is effectively a digital system which allows for ease of circuit design and layout. 2) VCOs can operate under a wide range of input voltages and there aren't metastability concerns that traditionally arise with quantizers with a strict full scale voltage. 3) The transfer function of a VCO, given by the following equation:

$$H_{VCO}(s) = \frac{\phi_{out}}{v_{ctrl}} = \frac{K_{VCO}}{s} \quad (2.9)$$

Where K_{vco} is the gain of the VCO and v_{ctrl} is the input voltage of the oscillator. Note the VCO serves effectively as an integrator, meaning an extra order of noise shaping is achieved. This makes the VCO-based ADC a very attractive choice for a quantizer for a neural recording application. A significant disadvantage of this technique, however, is that the voltage-to-frequency conversion operation is a highly-nonlinear behavior. Closed-loop feedback is still important to maintain high SNQRs with such an architecture.

CHAPTER 3

DESIGN CHOICES

The following chapter presents circuit design choices taken for the loop filter, quantizer, and DAC. Note that the designs for this circuit are still ongoing at the time of this writing and the design choices are not final.

3.1 Loop Filter Design for First Order

Second-order delta-sigma modulators are the lowest-order modulator capable of theoretically reaching approximately 120 dB of SQNR. As a VCO-based ADC achieves one order of noise shaping by itself, this means that only a first-order loop filter is needed for the transfer function. The oversampling ratio is initially set to 500 for a 5kHz bandwidth signal meaning the system is sampled at 2.5 MHz. The transfer function and state-space models of the loop filter will be designed using Delta-Sigma Toolbox in Matlab [6]. After optimizing zeros around the band center such that there are no significant undershoots in the noise-transfer function as well as setting the maximum out-band gain (OBG) to 1.5 to stabilize the system, the noise transfer function and loop filter before accounting for the VCO is given by:

$$NTF(z) = \frac{z - 1}{z + .667} \quad (3.1)$$

and the loop filter is:

$$LF(z) = \frac{0.667}{z - 1} \quad (3.2)$$

The entire system can then be modeled in Simulink to account for additional design parameters as shown in Figure 3.2. Attempts were made to use CppSim for faster simulations of a VCO-based ADC but the design was difficult to implement in the software. The noise transfer function is plotted in Figure with a predicted SQNR of 92.9 dB. While this does not quite reach

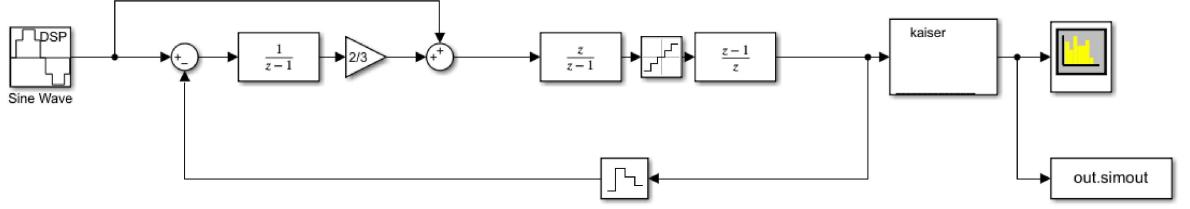


Figure 3.1: Simulink models of the first-order delta-sigma ADC with the VCO-based ADC accounted for. A ZOH block is used to represent the DAC of the system.

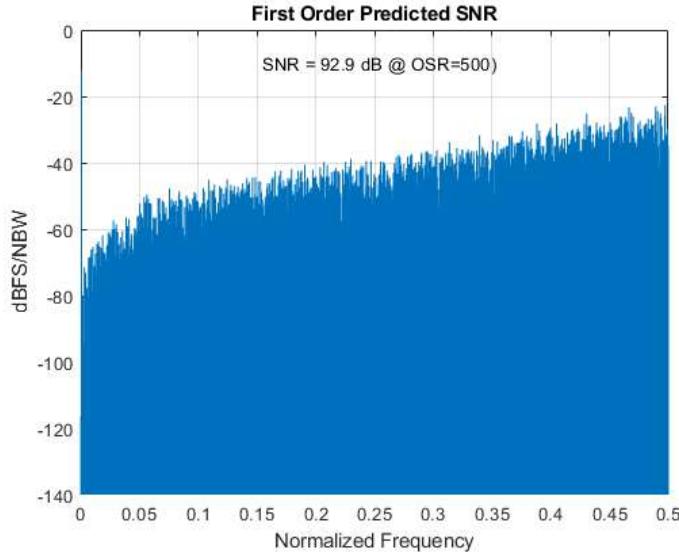


Figure 3.2: Predicted NTF behavior of the first-order delta sigma ADC. The SQNR is found to be 92.9 dB.

the specifications, further tuning of the model should yield a higher SQNR as it is achievable under the theoretical limit.

The basic design of an integrator in a loop filter consists of an op-amp with a resistor and capacitor. The transfer function of such an integrator is given by:

$$V_{out}(s) = -\frac{1}{sCR}V_{in}(s) \quad (3.3)$$

Notably, the use of an op amp leads to a highly linear integrator due to a virtual ground node between the resistor and capacitor. However, this requires that the output of the op amp has as minimal impedance as possible to minimize the effects of parasitic on linearity. One such method is to use a common-drain amplifier as a second stage but this will significantly reduce

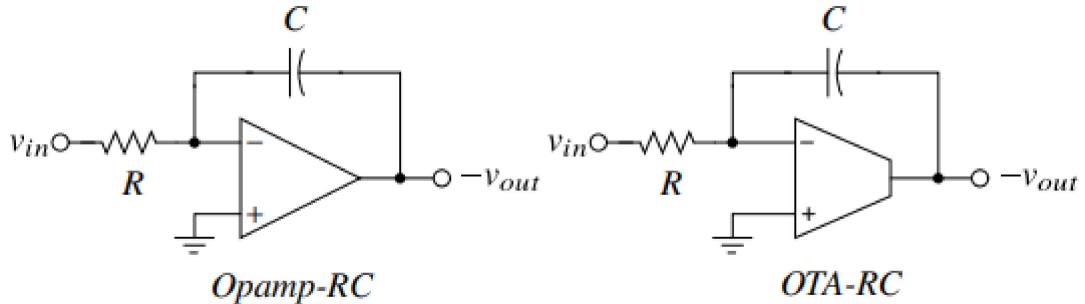


Figure 3.3: Op Amp RC and OTA-RC Models considered for the loop-filter

the output swing of the first stage. Instead, an OTA-RC stage should be used to account for this constraint.

The solution for the transfer function of a OTA-RC stage is given as follows:

$$\frac{v_x - v_{in}}{R} = \frac{v_x - v_{out}}{\frac{1}{sC}} = Gm v_x \quad (3.4)$$

$$(1 - \frac{Gm}{sC})v_x = v_{out} \quad (3.5)$$

$$\frac{v_{out}}{v_{in}} = \frac{1 - \frac{Gm}{sC}}{\frac{1}{GmR}} \quad (3.6)$$

$$\frac{v_{out}}{v_{in}} = -\frac{GmR}{GmR + 1} \frac{1}{sCR} (1 - \frac{sC}{Gm}) \quad (3.7)$$

where v_x is the virtual ground node and Gm is the gain of the OTA. Notably, an RHP zero has been inserted into the system which will cause phase lag. This is not too much of a concern due to the slow bandwidth of the delta-sigma modulator but a $\frac{1}{Gm}$ resistor can be inserted in series to the capacitor scaled by $\frac{GmR}{1+GmR}$ to remove the zero. The value of RC will be equal to the sampling period of the system with R being multiplied by a factor of 3/2 to implement the 2/3 gain in the loop filter.

A fully-differential folded-cascode stage for the OTA is the most optimal architecture for this system due to the need for a high-gain OTA and low power consumption with optimizing for speed not particularly needed. A two-stage system may increase the gain further although further analysis needs to be done to ensure the signal has enough swing. The desired gain of the op amp can be determined through a root-locus analysis of system and the ideal gain-bandwidth product can be found by representing the OTA

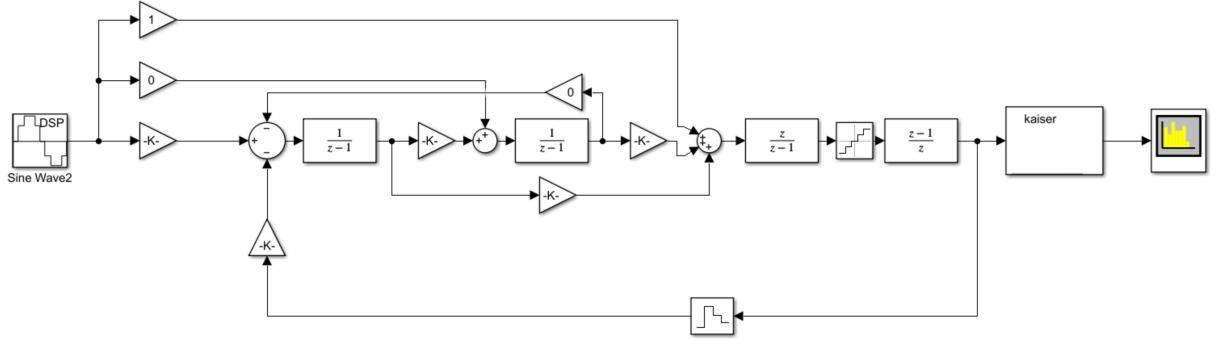


Figure 3.4: Simulink models of the second-order delta-sigma ADC with the VCO-based ADC accounted for. The coefficients were all determined through use of the Delta Sigma Toolbox.

as a one-pole system and sweeping gain versus SNR. This work is currently ongoing.

3.2 Loop Filter Design for Second Order

A similar process of Matlab and Simulink simulations were performed for creating a second-order CIFF-based model. The ideal noise transfer function of the system was found to be:

$$NTF(z) = \frac{(z-1)^2}{(s^2 - 1.225z + .4415)} \quad (3.8)$$

Simulations have predicted an achievable SQNR of a 50% FS signal to be 110.2 dB at an OSR of 500. At FS, the ideal SQNR was found to go as high as 147.1 dB. The model of the CIFF architecture used can be found in Figure 3.4.

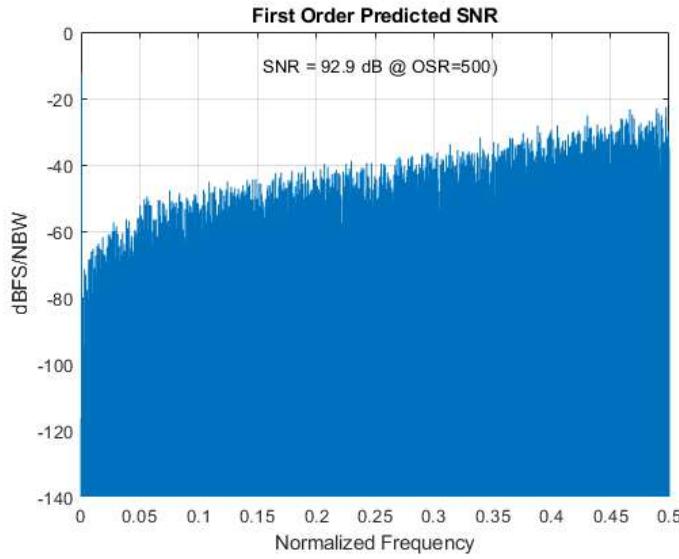


Figure 3.5: Predicted NTF behavior of the second-order delta sigma ADC. The SQNR is found to be 110.2 dB.

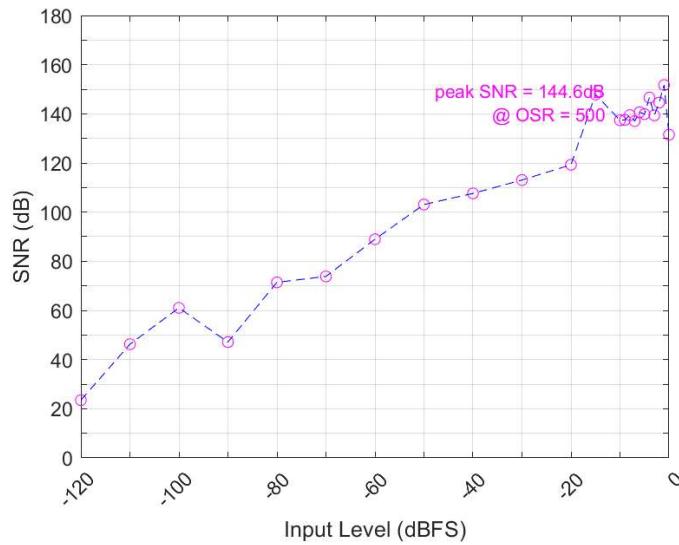


Figure 3.6: Sweep of system SQNR over input full-scale magnitude. The peak achievable SQNR is approximately 147.1 dB.

3.3 VCO-based ADC

The VCO-based ADC uses a 31-stage VCO to produce a 5-bit quantizer. The current choice of architecture is heavily-based on [7] as shown in Figure 3.7 and needs to be tweaked to match the low-bandwidth requirements of this application. It uses a ring-oscillator topology for simplicity of design and has a delay cell. A delay cell was designed to operate at the sampling frequency of 5MHz. However, currently it operates at a much higher frequency so more designs on the delay cell will be needed to achieve the appropriate sampling frequency. Next, two registers are implemented for tracking the difference in phase. These are two true-single phase clock registers to achieve a desired minimal logical delay. The second register is connected to the first register. Finally, a 6-transistor XOR was used to perform the difference operation. The model of the system in Cadence Virtuoso can be found in Figure 3.8.

3.4 DAC

A resistive NRZ DAC was initially explored as it adds the smallest possible thermal noise compared to other DACs. However, in low bandwidth applications, resistive DACs tend to reduce the loop gain due to loading at the input of the integrator worsening the linearity and tend to require large resistors in low-bandwidth designs. A current-steering DAC is likely a more optimal design for the DAC as it features less resistors.

Traditionally, DACs in delta-sigma modulators suffer from mismatches due to the true impedances and capacitances at DAC nodes. This requires the use of a large amount of DACs and a scheme to cycle them to take advantage of redundancy known as dynamic-element matching. With the VCO-based ADCs signal being naturally cycled across several DACs however, there is an implicit barrel-shift DEM scheme being implemented and as of now, there does not appear to be a need implement an additional DEM scheme. However, further simulations on power must be performed as the high switching frequency of a barrel-shift scheme has previously required the use of other DEM schemes to be implemented. [4]

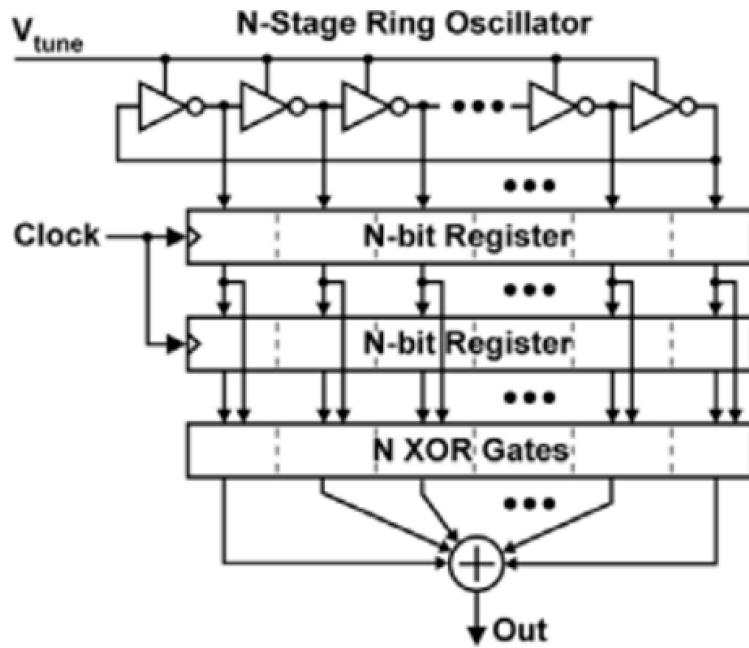


Figure 3.7: Figure from [7] showing block diagram level design of VCO-based ADC

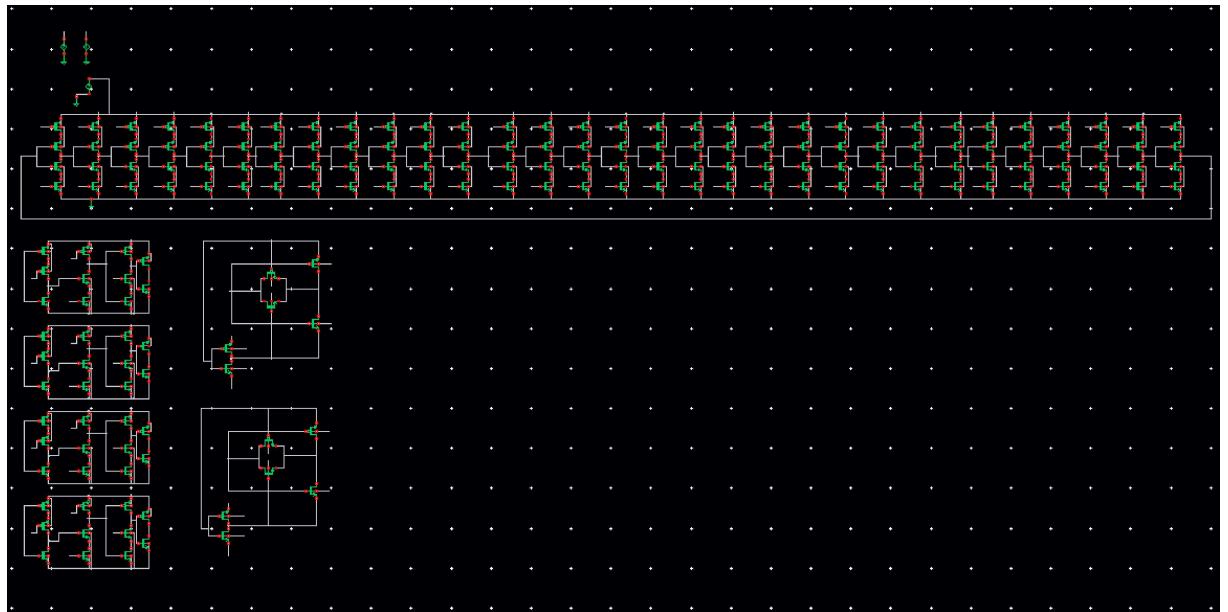


Figure 3.8: Cadence Virtuoso schematic of VCO-based ADC. Features 4-transistor delay cell, a TSPC positive-edge register, and a 6T-XOR gate

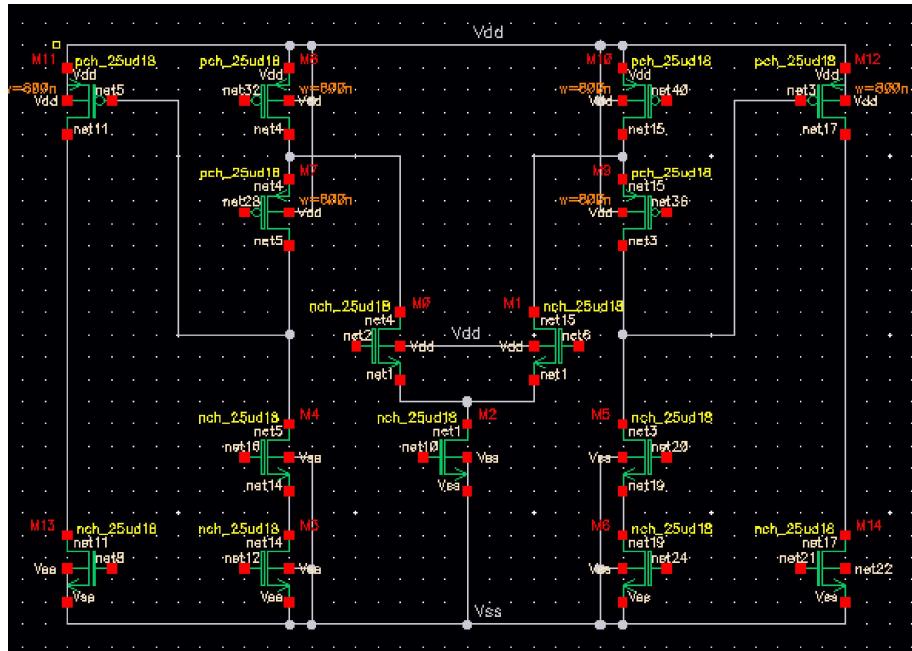


Figure 3.9: Potential 2-Stage Folded-Cascode Integrator Design.
Simulations on gain-bandwidth, noise, and swing will be needed to determine whether this is an appropriate model

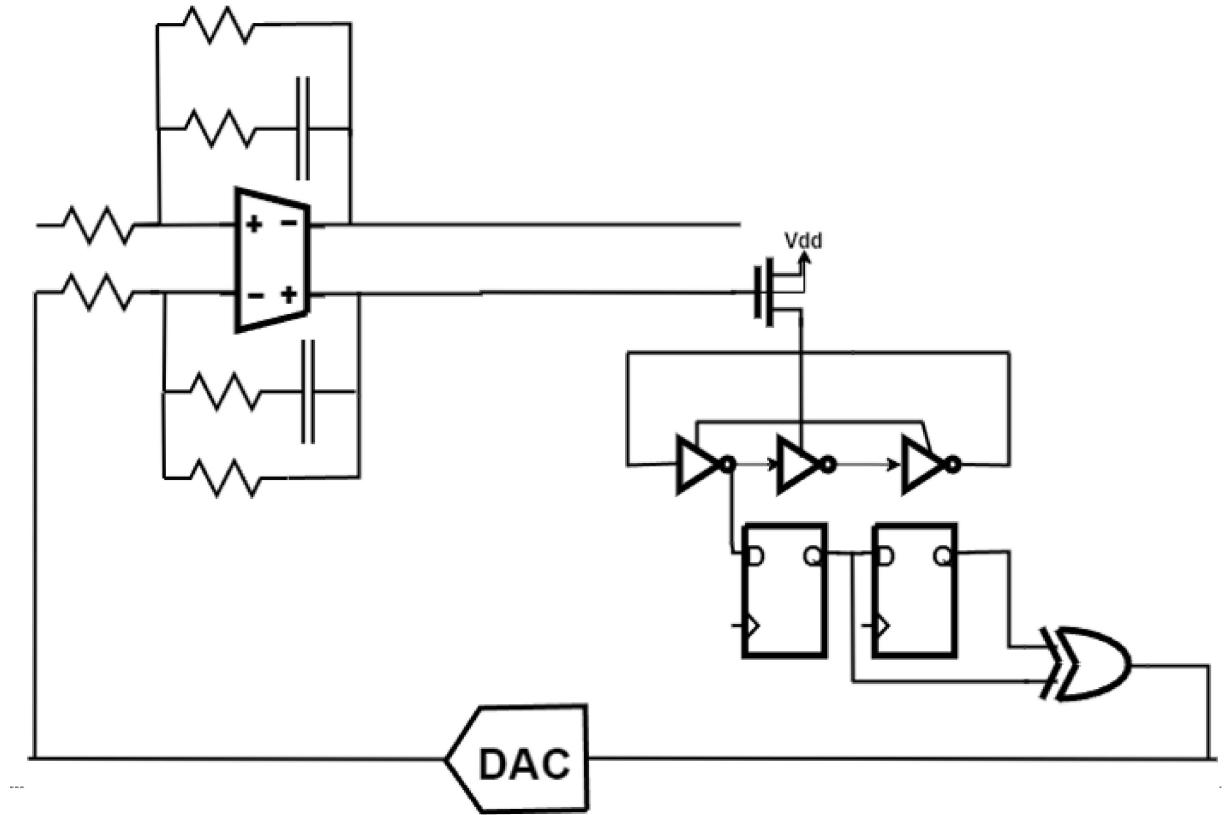


Figure 3.10: High Level Sketch of Second Order VCO-based ADC Design

CHAPTER 4

CONCLUSION

In conclusion, the steps and block-level designs of many continuous-time delta-sigma modulators with VCO-based ADCs were explored. A 92.9 dB and 110.2 dB SQNR model has so far been developed with the use of a 1st and 2nd order loop-filter respectively and a VCO-based ADC. The VCO-based ADC through its advantages in area and power consumption, additional order of noise shaping, and lack of metastability concerns were found to be highly optimal for neural-recording applications. By extension, the low-bandwidth low-power nature of this design could be used in other applications such as environmental sensors and IoT as well.

4.1 Next Steps

The full circuit design of the loop filter, the VCO-based ADC, and the DAC are still in progress. Schematic design will be continued in a TSMC 65nm PDK in Virtuoso. The loop filter still needs to be tested for its true gain-bandwidth product, phase margin, and noise figures. The VCO-based ADC has its register-design and logical effort calculations done but the ring oscillator needs appropriate delay cells to achieve the desired frequency. DAC designs need to be explored further to pick out the optimal architecture as well.

Further work may head in the direction of digital modelling of VCO-based ADCs. EDA tools like Virtuoso and SPICE as well as modelling tools like Verilog-A, Simulink, or CppSim tend to take long amounts of time performing numerical solutions of analog systems. Tools such as the MATLAB Delta Sigma Toolbox have been important in the design of delta-sigma modulators through state-space solutions but EDA-integrated tools would be needed to facilitate better design. As loop-filters and DACs can be expressed in

transfer function form and VCO-based ADCs are highly digital blocks, using event-driven or real number value models in SystemVerilog may facilitate fast simulation of delta-sigma modulators.

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