2021 IWLS Programming Contest: Team NTU-ALCOM

Authors: <u>Po-Chun Chien</u>, Yu-Shan Huang, Nai-Ning Ji, Hao-Ren Wang, Jie-Hong Roland Jiang <u>ALCom Lab</u>

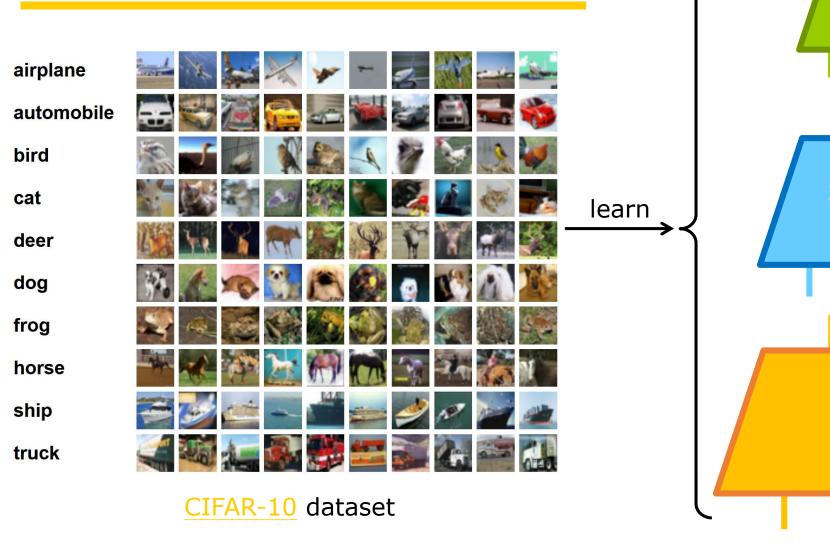


Graduate Institute of Electronics Engineering National Taiwan University





Problem Description



Small ≤ 10K gates AIG Medium ≤ 100K gates AIG Large ≤ 1M gates AIG

Problem Description

□ Target function to be learned:

height width #channels #bits per pixel
$$32 \times 32 \times 3 \times 8$$

$$f: \{0,1\}^{24,576} \rightarrow \{0,1\}^{10}$$

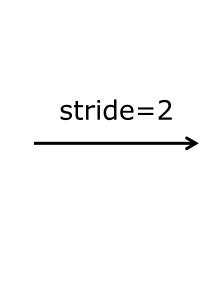
24,576 is larger than the size limit 10,000 of small AIGs!



Image Preprocessing

Down-sampling

0,0	0,1	0,2	0,3
1,0	1,1	1,2	1,3
2,0	2,1	2,2	2,3
3,0	3,1	3,2	3,3



0,0	0,2
2,0	2,2

1,0	1,2
3,0	3,2

0,1	0,3
2,1	2,3

1,1	1,3
3,1	3,3



Image Preprocessing

■ Bit truncation of each pixel

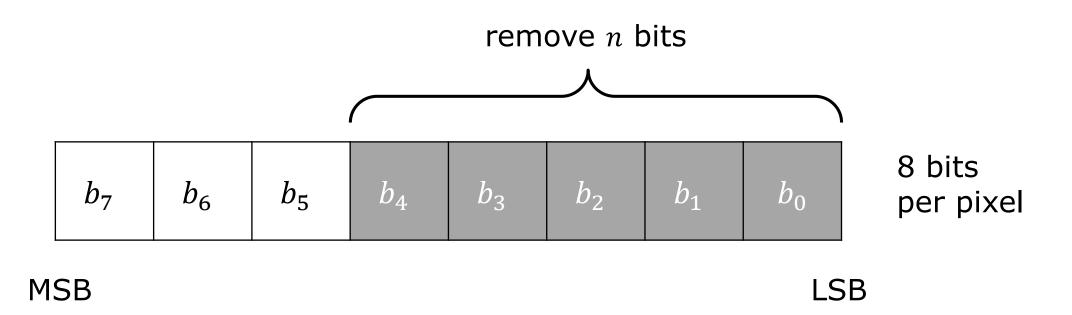




Image Preprocessing

□ Augmentation: flip, shift, scale, rotate...

0,0	0,1	0,2	0,3
1,0	1,1	1,2	1,3
2,0	2,1	2,2	2,3
3,0	3,1	3,2	3,3

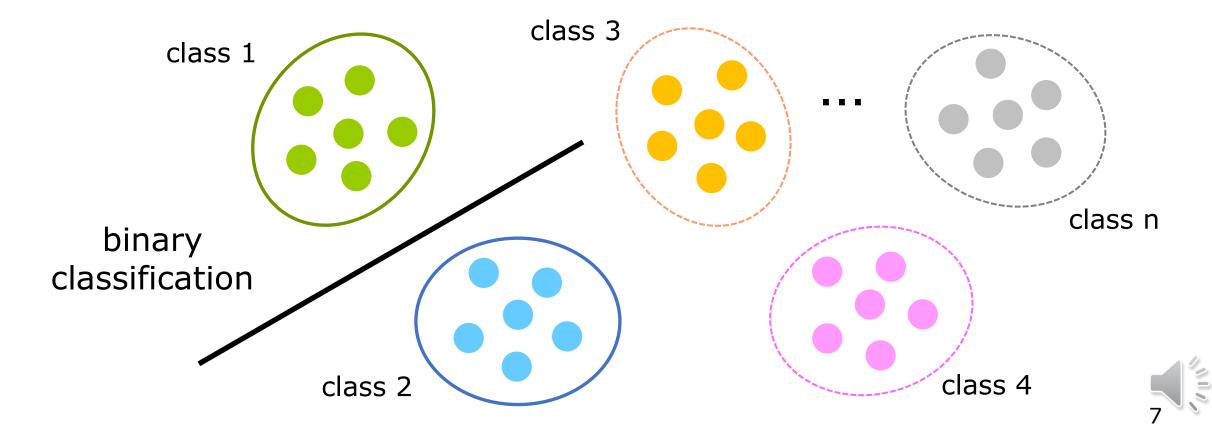


0,3	0,2	0,1	0,0
1,3	1,2	1,1	1,0
2,3	2,2	2,1	2,0
3,3	3,2	3,1	3,0



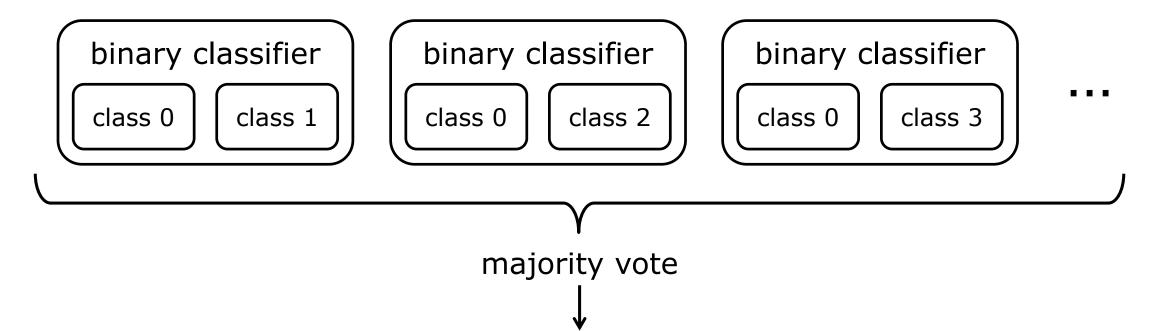
Learning Small Circuits

Construct multi-class classifier using one-against-one (OAO) approach with binary classifiers.



Learning Small Circuits

□ For CIFAR-10 dataset, there are C(10,2) = 45 binary classifiers in total.



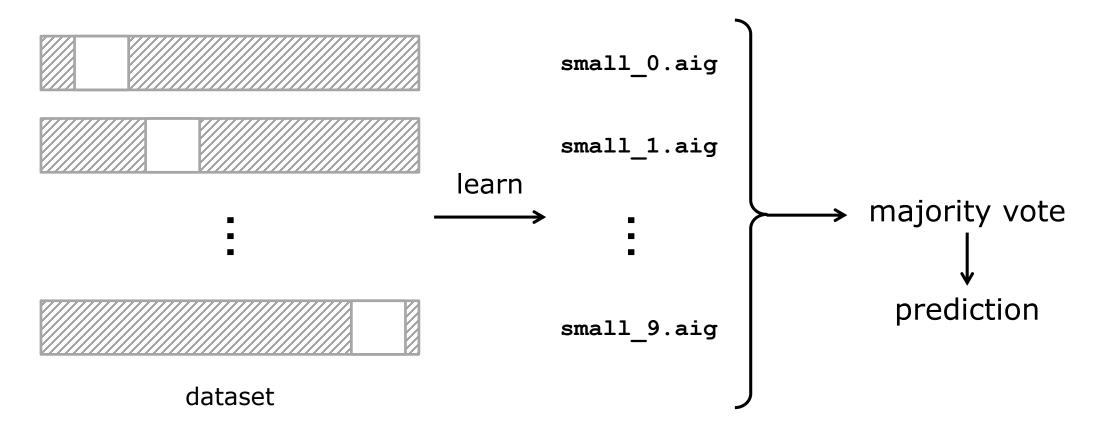
prediction

Learning Small Circuits

- □ Type of binary classifier:
 - decision tree classifier from scikit-learn [1]
- □ To restrict size and avoid overfitting:
 - maximum tree depth (max depth)
 - cost complexity pruning (ccp_alpha)

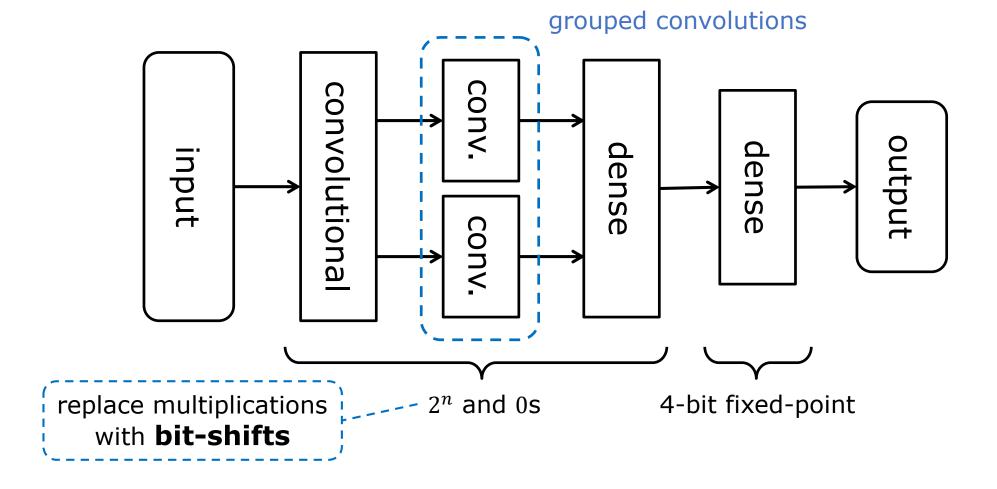
Learning Medium Circuits

■ Ensemble of 10 small classifiers trained with different portions of the dataset.



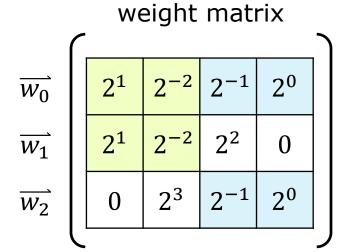
Learning Large Circuits

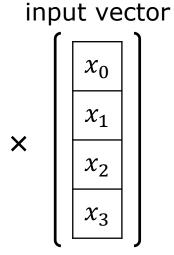
Shallow CNN with grouped convolutions and quantized weights.

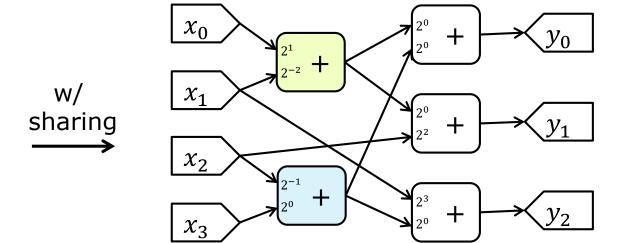


Learning Large Circuits

CNN synthesized with sub-adder sharing [3].







output vector

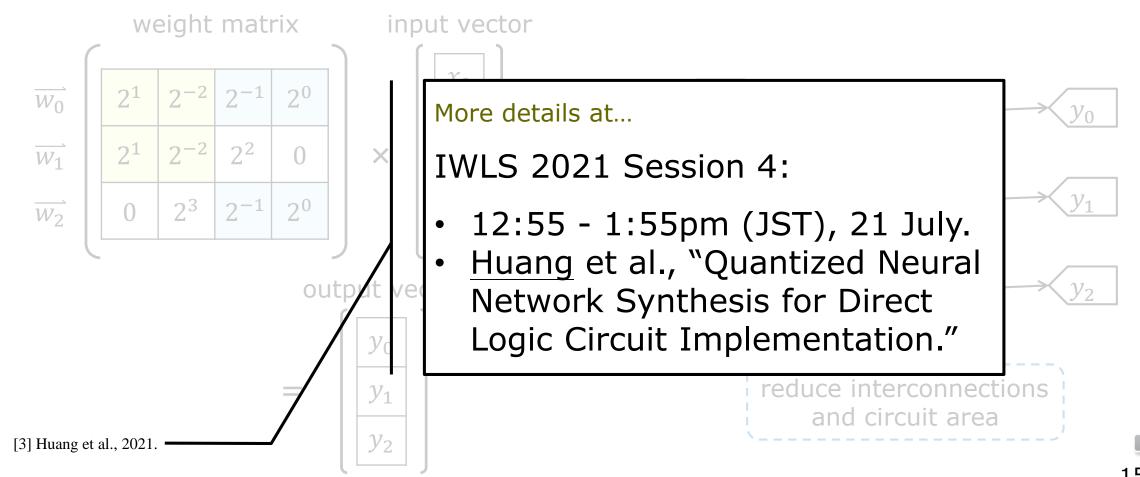
$$= \begin{bmatrix} y_0 \\ y_1 \\ y_2 \end{bmatrix}$$

reduce interconnections and circuit area

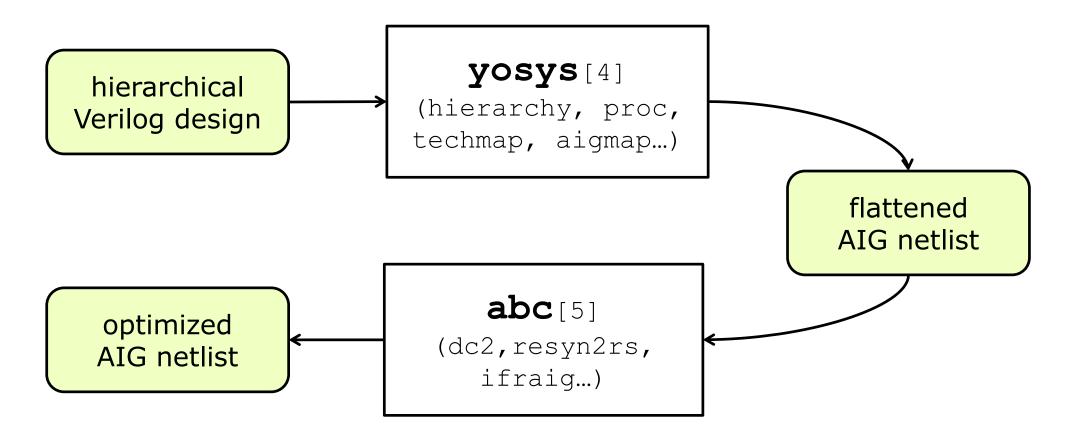
(30% lesser AIG-nodes)

Learning Large Circuits

CNN synthesized with sub-adder sharing [3].



Logic Synthesis



Our Results

Submitted version

	small	medium	large
size (#gates)	9,697	97,350	995,247
training acc.	44.96%	56.77%	59.33%
testing acc.	39.31%	44.69%	54.68%

Our Results

□ Newer version (after fine-tuning and bug fixing)

	small	medium	large	
size (#gates)	9,697 → 9,273	97,350 → 99,873	995,247 → 967,173	
training acc.	44.96% → 43.89%	56.77% → 54.99%	59.33% → 59.18	}
testing acc.	39.31% → 39.51%	44.69% → 45.44%	54.68% → 56.34	

smaller gap (less overfitting)

higher

Conclusions

Our methods and results can be summarized as follows.

	small	medium	large
model structure	decision tree	decision tree	neural network
size (#gates)	9,273	99,873	967,173
testing acc.	39.51%	45.44%	56.34%

■ The source code will be made public at https://github.com/NTU-ALComLab/IWLS2021.

THE END