

# PO-CHUN CHIEN

☎ +886-970760058    ✉ r07943091@ntu.edu.tw    🏠 b04901112.github.io

## RESEARCH INTERESTS

---

**Formal Verification:** Soft/Hard-ware Model Checking, QBF/SAT Solving, Automata Theory  
**Electronic Design Automation (EDA):** Logic Synthesis & Optimization, Computation Models  
**Machine Learning (ML):** Decision Tree, Deep Learning (DL), Machine Comprehension

## SKILLS

---

Programming: proficient in **C/C++**, **Python**, **VerilogHDL**, Cadence Skill, MATLAB  
Language: Mandarin Chinese, **English (IELTS 7.5, TOEFL 103, GRE 155/170/4.0)**

## EDUCATION

---

Received both B.S. and M.S. degree from **National Taiwan University (NTU)**. *Taipei, Taiwan*

**M.S. in Graduate Institute of Electronics Engineering (GIEE)** *Sep. 2018 - June 2020*

- Major in EDA, instructed by Prof. Jie-Hong Roland Jiang of ALCom Lab
- Overall GPA: 4.22 / 4.30

**B.S. in Department of Electrical Engineering** *Sep. 2015 - June 2018*

- Overall GPA: 4.16 / 4.30 *Top 5%*

## ACADEMIC/CONTEST AWARDS

---

2020 Lam Research Masters Thesis Excellence Award at NTU *Nov. 2020*  
**1<sup>st</sup> place** in the Chinese Institute of Electrical Engineering Thesis Award *Oct. 2020*  
**1<sup>st</sup> place** in 2019 ICCAD CADathlon *Nov. 2019*  
**1<sup>st</sup> place** in Formosa Grand Challenge “Taking with AI” *Mar. 2019*  
**GIEE scholarship** \* 4 semesters *Sep. 2018 - June 2020*  
**TSMC-NTU scholarship** \* 2 semesters *Sep. 2017 - June 2018*  
**NTU Presidential Award** \* 2 semesters *Sep. 2016 - June 2017*

## PUBLICATIONS

---

**P.-C. Chien** and J.-H. R. Jiang. Time Multiplexing via Circuit Folding. In Proc. of the IEEE/ACM Design Automation Conference (DAC), 2020.  
**P.-C. Chien**. Circuit Folding: From Combinational to Sequential Circuits. Master’s Thesis, National Taiwan University, 2020.  
**P.-C. Chien** and J.-H. R. Jiang. Time-frame Folding: Back to the Sequentiality. In Proc. of the IEEE/ACM International Conference of Computer-Aided Design (ICCAD), 2019.

## WORK EXPERIENCE

---

**Research Assistant** in ALCom Lab at NTU *July 2020 - present*  
**Teaching Assistant** of “Introduction to EDA” at NTU *Mar. - July 2020*  
**Teaching Assistant** of “Introduction to EDA” at NTU *Mar. - July 2019*  
**Teaching Assistant** of “DL for Human Language Processing” at NTU *Sep. 2018 - Jan. 2019*  
**Teaching Assistant** of “Advanced Deep Learning” at NTU *Mar. - July 2018*  
**Summer Intern at MediaTek ADCT/PDK Dept.** *Hsinchu, July - Aug. 2018*  
· Develop an automatic virtual-pin labeler for LVS on analog circuits.

## RESEARCH PROJECTS

---

### Compatible Equivalence Checking of X-valued Circuits

*July 2020 - present*

- Verify the equivalence of 2 X-valued (ternary logic) netlists, with the X-values serving as don't cares.
- Construct the miter circuit with dual-rail encoding, and adopt various optimization techniques.
- Identify and utilize the compatible equivalence relations of internal signals to guide the SAT solver.

### Machine Learning + Logic Synthesis

*May 2020 - present*

- Learn an unknown Boolean function from a training set consisting of input-output pairs.
- The learned function is in the form of And-Inverter Graph with strict hardware cost ( $\leq 5000$  gates).
- Methods: decision tree with fringe-feature detection, and neural network with pruning and quantization.
- Our team achieved the highest testing accuracy in most cases in the IWLS 2020 Programming Contest.

### Time Multiplexing (TM) via Circuit Folding

*Nov. 2019 - July 2020*

- The research manuscript was accepted and published by **DAC 2020**.
- TM is an important technique to overcome the I/O bandwidth bottleneck of FPGAs.
- Our new formulation achieves TM through structural and functional circuit folding at the logic level.
- Experiments show the effectiveness of the structural method and improved optimality of the functional method on look-up-table and flip-flop usage.

### Time-Frame Folding (TFF): Back to the Sequentiality

*Sep. 2018 - Nov. 2019*

- The research manuscript was accepted and published by **ICCAD 2019**.
- TFF is the reverse operation of time-frame expansion. It constructs a sequential circuit from an  $k$ -iterative combinational circuit.
- The constructed circuit is equivalent to the original circuit within the bounded  $k$  time-frames.
- Empirical evaluation demonstrates its ability in circuit size compaction and suggests potential use in testbench generation and bounded strategy generalization.

### Formosa Grand Challenge “Taking with AI”

*June 2018 - Mar. 2019*

- A nationwide ML competition hosted by Taiwan Ministry of Science and Technology.
- The goal is to build a conversational AI agent that understands Mandarin Chinese.
- Our team **ranked 1<sup>st</sup>** in the competition and won the final prize.

### Deep Neural Network using Stochastic Computing

*Sep. 2017 - June 2018*

- Implement Multiply-Accumulate (MAC) and various operations via stochastic computation.
- Build a neural network with lower hardware cost in terms of power consumption area-delay product on FPGA boards (Altera DE10-nano).
- **Regional Finalist** in Greater China of Innovate FPGA 2018.

## RELATED COURSE

---

**Verif.** SoC Verification, Logic Synthesis & Verification, Algorithms

**EDA** VLSI Testing, Physical Design, Data Structure & Programming

**ML** ML & have it deep and structured, Advanced DL, DL for Human Language Processing

**Others** Advanced Computer Architecture, Digital Signal Processing, Introduction to Cryptography

## PERSONAL TRAITS

---

Highly motivated and eager to learn new things.

Capable of working as an individual as well as in groups.

Hard-working and good at time management.