RK3288 SPA REF V1.0

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I2C address(7bit):

1.I2C0 Power: RK818 0x1C SYR827 0x40

2.I2C1 Sensor:

CM3218 0x10,0x0c

LSM330TR G:0x6a A:0x1e

MMA8452Q 0X1d MPU6500 0x34 LIS3DH 0X19 LSM303D 0X1d

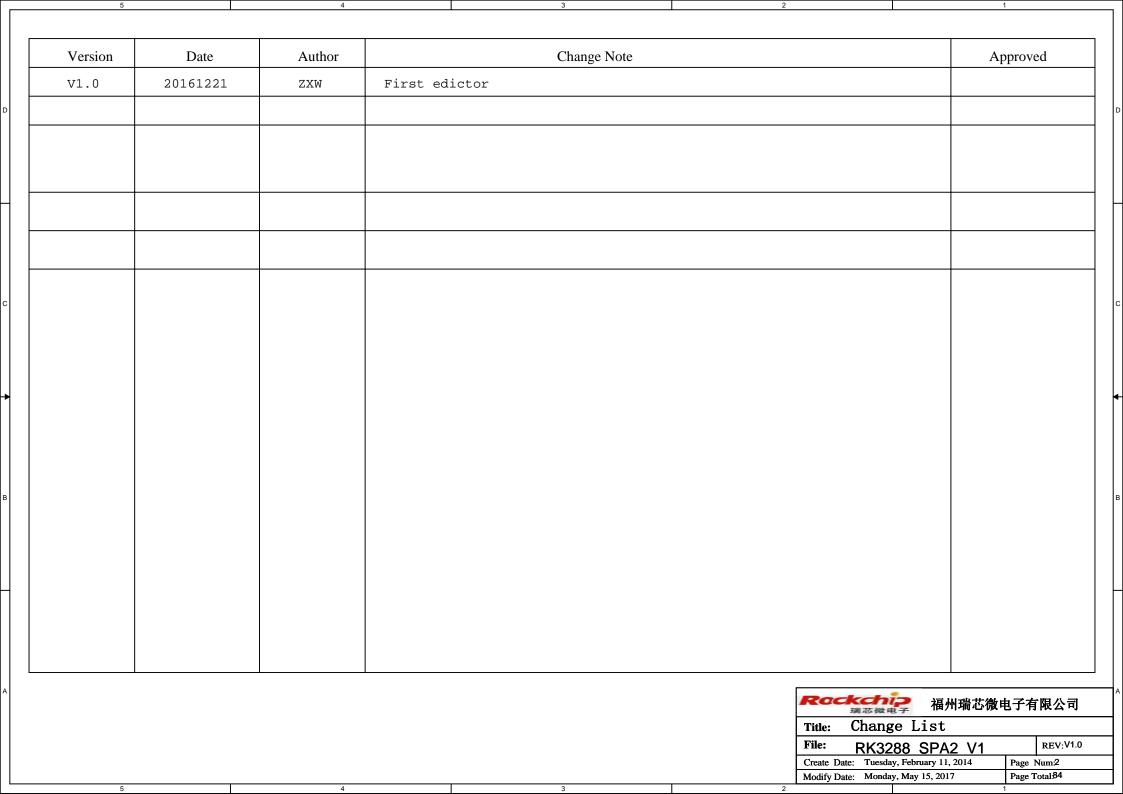
3.I2C2 Audio Codec:

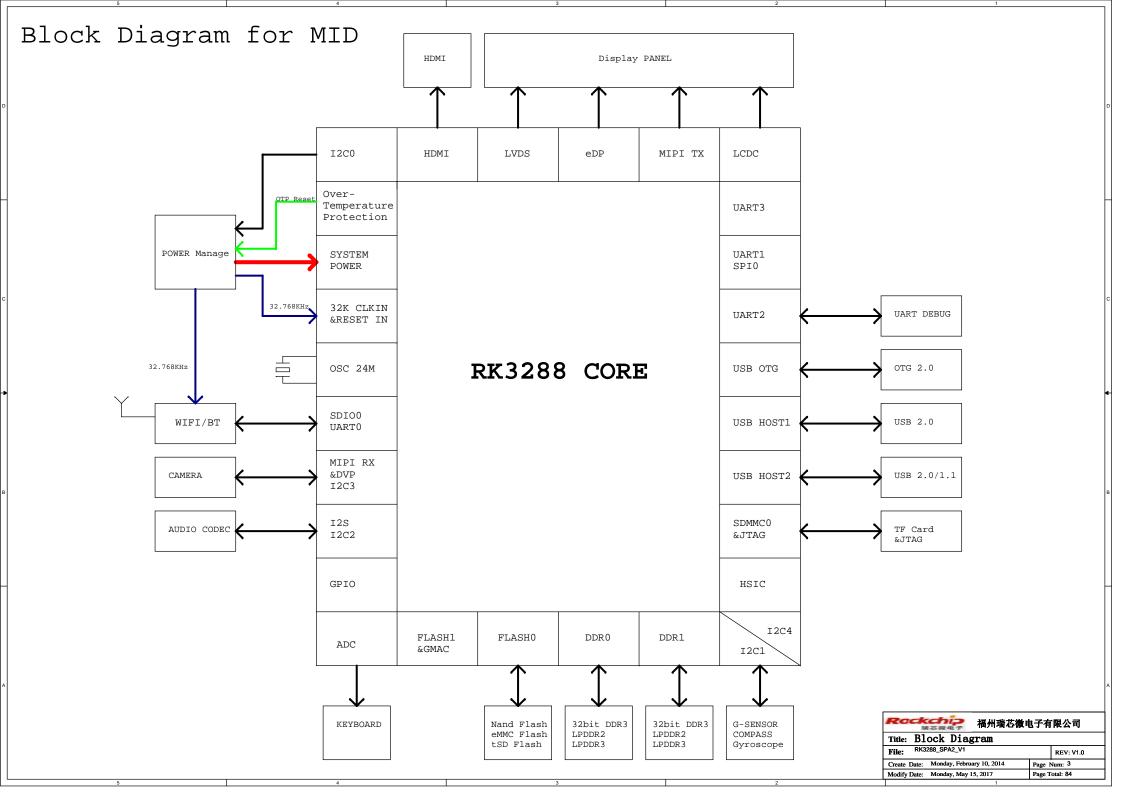
ALC5631 0x1a ES8316 0x10

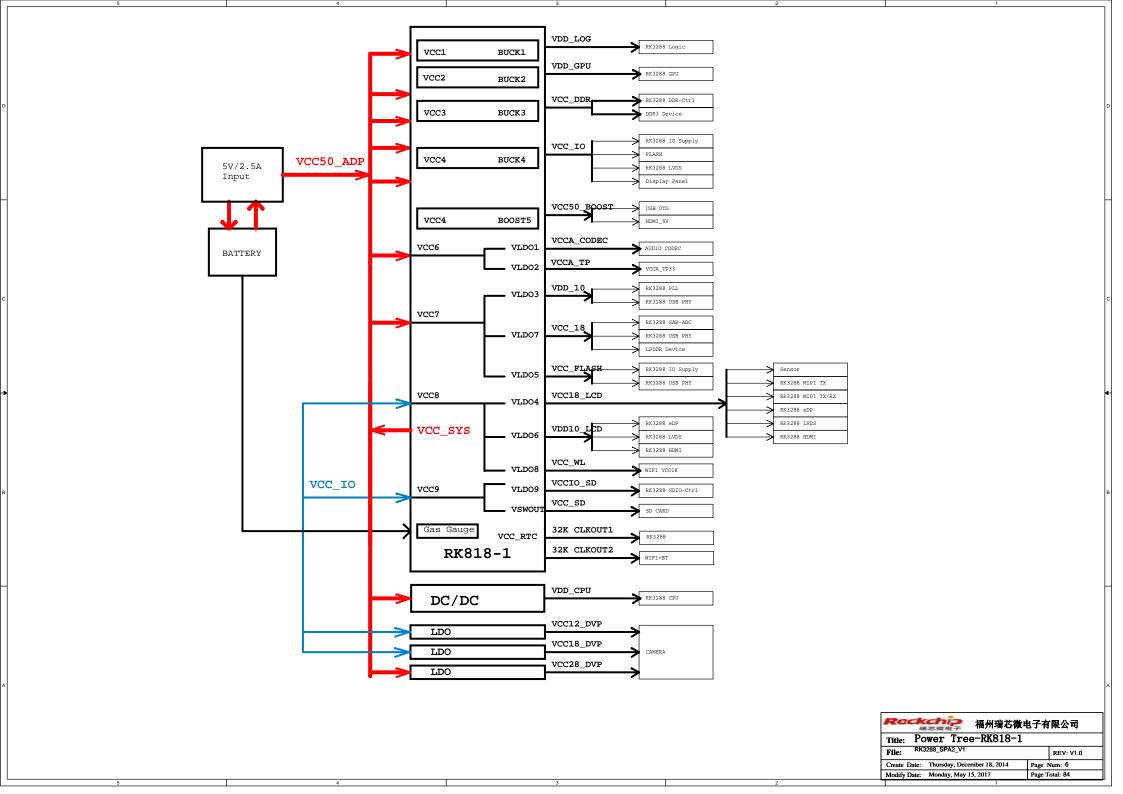
4.I2C3 Camera:

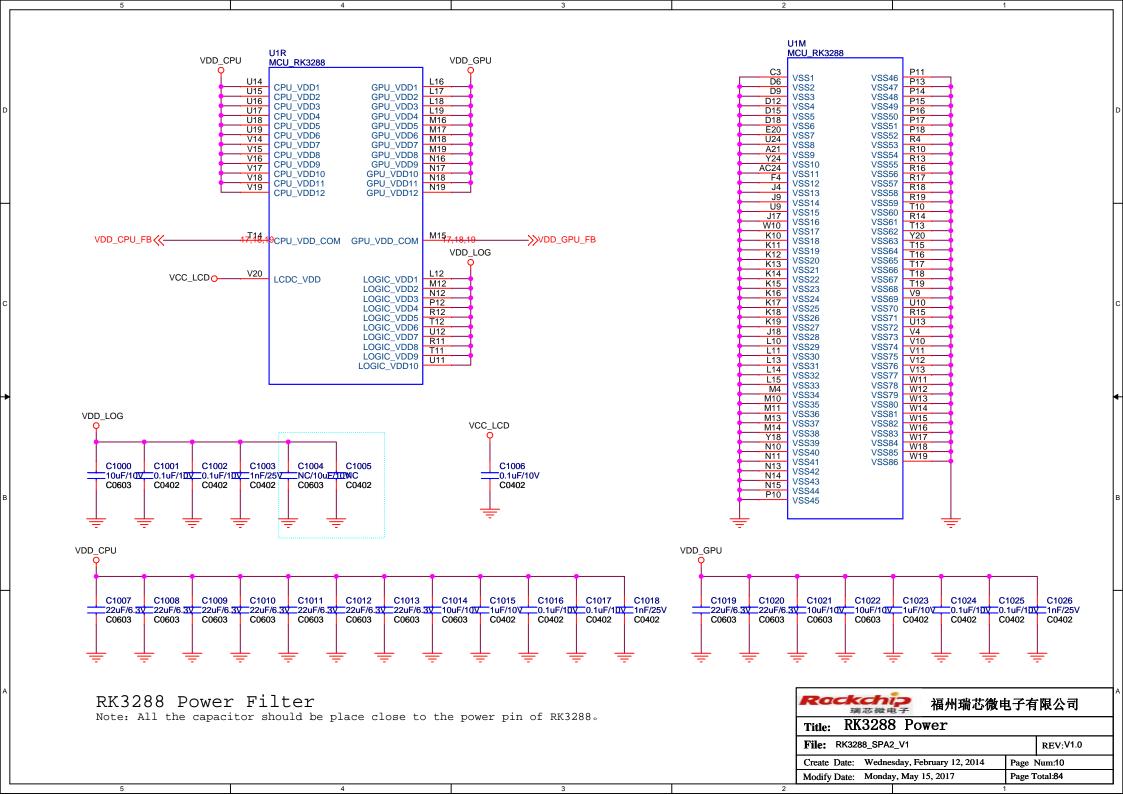
OV2659 0x30 OV8825 0x36

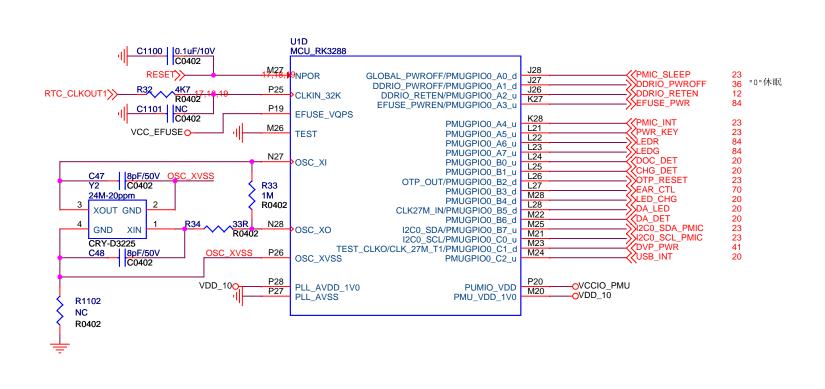


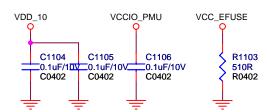








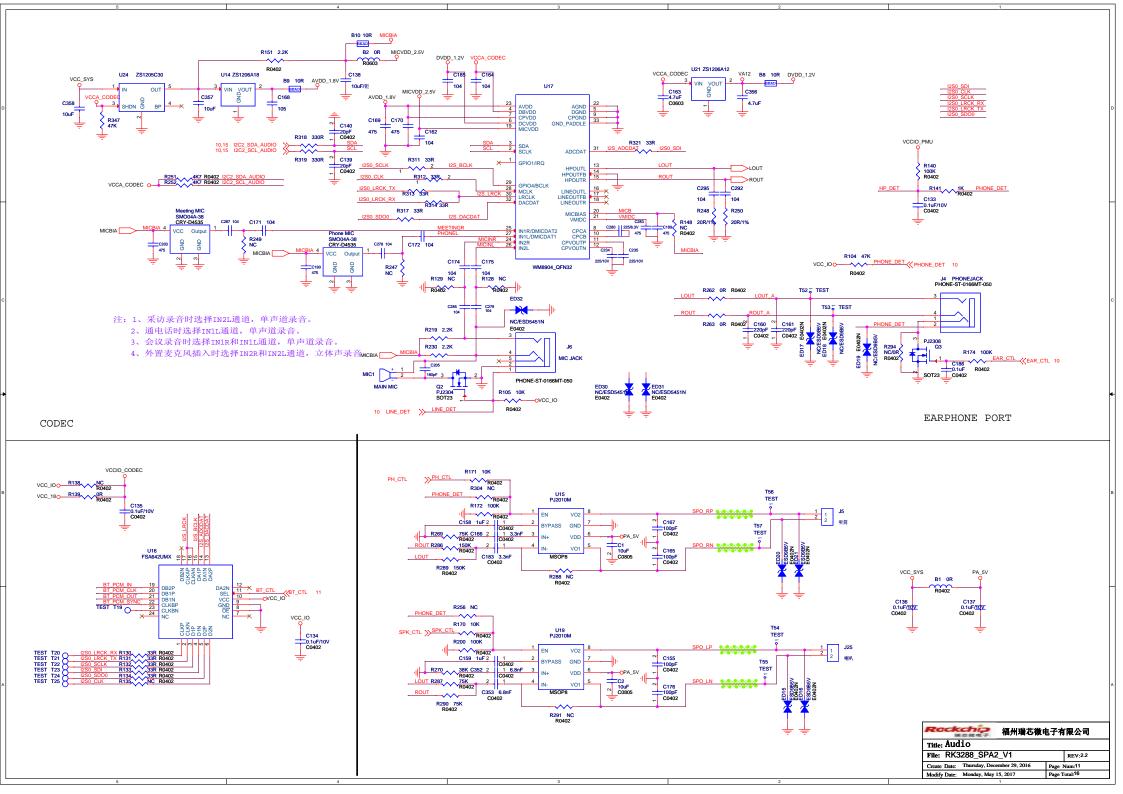




Note: All the capacitor should be place close to the power pin of RK3288.



3 2



RK3288 DDR Channel-0 RK3288 DDR Channel-1 MCU_RK3288 MCU_RK3288 B10,1,22,23,24,25,26 C1f,1,22,23,24,25,26 A10,1,22,23,24,25,26 E12,1,22,23,24,25,26 W2 23@#£5,26Q0 3.084.3.500.1 3.084.3.501.1 3.084.3.501.1 3.084.3.501.2 3.084.3.502.2 3. DDR0_A1 DDR0_A2 DDR' DDR1_A2 M521,22,23,24,25,26 DDR1_A4 M621,22,23,24,25,26 DDR1_A5 M21,22,23,24,25,26 M421,22,23,24,25,26 DDR0 D3 DDR1 D3 DDR0 A4 DDR1_A4 DDR1_A5 DDR1_A6 M321,22,23,24,25,26 M321,22,23,24,25,26 DDR0 D DDR0_A5 DDR1 DDR0 A6 DDR0_A0 A12, DDR0_A8 A14, DDR1_A6 DDR1_A7 DDR1_A8 DDR1_A9 DDR1_A10 P1 DDR1 D7 DDR0_D9 DDR0_D10 DDR1 DDR1 A9 DDR0_A10 D14 DDR1_A10 DDR1_A11 DDR1_A12 DDR1_A13 DDR1_A13 DDR1_A13 DDR0_A11 F14 DDR0 D11 DDR1 D1 SDDR1 A11 DDR0_D12 DDR0_D13 DDR0_A12 DDR0_A13 B14 DDR1 D1 DDR1_A13 DDR0 D14 DDR1 D14 DDR0_A14 DDR1 A14 DDR0_D15 DDR0_D16 DDR1_A15 DDR0 A15 DDR1 D16 DDR1_CLK L2 21,22,23,24,25,26 DDR1_CLK DDR1_CLKn DDR1_CLKn DDR1_CLKn DDR0 D18 SDDR0 CLKN **DDR1 D18** DDR0_D19 (DDR1_D19 DDR1_D20 NORO BAO DDR1_BA0 DDR0_BA1 DDR0_BA2 DDR1_BA1 DDR1_BA2 E15 DDR0_D22 DDR1_D22 DDR0_D23 < DDR0_D24 < SSDDR0 ODT0 DDR1 D24 -SSDDR1 ODTO DDR0_ODT0 DDR0_D25 DDR0_ODT1 DDR1_ODT1 DDR1 D25 DDR0_D26 DDR0_D27 DDR1_D26 DDR1_D27 B8 21,22,23,24,25,26 F1 51 23 24 25,26 H2_{21,22,23,24,25,26} DDR1_CS0N J3_{21,23,24,25,26} DDR1_CS1N DDR0_CSn0 DDR1_CSn0 DDR0_D28 DDR0_D29 DDR1_D28 DDR1_D29 DDR0_CSn1 DDR1_CSn1 F1 21,22,23,24,25,26 DDR1_CKE0 DDR1_CKE1 DDR0 CKE0 DDR1 CKE0 DDR0 D31 (DDR1 D31 2.42.28645.260S0 2.43.38645.260S0 2.63.38645.260S0 2.63.38645.260S1 2.63.28645.260S1 2.63.28645.260S2 2.63.28645.260S2 2.63.28645.260S3 2.63.28645.260S3 2A20 236646.260S0 B20 236646.260S0 B2 236846.360S1 24 32 23646.360S1 24 32 23646.360S1 25 23646.360S2 24 32 23646.360S2 24 32 23646.360S2 24 32 23646.360S3 NODRO RASN ->>DDR1_RASN DDR0 DQS0P / DDR0_RASn DDR1 DQS0P / DDR1_RASn DDR0_CASn DDR1 CASn DDR0_DOS1P DDR0_WEn SODRO WEN DDR1_DOS1P DDR1_WEn SDDR1 WEN DDR0_DQS1M DDR1_DQS1M E9 21.22 DDR0_RESET < <p>✓< DDR0_RST</p> DDR1_RESET ->>DDR1_RST DDR0_DQS2M M8 H12 DDR1_DQS3P DDR0_DOS3P -OVREE DDRO OVREE DDR1 DDR0_VREF DDR1_VREF H11 -OVREFAO DDR0 L8 -OVREFAO DDR1 DDR0_VREFAO DDR1_VREFAO 2 5 2 3 3 5 8 5 2 6 M 0 2 1 5 2 3 3 5 6 8 5 2 6 M 1 2 1 5 2 3 3 5 6 8 5 2 6 M 2 2 1 5 2 3 3 5 6 8 5 2 6 M 3 P7 R7 × L7 × G14 G15 G11 1 U5 23 BBR 5,26M0 1 G5 23 BBR 5,26M1 1 B3 23 BBR 5,26M2 1 D3 23 BBR 5,26M2 1 D3 23 BBR 5,26M3 DDR0 DM0 < DDR0_DM1 < DDR1_DM1 < NC2 NC5 NC3 NC6 H9 OVCC DDRC OVCC DDRC G8 × G12 × H15 × H17 DDR0_VDD1 VDD1 H7 DDR1_RETLE DDR1_VDD1 L9 DDR1_VDD2 M9 DDR0 RETLE DDR0_VDD2 DDR0_ATO DDR0_VDD3 DDR1_VDD3 DDR0_DTO1 DDR0_VDD4 DDR1_VDD4 DDR0_DTO0 DDR1_VDD5 P8 DDR0_VDD5 ×G17 H14 __OVCC_DDR OVCC DDR DDR1_PZQ R1201 R0402 240R%1 R0402 240R%1 R1200 DDRIO_RETEN R1203 100K R0402 R1202 100K R0402 120K DDRIO RETEN S || R1205 82K R0402 R1204 82K R0402 T.DDDD2/3 100% 82K VCC_DDRC VCC_DDR VCC_DDRC VREF_DDR0 VCC_DDRC VCC_DDR VCC_DDRC VREF_DDR1 R1206 1K%1 R0402 R1207 1K%1 R0402 C1201 C1202 C1203 R1208 C1204 C1206 C1208 R1209 C1209 0.1uE/10 1nF/25\/ 0.1uE/10V 11/0/1 0.1uF/10 0.1uE/10V 1K%1 C0603 C0402 C0402 C0402 R0402 C0402 C0402 C0402 C0402 C0402 R0402 C0402 VCC_DDR VCC_DDR C1210 | 0.1uF/10V | C0402 VRFFAO DDRO C1211 | 0.1uF/10V | C0402 VREFAO_DDR1 R1210 10K%1 R1211 10K%1 C1212 C1213 C1214 0 10F/10V 1nF/25V 0.1uE/10V 1nE/25\ Rockchip 第8後电子 C0402 C0402 福州瑞芯微电子有限公司 Title: RK3288 DDR Controler RK3288 K RK3288_SPA2_V1 REV:V1.0 RK3288 L Note: All the capacitor should be place close to Note: All the capacitor should be place close to Page Num:12 Create Date: Saturday, January 11, 2014 the power pin of RK3288. the power pin of RK3288. Modify Date: Monday, May 15, 2017 Page Total:84

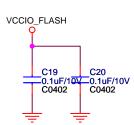


FLASH0_D0/EMMC_D0/GPIO3_A0_u FLASH0_D1/EMMC_D1/GPIO3_A1_u FLASH0_D2/EMMC_D2/GPIO3_A2_u FLASH0_D3/EMMC_D3/GPIO3_A3_u FLASH0_D4/EMMC_D4/GPIO3_A5_u FLASH0_D5/EMMC_D5/GPIO3_A5_u FLASH0_D6/EMMC_D6/GPIO3_A6_u FLASH0_D7/EMMC_D7/GPIO3_A7_u	AE37, 28, 29 AD37, 28, 29 AF3, 7, 28, 29 AF3, 7, 28, 20 AF3, 7, 28 AF3, 7, 28 AG37, 28 AG37, 28 AG37, 28 AG37, 28 AG37, 28 AF3, 7, 2
FLASHO_RDY/GPIO3_B0_u FLASHO_WP/EMMC_PWREN/GPIO3_B1_d FLASHO_RDN/GPIO3_B2_u FLASHO_CLE/GPIO3_B3_d FLASHO_CLE/GPIO3_B4_d FLASHO_CLE/GPIO3_B5_u FLASHO_CSNI/GPIO3_B5_u FLASHO_CSNI/GPIO3_B7_u FLASHO_CSNI/GPIO3_C0_u FLASHO_CSNI/GPIO3_C1_u FLASHO_DQS/EMMC_RSTNOUT/GPIO3_C1_u FLASHO_DQS/EMMC_LCLKOUT/GPIO3_C2_d FLASHO_DQS/EMMC_CLKOUT/GPIO3_C3_d FLASHO_VOLTAGE_SEL/GPIO3_C3_d	AH28 AH37,28 AH37,28 Y6 28 Y6 28 AF6,8 AF6
FLASH0_VDD	V9 OVCCIO_FLASH

AE3_{7.28.20}

U1Q MCU_RK3288 HOST_D0/MAC_TXD2/SDIO1_D0/FLASH1_D0/GPIO3_D0_u HOST_D1/MAC_TXD3/SDIO1_D1/FLASH1_D1/GPIO3_D1_u HOST_D2/MAC_RXD2/SDIO1_D2/FLASH1_D2/GPIO3_D2_u HOST_D3/MAC_RXD3/SDIO1_D3/FLASH1_D3/GPIO3_D3_u HOST_D4/MAC_TXD0/SDIO1_DET/FLASH1_D4/GPIO3_D4_u HOST_D5/MAC_TXD1/SDIO1_WRPRT/FLASH1_D5/GPIO3_D5_u	AB1 T14TEST T15TEST AD1 T16TEST AB2 AA3
HOST_D6/MAC_RXD0/SDI01_BKPWR/FLASH1_D6/GPI03_D6_u HOST_D7/MAC_RXD1/SDI01_INTn/FLASH1_D7/GPI03_D7_u HOST_CKOUTP/MAC_MDC/FLASH1_RDY/GPI04_A0_u HOST_CKOUTN/MAC_RXDV/FLASH0_CSn4/FLASH1_WP/GPI04_A1_u HOST_D8/MAC_RXEN/FLASH0_CSn5/FLASH1_RDN/GPI04_A2_u HOST_D9/MAC_CLK/FLASH0_CSn5/FLASH1_LE/GPI04_A3_u HOST_D10/MAC_TXEN/FLASH0_CSn7/FLASH1_CLE/GPI04_A4_u HOST_D11/MAC_MDI0/FLASH1_WRN/GPI04_A5_u HOST_D12/MAC_RXCLK/SDI01_CMD/FLASH1_CSn0/GPI04_A6_u HOST_D13/MAC_CRS/SDI01_CLKOUT/FLASH1_CSn0/GPI04_A6_u HOST_D14/MAC_CCL/FLASH1_DQS/FLASH1_CSn3/GPI04_B0_u	AC3 AC2 × AE1 × AE1 × AE2 × AD2 × Y5 × AB5 × AA5 ×
HOST_D15/MAC_TXCLK/SDIO1_PWREN/FLASH1_CSn2/GPIO4_B1_u	V8OVCCIO_FLASH

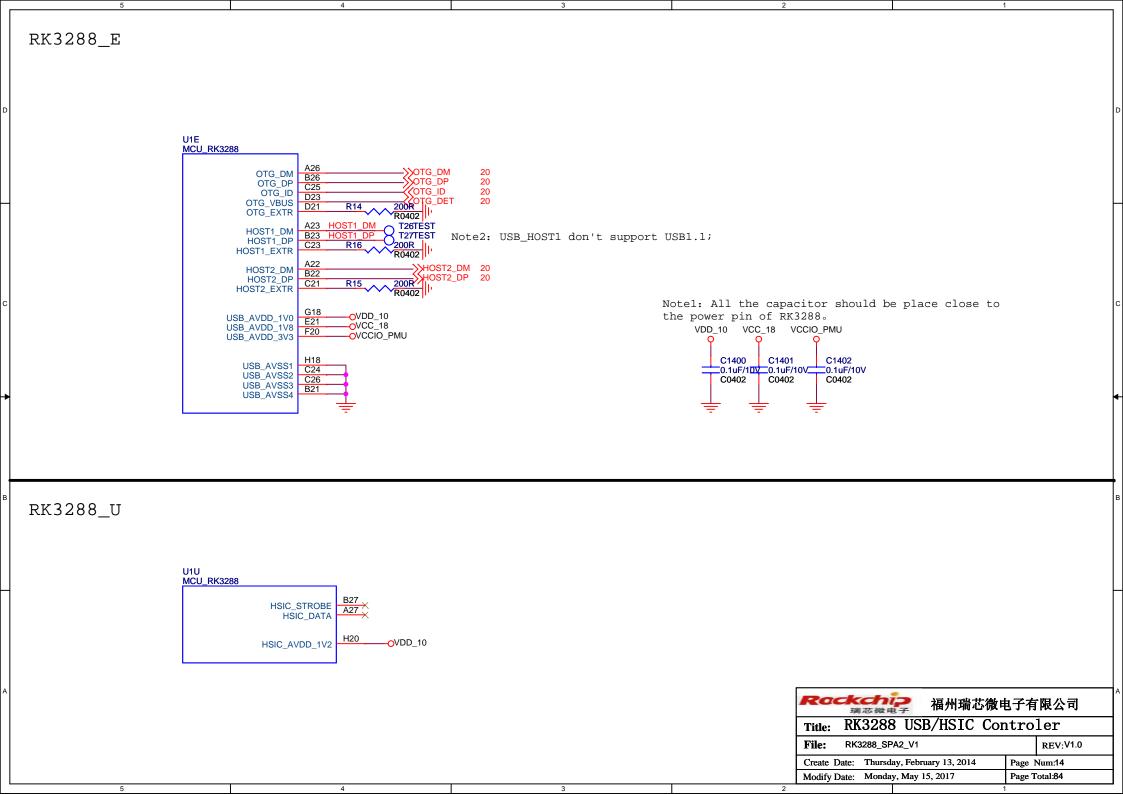
	VCCIO_FLASH=1.8V	VCCIO_FLASH=3.3V	
FLASHO_VOLTAGE_SEL	VCCIO_FLASH	Floating(Default)	

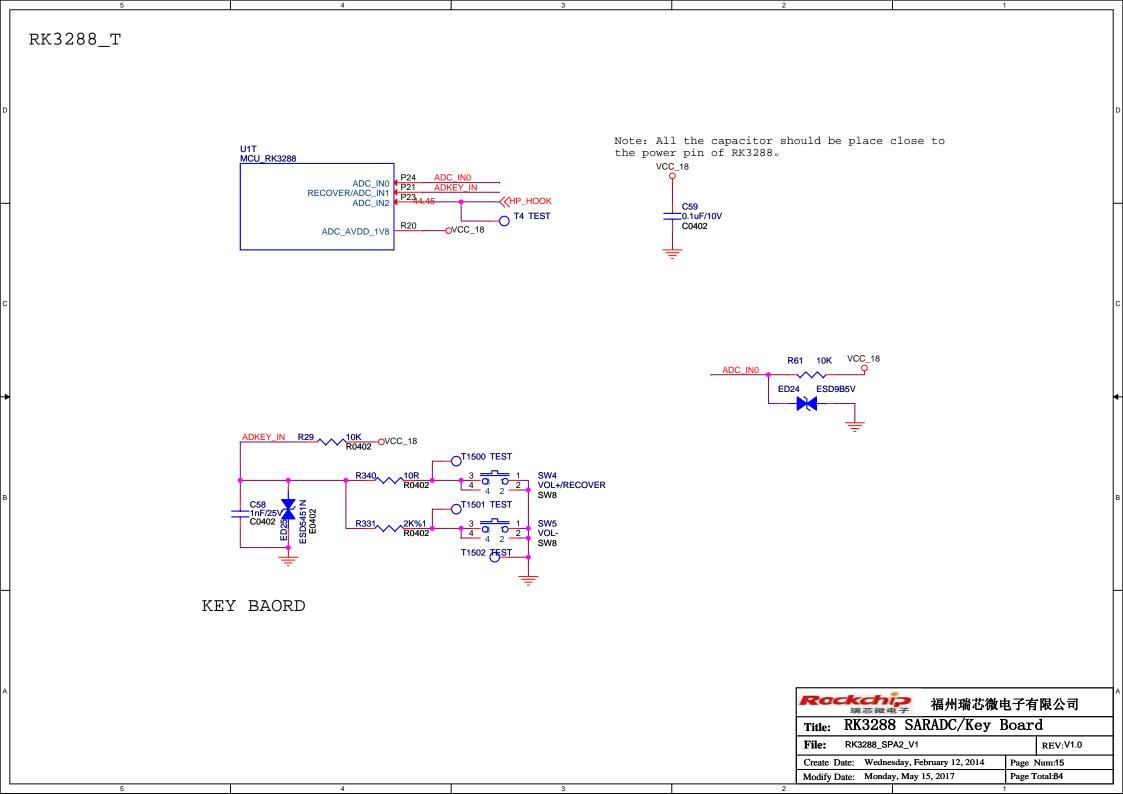


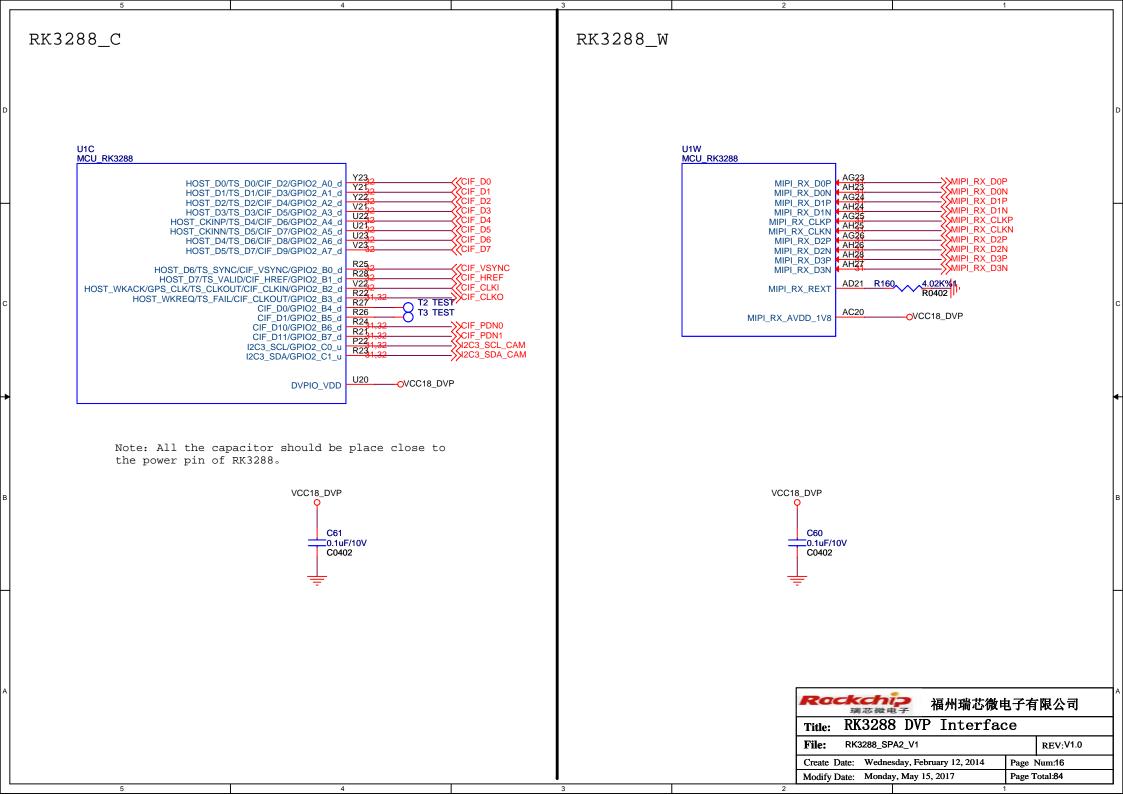
Note: All the capacitor should be place close to the power pin of RK3288.

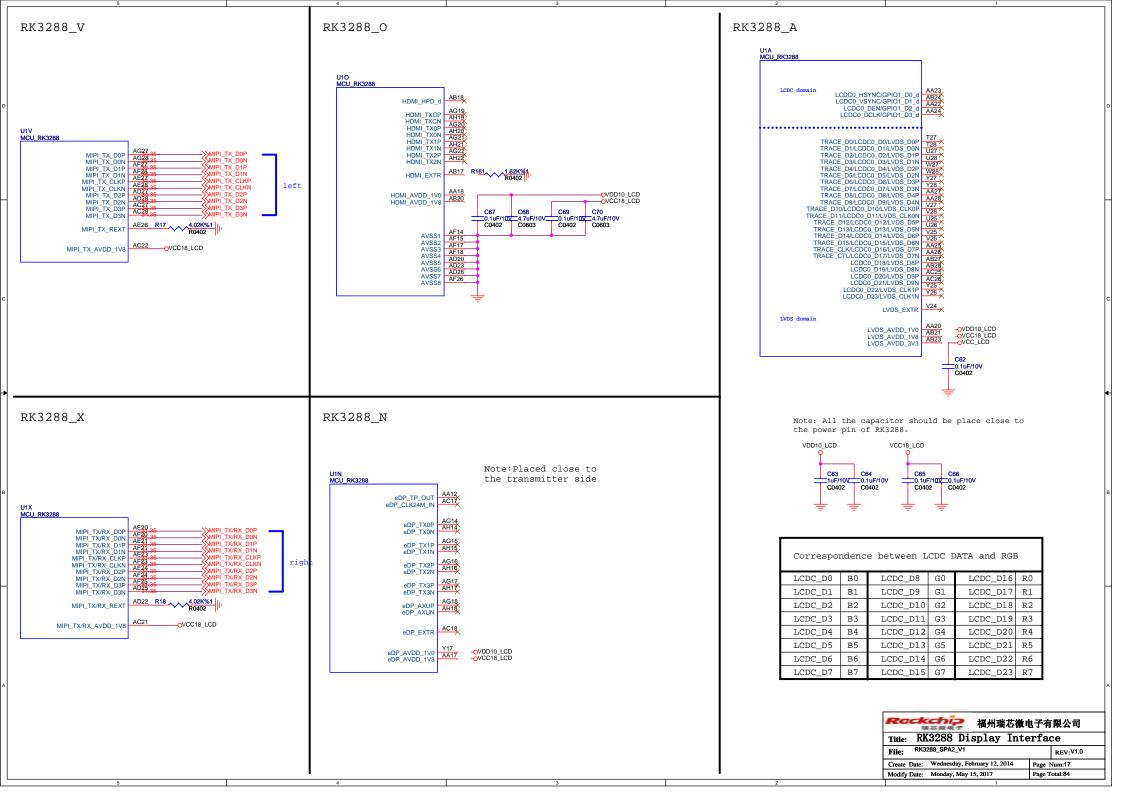
福州瑞芯徽电子有限公司					
Title: RK3288 Flash Control					
File:	RK3288_SPA	2_V1			REV:V1.0
Create I	Date: Tuesday,	November 29, 201	1	Page 1	Num:13
Modify Date: Monday, May 15, 2017		Page T	otal:84		

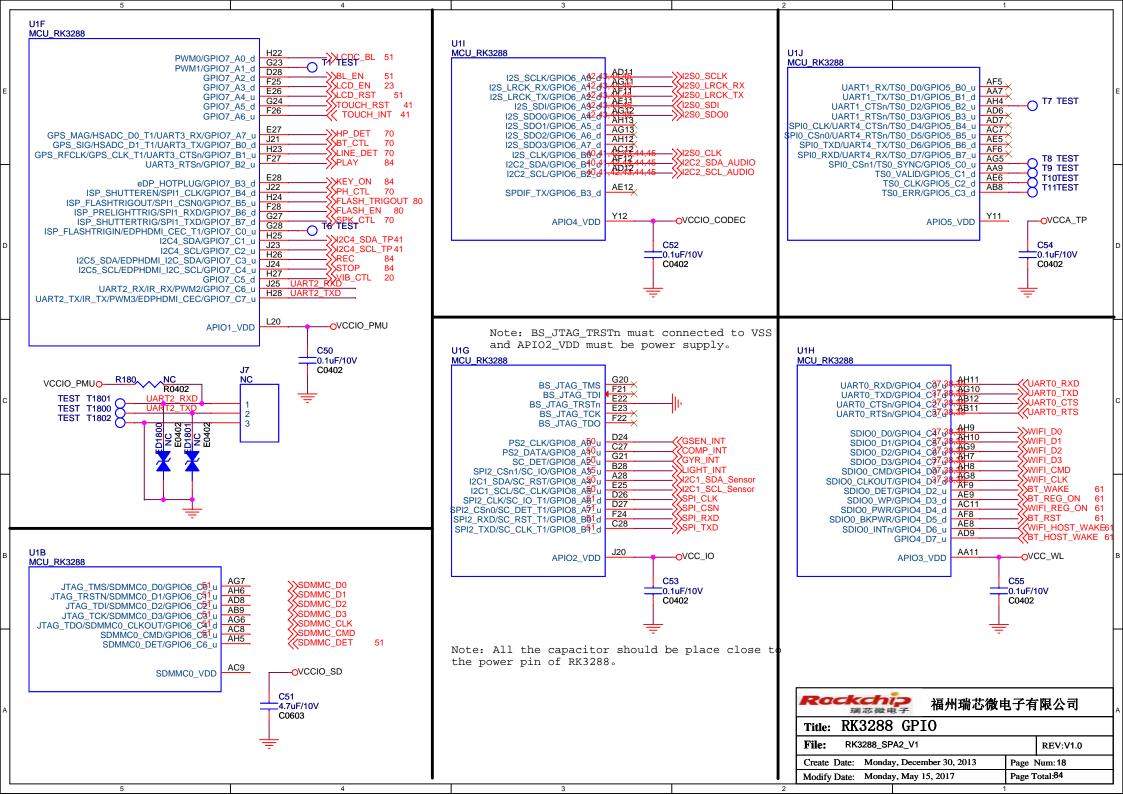
U1P MCU_RK3288

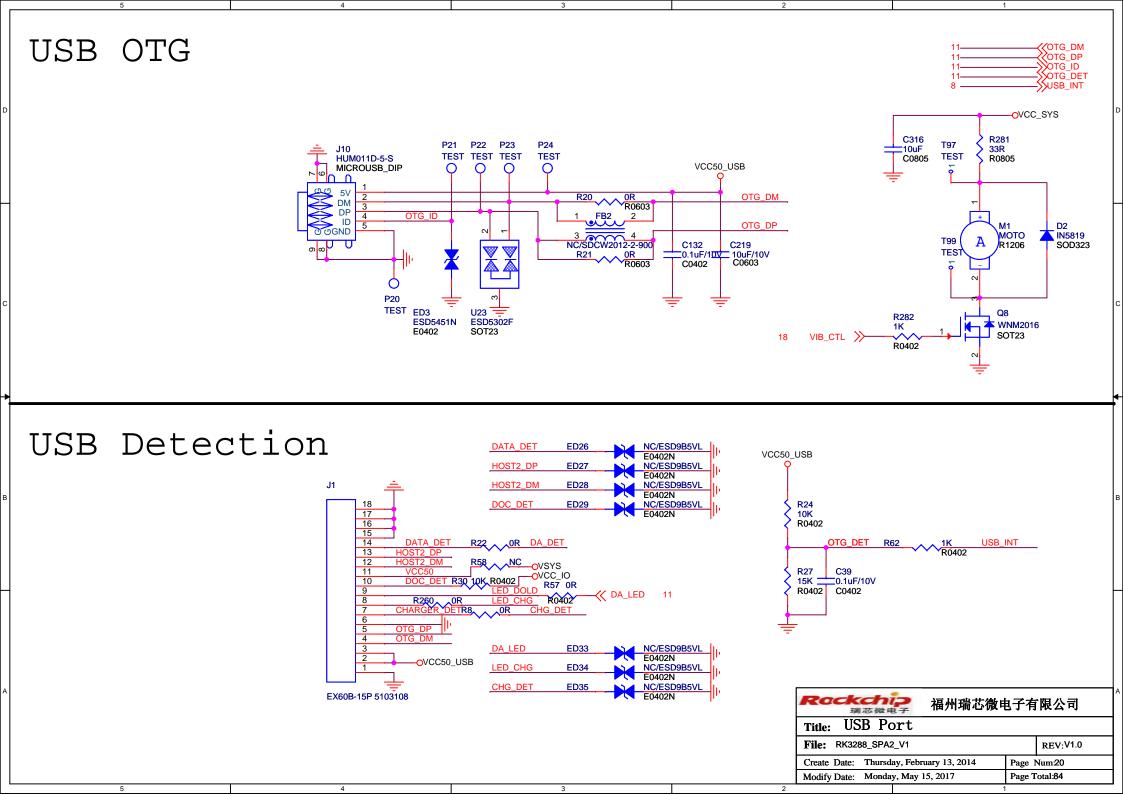


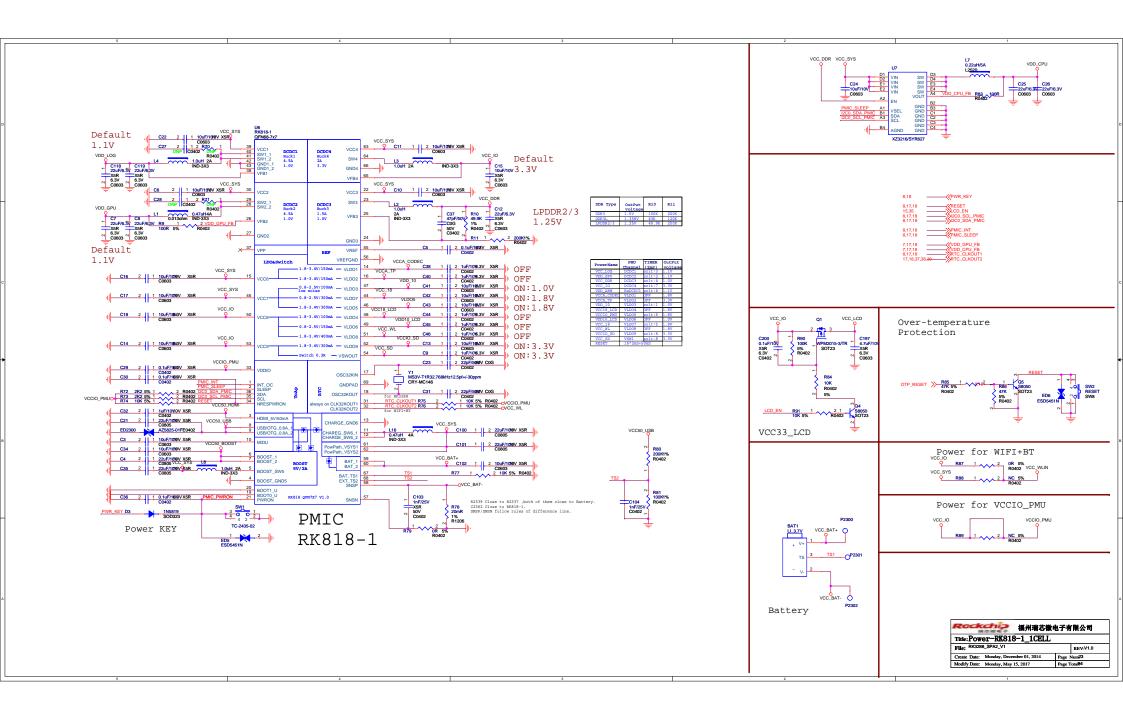


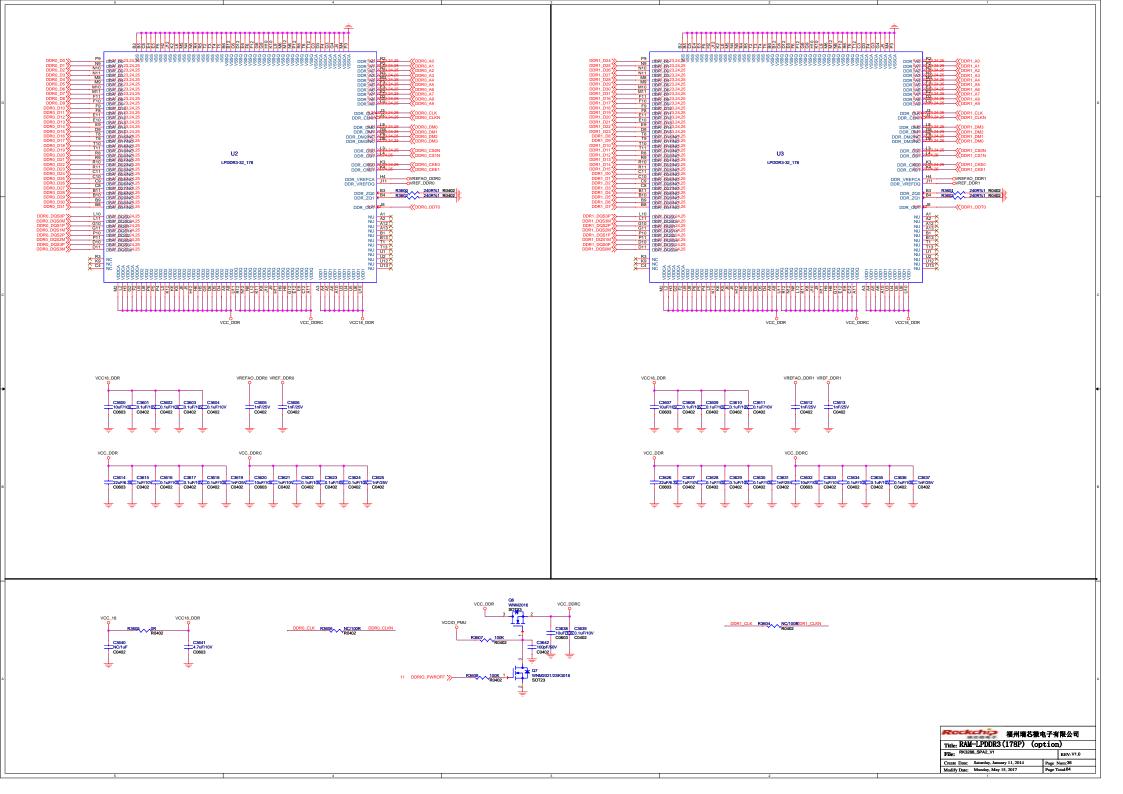






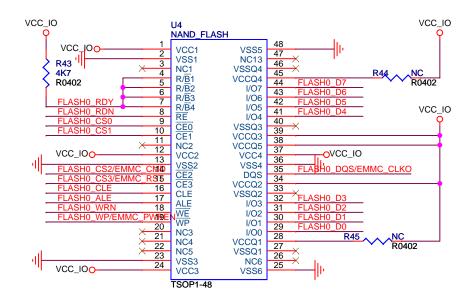


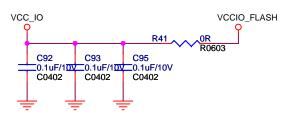




NAND FLASH

note: if use toshiba and sandisk Flash at DDR mode, VCCQ1 and VCCQ4 must be connected to VCC_IO $_{\circ}$





Note:
Reserve PAD for Update.

FLASHO_CLE T42 TEST



FLASH0_D0

FLASH0_D1 FLASH0_D2

₹FLASH0_D3

⟨FLASH0_D4

FLASH0 D5

FLASH0_D6 FLASH0_D7 FLASH0_RDY

FLASHO_RDN
FLASHO_ALE
FLASHO_CLE
FLASHO_WRN
FLASHO_CS0
FLASHO_CS1

FLASH0_WP/EMMC_PWREN

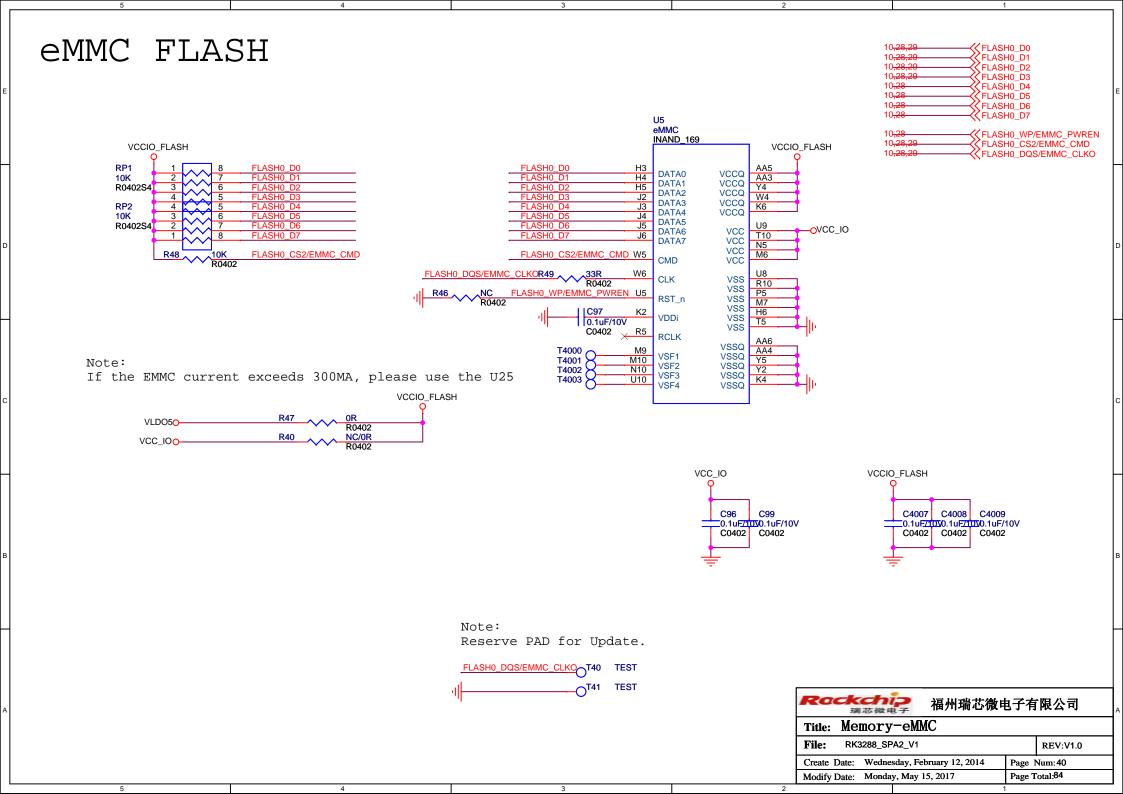
FLASH0_CS2/EMMC_CMD FLASH0_CS3/EMMC_RST

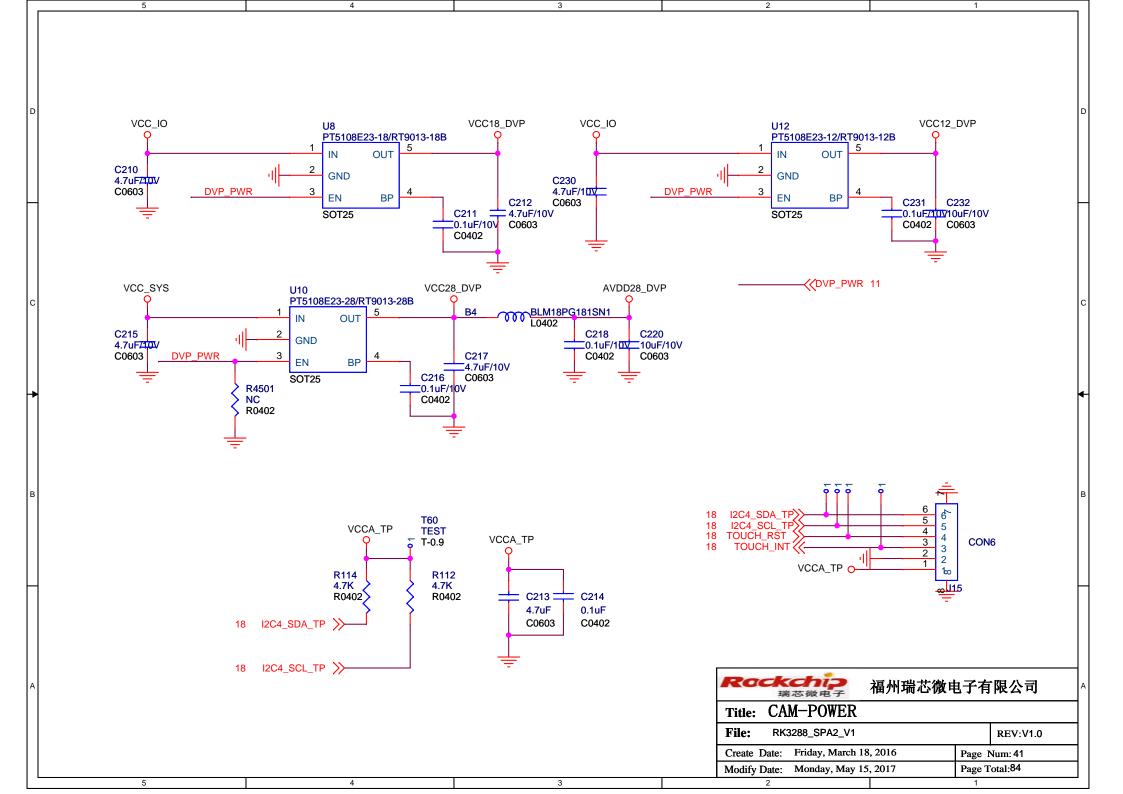
FLASH0_DQS/EMMC_CLKO

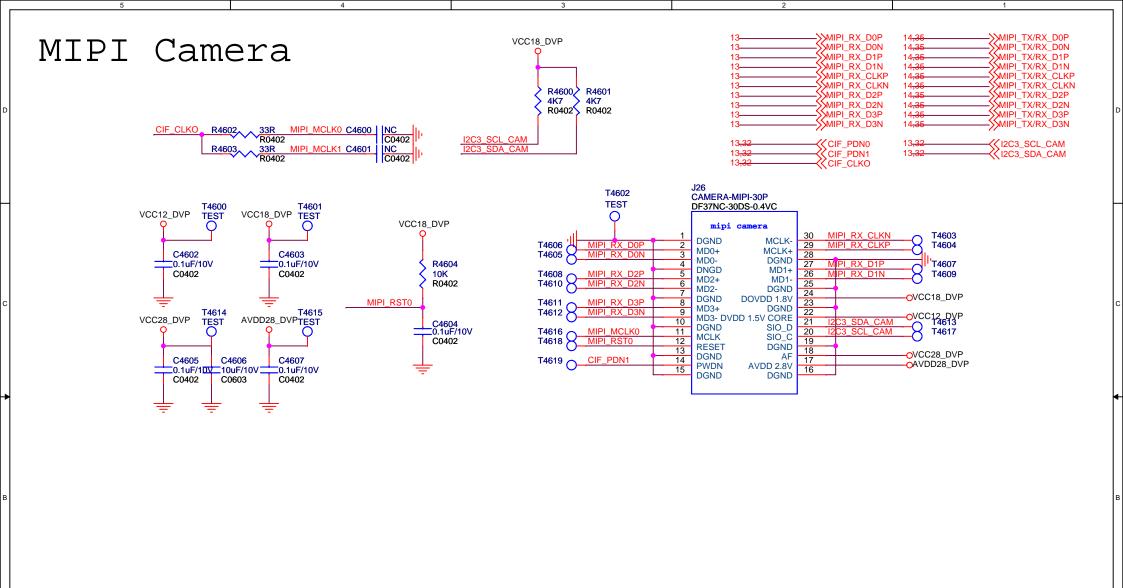
10,27,29

10,27,29

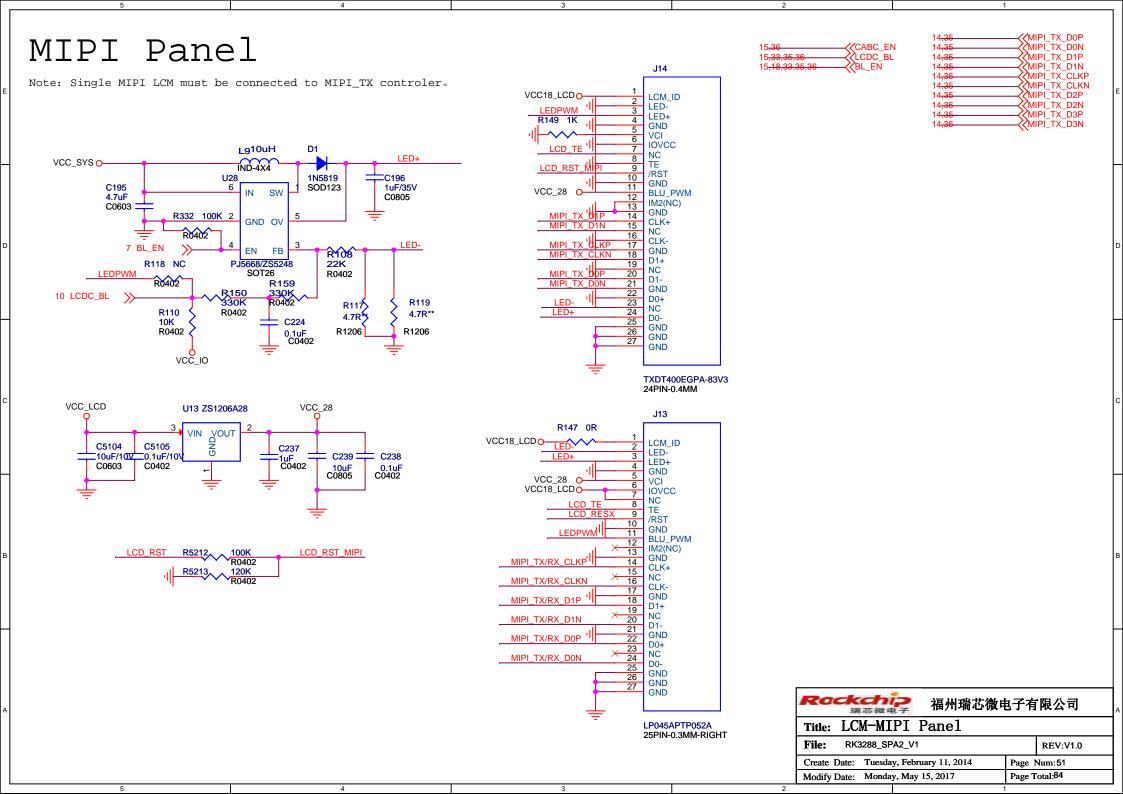
10,27,29



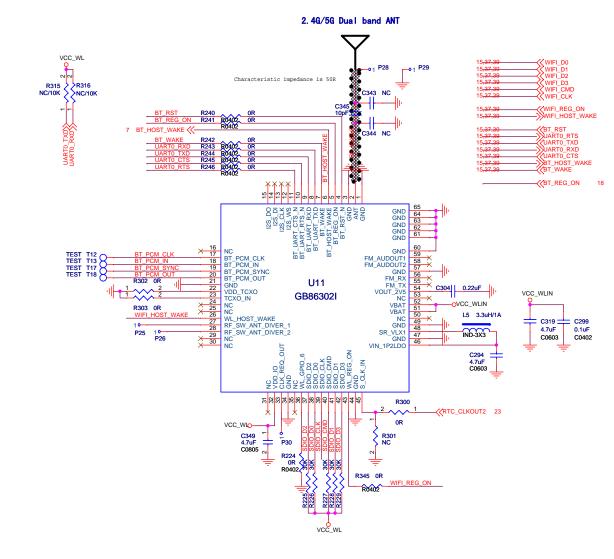


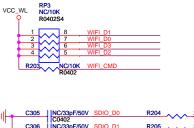






WIFI/WIFI ac/BT MODULE





all .	C305	NC/33pF/50V	SDIO_D0	R204	33R R0402	WIFI_D0
ال.		C0402			•	
٠.	C306	NC/33pF/50V	SDIO_D1	R205	33R R0402	WIFI_D1
		C0402			•	
	C307	NC/33pF/50V	SDIO_D2	R206	33R R0402	WIFI_D2
		C0402		~ ~ ·		
	C308	NC/33pF/50V	SDIO_D3	R207	33R R0402	WIFI_D3
	ľ i	C0402		~ ~ ·		
	C309	NC/33pF/50V	SDIO_CMD	R201	33R R0402	WIFI_CMD
		C0402				
	C310	NC/33pF/50V	SDIO_CLK	R202	33R R0402	WIFI_CLK
		C0402			_	

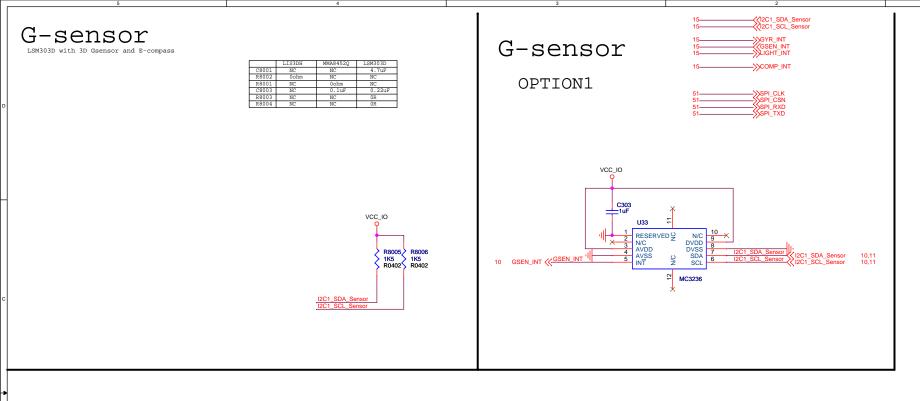
 福州瑞花微电子有限公司

 Title: WIFI ac/BT-AP6335 (option)

 File:
 REV:V1.0

 Create Date:
 Tuesday, April 22, 2014
 Page Num.61

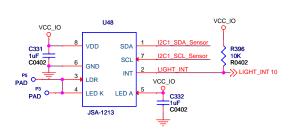
 Modify Date:
 Monday, May 15, 2017
 Page Total.94

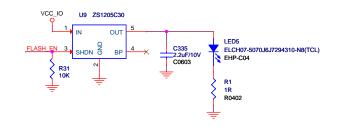


LIGHT-Sensor

OPTION1

note: Drive up to total 1.5A or 0.75A per channel.

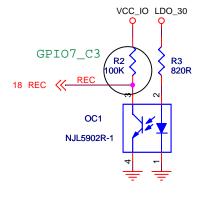




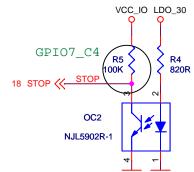
福州瑞芯徽电子有限公司				
Title: Sensor/VIB				
File: RK3288_SPA2_V1		REV:V1.0		
Create Date: Wednesday, February 12, 2014	Page 1	Num:80		
Modify Date: Monday, May 15, 2017	Page T	otal:84		

EFUSE Power

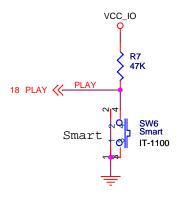
Note:Place the Component if need to write eFUSE

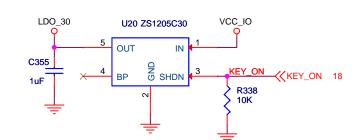


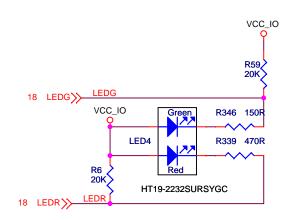
ΙΟ□	GPI07_C3	GPI07_C4	
REC	高н	高н	
STOP	低工	高田	
PLAY	低L	低L	
REW	高H 低L		



注:电阻R2、R5要调整为100K,否则REW键功能会有异常。







Rockchip 福州瑞芯徹电子有限公司					
Title: eFUSE (option)					
File: RK3288_SPA2_V1 REV:V1.0					
Create Date: Wednesday, February 26, 2014 Page Num84					
Modify Date: Monday, May 15, 2017 Page Total:84					