BCM43241

Single-Chip IEEE 802.11 a/b/g/n 2x2 MAC/Baseband/Radio with Integrated Bluetooth 4.0 + HS and FM Receiver

GENERAL DESCRIPTION

The Broadcom® BCM43241 single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 a/b/g and 2×2 IEEE 802.11n MAC/baseband/radio, Bluetooth 4.0 + HS, and FM radio receiver.

The BCM43241 takes advantage of the high throughput and extended range of the Broadcom second-generation MIMO solution. With MIMO, the information is sent and received over two or more antennas, simultaneously using the same frequency band, thus providing greater range and higher throughput, while maintaining compatibility with legacy IEEE 802.11a/b/g devices. This is accomplished through a combination of enhanced MAC and PHY implementations including spatial multiplexing modes in the transmitter and receiver, and advanced digital signal processing techniques to improve receive sensitivity. The BCM43241 architecture with its fully integrated dual-band radio transceiver supports 2 × 2 antennas. It also supports 20 and 40 MHz channels allowing for PHY Layer throughput up to 300 Mbps.

Using advanced design techniques and process technology to reduce active and idle power, the BCM43241 is designed to address the needs of highly mobile devices that require minimal power consumption and compact size.

GENERAL DESCRIPTION

It includes a power management unit that simplifies the system power topology and allows for operation directly from a mobile platform battery while maximizing battery life. The BCM43241 also includes power saving schemes such as single-core listen (OCL), single-core demodulation of SISO/STBC packets, and Dynamic ML.

The BCM43241 implements the highly sophisticated Enhanced Collaborative Coexistence radio coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative Bluetooth coexistence scheme along with coexistence support for external radios (such as GPS, WiMAX, or Ultra Wideband radio technologies, as well as cellular radios) and a single shared 2.4 GHz antenna for Bluetooth and WLAN. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

For the WLAN section, two alternative host interface options are included: an SDIO v3.0 interface, which can operate in 4 bit, 1 bit, or gSPI modes, and a High-Speed Inter-Chip (HSIC) interface (a USB 2.0 derivative for short-distance on-board connections). An independent, high-speed UART is provided for the Bluetooth host interface.

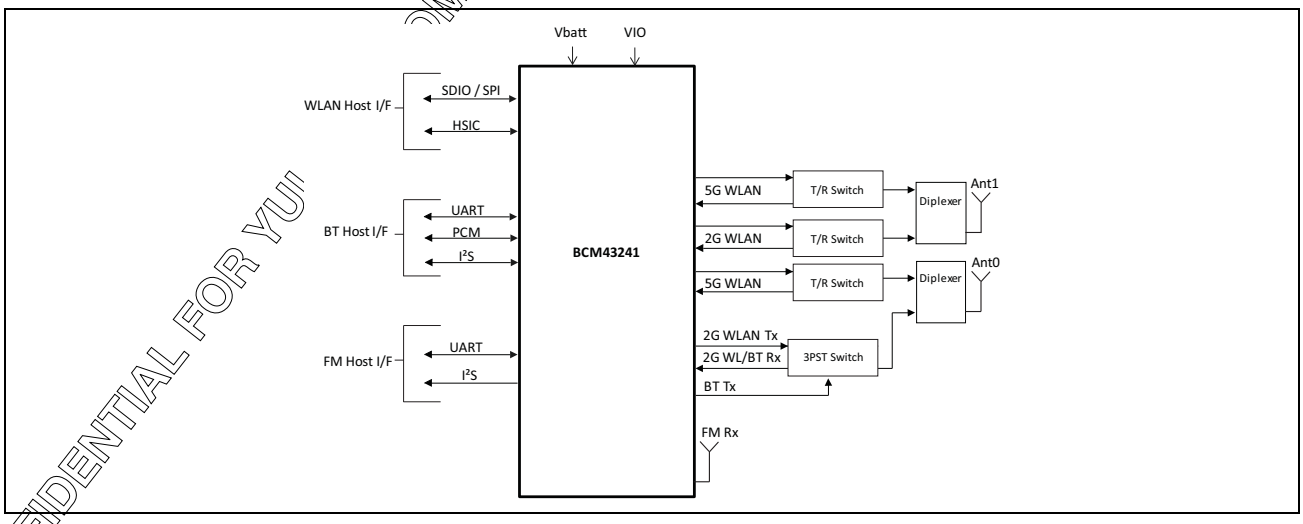

Figure 1: Functional Block Diagram

FEATURES

IEEE 802.11x Key Features

- Single-band 2.4 GHz IEEE 802.11 b/g/n or dual-band 2.4 GHz and 5 GHz IEEE 802.11 a/b/g/n
- Hardware support for virtual simultaneous dual band operation with sub 1 ms band switching time
- Dual-stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 300 Mbps for typical upper-layer throughput in excess of 200 Mbps
- Supports the IEEE 802.11n STBC (space-time block coding) in both TX and RX for improved range and power efficiency
- Contains integrated 2.4 GHz and 5 GHz Power Amplifiers as well as 11 RF control signals available to control external RF switches or LNAs
- Supports a single 2.4 GHz antenna shared between WLAN and Bluetooth
- Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN
- Internal fractional nPLL allows support for a wide range of reference clock frequencies
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other colocated wireless technologies such as GPS, WiMAX, or UWB
- Supports standard SDIO v3.0 (208 MHz, 4-bit and 1-bit), and gSPI (48 MHz) host interfaces
- Alternative host interface supports HSIC v1.0 (short-distance USB device)
- Integrated ARM® Cortex-M3™ processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. (This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 576 KB SRAM and 640 KB ROM.)
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices

FEATURES

Bluetooth and FM Key Features

- Complies with Bluetooth Core Specification Version 4.0 + HS with provisions for supporting future specifications
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports extended Synchronous Connections (eSCO) for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Interface support — Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data
- FM unit supports HCI for communication
- Low power consumption improves battery life of handheld devices
- FM receiver: 65 MHz to 108 MHz FM bands; supports the European Radio Data Systems (RDS) and the North American Radio Broadcast Data System (RBDS) standards
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound
- Automatic frequency detection for standard crystal and TCXO values

General Features

- Supports battery voltage range from 2.3V to 4.8V supplies with internal switching regulator
- Programmable dynamic power management
- 3072-bit OTP for storing board parameters
- 16 general-purpose I/Os (GPIOs)
- Package options:
  - FCFBGA (7.0 mm × 9.0 mm, 0.4 mm pitch)
  - WLCSP (5.88 mm × 4.40 mm, 0.2 mm pitch)

Security

- WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
- AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
- Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
- Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design

Revision History

Revision	*Date*	*Change Description*
MCS43241-DS204-R	5/19/12	**Updated:** • Bluetooth and FM Key Features on Cover • SDIO v3.0 maximum clock rate • Figure 3: “Mobile Phone Block System Diagram,” on page 21 • Figure 4: “Typical Power Topology,” on page 23 • “Power Supply Topology” on page 22 • Table 2: “Crystal Oscillator and External Clock – Requirements and Performance,” on page 29 • “Features” on page 32 • Table 4: “Power Control Pin Description,” on page 38 • “BBC Power Management” on page 39 • “RDS/RBDS” on page 64 • Figure 32: “WLAN Bootup Sequence,” on page 76 • Figure 39: “293-Bump WLCSP Bump Map (Bottom View),” on page 89 • Table 29: “Bluetooth Receiver RF Specifications,” on page 122 • Table 33: “FM Receiver Specifications,” on page 127 • Table 35: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 136 • Table 36: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 140 • Table 37: “WLAN 5 GHz Receiver Performance Specifications,” on page 141 • Table 38: “WLAN 5 GHz Transmitter Performance Specifications,” on page 145 • Table 40: “Core Buck Switching Regulator (CBUCK) Specifications,” on page 147 • Table 42: “CLDO Specifications,” on page 150 • Table 43: “LNLDO2 Specifications,” on page 151 • Table 44: “LNLDO1 Specifications,” on page 152 • Table 45: “BCM43241 WLAN Current Consumption 2.4 GHz,” on page 153 • Table 46: “BCM43241 WLAN Current Consumption 5 GHz,” on page 154 • Table 47: “BT Current Consumption,” on page 156

Revision	Date	Change Description
		• Table 48: "BLE Current Consumption," on page 157 • Table 49: "FM Current Consumption," on page 157 • Figure 52: "WLAN = ON, Bluetooth = ON," on page 172 • Figure 53: "WLAN = OFF, Bluetooth = OFF," on page 172 • Figure 54: "WLAN = ON, Bluetooth = OFF," on page 173 • Figure 55: "WLAN = OFF, Bluetooth = ON," on page 173 • "Preliminary Package Thermal Characteristics" on page 174 • Figure 58: "WLCSP Keep-Out Areas for PCB Layout — Bumps Facing Up," on page 177 **Removed:** • Specific ROM and RAM values for Bluetooth operation
MCS43241-DS203-R	01/26/12	**Updated:** • "UART Interface" on page 64 • Table 18: "FCFBGA and WLCSP Signal Descriptions," on page 97 • Table 28: "Recommended Operating Conditions and DC Characteristics," on page 116 • Table 35: "WLAN 2.4 GHz Receiver Performance Specifications," on page 131 • Table 36: "WLAN 2.4 GHz Transmitter Performance Specifications," on page 135 • Table 37: "WLAN 5 GHz Receiver Performance Specifications," on page 136 • Table 38: "WLAN 5 GHz Transmitter Performance Specifications," on page 140
MCS43241-DS202-R	12/9/11	**Updated:** • Table 18, "PACKAGEOPTION_2" signal description on page 115.
MCS43241-DS201-R	11/17/11	**Updated:** • "Ordering Information" on page 188.
MCS43241-DS200-R	10/14/11	Initial release

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About This Document

Purpose and Audience

This data sheet provides details about the functional, operational, and electrical characteristics of the Broadcom BCM43241. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Overview

Overview

The Broadcom BCM43241 single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 a/b/g/n (MAC/baseband/radio), Bluetooth 4.0 + EDR (enhanced data rate), and FM receiver. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the BCM43241 and their associated external interfaces, which are described in greater detail in the following sections.

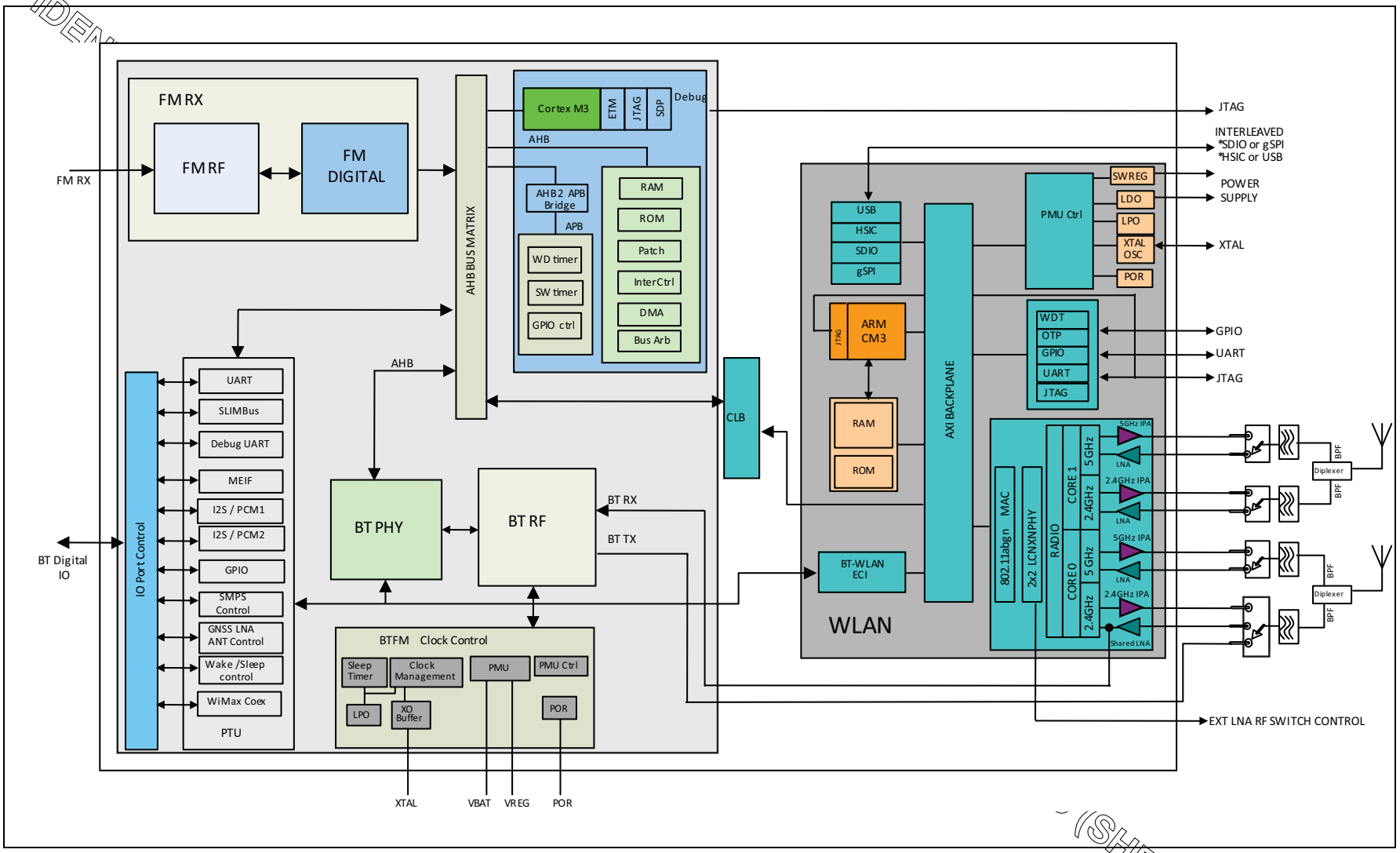


Figure 2: BCM43241 Block Diagram

Features

The BCM43241 supports the following features:

- IEEE 802.11a/b/g/n dual-band radio — virtual simultaneous dual-band operation
- Bluetooth v4.0 + EDR with integrated Class 1 PA
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single- and dual-antenna support
  - Single antenna with shared LNA
  - Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - SDIO v3.0 (1-bit/4-bit) — up to 208 MHz clock rate
  - gSPI — up to 48 MHz clock rate
  - HSIC (USB device interface for short distance on-board applications)
- BT host digital interface (can be used concurrently with above interfaces):
  - UART (up to 4 Mbps)
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- I^2S/PCM for FM/BT audio, HCI for FM block control
- HCI high-speed UART (H4, H4+, H5) transport support
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface)
- Bluetooth SmartAudio technology improves voice and music quality to headsets
- Bluetooth low-power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth wideband speech (WBS)
- FM advanced internal antenna support
- FM auto search/tuning functions
- FM multiple audio routing options: I^2S, PCM, eSCO, A2DP
- FM mono-stereo blend and switch, and soft mute support
- FM audio pause detect support
- Audio rate-matching algorithms
- Multiple simultaneous A2DP audio stream
- FM over Bluetooth operation and on-chip stereo headset emulation (SBC, MP3, and AAC+)
- MP3, AAC+ on-chip decoder for low power music playback

Standards Compliance

The BCM43241 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0 + HS
- Bluetooth 4.0 (Bluetooth Low Energy)
- 65 MHz to 108 MHz FM bands (US, Europe, and Japan)
- IEEE 802.11n — Handheld Device Class (Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The BCM43241 supports the following future drafts/standards:

- IEEE 802.11r — Fast Roaming (between APs)
- IEEE 802.11k — Resource Management
- IEEE 802.11w — Secure Management Frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11r Fast Roaming Support
  - IEEE 802.11k Radio Resource Measurement
- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (Hardware Accelerator)
  - TKIP (HW Accelerator)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4

  - CCXv5
  - WFAEC
- IEEE 802.15.2 Coexistence Compliance — on silicon solution compliant with IEEE 3 wire requirements

Mobile Device Usage Model

The BCM43241 incorporates a number of unique features to simplify integration into mobile phone platforms. Its flexible PCM and UART interfaces enable it to transparently connect with the existing circuits. In addition, the TCXO and LPO inputs allow the use of existing handset features to further minimize the size, power, and cost of the complete system.

- The PCM interface provides multiple modes of operation to support both master and slave as well as hybrid, interfacing to single or multiple external codec devices.
- The UART interface supports hardware flow control with tight integration to power control sideband signaling to support the lowest power operation.
- The TCXO interface accommodates any of the typical reference frequencies used by cell phones.
- FM digital interfaces can use either I^2S or PCM.
- The highly linear design of the radio transceiver ensures that the device has the lowest spurious emissions output regardless of the state of operation. It has been fully characterized in the global cellular bands.
- The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and intermodulation performance (distortion of the transmitted signal caused by the mixing of the cellular and Bluetooth transmissions) in the presence of any cellular transmission (GSM®, GPRS, CDMA, WCDMA, or iDEN). Minimal external filtering is required for integration inside the handset.

The BCM43241 is designed to provide direct interface with new and existing handset designs as shown in Figure 3.

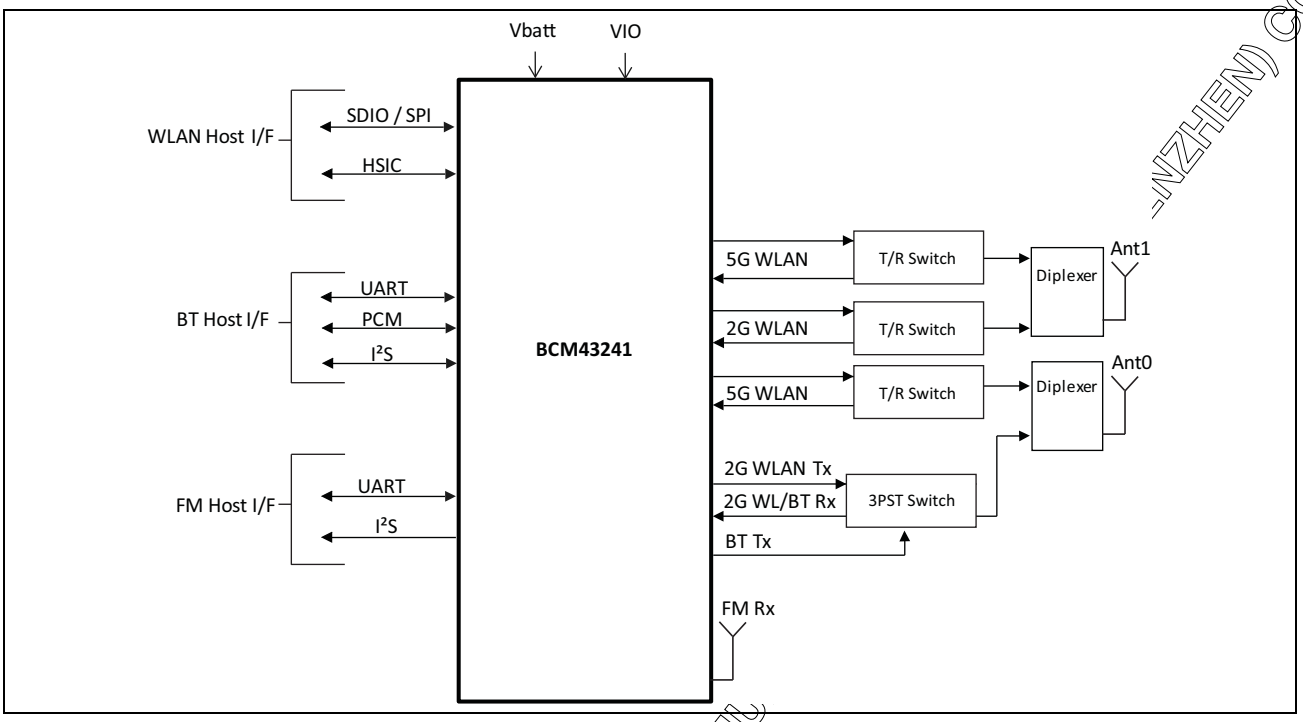


Figure 3: Mobile Phone Block System Diagram

Section 2: Power Supplies and Power Management

Power Supply Topology

One Buck regulator, multiple LDO regulators, and a Power Management Unit (PMU) are integrated into the BCM43241. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth, WLAN, and FM functions in embedded designs.

A single VBAT (2.3V to 4.8V) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the BCM43241.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK, CLDO, and LNLDOs power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDOs may be turned off/on based on the dynamic demands of the digital baseband.

The BCM43241 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNDLO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VIO supply) provide the BCM43241 with all the voltages it requires, further reducing leakage currents.

BCM43241 PMU Features

- VBAT to 1.35Vout (600 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (125 mA maximum) LDO3P3
- 1.35V to 1.2Vout (150 mA and 325 mA maximum) LNLDOs
- 1.35V to 1.2out (300 mA maximum) CLDO
- Additional internal LDOs (not externally accessible)

Figure 4 shows the regulators and a typical power topology.

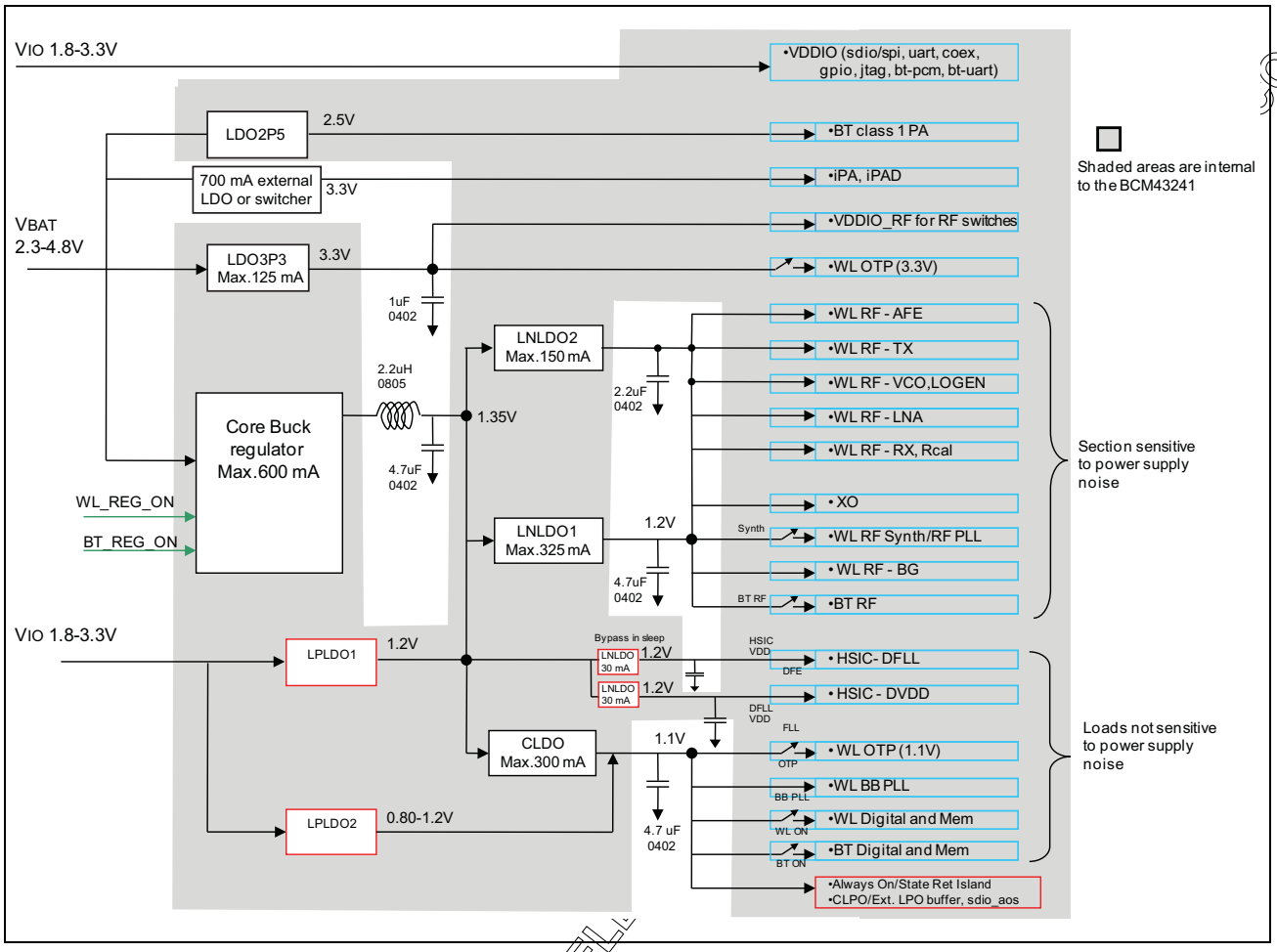


Figure 4: Typical Power Topology

WLAN Power Management

The BCM43241 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43241 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the BCM43241 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43241 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM43241 WLAN power states are described as follows:

- Active mode — All WLAN blocks in the BCM43241 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode — The radio, analog domains, and most of the linear regulators are powered down. The rest of the BCM43241 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode — Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the HSIC or SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
- Power-down mode — The BCM43241 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic, reenabling the internal regulators.

PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Power-off Shutdown

The BCM43241 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the BCM43241 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the BCM43241 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the BCM43241, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the BCM43241 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

Two signals on the BCM43241, the frequency reference input (WRF_XTAL_CAB_OP) and the LPO_IN input, are designed to be high-impedance inputs that do not load down the driving signal even if the chip does not have VDDIO power applied to it.

When the BCM43241 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

Power-Up/Power-Down/Reset Circuits

The BCM43241 has two signals (see Table 1) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 22: "Power-Up Sequence and Timing," on page 171.

Table 1: Power-Up/Power-Down/Reset Control Signals

Signal	*Description*
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM43241 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal BCM43241 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Section 3: Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Note: The crystal and TCXO implementations have different power supplies (WRF_XTAL_VDD1P2 for crystal, WRF_TCXO_VDD for TCXO).

Crystal Interface and Clock Generation

The BCM43241 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 5. Consult the reference schematics for the latest configuration.

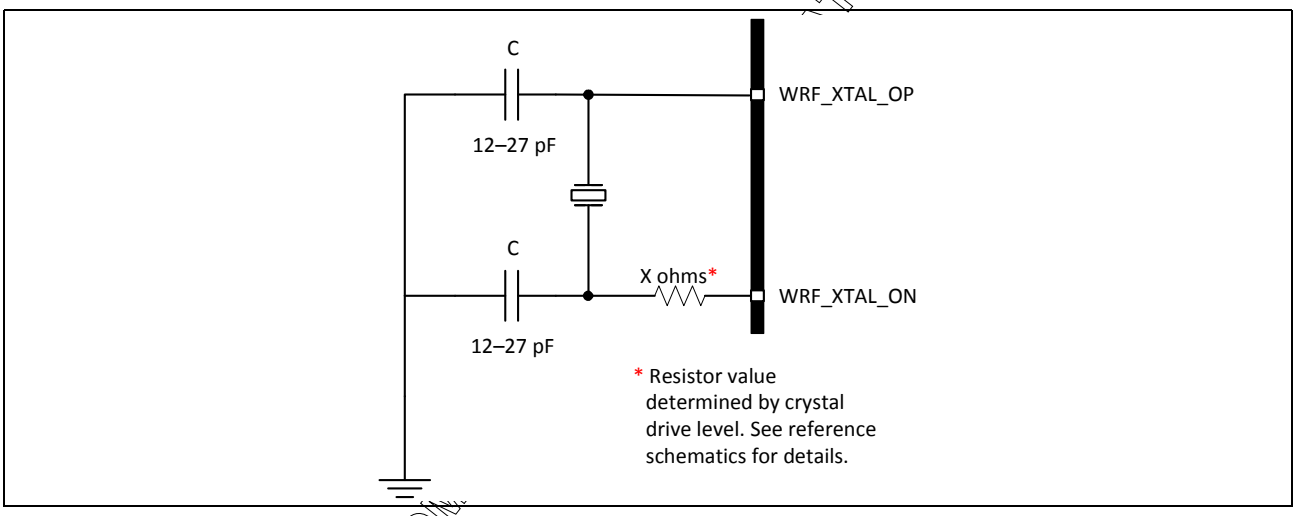


Figure 5: Recommended Oscillator Configuration

A fractional-N synthesizer in the BCM43241 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The default frequency reference is a 37.4 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in Table 2 on page 29.

Note: The fractional-N synthesizer can support alternative reference frequencies. Frequencies other than the default, however, require support to be added in the driver plus additional extensive system testing. Contact Broadcom for further details.

TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the Phase Noise requirements listed in Table 2. When the clock is provided by an external TCXO, there are two possible connection methods, shown in Figure 6 and Figure 7:

1. If the TCXO is dedicated to driving the BCM43241, it should be connected to the WRF_XTAL_OP pin through an external 1000 pF coupling capacitor, as shown in Figure 6. The internal clock buffer connected to this pin will be turned OFF when the BCM43241 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P2 pin.
2. For 2.4 GHz operation only, an alternative is to DC-couple the TCXO to the WRF_TCXO_CK pin, as shown in Figure 7. Use this method when the same TCXO is shared with other devices and a change in the input impedance is not acceptable because it may cause a frequency shift that cannot be tolerated by the other device sharing the TCXO. This pin is connected to a clock buffer powered from WRF_TCXO_VDD. If the power supply to this buffer is always on (even in sleep mode), the clock buffer is always on, thereby ensuring a constant input impedance in all states of the device. The maximum current drawn from WRF_TCXO_VDD is approximately 500 µA.

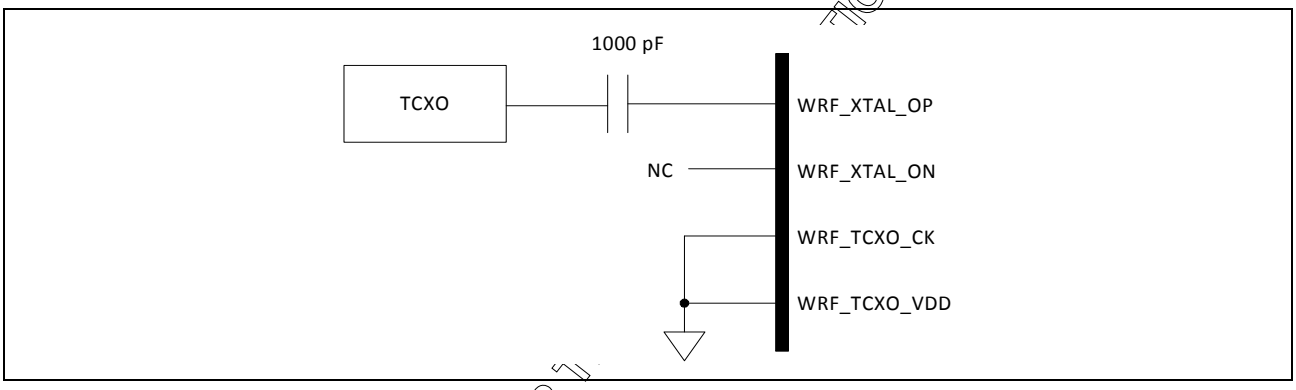


Figure 6: Recommended Circuit to Use with an External Dedicated TCXO

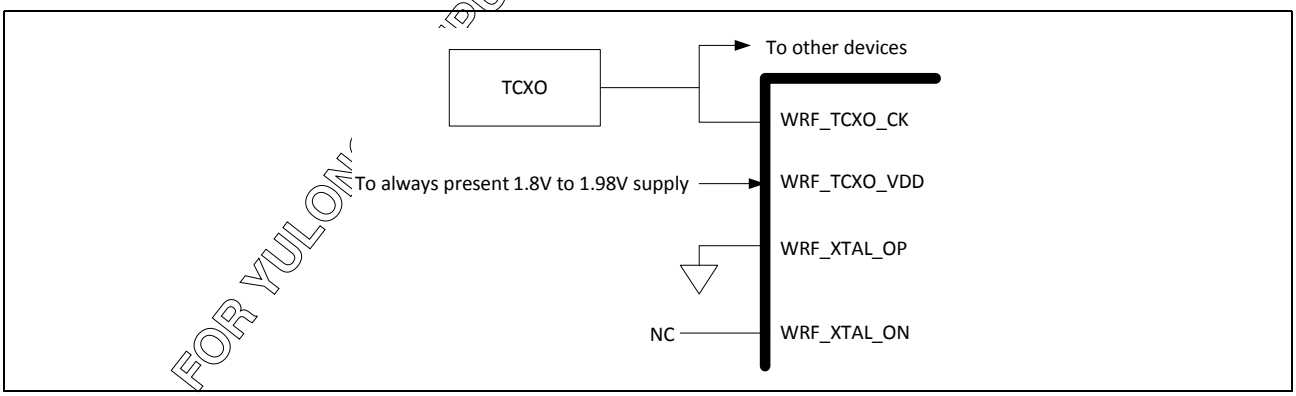


Figure 7: Recommended Circuit to Use with an External Shared TCXO

Table 2: Crystal Oscillator and External Clock – Requirements and Performance

		Crystal[a]			External Frequency Reference[b c]			
Parameter	**Conditions/Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Frequency	–	Between 12 MHz and 52 MHz[d]						
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–		Ω
Drive level	External crystal specification requirement	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_OP)	Resistive	–	–	–	12k	17k	–	Ω
	Capacitive	–	–	–	–	–	6	pF
Input impedance (WRF_TCXO_IN)	Resistive	–	–	–	17k	31k	–	Ω
	Capacitive	–	–	–	–	–	2	pF
WRF_XTAL_OP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_OP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_OP input voltage (see Figure 6)	AC-coupled analog signal	–	–	–	400	–	1200	mV_{p-p}
WRF_TCXO_IN Input voltage (see Figure 7)	DC-coupled analog signal	–	–	–	400	–	2500	mV_{p-p}
Frequency tolerance Initial + over temperature	Without trimming	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–131	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–138	dBc/Hz
Phase Noise (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–139	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–146	dBc/Hz
Phase Noise (IEEE 802.11n, 2.4 GHz	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–136	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–143	dBc/Hz
Phase Noise (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–144	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–151	dBc/Hz

a. (Crystal) Use WRF_XTAL_OP and WRF_XTAL_ON, internal power to pin WRF_XTAL_VDD1P2.
b. (TCXO) See "TCXO" on page 28 for alternative connection methods.

c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. The frequency step size is approximately 80 Hz resolution.

Frequency Selection

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset reference frequencies of 12, 13, 14.4, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8, 20, 26, 37.4, and 52 MHz, but also other frequencies in this range, with approximately 80 Hz resolution. The BCM43241 must have the reference frequency set correctly in order for any of the UART or PCM interfaces to function correctly, since all bit timing is derived from the reference frequency.

Note: The fractional-N synthesizer can support many reference frequencies. However, frequencies other than the default require support to be added in the driver plus additional, extensive system testing. Contact Broadcom for further details.

The reference frequency for the BCM43241 may be set in the following ways:

- Set the *xtalfreq=xxxxx* parameter in the nvram.txt file (used to load the driver) to correctly match the crystal frequency.
- Autodetect any of the standard handset reference frequencies using an external LPO clock.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the BCM43241 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto frequency detection to work correctly, the BCM43241 must have a valid and stable 32.768 kHz LPO clock that meets the requirements listed in Table 3 on page 31 and is present during power-on reset.

External 32.768 kHz Low-Power Oscillator

The BCM43241 uses a secondary low-frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some WLAN applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach for WLAN is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 3. If Bluetooth or FM is used then the use of an external clock is always required.

Table 3: External 32.768 kHz Sleep Clock Specifications

Parameter	*LPO Clock*	*Units*
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	0.2–3.3	V, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[a]	>100k <5	Ω pF
Clock jitter (integrated over 300 Hz–15 kHz)	<5	ns
Clock jitter (during initial start-up)	<10,000	ppm

a. When power is applied or switched off.

Section 4: Bluetooth + FM Subsystem Overview

The Broadcom BCM43241 is a Bluetooth 4.0 + EDR-compliant baseband processor/2.4 GHz transceiver with an integrated FM/RDS/RBDS receiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth plus FM radio solution.

The BCM43241 is the optimal solution for any Bluetooth voice and/or data application that also requires an FM radio receiver. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high-speed UART and PCM for audio. The FM subsystem supports the HCI control interface, as well as I^2S and PCM interfaces. The BCM43241 incorporates all Bluetooth 4.0 features including Secure Simple Pairing, Sniff Subrating, as well as Encryption Pause and Resume.

The BCM43241 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

Features

Major Bluetooth features of the BCM43241 include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.0 + (Enhanced Data Rate) EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO) — Voice Connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.0 + HS packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support

- Trigger Broadcom fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see "Host Controller Power Management" on page 38)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and autodetection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

Major FM Radio features include:

- 65 MHz to 108 MHz FM bands supported (US, Europe, and Japan)
- FM subsystem control using the Bluetooth HCI interface
- FM subsystem operates from the system clock
- Improved audio interface capabilities with full-featured bidirectional PCM and I^2S
- I^2S can be master or slave.

FM Receiver-Specific Features Include:

- Excellent FM radio performance with 1 µV sensitivity for 26 dB (S+N)/N
- Signal-dependent stereo/mono blending
- Signal-dependent soft mute
- Auto search and tuning modes
- Audio silence detection
- RDS and RBDS demodulator and decoder with filter and buffering functions
- Automatic frequency jump

Bluetooth Radio

The BCM43241 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmit

The BCM43241 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4−DQPSK for 2 Mbps and 8−DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4−DQPSK, and 8−DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the BCM43241 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM43241 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM43241 uses an internal RF and IF loop filter.

Calibration

The BCM43241 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation throughout the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Section 5: Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode bluetooth Low Energy (BT and BLE operation)
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

Bluetooth Low Energy

The BCM43241 is forward compatible with the impending Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller, which takes commands from the software, and other controllers, which are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

Test Mode Support

The BCM43241 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM43241 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the BCM43241 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management
- FM Power Management

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

Host Controller Power Management

When running in UART mode, the BCM43241 may be configured so that dedicated signals are used for power management handshaking between the BCM43241 and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth-defined power saving modes and standby modes of operation.

Table 4 describes the power-control handshake signals used with the UART interface.

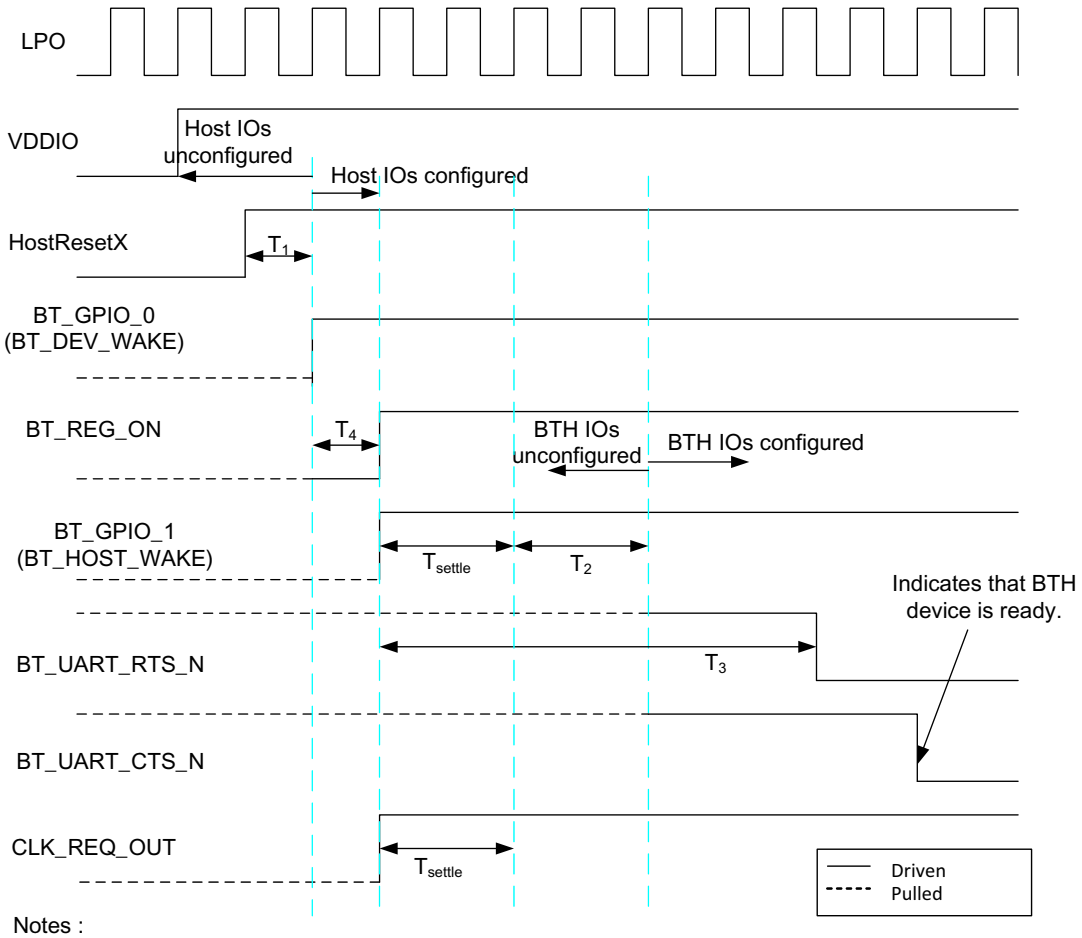
Table 4: Power Control Pin Description

Signal	*Mapped to Pin*	*Type*	*Description*
BT_DEV_WAKE	BT_GPIO_0	I	Bluetooth device wake-up: Signal from the host to the BCM43241 indicating that the host requires attention. • Asserted: The Bluetooth device must wake up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	BT_GPIO_1	O	Host wake-up. Signal from the BCM43241 to the host indicating that the BCM43241 requires attention. • Asserted: Host device must wake up or remain awake. • Deasserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	BT_CLK_REQ_OUT WL_CLK_REQ_OUT	O	The BCM43241 asserts CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The CLK_REQ polarity is active-high.

Table 4: Power Control Pin Description (Cont.)

Signal	Mapped to Pin	Type	Description

Note: Pad function Control Register is set to 0 for these pins. See "Multiplexed Bluetooth GPIO Signals" on page 112 for more details.



Notes :

- T_1 is the time for host to settle its IOs after a reset.
- T_2 is the time for the BTH device to settle its IOs after a reset and ref clk settling time elapsed.
- T_3 is the time for the BT device to complete initialization and drive BT_UART_RTS_N low.
- T_4 is the setup time for BT_WAKE prior to driving BT_REG_ON high; BT_DEV_WAKE must be high prior to BT_REG_ON being released. BT_DEV_WAKE should not be driven low until after the host has completed configuration.
- T_{settle} is the time for the ref clk signal from the host to be guaranteed to have settled.

Figure 8: Start-up Signaling Sequence

BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the BCM43241 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the BCM43241 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the BCM43241 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

  During the low-power shutdown state, provided VDDIO remains applied to the BCM43241, all outputs/inputs keep their existing states. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the BCM43241 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

  Two BCM43241 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the BCM43241 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

FM Power Management

The BCM43241 FM subsystem can operate independently of, or in tandem with, the Bluetooth RF and BBC subsystems. The FM subsystem power management scheme operates in conjunction with the Bluetooth RF and BBC subsystems. The FM block does not have a low power state, it is either on or off.

Wideband Speech

The BCM43241 provides support for wideband speech (WBS) using on-chip Smart Audio technology. The BCM43241 can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bitstream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bitstream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The BCM43241 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 9 and Figure 10 show audio waveforms with and without Packet Loss Concealment. Broadcom PLC/BEC algorithms also support wideband speech.

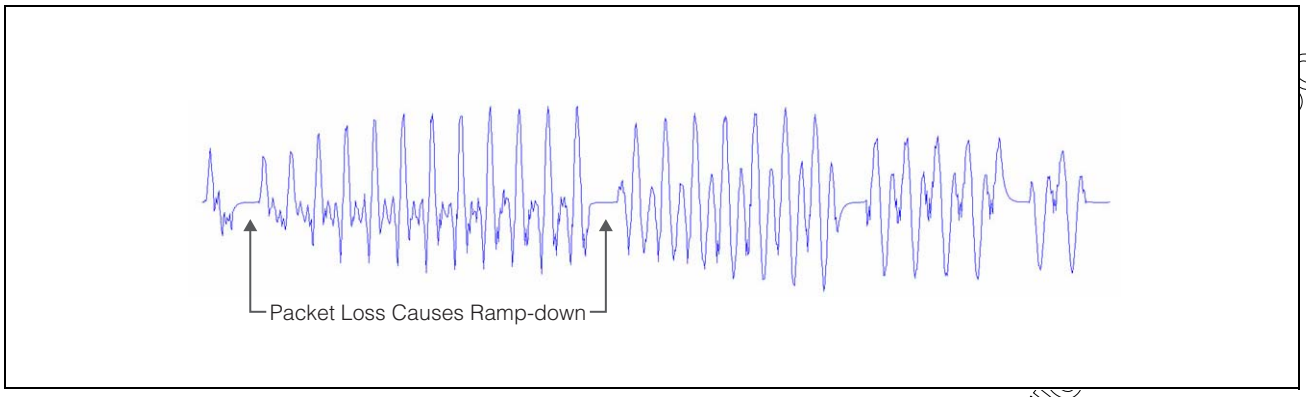


Figure 9: CVSD Decoder Output Waveform Without PLC

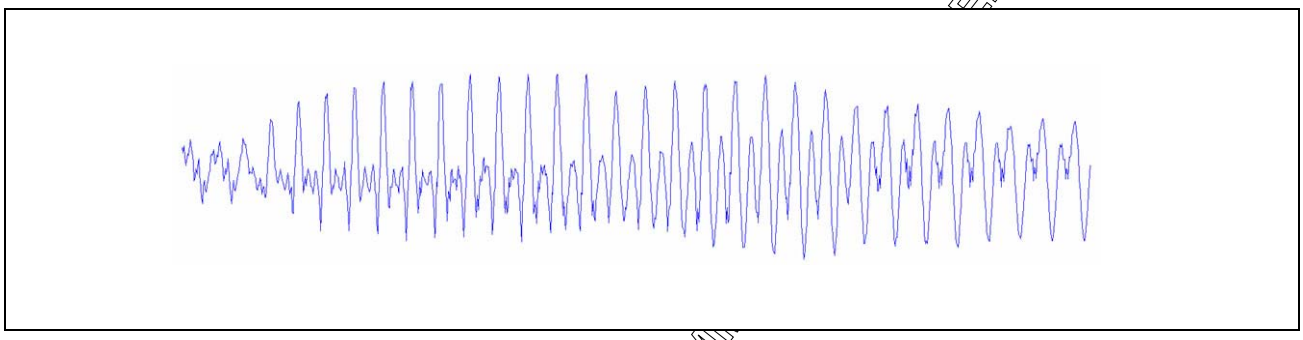


Figure 10: CVSD Decoder Output Waveform After Applying PLC

Audio Rate-Matching Algorithms

The BCM43241 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth or FM audio data rates.

Codec Encoding

The BCM43241 can support SBC and mSBC encoding and decoding for wideband speech.

Multiple Simultaneous A2DP Audio Stream

The BCM43241 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

FM Over Bluetooth

FM Over Bluetooth enables the BCM43241 to stream data from FM over Bluetooth without requiring the host to be awake. This can significantly extend battery life for usage cases where someone is listening to FM radio on a Bluetooth headset.

Burst Buffer Operation

The BCM43241 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

Adaptive Frequency Hopping

The BCM43241 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

Advanced Bluetooth/WLAN Coexistence

The BCM43241 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The BCM43241 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The BCM43241 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The BCM43241 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

Fast Connection (Interlaced Page and Inquiry Scans)

The BCM43241 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

Section 6: Music and Audio

The BCM43241 provides superior total system current during music or audio playback and recording. To enable these functions, several features of the device are combined to provide superior system power consumption.

MP3 Encoder

- ISO/IEC 11172-3 compliant
- Supports 32 kHz sampling frequencies only
- Encodes mono and stereo signals

MP3 Decoder

The MP3 decoder supports mono and stereo audio recording with the following specifications:

- Supports MPEG-1 Layer 3 decoding
- Output is fully bit compliant with MPEG-1 standard specification
- Supports sampling frequencies from 32 kHz to 48 kHz
- Minimum bit-rate supported 32 Kbps and maximum bit-rate supported 320 Kbps for Layer 3

AAC/AAC+ Decoder

Compliant to ISO/IEC 14496-3: 2004 specifications:

- MPEG-2, MPEG-4 AAC LC decoding up to level 2
- SBR tool, up to level 3
- Low power SBR tool
- Full support up to level 3 for the HE AAC profile
- Implicit and explicit SBR signaling mechanisms
- Mono and stereo channel streams decoding sampling frequencies from 8 kHz to 96 kHz only
- ADTS frame decoding

Section 7: Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM® Cortex-M3™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains ROM memory for program storage and boot ROM, and RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the BCM43241 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the BCM4329 and BCM4330 devices.

RAM, ROM, and Patch Memory

The BCM43241 Bluetooth core has internal RAM, which is mapped between general-purpose scratch pad memory and patch memory, and ROM, which is used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

Reset

The BCM43241 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

Section 8: Bluetooth Peripheral Transport Unit

PCM Interface

The BCM43241 supports two independent PCM interfaces that share the pins with the I^2S interfaces. The PCM Interface on the BCM43241 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM43241 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43241.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Slot Mapping

The BCM43241 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The BCM43241 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is 3-bit periods, and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The BCM43241 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM43241 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The BCM43241 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

Multiplexed Bluetooth and FM Over PCM

In this mode of operation, the BCM43241 multiplexes both FM and Bluetooth audio PCM channels over the same interface, reducing the number of required I/Os. This mode of operation is initiated through an HCI command from the host. The format of the data stream consists of three channels: a Bluetooth channel followed by two FM channels (audio left and right). In this mode of operation, the bus data rate only supports 48 kHz operation per channel with 16 bits sent for each channel. This is done to allow the low data rate Bluetooth data to coexist in the same interface as the higher speed I^2S data. To accomplish this, the Bluetooth data is repeated six times for 8 kHz data and three times for 16 kHz data. An initial sync pulse on the PCM_SYNC line is used to indicate the beginning of the frame.

To support multiple Bluetooth audio streams within the Bluetooth channel, both 16 kHz and 8 kHz streams can be multiplexed. This mode of operation is only supported when the Bluetooth host is the master. Figure 11 shows the operation of the multiplexed transport with three simultaneous SCO connections. To accommodate additional SCO channels, the transport clock speed is increased. To change between modes of operation, the transport must be halted and restarted in the new configuration.

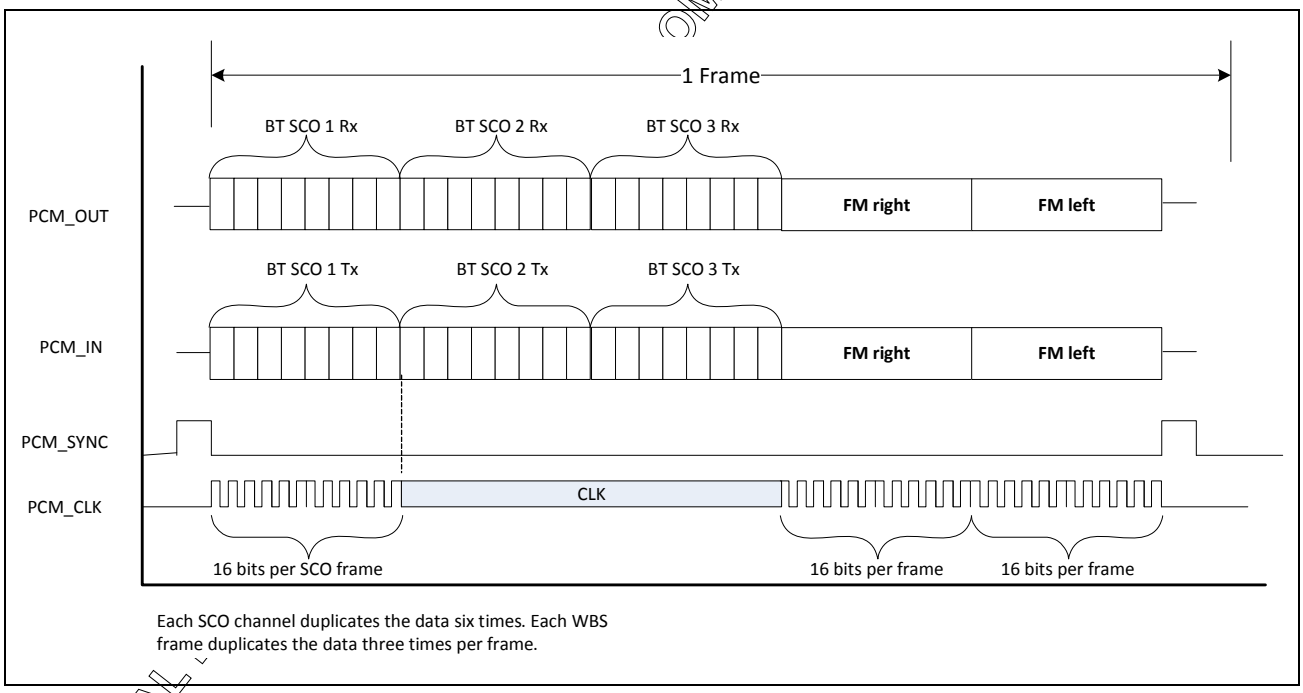


Figure 11: Functional Multiplex Data Diagram

Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. Also, the PCM bus can operate at a rate of up to 24 MHz in this mode. This mode of operation is initiated with an HCI command from the host.

PCM Interface Timing

Short Frame Sync, Master Mode

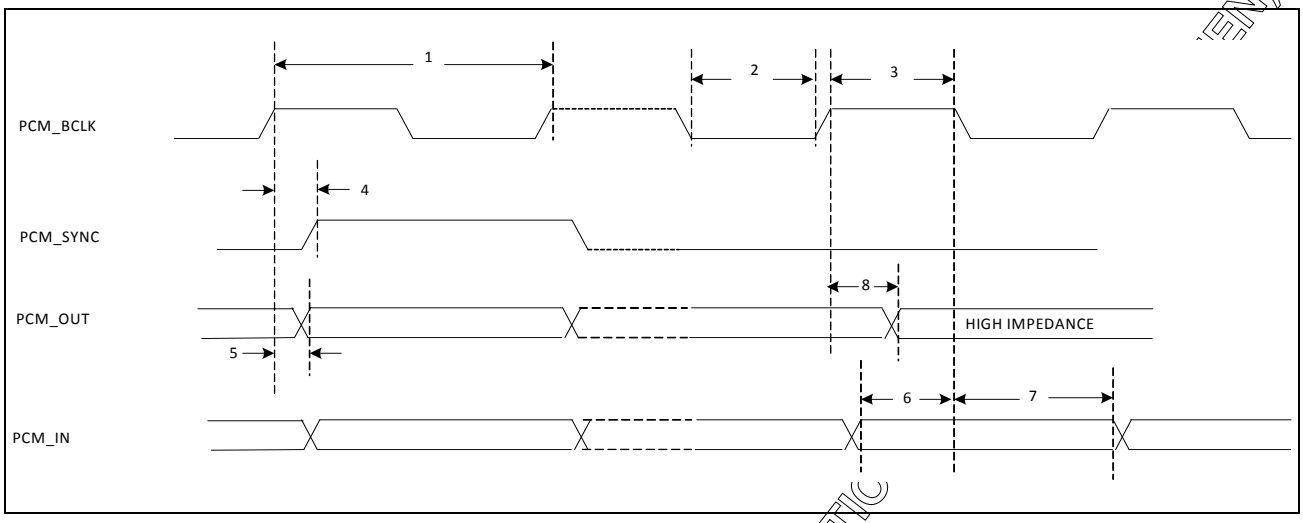


Figure 12: PCM Timing Diagram (Short Frame Sync, Master Mode)

Table 5: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

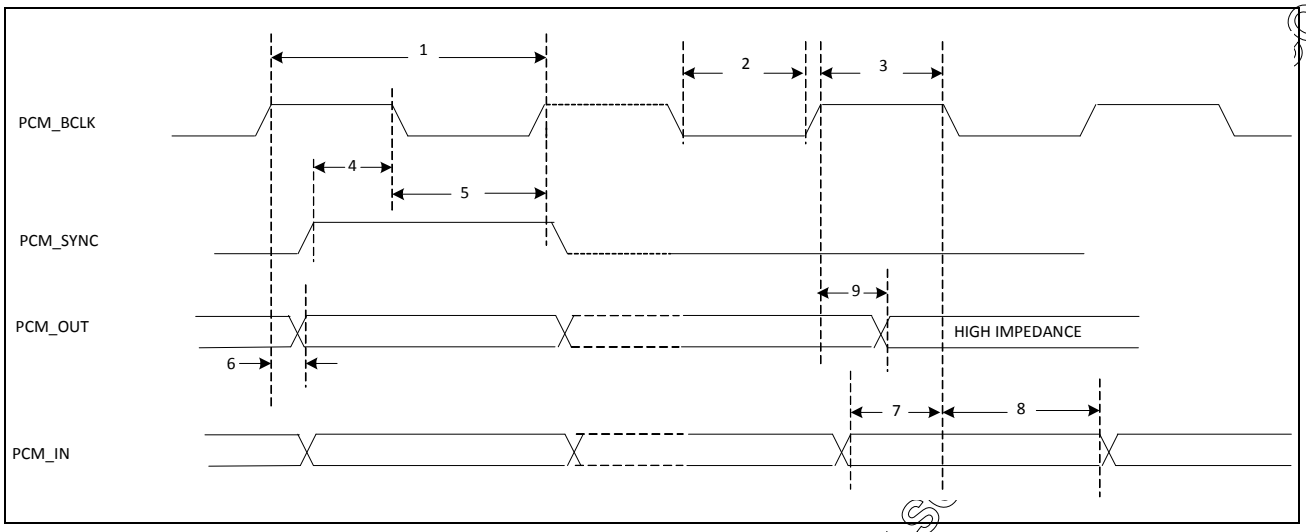


Figure 13: PCM Timing Diagram (Short Frame Sync, Slave Mode)

Table 6: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

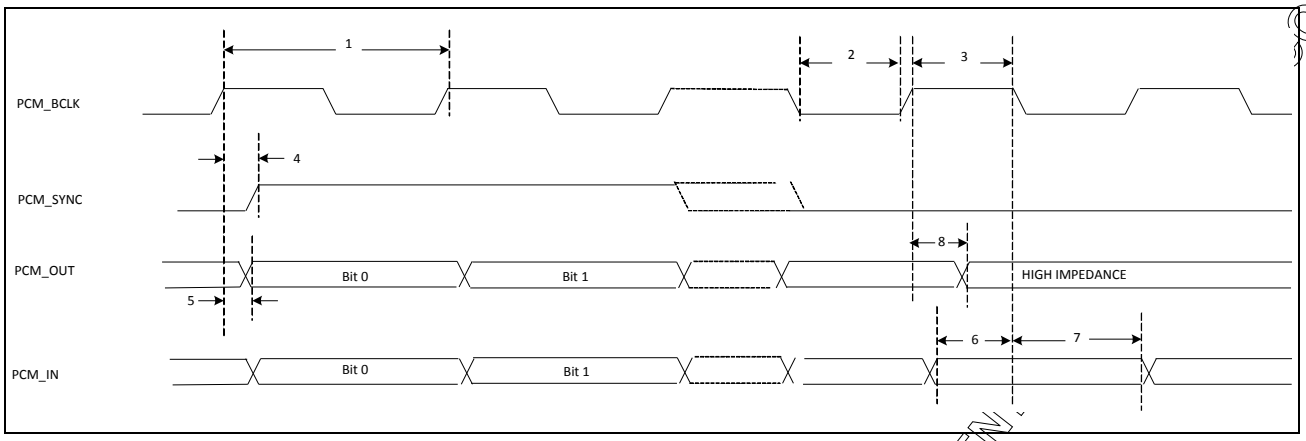


Figure 14: PCM Timing Diagram (Long Frame Sync, Master Mode)

Table 7: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

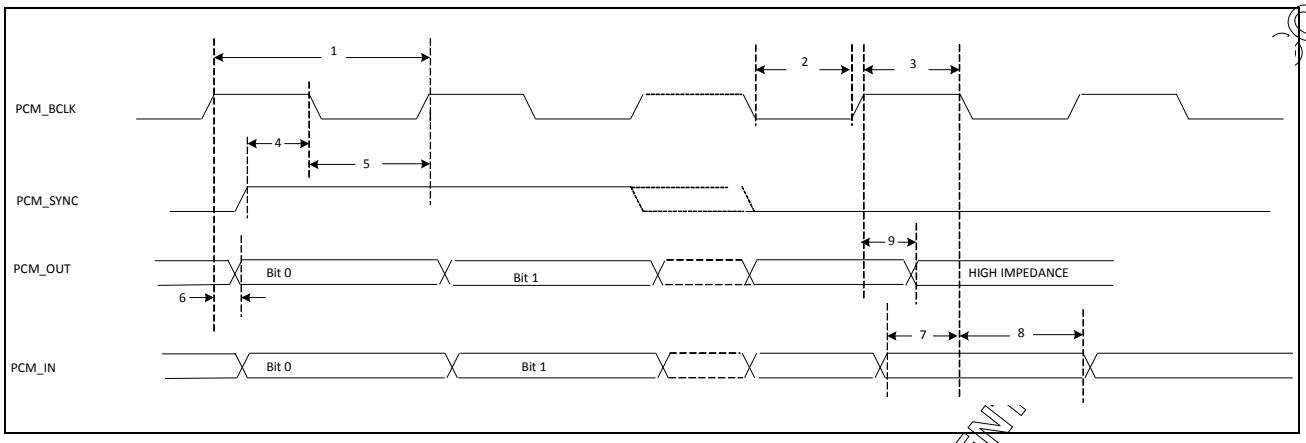


Figure 15: PCM Timing Diagram (Long Frame Sync, Slave Mode)

Table 8: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

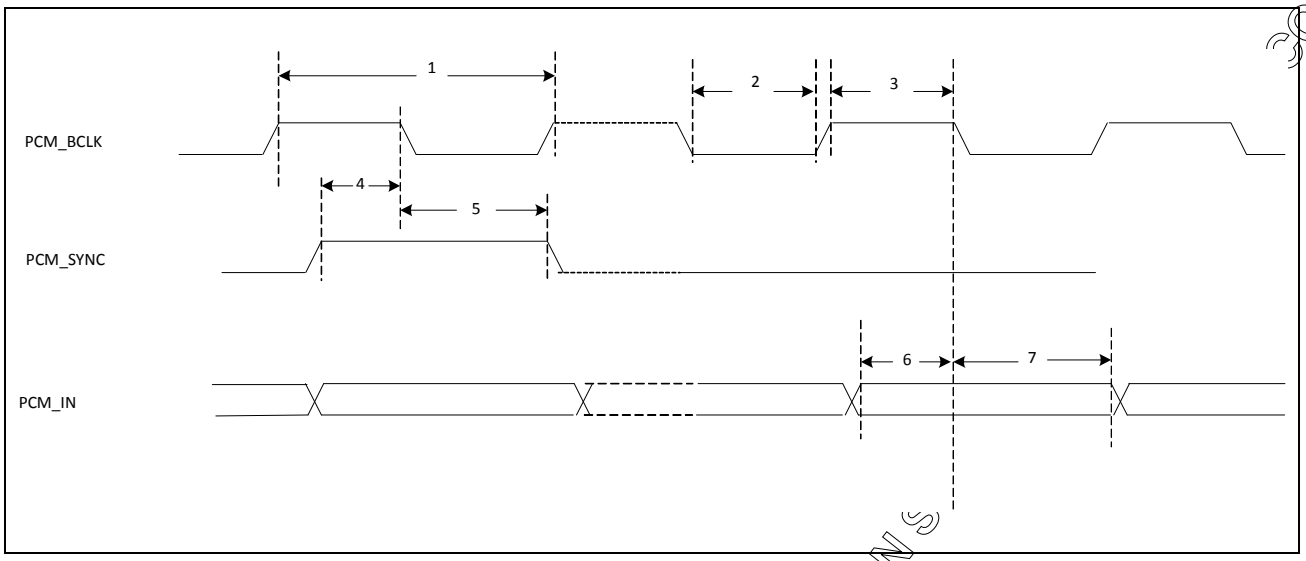


Figure 16: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

Table 9: PCM Burst Mode (Receive Only, Short Frame Sync)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock HIGH	20.8	–	–	ns
3	PCM bit clock LOW	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

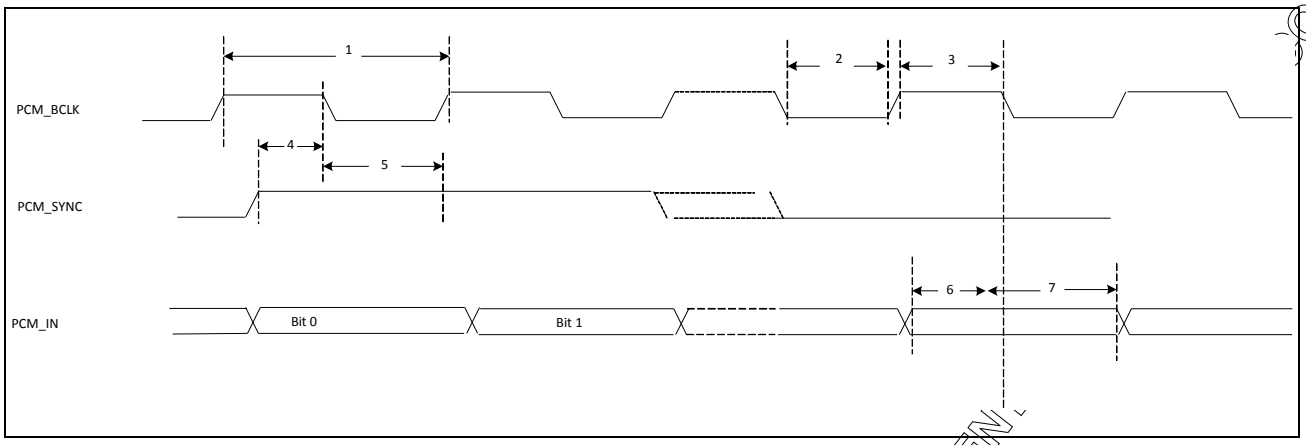


Figure 17: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

Table 10: PCM Burst Mode (Receive Only, Long Frame Sync)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock HIGH	20.8	–	–	ns
3	PCM bit clock LOW	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

UART Interface

The BCM43241 shares a single UART for Bluetooth and FM. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification ("Three-wire UART Transport Layer"). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM43241 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM43241 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 11: Example of Common Baud Rates

Desired Rate	*Actual Rate*	*Error (%)*
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

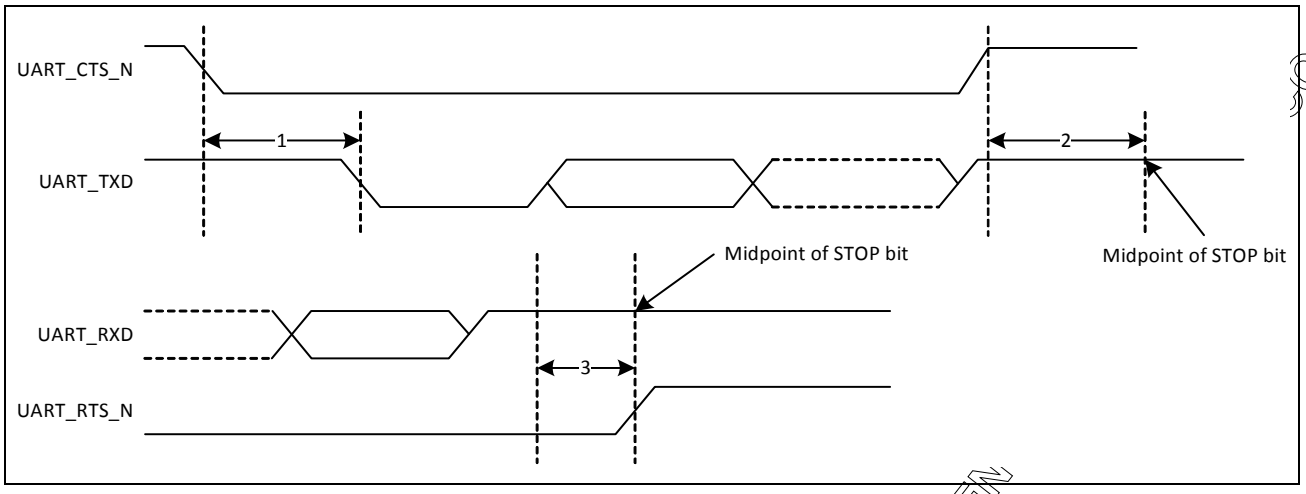


Figure 18: UART Timing

Table 12: UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

I²S Interface

The BCM43241 supports two independent I²S digital audio ports: one for Bluetooth audio, and one for high-fidelity FM audio. The I²S interface for FM audio supports both master and slave modes. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the BCM43241 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

I²S Timing

Note: Timing values specified in Table 13 are relative to high and low threshold levels.

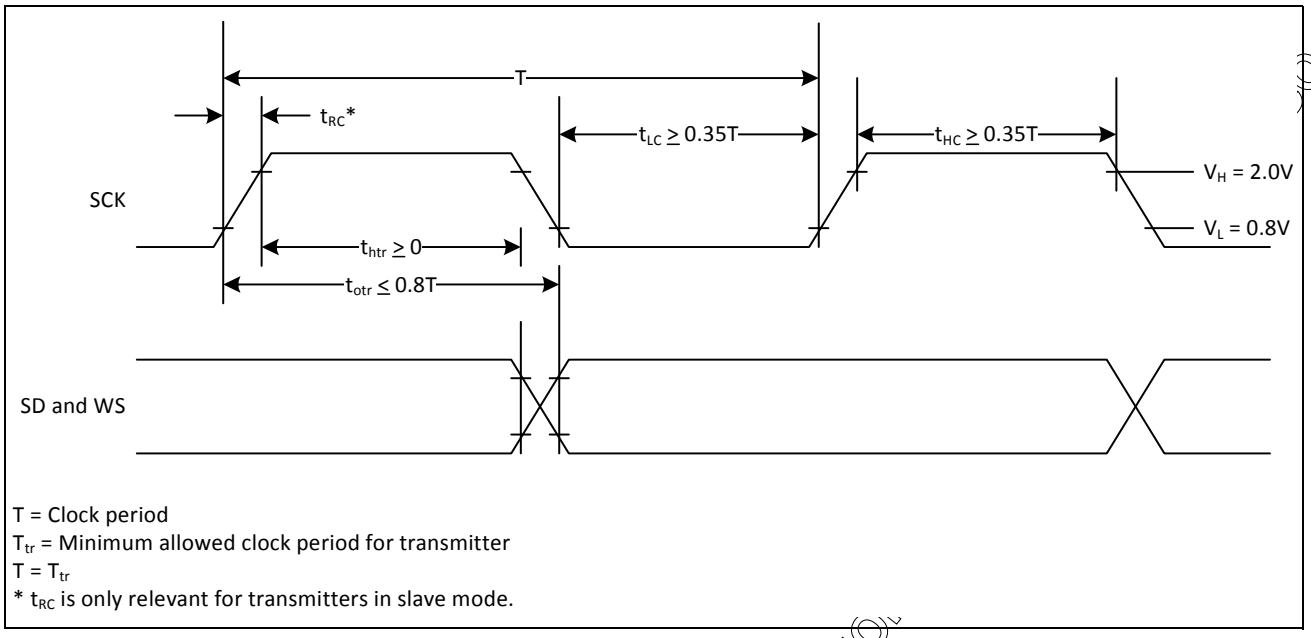
Table 13: Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	1
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–			–	4
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	5
Hold time t_{htr}	0	–	–	–		–	–	–	4
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time t_{hr}	–	–	–	–	–	0	–	–	6

Note:

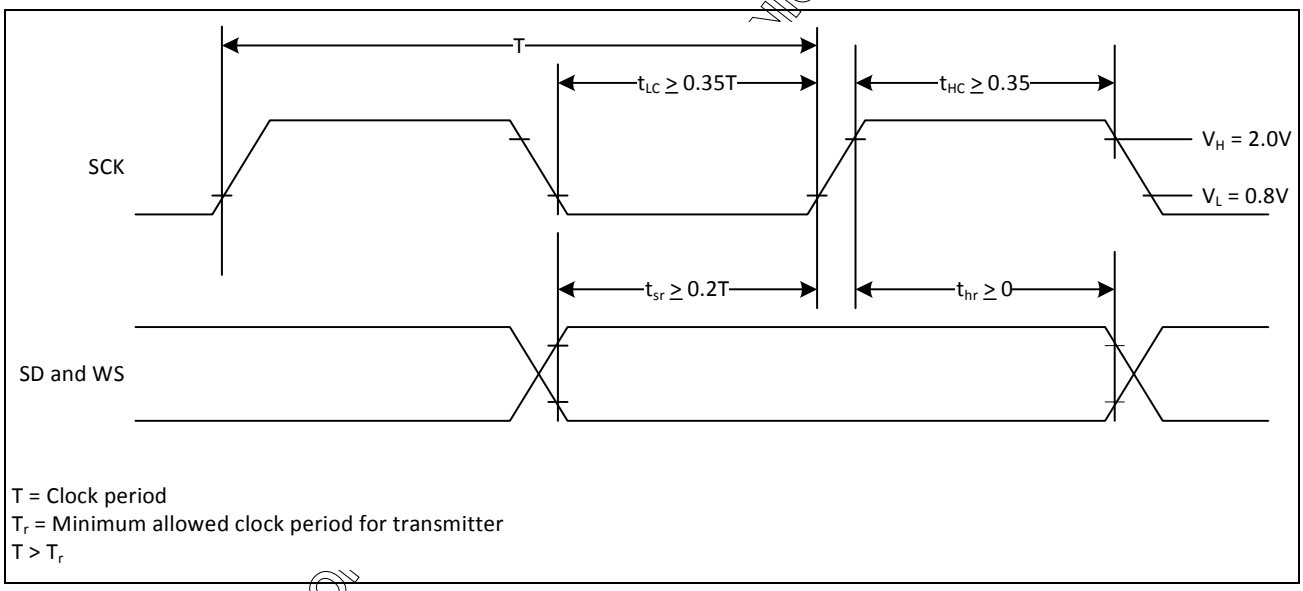
- The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
- Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC}, which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- The data setup and hold time must not be less than the specified receiver setup and hold time.

Note: The time periods specified in Figure 19 and Figure 20 are defined by the transmitter speed. The receiver specifications must match transmitter performance.



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 19: I²S Transmitter Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Figure 20: I²S Receiver Timing

Section 9: FM Receiver Subsystem

FM Radio

The BCM43241 includes a completely integrated FM radio receiver with RDS/RBDS covering all FM bands from 65 MHz to 108 MHz. The receiver is controlled through commands on the HCI. FM received audio is available in digital form through I^2S or PCM. The FM radio operates from the external clock reference.

Digital FM Audio Interfaces

The FM audio can be transmitted via the shared PCM and I^2S pins, and the sampling rate is programmable. The BCM43241 supports a three-wire PCM or I^2S audio interface in either master or slave configuration. The master or slave configuration is selected using vendor-specific commands over the HCI interface. In addition, multiple sampling rates are supported, derived from either the FM or Bluetooth clocks. In master mode, the clock rate is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

In slave mode, any clock rate is supported up to a maximum of 3.072 MHz.

FM Over Bluetooth

The BCM43241 can output received FM audio onto Bluetooth using one of following three links: eSCO, WBS, and A2DP. In all of the above modes, once the link has been set up, the host processor can enter sleep mode while the BCM43241 continues to stream FM audio to the remote Bluetooth device, allowing the system current consumption to be minimized.

eSCO

In this use case, the stereo FM audio is downsampled to 8 kHz, and a mono or stereo stream is then sent through the Bluetooth eSCO link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

Wideband Speech Link

In this case, the stereo FM audio is downsampled to 16 kHz, and a mono or stereo stream is then sent through the Bluetooth wideband speech link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

A2DP

In this case, the stereo FM audio is encoded by the on-chip SBC encoder and transported as an A2DP link to a remote Bluetooth device. Sampling rates of 48 kHz, 44.1 kHz, and 32 kHz joint stereo are supported. An A2DP 'lite' stack is implemented in the BCM43241 to support this use case, which eliminates the need to route the SBC-encoded audio back to the host to create the A2DP packets.

Autotune and Search Algorithms

The BCM43241 supports a number of FM search and tune functions. This allows the host to implement many convenient user functions, which are accessed through the Broadcom FM stack.

- Tune to Play — Allows the FM receiver to be programmed to a specific frequency.
- Search for SNR > Threshold — Checks the power level of the available channel and the estimated SNR of the channel to help achieve precise control of the expected sound quality for the selected FM channel. Specifically, the host can adjust its SNR requirements to retrieve a signal with a specific sound quality or adjust this to return the weakest channels.
- Alternate Frequency Jump — Allows the FM receiver to automatically jump to an alternate FM channel that carries the same information, but has a better SNR. For example, when traveling, a user may pass through a region where a number of channels carry the same station. When the user passes from one area to the next, the FM receiver can automatically switch to another channel with a stronger signal to spare the user from having to manually change the channel to continue listening to the same station.

Audio Features

A number of features are implemented in the BCM43241 to provide the best possible audio experience for the user.

- Mono/Stereo Blend or Switch: The BCM43241 provides automatic control of the stereo or mono settings based on the FM signal carrier-to-noise ratio (C/N). This feature is used to maintain the best possible audio SNR based on the FM channel condition. Two modes of operation are supported:
  - Blend: In this mode, fine control of stereo separation is used to achieve optimal audio quality over a wide range of input C/N. The amount of separation is fully programmable. In Figure 21, the separation is programmed to maintain a minimum 50 dB SNR across the blend range.
  - Switch: In this mode, the audio switches from full stereo to full mono at a predetermined level to

maintain optimal audio quality. The stereo-to-mono switch point and the mono-to-stereo switch point are fully programmable to provide the desired amount of audio SNR. In Figure 22, the switch point is programmed to switch to mono to maintain a 40 dB SNR.

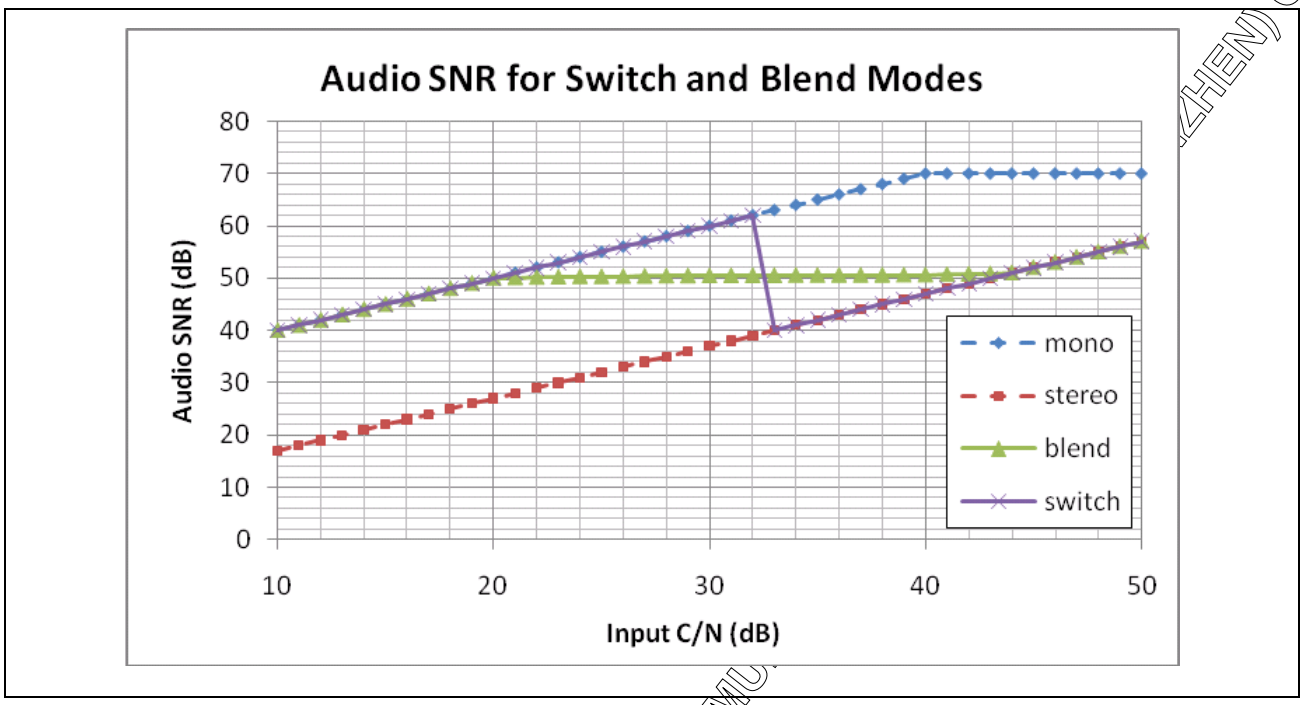


Figure 21: Example Blend/Switch Usage

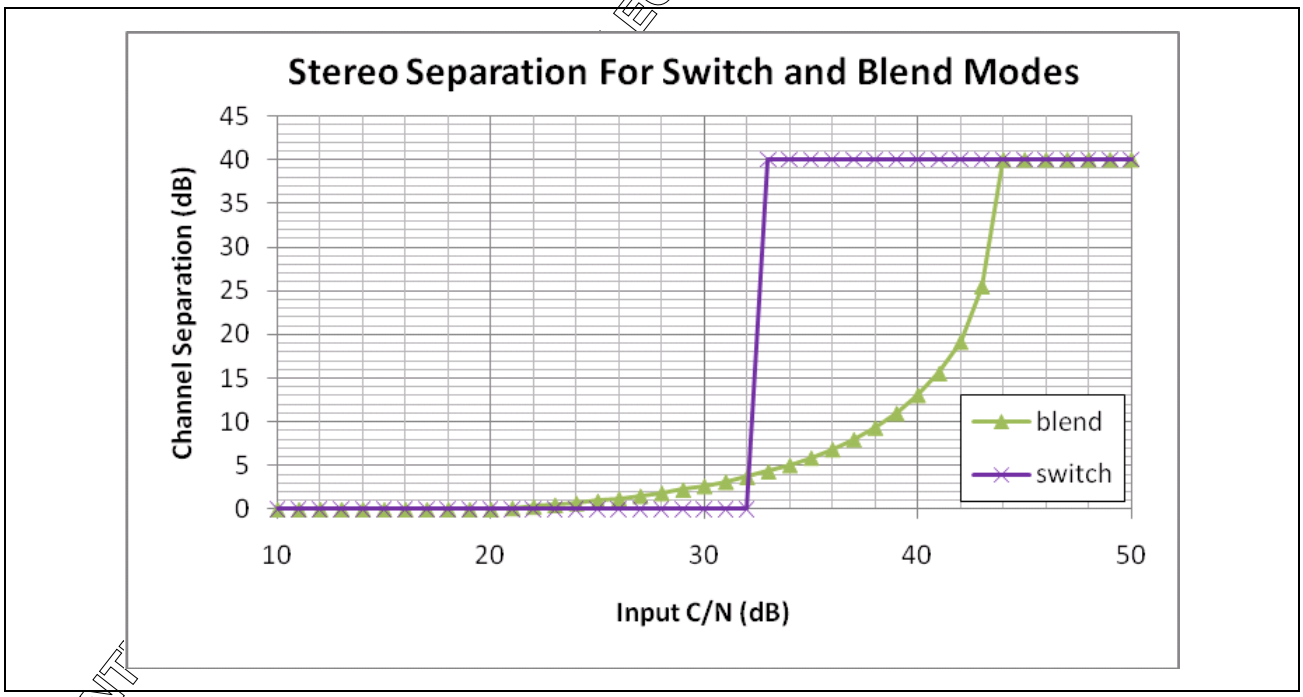


Figure 22: Example Blend/Switch Separation

- Soft Mute: Improves the user experience by dynamically muting the output audio proportionate to the FM signal C/N. This prevents the user from being assaulted with a blast of static. The mute characteristic is fully programmable to accommodate fine-tuning of the output signal level. An example mute characteristic is shown in Figure 23.

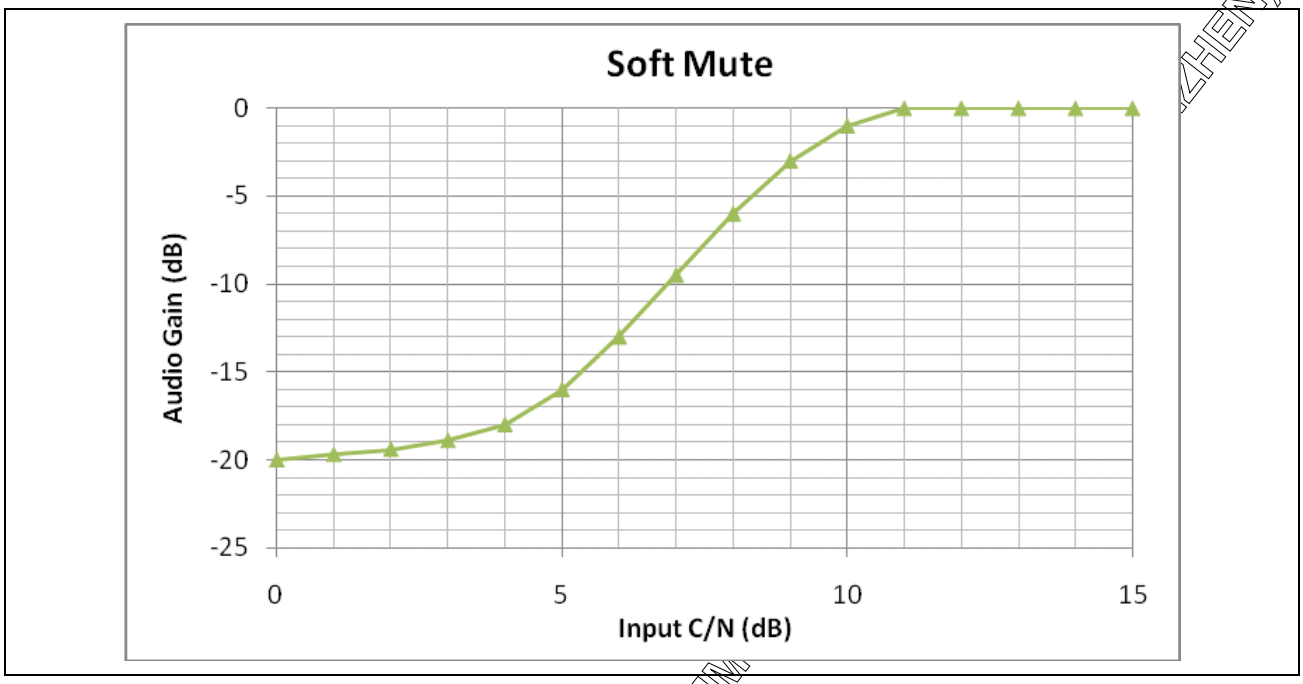


Figure 23: Example Soft Mute Characteristic

- High Cut: A programmable high-cut filter is provided to reduce the amount of high-frequency noise caused by static in the output audio signal. Like the soft mute circuit, it is fully programmable to allow for any amount of high cut based on the FM signal C/N.
- Audio Pause Detect: The FM receiver monitors the magnitude of the audio signal and notifies the host through an interrupt when the magnitude of the signal has fallen below the threshold set for a programmable period. This feature can be used to provide alternate frequency jumps during periods of silence to minimize disturbances to the listener. Filtering techniques are used within the audio pause detection block to provide more robust presence-to-silence detection and silence-to-presence detection.
- Automatic Antenna Tuning: The BCM43241 has an on-chip automatic antenna tuning network. When used with a single off-chip inductor, the on-chip circuitry automatically chooses an optimal on-chip matching component to obtain the highest signal strength for the desired frequency. The high-Q nature of this matching network simultaneously provides out-of-band blocking protection as well as a reduction of radiated spurious emissions from the FM antenna. It is designed to accommodate a wide range of external wire antennas.

On-Chip MP3 Encoding

In this mode of operation, the device can record the FM audio to MP3, then output the MP3 data over the HCI interface. The feature effectively offloads the MP3 recording processing load from the host and assists in FM time shift applications. This feature can also be used in conjunction with burst mode buffering to provide significant FM system record times.

RDS/RBDS

The BCM43241 integrates an RDS/RBDS modem and decoder. The decoder includes programmable filtering and buffering functions. The RDS/RBDS data can be read out through the HCI interface.

Supported RDS/RBDS functionality includes:

- Block decoding, error correction, and synchronization
- Flywheel synchronization feature allows the host to set parameters for acquisition, maintenance, and loss of sync. (It is possible to set up the BCM43241 such that synch is achieved when a minimum of two good blocks (error-free) are decoded in sequence. The number of good blocks required for sync is programmable.)
- Storage capability up to 126 blocks of RDS data
- Full or partial block B match detect and interrupt to host
- Audio pause detection with programmable parameters
- Program Identification (PI) code detection and interrupt to host
- Automatic frequency jump

Section 10: WLAN Global Functions

WLAN CPU and Memory Subsystem

The BCM43241 includes an integrated ARM Cortex-M3™ processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for Thumb®-2 instruction set. ARM Cortex-M3 delivers 30% more performance gain over ARM7TDMI.

At 0.19 µW/MHz, the Cortex-M3 is the most power-efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for Code and Data access (ICode/DCode and System buses). ARM Cortex-M3 supports extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 576 KB RAM and 640 KB ROM.

One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 3072-bit One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

GPIO Interface

The BCM43241 has 16 general-purpose I/O (GPIO) that can be used to connect to various external devices.

Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. An internal (programmable) pull-up/pull-down resistor is included on each GPIO.

External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external colocated wireless device, such as GPS, WiMAX, or UWB, to manage wireless medium sharing for optimum performance. The following signals can be enabled by software on the indicated WL_GPIO pins:

- ERCX_STATUS WL_GPIO2
- ERCX_FREQ WL_GPIO3
- ERCX_RF_ACTIVE WL_GPIO4
- ERCX_TXCONF WL_GPIO5
- ERCX_PRISEL WL_GPIO12

UART Interface

One UART interface can be enabled by software as an alternate function on pins WL_GPIO_14 and WL_GPIO_15. Provided primarily for debugging during development, this UART enables the BCM43241 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of 64 × 8 in each direction.

JTAG Interface

The BCM43241 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

The JTAG interface (multiplexed on the GPIO pins) is enabled when the JTAG_SEL pin is asserted high.

Section 11: WLAN Host Interfaces

SDIO v3.0

The BCM43241 WLAN section supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50 (100 MHz), SDR104 (208 MHz) and DDR50 (50 MHz, dual data rates) in addition to the 3.3V default speed (25 MHz) and high speed (50 MHz). For the exact BCM43241 SDIO timings, see Section 21: "Interface Timing and AC Characteristics," on page 158.

The BCM43241 has the ability to map the interrupt signal onto a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

The BCM43241 supports the new SDIO 3.0 cmd11 to switch from 3.3V signaling to 1.8V signaling.

SDIO mode is enabled using the strapping option pins strap_host_ifc_[3:1] (Table 21: "WLAN GPIO Functions and Strapping Options (Advance Information)," on page 111).

Three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

SDIO Pin Descriptions

Table 14: SDIO Pin Description

SD 4-Bit Mode		*SD 1-Bit Mode*		*gSPI Mode*	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait	NC	Not used
DATA3	Data line 3	N/C	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

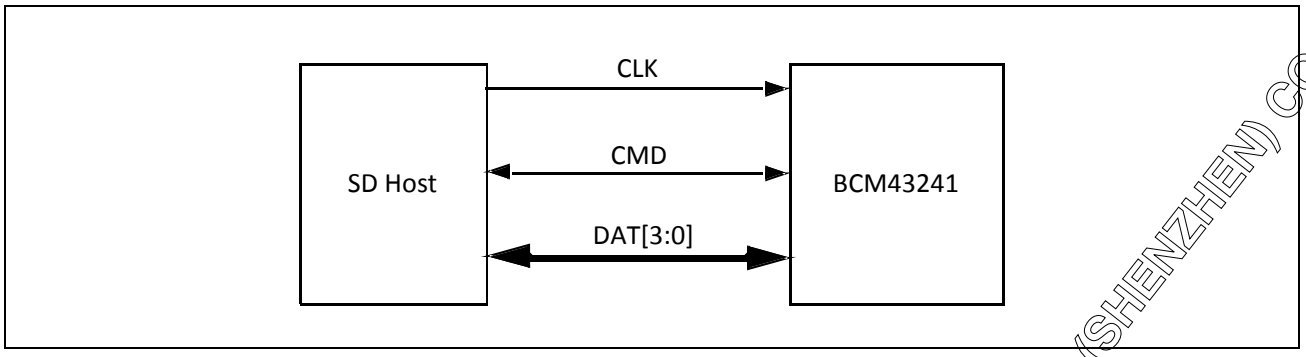


Figure 24: Signal Connections to SDIO Host (SD 4-Bit Mode)

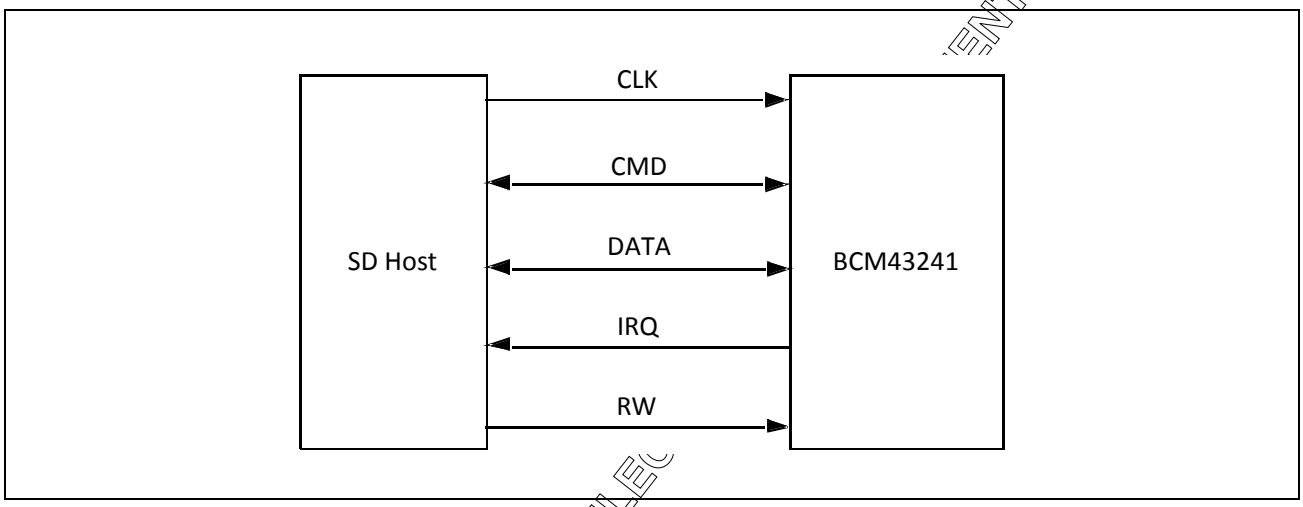


Figure 25: Signal Connections to SDIO Host (SD 1-Bit Mode)

Generic SPI Mode

In addition to the full SDIO mode, the BCM43241 includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Supports up to 48 MHz operation
- Supports fixed delays for responses and data from device
- Supports alignment to host gSPI frames (16 or 32 bits)
- Supports up to 2 KB frame size per transfer
- Supports little endian and big endian configurations
- Supports configurable active edge for shifting
- Supports packet transfer through DMA for WLAN

gSPI mode is enabled using the strapping option pins strap_host_ifc_[3:1], Table 21: "WLAN GPIO Functions and Strapping Options (Advance Information)," on page 111.

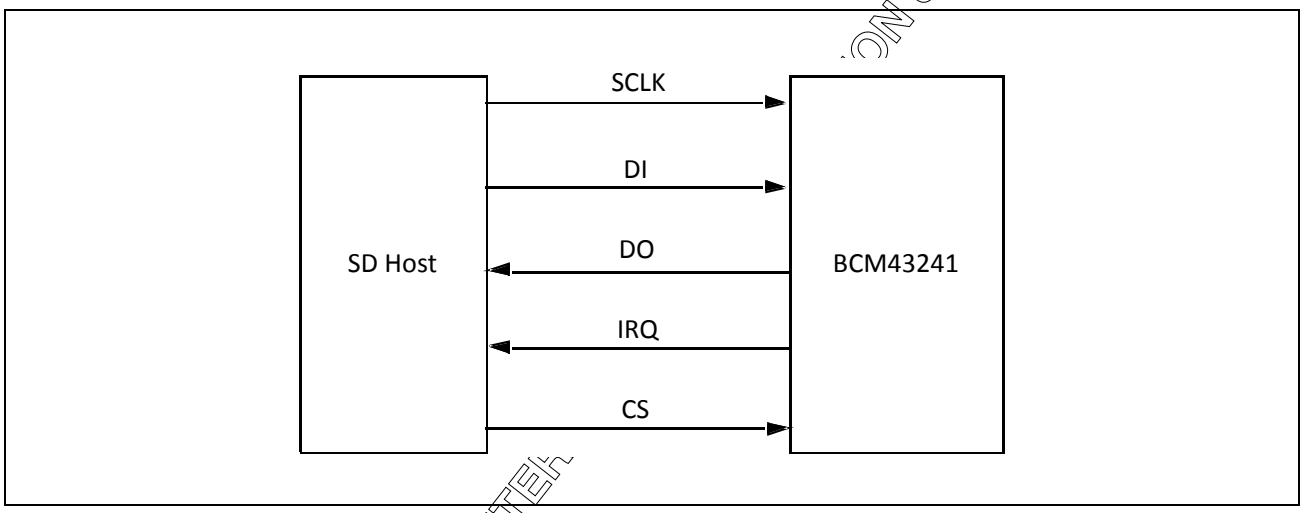


Figure 26: Signal Connections to SDIO Host (gSPI Mode)

SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianness is supported in both modes. Figure 27 and Figure 28 show the basic write and write/read commands.

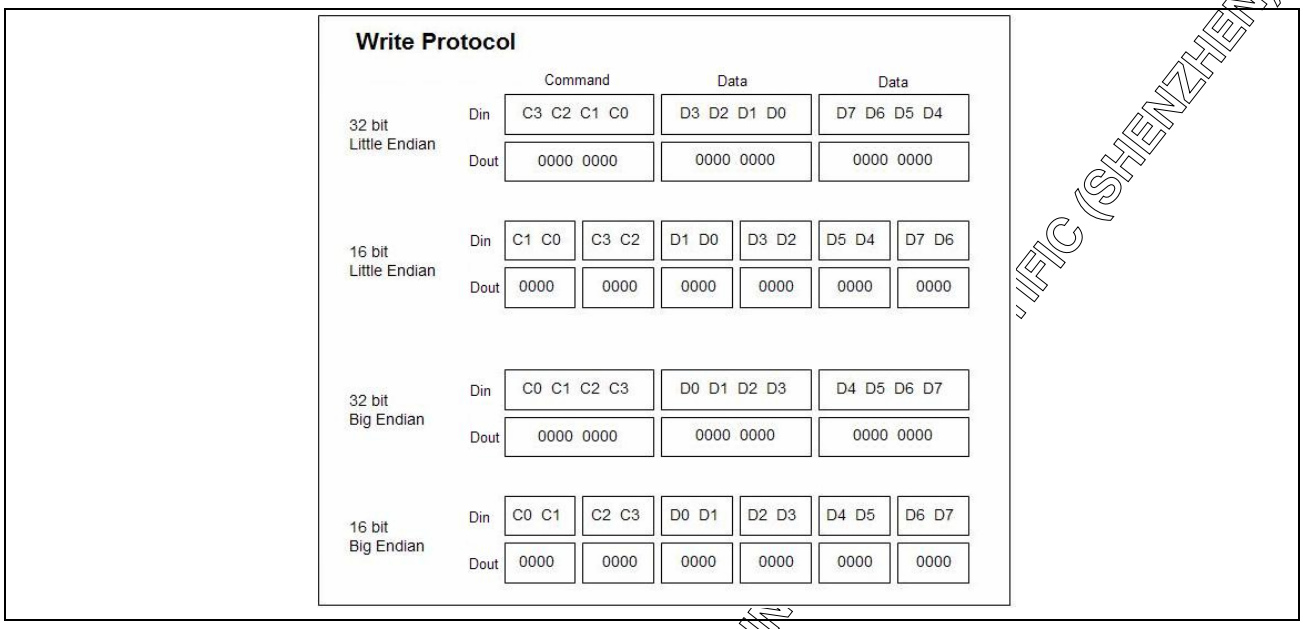


Figure 27: gSPI Write Protocol

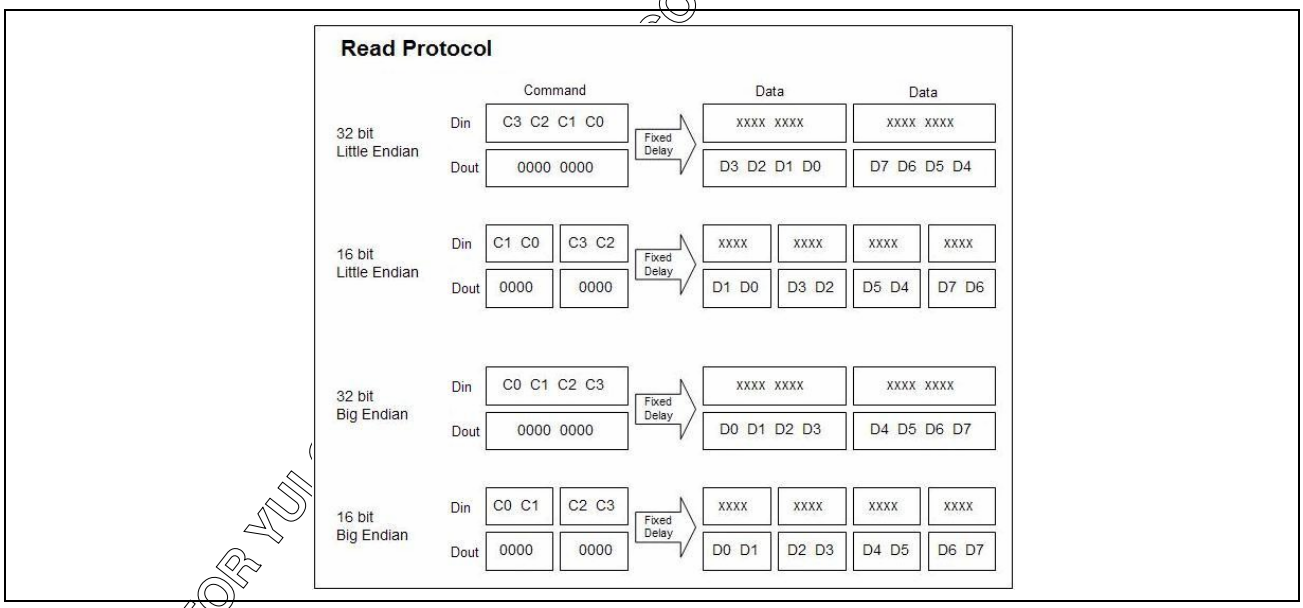


Figure 28: gSPI Read Protocol

Command Structure

The gSPI command structure is 32 bits. The bit positions and definitions are shown in Figure 29.

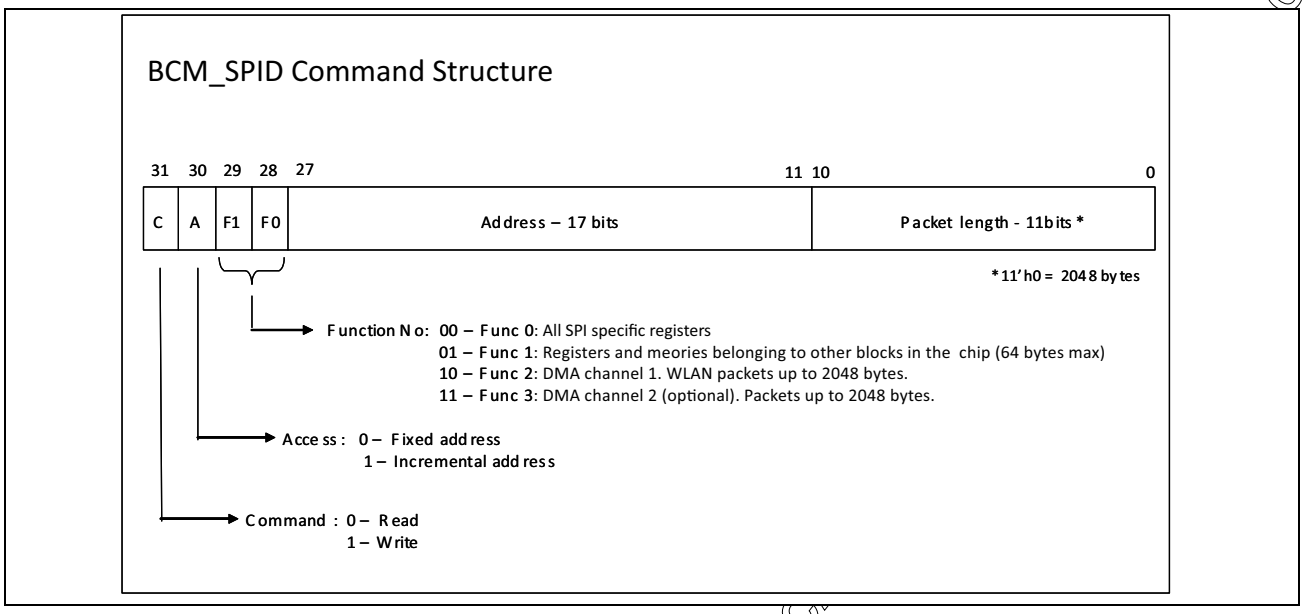


Figure 29: gSPI Command Structure

Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

Write/Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising clock edge of the clock burst for the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go high between the command/address and the data and b) the time interval between the command/address is not fixed.

Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about any packet errors, protocol errors, information about available packet in the RX queue, etc. The status information helps in reducing the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification is shown in Figure 30 and Figure 31 on page 73. See Table 15 on page 73 for information on status field details.

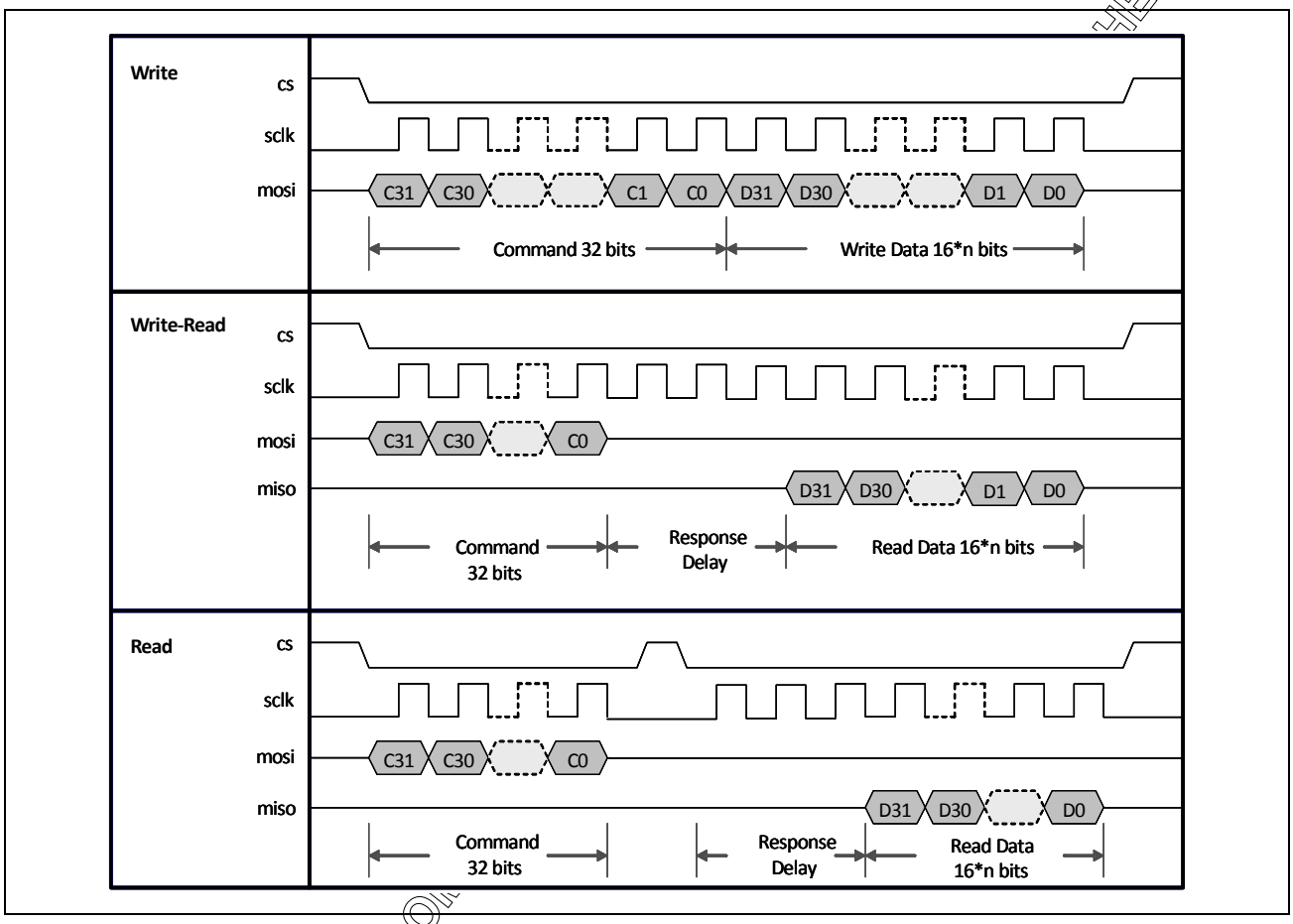


Figure 30: gSPI Signal Timing Without Status

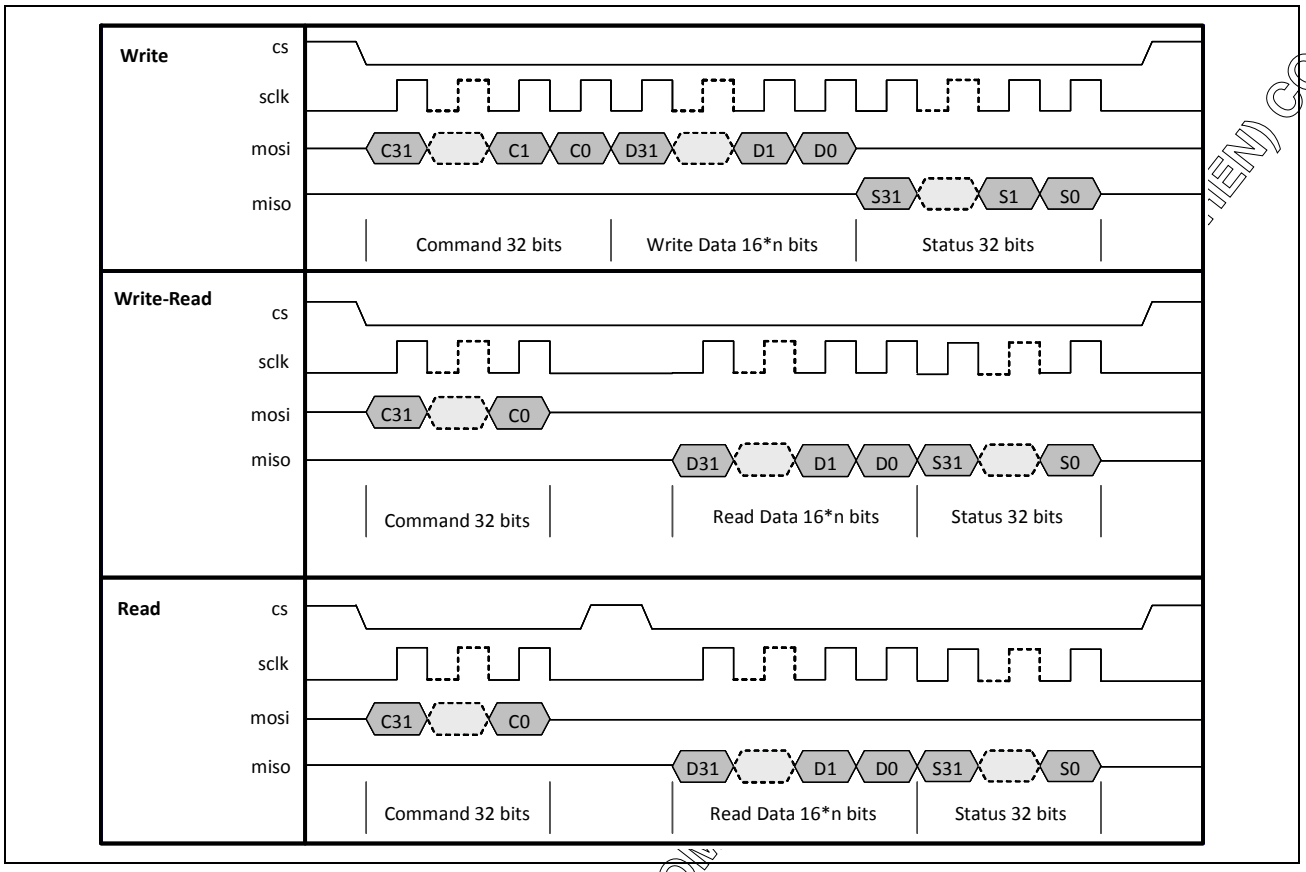


Figure 31: gSPI Signal Timing with Status (Response Delay = 0)

Table 15: gSPI Status Field Details

Bit	*Name*	*Description*
0	Data not available	The requested read data is not available.
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command
3	F2 interrupt	F2 channel interrupt
4	F3 interrupt	F3 channel interrupt
5	F2 RX Ready	F2 FIFO is ready to receive data (FIFO empty)
6	F3 RX Ready	F3 FIFO is ready to receive data (FIFO empty)
7	Reserved	–
8	F2 Packet Available	Packet is available/ready in F2 TX FIFO
9:19	F2 Packet Length	Length of packet available in F2 FIFO
20	F3 Packet Available	Packet is available/ready in F3 TX FIFO
21:31	F3 Packet Length	Length of packet available in F3 FIFO

gSPI Host-Device Handshake

To initiate communication through the gSPI after power-up, the host needs to bring up the WLAN/Chip by writing to the wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the BCM43241 is ready for data transfer. The device can signal an interrupt to the host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the host using the WLAN IRQ line whenever it has any information to pass to the host. On getting an interrupt, the host needs to read the interrupt and/or status register to determine the cause of interrupt and then take necessary actions.

Bootup Sequence

After power-up, the gSPI host needs to wait 150 ms for the device to be out of reset. For this, the host needs to poll with a read command to F0 addr 0x14. Address 0x14 contains a predefined bit pattern. As soon as the host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the host needs to set the wake-up WLAN bit (F0 reg 0x00 bit 7). The wake-up WLAN issues a clock request to the PMU.

For the first time after power-up, the host must wait for the availability of low-power clock inside the device. Once that is available, the host must write to a PMU register to set the crystal frequency, which turns on the PLL. After the PLL is locked, the chipActive interrupt is issued to the host. This interrupt indicates the device awake/ready status. See Table 16 for information on gSPI registers.

In Table 16, the following notation is used for register access:

- R: Readable from host and CPU
- W: Writable from host
- U: Writable from CPU

Table 16: gSPI Registers

Address	Register	Bit	Access	Default	Description
x0000	Word length	0	R/W/U	0	0: 16-bit word length 1: 32-bit word length
	Endianness	1	R/W/U	0	0: Little Endian 1: Big Endian
	High-speed mode	4	R/W/U	1	0: Normal mode. RX and TX at different edges. 1: High speed mode. RX and TX on same edge (default).
	Interrupt polarity	5	R/W/U	1	0: Interrupt active polarity is low. 1: Interrupt active polarity is high (default).
	Wake-up	7	R/W	0	A write of 1 will denote a wake-up command from the host to the device. This will be followed by an F2 Interrupt from the gSPI device to the host, indicating device awake status.
x0001	Response delay	7:0	R/W/U	8'h04	Configurable read response delay in multiples of 8 bits.

Table 16: gSPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x0002	Status enable	0	R/W	1	0: no status sent to host after read/write 1: status sent to host after read/write
	Interrupt with status	1	R/W	0	0: do not interrupt if status is sent 1: interrupt host even if status is sent
	Response delay for all	2	R/W	0	0: response delay applicable to F1 read only 1: response delay applicable to all function read
x0003	Reserved	–	–	–	–
x0004	Interrupt register	0	R/W	0	Requested data not available; cleared by writing a 1 to this location
		1	R	0	F2/F3 FIFO underflow due to last read
		2	R	0	F2/F3 FIFO overflow due to last write
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow due to last write
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006–x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular Interrupt is enabled if a corresponding bit is set
x0008–x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C–x000D	F1 info register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 max packet size
x000E–x000F	F2 info register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 max packet size
x0010–x0011	F3 info register	0	R/U	1	F3 enabled
		1	R	0	F3 ready for data transfer
		15:2	R/U	14'h800	F3 max packet size
x0014–x0017	Test–Read only register	31:0	R	32'hFEED BEAD	This register contains a predefined pattern, which the host can read and determine if the gSPI interface is working properly.
x0018–x001B	Test–R/W register	31:0	R/W/U	32'h0000 0000	This is a dummy register where the host can write some pattern and read it back to determine if the gSPI interface is working properly.

Figure 32 shows the WLAN bootup sequence from power-up to firmware download.

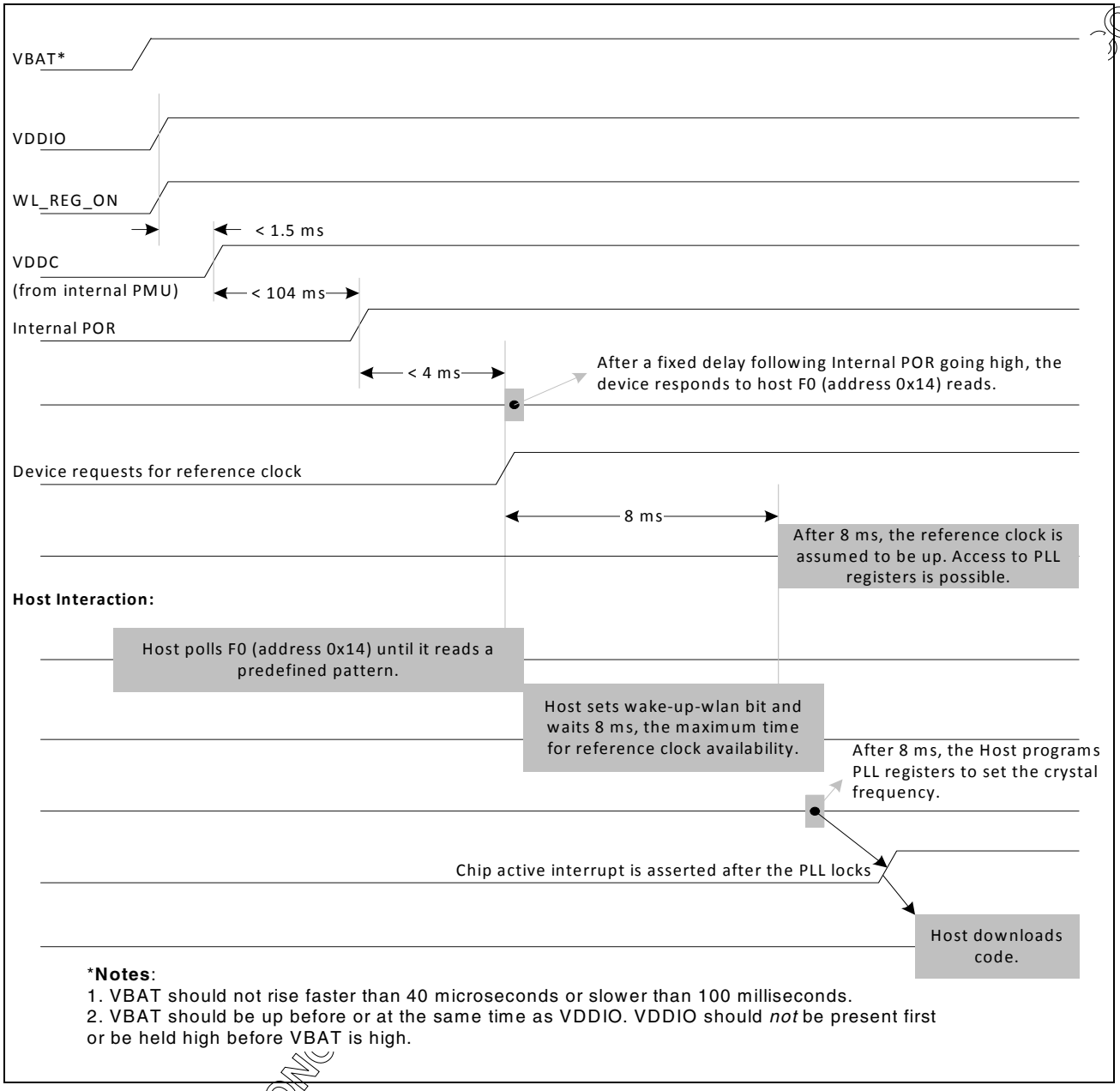


Figure 32: WLAN Bootup Sequence

HSIC Interface

As an alternative to SDIO, an HSIC host interface can be enabled using the strapping option pins strap_host_ifc_[3:1] (Table 21: “WLAN GPIO Functions and Strapping Options (Advance Information),” on page 111. HSIC is a simplified derivative of the USB2.0 interface designed to replace a standard USB PHY and cable for short distances (up to 10 cm) on board point-to-point connections. Using two signals, a bidirectional data strobe (STROBE) and a bidirectional DDR data signal (DATA), it provides high-speed serial 480 Mbps USB transfers that are 100% host driver compatible with traditional USB 2.0 cable-connected topologies.

Figure 33 shows the blocks in the HSIC device core.

Key features of HSIC include:

- High-speed 480 Mbps data rate only
- Source-synchronous serial interface using 1.2V LVCMOS signal levels
- No power consumed except when a data transfer is in progress
- Maximum trace length of 10 cm
- No Plug-n-Play support, no hot attach/removal

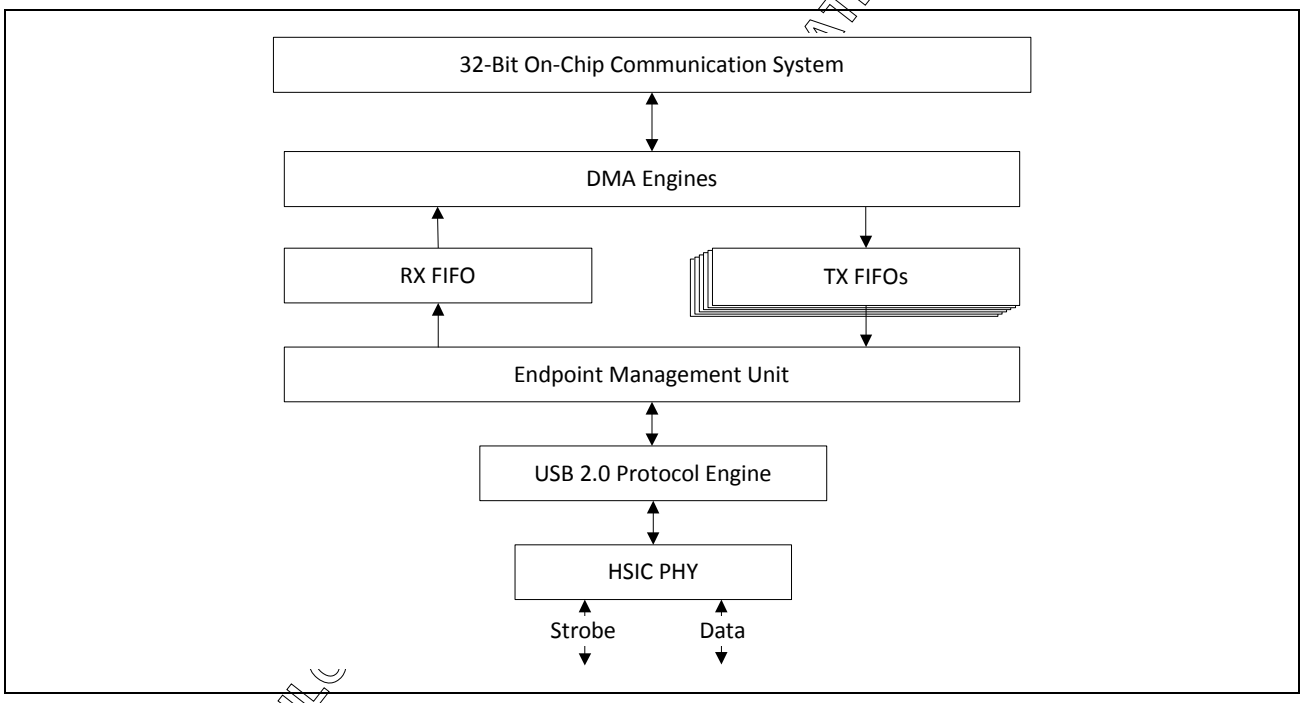


Figure 33: HSIC Device Block Diagram

Section 12: Wireless LAN MAC and PHY

MAC Features

The BCM43241 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

MAC Description

The BCM43241 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 34 on page 79.

The following sections provide an overview of the important modules in the MAC.

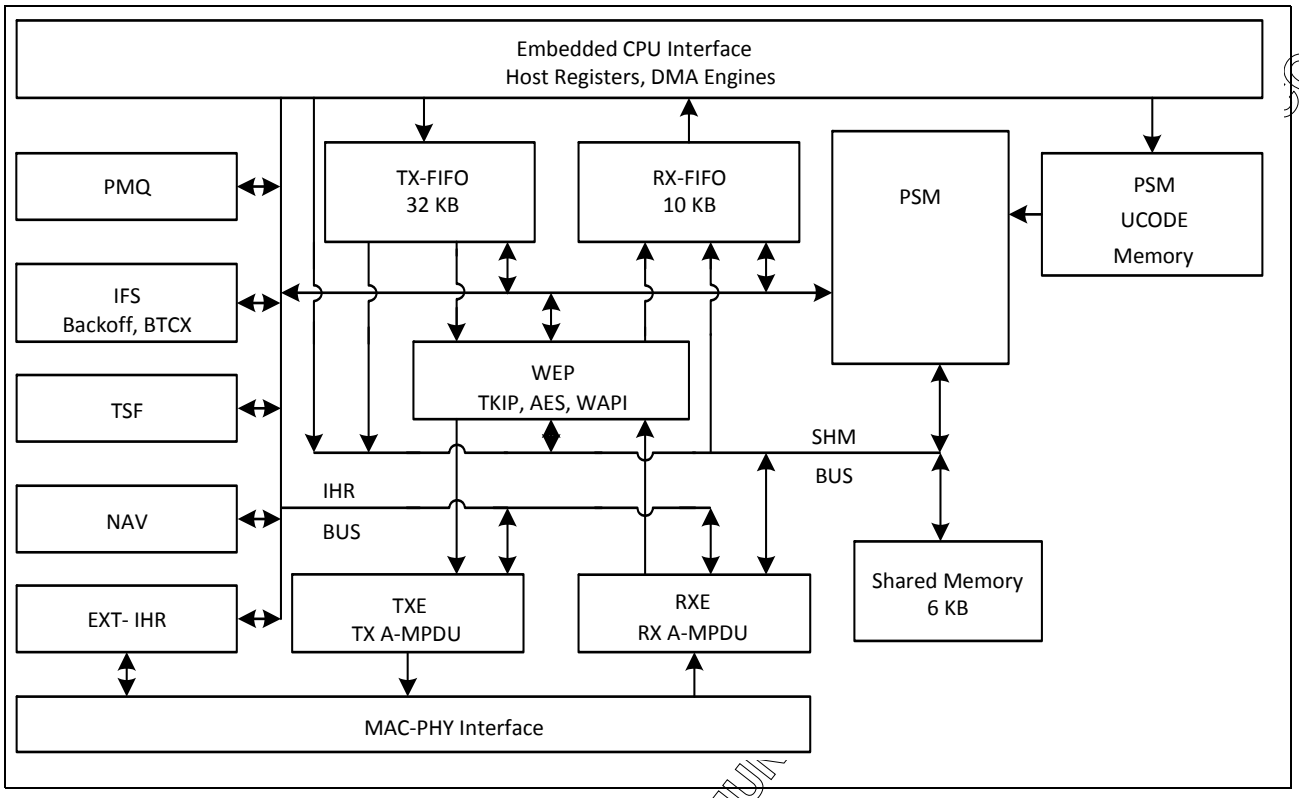


Figure 34: WLAN MAC Architecture

PSM

The programmable state machine (PSM) is a microcoded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are colocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface, which can be controlled either by the host or by the PSM to configure and control the PHY.

WLAN PHY Description

The BCM43241 supports IEEE 802.11a/b/g/n dual-stream to provide maximum data rates up to 300 Mbps.

The PHY has been designed to work with interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous Rx-Rx.

PHY Features

- Supports IEEE 802.11a, 11b, 11g, and 11n dual-stream PHY standards
- IEEE 802.11n dual-stream operation in 20 MHz and 40 MHz channels
- Supports Optional Short GI and Green Field modes in Tx and Rx
- Supports optional space-time block code (STBC) receive of two space-time streams
- Supports IEEE 802.11h/k for worldwide operation
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Supports power saving schemes such as single-core listen (OCL), single-core demodulation of SISO/STBC packets based on RSSI, and dynamic ML turn-off based on RSSI
- Algorithms to improve performance in presence of Bluetooth
- Simultaneous Rx-Rx (WL-BT) architecture
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications
- Closed-loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet Rx antenna diversity
- Designed to meet FCC and other worldwide regulatory requirements
- Tx LDPC for improved range and power efficiency
- Hardware support for faster switch times between channels/bands

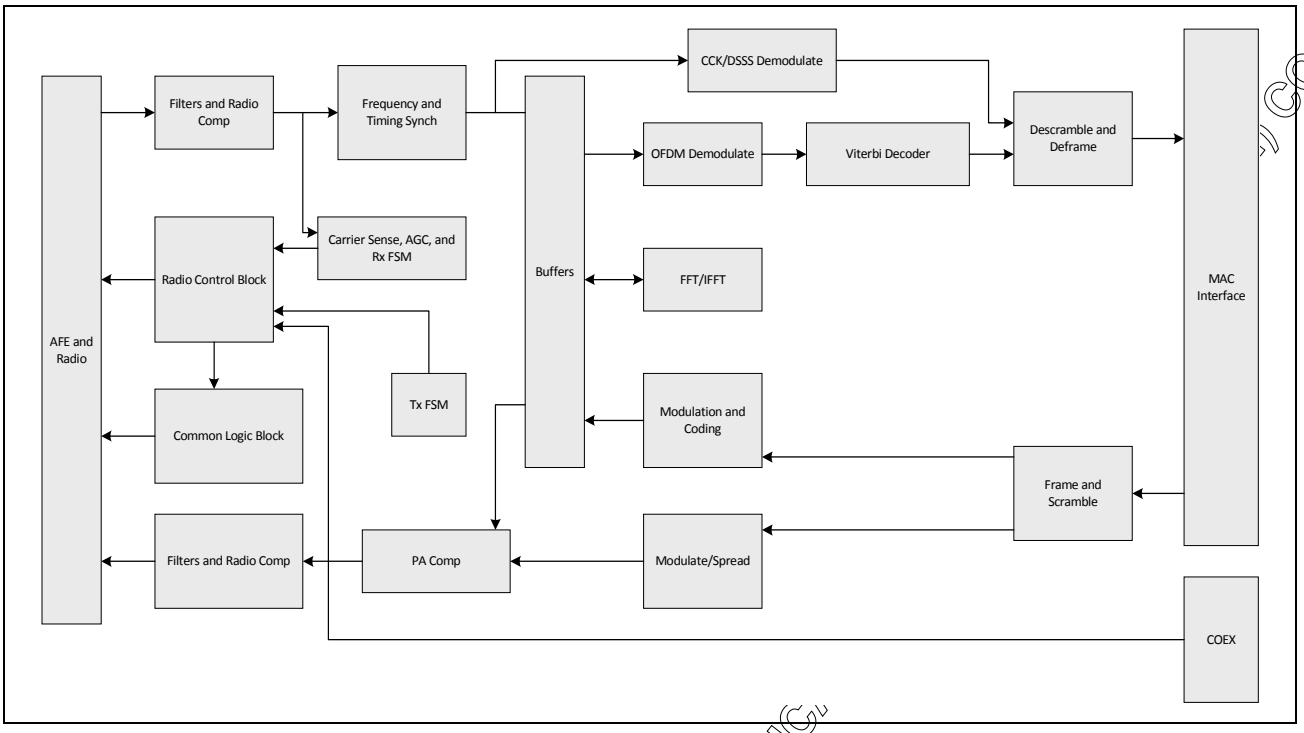


Figure 35: WLAN PHY Block Diagram

The PHY is capable of fully calibrating the RF front end to extract the highest performance. On power-up, the PHY performs a full suite of calibration to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift thus maintaining high-performance over time. A closed loop transmit control algorithm maintains the output power to required level with capability control Tx power on a per packet basis.

One of the key feature of the PHY is two space-time stream receive capability. The STBC scheme can obtain diversity gains by using multiple transmit antennas in AP (Access Point) in a fading channel environment, without increasing the complexity at the STA. Details of the STBC receive are shown in the block diagram in Figure 36 on page 84.

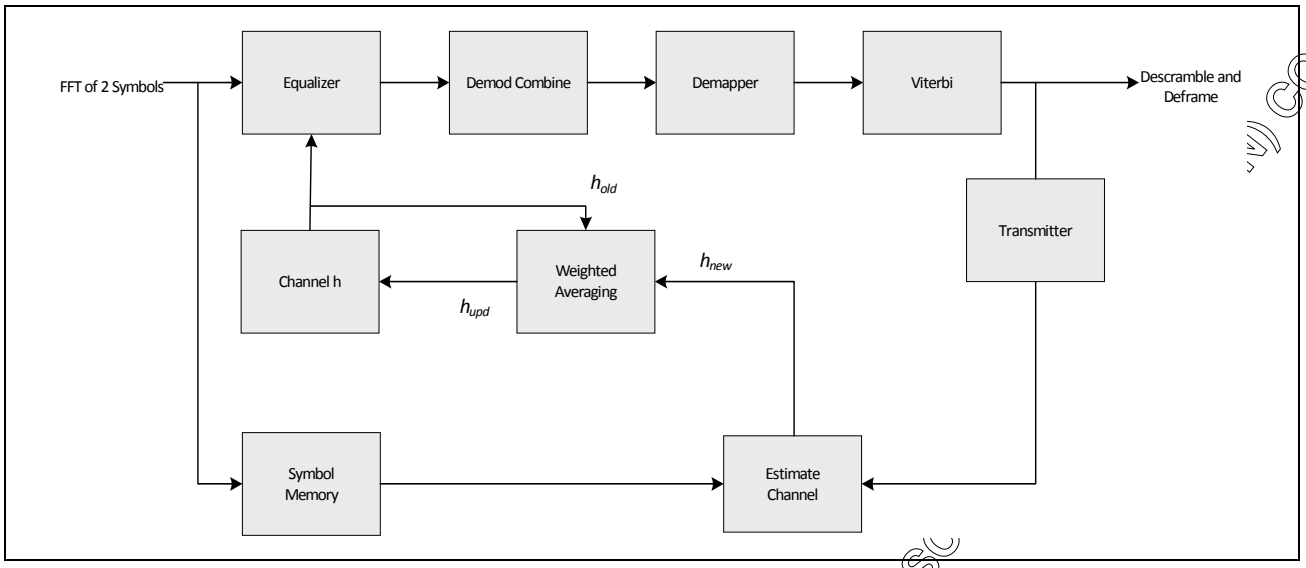


Figure 36: STBC Receive Block Diagram

In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. Channel estimate is refined on every pair of symbols using the received symbols and reconstructed symbols.

Section 13: WLAN Radio Subsystem

The BCM43241 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems (but not both simultaneously). It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Up to 11 RF control signals are available to drive the external RF switches and support external power amplifiers and low noise amplifiers for each band. See the reference board schematics for further details.

Receiver Path

The BCM43241 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. Control signals are available that can support the use of optional external low noise amplifiers (LNA), which can increase the receive sensitivity by several dB.

Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively.

Linear on-chip Power Amplifiers (PA) are included for both 2.4 GHz and 5GHz. Closed loop power control is also provided, as are spare RF control signals that can be used to support external RF switches for either or both bands.

Calibration

The BCM43241 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variation across components. This enables the BCM43241 to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip.

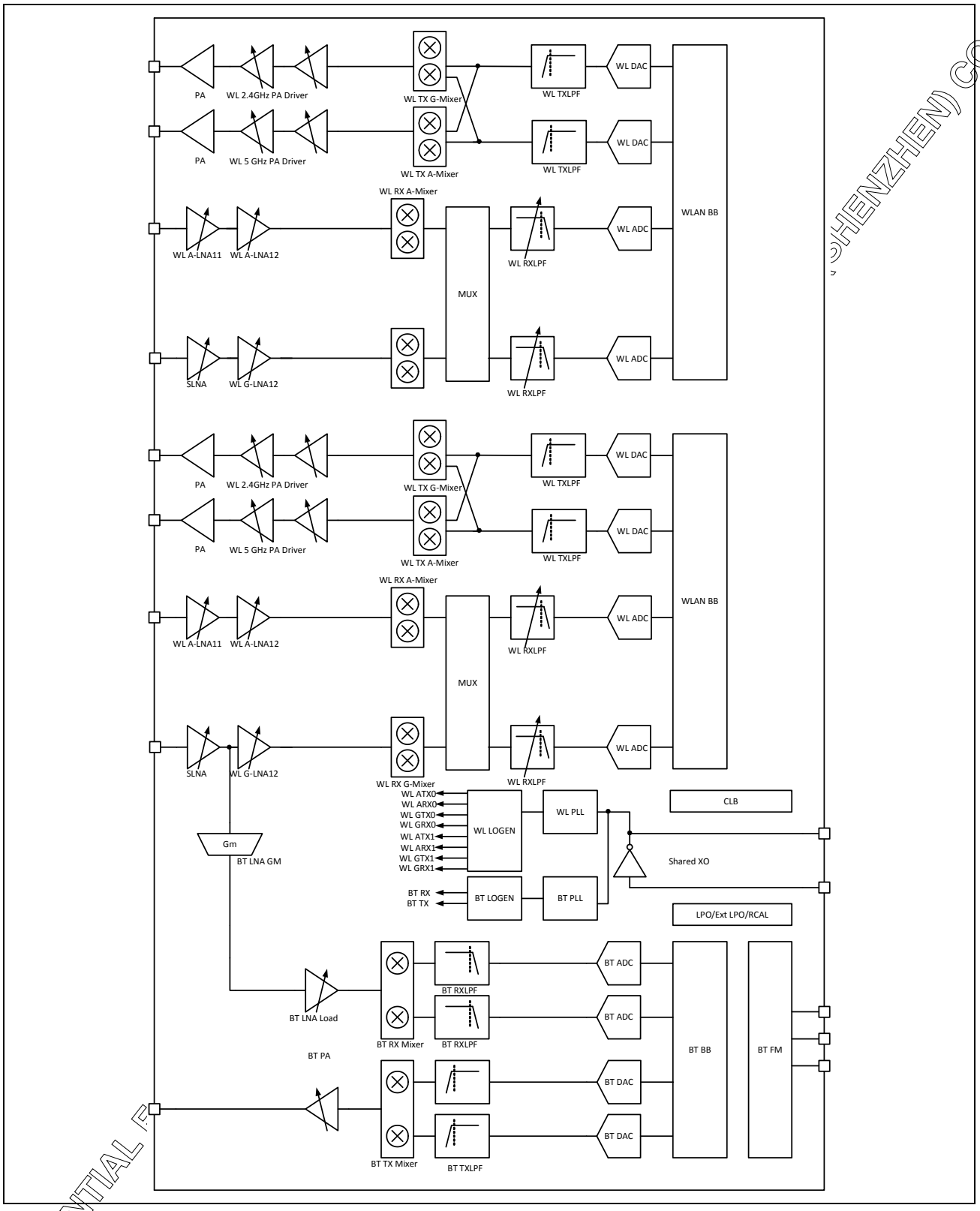


Figure 37: Radio Functional Block Diagram

Section 14: Pinout and Signal Descriptions

Signal Assignments

Figure 38 on page 88 shows the FCFBGA ball map. Figure 39 on page 89 shows the WLCSP bump map. For pin lists by pin/bump name and number, refer to Section 26: "Pin List," on page 179.

Table 17 on page 90 contains the WLCSP bump coordinates.

Table 18 on page 99 contains the signal description for all packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	BT_UART_TXD	BT_LPO_IN	BT_PCM_CLK	BT_PCM_OUT	RF_SW_CTRL_7	RF_SW_CTRL_5	RF_SW_CTRL_1	GMODE_EXT_LNA_PU_CORE0	GMODE_PA_EN_CORE0	GPIO_7	GPIO_6	GPIO_3	GPIO_0	GPIO_1	SR_VLX	SR_VLX	A
B	BT_UART_RXD	BT_GPIO_4	BT_I2S_WS	BT_GPIO_3	BT_PCM_IN	RF_SW_CTRL_6	RF_SW_CTRL_3	AMODE_PA_EN_CORE0	GPIO_13	GPIO_8	GPIO_2	JTAG_SEL	EXT_XTAL_PU	SR_PVSS	SR_PVSS	SR_PVSS	B
C	BT_I2S_CLK	BT_UART_RTS_N													SR_VDDBATP5V	SR_VDDBATP5V	C
D	BT_I2S_DO	BT_VDDC_ISO_2		BT_PCM_SYNC	BT_GPIO_2	RF_SW_CTRL_4	RF_SW_CTRL_0	RF_SW_CTRL_2	GPIO_12	AMODE_EXT_LNA_PU_CORE0	GPIO_11	GPIO_5	PMU_AVSS		SR_VDDBATA5V	SR_VDDBATA5V	D
E	BT_CLK_REQ	BT_I2S_DI		BT_VDDC_ISO_1							GPIO_9		VOUT_LDO3P3		VOUT_CLDO	VOUT_CLDO	E
F	BT_HOST_WAKE	BT_UART_CTS_N		BT_VDDO	BT_VDDC	BT_VDDC				GPIO_4					VOUT_LNLDO1	VOUT_LNLDO1	F
G	BT_TM1	BT_DEV_WAKE													LDO_VDD1P5	LDO_VDD1P5	G
H	FM_VCOVDD	BTFM_RGND		BT_GPIO_5		BT_VDDC	VSS	VDD					VOUT_LNLDO2		VOUT_HSICAVDD	HSIC_STROBE	H
J	FM_LNAVDD	BTFM_RGND		FM_PLLVDD		VSS		VDDIO_RF		VSS			WLREG_ON		HSIC_RREFHSIC	HSIC_DATA	J
K	FM_RFIN	FM_RFAUX		BTFM_RGND			VDD	VDD			VDDIO		BTREG_ON		HSIC_DVDD1p2	SDIO_DATA_2	K
L	BT_VCOVDD	BTFM_RGND		BTFM_RGND		VSS	GPIO_10			OTP_VDD33			VSS		SDIO_DATA_1	SDIO_DATA_3	L
M	BT_LNAVDD	BTFM_RGND		BT_PLLVDD		GPIO_15			VSS	VDD	VDDIO_RF	VDDIO_SD	HSIC_AGND12PLL		SDIO_DATA_0	SDIO_CLK	M
N	BT_RF	BTFM_RGND		BTFM_RGND		GPIO_14		VDD					RF_SW_CTRL_9		RF_SW_CTRL_11	SDIO_CMD	N
P	BT_PAVDD	BT_VBAT		BT_IFVDD		VSS		VDD	VSS	VDD	RF_SW_CTRL_8	PALDO_PU	GMODE_EXT_LNA_PU_CORE1		AMODE_EXT_LNA_PU_CORE1	RF_SW_CTRL_10	P
R	WRF_RFIN_2G_CORE0	RGND		RGND		VSS					GMODE_PA_EN_CORE1		AMODE_PA_EN_CORE1		VSS	AVDD_BBPLL	R
T	RGND	WRF_RX2G_VDD1P2_CORE0		WRF_PADRV2G_VDD3P3_CORE0		RGND	RGND	RGND	VSS	RGND					WRF_XTAL_CAB_GND1P2	WRF_TCXO_CKIN2V	T
U	WRF_PAOUT_2G_CORE0	RGND		RGND						WRF_AFE_VDD1P2_CORE1			WRF_TCXO_VDD1P8		WRF_XTAL_CAB_GND1P2	WRF_XTAL_CAB_XON	U
V	WRF_PA_VDD3P3_CORE0	RGND			WRF_PADRV5G_VDD3P3_CORE0	RGND	WRF_AFE_VDD1P2_CORE0	RGND	RGND	RGND	RGND		WRF_PADRV5G_VDD3P3_CORE1		WRF_XTAL_CAB_VDD1P2	WRF_XTAL_CAB_XOP	V
W	WRF_PAOUT_5G_CORE0	RGND													RGND	RGND	W
Y	RGND		RGND	RGND	RGND	WRF_TX_VDD1P2_CORE0	WRF_GPIO_OUT	WRF_TX_VDD1P2_CORE1	RGND	RGND	WRF_PADRV2G_VDD3P3_CORE1	RGND	RGND	RGND	RGND	WRF_RX5G_VDD1P2_CORE1	Y
AA	WRF_RFIN_5G_CORE0	RGND	WRF_RX5G_VDD1P2_CORE0	RGND	WRF_SYNTH_VDD1P2	RGND	WRF_VCO_VDD1P2	WRF_RX2G_VDD1P2_CORE1	WRF_RFIN_2G_CORE1	RGND	WRF_PAOUT_2G_CORE1	WRF_PA_VDD3P3_CORE1	WRF_PAOUT_5G_CORE1	RGND	WRF_RFIN_5G_CORE1	RGND	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 38: 208-Ball FCFBGA Ball Map (Top View)

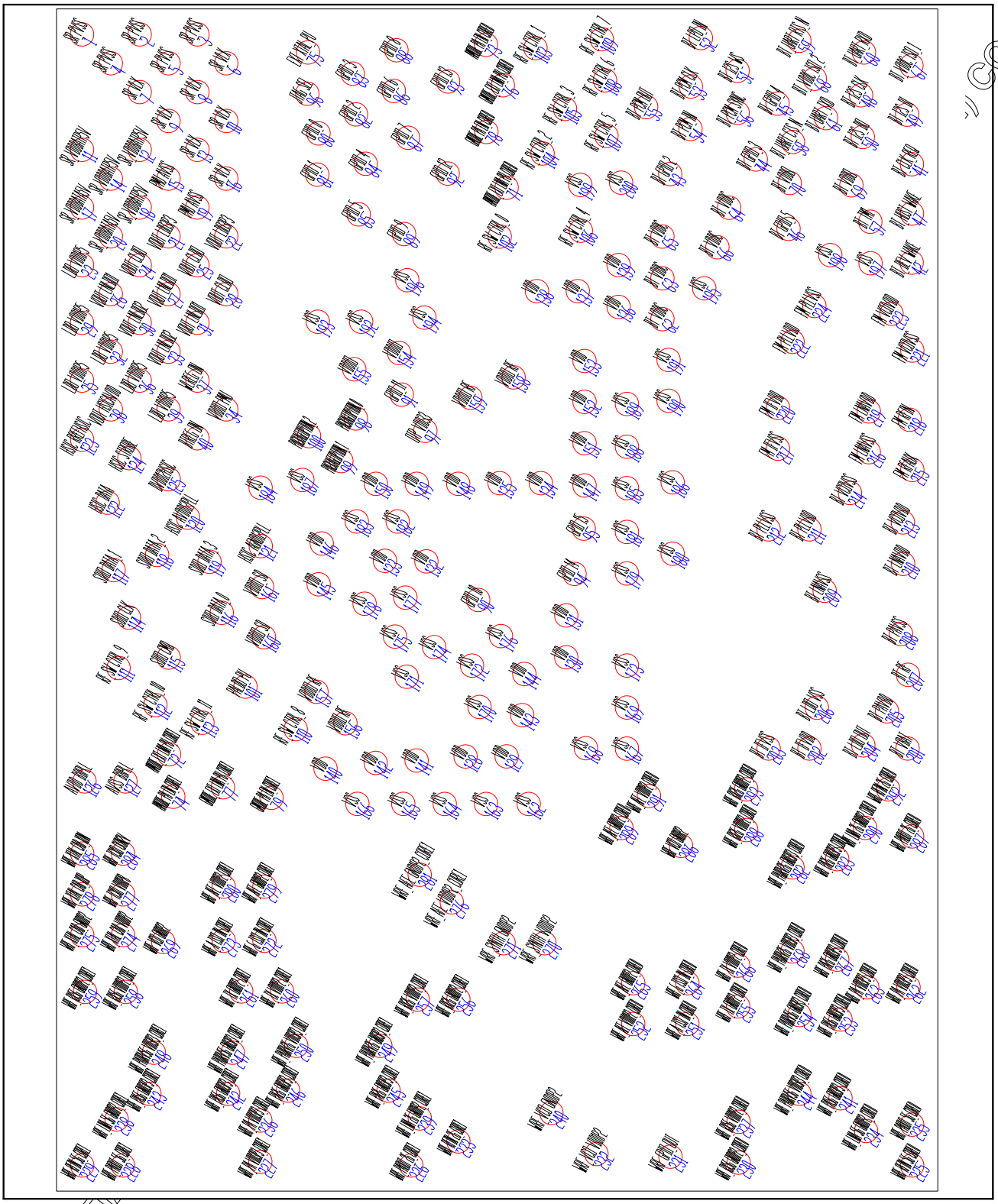


Figure 39: 293-Bump WLCSP Bump Map (Bottom View)

Table 17: WLCSP 293-Bump Coordinates

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
1	SR_PVSS	–2773.008	2035.008	2773.008	2035.008
2	SR_PVSS	–2773.008	1752.165	2773.008	1752.165
3	SR_PVSS	–2773.008	1469.322	2773.008	1469.322
4	SR_PVSS	–2631.5865	1893.5865	2631.5865	1893.5865
5	SR_PVSS	–2631.5865	1610.7435	2631.5865	1610.7435
6	SR_VLX	–2631.5865	1327.9005	2631.5865	1327.9005
7	SR_VLX	–2490.165	1752.165	2490.165	1752.165
8	SR_VLX	–2490.165	1469.322	2490.165	1469.322
9	SR_VLX	–2348.7435	1610.7435	2348.7435	1610.7435
10	SR_VLX	–2348.7435	1327.9005	2348.7435	1327.9005
11	SR_VDDBATP5V	–2207.322	2035.008	2207.322	2035.008
12	SR_VDDBATP5V	–2207.322	1752.165	2207.322	1752.165
13	SR_VLX	–2207.322	1469.322	2207.322	1469.322
14	SR_VDDBATP5V	–2065.9005	1893.5865	2065.9005	1893.5865
15	PMU_AVSS	–2065.9005	1610.7435	2065.9005	1610.7435
16	SR_VLX	–2065.9005	1327.9005	2065.9005	1327.9005
17	SR_VDDBATA5V	–1924.479	2035.008	1924.479	2035.008
18	SR_VDDBATP5V	–1924.479	1752.165	1924.479	1752.165
19	PMU_AVSS	–1924.479	1469.322	1924.479	1469.322
20	SR_VDDBATA5V	–1783.0575	1893.5865	1783.0575	1893.5865
21	VOUT_LDO3P3	–1783.0575	1610.7435	1783.0575	1610.7435
22	VOUT_LDO3P3	–1783.0575	1327.9005	1783.0575	1327.9005
23	LDO_VDD1P5	–1641.636	2035.008	1641.636	2035.008
24	VOUT_CLDO	–1641.636	1752.165	1641.636	1752.165
25	VOUT_CLDO	–1641.636	1469.322	1641.636	1469.322
26	VOUT_LNLDO1	–1500.2145	1893.5865	1500.2145	1893.5865
27	VOUT_LNLDO1	–1500.2145	1610.7435	1500.2145	1610.7435
28	VOUT_CLDO	–1500.2145	1327.9005	1500.2145	1327.9005
29	LDO_VDD1P5	–1358.793	2035.008	1358.793	2035.008
30	VOUT_LNLDO2	–1358.793	1752.165	1358.793	1752.165
31	VOUT_LNLDO1	–1358.793	1469.322	1358.793	1469.322
32	LDO_VDD1P5	–1217.3715	1893.5865	1217.3715	1893.5865
33	VOUT_LNLDO2	–1217.3715	1610.7435	1217.3715	1610.7435

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
34	VDDIO_PMU	–934.5285	1327.9005	934.5285	1327.9005
35	LDO_VDD1P5	–1075.95	2035.008	1075.95	2035.008
36	LDO_VDD1P5	–1075.95	1752.165	1075.95	1752.165
37	WLREG_ON	–1075.95	1469.322	1075.95	1469.322
38	VOUT_HSICAVDD	–934.5285	1893.5865	934.5285	1893.5865
39	LDO_VDD1P5	–934.5285	1610.7435	934.5285	1610.7435
40	BTREG_ON	–793.11	1469.32	793.11	1469.32
41	BT_CLK_REQ	–2136.55	–2032.84	2136.55	–2032.84
42	BT_DEV_WAKE	–1654.26	–2031.52	1654.26	–2031.52
43	BT_GPIO_2	–2088.42	–848.25	2088.42	–848.25
44	BT_GPIO_3	–2160.16	–1267.4	2160.16	–1267.4
45	BT_GPIO_4	–2433.61	–1373.91	2433.61	–1373.91
46	BT_GPIO_5	–1819.67	–1428.15	1819.67	–1428.15
47	BT_HOST_WAKE	–1894.88	–2032.96	1894.88	–2032.96
48	BT_I2S_CLK	–2474.78	–1783.81	2474.78	–1783.81
49	BT_I2S_DI	–2379.64	–2009.44	2379.64	–2009.44
50	BT_I2S_DO	–2270.29	–1792.11	2270.29	–1792.11
51	BT_I2S_WS	–2594.45	–1178.34	2594.45	–1178.34
52	BT_LPO_IN	–2755.26	–998.45	2755.26	–998.45
53	BT_PCM_CLK	–2517.61	–949.34	2517.61	–949.34
54	BT_PCM_IN	–2309.29	–947.65	2309.29	–947.65
55	BT_PCM_OUT	–2416.79	–730.5	2416.79	–730.5
56	BT_PCM_SYNC	–2388.11	–1178.63	2388.11	–1178.63
57	BT_TM1	–1854.63	–1829.16	1854.63	–1829.16
58	BT_UART_CTS_N	–2245.81	–1449.55	2245.81	–1449.55
59	BT_UART_RTS_N	–2742.18	–1481.2	2742.18	–1481.2
60	BT_UART_RXD	–2684.35	–1797.75	2684.35	–1797.75
61	BT_UART_TXD	–2362.87	–1612.63	2362.87	–1612.63
62	BT_VDDC	–1377	–810	1377	–810
63	BT_VDDC	–1577	–810	1577	–810
64	BT_VDDC	–1923.31	–1136.97	1923.31	–1136.97
65	BT_VDDC	–1782	–810	1782	–810
66	BT_VDDC	–1729.55	–1079.45	1729.55	–1079.45
67	BT_VDDC_ISO_1	–2619.66	–2030.58	2619.66	–2030.58

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
68	BT_VDDC_ISO_2	–2556.08	–1557	2556.08	–1557
69	BT_VDDO	–2033.19	–1736.4	2033.19	–1736.4
70	BT_VDDO	–2044.69	–1433.94	2044.69	–1433.94
71	AMODE_EXT_LNA_PU_CORE0	–2021.62	–46.37	2021.62	–46.37
72	AMODE_EXT_LNA_PU_CORE1	756.24	1608.26	–756.24	1608.26
73	AMODE_PA_EN_CORE0	–2722.37	54.68	2722.37	54.68
74	AMODE_PA_EN_CORE1	964.45	1587.37	–964.45	1587.37
75	EXT_XTAL_PU	–2684.66	927.19	2684.66	927.19
76	GMODE_EXT_LNA_PU_CORE0	–2523.47	–27.89	2523.47	–27.89
77	GMODE_EXT_LNA_PU_CORE1	918.25	1344.17	–918.25	1344.17
78	GMODE_PA_EN_CORE0	–2294.91	52.45	2294.91	52.45
79	GMODE_PA_EN_CORE1	969.92	1106.23	–969.92	1106.23
80	GPIO_0	–2287.81	875.59	2287.81	875.59
81	GPIO_1	–2085.92	882.04	2085.92	882.04
82	GPIO_2	–2380.9	691.65	2380.9	691.65
83	GPIO_3	–2580.59	708.26	2580.59	708.26
84	GPIO_4	–2138.91	644.56	2138.91	644.56
85	GPIO_5	–1890.86	678.61	1890.86	678.61
86	GPIO_6	–2495.73	506.56	2495.73	506.56
87	GPIO_7	–2266.62	436.96	2266.62	436.96
88	GPIO_8	–2695.34	493.43	2695.34	493.43
89	GPIO_9	–1794.26	456.06	1794.26	456.06
90	GPIO_10	–0.37	93.08	0.37	93.08
91	GPIO_11	–1007.07	467.95	1007.07	467.95
92	GPIO_12	–2090.92	242.8	2090.92	242.8
93	GPIO_13	–2542.12	240.25	2542.12	240.25
94	GPIO_14	–128.1	–379.23	128.1	–379.23
95	GPIO_15	–349.77	–424.28	349.77	–424.28
96	JTAG_SEL	–2482.21	930.68	2482.21	930.68
97	OTP_VDD33	–829.64	352.06	829.64	352.06
98	PACKAGEOPTION_0	–889.99	692.47	889.99	692.47
99	PACKAGEOPTION_1	–681	763.57	681	763.57
100	PACKAGEOPTION_2	–803.63	922.09	803.63	922.09
101	PALDO_PU	424.57	1233.75	–424.57	1233.75

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
102	RF_SW_CTRL_0	–1781.81	–12.4	1781.81	–12.4
103	RF_SW_CTRL_1	–2705.65	–187.82	2705.65	–187.82
104	RF_SW_CTRL_2	–2189.37	–222.29	2189.37	–222.29
105	RF_SW_CTRL_3	–2407.59	–332.55	2407.59	–332.55
106	RF_SW_CTRL_4	–1810.8	–410.12	1810.8	–410.12
107	RF_SW_CTRL_5	–2275.64	–535.8	2275.64	–535.8
108	RF_SW_CTRL_6	–2548.05	–528.65	2548.05	–528.65
109	RF_SW_CTRL_7	–2749.38	–512.75	2749.38	–512.75
110	RF_SW_CTRL_8	633.15	987.34	–633.15	987.34
111	RF_SW_CTRL_9	333.15	1855.94	–333.15	1855.94
112	RF_SW_CTRL_10	515.32	1675.19	–515.32	1675.19
113	RF_SW_CTRL_11	601.47	1444.78	–601.47	1444.78
114	SDIO_CLK	86.08	1805.07	–86.08	1805.07
115	SDIO_CMD	282.14	1610.22	–282.14	1610.22
116	SDIO_DATA_0	62.83	1349.84	–62.83	1349.84
117	SDIO_DATA_1	–146.47	1880.3	146.47	1880.3
118	SDIO_DATA_2	–220.8	1666.85	220.8	1666.85
119	SDIO_DATA_3	–187.54	1409.94	187.54	1409.94
120	HSIC_AVDD12PLL	–403.96	1515.31	403.96	1515.31
121	HSIC_AGND12PLL	–263.96	1158.7	263.96	1158.7
122	HSIC_DATA	–477.33	1909.13	477.33	1909.13
123	HSIC_RREFHSIC	–786.18	2034.4	786.18	2034.4
124	HSIC_STROBE	–695.4	1802.88	695.4	1802.88
125	DVDD12HSIC	–592	1610	592	1610
126	AVDD_BBPLL	889.51	2022.77	–889.51	2022.77
127	AVSS_BBPLL	889.51	1822.07	–889.51	1822.07
128	VDD	767.23	155.15	–767.23	155.15
129	VDD	766.6	–46.48	–766.6	–46.48
130	VDD	280.84	–338.69	–280.84	–338.69
131	VDD	75.82	–338.69	–75.82	–338.69
132	VDD	–189.52	346.84	189.52	346.84
133	VDD	–192	550	192	550
134	VDD	–573.05	–213.91	573.05	–213.91
135	VDD	–573.05	–11.99	573.05	–11.99

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
136	VDD	–1437	–595	1437	–595
137	VDD	–1514	–395	1514	–395
138	VDD	–1514	–195	1514	–195
139	VDD	–1642	–595	1642	–595
140	VDD	826.69	841.24	–826.69	841.24
141	VDD	786.69	394.94	–786.69	394.94
142	VDD	798.69	595.65	–798.69	595.65
143	VDD	564.54	–122.92	–564.54	–122.92
144	VDD	362.32	–132.92	–362.32	–132.92
145	VDD	–77	875	77	875
146	VDD	–277	860	277	860
147	VDD	–561.67	–428.15	561.67	–428.15
148	VDD	–569.84	190.95	569.84	190.95
149	VDD	–569.84	394.12	569.84	394.12
150	VDD	–569.84	594.13	569.84	594.13
151	VDD	–768.83	–428.15	768.83	–428.15
152	VDD	–971.7	–428.15	971.7	–428.15
153	VDD	–1172	–428.15	1172	–428.15
154	VDDIO	–1210.96	480.41	1210.96	480.41
155	VDDIO	–1130.96	700.28	1130.96	700.28
156	VDDIO_RF	604.27	743.97	–604.27	743.97
157	VDDIO_RF	449.59	885.76	–449.59	885.76
158	VDDIO_RF	–1091.53	–80.36	1091.53	–80.36
159	VDDIO_RF	–991.53	131.16	991.53	131.16
160	VDDIO_SD	182.23	1142.93	–182.23	1142.93
161	VDDIO_SD	–63.58	1152	63.58	1152
162	VSS	999.84	–154.67	–999.84	–154.67
163	VSS	999.84	54.25	–999.84	54.25
164	VSS	999.84	257.12	–999.84	257.12
165	VSS	999.43	460.38	–999.43	460.38
166	VSS	999.43	685.13	–999.43	685.13
167	VSS	728.5	–636.15	–728.5	–636.15
168	VSS	726.59	–434.92	–726.59	–434.92
169	VSS	527.11	–636.15	–527.11	–636.15

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
170	VSS	524.36	86.29	–524.36	86.29
171	VSS	376	443.09	–376	443.09
172	VSS	321.71	123.17	–321.71	123.17
173	VSS	321.04	–636.15	–321.04	–636.15
174	VSS	230.71	308.68	–230.71	308.68
175	VSS	179	500.71	–179	500.71
176	VSS	176.78	–18.64	–176.78	–18.64
177	VSS	–12	450	12	450
178	VSS	18	650	–18	650
179	VSS	–130.08	–636.15	130.08	–636.15
180	VSS	–227	–860	227	–860
181	VSS	–333.61	–636.15	333.61	–636.15
182	VSS	–384.89	487.85	384.89	487.85
183	VSS	–384.89	688.17	384.89	688.17
184	VSS	–550.68	1159.49	550.68	1159.49
185	VSS	–548.46	–636.15	548.46	–636.15
186	VSS	–577	–860	577	–860
187	VSS	–588.45	954.59	588.45	954.59
188	VSS	–751.65	–636.15	751.65	–636.15
189	VSS	–961.03	–636.15	961.03	–636.15
190	VSS	–977	–840	977	–840
191	VSS	–1177	–840	1177	–840
192	VSS	–1364.5	666.71	1364.5	666.71
193	VSS	–1364.5	879.01	1364.5	879.01
194	VSS	–1384.5	356.57	1384.5	356.57
195	VSS	–1527.95	–1015.11	1527.95	–1015.11
196	VSS	–1568.04	440.62	1568.04	440.62
197	VSS	–1651.28	–1830.05	1651.28	–1830.05
198	VSS	–1691.28	–1632.78	1691.28	–1632.78
199	VSS	–2035.34	–407.56	2035.34	–407.56
200	VSS	–2046.09	–607.22	2046.09	–607.22
201	BT_VBAT	728.001	–2011.6575	–728.001	–2011.6575
202	BT_IFVDD	728.001	–1530.414	–728.001	–1530.414
203	BT_IFVSS	728.001	–1330.416	–728.001	–1330.416

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
204	BT_LDO_OUT	712.5795	–1794.87	–712.5795	–1794.87
205	BT_PAVDD	546.1155	–1910.9745	–546.1155	–1910.9745
206	BT_PALDO_VSS	528.003	–1566.9	–528.003	–1566.9
207	BT_RF	366.471	–2013.894	–366.471	–2013.894
208	BT_PAVSS	166.473	–1979.4465	–166.473	–1979.4465
209	BT_LNAVSS	–45.207	–1605.096	45.207	–1605.096
210	BT_LNAVDD	–177.3045	–1989.6795	177.3045	–1989.6795
211	BT_PLLVDD	–346.4775	–1530.414	346.4775	–1530.414
212	BT_PLLVSS	–346.4775	–1330.416	346.4775	–1330.416
213	BT_VCOVDD	–380.376	–1988.505	380.376	–1988.505
214	BT_VCOVSS	–524.619	–1729.116	524.619	–1729.116
215	FM_RFAUX	–637.488	–2034.9	637.488	–2034.9
216	FM_LNAVSS	–724.617	–1821.519	724.617	–1821.519
217	FM_IFVSS	–741.8205	–1376.451	741.8205	–1376.451
218	FM_RFIN	–883.71	–2021.517	883.71	–2021.517
219	FM_LNAVDD	–924.615	–1821.519	924.615	–1821.519
220	FM_IFVDD	–941.8185	–1376.451	941.8185	–1376.451
221	FM_VCOVSS	–1223.3565	–2034.9	1223.3565	–2034.9
222	FM_PLLVDD	–1265.8905	–1447.8975	1265.8905	–1447.8975
223	FM_VCOVDD	–1404.045	–1933.0245	1404.045	–1933.0245
224	FM_PLLVSS	–1441.638	–1554.714	1441.638	–1554.714
225	WRF_RFIN_5G_CORE0	2772	–2034	–2772	–2034
226	WRF_PAOUT_2G_CORE1	2772	421.0155	–2772	421.0155
227	WRF_PA_VDD3P3_CORE1	2754.18	1160.793	–2754.18	1160.793
228	WRF_PAOUT_5G_CORE1	2772	1834.002	–2772	1834.002
229	WRF_RFIN_5G_CORE1	2772	2034	–2772	2034
230	WRF_RX5G_GND1P2_CORE0	2758.185	–1183.2615	–2758.185	–1183.2615
231	WRF_GPIO_OUT	2729.025	–849.3525	–2729.025	–849.3525
232	WRF_VCO_VDD1P2	2716.0875	–486.5805	–2716.0875	–486.5805
233	WRF_RFIN_2G_CORE1	2654.55	189.999	–2654.55	189.999
234	WRF_LNA_5G_GND1P2_CORE0	2603.187	–1808.2755	–2603.187	–1808.2755
235	WRF_PAOUT_5G_CORE0	2572.002	–2034	–2572.002	–2034
236	WRF_PA_VDD3P3_CORE1	2551.8555	1160.793	–2551.8555	1160.793
237	WRF_RX5G_VDD1P2_CORE0	2558.187	–1183.2615	–2558.187	–1183.2615

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
238	WRF_LNA_5G_GND1P2_CORE1	2546.2755	1865.187	–2546.2755	1865.187
239	WRF_LNA_2G_GND1P2_CORE1	2541.5955	379.3005	–2541.5955	379.3005
240	WRF_VCO_GND1P2	2514.843	–265.869	–2514.843	–265.869
241	WRF_PA5G_GND3P3_CORE0	2442.672	–1682.757	–2442.672	–1682.757
242	WRF_PA5G_GND3P3_CORE1	2420.757	1318.608	–2420.757	1318.608
243	WRF_PA5G_GND3P3_CORE1	2420.757	1704.672	–2420.757	1704.672
244	WRF_PADRV5G_VDD3P3_CORE0	2420.658	–1481.2155	–2420.658	–1481.2155
245	WRF_PA2G_GND3P3_CORE1	2404.9035	532.4805	–2404.9035	532.4805
246	WRF_PA2G_GND3P3_CORE1	2404.9035	1025.0145	–2404.9035	1025.0145
247	WRF_PADRV5G_GND3P3_CORE1	2219.2155	1296.477	–2219.2155	1296.477
248	WRF_PADRV5G_VDD3P3_CORE1	2219.2155	1682.658	–2219.2155	1682.658
249	WRF_PADRV2G_GND3P3_CORE1	2185.497	572.787	–2185.497	572.787
250	WRF_PADRV2G_VDD3P3_CORE1	2185.497	984.708	–2185.497	984.708
251	WRF_A_TSSI_IN_CORE0	2078.6895	–932.3685	–2078.6895	–932.3685
252	WRF_AFE_VDD1P2_CORE0	2078.6895	–666.9	–2078.6895	–666.9
253	WRF_PA5G_GND3P3_CORE0	2056.608	–1682.757	–2056.608	–1682.757
254	WRF_PADRV5G_GND3P3_CORE0	2034.477	–1481.2155	–2034.477	–1481.2155
255	WRF_TX_GND1P2_CORE0	1992.312	–1181.0655	–1992.312	–1181.0655
256	WRF_RX2G_GND1P2_CORE1	1958.823	189.999	–1958.823	189.999
257	WRF_RX2G_VDD1P2_CORE1	1958.823	389.997	–1958.823	389.997
258	WRF_RX5G_VDD1P2_CORE1	1921.2615	1820.187	–1921.2615	1820.187
259	WRF_RX5G_GND1P2_CORE1	1921.2615	2020.185	–1921.2615	2020.185
260	WRF_TX_VDD1P2_CORE1	1919.0655	1054.314	–1919.0655	1054.314
261	WRF_TX_GND1P2_CORE1	1919.0655	1254.312	–1919.0655	1254.312
262	WRF_PA_VDD3P3_CORE0	1898.793	–2016.18	–1898.793	–2016.18
263	WRF_PA_VDD3P3_CORE0	1898.793	–1813.8555	–1898.793	–1813.8555
264	WRF_G_TSSI_IN_CORE0	1878.6915	–932.3685	–1878.6915	–932.3685
265	WRF_AFE_GND1P2_CORE0	1878.6915	–666.9	–1878.6915	–666.9
266	WRF_TX_VDD1P2_CORE0	1792.314	–1181.0655	–1792.314	–1181.0655
267	WRF_PA2G_GND3P3_CORE0	1763.0145	–1666.9035	–1763.0145	–1666.9035
268	WRF_PADRV2G_VDD3P3_CORE0	1722.708	–1447.497	–1722.708	–1447.497
269	WRF_VCO_GND1P2	1676.394	1636.812	–1676.394	1636.812
270	WRF_SYNTH_VDD1P2	1682.532	–231.5745	–1682.532	–231.5745
271	WRF_SYNTH_GND1P2	1682.532	–31.5765	–1682.532	–31.5765

Table 17: WLCSP 293-Bump Coordinates (Cont.)

		Package Top-Side View Bump Facing Down (0,0 center of die)		Package Bottom-Side View Bump Facing Up (0,0 center of die)	
Bump #	**Net Name**	**X-Coordinate**	**Y-Coordinate**	**X-Coordinate**	**Y-Coordinate**
272	WRF_G_TSSI_IN_CORE1	1670.3685	1140.6915	–1670.3685	1140.6915
273	WRF_A_TSSI_IN_CORE1	1670.3685	1340.6895	–1670.3685	1340.6895
274	WRF_XTAL_CAB_VDD1P2	1642.995	1834.002	–1642.995	1834.002
275	WRF_XTAL_CAB_GND1P2	1642.995	2034	–1642.995	2034
276	WRF_AFE_VDD1P2_CORE1	1482.084	222.6015	–1482.084	222.6015
277	WRF_TCXO_VDD1P8	1442.997	1834.002	–1442.997	1834.002
278	WRF_XTAL_CAB_XOP	1442.997	2034	–1442.997	2034
279	WRF_AFE_GND1P2_CORE1	1404.9	1140.6915	–1404.9	1140.6915
280	WRF_AFE_VDD1P2_CORE1	1404.9	1340.6895	–1404.9	1340.6895
281	WRF_AFE_GND1P2_CORE1	1346.841	379.89	–1346.841	379.89
282	WRF_PADRV2G_GND3P3_CORE0	1310.787	–1447.497	–1310.787	–1447.497
283	WRF_PA2G_GND3P3_CORE0	1270.4805	–1666.9035	–1270.4805	–1666.9035
284	WRF_TCXO_CKIN2V	1242.999	1834.002	–1242.999	1834.002
285	WRF_XTAL_CAB_XON	1242.999	2034	–1242.999	2034
286	WRF_VCO_GND1P2	1205.37	–901.395	–1205.37	–901.395
287	WRF_PAOUT_2G_CORE0	1159.0155	–2034	–1159.0155	–2034
288	WRF_RX2G_VDD1P2_CORE0	1127.997	–1220.823	–1127.997	–1220.823
289	WRF_AFE_GND1P2_CORE0	1117.89	–608.841	–1117.89	–608.841
290	WRF_LNA_2G_GND1P2_CORE0	1117.3005	–1803.5955	–1117.3005	–1803.5955
291	WRF_AFE_VDD1P2_CORE0	960.6015	–744.084	–960.6015	–744.084
292	WRF_RFIN_2G_CORE0	927.999	–1916.55	–927.999	–1916.55
293	WRF_RX2G_GND1P2_CORE0	927.999	–1220.823	–927.999	–1220.823

Signal Descriptions

The signal name, type, and description of each pin in the BCM43241 are listed in Table 18. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any. See also Table 19 on page 109 for resistor strapping options.

Table 18: FCFBGA and WLCSP Signal Descriptions

Signal Name	*FCFBGA Ball#*	*WLCSP Bump#*	*Type*	*Description*
WLAN Radio				
AVDD_BBPLL	R16	126	I	Baseband PLL supply
AVSS_BBPLL	–	127	I	Baseband PLL ground
WRF_XTAL_CAB_XON	U16	285	O	XTAL output
WRF_XTAL_CAB_XOP	V16	278	I	XTAL input
WRF_A_TSSI_IN_CORE1	–	273	I	5G TSSI input core 1
WRF_G_TSSI_IN_CORE1	–	272	I	2.4G TSSI input core 1
WRF_RFIN_2G_CORE1	AA9	233	I	2.4G RF input core 1
WRF_RFIN_5G_CORE1	AA15	229	I	5G RF input core 1
WRF_GPIO_OUT	Y7	231	O	WLAN Radio GPIO
WRF_TCXO_CKIN2V	T16	284	I	TCXO buffered input. When not using a TCXO this pin should be connected to ground.
WRF_SYNTH_VDD1P2	AA5	270	I	Clock and miscellaneous supplies
WRF_TCXO_VDD1P8	U13	277		
WRF_VCO_VDD1P2	AA7	232		
WRF_XTAL_CAB_VDD1P2	V15	274		
WRF_XTAL_CAB_GND1P2	T15, U15	275	I	Clock and miscellaneous grounds
WRF_SYNTH_GND1P2	–	271		
WRF_AFE_VDD1P2_CORE1	U10	276, 280	I	WLAN core 1 radio supplies
WRF_PADRV2G_VDD3P3_CORE1	Y11	250		
WRF_PADRV5G_VDD3P3_CORE1	V13	248		
WRF_TX_VDD1P2_CORE1	Y8	260		
WRF_RX2G_VDD1P2_CORE1	AA8	257		
WRF_RX5G_VDD1P2_CORE1	Y16	258		

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	WLCSP Bump#	Type	Description
WRF_AFE_GND1P2_CORE1	–	279, 281	I	WLAN core 1 radio grounds
WRF_LNA_2G_GND1P2_CORE1	–	239		
WRF_LNA_5G_GND1P2_CORE1	–	238		
WRF_PADRV2G_GND3P3_CORE1	–	249		
WRF_PADRV5G_GND3P3_CORE1	–	247		
WRF_RX2G_GND1P2_CORE1	–	256		
WRF_RX5G_GND1P2_CORE1	–	259		
WRF_TX_GND1P2_CORE1	–	261		
WRF_VCO_GND1P2	–	240, 269, 286		
WRF_A_TSSI_IN_CORE0	–	251	I	5G TSSI input core 0
WRF_G_TSSI_IN_CORE0	–	264	I	2.4G TSSI input core 0
WRF_RFIN_2G_CORE0	R1	292	I	2.4G RF input core 0
WRF_RFIN_5G_CORE0	AA1	225	I	5G RF input core 0
WRF_PAOUT_2G_CORE0	U1	287	O	2.4 GHz RF output for Core 0
WRF_PAOUT_2G_CORE1	AA11	226	O	2.4 GHz RF output for Core 1
WRF_PAOUT_5G_CORE0	W1	235	O	5 GHz RF output for Core 0
WRF_PAOUT_5G_CORE1	AA13	228	O	5 GHz RF output for Core 1
WRF_AFE_VDD1P2_CORE0	V7	252, 291	I	WLAN core 0 radio supplies
WRF_PADRV2G_VDD3P3_CORE0	T4	268		
WRF_PADRV5G_VDD3P3_CORE0	V5	244		
WRF_TX_VDD1P2_CORE0	Y6	266		
WRF_RX2G_VDD1P2_CORE0	T2	288		
WRF_RX5G_VDD1P2_CORE0	AA3	237		
WRF_AFE_GND1P2_CORE0	–	265, 289	I	WLAN core 0 radio grounds
WRF_LNA_2G_GND1P2_CORE0	–	290		
WRF_LNA_5G_GND1P2_CORE0	–	234		
WRF_PADRV2G_GND3P3_CORE0	–	282		
WRF_PADRV5G_GND3P3_CORE0	–	254		
WRF_RX2G_GND1P2_CORE0	–	293		
WRF_RX5G_GND1P2_CORE0	–	230		
WRF_TX_GND1P2_CORE0	–	255		
WRF_PA_VDD3P3_CORE1	AA12	227, 236	I	WLAN PA Supplies (Core 1)
WRF_PA_VDD3P3_CORE0	V1	262, 263	I	WLAN PA Supplies (Core 0)
WRF_PA5G_GND3P3_CORE0	–	241, 253	I	WLAN 5 GHz PA Ground (Core 0)
WRF_PA5G_GND3P3_CORE1	–	242, 243	I	WLAN 5 GHz PA Ground (Core 1)

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	WLCSP Bump#	Type	Description
WRF_PA2G_GND3P3_CORE0	–	267, 283	I	WLAN 2.4 GHz PA Ground (Core 0)
WRF_PA2G_GND3P3_CORE1	–	245, 246	I	WLAN 2.4 GHz PA Ground (Core 1)
WLAN Digital				
HSIC_STROBE	H16	124	I/O	HSIC strobe
HSIC_DATA	J16	122	I/O	HSIC data
HSIC_RREFHSIC	J15	123	I	HSIC reference resistor input. If HSIC is used, connect this pin to ground via a 51-ohm 5% resistor.
HSIC_DVDD1P2	K15	–	I	HSIC Digital 1.2V supply
SDIO_DATA_3	L16	119	I/O	SDIO data lines
SDIO_DATA_2	K16	118		
SDIO_DATA_1	L15	117		
SDIO_DATA_0	M15	116		
SDIO_CLK	M16	114	I	SDIO clock
SDIO_CMD	N16	115		SDIO command
RF_SW_CTRL_0	D7	102	O	WLAN RF switch control outputs
RF_SW_CTRL_1	A7	103		
RF_SW_CTRL_2	D8	104		
RF_SW_CTRL_3	B7	105		
RF_SW_CTRL_4	D6	106		
RF_SW_CTRL_5	A6	107		
RF_SW_CTRL_6	B6	108		
RF_SW_CTRL_7	A5	109		
RF_SW_CTRL_8	P11	110		
RF_SW_CTRL_9	N13	111		
RF_SW_CTRL_10	P16	112		
RF_SW_CTRL_11	N15	113		
GMODE_EXT_LNA_PU_CORE0	A8	76	O	2.4G external LNA control core 0
AMODE_EXT_LNA_PU_CORE0	D10	71	O	5G external LNA control core 0
GMODE_PA_EN_CORE0	A9	78	O	2.4G external PA control core 0
AMODE_PA_EN_CORE0	B8	73	O	5G external PA control core 0
GMODE_EXT_LNA_PU_CORE1	P13	77	O	2.4G external LNA control core 1
AMODE_EXT_LNA_PU_CORE1	P15	72	O	5G external LNA control core 1
GMODE_PA_EN_CORE1	R11	79	O	2.4G external PA control core 1
AMODE_PA_EN_CORE1	R13	74	O	5G external PA control core 1

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	*FCFBGA Ball#*	*WLCSP Bump#*	*Type*	*Description*
GPIO_15/UART_TX	M6	95	I/O	The WLAN GPIO or UART Tx signal
GPIO_14/UART_RX	N6	94		The WLAN GPIO or UART Rx signal
GPIO_13	B9	93		WLAN GPIOs
GPIO_11	D11	91		
GPIO_10	L7	90		
GPIO_9	E11	89		
GPIO_8	B10	88		
GPIO_7	A10	87		
GPIO_12/ERCX_PRISEL	D9	92	I/O	This pin can be programmed to be a GPIO, the JTAG TRST_L signal, or the external coexistence ERCX_PRISEL output.
GPIO_6	A11	86	I/O	GPIO_6/SPI_MODE_SEL (Strap Option)
GPIO_5/TDO/ERCX_TXCONF	D12	85	I/O	This pin can be programmed to be a GPIO, the JTAG TDO signal, or the external coexistence ERCX_TXCONF signal.The ERCX_TXCONF pin is an output asserted when WLAN is requesting priority. It can be wire-ORed with BT_I2S_DO/ BT_RX_PRIORITY to create the WCN_PRIORITY signal for LTE coexistence.
GPIO_4/TDI/ERCX_RFACTIVE	F10	84	I/O	This pin can be programmed to be a GPIO, the JTAG TDI signal, or the external coexistence ERCX_RF_ACTIVE signal. The ERCX_RFACTIVE pin is an input that should be asserted by the external coexisting device when it is active. It can be connected with BT_I2S_WS/MWS_RX and then to the LTE modem LTE_PRIORITY signal for LTE coexistence.
GPIO_3/TMS/ERCX_FREQ	A12	83	I/O	This pin can be programmed to be a GPIO, the JTAG TMS signal, or the external coexistence ERCX_FREQ signal. The ERCX_FREQ is an input signal that can be connected with BT_I2S_CLK/MWS_TX to create the LTE TX signal for LTE coexistence.

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	*FCFBGA Ball#*	*WLCSP Bump#*	*Type*	*Description*
GPIO_2/TCK/ERCX_STATUS	B11	82	I/O	This pin can be programmed to be a GPIO, the JTAG TCK signal, the external coexistence ERCX_STATUS signal, or an HSIC_READY output to the host, indicating that the device is ready to respond with a CONNECT when it sees IDLE on the HSIC bus.ERCX_STATUS is an input for synchronization with an external coexisting device. It can be connected with BT_I2S_DI/ FRAME_SYNC and then to LTE modem LTE_FRAME_SYNC for LTE coexistence.
GPIO_1/WL_DEV_WAKE	A14	81	I/O	This pin can be programmed to be a GPIO or an AP_READY or HSIC_HOST_READY input from the host indicating that it is awake. This pin is also used as an out-of- band wake-up when the host wants to wake WLAN from the deep sleep mode.
GPIO_0/WL_HOST_WAKE	A13	80	I/O	This pin can be programmed to be a GPIO or a WLAN_HOST_WAKE output indicating that host wake-up should be performed.
JTAG_SEL	B12	96	I	JTAG select. The JTAG interface (multiplexed on the GPIO pins) is enabled when this pin is asserted high.
PALDO_PU	P12	101	O	External PA LDO/Switcher power-up signal
EXT_XTAL_PU	B13	75	O	External Xtal oscillator power-up signal
VDD	H8, K7, K8, M10, N8, P8, P10	128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153	I	Digital always-on core supply
OTP_VDD33	L10	97	I	3.3V OTP power supply

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	WLCSP Bump#	Type	Description
VDDIO	K11	154, 155	I	1.8V to 3.3V IO supply
VDDIO_SD	M12	160, 161	I	1.8 to 3.3V SDIO IO supply
VDDIO_RF	J8, M11	156, 157, 158, 159	I	3.3V RF control IO supply
VSS	H7, J6, J10, L6, L13, M9, P6, P9, R6, R15, T9	162, 163, 164, 165, 166, 167 168, 169, 170 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200	I	Core ground
DVDD12HSIC	–	125	I	1.2V supply for the HSIC PHY digital domain
HSIC_AGND12PLL	M13	121	I	Analog ground for HSIC PLL
HSIC_AVDD12PLL	–	120	I	1.2V analog supply for the HSIC PLL
PACKAGEOPTION_0	–	98	I	Connect to Ground
PACKAGEOPTION_1	–	99	I	Connect to Ground
PACKAGEOPTION_2	–	100	I	Connect to VDDIO
VOUT_HSICAVDD	H15	38	O	1.2V output of HSIC LDO, for HSIC PHY analog domain

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	WLCSP Bump#	Type	Description
RGND	R2, R4, T1, T6, T7, T8, T10, U2, U4, V2, V6, V8, V9, V10, V11, W2, W15, W16, Y1, Y3, Y4, Y5, Y9, Y10, Y12, Y13, Y14, Y15, AA2, AA4, AA6, AA10, AA14, AA16	–	I	WLAN Radio ground
Bluetooth-FM Radio				
BT_IFVSS	–	203	I	BT FM Radio ground
BT_LNAVSS	–	209		
BT_PALDO_VSS	–	206		
BT_PAVSS	–	208		
BT_PLLVSS	–	212		
BT_VCOVSS	–	214		
FM_IFVSS	–	217		
FM_PLLVSS	–	224		
FM_VCOVSS	–	221		
BT_IFVDD	P4	202	I	1.2V Bluetooth IF block power supply
BT_LDO_OUT	–	204	O	BT PA LDO output pin. 2.2 µF external capacitor to be connected to this pin
BT_LNAVDD	M1	210	I	1.2V Bluetooth LNA power supply
BT_LNAVSS	–	209	I	Bluetooth LNA ground
BT_PAVDD	P1	205	I	Bluetooth PA supply
BT_PLLVDD	M4	211	I	Bluetooth RF PLL power supply
BT_RF	N1	207	O	Bluetooth transceiver RF antenna port
BT_VBAT	P2	201	I	VBAT for Bluetooth
BT_VCOVDD	L1	213	I	Bluetooth VCO Supply
FM_IFVDD	–	220	I	FM IF power supply

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	WLCSP Bump#	Type	Description
FM_IFVSS	–	217	I	FM IF ground
FM_LNAVDD	J1	219	I	FM receiver power supply
FM_LNAVSS	–	216	I	FM receiver ground
FM_PLLVDD	J4	222	I	FM PLL power supply
FM_PLLVSS	–	224	I	FM PLL ground
FM_RFAUX	K2	215	I	FM radio auxiliary antenna port
FM_RFIN	K1	218	I	FM radio antenna port
FM_VCOVDD	H1	223	I	FM VCO supply
BTFM_RGND	H2, J2, K4, L2, L4, M2, N2, N4	–	I	BT/FM Radio ground
Bluetooth-FM Digital				
BT_TM1	G1	57	I/O	BT test mode pin
BT_DEV_WAKE	G2	42	I/O	BT device wake
BT_HOST_WAKE	F1	47	I/O	BT host wake
BT_GPIO_2	D5	43	I/O	BT GPIO
BT_GPIO_3	B4	44	I/O	BT GPIO
BT_GPIO_4	B2	45	I/O	BT GPIO
BT_GPIO_5	H4	46	I/O	BT GPIO
BT_UART_CTS_N	F2	58	I/O	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface
BT_UART_RTS_N	C2	59	I/O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface
BT_UART_TXD	A1	61	I/O	UART serial output. Serial data output for the HCI UART interface
BT_UART_RXD	B1	60	I/O	UART serial input. Serial data input for the HCI UART interface
BT_I2S_CLK	C1	48	I/O	I2S clock; can be master (output) or slave (input)
BT_I2S_DO	D1	50	I/O	I2S data output
BT_I2S_DI	E2	49	I/O	I2S data input
BT_I2S_WS	B3	51	I/O	I2S WS: can be master (output) or slave (input)
BT_PCM_IN	B5	54	I/O	PCM data input or SLIMbus transport sensing
BT_PCM_CLK	A3	53	I/O	PCM or SLIMbus clock; can be master (output) or slave (input)

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	*FCFBGA Ball#*	*WLCSP Bump#*	*Type*	*Description*
BT_PCM_SYNC	D4	56	I/O	PCM sync; can be master (output) or slave (input); or SLIMbus data
BT_PCM_OUT	A4	55	I/O	PCM data output
BT_CLK_REQ	E1	41	I/O	BT clock request
BT_LPO_IN	A2	52	I	External sleep clock input (32.758 kHz)
BT_VDDC	F5, F6, H6	62, 63, 64, 65, 66	I	BT digital core 1.2V supply
BT_VDDC_ISO_1	E4	67	I	Core supply for power-on/off island VDDC_G
BT_VDDC_ISO_2	D2	68	I	Core supply for power-on/off island VDDB
BT_VDDO	F4	69, 70	I	I/O supply for Bluetooth
PMU				
SR_PVSS	B14, B15, B16	1, 2, 3, 4, 5	I	Switcher ground
SR_VDDBATA5V	D15, D16	17, 20	I	Battery voltage input for band-gap and LDO3P3
SR_VDDBATP5V	C15, C16	11, 12, 14, 18	I	Battery voltage input for the CBUCK switcher
SR_VLX	A15, A16	6, 7, 8, 9, 10, 13, 16	O	Switcher output (1.35V default)
LDO_VDD1P5	G15, G16	23, 29, 32, 35, 36, 39	I	LDO input for CLDO, HSICLDO, LNLDO1, and LNLDO2. Also voltage feedback input for CBUCK. (1.35V default)
BTREG_ON	K13	40	I	Used by PMU to power up or power down the internal BCM43241 regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Table 18: FCFBGA and WLCSP Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	WLCSP Bump#	Type	Description
WLREG_ON	J13	37	I	Used by PMU to power up or power down the internal BCM43241 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
PMU_AVSS	D13	15, 19	I	PMU ground
VOUT_LDO3P3	E13	21, 22	O	3.3V LDO output
VOUT_LNLDO1	F15, F16	26, 27, 31	O	1.2V LNLDO1 output
VOUT_LNLDO2	H13	30, 33	O	1.2V LNLDO2 output
VOUT_CLDO	E15, E16	24, 25, 28	O	1.2V Digital core LDO output
VDDIO_PMU	–	34	I	PMU IO supply

WLAN GPIO Signals and Strapping Options

The pins listed in Table 19 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 19: WLAN GPIO Functions and Strapping Options (Advance Information)

Pin Name	FCFBGA Pin	WLCSP Pin #	Default	Function	Description
SDIO_DATA_1	L15	117	0	strap_host_ifc_1	The three strap pins strap_host_ifc_[3:1] together select the host interface to enable: 0XX: SDIO 10X: gSPI 110: normal HSIC 111: bootloader-less HSIC
SDIO_DATA_2	K16	118	0	strap_host_ifc_2	–
GPIO_6	A11	86	0	strap_host_ifc_3	–
GPIO_7	A10	87	1	OTPEnabled	When this bit is 0, OTP is not powered up by default, but SW can enable it by altering MInRsrcMask. This pin also selects the use of OTP or the default CIS in the SDIO core, as described in the OTP select table (see Table 20).
GPIO_8	B10	88	0	strap_sflashPresent_sdioPadVddio	In SDIO mode, this pin acts as sdio_padVddio strap. In USB mode, this pin acts as sflashPresent strap.
GPIO_9	E11	89	1	ARM Remap[0]	0: Boot from SRAM, ARM held in reset. 1: Boot from ROM by remapping the ARM core exception vectors there, ARM running out of reset.
GPIO_10	L7	90	0	spromPresent/ flashType	When this bit is set to 1, this pin selects the use of an external SPROM multiplexed onto the GPIO lines. GPIO8 = CLK, GPIO9 = CS, GPIO10 = input data from SPROM, GPIO11 = data output to SPROM If sflashPresent = 1, then this strapping option decides the type of sflash used.

Table 19: WLAN GPIO Functions and Strapping Options (Advance Information) (Cont.)

Pin Name	FCFBGA Pin	WLCSP Pin #	Default	Function	Description
GPIO_11	D11	91	0	IlpDivEn	0: Select external sleep clock or LPO clock (based on the value on LPOSelect strap) as ILP clock. 1: Select the clock derived by dividing the ALP clock by IlpDiv. If this field is set to 1, the ResourceInitMode option must be set to 10 for ALP clock available.
GPIO_13	B9	93	0	LPOSelect	0: Select external sleep clock as ILP clock. 1: Select internal LPO clock. This value is ignored if the LPOAutoDetEn option is set to 1.
GPIO_15, GPIO_14	M6 N6	95 94	10	ResourceInitMode [1:0]	00: For PMU to power up to ILP clock available (no backplane clock), 01: Power up to ILP clock request. 10: ALP clock available. 11: HT clock available. This field must be set to 10 for the ALP clock available if IlpDivEn strap is set to 1. This field may not be set to 11 for implementations using an oscillator running at other than 30 MHz because the PLL must be reprogrammed before it is enabled.

Table 20: OTP Select

UseSprom	OTPEnabled	OTP State	CIS Source	ChipID Source
0	0	OFF	Default	Default
0	1	ON	OTP if programmed, else default.	OTP if programmed, else default.
1	0	OFF	SPROM	Default
1	1	ON	SPROM	OTP if programmed, else default.

Table 21: WLAN GPIO Functions and Strapping Options (Advance Information)

Pin Name	FCFBGA Pin	WLCSP Pin #	Default	Function	Description
SDIO_DATA_1	L15	117	0	strap_host_ifc_1	The three pins strap_host_ifc_[3:1] together select the host interface mode: • 0XX: SDIO • 10X: gSPI • 110: normal HSIC • 111: bootloader-less HSIC
SDIO_DATA_2	K16	118	0	strap_host_ifc_2	
GPIO_6	A11	86	0	strap_host_ifc_3	

Multiplexed Bluetooth GPIO Signals

The Bluetooth GPIO pins (BT_GPIO_0 to BT_GPIO_7) are multiplexed pins and can be programmed to be used as GPIOs or for other Bluetooth interface signals such as I^2S. The specific function for a given BT_GPIO_X pin is chosen by programming the Pad Function Control Register for that specific pin. Table 22 shows the possible options for each BT_GPIO_X pin. Note that each BT_GPIO_X pin's Pad Function Control Register Setting is independent (BT_GPIO_1 can be set to Pad Function 7 at the same time that BT_GPIO_3 is set to PAD Function 0). When the Pad Function Control Register is set to 0 the BT_GPIOs do not have specific functions assigned to them and behave as generic GPIOs. The A_GPIO_X pins described below are multiplexed behind the BCM43241 PCM and I^2S interface pins.

Table 22: GPIO Multiplexing Matrix

	Pad Function Control Register Setting							
Pin Name	***0***	***1***	***2***	***3***	***4***	***5***	***6***	***7***
BT_UART_CTS_N	UART_CTS_N	–	–	–	–	–	–	A_GPIO[1]
BT_UART_RTS_N	UART_RTS_N	–	–	–	–	–	–	A_GPIO[0]
BT_UART_RXD	UART_RXD	–	–	–	–	–	–	GPIO[5]
BT_UART_TXD	UART_TXD	–	–	–	–	–	–	GPIO[4]
BT_PCM_IN	A_GPIO[3]	PCM_IN	PCM_IN	HCLK		–	–	I2S_SSDI/MSDI
BT_PCM_OUT	A_GPIO[2]	PCM_OUT	PCM_OUT	LINK_IND		I2S_MSDO	–	I2S_SSDO
BT_PCM_SYNC	A_GPIO[1]	PCM_SYNC	PCM_SYNC	HCLK	INT_LPO	I2S_MWS	–	I2S_SWS
BT_PCM_CLK	A_GPIO[0]	PCM_CLK	PCM_CLK	–	–	I2S_MSCK	–	I2S_SSCK
BT_I2S_DO	A_GPIO[5]	PCM_OUT	–	–	I2S_SSDO	I2S_MSDO	–	STATUS
BT_I2S_DI	A_GPIO[6]	PCM_IN	–	HCLK	I2S_SSDI/ MSDI	–	–	TX_CON_FX
BT_I2S_WS	GPIO[7]	PCM_SYNC	–	LINK_IND	–	I2S_MWS	–	I2S_SWS
BT_I2S_CLK	GPIO[6]	PCM_CLK	–	–	INT_LPO	I2S_MSCK	–	I2S_SSCK
BT_GPIO_5[a]	GPIO[5]	HCLK	–	I2S_MSCK	I2S_SSCK	–	–	CLK_REQ
BT_GPIO_4[a]	GPIO[4]	LINK_IND		I2S_MSDO	I2S_SSDO	–	–	–
BT_GPIO_3[a]	GPIO[3]	–		I2S_MWS	I2S_SWS	–	–	–
BT_GPIO_2[a]	GPIO[2]	–	–	–	I2S_SSDI/ MSDI	–	–	–
BT_GPIO_1	GPIO[1]	–	–	–	–	–	–	CLASS1[2]
BT_GPIO_0	GPIO[0]	–	–	–	clk_12p288	–	–	–
CLK_REQ	WL/BT_CLK_REQ	–	–	–	–	–	–	A_GPIO[7]

a. Available only in the WLCSP package.

The multiplexed GPIO signals are described in Table 23.

Table 23: Multiplexed GPIO Signals

Pin Name	*Type*	*Description*
UART_CTS_N	I	Host UART clear to send
UART_RTS_N	O	Device UART request to send
UART_RXD	I	Device UART receive data
UART_TXD	O	Host UART transmit data
PCM_IN	I	PCM data input
PCM_OUT	O	PCM data output
PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input)
PCM_CLK	I/O	PCM clock, can be master (output) or slave (input)
GPIO[7:0]	I/O	General-purpose I/O
A_GPIO[7:0]	I/O	A group general-purpose I/O
I2S_MSDO	O	I^2S master data output
I2S_MWS	O	I^2S master word select
I2S_MSCK	O	I^2S master clock
I2S_SSCK	I	I^2S slave clock
I2S_SSDO	O	I^2S slave data output
I2S_SWS	I	I^2S slave word select
I2S_SSDI/MSDI	I	I^2S slave/master data input
STATUS	O	Signals Bluetooth priority status
TX_CON_FX	I	WLAN-BT coexist. Transmission confirmation; permission for BT to transmit
RF_ACTIVE	O	WLAN-BT coexist. Asserted (logic high) during local BT RX and TX slots
LINK_IND	O	BT receiver/transmitter link indicator
CLK_REQ	O	WLAN/BT clock request output

I/O States

The following notations are used in Table 24:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 24: I/O States

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/ Sleep (All Power Present)*	*Power-Down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)*	*(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present*	*(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present*	*Power Rail*
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)		–
BT_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)		–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active-high	High-Z, NoPull	Open drain. Active-high	Open drain. Active-high.		BT_VDDO
BT_HOST_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_DEV_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_GPIO 2,3,4,5	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_UART_CTS	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU		BT_VDDO
BT_UART_RTS	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU		BT_VDDO

Table 24: I/O States (Cont.)

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/ Sleep (All Power Present)*	*Power-Down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)*	*(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present*	*(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present*	*Power Rail*
BT_UART_RXD	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU		BT_VDDO
BT_UART_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU		BT_VDDO
SDIO Data	I/O	N	Input/Output; PU	Input; PU	High-Z, NoPull	Input; PU	Input; PU		WL_VDDIO
SDIO CMD	I/O	N	Input/Output; PU	Input; PU	High-Z, NoPull	Input; PU	Input; PU		WL_VDDIO
SDIO_CLK	I	N	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; NoPull	Input; NoPull		WL_VDDIO
BT_PCM_CLK	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_PCM_IN	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_PCM_OUT	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_PCM_SYNC	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_I2S_WS	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_I2S_CLK	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_I2S_DI	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
BT_I2S_DO	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD		BT_VDDO
WL GPIO_0	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD		WL_VDDIO
WL GPIO_1	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU		WL_VDDIO
WL GPIO_2	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU		WL_VDDIO
WL GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU		WL_VDDIO

Table 24: I/O States (Cont.)

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/ Sleep (All Power Present)*	*Power-Down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)*	*(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present*	*(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present*	*Power Rail*
WL GPIO_4	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: noPull])	Input/Output; PU, PD, NoPull (programmable [Default: noPull])	High-Z, NoPull	Input; NoPull	Input; NoPull		WL_VDDIO
WL GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU		WL_VDDIO
WL GPIO_6	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD		WL_VDDIO

Note:

1. Keeper column: N=pad has no keeper. Y=pad has a keeper. Keeper is always active except in Power-down state.
2. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to floating pad (SDIO_CLK, for example).
3. In the Power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.
4. Depending on whether the PCM interface is enabled and the configuration of PCM is in master or slave mode, it can be either output or input.
5. Depending on whether the I^2S interface is enabled and the configuration of I^2S is in master or slave mode, it can be either output or input.

Section 15: DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 25 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 25: Absolute Maximum Ratings

Rating	*Symbol*	*Value*	*Unit*
DC supply for VBAT	VBAT	–0.5 to +5.5	V
DC supply voltage for I/O	VDDIO	–0.5 to 3.8	V
DC supply voltage for RF	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
DC supply voltage for RF I/Os and PA supply	VDDIO_RF	–0.5 to 3.8	V
DC input supply voltage for CLDO and LNLDO1	–	–0.5 to 2.1	V
WRF_TCXO_VDD	–	–0.5 to 1.98	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum Junction Temperature	T_j	125	°C

Environmental Ratings

The environmental ratings are shown in Table 26.

Table 26: Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85	°C	Functional operation[a]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 27: ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	TBD	V
Machine Model (MM)	ESD_HAND_MM	Machine model contact	TBD	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	TBD	V

Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 28 and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 28: Recommended Operating Conditions and DC Characteristics

		Value			
Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
DC supply voltage for VBAT	VBAT	2.3[a]	–	4.8[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	-	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	-	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					

Table 28: Recommended Operating Conditions and DC Characteristics (Cont.)

		Value			
Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output Low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins					
For VDDIO_RF = 3.3V:					
Output High Voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output Low Voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

a. The BCM43241 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.0V < VBAT < 4.8V.
b. The maximum continuous supply voltage is 4.8V. Brief spikes above 4.8V can be tolerated. Specifically, voltages as high as 5.5V for up to 10 seconds cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds cumulative duration over the lifetime of the device are allowed.

Section 16: Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 26: "Environmental Ratings," on page 118 and Table 28: "Recommended Operating Conditions and DC Characteristics," on page 119. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

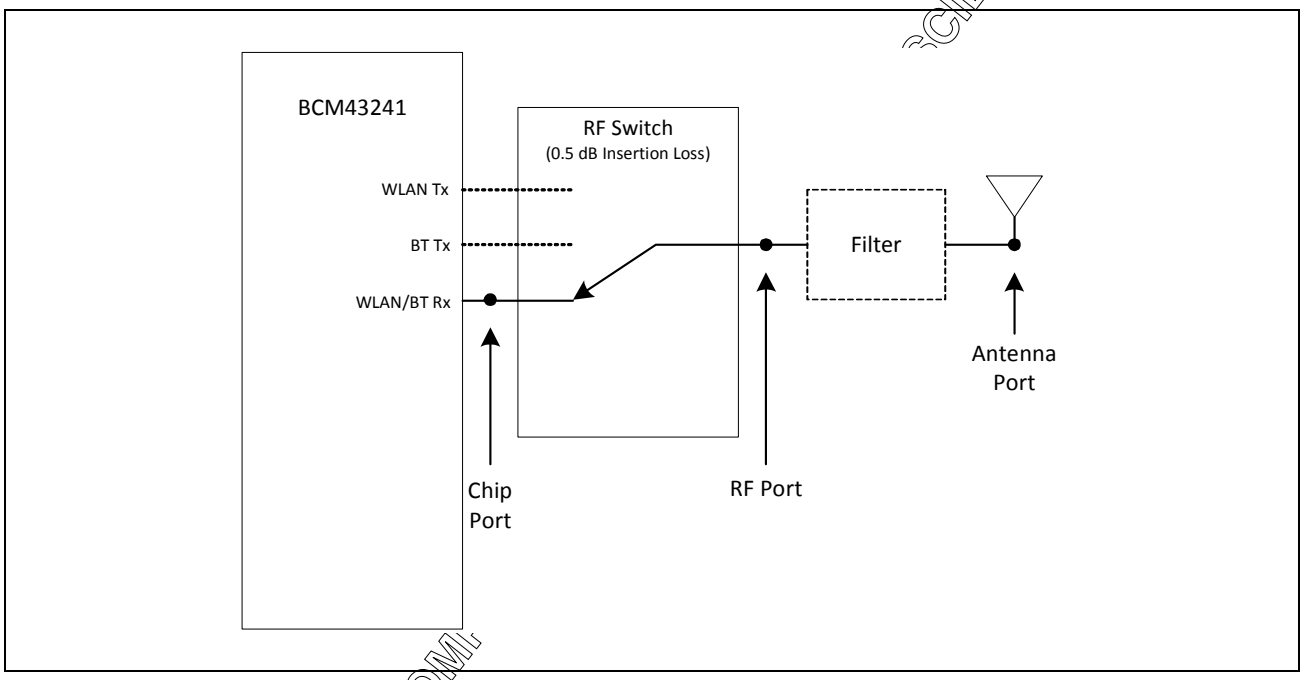


Figure 40: RF Port Location for Bluetooth Testing

Note: All Bluetooth specifications are measured at the Chip port unless otherwise specified.

Table 29: Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4–DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8–DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
Interference Performance[a]					
C/I co-channel	GFSK, 0.1% BER	–	8.5	–	dB
C/I 1-MHz adjacent channel	GFSK, 0.1% BER	–	–5	–	dB
C/I 2-MHz adjacent channel	GFSK, 0.1% BER	–	–35	–	dB
C/I ≥ 3-MHz adjacent channel	GFSK, 0.1% BER	–	–49	–	dB
C/I image channel	GFSK, 0.1% BER	–	–31	–	dB
C/I 1-MHz adjacent to image channel	GFSK, 0.1% BER	–	–42	–	dB
C/I co-channel	π/4–DQPSK, 0.1% BER	–	10	–	dB
C/I 1-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–10	–	dB
C/I 2-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–35	–	dB
C/I ≥ 3-MHz adjacent channel	8–DPSK, 0.1% BER	–	–50	–	dB
C/I image channel	π/4–DQPSK, 0.1% BER	–	–28	–	dB
C/I 1-MHz adjacent to image channel	π/4–DQPSK, 0.1% BER	–	–45	–	dB
C/I co-channel	8–DPSK, 0.1% BER	–	17	–	dB
C/I 1 MHz adjacent channel	8–DPSK, 0.1% BER	–	–4	–	dB
C/I 2 MHz adjacent channel	8–DPSK, 0.1% BER	–	–33	–	dB
C/I ≥ 3-MHz adjacent channel	8–DPSK, 0.1% BER	–	–47	–	dB
C/I Image channel	8–DPSK, 0.1% BER	–	–21	–	dB
C/I 1-MHz adjacent to image channel	8–DPSK, 0.1% BER	–	–39	–	dB

Table 29: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer					
	GFSK (1 Mbps)[b]				
698–716 MHz	WCDMA	–	–8.5		dBm
776–794 MHz	WCDMA	–	–8.5	–	dBm
824–849 MHz	GSM850	–	–10.9	–	dBm
824–849 MHz	WCDMA	–	–10.3	–	dBm
880–915 MHz	E-GSM	–	–11.3	–	dBm
880–915 MHz	WCDMA	–	–10.9	–	dBm
1710–1785 MHz	GSM1800	–	–17.3	–	dBm
1710–1785 MHz	WCDMA	–	–16.4	–	dBm
1850–1910 MHz	GSM1900	–	–18.5	–	dBm
1850–1910 MHz	WCDMA	–	–17.8	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18.8	–	dBm
1920–1980 MHz	WCDMA	–	–18.1	–	dBm
2010–2025 MHz	TD–SCDMA	–	–19.3	–	dBm
2500–2570 MHz	WCDMA	–	–18.1	–	dBm
	π/4 DPSK (2 Mbps)[b]				
698–716 MHz	WCDMA	–	–5.9	–	dBm
776–794 MHz	WCDMA	–	–5.9	–	dBm
824–849 MHz	GSM850	–	–8.4	–	dBm
824–849 MHz	WCDMA	–	–8	–	dBm
880–915 MHz	E-GSM	–	–8.6	–	dBm
880–915 MHz	WCDMA	–	–8.6	–	dBm
1710–1785 MHz	GSM1800	–	–14.4	–	dBm
1710–1785 MHz	WCDMA	–	–14.3	–	dBm
1850–1910 MHz	GSM1900	–	–15.2	–	dBm
1850–1910 MHz	WCDMA	–	–14.6	–	dBm
1880–1920 MHz	TD-SCDMA	–	–16.3	–	dBm
1920–1980 MHz	WCDMA	–	–15.2	–	dBm
2010–2025 MHz	TD-SCDMA	–	–16.7	–	dBm
2500–2570 MHz	WCDMA	–	–16.7	–	dBm

Table 29: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
		8DPSK (3 Mbps)[c]			
698–716 MHz	WCDMA	–	–7.5	–	dBm
776–794 MHz	WCDMA	–	–7.5	–	dBm
824–849 MHz	GSM850	–	–10.0	–	dBm
824–849 MHz	WCDMA	–	–9.7	–	dBm
880–915 MHz	E-GSM	–	–10.0	–	dBm
880–915 MHz	WCDMA	–	–9.7	–	dBm
1710–1785 MHz	GSM1800	–	–16.3	–	dBm
1710–1785 MHz	WCDMA	–	–15.6	–	dBm
1850–1910 MHz	GSM1900	–	–17.4	–	dBm
1850–1910 MHz	WCDMA	–	–16.9	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18.1	–	dBm
1920–1980 MHz	WCDMA	–	–17.5	–	dBm
2010–2025 MHz	TD-SCDMA	–	–19.1	–	dBm
2500–2570 MHz	WCDMA	–	–18.5	–	dBm
Spurious Emissions					
30 MHz–1 GHz			–	–62	dBm
1–12.75 GHz			–	–47	dBm
851–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
b. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = –84.5 dBm.
c. Bluetooth reference level for the wanted signal at the Bluetooth chip port = –79.5 dBm.

Table 30: Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) Tx power at Bluetooth		11.0	13.0	–	dBm
QPSK Tx Power at Bluetooth		8.0	10.0	–	dBm
8PSK Tx Power at Bluetooth		8.0	10.0	–	dBm
Power control step		2	4	6	dB
Note: Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–		1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–	–20.0	dBm
|M – N| ≥ 2.5 MHz			–	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [a, b]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [b, c, d]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
Rx LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
GPS Band Spurious Emissions					
Spurious emissions		–	–150	–127	dBm
Out-of-Band Noise Floor [e]					
65–108 MHz	FM Rx	–	–140	–	dBm/Hz
776–794 MHz	CDMA2000	–	–140	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–140	–	dBm/Hz
925–960 MHz	E-GSM	–	–140	–	dBm/Hz
1570–1580 MHz	GPS	–	–140	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–140	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–140	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–140	–	dBm/Hz

a. The maximum value represents the value required for Bluetooth qualification as defined in the v4.0 specification.
b. The spurious emissions during Idle mode are the same as specified in Table 30 on page 125.
c. Specified at the Bluetooth Antenna port.
d. Meets this specification using a front-end band-pass filter.
e. Transmitted power in cellular and FM bands at the Bluetooth Antenna port. See Figure 40 on page 121 for location of the port.

Table 31: Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±10	±25	kHz
DH3 packet	–	±10	±40	kHz
DH5 packet	–	±10	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	–	175	kHz
10101010 sequence in payload[b]	115	–	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 32: BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Freq range	–	2402		2480	MHz
Rx sense	GFSK, .1% BER, 1 Mbps	–	-95.0	–	dBm
Tx power[a]	–	–	8.5	–	dBm
Mod Char: delta f1 avg	–	225	–	275	KHz
Mod Char: delta f2 max[b]	–	99.9	–	–	%
Mod Char: ratio	–	0.8	–	–	%

a. BLE Tx power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc.). The output is capped at 12 dBm out. The BLE Tx power at the antenna port cannot exceed the 10 dBm specification limit.
b. At least 99.9% of all delta F2 max freq values recorded over 10 pkts must be greater than 185 kHz.

Section 17: FM Receiver Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified inTable 26: “Environmental Ratings,” on page 118 and Table 28: “Recommended Operating Conditions and DC Characteristics,” on page 119. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Table 33: FM Receiver Specifications

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
RF Parameters					
Operating frequency[b]	Frequencies inclusive	65	–	108	MHz
Sensitivity[c]	FM only	–	–0.5	–	dBµV EMF
	Δf = 22.5 kHz, fmod = 1 kHz	–	0.95	–	µV EMF
	SNR ≥ 26 dB	–	–6.5	–	dBµV
Receiver adjacent channel selectivity[c,d]	Measured for 30 dB SNR at the audio output. Wanted Signal: 23 dBµV EMF (14.1 µV EMF), Δf = 22.5 kHz, fmod = 1 kHz Interferer: Δf = 22.5 kHz, fmod = 1 kHz				
	At ±200 kHz	–	51	–	dB
	At ±400 kHz	–	62	–	dB
Intermediate signal plus noise-to-noise ratio (S+N)/N, stereo[c]	Vin = 20 dBµV EMF (10 µV EMF), Δf = 22.5 kHz, fmod = 1 kHz BAF = 300 Hz to 15 kHz, A-weighted mono	45	53	–	dB

Table 33: FM Receiver Specifications (Cont.)

Parameter	*Conditions*[a]	*Minimum*	*Typical*	*Maximum*	*Units*
Intermodulation performance[c,d]	Blocker level increased until desired at 30 dB SNR Wanted Signal: 33 dBµV EMF (45 µV EMF), Δf =22.5 kHz, fmod = 1 kHz Modulated Interferer: At f_{Wanted} ±400 kHz and ±4 MHz Δf =22.5 kHz, fmod = 1 kHz CW Interferer: At f_{Wanted} ±800 kHz and ±8 MHz	–	55	–	dBc
AM suppression, mono[c]	Vin = 23 dBµV EMF (14.1 µV EMF), Δf = 22.5 kHz, fmod = 1 kHz AM at 400 Hz with m = 0.3 No A-weighted or any other filtering applied	40	–	–	dB
RDS					
RDS sensitivity[e,f]	Δf = 32 kHz, fmod=1 kHz, Δf Pilot = 7.5 kHz	–	16	–	dBµV EMF
	95% of blocks decoded with no errors after correction RDS deviation=1.2 kHz	–	6.3	–	µV EMF
		–	10	–	dBµV
	RDS deviation = 2 kHz	–	12	–	dBµV EMF
		–	4	–	µV EMF
		–	6	–	dBµV
RDS selectivity[f]	Wanted Signal: 33 dBµV EMF (45 µV EMF), 2 kHz RDS deviation Δf = 32 kHz, fmod=1 kHz, Δf Pilot = 7.5 kHz Interferer: Δf = 40 kHz, fmod = 1 kHz Interferer level for 95% of blocks decoded with no errors after correction				
	±200 kHz	–	49	–	dB
	±300 kHz	–	52	–	dB
	±400 kHz	–	52	–	dB
RF Input					
RF input impedance		1.5	–		kΩ
Antenna tuning capacitor		2.5	–	30	pF

Table 33: FM Receiver Specifications (Cont.)

Parameter	*Conditions*[a]	*Minimum*	*Typical*	*Maximum*	*Units*
Maximum input level[c]	Δf = 22.5 kHz, fmod = 1 kHz SNR > 26 dB	–	105	–	dBµV EMF
		–	178	–	mV EMF
		–	99	–	dBµV
RF conducted emissions	Local oscillator breakthrough measured on the reference port	–	–	–55	dBm
	GPS 869–894, 925–960 MHz, 1805–1880 MHz, 1930–1990 MHz	–	–	–90	dBm

Table 33: FM Receiver Specifications (Cont.)

Parameter	*Conditions*[a]	*Minimum*	*Typical*	*Maximum*	*Units*
RF blocking levels at the FM antenna input 40 dB SNR (assumes a 50Ω at the radio input and excludes spurs)	GSM850, E-GSM (standard/edge), BW = 0.2 MHz, 824–849, 880-915	0	–	–	dBm
	GSM DCS 1800, PCS 1900 (standard, edge), BW = 0.2 MHz, 1710–1785, 1850–1910	–5	–	–	dBm
	WCDMA - II(I), III(IV,X), BW = 5MHz, 1850–1980 (1920-1980), 1710–1785 (1710–1755, 1710–1770),	–5	–	–	dBm
	WCDMA - V(VI), VIII, XII, XIII, XIV, BW=5 MHz, 824–849 (830–840), 880–915,	–5	–	–	dBm
	CDMA2000, CDMA One, 1.25 MHz, 824–849, 887–925, 776–794	–10	–	–	dBm
	CDMA2000, CDMA One, BW= 1.25MHz, 1850–1910, 1750–1780, 1920–1980	–5	–	–	dBm
	BT, BW = 1 MHz, 2402–2480	–20	–	–	dBm
	WLAN-g/b, BW = 20 MHz, 2400–2483.5	–20	–	–	dBm
	WLAN-a, BW = 20M Hz, 4915–5825	–20	–	–	dBm
Tuning					
Frequency step	–	10	–		kHz

Table 33: FM Receiver Specifications (Cont.)

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
Settling time	Single frequency switch in any direction to a frequency within the bands 88–108 MHz or 76–90 MHz. Time measured to within 5 kHz of the final frequency.	–	150	–	µs
Search time	Total time for an automatic search to sweep from 88–108 MHz or 76–90 MHz (and reverse direction) assuming no channels found.	–	–	8	sec
General Audio					
Audio output level[g]	Vin = 66 dBµV EMF (2 mV EMF) Δf = 22.5 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz	–14.5	–	-12.5	dBFS
Maximum audio output level[h]	Vin = 66 dBµV EMF (2 mV EMF), Δf = 100 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz	–	–	0	dBFS
Soft mute attenuation and start level	Muting is performed dynamically proportional to the FM wanted input signal C/N. The muting characteristic is fully programmable. See "Audio Features" on page 61 for further details.				
Maximum signal plus noise-to-noise ratio (S+N)/N, mono[i]	Vin = 66 dBµV EMF (2 mV EMF) Δf = 22.5 kHz, fmod = 1 kHz	–	69	–	dB
Maximum signal plus noise-to-noise ratio (S+N)/N, stereo[g]	Vin = 66 dBµV EMF (2 mV EMF) Δf = 22.5 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz	–	64	–	dB
Total harmonic distortion, mono	Vin = 66 dBµV EMF (2 mV EMF), Δf = 75 kHz, fmod = 400 Hz	–	–	0.8	%
	Δf = 75 kHz, fmod = 1 kHz	–	–	0.8	%
	Δf = 75 kHz, fmod = 3 kHz	–	–	0.8	%
	Δf = 100 kHz, fmod = 1 kHz,	–	–	1.0	%
Total harmonic distortion, stereo	Vin = 66 dBµV EMF (2 mV EMF) Δf = 67.5 kHz, fmod = 1 kHz, Δf Pilot=7.5kHz, L=R			1.5	%
Audio spurious products[i]	Vin = 66 dBµV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz, Range from 300 Hz to 15 kHz, with respect to 1 kHz tone	–		–60	dBc

Table 33: FM Receiver Specifications (Cont.)

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
Audio bandwidth, upper (–3 dB point)	Vin = 66 dBµV EMF (2 mV EMF) Δf = 8 kHz, for 50 µs	15	–	–	kHz
Audio bandwidth, lower (–3 dB point)		–	–	20	Hz
Audio in-band ripple	100 Hz to 13 kHz, Vin = 66 dBµV EMF (2 mV EMF) Δf = 8 kHz, for 50 µs	–0.5	-	0.5	dB
Deemphasis time constant tolerance	With respect to 50 µs and 75 µs	–	–	±5	%
RSSI range	With 1 dB resolution and ±5 dB accuracy at room temp	3	–	83	dBµV EMF
		1.41	–	1.41E+04	µV EMF
		–3	–	77	dBuV
Stereo Decoder					
Stereo channel separation	Forced Stereo mode Vin = 66 dBµV EMF(2 mV EMF), Δf = 67.5kHz, fmod = 1kHz, Δf Pilot = 6.75kHz R = 0, L= 1	–	48	–	dB
Mono Stereo Blend and Switching	Blending and switching is dynamically proportional to the FM wanted input signal C/N. The blending and switching characteristics are fully programmable. "Audio Features" on page 61 for further details.				
Pilot suppression	Vin = 66 dBµV EMF (2 mV EMF), Δf = 75 kHz, fmod = 1 kHz,	46	–	–	dB
Pause Detection					
Audio level at which a pause is detected	Relative to 1kHz tone, Δf = 22.5 kHz	–	–	–	–
	4 values in 3 dB steps	–21	–	–12	dB
Audio pause duration	4 values	20	–	40	ms

a. The following conditions are applied to all relevant tests unless otherwise indicated: Preemphasis and deemphasis of 50 µs, R = L for mono, BAF = 300 Hz to 15 kHz, A-weighted filtering applied.

b. Please contact Broadcom regarding applications that will operate between 65 and 76 MHz.
c. Wanted signal: Δf = 22.5 kHz, fmod = 1 kHz.
d. Interferer: Δf = 22.5 kHz, fmod = 1 kHz.
e. RDS sensitivity numbers are for 87.5 to 108 MHz only.
f. Vin = Δf = 32 kHz, fmod=1 kHz, Δf Pilot = 7.5 kHz, 95% of blocks decoded with no errors after correction.
g. Vin = 66 dBµV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz.
h. Vin = 66 dBµV EMF (2 mV EMF), Δf = 100 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz.
i. Vin = 66 dBµV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz.

Section 18: WLAN RF Specifications

Introduction

The BCM43241 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz band or the 5 GHz band. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 26: "Environmental Ratings," on page 118 and Table 28: "Recommended Operating Conditions and DC Characteristics," on page 119. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

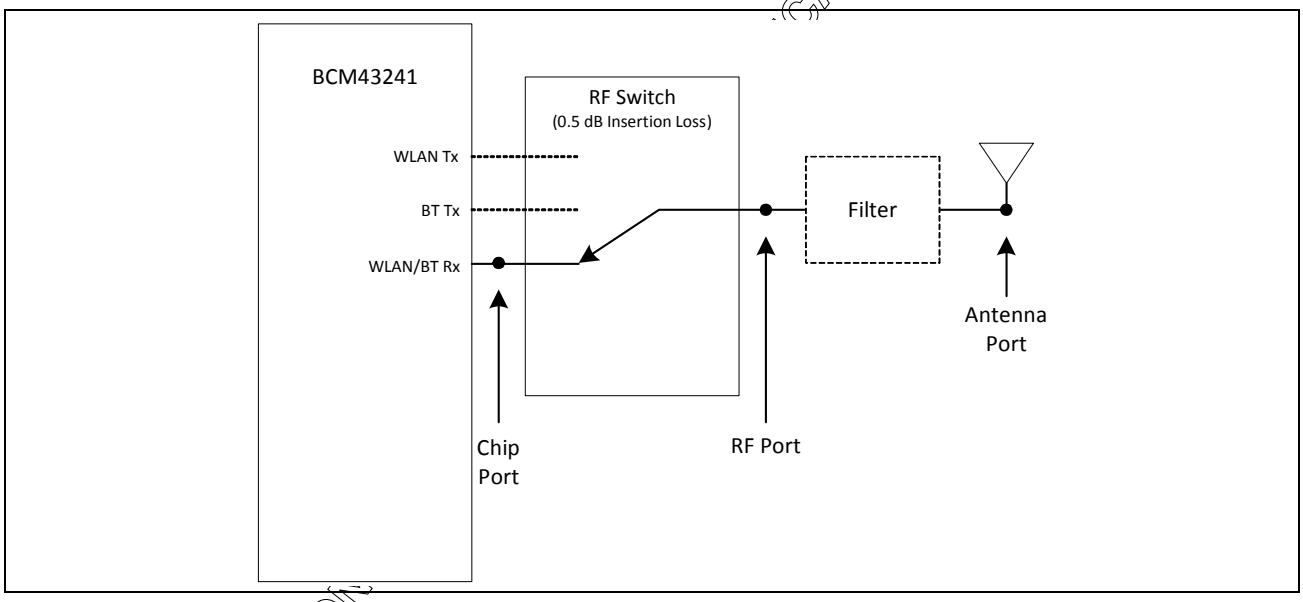


Figure 41: Port Locations

Note: All WLAN specifications are measured at the chip port, unless otherwise specified.

2.4 GHz Band General RF Specifications

Table 34: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
Tx/Rx switch time	Including TX ramp down	–	–	5	µs
Rx/Tx switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 35 are measured at the chip port, unless otherwise specified.

Table 35: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
SISO RX sensitivity (8% PER for 1024 octet PSDU)[a]	1 Mbps DSSS	–	–99.0	–	dBm
	2 Mbps DSSS	–	–96.0	–	dBm
	5.5 Mbps DSSS	–	–94.2	–	dBm
	11 Mbps DSSS	–	–90.4	–	dBm
SISO RX sensitivity (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–94.0	–	dBm
	9 Mbps OFDM	–	–93.1	–	dBm
	12 Mbps OFDM	–	–91.7	–	dBm
	18 Mbps OFDM	–	–89.6	–	dBm
	24 Mbps OFDM	–	–85.6	–	dBm
	36 Mbps OFDM	–	–83	–	dBm
	48 Mbps OFDM	–	–77.7	–	dBm
	54 Mbps OFDM	–	–76.5	–	dBm
MIMO RX sensitivity (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–95.0	–	dBm/core
	9 Mbps OFDM	–	–94.2	–	dBm/core
	12 Mbps OFDM	–	–93.5	–	dBm/core
	18 Mbps OFDM	–	–92.6	–	dBm/core
	24 Mbps OFDM	–	–88.6	–	dBm/core
	36 Mbps OFDM	–	–86	–	dBm/core
	48 Mbps OFDM	–	–80.7	–	dBm/core
	54 Mbps OFDM	–	–79.5	–	dBm/core
SISO RX sensitivity (10% PER for 4096 octet PSDU)[a,b]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 7	–	–73.9	–	dBm
	MCS 6	–	–75.6	–	dBm
	MCS 5	–	–77	–	dBm
	MCS 4	–	–81.4	–	dBm
	MCS 3	–	–84.5	–	dBm
	MCS 2	–	–88.3	–	dBm
	MCS 1	–	–90.5	–	dBm
	MCS0	–	–92.5	–	dBm

Table 35: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
MIMO RX sensitivity (10% PER for 4096 octet PSDU)[a,b]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS 15		–	–70.4	–	dBm (total)
	MCS 8		–	–90.1	–	dBm (total)
	MCS 7		–	–76.9	–	dBm/core
	MCS 6		–	–78.6	–	dBm/core
	MCS 5		–	–80	–	dBm/core
	MCS 4		–	–84.4	–	dBm/core
	MCS 3		–	–87.5	–	dBm/core
	MCS 2		–	–91.1	–	dBm/core
	MCS 1		–	–93.2	–	dBm/core
	MCS0		–	–94.0	–	dBm/core
Blocking level for 1dB Rx sensitivity degradation (without external filtering)[c]	776–794 MHz	CDMA2000	–20	–	–	dBm
	824–849 MHz[d]	cdmaOne	–24.5	–	–	dBm
	824–849 MHz	GSM850	–20	–	–	dBm
	880–915 MHz	E-GSM	–18	–	–	dBm
	1710–1785 MHz	GSM1800	–20	–	–	dBm
	1850–1910 MHz	GSM1800	–22	–	–	dBm
	1850–1910 MHz	cdmaOne	–32	–	–	dBm
	1850–1910 MHz	WCDMA	–29	–	–	dBm
	1920–1980 MHz	WCDMA	–32	–	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	Rx PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–19.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–19.5	–	–	dBm
LPF 3 dB Bandwidth	–		9	–	10	MHz

Table 35: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
Maximum receiver gain	–	–	–	105	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[e]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		6	10	–	dB
Receiver cascaded noise figure	At maximum gain		–	3.5	–	dB

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
c. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.

d. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
e. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 36 are measured at the chip port output, unless otherwise specified.

Table 36: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands (at 18 dBm, ≥90% duty cycle, 1 Mbps CCK)[a]	76–108 MHz	FM Rx	–	TBD	–	dBm/Hz
	776–794 MHz	–	–	TBD		dBm/Hz
	869–960 MHz	CDMAOne, GSM850	–	TBD	–	dBm/Hz
	925–960 MHz	E-GSM	–	TBD	–	dBm/Hz
	1570–1580 MHz	GPS	–	TBD	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	TBD	–	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne, WCDMA	–	TBD	–	dBm/Hz
	2110–2170 MHz	WCDMA		TBD	–	dBm/Hz
Harmonic level (with ≥90% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–	TBD	dBm/1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–	TBD	dBm/1 MHz
TX power at chip port for highest power level setting at 25°C, VBAT = 3.6V, spectral mask and EVM compliance[b,b]	11b – 1 Mbps		–	20.5	–	dBm
	11g – 6 Mbps		–	19.5	–	dBm
	11g – 54 Mbps @ –25 dB EVM, single Tx chain		–	19.5	–	dBm
	11g – 54 Mbps @ –25 dB EVM, 2 TX chains, CDD		–	19	–	dBm
	MCS7 – HT20 @ –28 dB EVM, single TX chain		–	17.5	–	dBm
	MCS7 – HT20 @ –28 dB EVM, 2SS		–	17	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
Tx power control dynamic range	–		20	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port Tx	Z_o = 50Ω		4	6	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.
b. Derate by 1 dB for PA_Vdd supply (direct supply to PA) of 3V.

WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 37 are measured at the chip port input, unless otherwise specified.

Table 37: WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	4900	–	5845	MHz
SISO RX sensitivity (10% PER for 1000 octet PSDU)[a]	6 Mbps OFDM	–	–92.4	–	dBm
	9 Mbps OFDM	–	–91.1	–	dBm
	12 Mbps OFDM	–	–89.7	–	dBm
	18 Mbps OFDM	–	–87.6	–	dBm
	24 Mbps OFDM	–	–83.6	–	dBm
	36 Mbps OFDM	–	–81	–	dBm
	48 Mbps OFDM	–	–76.2	–	dBm
	54 Mbps OFDM	–	–75.1	–	dBm
MIMO RX sensitivity (10% PER for 1000 octet PSDU)[a]	6 Mbps OFDM	–	–93.5	–	dBm/core
	9 Mbps OFDM	–	–93	–	dBm/core
	12 Mbps OFDM	–	–91.7	–	dBm/core
	18 Mbps OFDM	–	–90.6	–	dBm/core
	24 Mbps OFDM	–	–86.6	–	dBm/core
	36 Mbps OFDM	–	–84	–	dBm/core
	48 Mbps OFDM	–	–79.2	–	dBm/core
	54 Mbps OFDM	–	–78.0	–	dBm/core
SISO RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 7	–	–71.9	–	dBm
	MCS 6	–	–73.6	–	dBm
	MCS 5	–	–75	–	dBm
	MCS 4	–	–79.4	–	dBm
	MCS 3	–	–82.5	–	dBm
	MCS 2	–	–86.3	–	dBm
	MCS 1	–	–88.5	–	dBm
	MCS 0	–	–90.5	–	dBm

Table 37: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
MIMO RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 15	–	–69.0	–	dBm (total)
	MCS 8	–	–89.0	–	dBm (total)
	MCS 7	–	–74.9	–	dBm/core
	MCS 6	–	–76.6	–	dBm/core
	MCS 5	–	–78	–	dBm/core
	MCS 4	–	–82.4	–	dBm/core
	MCS 3	–	–85.5	–	dBm/core
	MCS 2	–	–89.3		dBm/core
	MCS 1	–	–91.2	–	dBm/core
	MCS 0	–	–92.5	–	dBm/core
SISO RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS 7	–	–69.4	–	dBm
	MCS 6	–	–71.1	–	dBm
	MCS 5	–	–72.5	–	dBm
	MCS 4	–	–77	–	dBm
	MCS 3	–	–80	–	dBm
	MCS 2	–	–83.8	–	dBm
	MCS 1	–	–86	–	dBm
	MCS 0	–	–88.1	–	dBm
MIMO RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS 15	–	–67.0	–	dBm (total)
	MCS 8	–	–86.5	–	dBm (total)
	MCS 7	–	–71.9	–	dBm/core
	MCS 6	–	–73.7	–	dBm/core
	MCS 5	–	–75.1	–	dBm/core
	MCS 4	–	–79.6	–	dBm/core
	MCS 3	–	–82.7	–	dBm/core
	MCS 2	–	–86.5	–	dBm/core
	MCS 1	–	–88.6	–	dBm/core
	MCS 0	–	–90.4	–	dBm/core

Table 37: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blocking level for 1 dB Rx Sensitivity degradation (without external filtering)[b]	776–794 MHz	CDMA2000	–21	–	–	dBm
	824–849 MHz	CDMAOne	–20	–	–	dBm
	824–849 MHz	GSM850	–12	–	–	dBm
	880–915 MHz	E-GSM	–12	–	–	dBm
	1710–1785 MHz	GSM1800	–15	–	–	dBm
	1850–1910 MHz	GSM1800	–15	–	–	dBm
	1850–1910 MHz	CDMAOne	–20	–	–	dBm
	1850–1910 MHz	WCDMA	–24	–	–	dBm
	1920–1980 MHz	WCDMA	–24	–	–	dBm
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps		–29.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps		–29.5	–	–	dBm
LPF 3 dB bandwidth	–		9	–	18	MHz
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[c] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	100	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[d]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB

Table 37: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Return loss	Z_o = 50Ω	6	10	–	dB
Receiver cascaded noise figure	At maximum gain	–	5.0	–	dB

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. For 65 Mbps, the size is 4096.
d. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 38 are measured at the chip port, unless otherwise specified.

Table 38: WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands (at 18 dBm)[a], >90% duty cycle, OFDM	76–108 MHz	FM Rx	–	TBD	–	dBm/Hz
	776–794 MHz	–	–	TBD	–	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	–	TBD	–	dBm/Hz
	925–960 MHz	E-GSM	–	TBD	–	dBm/Hz
	1570–1580 MHz	GPS	–	TBD	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	TBD	–	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne, WCDMA	–	TBD	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	TBD	–	dBm/Hz
	2400–2483 MHz	BT/WLAN	–	TBD	–	dBm/Hz
Harmonic level (at 18 dBm)	9.8–11.570 GHz	2nd harmonic	–	TBD	–	dBm/MHz
TX power at chip port for highest power level setting at 25°C, VBAT = 3.6V, spectral mask and EVM compliance[b], [b]	11a – 6 Mbps – single TX chain		–	18	–	dBm
	11a – 6 Mbps – 2 TX chains – CDD		–	18	–	dBm
	11a – 54 Mbps @ –25 dB EVM – single TX chain		–	18	–	dBm
	11a – 54 Mbps @ –25 dB EVM – 2 TX chains – CDD		–	18	–	dBm
	MCS7 – HT20 @ –28 dB EVM – single TX chain		–	16	–	dBm
	MCS7 – HT20 @ –28 dB EVM – 2SS		–	16	–	dBm
	MCS7 – HT40 @ –28 dB EVM – single TX chain		–	16	–	dBm
	MCS7 – HT40 @ –28 dB EVM – 2SS		–	16	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.8	1[b]	Degrees
Tx power control dynamic range	–		20	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB

Table 38: WLAN 5 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Return loss	Z_o = 50Ω	–	6	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also apply to usages within these bands.
b. Applicable for channels 5550 MHz, 5755 MHz, and 5805 MHz.

General Spurious Emissions Specifications

Table 39: General Spurious Emissions Specifications

Parameter	Condition/Notes		Min	Typ	Max	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
Tx Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–	TBD	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–	TBD	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–	TBD	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–	TBD	dBm
Rx/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–78	–63	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–68.5[a]	–53	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–96	–53	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–96	–53	dBm

a. For frequencies other than 3.2 GHz, the emissions value is –96 dBm. The value presented in table is the result of LO leakage at 3.2 GHz.

Section 19: Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside of the specification limits provided in this section.

Core Buck Switching Regulator

Table 40: Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min	Typ	Max	Units
Input Supply Voltage VBAT (DC)	DC voltage range inclusive of disturbances.	2.3	3.6	4.8[a]	V
PWM mode switching frequency	Forced PWM without FLL enabled	2.8	4	5.2	MHz
	Forced PWM with FLL enabled	3.6	4	4.4	MHz
PWM output current	–	–	–	600	mA
Output Current Limit	Peak inductor current	1100	1400	–	mA
Output Voltage Range	Programmable, 30 mV steps Default = 1.35V	1.2	1.35	1.5	V
PWM Output Voltage DC Accuracy	Includes load and line regulation. Forced PWM mode	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max Ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap+Board total-ESR < 20 mΩ, Cout > 1.9 µF, ESL < 200 pH	–	7	20	mVpp
PWM Mode Peak Efficiency	Peak Efficiency at 200 mA load Vout = 1.35V, VBAT = 3.6V at 25°C, Fsw = 4 MHz 2.2 µH inductor 0806 with DCR = 0.11Ω ±25% and ACR <1Ω at 4 MHz	78	86	–	%
PFM Mode Efficiency	10 mA load current Vout = 1.35V, VBAT = 3.6V at 25°C, Cap+Board total-ESR < 20 mΩ, Cout = 4.7 µF, ESL < 200 pH FLL = OFF 0806-size, L = 2.2 µH, DCR = 110 mΩ ±25%, ACR < 2Ω	70	81	–	%

Table 40: Core Buck Switching Regulator (CBUCK) Specifications (Cont.)

Specification	Notes	Min	Typ	Max	Units
LPOM Efficiency	1 mA load current, Vout = 1.35V, VBAT = 3.6V at 25°C, Cap+Board total–ESR < 20 mΩ, Cout = 4.7 µF, ESL < 200 pH FLL = OFF L = 2.2 µH, DCR = 240 mΩ ±25%, ACR < 2Ω	62	72	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	674	850	µs
External Inductor	0806 with DCR = 0.11Ω ± 25% and ACR <1Ω	–	2.2	–	µH
External Output Capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, ± 20%, 6.3V	2[b]	4.7	10[c]	µF
External Input Capacitor	For SR_VDDBATP5V pin, Ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V, 4.7 µF	0.67[b]	4.7	–	µF
Input Supply Voltage Ramp-Up Time	0 to 4.3V	40	–	100,000	µs

a. The maximum continuous supply voltage is 4.8V. Brief spikes above 4.8V can be tolerated. Specifically, voltages as high as 5.5V for up to 10 seconds cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds cumulative duration over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
c. Total capacitance includes those capacitors connected at the far end of the active load.

3.3V LDO (LDO3P3)

Table 41: LDO3P3 Specifications

Specification	*Notes*	*Min*	*Typ*	*Max*	*Units*
Input Supply Voltage	Min= V_o + 0.15V = 3.45V (for Vo = 3.3V) dropout voltage requirement must be met under maximum load for performance specifications.	2.3	3.6	4.8	V
Output current	–	0.1	–	125	mA
Output Voltage, V_o	Default = 3.3V	2.4	3.3	3.4	V
Dropout Voltage	At max load.	–	–	150	mV
Output Voltage DC Accuracy	Includes Line/Load regulation. Load > 0.1 mA	–5		+5	%
Quiescent Current	No load	–	8	16	µA
	Max load		1000	1200	µA
Line Regulation	V_{in} from (V_o + 0.15V) to 4.8V, max load	-0.2	–	3.5	mV/V
Load Regulation	Load from 1 mA to 125 mA, V_{in} = 3.6V	–	0.3	0.45	mV/mA
PSRR	VBAT ≥ 3.6V, V_o = 3.3V, C_o = 2.2 µF, Max load, 100 Hz to 100 kHz	20	–	–	dB
LDO Turn-ON time	Chip already powered up.	–	–	150	µs
External Output Capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5m–240 mΩ), ± 10%, 10V	0.7[a]	2.2	4.7	µF
External Input Capacitor	For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402, ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	0.55[a]	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

CLDO

Table 42: CLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input Supply Voltage, V_{in}	Min $V_{in} = V_o + 0.15V = 1.35V$ (for Vo = 1.2V) dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	–	0.2	–	300	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout Voltage	At max load	–	–	150	mV
Output Voltage DC Accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent Current	No load	–	24		µA
	Max load	–	2100	–	µA
Line Regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 300 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
PSRR	@1 kHz, Vin ≥ V_o + 0.15V, C_o = 4.7 µF	20	–		dB
Start-up Time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 99% of V_o	–	550	850	µs
LDO Turn-on Time	LDO turn-on time when rest of the chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.32[a]	4.7	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO2

Table 43: LNLDO2 Specifications

Specification	*Notes*	*Min*	*Typ*	*Max*	*Units*
Input Supply Voltage, Vin	Min Vin = V_o + 0.15V = 1.35V (for V_o = 1.2V) dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	–	–	–	150	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout Voltage	At maximum load	–	–	150	mV
Output Voltage DC Accuracy	includes Line/Load regulation	–4	–	+4	%
Quiescent Current	No load	–	44	–	µA
	Max load		970	990	µA
Line Regulation	V_{in} from (V_o + 0.15V) to 1.5V, max load	–	–	5.5	mV/V
Load Regulation	Load from 1 mA to 150 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Output Noise	@30 kHz, 60-150 mA load C_o = 2.2 µF @100 kHz, 60-150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO Turn-on Time	LDO turn-on time when rest of chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[a]	2.2	4.7	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO1

Table 44: LNLDO1 Specifications

Specification	*Notes*	*Min*	*Typ*	*Max*	*Units*
Input Supply Voltage , Vin	Min $V_{in} = V_o$ +0.15V = 1.35V (for V_o = 1.2V) dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	–	0.2	–	325	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout Voltage	At maximum load	–	–	150	mV
Output Voltage DC Accuracy	includes Line/Load regulation	–4	–	+4	%
Quiescent Current	No load	–	88	–	µA
	Max load		2100	–	µA
Line Regulation	V_{in} from (V_o + 0.15V) to 1.5V, 300 mA load	–	–	+5	mV/V
Load Regulation	Load from 1 mA to 300 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Output Noise	@30 kHz, 60-325 mA load C_o = 4.7 µF @100 kHz, 60-325 mA load C_o = 4.7 µF	–	–	60 30	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 4.7 µF, V_o = 1.2V	20	–	–	dB
Start-up Time of PMU	VIO up and steady. Time from REG_ON rise edge to LNLDO1 reaching 99% of V_o	–	550	850	µs
LDO Turn-on Time	LDO turn-on time when rest of chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	1.32[a]	4.7	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

Section 20: System Current Consumption

Note:

- Values in this data sheet are design goals and are subject to change based on the results of device characterization.
- Unless otherwise stated, these values apply for the conditions specified in Table 28: "Recommended Operating Conditions and DC Characteristics," on page 119.

WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 45 and Table 46 on page 154.

All values in the tables are with the Bluetooth core in reset (that is, Bluetooth and FM are off).

Table 45: BCM43241 WLAN Current Consumption 2.4 GHz

	Typical, Host I/F=SDIO		*Unit*
Parameter	***VBAT=3.6V***	***VDDIO=1.8V***	
OFF (WL_REG_ON = Low, BT_REG_ON = low)	3	3	µA
Sleep (Interbeacon sleep)	4.3	153	µA
IEEE PS mode DTIM=1	1100	153	µA
IEEE PS mode DTIM=3	367	153	µA
Listen Current (1x1, OCL)	57	0.026	mA
Listen Current (2x2)	77	0.026	mA
Continuous Rx mode 54 Mbps(1x1 SCD)	62	0.026	mA
Continuous Rx mode 54 Mbps(2x2 MRC)	80	0.026	mA
Continuous Rx mode MCS7 - HT 20(1x1 SCD)	62	0.026	mA
Continuous Rx mode MCS7 - HT 20(2x2 MRC)	80	0.026	mA
Continuous Rx mode MCS8 - HT 20(2x2)	76.6	0.026	mA
Continuous Rx mode MCS15 - HT 20(2x2)	85	0.026	mA
Continuous Tx mode 1 Mbps	304 [@20.5 dBm]	0.026	mA
Continuous Tx mode 54 Mbps[SISO]	295 [@19.5 dBm]	0.026	mA
Continuous Tx mode 54 Mbps[CDD]	553 [@19.5 dBm]	0.026	mA
Continuous Tx mode MCS7 - HT20[SISO]	265 [@17.5 dBm]	0.026	mA
Continuous Tx mode MCS7 - HT20[CDD]	481 [@17.5 dBm]	0.026	mA
Continuous Tx mode MCS8 - HT20	542 [@19 dBm]	0.026	mA
Continuous Tx mode MCS15 - HT20	540 [@17.5 dBm]	0.026	mA

Table 45: BCM43241 WLAN Current Consumption 2.4 GHz (Cont.)

	Typical, Host I/F=SDIO		Unit
Parameter	**VBAT=3.6V**	**VDDIO=1.8V**	

Note:

- All Tx powers are referred at chip output per core.
- Continuous Tx/Rx currents correspond to 100% duty-cycle and are measured using packet engine.
- Listen-current measured when no carrier is present.

Table 46: BCM43241 WLAN Current Consumption 5 GHz

	Typical, Host I/F=SDIO		Unit
Parameter	**VBAT=3.6V**	**VDDIO=1.8V**	
OFF (WL_REG_ON = Low, no VDDIO)	3	3	µA
Sleep (Interbeacon sleep)	4.3	153	µA
IEEE PS mode DTIM=1	1100	153	µA
IEEE PS mode DTIM=3	367	153	µA
Listen Current (1×1, OCL)	62	0.026	mA
Listen Current (2×2)	85	0.026	mA
Continuous Rx mode 6 Mbps(1×1 SCD)	67	0.026	mA
Continuous Rx mode 6 Mbps(2×2 MRC)	88	0.026	mA
Continuous Rx mode 54 Mbps(1×1 SCD)	67	0.026	mA
Continuous Rx mode 54 Mbps(2×2 MRC)	88	0.026	mA
Continuous Rx mode MCS7 - HT 20(1×1 SCD)	67	0.026	mA
Continuous Rx mode MCS7 - HT 20(2×2 MRC)	88	0.026	mA
Continuous Rx mode MCS7 - HT 40(1×1 SCD)	93	0.026	mA
Continuous Rx mode MCS7 - HT 40(2×2 MRC)	125	0.026	mA
Continuous Rx mode MCS8 - HT 20	91	0.026	mA
Continuous Rx mode MCS8 - HT 40	130	0.026	mA
Continuous Rx mode MCS15 - HT 20	96	0.026	mA
Continuous Rx mode MCS15 - HT 40	138	0.026	mA
Continuous Tx mode 6 Mbps[SISO]	270 [@18 dBm]	0.026	mA
Continuous Tx mode 6 Mbps[CDD]	485 [@18 dBm]	0.026	mA
Continuous Tx mode 54 Mbps[SISO]	268 [@18 dBm]	0.026	mA
Continuous Tx mode 54 Mbps[CDD]	485 [@18 dBm]	0.026	mA
Continuous Tx mode MCS7 - HT20[SISO]	269 [@17 dBm]	0.026	mA
Continuous Tx mode MCS7 - HT20[CDD]	486[@17 dBm]	0.026	mA
Continuous Tx mode MCS7 - HT40[SISO]	278 [@17 dBm]	0.026	mA
Continuous Tx mode MCS7 - HT40[CDD]	510 [@17 dBm]	0.026	mA

Table 46: BCM43241 WLAN Current Consumption 5 GHz (Cont.)

Parameter	Typical, Host I/F=SDIO		Unit
	VBAT=3.6V	VDDIO=1.8V	
Continuous Tx mode MCS8 - HT20	508 [@18 dBm]	0.026	mA
Continuous Tx mode MCS8 - HT40	547 [@18 dBm]	0.026	mA
Continuous Tx mode MCS15 - HT20	512 [@17 dBm]	0.026	mA
Continuos Tx mode MCS15 - HT40	540 [@17 dBm]	0.026	mA

Note:

- All Tx powers are referred at chip output per core.
- Continuous Tx/Rx currents correspond to 100% duty-cycle and are measured using packet engine.
- Listen-current measured when no carrier is present.

Bluetooth and FM Current Consumption

The Bluetooth and FM current consumption measurements are shown in Table 47, Table 48: "BLE Current Consumption," on page 157, and Table 49: "FM Current Consumption," on page 157, respectively.

Note:

- The WLAN core is in reset (WL_REG_ON = low) for all measurements provided in Table 47.
- For FM measurements, the Bluetooth core is in Sleep mode.
- The BT current consumption numbers are measured based on GFSK Tx output power = 13 dBm. The BLE current consumption numbers are measured based on a 10 dBm Tx output power.

Table 47: BT Current Consumption

Parameters	*Typical (VBAT = 3.6V)*	*Typical (VIO = 1.8V)*	*Unit*
HCI Mode	3.450	0.010	mA
Sleep with Ext LPO	0.009	0.082	mA
Reset	0.007	0.005	mA
Standard 1.28s Inquiry Scan	0.158	0.081	mA
Standard 2.56s Inquiry Scan	0.078	0.084	mA
Standard R1 Page and 1.28s Inquiry Scan	0.284	0.081	mA
Standard R1 Page and 2.56s Inquiry Scan	0.221	0.081	mA
Standard R2 Page and 2.56s Inquiry Scan	0.147	0.084	mA
500ms Sniff Att = 4 Master	0.126	0.084	mA
500ms Sniff Att = 4 Slave	0.108	0.084	mA
DM1DH1 Master TXRX	22.760	0.021	mA
DM1DH1 Slave TXRX	22.600	0.022	mA
DM3DH3 Master TXRX	28.149	0.031	mA
DM3DH3 Slave TXRX	27.900	0.032	mA
DM5DH5 Master TXRX	28.852	0.035	mA
DM5DH5 Slave TXRX	28.377	0.034	mA
3DH53DH1 Master TXRX	26.430	0.086	mA
3DH53DH1 Slave TXRX	26.234	0.086	mA
3DH53DH1 TX Master	28.843	0.028	mA
3DH53DH1 TX Slave	32.567	0.029	mA
3DH53DH1 RX Master	13.829	0.116	mA
3DH53DH1 RX Slave	13.753	0.117	mA
HV3 Master	10.391	0.041	mA
HV3 Slave	7.156	0.040	mA

Table 47: BT Current Consumption (Cont.)

Parameters	Typical (VBAT = 3.6V)	Typical (VIO = 1.8V)	Unit
HV3 Master R1 Page and 1.28s Inquiry Scan	10.635	0.041	mA
HV3 Slave R1 Page and 1.28s Inquiry Scan	7.835	0.040	mA
HV3 Master R1 Page and 2.56s Inquiry Scan	10.591	0.041	mA
HV3 Slave R1 Page and 2.56s Inquiry Scan	7.659	0.040	mA

Table 48: BLE Current Consumption

Parameter	Typical	Typical (VIO = 1.8V)	Unit
Adv - Unconnectable 1.00 sec	0.053	0.088	mA
Adv - Unconnectable 1.28 sec	0.041	0.087	mA
Adv - Unconnectable 2.00 sec	0.034	0.090	mA
Adv - Connectable 20 msec	1.876	0.089	mA
Scan 1.28 sec	0.150	0.087	mA
Connected 7.5 ms	3.002	0.012	mA
Connected 1 sec	0.153	0.088	mA
Connected 1.28 sec	0.148	0.087	mA
Connected 2 sec	0.138	0.088	mA

Table 49: FM Current Consumption

Parameter	Power	Typical (VBAT = 3.6V)	Typical (VIO = 1.8V)	Unit
FMRX: FM only and digital (I^2S) audio only	–47 dBm	6.198	0.220	mA
FMRX: FM + RDS and digital (I^2S) audio only	–	6.197	0.220	mA

Section 21: Interface Timing and AC Characteristics

SDIO/gSPI Timing

SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 42 and Table 50.

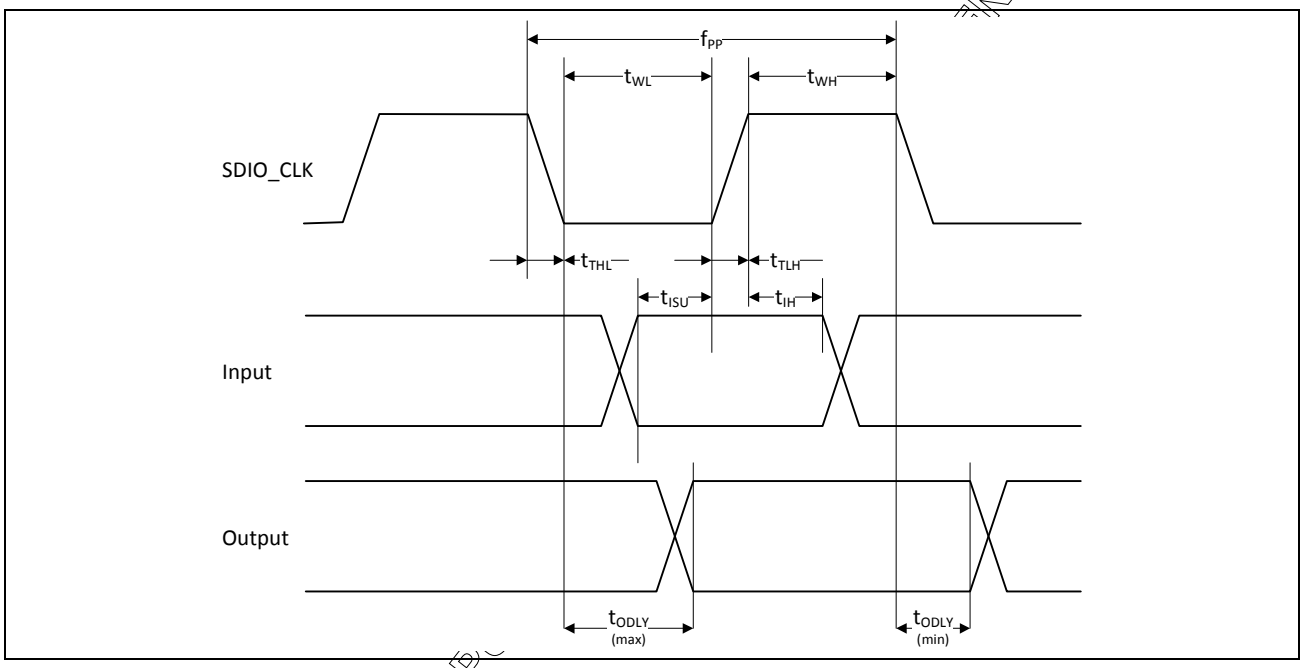


Figure 42: SDIO Bus Timing (Default Mode)

Table 50: SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns

Table 50: SDIO Bus Timing[a] Parameters (Default Mode) (Cont.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 43 and Table 51.

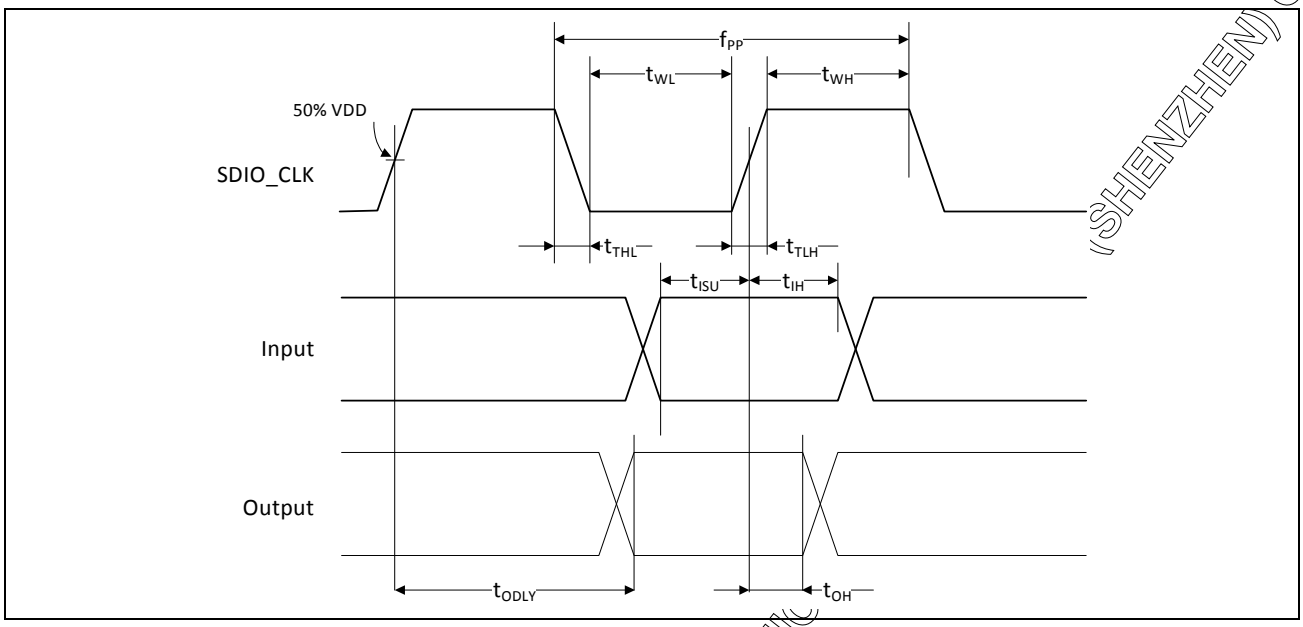


Figure 43: SDIO Bus Timing (High-Speed Mode)

Table 51: SDIO Bus Timing[a] Parameters (High-Speed Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO Bus Timing Specifications in SDR Modes

Clock Timing

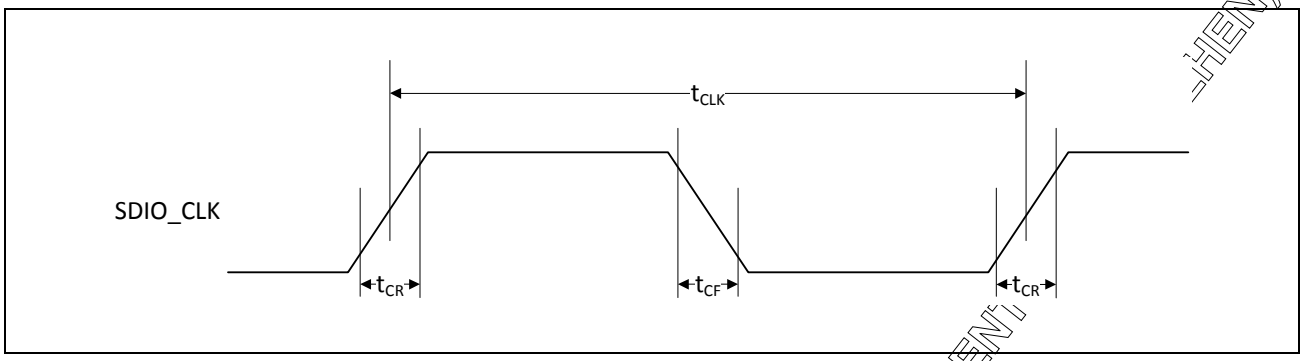


Figure 44: SDIO Clock Timing (SDR Modes)

Table 52: SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30	70	%	–

Card Input Timing

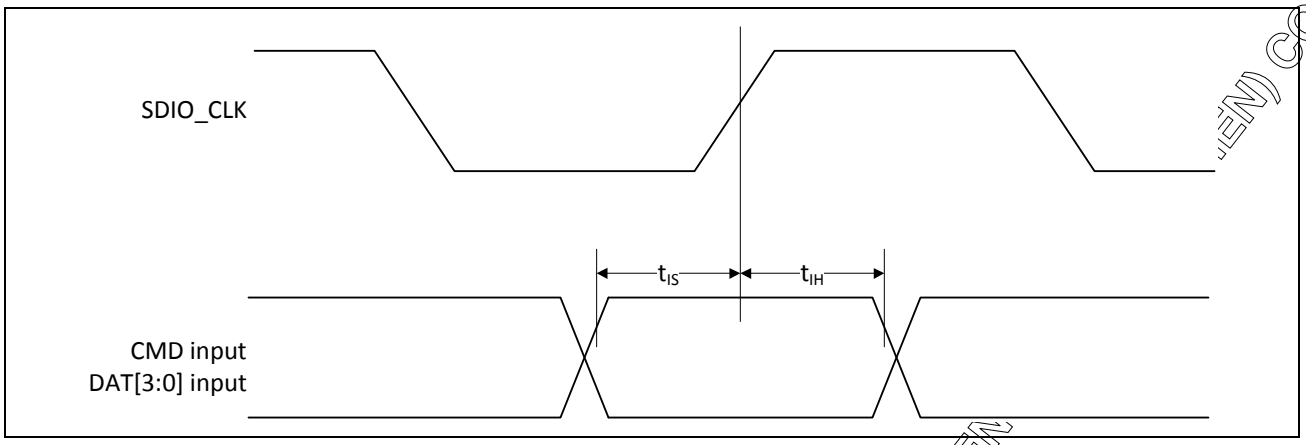


Figure 45: SDIO Bus Input Timing (SDR Modes)

Table 53: SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	*Minimum*	*Maximum*	*Unit*	*Comments*
SDR104 Mode				
t_{IS}	1.70[a]	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

a. SDIO 3.0 specification value is 1.40 ns.

Card Output Timing

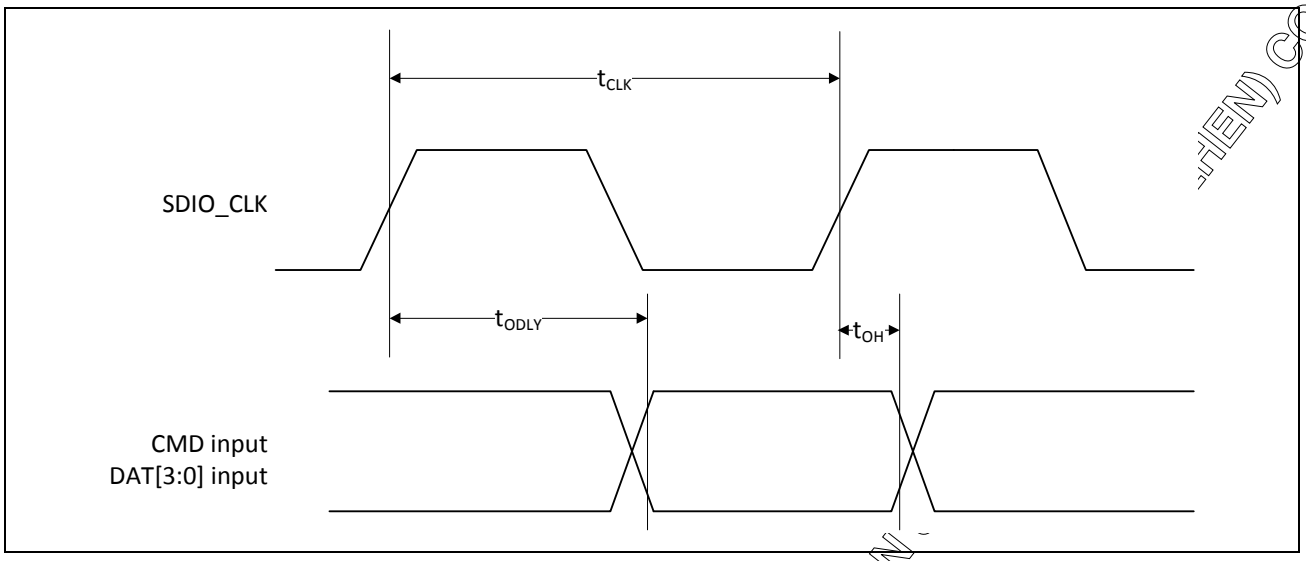


Figure 46: SDIO Bus Output Timing (SDR Modes up to 100 MHz)

Table 54: SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	*Minimum*	*Maximum*	*Unit*	*Comments*
t_{ODLY}	–	7.85[a]	ns	t_{CLK} ≥ 10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

a. SDIO 3.0 specification value is 7.5 ns.

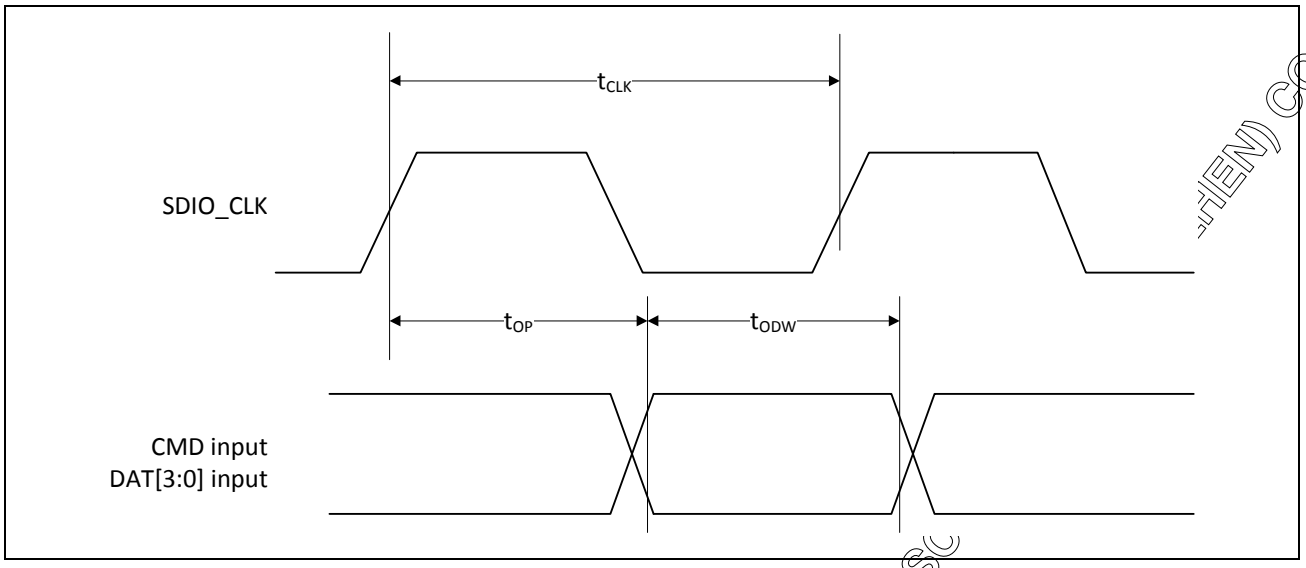


Figure 47: SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

Table 55: SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	*Minimum*	*Maximum*	*Unit*	*Comments*
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20 to +125 degrees during operation

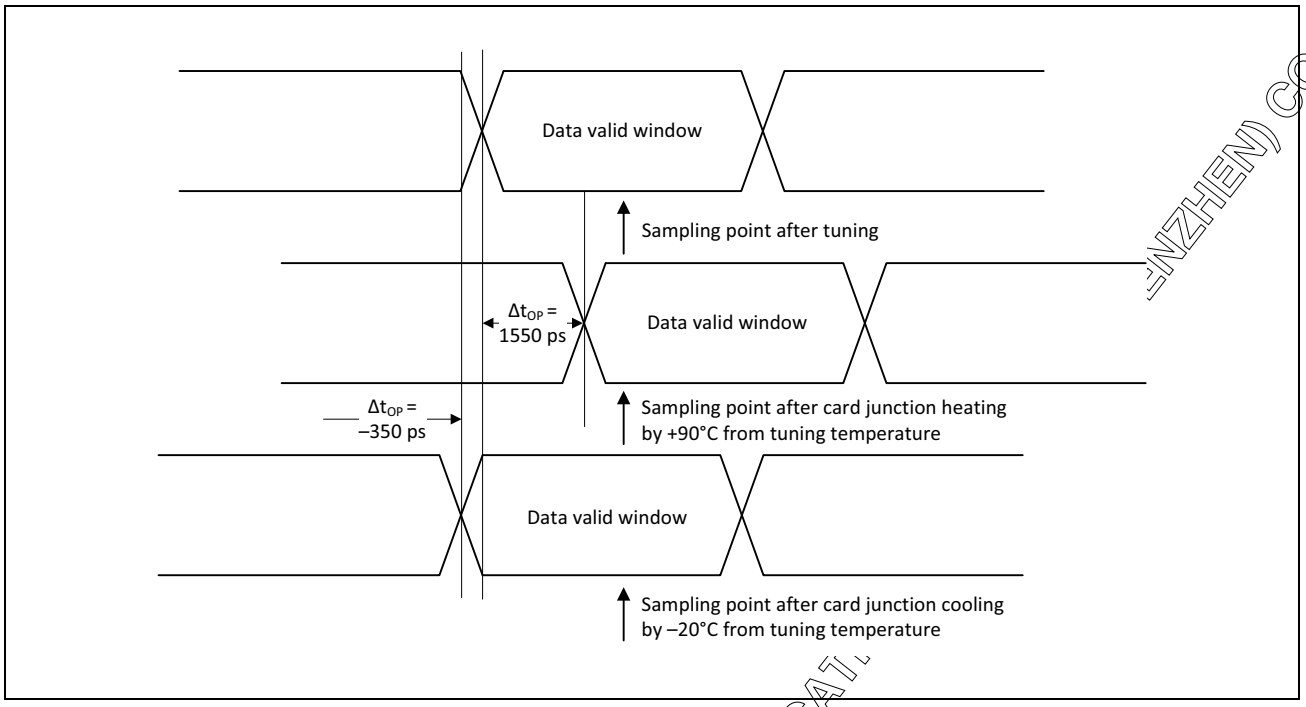


Figure 48: Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

SDIO Bus Timing Specifications in DDR50 Mode

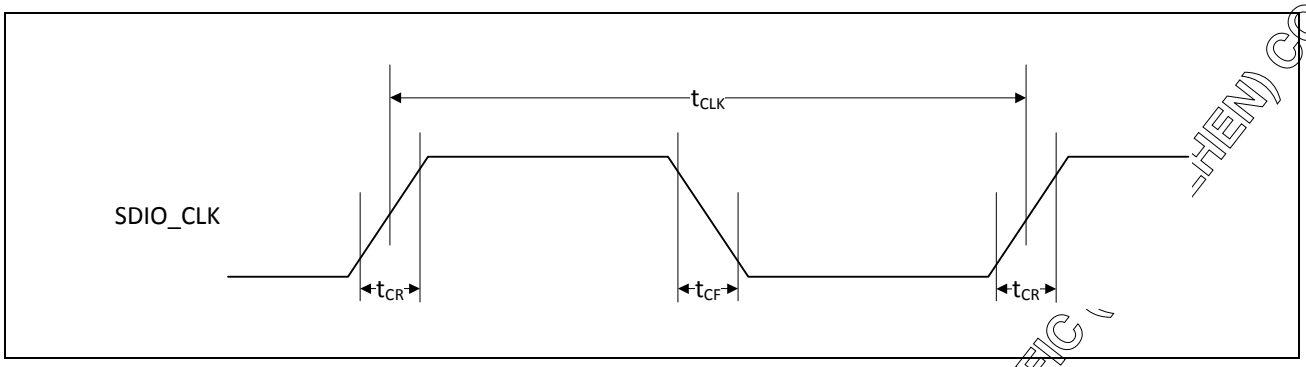


Figure 49: SDIO Clock Timing (DDR50 Mode)

Table 56: SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45	55	%	–

Data Timing

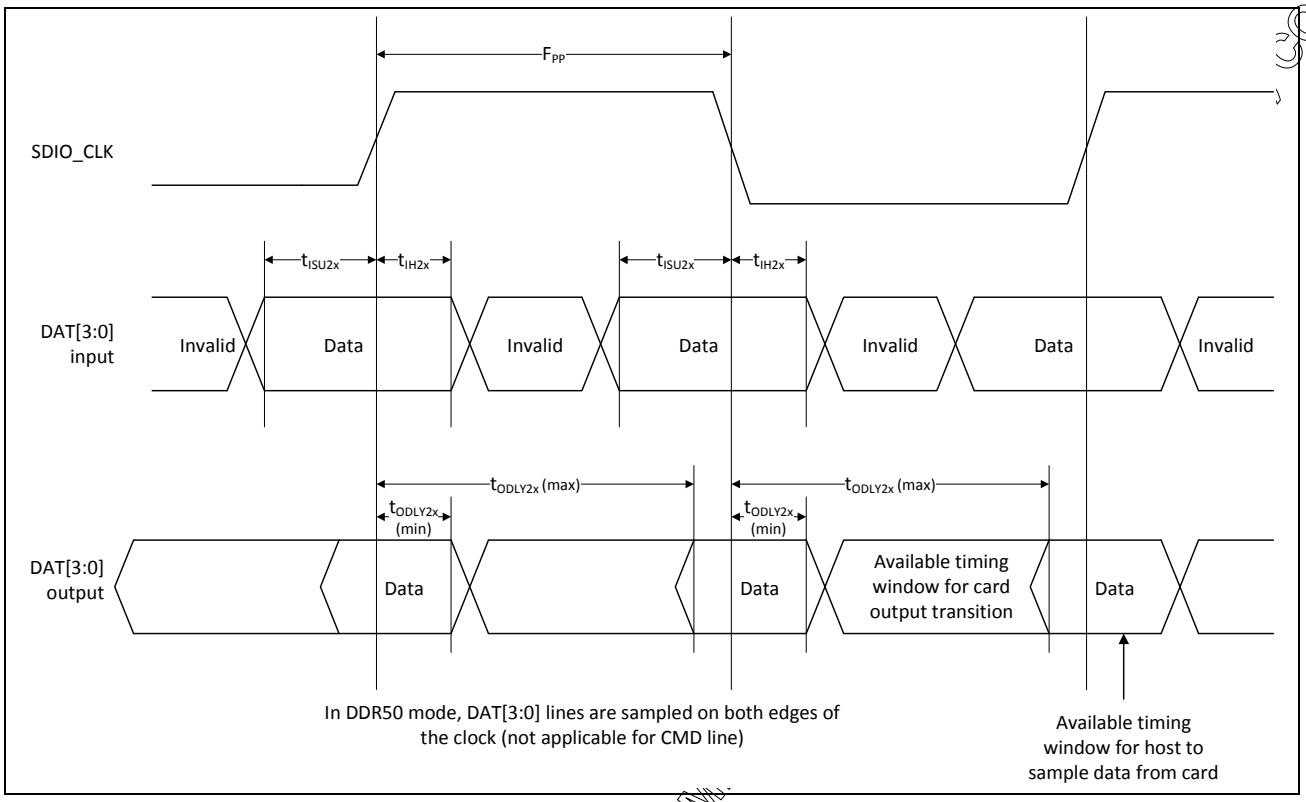


Figure 50: SDIO Data Timing (DDR50 Mode)

Table 57: SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.85[a]	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15pF (1 Card)

a. SDIO 3.0 specification value is 7.0 ns.

gSPI Signal Timing

The gSPI host and device always use the rising edge of clock to sample data.

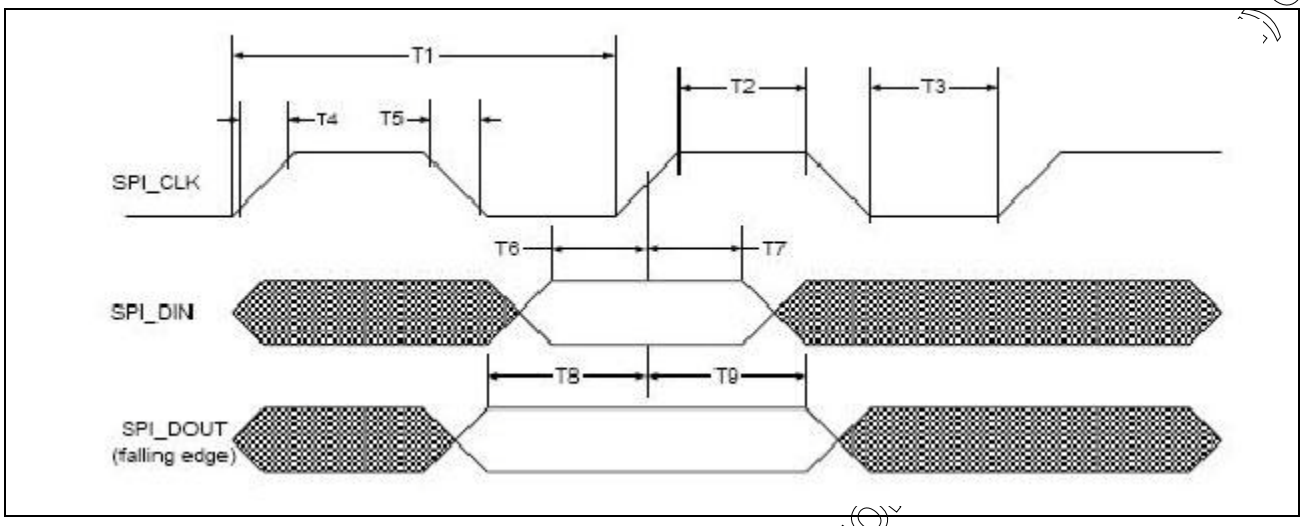


Figure 51: gSPI Timing

Table 58: gSPI Timing Parameters

Parameter	*Symbol*	*Minimum*	*Maximum*	*Units*	*Note*
Clock period	T1	20.8	–	ns	F_{max} = 48 MHz
Clock high/low	T2/T3	(0.45 × T1) – T4	(0.55 × T1) – T4	ns	–
Clock rise/fall time[a]	T4/T5	–	2.5	ns	Measured from 10% to 90% of VDDIO
Input setup time	T6	5.0	–	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	5.0	–	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	–	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	–	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock[b]	–	7.86	–	ns	CSX fall to 1st rising edge
Clock to CSX[a]	–	–	–	ns	Last falling edge to CSX high

a. Limit applies when SPI_CLK = Fmax. For slower clock speeds, longer rise/fall times are acceptable provided that the transitions are monotonic.
b. SPI_CSx remains active for entire duration of gSPI read/write/write-read transaction (overall words for multiple-word transaction)

HSIC Interface Specifications

Table 59: HSIC Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Comments
HSIC signaling voltage	V_{DD}	1.1	1.2	1.3	V	–
I/O voltage input low	V_{IL}	–0.3	–	$0.35 \times V_{DD}$	V	–
I/O Voltage input high	V_{IH}	$0.65 \times V_{DD}$	–	$V_{DD} + 0.3$	V	–
I/O voltage output low	V_{OL}	–	–	$0.25 \times V_{DD}$	V	–
I/O voltage output high	V_{OH}	$0.75 \times V_{DD}$	–	–	V	–
I/O pad drive strength	O_D	40	–	60	Ω	Controlled output impedance driver
I/O weak keepers	I_L	20	–	70	mA	–
I/O input impedance	Z_I	100	–	–	kΩ	–
Total capacitive load[a]	C_L	3	–	14	pF	–
Characteristic trace impedance	T_I	45	50	55	Ω	–
Circuit board trace length	T_L	–	–	10	cm	–
Circuit board trace propagation skew[b]	T_S	–	–	15	ps	–
STROBE frequency[c]	F_{STROBE}	239.988	240	240.012	MHz	± 500 ppm
Slew rate (rise and fall) STROBE and DATA[c]	T_{slew}	$0.60 \times V_{DD}$	1.0	1.2	V/ns	Averaged from 30% ~ 70% points
Receiver data setup time (with respect to STROBE)[c]	T_s	300	–	–	ps	Measured at the 50% point
Receiver data hold time (with respect to STROBE)[c]	T_b	300	–	–	ps	Measured at the 50% point

a. Total Capacitive Load (C_L), includes device Input/Output capacitance, and capacitance of a 50Ω PCB trace with a length of 10 cm.
b. Maximum propagation delay skew in STROBE or DATA with respect to each other. The trace delay should be matched between STROBE and DATA to ensure that the signal timing is within specification limits at the receiver.
c. Jitter and duty cycle are not separately specified parameters, they are incorporated into the values in the table above.

JTAG Timing

Table 60: JTAG Timing Characteristics

Signal Name	*Period*	*Output Maximum*	*Output Minimum*	*Setup*	*Hold*
TCK	125 ns	–	–	–	
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

Section 22: Power-Up Sequence and Timing

Sequencing of Reset and Regulator Control Signals

The BCM43241 has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 52, Figure 53 on page 172, and Figure 54 and Figure 55 on page 173). The timing values indicated are minimum required values; longer delays are also acceptable.

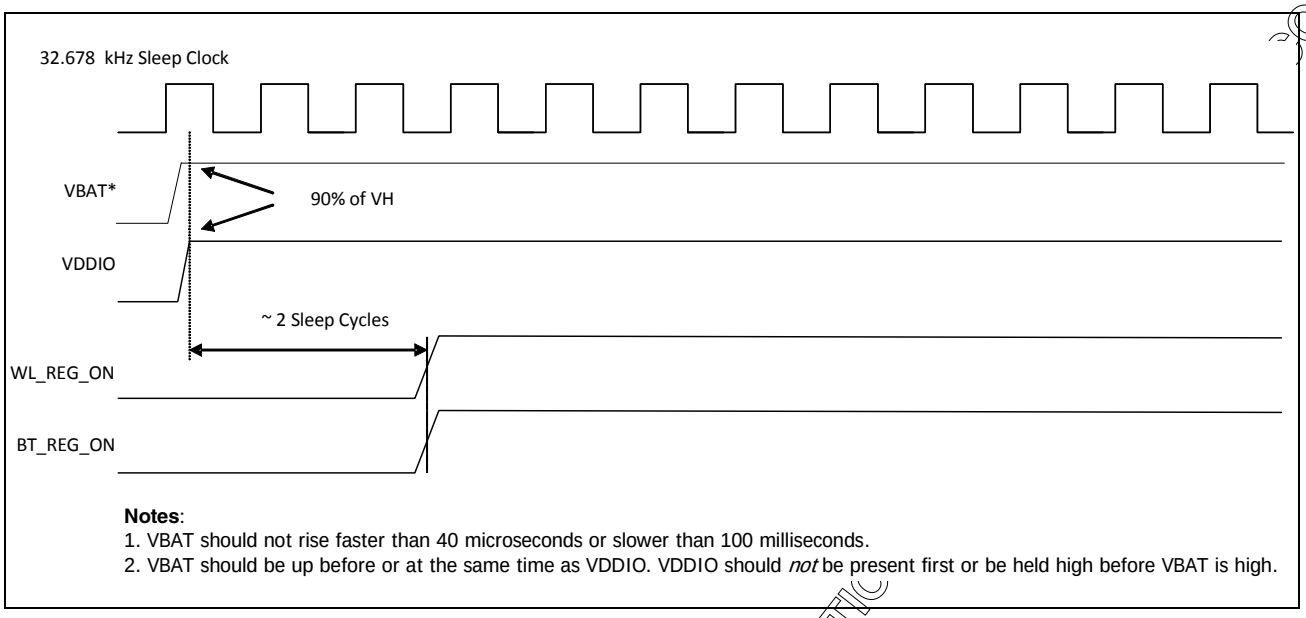
Note:

- The WL_REG_ON and BT_REG_ON signals are ORed in the BCM43241. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the BCM43241 regulators.
- The reset requirements for the Bluetooth core are also applicable for the FM core. In other words, if FM is to be used, then the Bluetooth core must be enabled.
- The BCM43241 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the 0.6V threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

Description of Control Signals

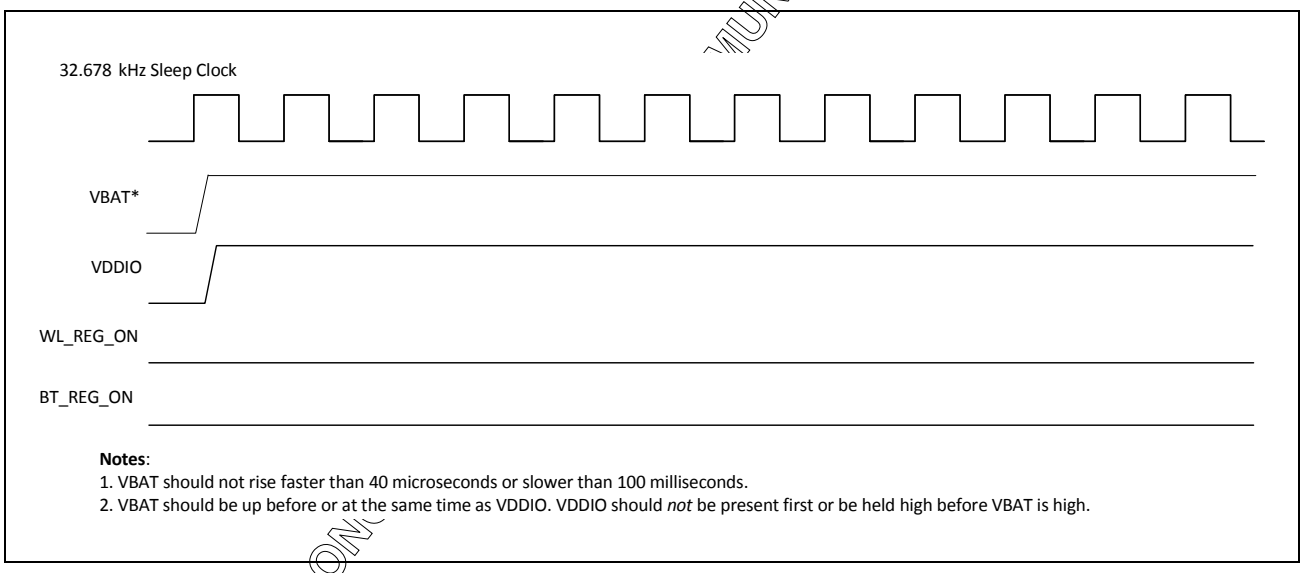
- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM43241 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal BCM43241 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Control Signal Timing Diagrams



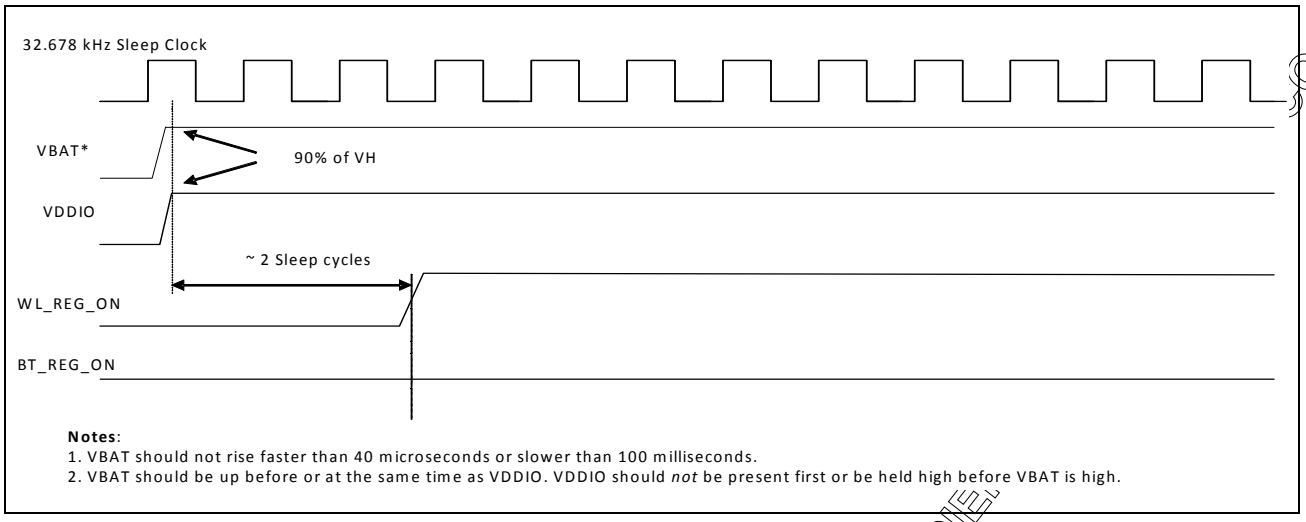
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should *not* be present first or be held high before VBAT is high.

Figure 52: WLAN = ON, Bluetooth = ON



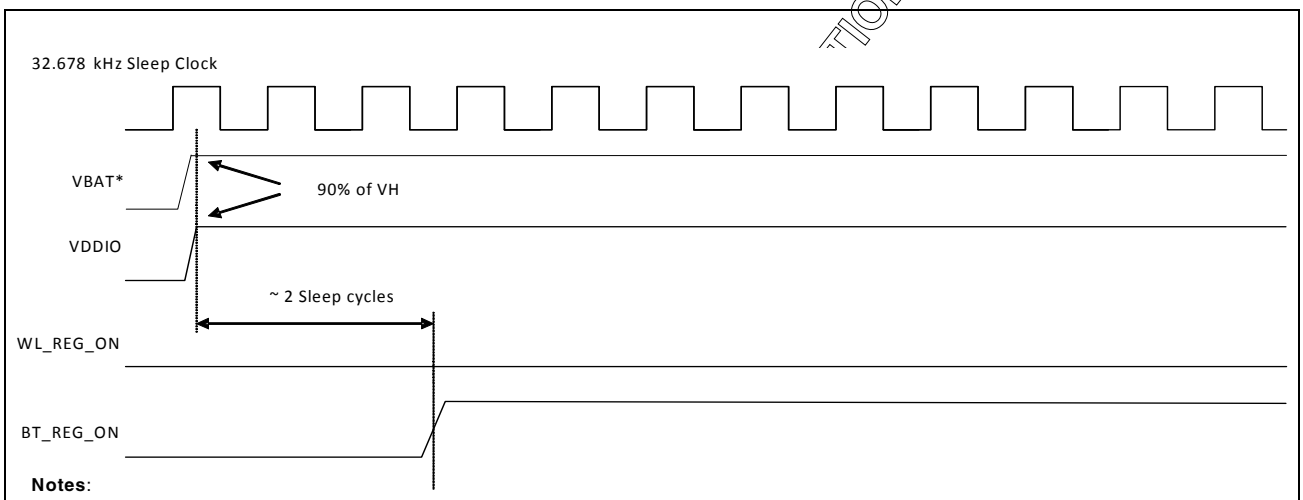
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should *not* be present first or be held high before VBAT is high.

Figure 53: WLAN = OFF, Bluetooth = OFF



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should *not* be present first or be held high before VBAT is high.

Figure 54: WLAN = ON, Bluetooth = OFF



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should *not* be present first or be held high before VBAT is high.

Figure 55: WLAN = OFF, Bluetooth = ON

Section 23: Package Information

Preliminary Package Thermal Characteristics

Table 61: Package JEDEC Thermal Characteristics[a]

Characteristic	*FCFBGA*	*WLCSP*
θ_{JA} (°C/W) (value in still air)	36.30	39.11
θ_{JB} (°C/W)	10.84	5.98
θ_{JC} (°C/W)	18.57	2.12
Ψ_{JT} (°C/W)	8.89	2.23
Ψ_{JB} (°C/W)	15.67	10.58
Maximum junction temperature T_j[b]	125	125
Maximum power dissipation (W)	1.66	1.66

a. No heat sink, TA = 55°C, P = 1.66W continuous dissipation.
b. Absolute junction temperature limits are maintained through active thermal monitoring and turning off one of the Tx chains.

Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

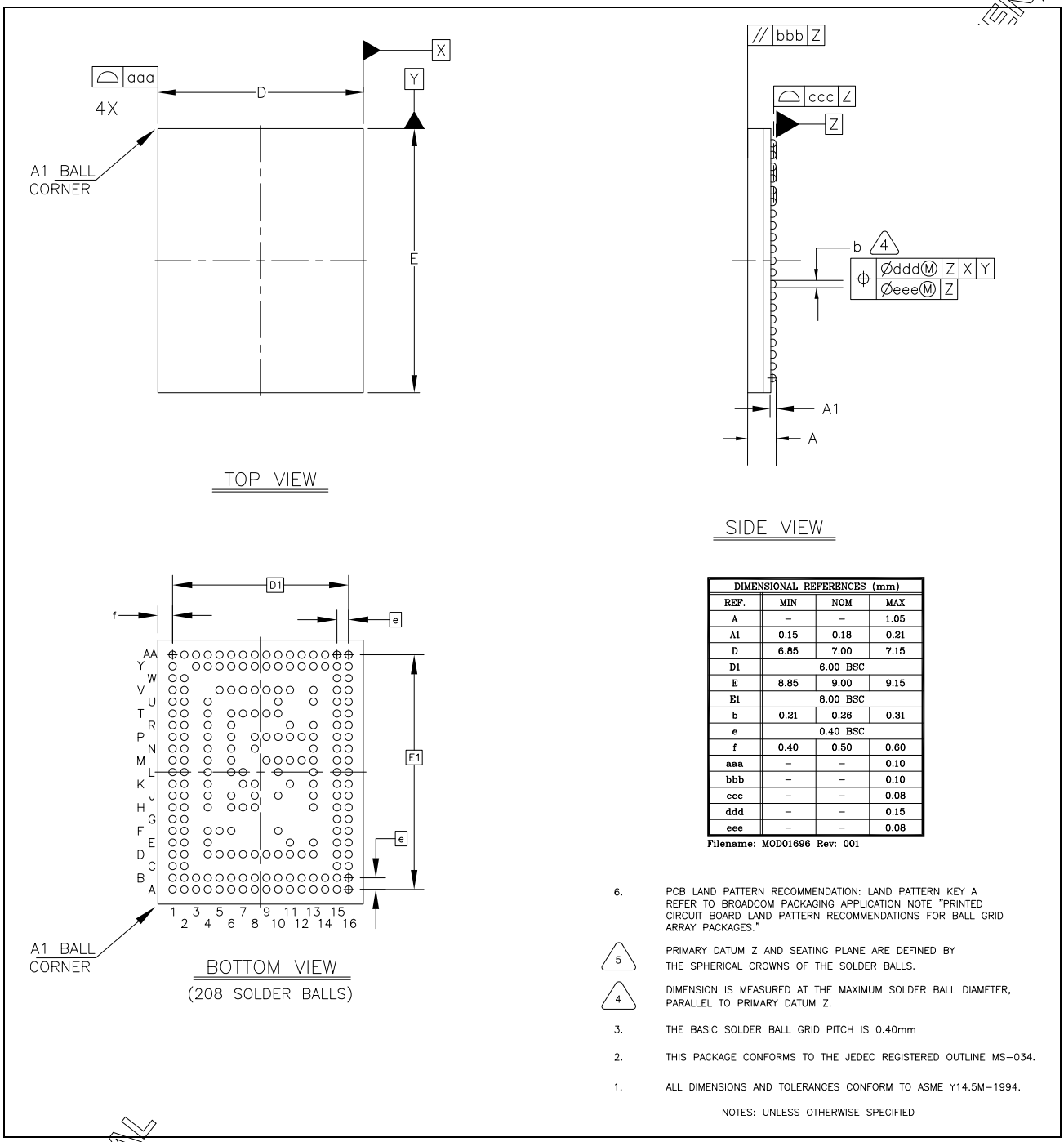
Where:

- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

Environmental Characteristics

For environmental characteristics data, see Table 26: “Environmental Ratings,” on page 118.

Section 24: Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.05
A1	0.15	0.18	0.21
D	6.85	7.00	7.15
D1		6.00 BSC	
E	8.85	9.00	9.15
E1		8.00 BSC	
b	0.21	0.26	0.31
e		0.40 BSC	
f	0.40	0.50	0.60
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD01696 Rev: 001

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

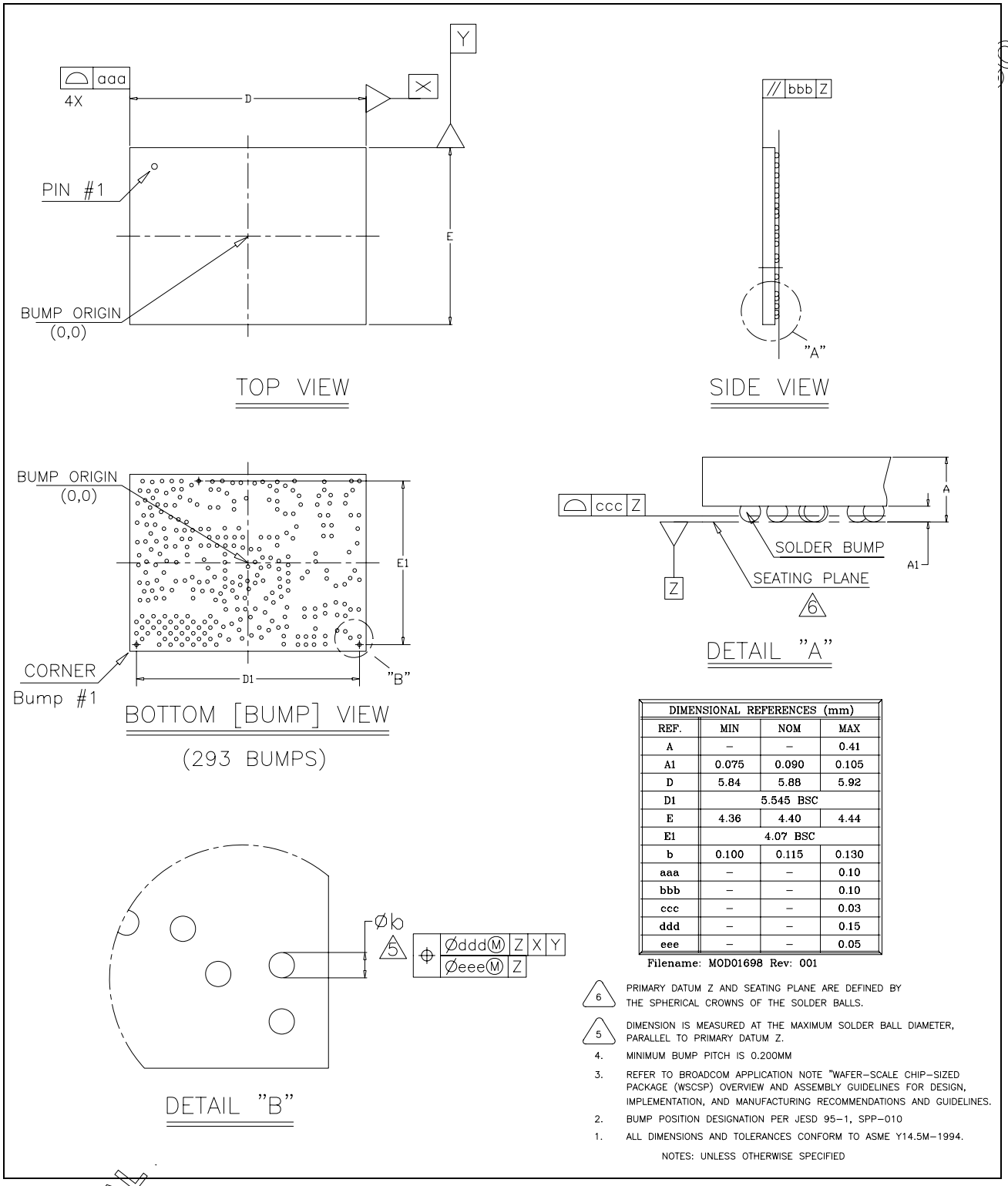
3. THE BASIC SOLDER BALL GRID PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MS-034.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 56: 208-Ball FCFBGA Package Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.41
A1	0.075	0.090	0.105
D	5.84	5.88	5.92
D1		5.545 BSC	
E	4.36	4.40	4.44
E1		4.07 BSC	
b	0.100	0.115	0.130
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD01698 Rev: 001

6 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

4. MINIMUM BUMP PITCH IS 0.200MM
3. REFER TO BROADCOM APPLICATION NOTE "WAFER-SCALE CHIP-SIZED PACKAGE (WSCSP) OVERVIEW AND ASSEMBLY GUIDELINES FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.
2. BUMP POSITION DESIGNATION PER JESD 95-1, SPP-010
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 57: 293-Bump WLCSP Package Mechanical Information

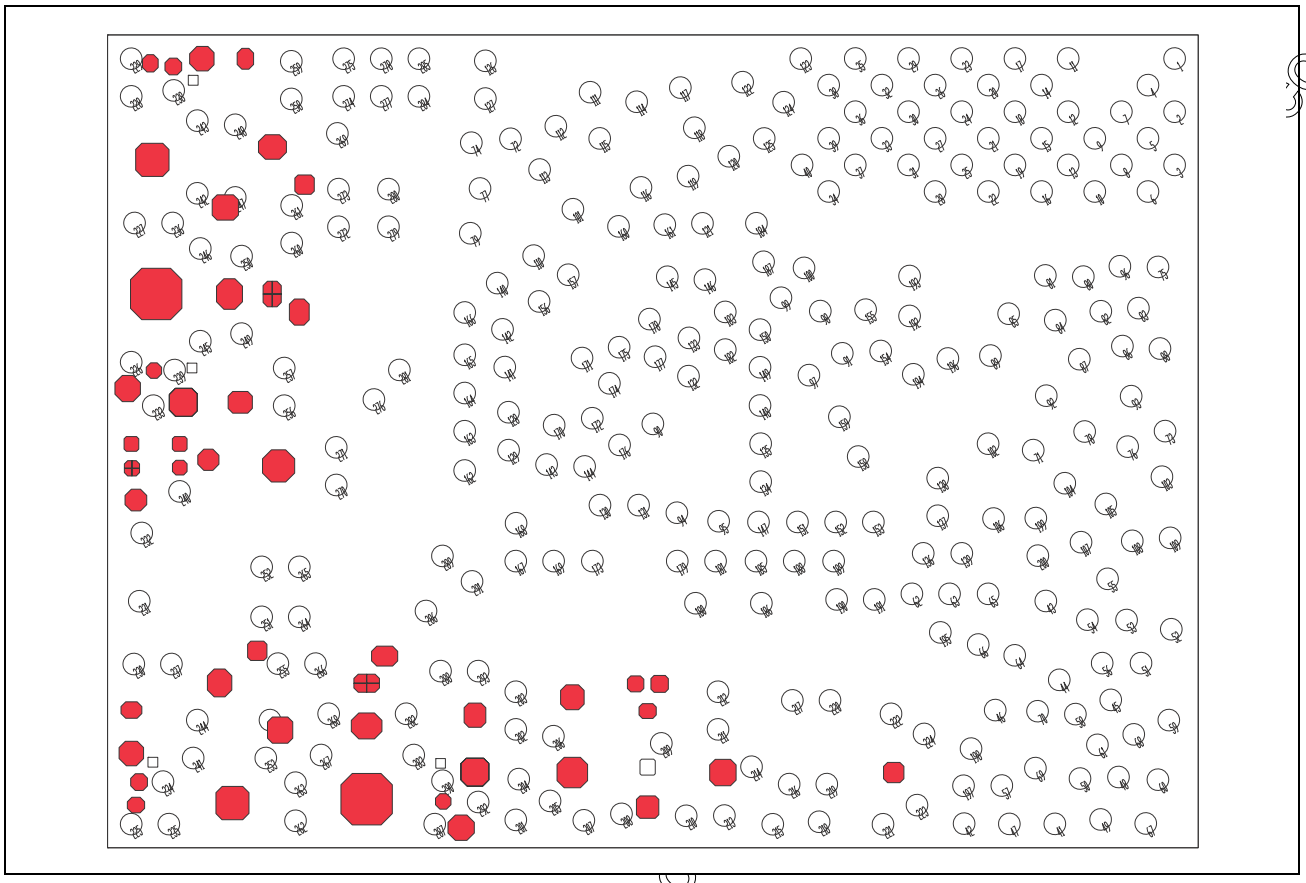


Figure 58: WLCSP Keep-Out Areas for PCB Layout — Bumps Facing Up

Note: No top-layer metal is allowed in keep-out areas.

Section 25: Ordering Information

Part Number	*Package*	*Description*	*Operating Ambient Temperature*
BCM43241FKFFBG	FCFBGA (7.00 mm x 9.00 mm, 0.4 mm pitch)	Single-band 2.4 GHz WLAN + BT 4.0 + FM Rx	–30°C to +85°C
BCM43241FKWBG	WLCSP (5.88 mm x 4.40 mm, 0.2 mm pitch)	Single-band 2.4 GHz WLAN + BT 4.0 + FM Rx	–30°C to +85°C
BCM43241GKFFBG	FCFBGA (7.00 mm x 9.00 mm, 0.4 mm pitch)	Single-band 2.4 GHz WLAN + BT 4.0	–30°C to +85°C
BCM43241GKWBG	WLCSP (5.88 mm x 4.40 mm, 0.2 mm pitch)	Single-band 2.4 GHz WLAN + BT 4.0	–30°C to +85°C
BCM43241XKFFBG	FCFBGA (7.00 mm x 9.00 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.0 + FM	–30°C to +85°C
BCM43241XKWBG	WLCSP (5.88 mm x 4.40 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.0 + FM	–30°C to +85°C
BCM43241DKFFBG	FCFBGA (7.00 mm x 9.00 mm, 0.4 mm pitch)	Dual-band WLAN + BT 4.0	–30°C to +85°C
BCM43241DKWBG	WLCSP (5.88 mm x 4.40 mm, 0.2 mm pitch)	Dual-band WLAN + BT 4.0	–30°C to +85°C
BCM43241ZKFFBG	FCFBGA (7.00 mm x 9.00 mm, 0.4 mm pitch)	Dual-band WLAN	–30°C to +85°C
BCM43241ZKWBG	WLCSP (5.88 mm x 4.40 mm, 0.2 mm pitch)	Dual-band WLAN	–30°C to +85°C

Section 26: Pin List

This section presents the pin list for the BCM43241 device:

Table 62: 293-Bump WLCSP Package Pin List By Pin Number

Bump	Name
1	SR_PVSS
2	SR_PVSS
3	SR_PVSS
4	SR_PVSS
5	SR_PVSS
6	SR_VLX
7	SR_VLX
8	SR_VLX
9	SR_VLX
10	SR_VLX
11	SR_VDDBATP5V
12	SR_VDDBATP5V
13	SR_VLX
14	SR_VDDBATP5V
15	PMU_AVSS
16	SR_VLX
17	SR_VDDBATA5V
18	SR_VDDBATP5V
19	PMU_AVSS
20	SR_VDDBATA5V
21	VOUT_LDO3P3
22	VOUT_LDO3P3
23	LDO_VDD1P5
24	VOUT_CLDO
25	VOUT_CLDO
26	VOUT_LNLDO1
27	VOUT_LNLDO1
28	VOUT_CLDO
29	LDO_VDD1P5
30	VOUT_LNLDO2
31	VOUT_LNLDO1
32	LDO_VDD1P5
33	VOUT_LNLDO2
34	VDDIO_PMU
35	LDO_VDD1P5
36	LDO_VDD1P5
37	WLREG_ON
38	VOUT_HSICAVDD
39	LDO_VDD1P5
40	BTREG_ON
41	BT_CLK_REQ
42	BT_DEV_WAKE
43	BT_GPIO_2
44	BT_GPIO_3
45	BT_GPIO_4
46	BT_GPIO_5
47	BT_HOST_WAKE
48	BT_I2S_CLK
49	BT_I2S_DI
50	BT_I2S_DO
51	BT_I2S_WS
52	BT_LPO_IN
53	BT_PCM_CLK
54	BT_PCM_IN
55	BT_PCM_OUT
56	BT_PCM_SYNC

Bump	Name
57	BT_TM1
58	BT_UART_CTS_N
59	BT_UART_RTS_N
60	BT_UART_RXD
61	BT_UART_TXD
62	BT_VDDC
63	BT_VDDC
64	BT_VDDC
65	BT_VDDC
66	BT_VDDC
67	BT_VDDC_ISO_1
68	BT_VDDC_ISO_2
69	BT_VDDO
70	BT_VDDO
71	AMODE_EXT_LNA_PU_CORE0
72	AMODE_EXT_LNA_PU_CORE1
73	AMODE_PA_EN_CORE0
74	AMODE_PA_EN_CORE1
75	EXT_XTAL_PU
76	GMODE_EXT_LNA_PU_CORE0
77	GMODE_EXT_LNA_PU_CORE1
78	GMODE_PA_EN_CORE0
79	GMODE_PA_EN_CORE1
80	GPIO_0
81	GPIO_1
82	GPIO_2
83	GPIO_3
84	GPIO_4
85	GPIO_5
86	GPIO_6
87	GPIO_7
88	GPIO_8
89	GPIO_9
90	GPIO_10
91	GPIO_11
92	GPIO_12
93	GPIO_13
94	GPIO_14

Bump	Name
95	GPIO_15
96	JTAG_SEL
97	OTP_VDD33
98	PACKAGEOPTION_0
99	PACKAGEOPTION_1
100	PACKAGEOPTION_2
101	PALDO_PU
102	RF_SW_CTRL_0
103	RF_SW_CTRL_1
104	RF_SW_CTRL_2
105	RF_SW_CTRL_3
106	RF_SW_CTRL_4
107	RF_SW_CTRL_5
108	RF_SW_CTRL_6
109	RF_SW_CTRL_7
110	RF_SW_CTRL_8
111	RF_SW_CTRL_9
112	RF_SW_CTRL_10
113	RF_SW_CTRL_11
114	SDIO_CLK
115	SDIO_CMD
116	SDIO_DATA_0
117	SDIO_DATA_1
118	SDIO_DATA_2
119	SDIO_DATA_3
120	HSIC_AVDD12PLL
121	HSIC_AGND12PLL
122	HSIC_DATA
123	HSIC_RREFHSIC
124	HSIC_STROBE
125	DVDD12HSIC
126	AVDD_BBPLL
127	AVSS_BBPLL
128	VDD
129	VDD
130	VDD
131	VDD
132	VDD

Bump	Name
133	VDD
134	VDD
135	VDD
136	VDD
137	VDD
138	VDD
139	VDD
140	VDD
141	VDD
142	VDD
143	VDD
144	VDD
145	VDD
146	VDD
147	VDD
148	VDD
149	VDD
150	VDD
151	VDD
152	VDD
153	VDD
154	VDDIO
155	VDDIO
156	VDDIO_RF
157	VDDIO_RF
158	VDDIO_RF
159	VDDIO_RF
160	VDDIO_SD
161	VDDIO_SD
162	VSS
163	VSS
164	VSS
165	VSS
166	VSS
167	VSS
168	VSS
169	VSS
170	VSS

Bump	Name
171	VSS
172	VSS
173	VSS
174	VSS
175	VSS
176	VSS
177	VSS
178	VSS
179	VSS
180	VSS
181	VSS
182	VSS
183	VSS
184	VSS
185	VSS
186	VSS
187	VSS
188	VSS
189	VSS
190	VSS
191	VSS
192	VSS
193	VSS
194	VSS
195	VSS
196	VSS
197	VSS
198	VSS
199	VSS
200	VSS
201	BT_VBAT
202	BT_IFVDD
203	BT_IFVSS
204	BT_LDO_OUT
205	BT_PAVDD
206	BT_PALDO_VSS
207	BT_RF
208	BT_PAVSS

Bump	Name
209	BT_LNAVSS
210	BT_LNAVDD
211	BT_PLLVDD
212	BT_PLLVSS
213	BT_VCOVDD
214	BT_VCOVSS
215	FM_RFAUX
216	FM_LNAVSS
217	FM_IFVSS
218	FM_RFIN
219	FM_LNAVDD
220	FM_IFVDD
221	FM_VCOVSS
222	FM_PLLVDD
223	FM_VCOVDD
224	FM_PLLVSS
225	WRF_RFIN_5G_CORE0
226	WRF_PAOUT_2G_CORE1
227	WRF_PA_VDD3P3_CORE1
228	WRF_PAOUT_5G_CORE1
229	WRF_RFIN_5G_CORE1
230	WRF_RX5G_GND1P2_CORE0
231	WRF_GPIO_OUT
232	WRF_VCO_VDD1P2
233	WRF_RFIN_2G_CORE1
234	WRF_LNA_5G_GND1P2_CORE0
235	WRF_PAOUT_5G_CORE0
236	WRF_PA_VDD3P3_CORE1
237	WRF_RX5G_VDD1P2_CORE0
238	WRF_LNA_5G_GND1P2_CORE1
239	WRF_LNA_2G_GND1P2_CORE1
240	WRF_VCO_GND1P2
241	WRF_PA5G_GND3P3_CORE0
242	WRF_PA5G_GND3P3_CORE1
243	WRF_PA5G_GND3P3_CORE1
244	WRF_PADRV5G_VDD3P3_CORE0
245	WRF_PA2G_GND3P3_CORE1
246	WRF_PA2G_GND3P3_CORE1

Bump	Name
247	WRF_PADRV5G_GND3P3_CORE1
248	WRF_PADRV5G_VDD3P3_CORE1
249	WRF_PADRV2G_GND3P3_CORE1
250	WRF_PADRV2G_VDD3P3_CORE1
251	WRF_A_TSSI_IN_CORE0
252	WRF_AFE_VDD1P2_CORE0
253	WRF_PA5G_GND3P3_CORE0
254	WRF_PADRV5G_GND3P3_CORE0
255	WRF_TX_GND1P2_CORE0
256	WRF_RX2G_GND1P2_CORE1
257	WRF_RX2G_VDD1P2_CORE1
258	WRF_RX5G_VDD1P2_CORE1
259	WRF_RX5G_GND1P2_CORE1
260	WRF_TX_VDD1P2_CORE1
261	WRF_TX_GND1P2_CORE1
262	WRF_PA_VDD3P3_CORE0
263	WRF_PA_VDD3P3_CORE0
264	WRF_G_TSSI_IN_CORE0
265	WRF_AFE_GND1P2_CORE0
266	WRF_TX_VDD1P2_CORE0
267	WRF_PA2G_GND3P3_CORE0
268	WRF_PADRV2G_VDD3P3_CORE0
269	WRF_VCO_GND1P2
270	WRF_SYNTH_VDD1P2
271	WRF_SYNTH_GND1P2
272	WRF_G_TSSI_IN_CORE1
273	WRF_A_TSSI_IN_CORE1
274	WRF_XTAL_CAB_VDD1P2
275	WRF_XTAL_CAB_GND1P2
276	WRF_AFE_VDD1P2_CORE1
277	WRF_TCXO_VDD1P8
278	WRF_XTAL_CAB_XOP
279	WRF_AFE_GND1P2_CORE1
280	WRF_AFE_VDD1P2_CORE1
281	WRF_AFE_GND1P2_CORE1
282	WRF_PADRV2G_GND3P3_CORE0
283	WRF_PA2G_GND3P3_CORE0
284	WRF_TCXO_CKIN2V

Bump	Name
285	WRF_XTAL_CAB_XON
286	WRF_VCO_GND1P2
287	WRF_PAOUT_2G_CORE0
288	WRF_RX2G_VDD1P2_CORE0
289	WRF_AFE_GND1P2_CORE0
290	WRF_LNA_2G_GND1P2_CORE0
291	WRF_AFE_VDD1P2_CORE0
292	WRF_RFIN_2G_CORE0
293	WRF_RX2G_GND1P2_CORE0

Table 63: 293-Bump WLCSP Package Pin List By Pin Name

Name	Bump
AMODE_EXT_LNA_PU_CORE0	71
AMODE_EXT_LNA_PU_CORE1	72
AMODE_PA_EN_CORE0	73
AMODE_PA_EN_CORE1	74
AVDD_BBPLL	126
AVSS_BBPLL	127
BT_CLK_REQ	41
BT_DEV_WAKE	42
BT_GPIO_2	43
BT_GPIO_3	44
BT_GPIO_4	45
BT_GPIO_5	46
BT_HOST_WAKE	47
BT_I2S_CLK	48
BT_I2S_DI	49
BT_I2S_DO	50
BT_I2S_WS	51
BT_IFVDD	202
BT_IFVSS	203
BT_LDO_OUT	204
BT_LNAVDD	210
BT_LNAVSS	209
BT_LPO_IN	52
BT_PALDO_VSS	206
BT_PAVDD	205
BT_PAVSS	208
BT_PCM_CLK	53
BT_PCM_IN	54
BT_PCM_OUT	55
BT_PCM_SYNC	56
BT_PLLVDD	211
BT_PLLVSS	212
BT_RF	207
BT_TM1	57
BT_UART_CTS_N	58
BT_UART_RTS_N	59
BT_UART_RXD	60
BT_UART_TXD	61
BT_VBAT	201
BT_VCOVDD	213
BT_VCOVSS	214
BT_VDDC	62
BT_VDDC	63
BT_VDDC	64
BT_VDDC	65
BT_VDDC	66
BT_VDDC_ISO_1	67
BT_VDDC_ISO_2	68
BT_VDDO	69
BT_VDDO	70
BTREG_ON	40
DVDD12HSIC	125
EXT_XTAL_PU	75
FM_IFVDD	220
FM_IFVSS	217
FM_LNAVDD	219
FM_LNAVSS	216
FM_PLLVDD	222
FM_PLLVSS	224
FM_RFAUX	215
FM_RFIN	218
FM_VCOVDD	223
FM_VCOVSS	221
GMODE_EXT_LNA_PU_CORE0	76
GMODE_EXT_LNA_PU_CORE1	77
GMODE_PA_EN_CORE0	78
GMODE_PA_EN_CORE1	79
GPIO_0	80
GPIO_1	81
GPIO_10	90
GPIO_11	91
GPIO_12	92
GPIO_13	93
GPIO_14	94

Name	Bump
GPIO_15	95
GPIO_2	82
GPIO_3	83
GPIO_4	84
GPIO_5	85
GPIO_6	86
GPIO_7	87
GPIO_8	88
GPIO_9	89
HSIC_AGND12PLL	121
HSIC_AVDD12PLL	120
HSIC_DATA	122
HSIC_RREFHSIC	123
HSIC_STROBE	124
JTAG_SEL	96
LDO_VDD1P5	23
LDO_VDD1P5	29
LDO_VDD1P5	32
LDO_VDD1P5	35
LDO_VDD1P5	36
LDO_VDD1P5	39
OTP_VDD33	97
PACKAGEOPTION_0	98
PACKAGEOPTION_1	99
PACKAGEOPTION_2	100
PALDO_PU	101
PMU_AVSS	15
PMU_AVSS	19
RF_SW_CTRL_0	102
RF_SW_CTRL_1	103
RF_SW_CTRL_10	112
RF_SW_CTRL_11	113
RF_SW_CTRL_2	104
RF_SW_CTRL_3	105
RF_SW_CTRL_4	106
RF_SW_CTRL_5	107
RF_SW_CTRL_6	108
RF_SW_CTRL_7	109

Name	Bump
RF_SW_CTRL_8	110
RF_SW_CTRL_9	111
SDIO_CLK	114
SDIO_CMD	115
SDIO_DATA_0	116
SDIO_DATA_1	117
SDIO_DATA_2	118
SDIO_DATA_3	119
SR_PVSS	1
SR_PVSS	2
SR_PVSS	3
SR_PVSS	4
SR_PVSS	5
SR_VDDBATA5V	17
SR_VDDBATA5V	20
SR_VDDBATP5V	11
SR_VDDBATP5V	12
SR_VDDBATP5V	14
SR_VDDBATP5V	18
SR_VLX	6
SR_VLX	7
SR_VLX	8
SR_VLX	9
SR_VLX	10
SR_VLX	13
SR_VLX	16
VDD	128
VDD	129
VDD	130
VDD	131
VDD	132
VDD	133
VDD	134
VDD	135
VDD	136
VDD	137
VDD	138
VDD	139

Name	Bump
VDD	140
VDD	141
VDD	142
VDD	143
VDD	144
VDD	145
VDD	146
VDD	147
VDD	148
VDD	149
VDD	150
VDD	151
VDD	152
VDD	153
VDDIO	154
VDDIO	155
VDDIO_PMU	34
VDDIO_RF	156
VDDIO_RF	157
VDDIO_RF	158
VDDIO_RF	159
VDDIO_SD	160
VDDIO_SD	161
VOUT_CLDO	24
VOUT_CLDO	25
VOUT_CLDO	28
VOUT_HSICAVDD	38
VOUT_LDO3P3	21
VOUT_LDO3P3	22
VOUT_LNLDO1	26
VOUT_LNLDO1	27
VOUT_LNLDO1	31
VOUT_LNLDO2	30
VOUT_LNLDO2	33
VSS	162
VSS	163
VSS	164
VSS	165

Name	Bump
VSS	166
VSS	167
VSS	168
VSS	169
VSS	170
VSS	171
VSS	172
VSS	173
VSS	174
VSS	175
VSS	176
VSS	177
VSS	178
VSS	179
VSS	180
VSS	181
VSS	182
VSS	183
VSS	184
VSS	185
VSS	186
VSS	187
VSS	188
VSS	189
VSS	190
VSS	191
VSS	192
VSS	193
VSS	194
VSS	195
VSS	196
VSS	197
VSS	198
VSS	199
VSS	200
WLREG_ON	37
WRF_A_TSSI_IN_CORE0	251
WRF_A_TSSI_IN_CORE1	273

Name	Bump
WRF_AFE_GND1P2_CORE0	265
WRF_AFE_GND1P2_CORE0	289
WRF_AFE_GND1P2_CORE1	279
WRF_AFE_GND1P2_CORE1	281
WRF_AFE_VDD1P2_CORE0	252
WRF_AFE_VDD1P2_CORE0	291
WRF_AFE_VDD1P2_CORE1	276
WRF_AFE_VDD1P2_CORE1	280
WRF_G_TSSI_IN_CORE0	264
WRF_G_TSSI_IN_CORE1	272
WRF_GPIO_OUT	231
WRF_LNA_2G_GND1P2_CORE0	290
WRF_LNA_2G_GND1P2_CORE1	239
WRF_LNA_5G_GND1P2_CORE0	234
WRF_LNA_5G_GND1P2_CORE1	238
WRF_PA_VDD3P3_CORE1	227
WRF_PA_VDD3P3_CORE1	236
WRF_PA5G_GND3P3_CORE0	241
WRF_PA5G_GND3P3_CORE1	242
WRF_PA5G_GND3P3_CORE1	243
WRF_PA2G_GND3P3_CORE1	245
WRF_PA2G_GND3P3_CORE1	246
WRF_PA5G_GND3P3_CORE0	253
WRF_PA_VDD3P3_CORE0	262
WRF_PA_VDD3P3_CORE0	263
WRF_PA2G_GND3P3_CORE0	267
WRF_PA2G_GND3P3_CORE0	283
WRF_PADRV2G_GND3P3_CORE0	282
WRF_PADRV2G_GND3P3_CORE1	249
WRF_PADRV2G_VDD3P3_CORE0	268
WRF_PADRV2G_VDD3P3_CORE1	250
WRF_PADRV5G_GND3P3_CORE0	254
WRF_PADRV5G_GND3P3_CORE1	247
WRF_PADRV5G_VDD3P3_CORE0	244
WRF_PADRV5G_VDD3P3_CORE1	248
WRF_PAOUT_2G_CORE0	287
WRF_PAOUT_2G_CORE1	226
WRF_PAOUT_5G_CORE0	235
WRF_PAOUT_5G_CORE1	228
WRF_RFIN_2G_CORE0	292
WRF_RFIN_2G_CORE1	233
WRF_RFIN_5G_CORE0	225
WRF_RFIN_5G_CORE1	229
WRF_RX2G_GND1P2_CORE0	293
WRF_RX2G_GND1P2_CORE1	256
WRF_RX2G_VDD1P2_CORE0	288
WRF_RX2G_VDD1P2_CORE1	257
WRF_RX5G_GND1P2_CORE0	230
WRF_RX5G_GND1P2_CORE1	259
WRF_RX5G_VDD1P2_CORE0	237
WRF_RX5G_VDD1P2_CORE1	258
WRF_SYNTH_GND1P2	271
WRF_SYNTH_VDD1P2	270
WRF_TCXO_CKIN2V	284
WRF_TCXO_VDD1P8	277
WRF_TX_GND1P2_CORE0	255
WRF_TX_GND1P2_CORE1	261
WRF_TX_VDD1P2_CORE0	266
WRF_TX_VDD1P2_CORE1	260
WRF_VCO_GND1P2	240
WRF_VCO_GND1P2	269
WRF_VCO_GND1P2	286
WRF_VCO_VDD1P2	232
WRF_XTAL_CAB_GND1P2	275
WRF_XTAL_CAB_VDD1P2	274
WRF_XTAL_CAB_XON	285
WRF_XTAL_CAB_XOP	278

Table 64: 208-Pin FCFBGA Package Pin List By Pin Number

Pin	Name
A1	BT_UART_TXD
A2	BT_LPO_IN
A3	BT_PCM_CLK
A4	BT_PCM_OUT
A5	RF_SW_CTRL_7
A6	RF_SW_CTRL_5
A7	RF_SW_CTRL_1
A8	GMODE_EXT_LNA_PU_CORE0
A9	GMODE_PA_EN_CORE0
A10	GPIO_7
A11	GPIO_6
A12	GPIO_3/TMS
A13	GPIO_0/WL_HOST_WAKE
A14	GPIO_1/WL_DEV_WAKE
A15	SR_VLX
A16	SR_VLX
B1	BT_UART_RXD
B2	BT_GPIO_4
B3	BT_I2S_WS
B4	BT_GPIO_3
B5	BT_PCM_IN
B6	RF_SW_CTRL_6
B7	RF_SW_CTRL_3
B8	AMODE_PA_EN_CORE0
B9	GPIO_13
B10	GPIO_8
B11	GPIO_2/TCK
B12	JTAG_SEL
B13	EXT_XTAL_PU
B14	SR_PVSS
B15	SR_PVSS
B16	SR_PVSS
C1	BT_I2S_CLK
C2	BT_UART_RTS_N
C15	SR_VDDBATP5V
C16	SR_VDDBATP5V
D1	BT_I2S_DO

Pin	Name
D2	BT_VDDC_ISO_2
D4	BT_PCM_SYNC
D5	BT_GPIO_2
D6	RF_SW_CTRL_4
D7	RF_SW_CTRL_0
D8	RF_SW_CTRL_2
D9	GPIO_12
D10	AMODE_EXT_LNA_PU_CORE0
D11	GPIO_11
D12	GPIO_5/TDO/UART_TX
D13	PMU_AVSS
D15	SR_VDDBATA5V
D16	SR_VDDBATA5V
E1	BT_CLK_REQ
E2	BT_I2S_DI
E4	BT_VDDC_ISO_1
E11	GPIO_9
E13	VOUT_LDO3P3
E15	VOUT_CLDO
E16	VOUT_CLDO
F1	BT_HOST_WAKE
F2	BT_UART_CTS_N
F4	BT_VDDO
F5	BT_VDDC
F6	BT_VDDC
F10	GPIO_4/TDI/UART_RX
F15	VOUT_LNLDO1
F16	VOUT_LNLDO1
G1	BT_TM1
G2	BT_DEV_WAKE
G15	LDO_VDD1P5
G16	LDO_VDD1P5
H1	FM_VCOVDD
H2	BTFM_RGND
H4	BT_GPIO_5
H6	BT_VDDC
H7	VSS

Pin	Name
H8	VDD
H13	VOUT_LNLDO2
H15	VOUT_HSICAVDD
H16	HSIC_STROBE
J1	FM_LNAVDD
J2	BTFM_RGND
J4	FM_PLLVDD
J6	VSS
J8	VDDIO_RF
J10	VSS
J13	WLREG_ON
J15	HSIC_RREFHSIC
J16	HSIC_DATA
K1	FM_RFIN
K2	FM_RFAUX
K4	BTFM_RGND
K7	VDD
K8	VDD
K11	VDDIO
K13	BTREG_ON
K15	HSIC_DVDD1P2
K16	SDIO_DATA_2
L1	BT_VCOVDD
L2	BTFM_RGND
L4	BTFM_RGND
L6	VSS
L7	GPIO_10
L10	OTP_VDD33
L13	VSS
L15	SDIO_DATA_1
L16	SDIO_DATA_3
M1	BT_LNAVDD
M2	BTFM_RGND
M4	BT_PLLVDD
M6	GPIO_15
M9	VSS
M10	VDD
M11	VDDIO_RF

Pin	Name
M12	VDDIO_SD
M13	HSIC_AGND12PLL
M15	SDIO_DATA_0
M16	SDIO_CLK
N1	BT_RF
N2	BTFM_RGND
N4	BTFM_RGND
N6	GPIO_14
N8	VDD
N13	RF_SW_CTRL_9
N15	RF_SW_CTRL_11
N16	SDIO_CMD
P1	BT_PAVDD
P2	BT_VBAT
P4	BT_IFVDD
P6	VSS
P8	VDD
P9	VSS
P10	VDD
P11	RF_SW_CTRL_8
P12	PALDO_PU
P13	GMODE_EXT_LNA_PU_CORE1
P15	AMODE_EXT_LNA_PU_CORE1
P16	RF_SW_CTRL_10
R1	WRF_RFIN_2G_CORE0
R2	RGND
R4	RGND
R6	VSS
R11	GMODE_PA_EN_CORE1
R13	AMODE_PA_EN_CORE1
R15	VSS
R16	AVDD_BBPLL
T1	RGND
T2	WRF_RX2G_VDD1P2_CORE0
T4	WRF_PADRV2G_VDD3P3_CORE0
T6	RGND
T7	RGND
T8	RGND

Pin	Name
T9	VSS
T10	RGND
T15	WRF_XTAL_CAB_GND1P2
T16	WRF_TCXO_CKIN2V
U1	WRF_PAOUT_2G_CORE0
U2	RGND
U4	RGND
U10	WRF_AFE_VDD1P2_CORE1
U13	WRF_TCXO_VDD1P8
U15	WRF_XTAL_CAB_GND1P2
U16	WRF_XTAL_CAB_XON
V1	WRF_PA_VDD3P3_CORE0
V2	RGND
V5	WRF_PADRV5G_VDD3P3_CORE0
V6	RGND
V7	WRF_AFE_VDD1P2_CORE0
V8	RGND
V9	RGND
V10	RGND
V11	RGND
V13	WRF_PADRV5G_VDD3P3_CORE1
V15	WRF_XTAL_CAB_VDD1P2
V16	WRF_XTAL_CAB_XOP
W1	WRF_PAOUT_5G_CORE0
W2	RGND
W15	RGND
W16	RGND
Y1	RGND
Y3	RGND
Y4	RGND
Y5	RGND
Y6	WRF_TX_VDD1P2_CORE0
Y7	WRF_GPIO_OUT
Y8	WRF_TX_VDD1P2_CORE1
Y9	RGND
Y10	RGND
Y11	WRF_PADRV2G_VDD3P3_CORE1
Y12	RGND
Y13	RGND
Y14	RGND
Y15	RGND
Y16	WRF_RX5G_VDD1P2_CORE1
AA1	WRF_RFIN_5G_CORE0
AA2	RGND
AA3	WRF_RX5G_VDD1P2_CORE0
AA4	RGND
AA5	WRF_SYNTH_VDD1P2
AA6	RGND
AA7	WRF_VCO_VDD1P2
AA8	WRF_RX2G_VDD1P2_CORE1
AA9	WRF_RFIN_2G_CORE1
AA10	RGND
AA11	WRF_PAOUT_2G_CORE1
AA12	WRF_PA_VDD3P3_CORE1
AA13	WRF_PAOUT_5G_CORE1
AA14	RGND
AA15	WRF_RFIN_5G_CORE1
AA16	RGND

Table 65: 208-Pin FCFBGA Package Pin List By Pin Name

Name	Pin
AMODE_EXT_LNA_PU_CORE0	D10
AMODE_EXT_LNA_PU_CORE1	P15
AMODE_PA_EN_CORE0	B8
AMODE_PA_EN_CORE1	R13
AVDD_BBPLL	R16
BT_CLK_REQ	E1
BT_DEV_WAKE	G2
BT_GPIO_2	D5
BT_GPIO_3	B4
BT_GPIO_4	B2
BT_GPIO_5	H4
BT_HOST_WAKE	F1
BT_I2S_CLK	C1
BT_I2S_DI	E2
BT_I2S_DO	D1
BT_I2S_WS	B3
BT_IFVDD	P4
BT_LNAVDD	M1
BT_LPO_IN	A2
BT_PAVDD	P1
BT_PCM_CLK	A3
BT_PCM_IN	B5
BT_PCM_OUT	A4
BT_PCM_SYNC	D4
BT_PLLVDD	M4
BT_RF	N1
BT_TM1	G1
BT_UART_CTS_N	F2
BT_UART_RTS_N	C2
BT_UART_RXD	B1
BT_UART_TXD	A1
BT_VBAT	P2
BT_VCOVDD	L1
BT_VDDC	F5
BT_VDDC	F6
BT_VDDC	H6
BT_VDDC_ISO_1	E4
BT_VDDC_ISO_2	D2
BT_VDDO	F4
BTFM_RGND	H2
BTFM_RGND	J2
BTFM_RGND	K4
BTFM_RGND	L2
BTFM_RGND	L4
BTFM_RGND	M2
BTFM_RGND	N2
BTFM_RGND	N4
BTREG_ON	K13
EXT_XTAL_PU	B13
FM_LNAVDD	J1
FM_PLLVDD	J4
FM_RFAUX	K2
FM_RFIN	K1
FM_VCOVDD	H1
GMODE_EXT_LNA_PU_CORE0	A8
GMODE_EXT_LNA_PU_CORE1	P13
GMODE_PA_EN_CORE0	A9
GMODE_PA_EN_CORE1	R11
GPIO_0/WL_HOST_WAKE	A13
GPIO_1/WL_DEV_WAKE	A14
GPIO_10	L7
GPIO_11	D11
GPIO_12	D9
GPIO_13	B9
GPIO_14	N6
GPIO_15	M6
GPIO_2/TCK	B11
GPIO_3/TMS	A12
GPIO_4/TDI/UART_RX	F10
GPIO_5/TDO/UART_TX	D12
GPIO_6	A11
GPIO_7	A10
GPIO_8	B10
GPIO_9	E11

Name	Pin
HSIC_AGND12PLL	M13
HSIC_DATA	J16
HSIC_DVDD1P2	K15
HSIC_RREFHSIC	J15
HSIC_STROBE	H16
JTAG_SEL	B12
LDO_VDD1P5	G15
LDO_VDD1P5	G16
OTP_VDD33	L10
PALDO_PU	P12
PMU_AVSS	D13
RF_SW_CTRL_0	D7
RF_SW_CTRL_1	A7
RF_SW_CTRL_10	P16
RF_SW_CTRL_11	N15
RF_SW_CTRL_2	D8
RF_SW_CTRL_3	B7
RF_SW_CTRL_4	D6
RF_SW_CTRL_5	A6
RF_SW_CTRL_6	B6
RF_SW_CTRL_7	A5
RF_SW_CTRL_8	P11
RF_SW_CTRL_9	N13
RGND	R2
RGND	R4
RGND	T1
RGND	T6
RGND	T7
RGND	T8
RGND	T10
RGND	U2
RGND	U4
RGND	V2
RGND	V6
RGND	V8
RGND	V9
RGND	V10
RGND	V11

Name	Pin
RGND	W2
RGND	W15
RGND	W16
RGND	Y1
RGND	Y3
RGND	Y4
RGND	Y5
RGND	Y9
RGND	Y10
RGND	Y12
RGND	Y13
RGND	Y14
RGND	Y15
RGND	AA2
RGND	AA4
RGND	AA6
RGND	AA10
RGND	AA14
RGND	AA16
SDIO_CLK	M16
SDIO_CMD	N16
SDIO_DATA_0	M15
SDIO_DATA_1	L15
SDIO_DATA_2	K16
SDIO_DATA_3	L16
SR_PVSS	B14
SR_PVSS	B15
SR_PVSS	B16
SR_VDDBATA5V	D15
SR_VDDBATA5V	D16
SR_VDDBATP5V	C15
SR_VDDBATP5V	C16
SR_VLX	A15
SR_VLX	A16
VDD	H8
VDD	K7
VDD	K8
VDD	M10

Name	Pin
VDD	N8
VDD	P8
VDD	P10
VDDIO	K11
VDDIO_RF	J8
VDDIO_RF	M11
VDDIO_SD	M12
VOUT_CLDO	E15
VOUT_CLDO	E16
VOUT_HSICAVDD	H15
VOUT_LDO3P3	E13
VOUT_LNLDO1	F15
VOUT_LNLDO1	F16
VOUT_LNLDO2	H13
VSS	H7
VSS	J6
VSS	J10
VSS	L6
VSS	L13
VSS	M9
VSS	P6
VSS	P9
VSS	R6
VSS	R15
VSS	T9
WLREG_ON	J13
WRF_AFE_VDD1P2_CORE0	V7
WRF_AFE_VDD1P2_CORE1	U10
WRF_GPIO_OUT	Y7
WRF_PA_VDD3P3_CORE0	V1
WRF_PA_VDD3P3_CORE1	AA12
WRF_PADRV2G_VDD3P3_CORE0	T4
WRF_PADRV2G_VDD3P3_CORE1	Y11
WRF_PADRV5G_VDD3P3_CORE0	V5
WRF_PADRV5G_VDD3P3_CORE1	V13
WRF_PAOUT_2G_CORE0	U1
WRF_PAOUT_2G_CORE1	AA11
WRF_PAOUT_5G_CORE0	W1
WRF_PAOUT_5G_CORE1	AA13
WRF_RFIN_2G_CORE0	R1
WRF_RFIN_2G_CORE1	AA9
WRF_RFIN_5G_CORE0	AA1
WRF_RFIN_5G_CORE1	AA15
WRF_RX2G_VDD1P2_CORE0	T2
WRF_RX2G_VDD1P2_CORE1	AA8
WRF_RX5G_VDD1P2_CORE0	AA3
WRF_RX5G_VDD1P2_CORE1	Y16
WRF_SYNTH_VDD1P2	AA5
WRF_TCXO_CKIN2V	T16
WRF_TCXO_VDD1P8	U13
WRF_TX_VDD1P2_CORE0	Y6
WRF_TX_VDD1P2_CORE1	Y8
WRF_VCO_VDD1P2	AA7
WRF_XTAL_CAB_GND1P2	T15
WRF_XTAL_CAB_GND1P2	U15
WRF_XTAL_CAB_VDD1P2	V15
WRF_XTAL_CAB_XON	U16
WRF_XTAL_CAB_XOP	V16

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