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RK3328

Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Note:

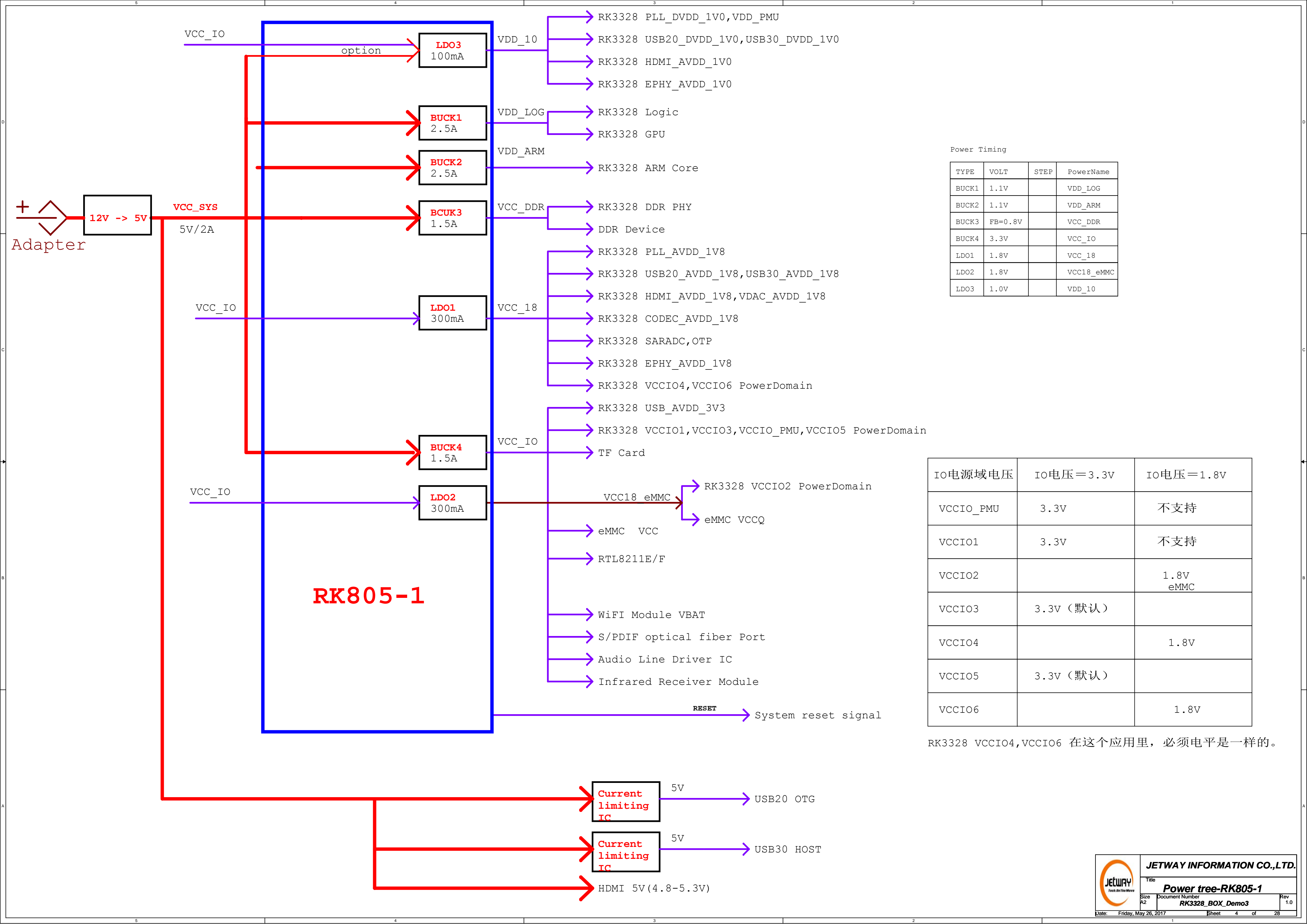
Component parameter description

1. DNP stands for component not mounted temporarily

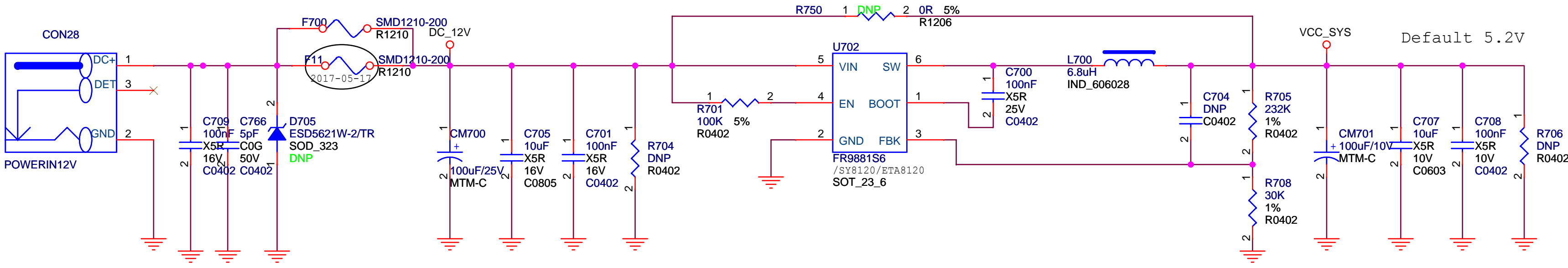
2. If Value or option is DNP, which means the area is reserved without being mounted

5					4					3					2					1									
Version					Date					Author					Change Note										Approved				
V1.0					20170309					ZDZ					First edictor														



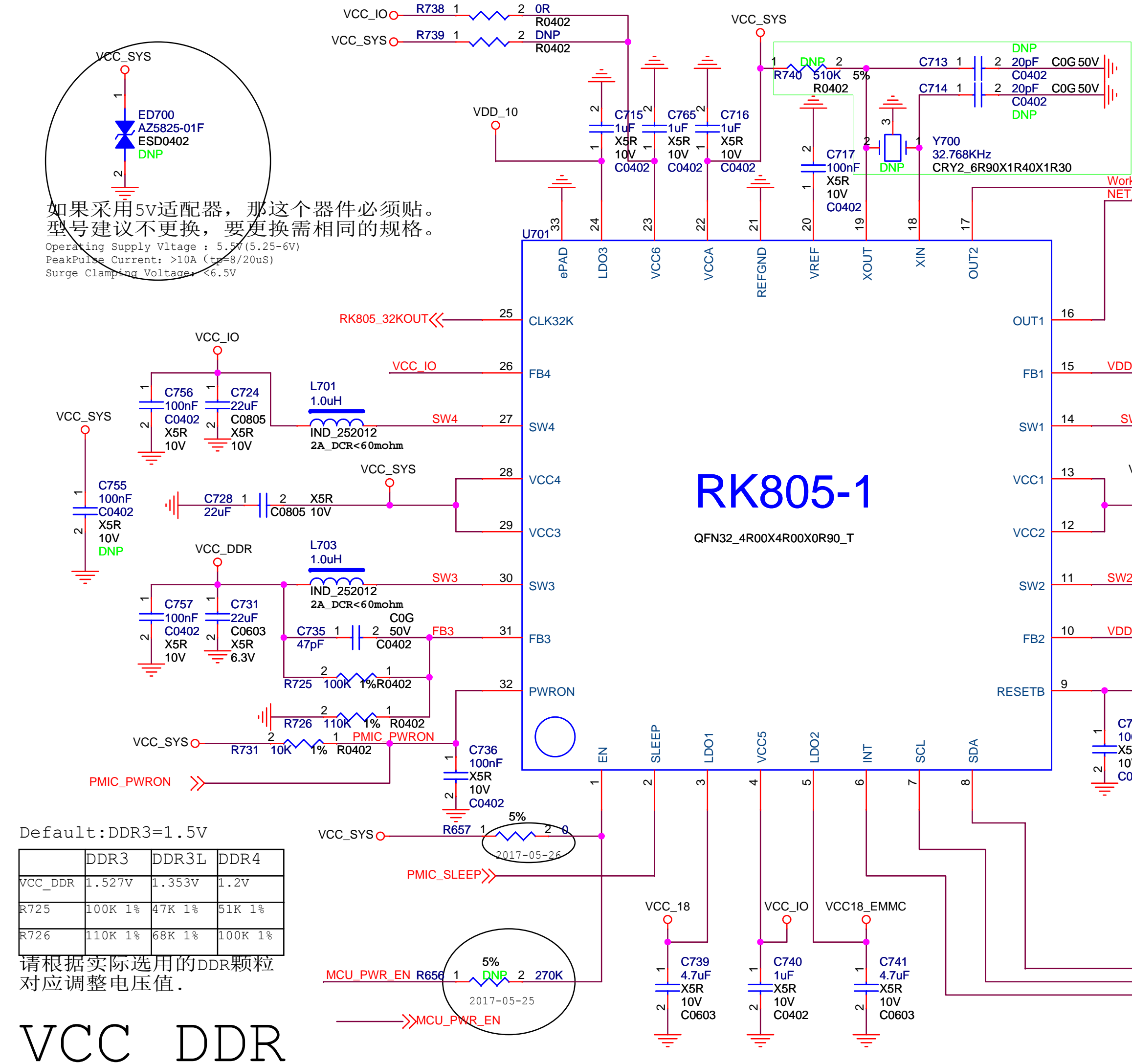




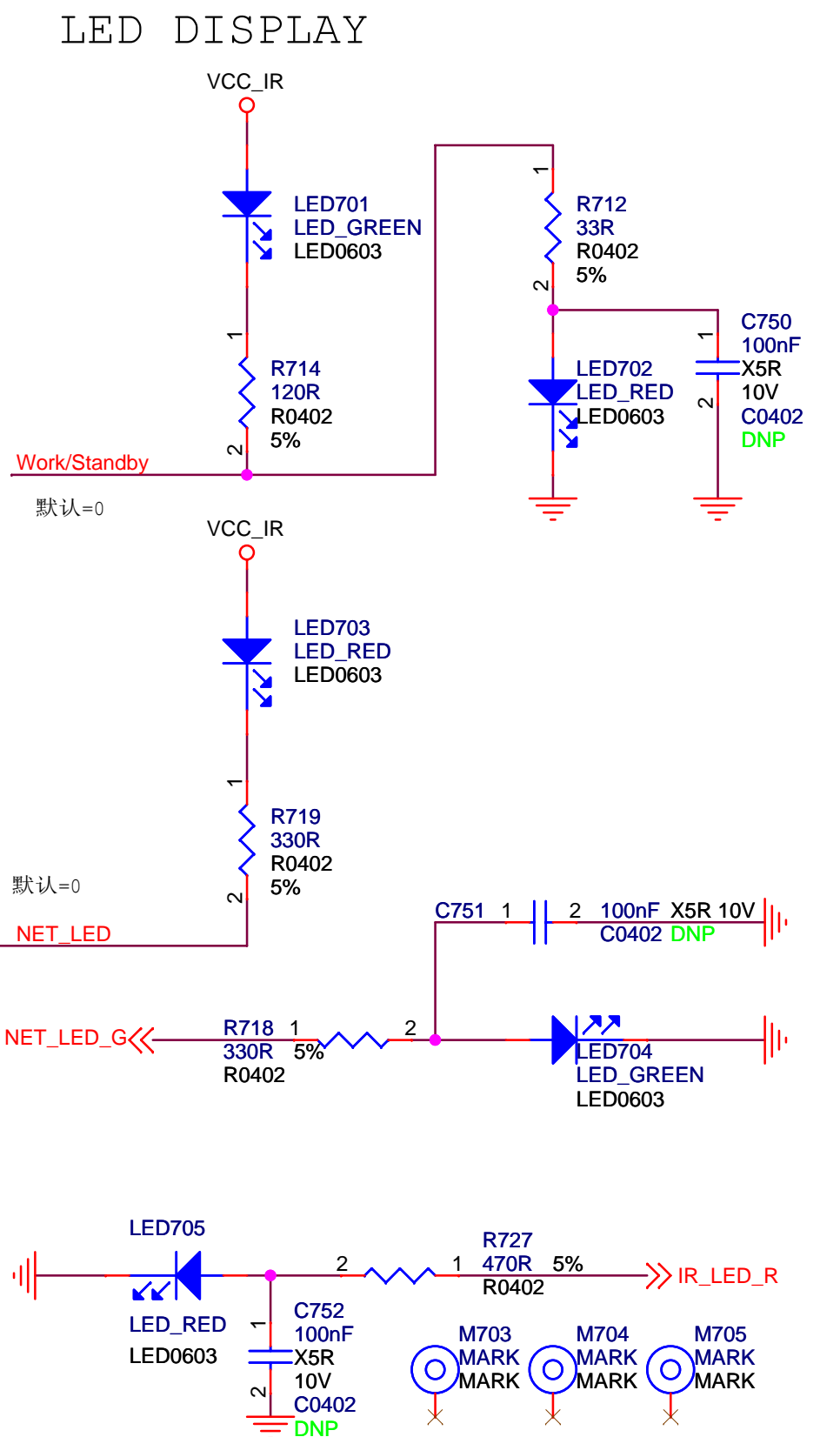


DC12V

VCC SYS



- 1: 如WIFI/BT需要32.768KHz时钟，默认由CPU提供32.769KHz时钟，默认不贴。
- 2: 如果修改了PLL分频，造成无法分出32.769KHz时钟，然后WIFI/BT又需要32.768KHz时钟，那么这部分电路需要贴上。
- 3: WIFI/BT不用32.768KHz时钟，这部分可以不贴。模组是否需要32.768KHz，请见各WIFI/BT模组分页说明。



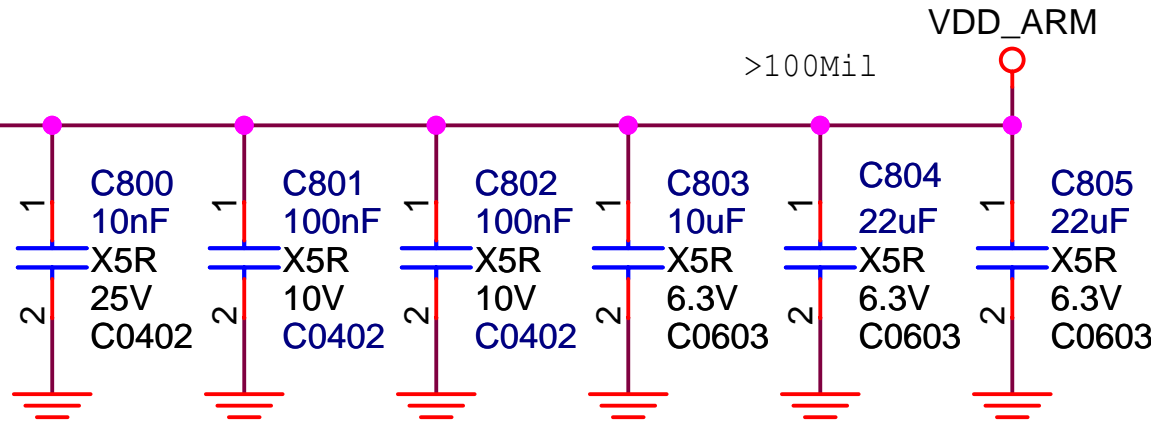
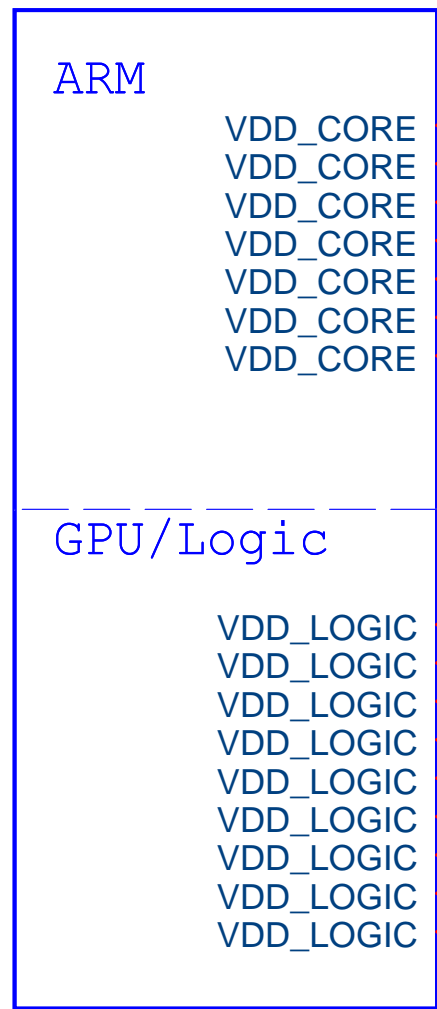
Default:DDR3=1.5V

	DDR3	DDR3L	DDR4
VCC_DDR	1.527V	1.353V	1.2V
R725	100K 1%	47K 1%	51K 1%
R726	110K 1%	68K 1%	100K 1%

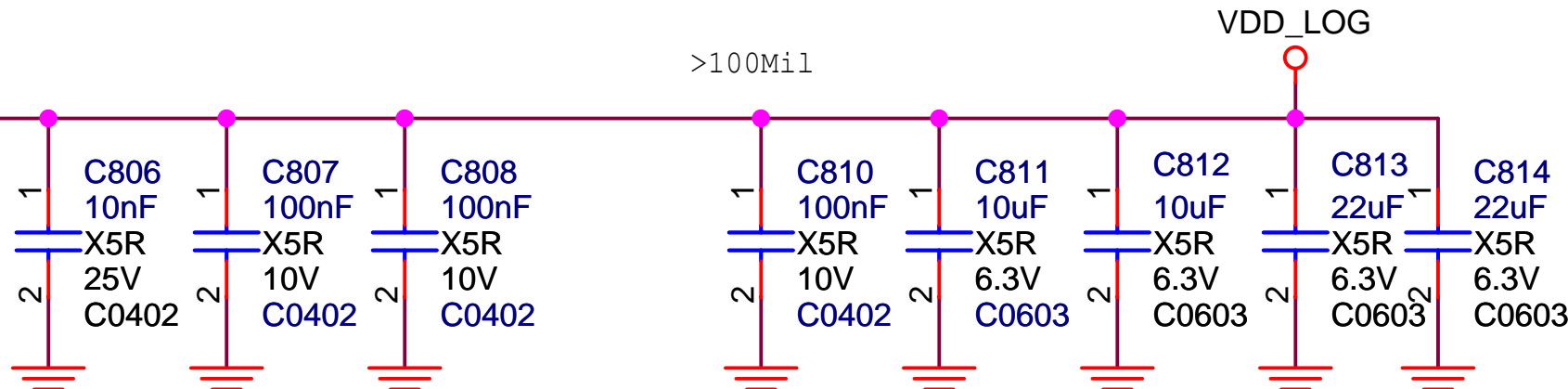
请根据实际选用的DDR颗粒对应调整电压值。

VCC\_DDR

U800N



PCB LAYOUT注意：电容都要靠近主控，其中一个22uF电容需要放在管脚正下方。

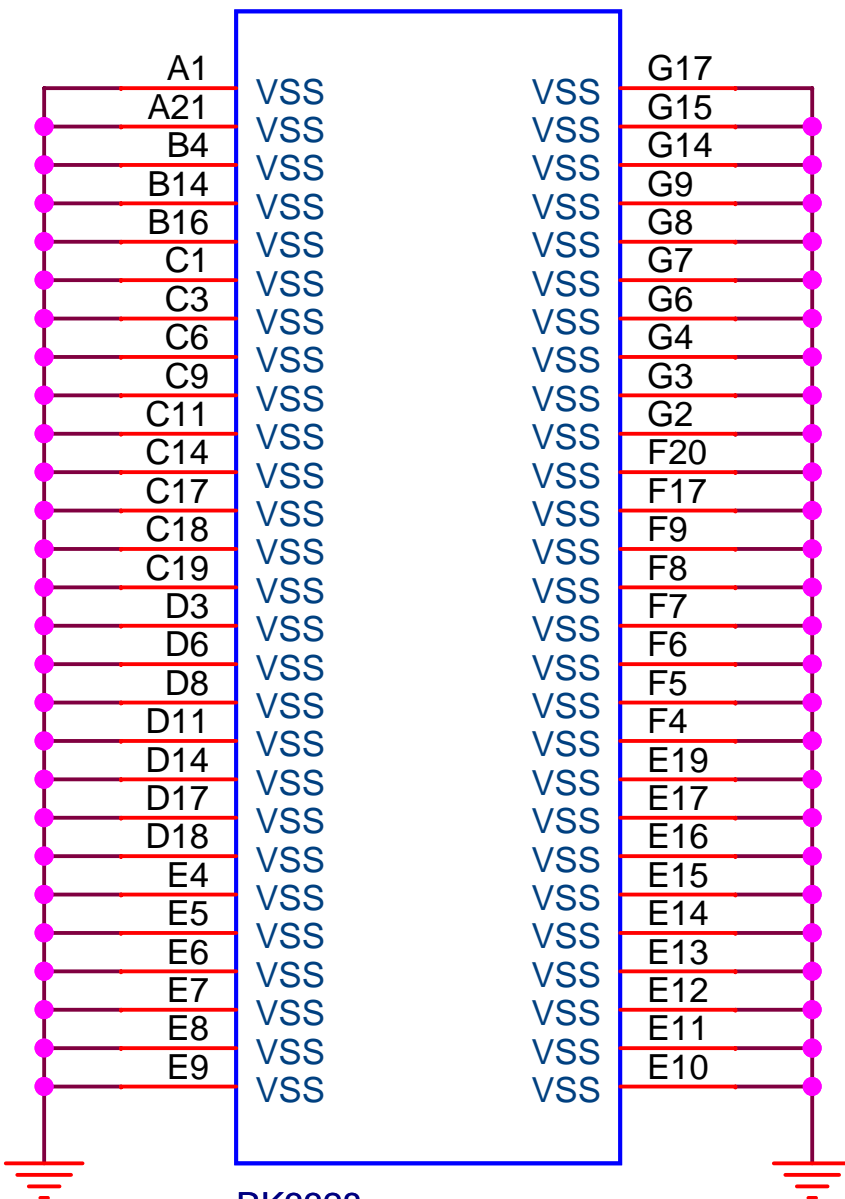


PCB LAYOUT注意：电容都要靠近主控，其中一个22uF电容需要放在管脚正下方。

RK3328

BGA395\_14R00X14R00X1R24

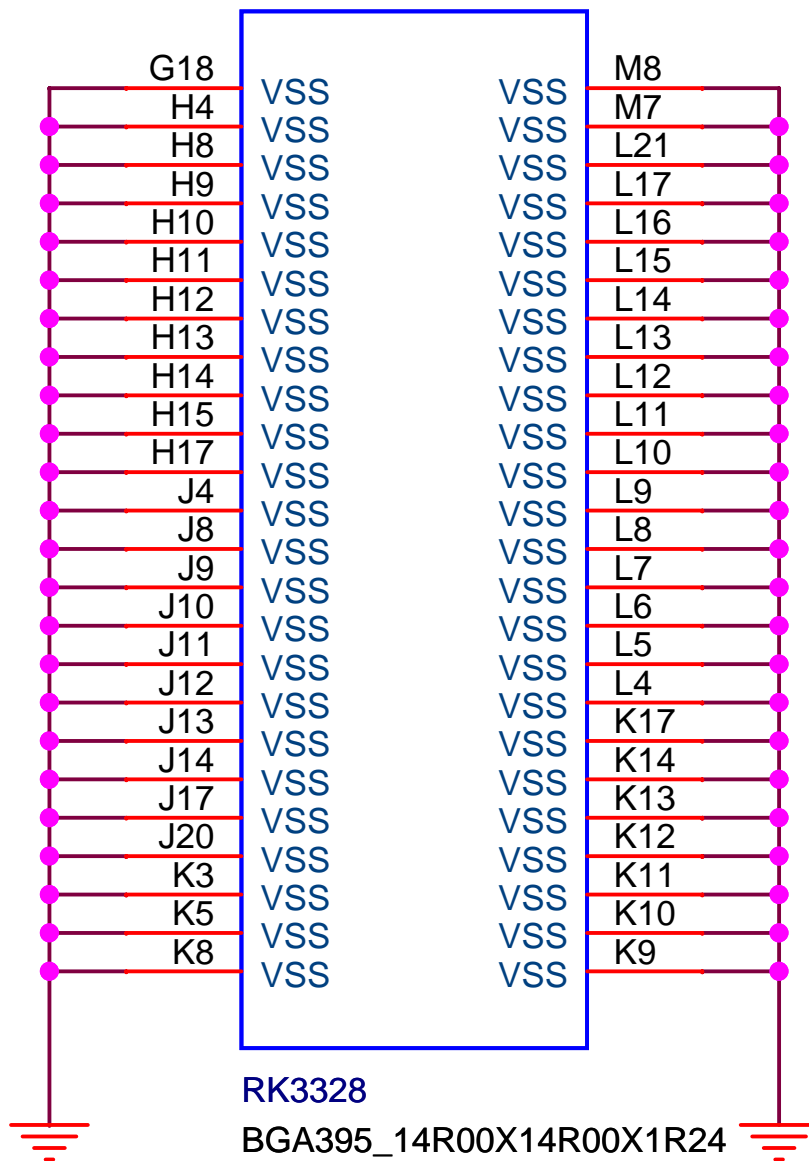
U800O



RK3328

BGA395\_14R00X14R00X1R24

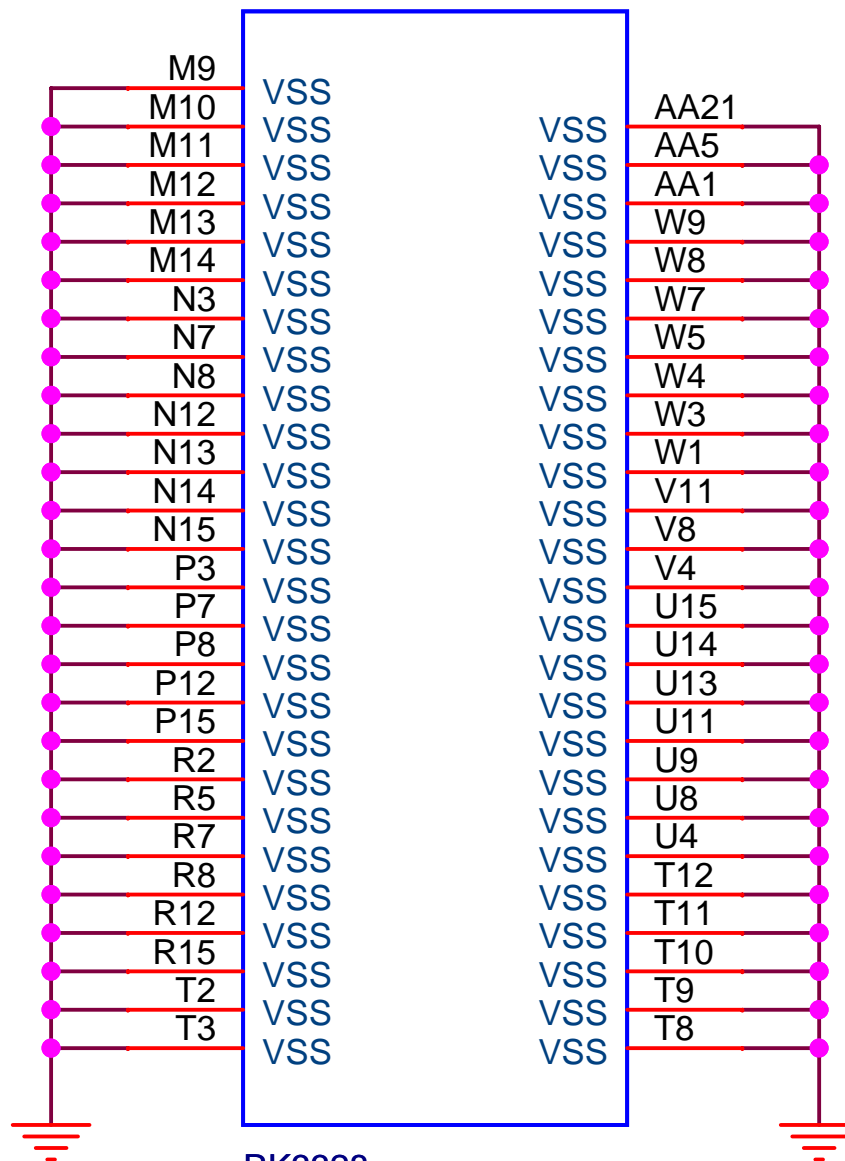
U800P



RK3328

BGA395\_14R00X14R00X1R24

U800Q



RK3328

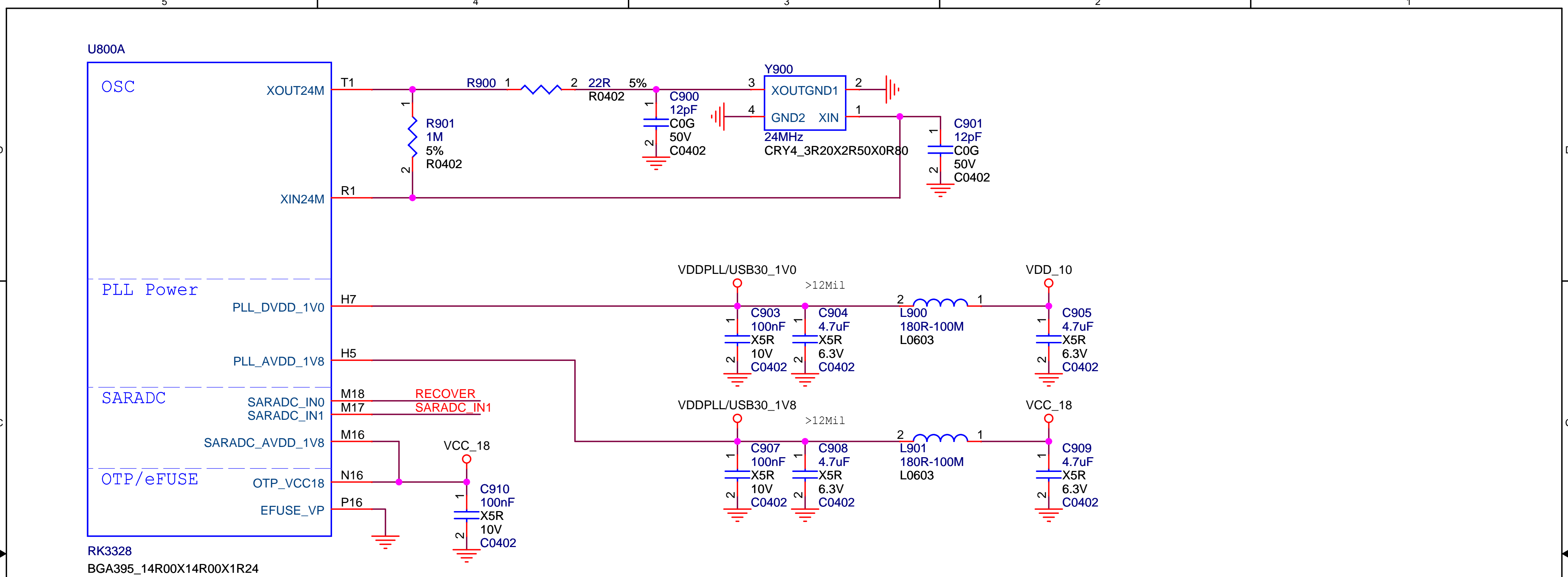
BGA395\_14R00X14R00X1R24




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Title  
**RK3328 Power**

Size A4 Document Number **RK3328\_BOX\_Demo3** Rev 1.0



SARADC_IN0 BOM版本	SARADC_IN1 PCB版本	Up阻值	Down阻值	
Recover		DNP	10K	
BOM1		110K	10K	
BOM2		100K	20K	
BOM3		100K	33K	
BOM4		36K	18K	
BOM5		51K	36K	
BOM6		51K	51K	
BOM7		36K	51K	
BOM8		18K	36K	
BOM9		33K	100K	
BOM10		20K	100K	
BOM11		10K	110K	
BOM12		10K	DNP	



**JETWAY**  
Tech. On The Move

**JETWAY INFORMATION CO.,LTD.**

Title  
**RK3328 OSC/PLL/OTP/SARADC**

Size  
A4

Document Number  
**RK3328\_BOX\_Demo3**

Rev  
1.0

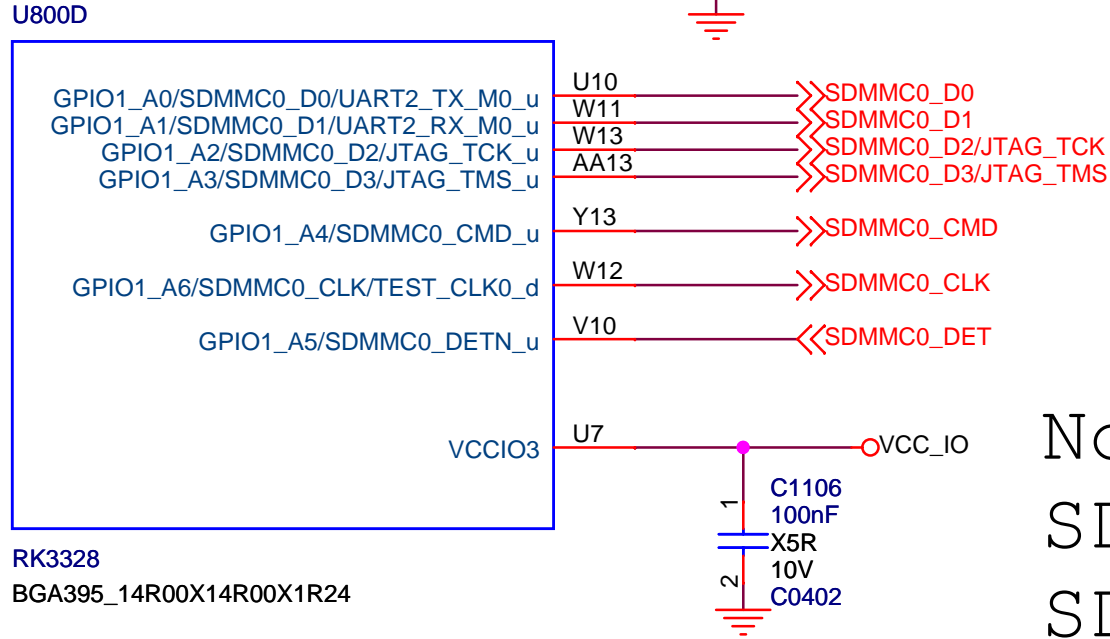
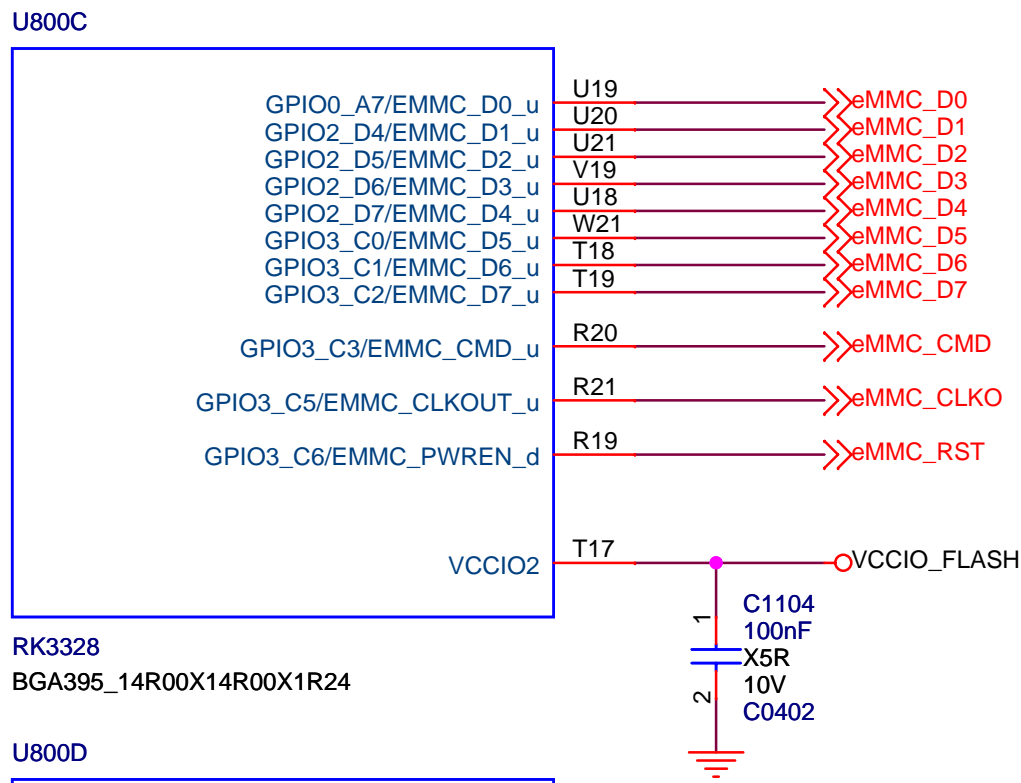
Date: Friday, May 26, 2017

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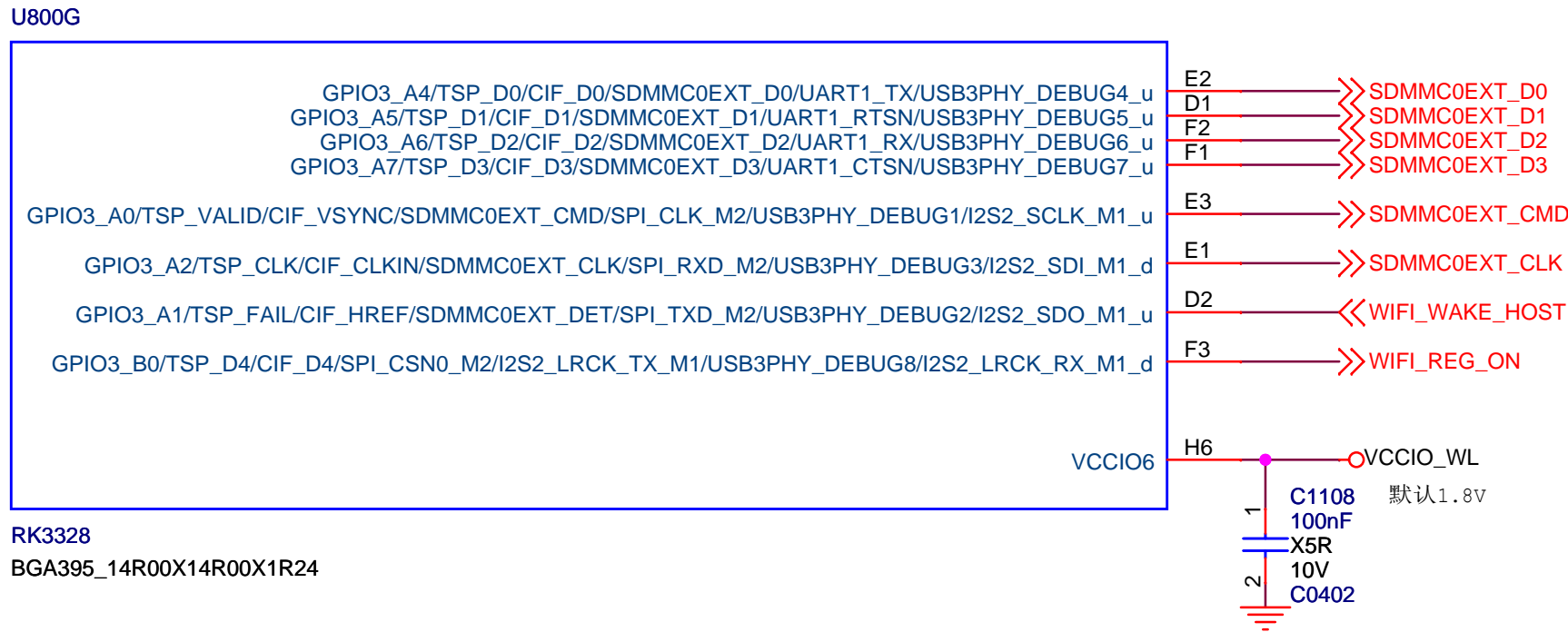




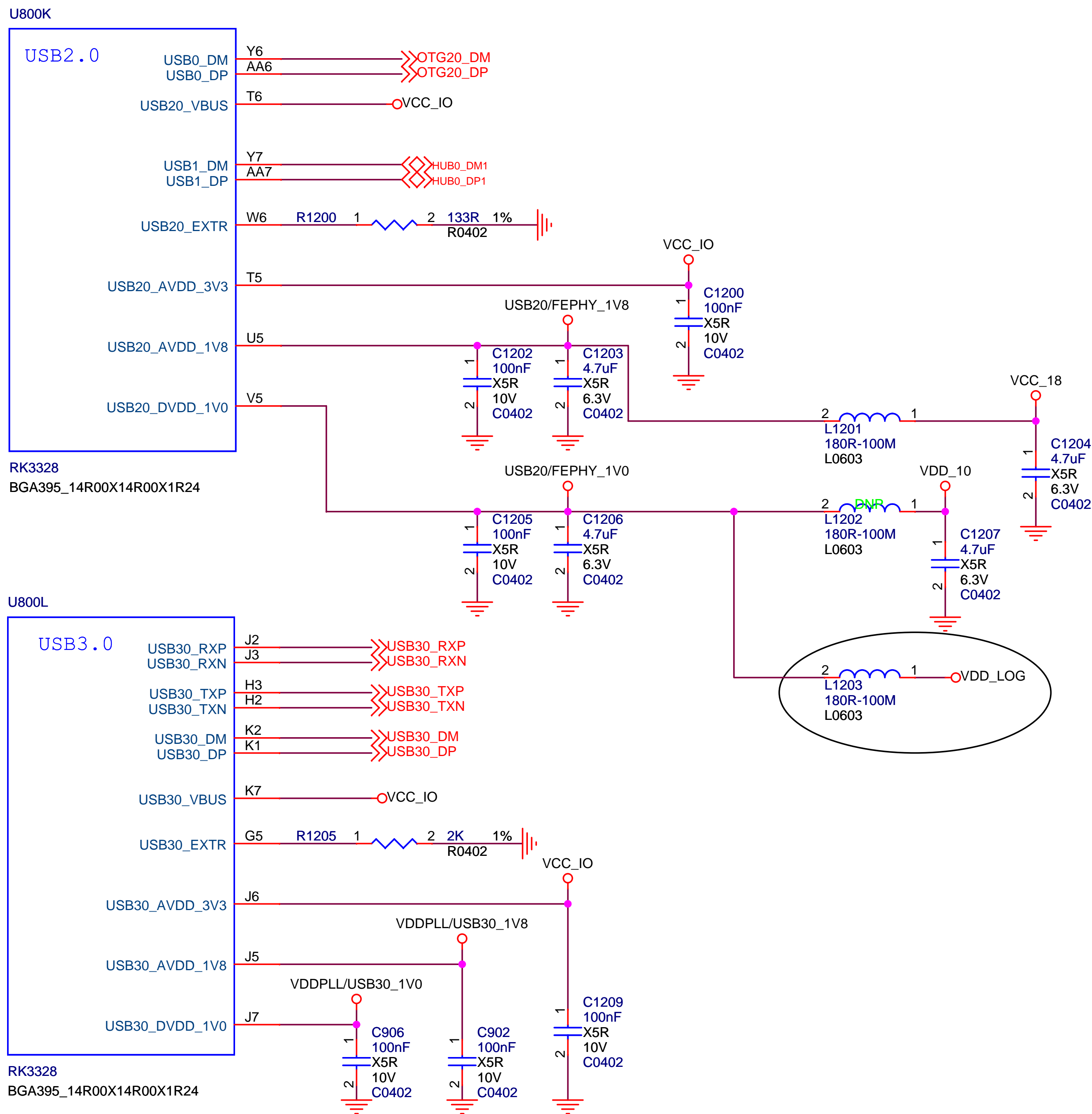


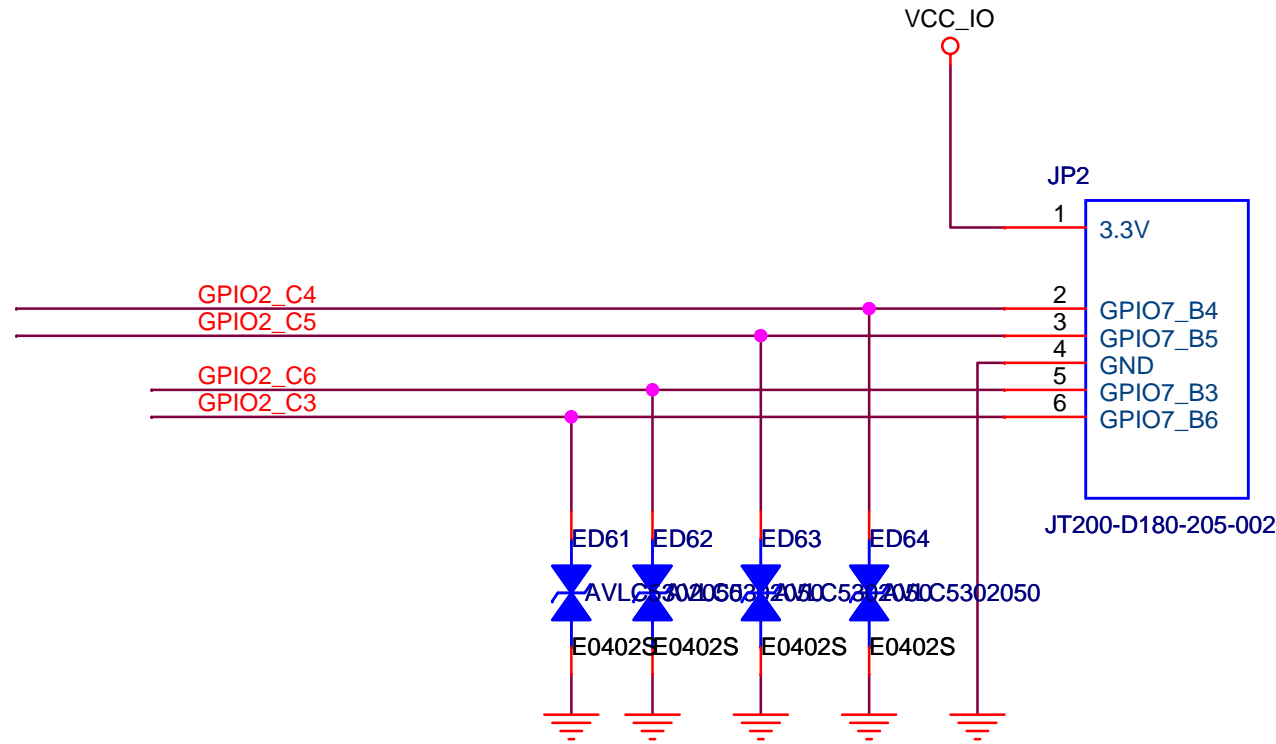
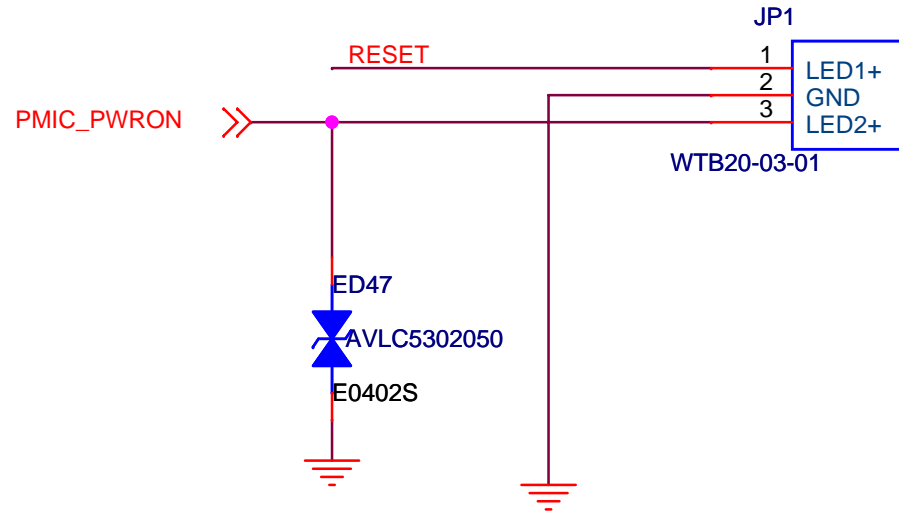
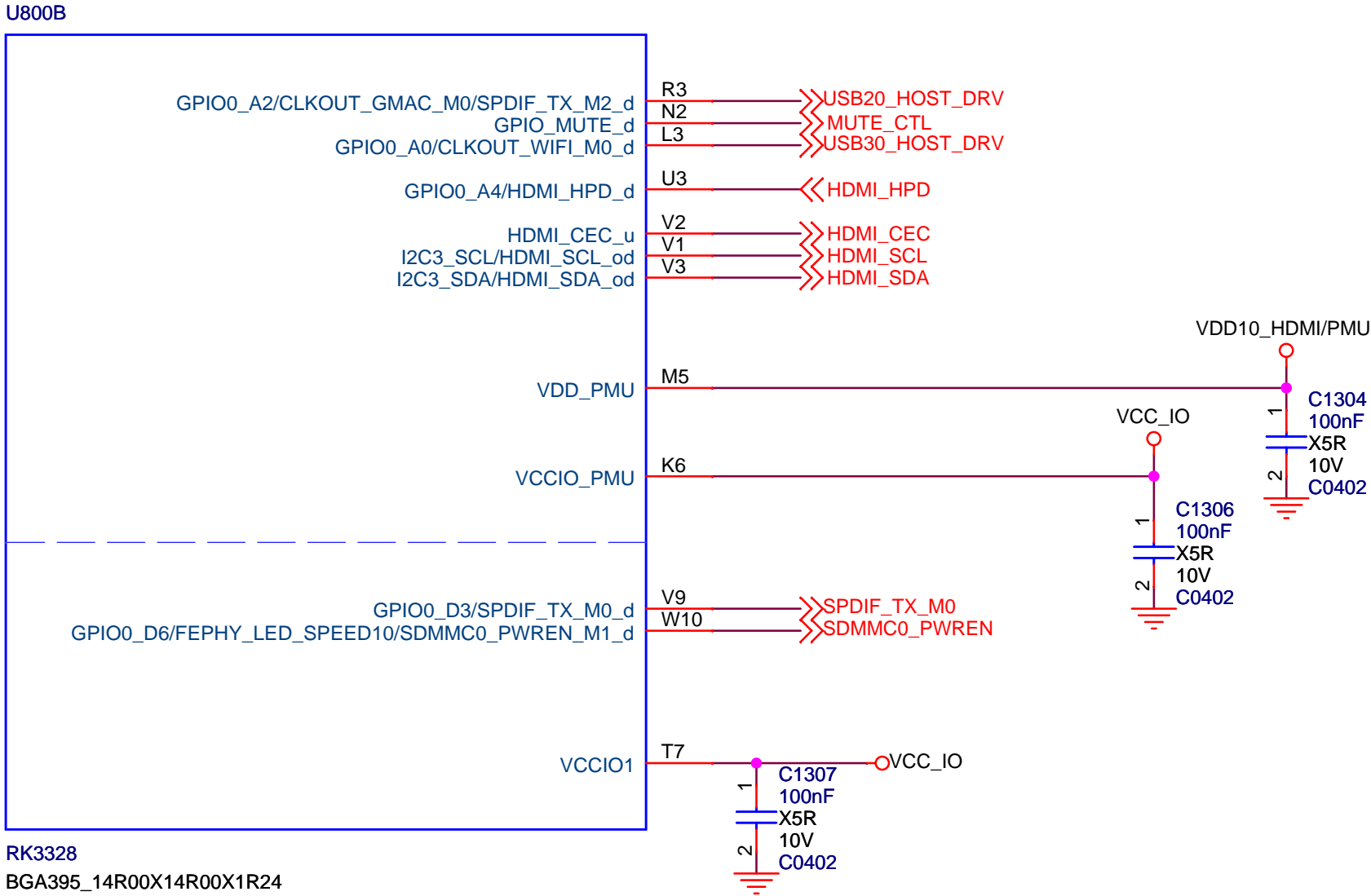
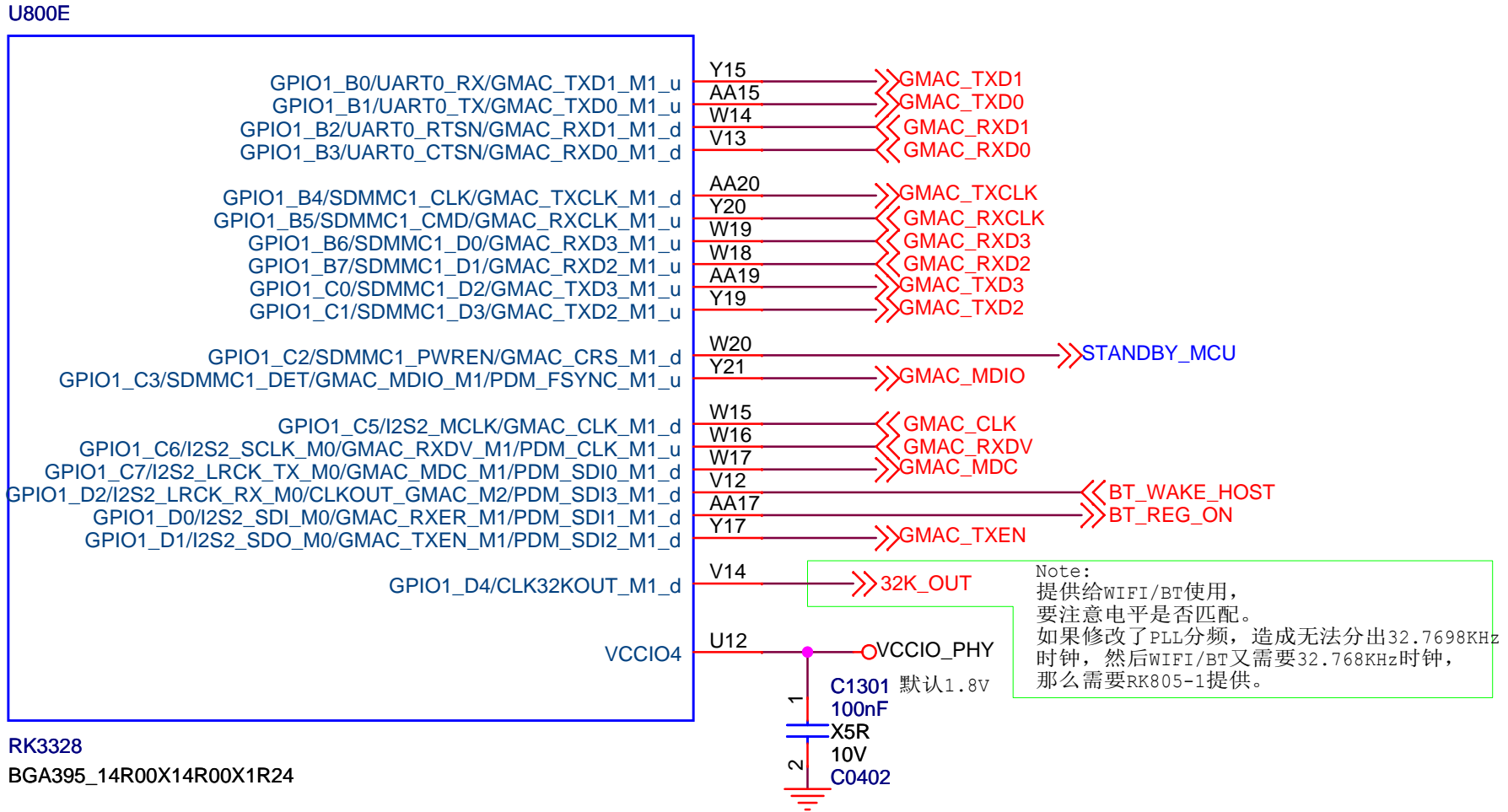
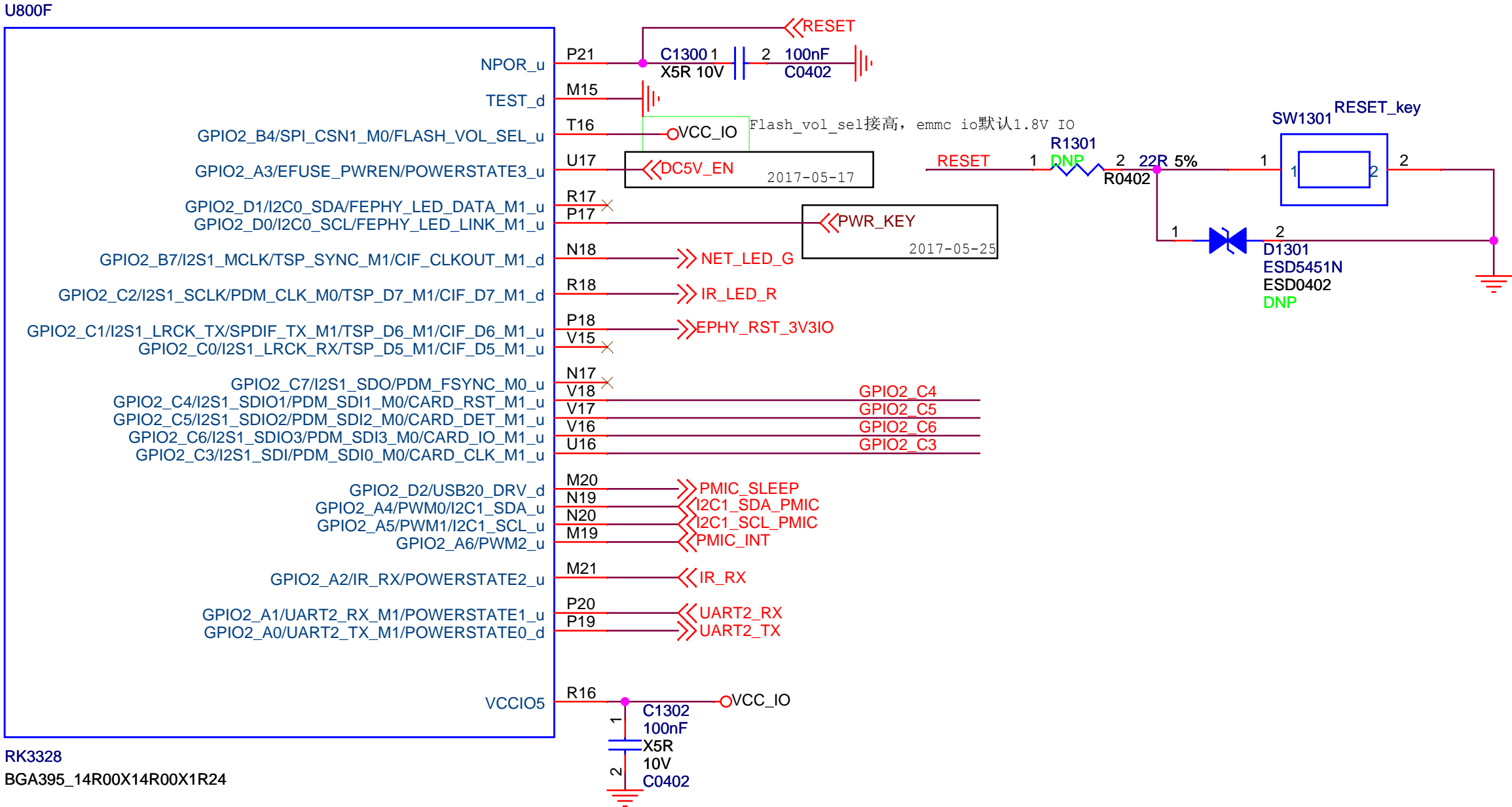


Note:  
SDMMC0支持SD Boot  
SDMMC0EXT不支持SD Boot



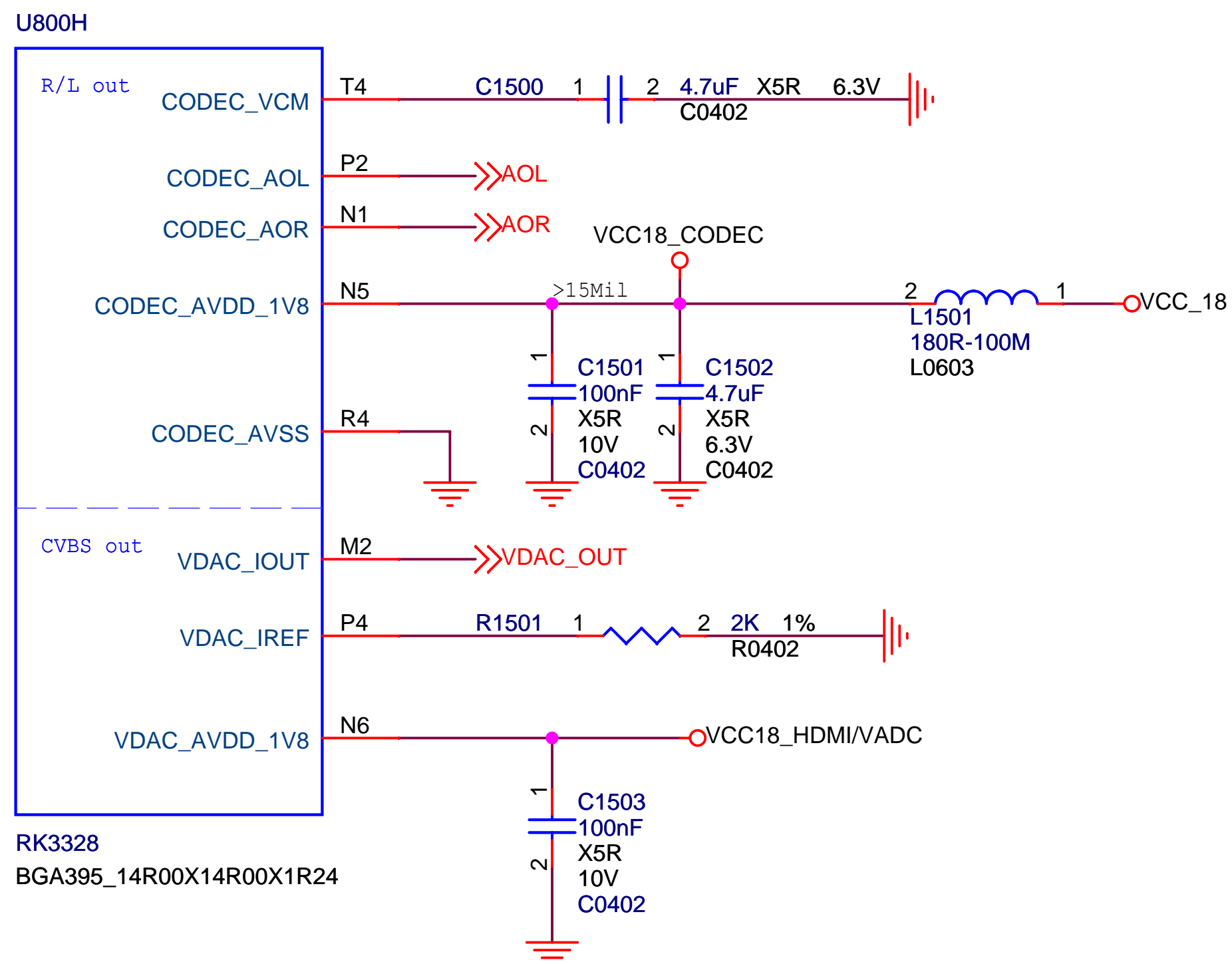
Note:  
布局时，要优先考虑SDMM0EXT走线尽量短

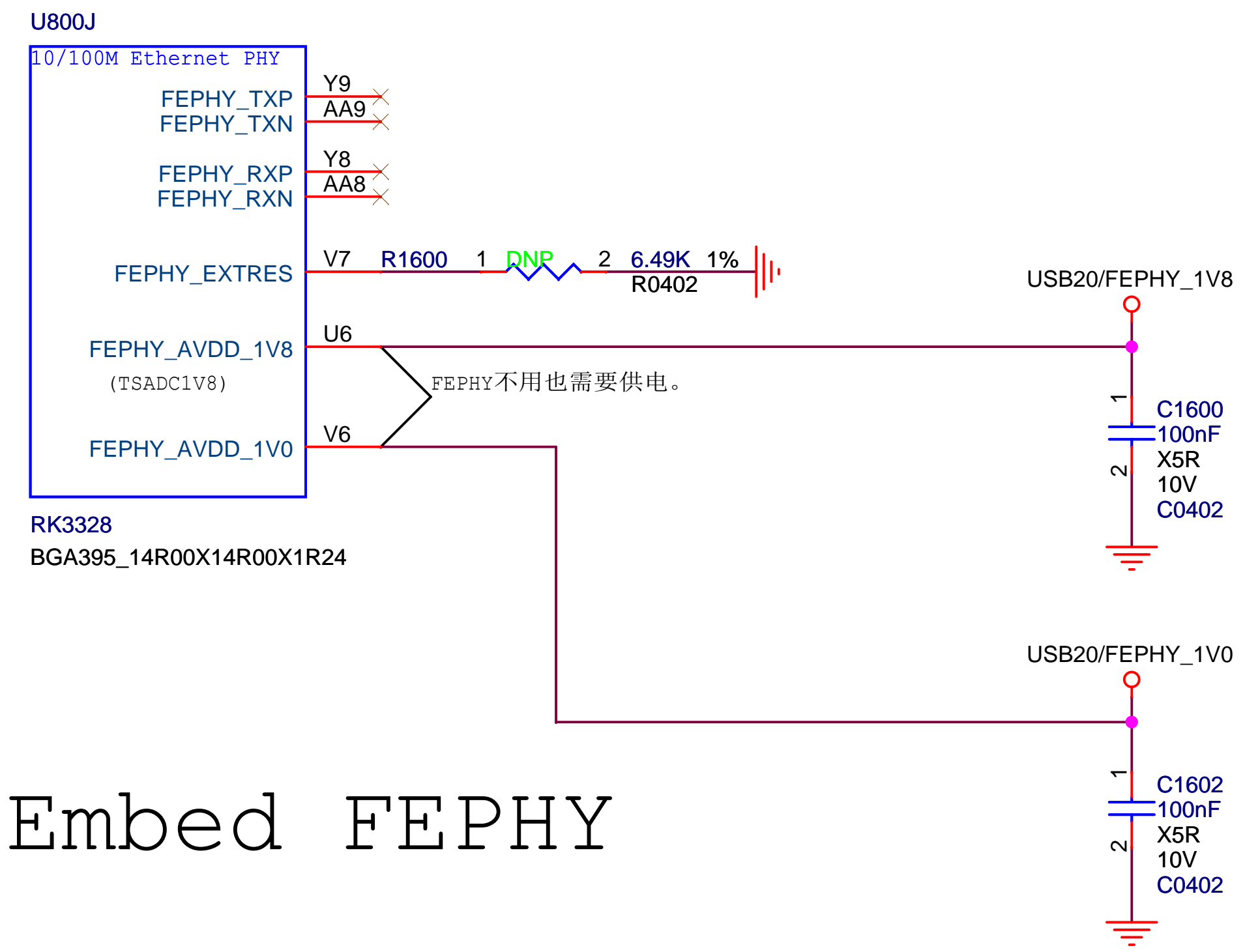






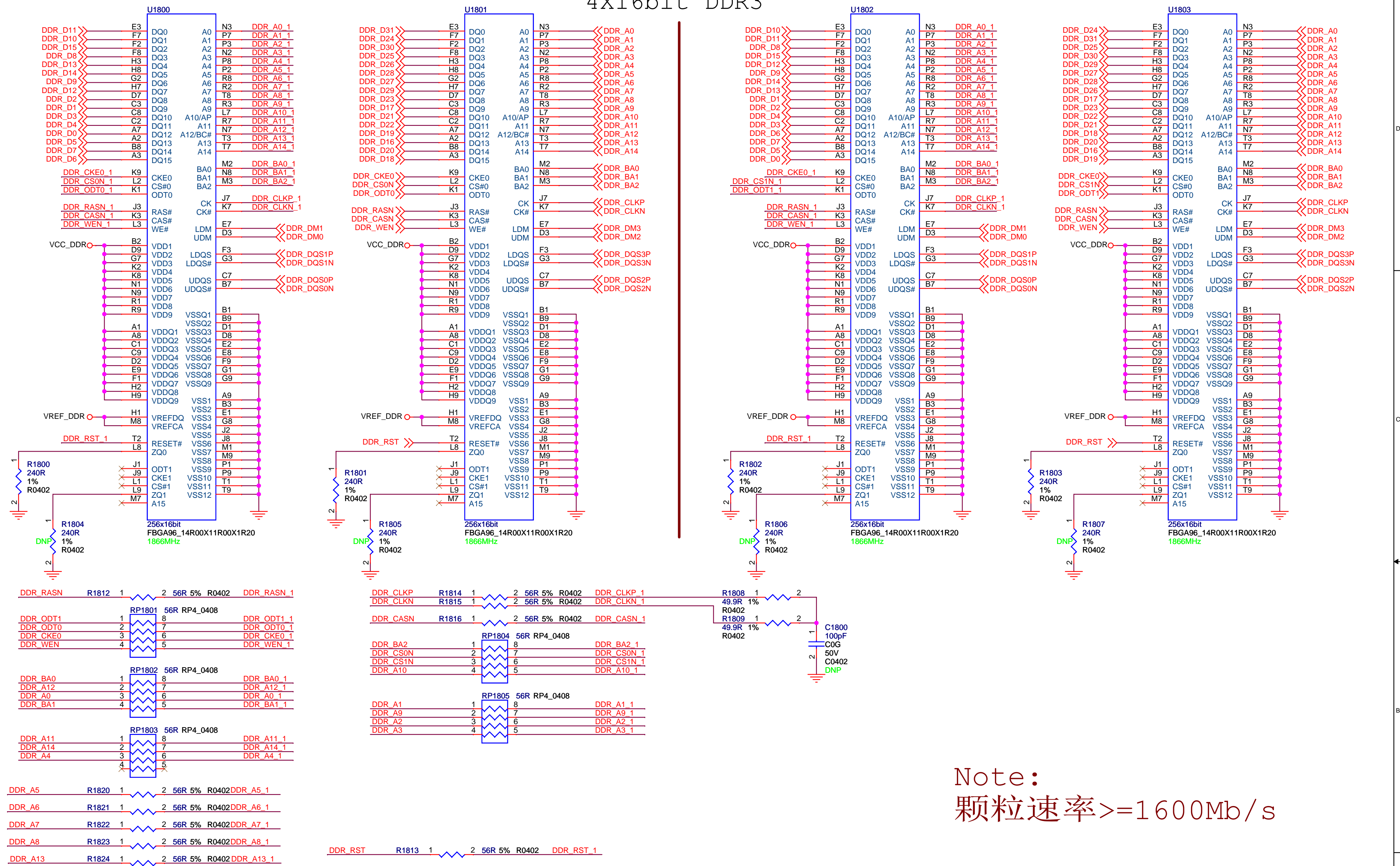






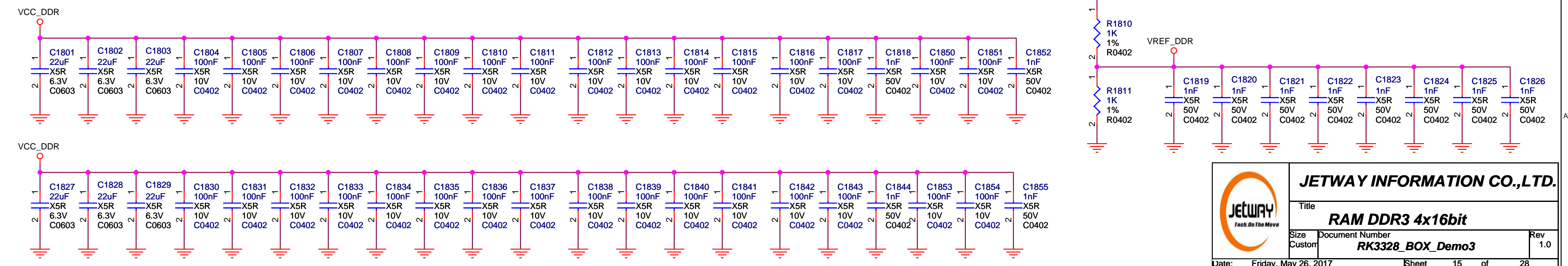
Embed FEPHY

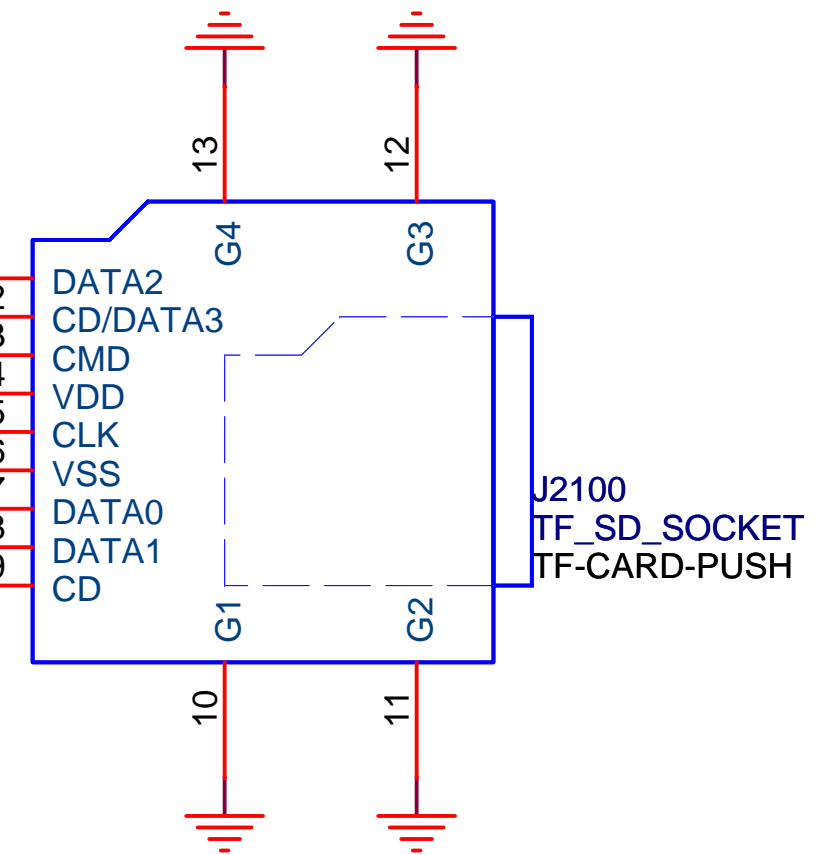
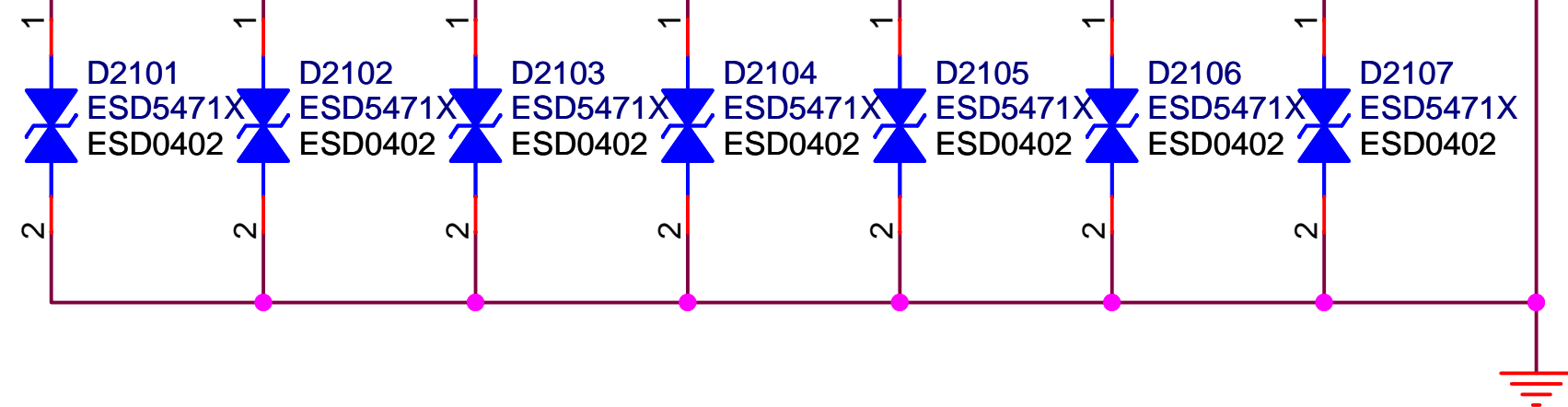
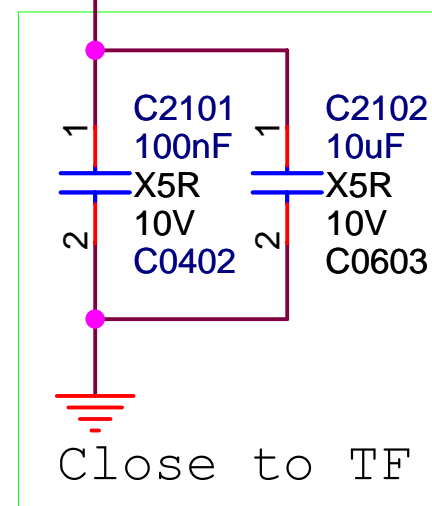
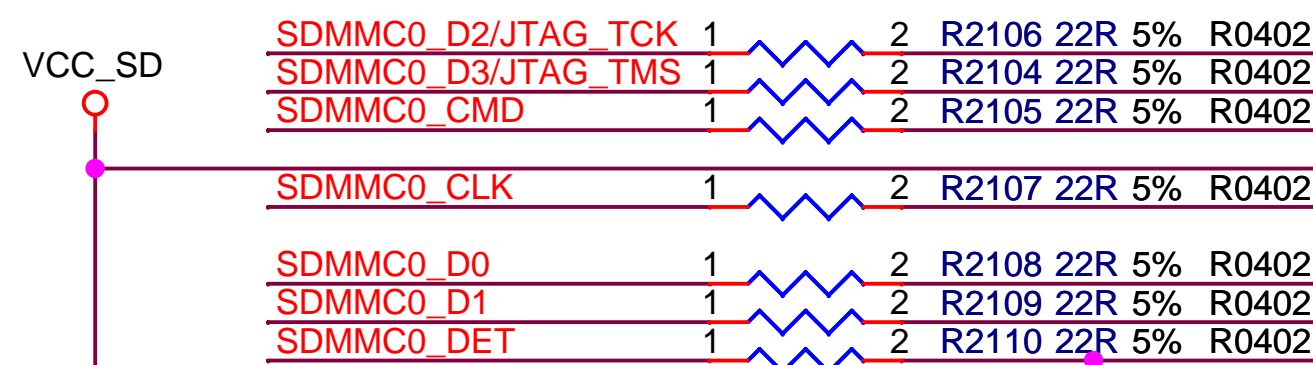
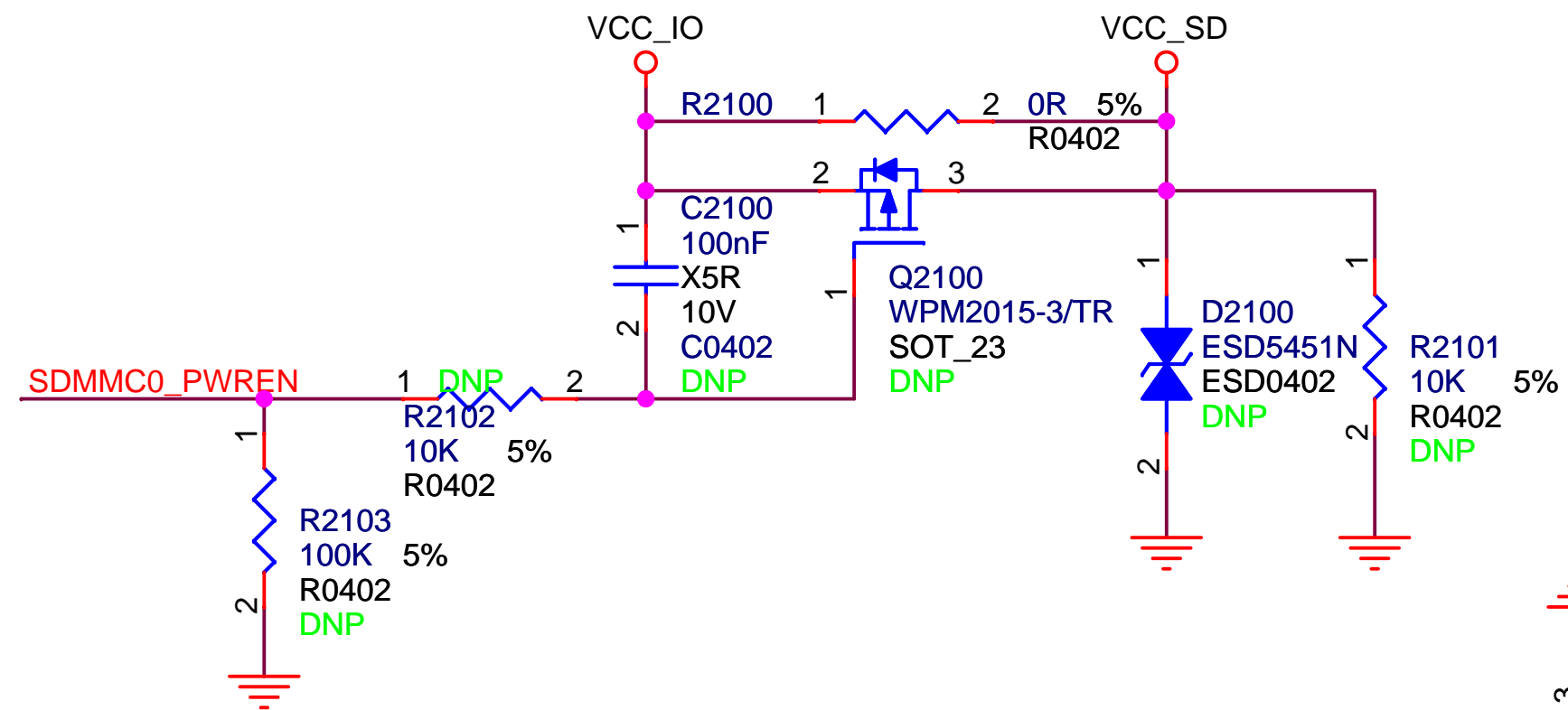
# 4X16bit DDR3



Note:  
颗粒速率 $\geq 1600\text{Mb/s}$

## DDR3 FILTER

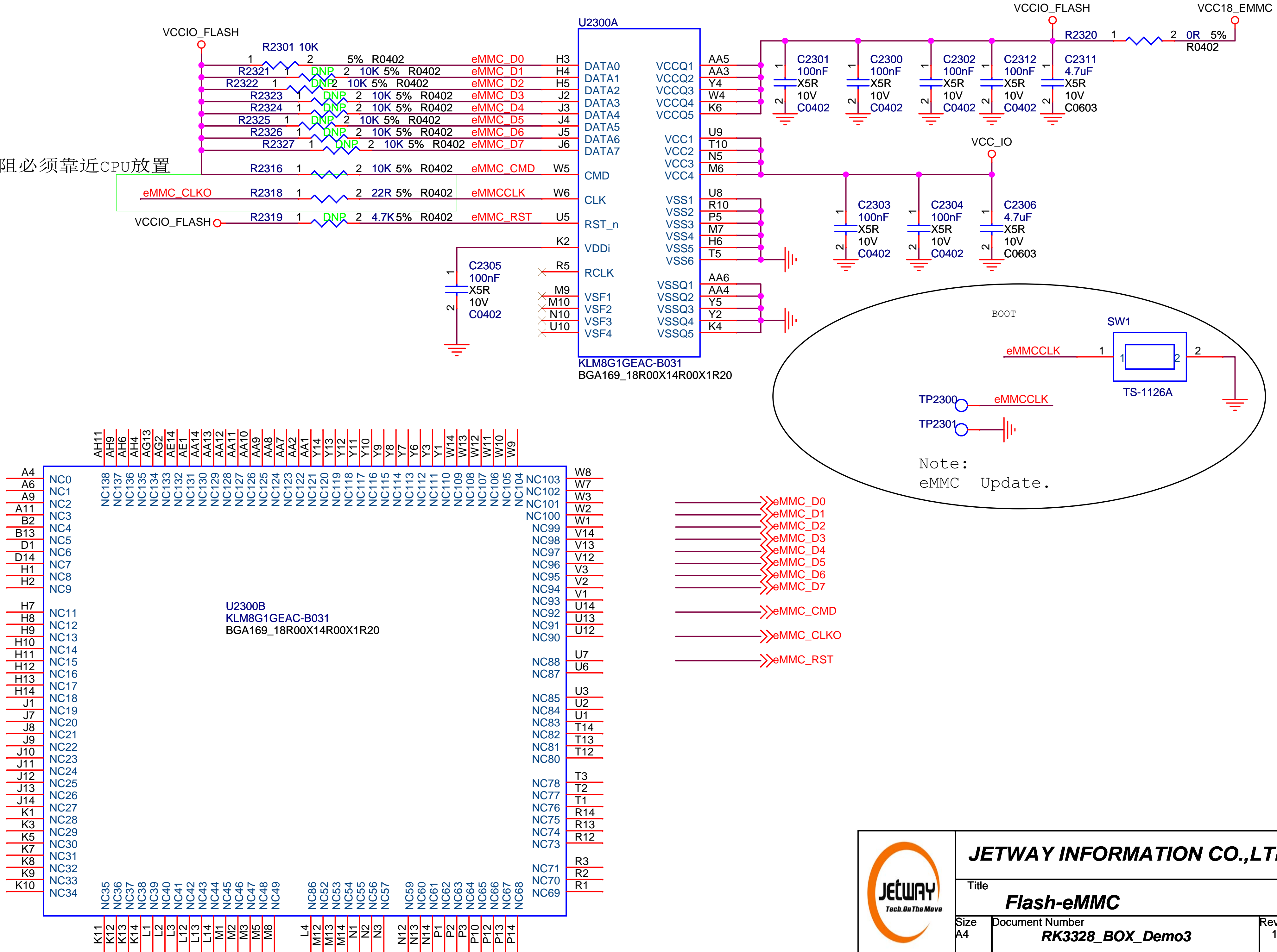


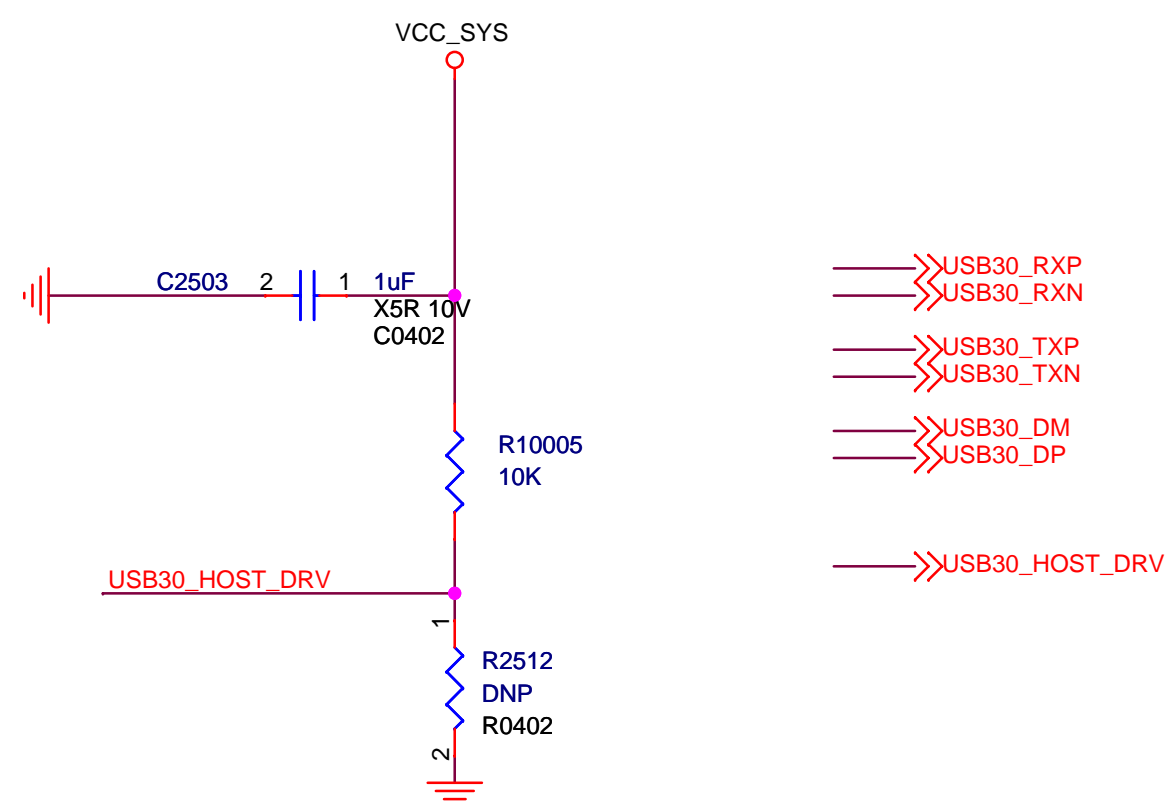
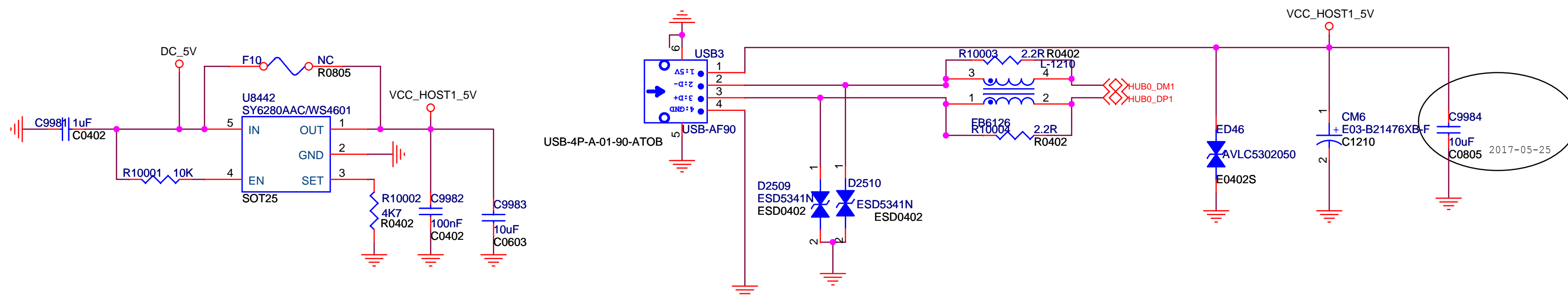
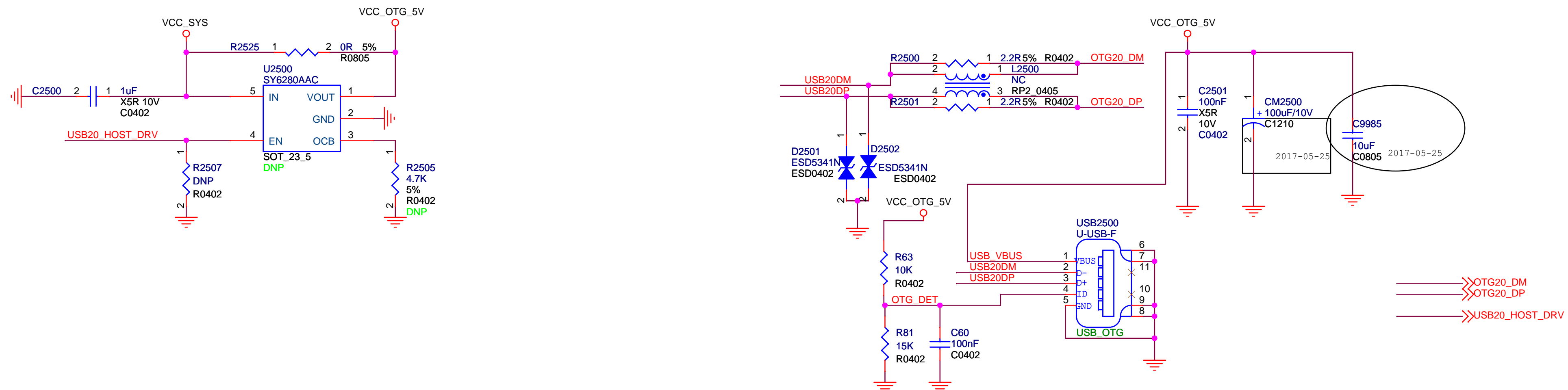


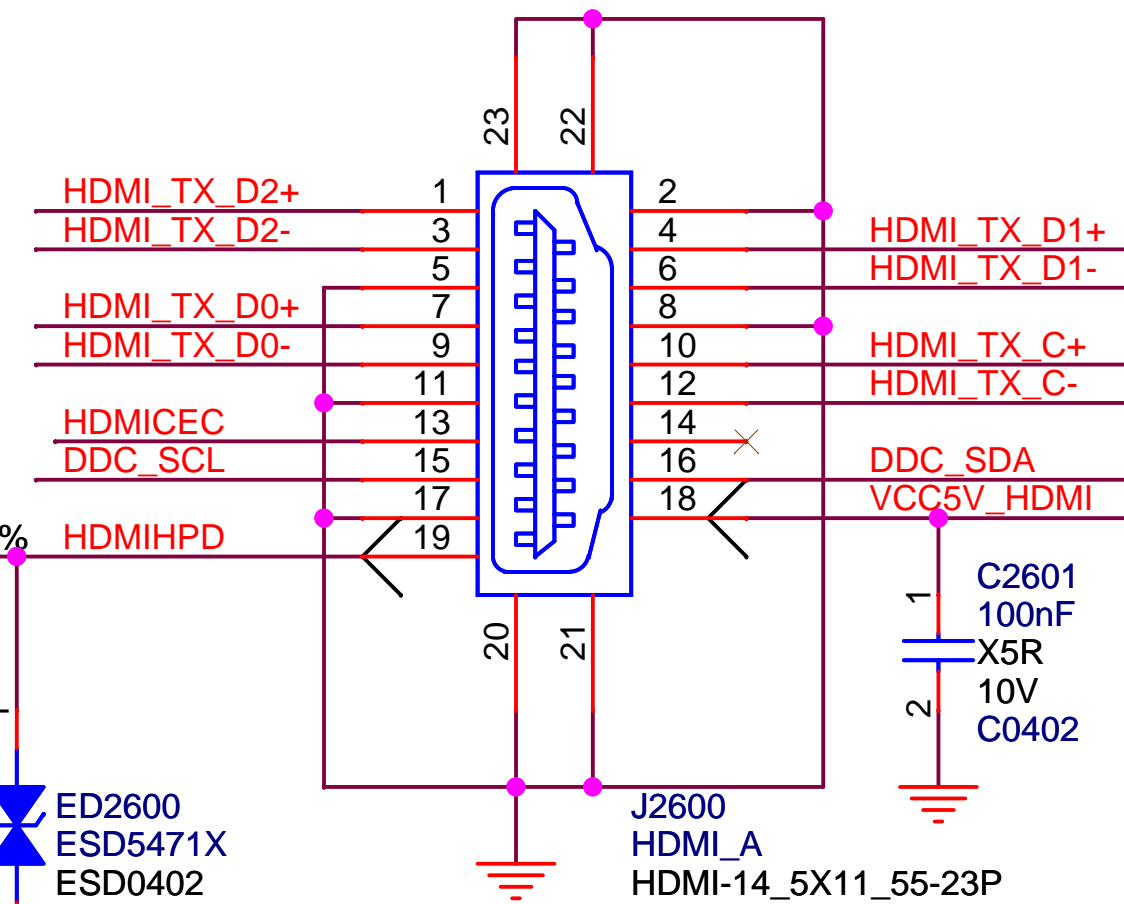
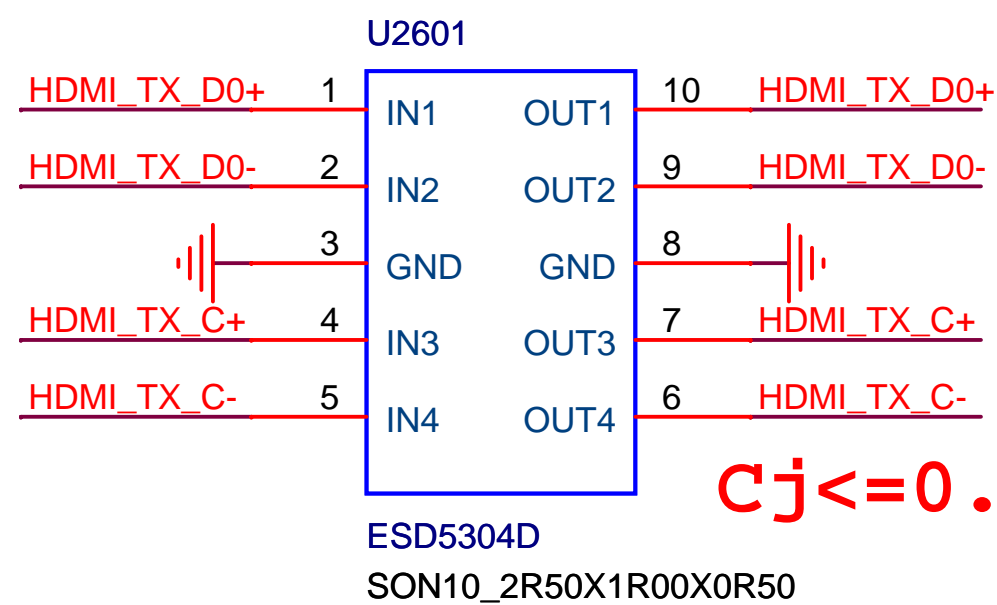
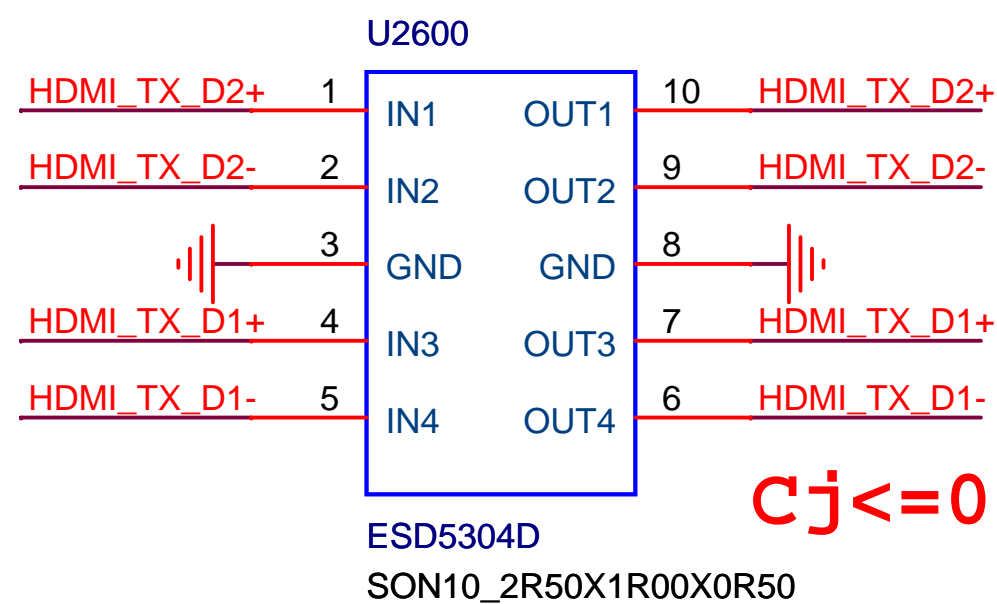
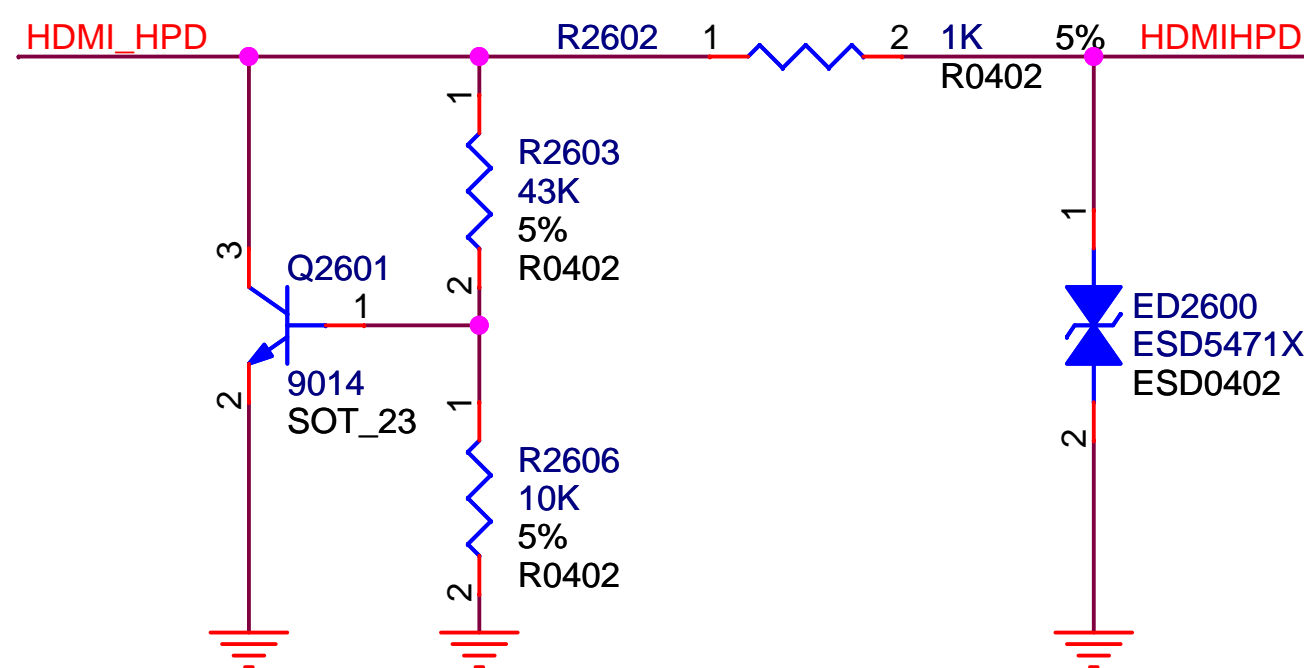
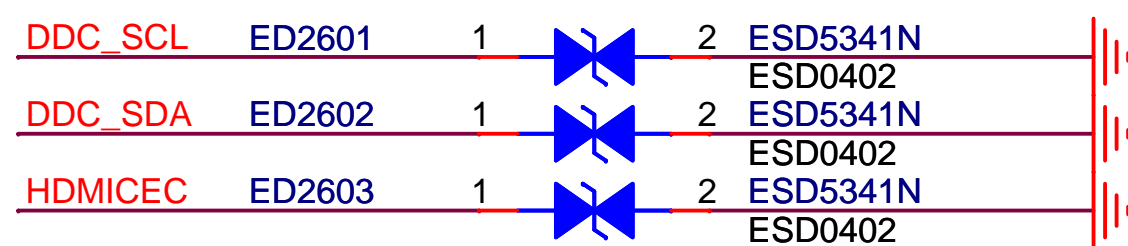
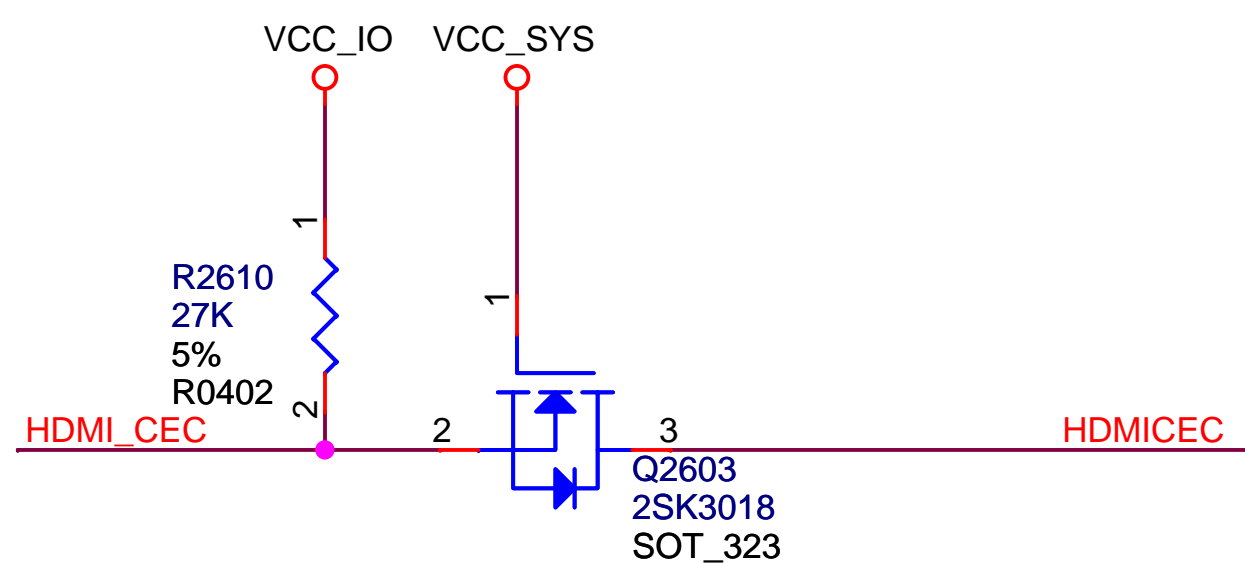
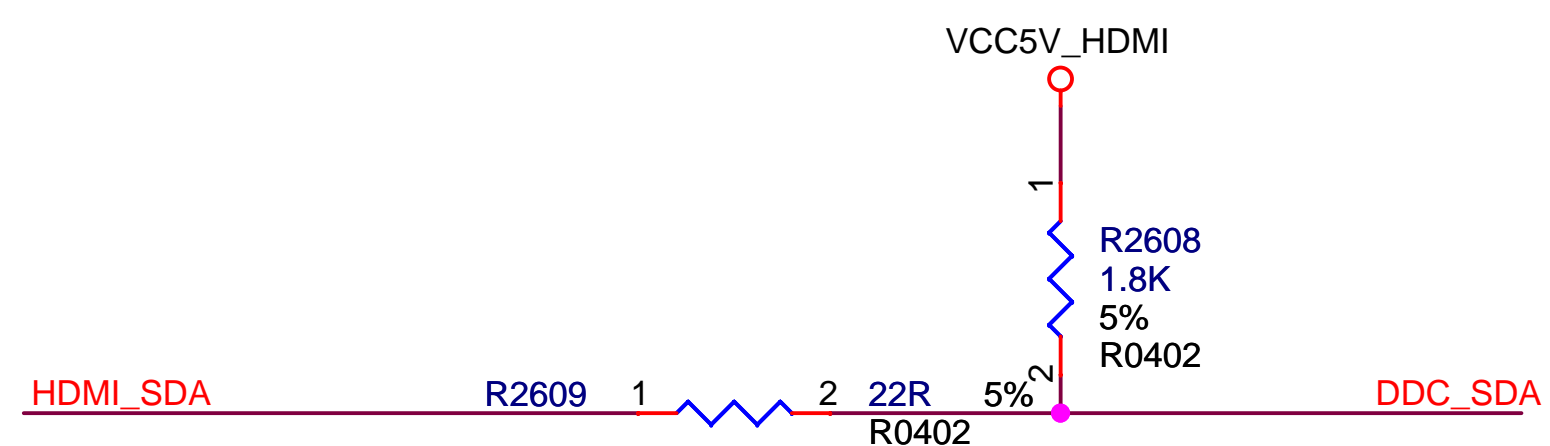
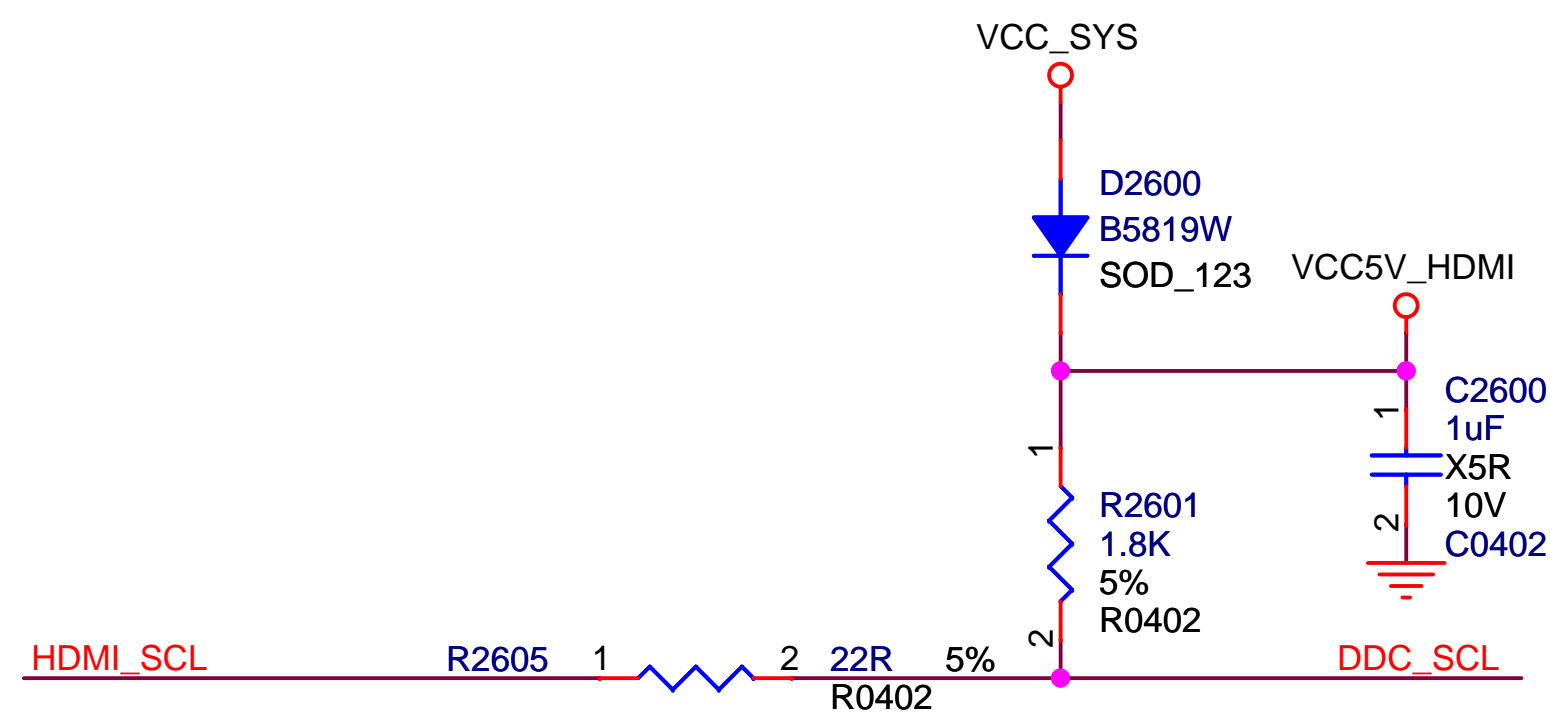
TF Card



Note:  
22R电阻必须靠近CPU放置



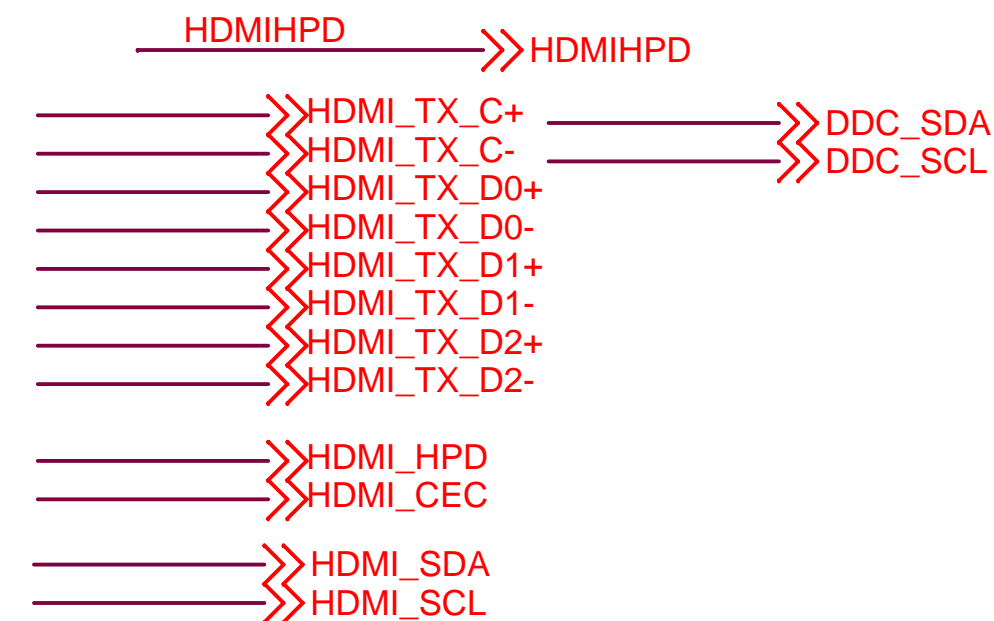




HDMI OUT

$Cj \leq 0.4pF$

$Cj \leq 0.4pF$

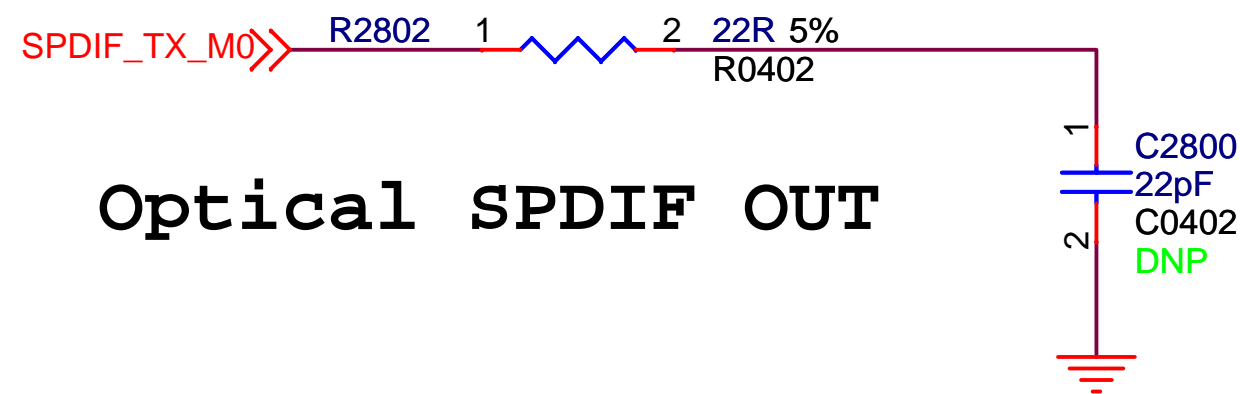


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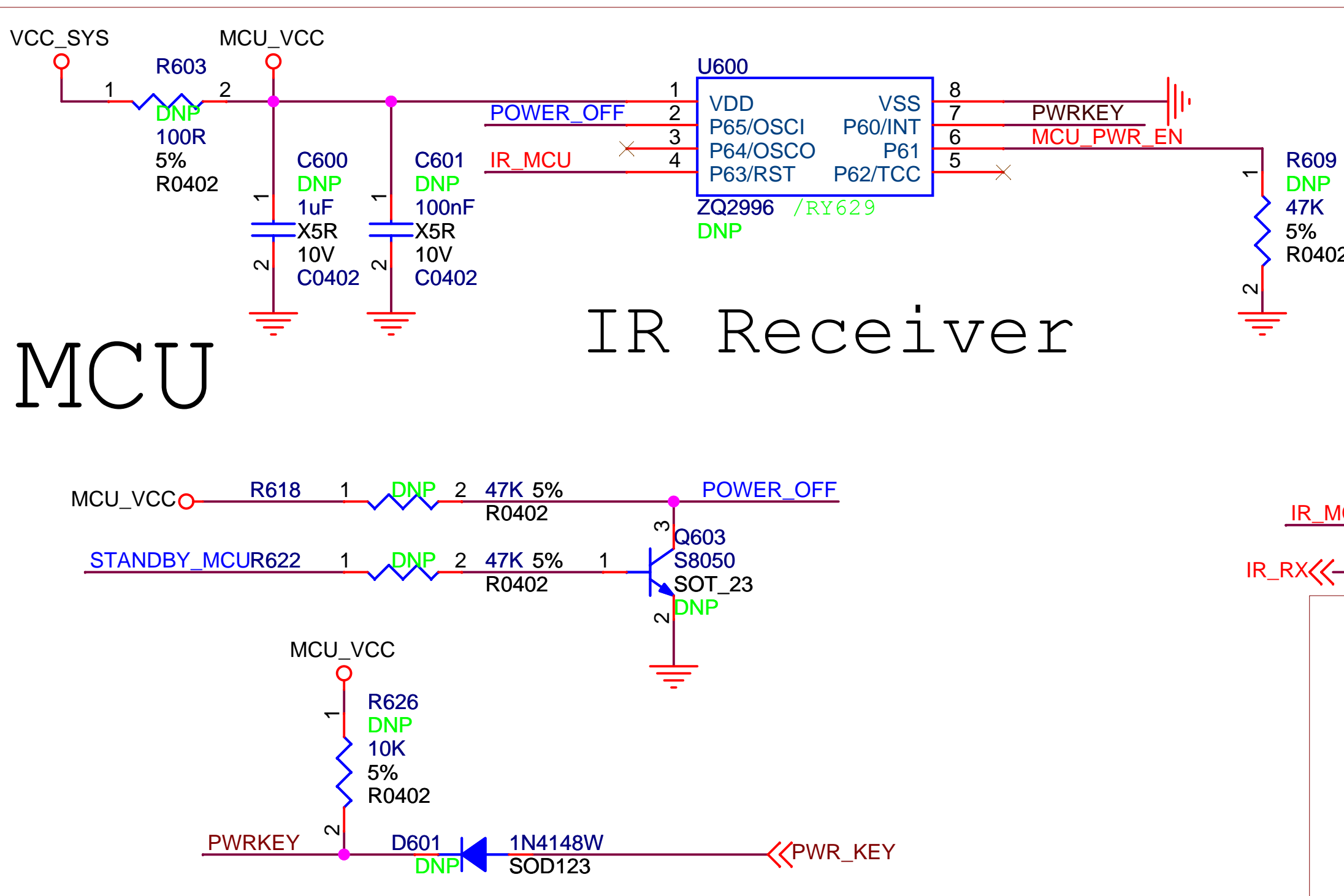
Title  
**HDMI OUT Port**

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## Optical SPDIF OUT

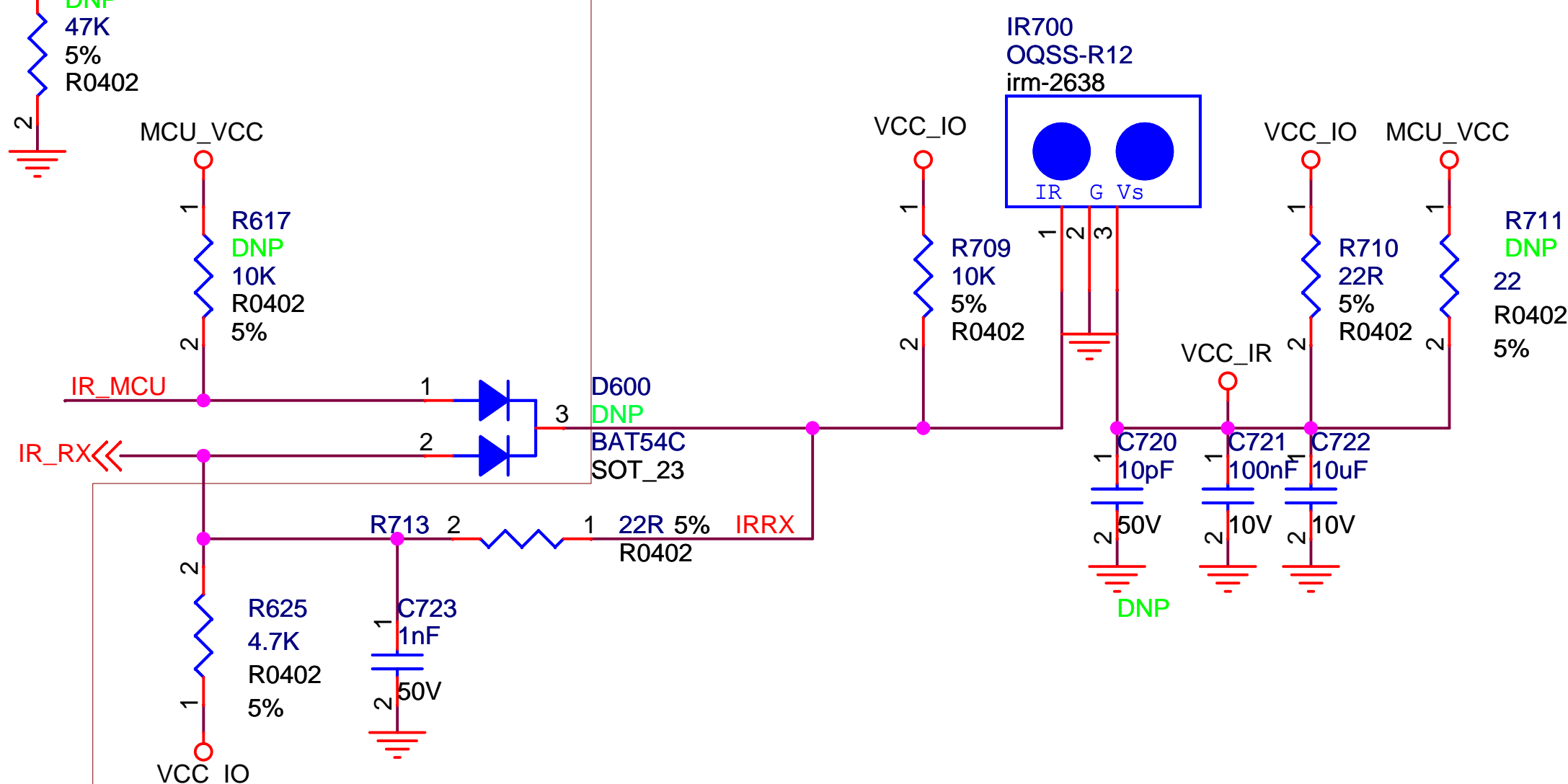


## MCU

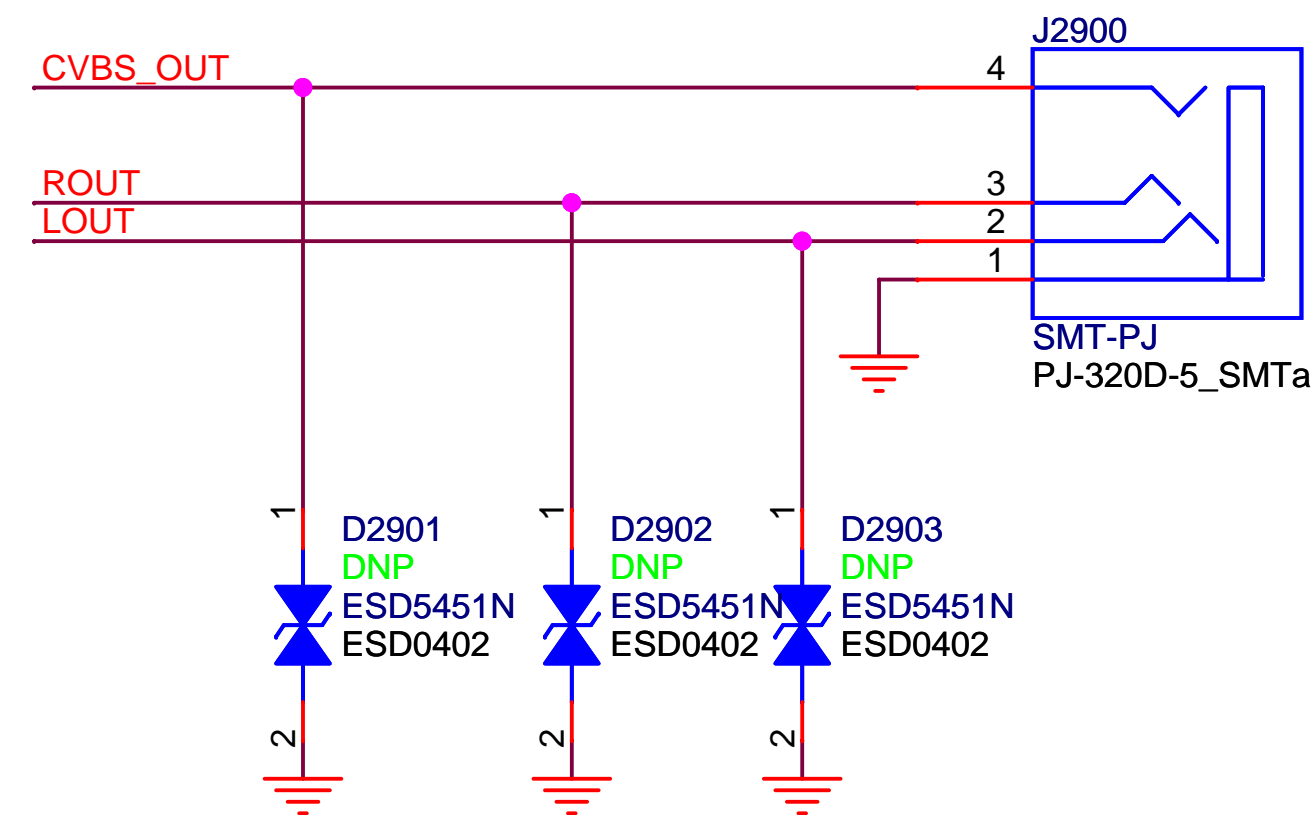
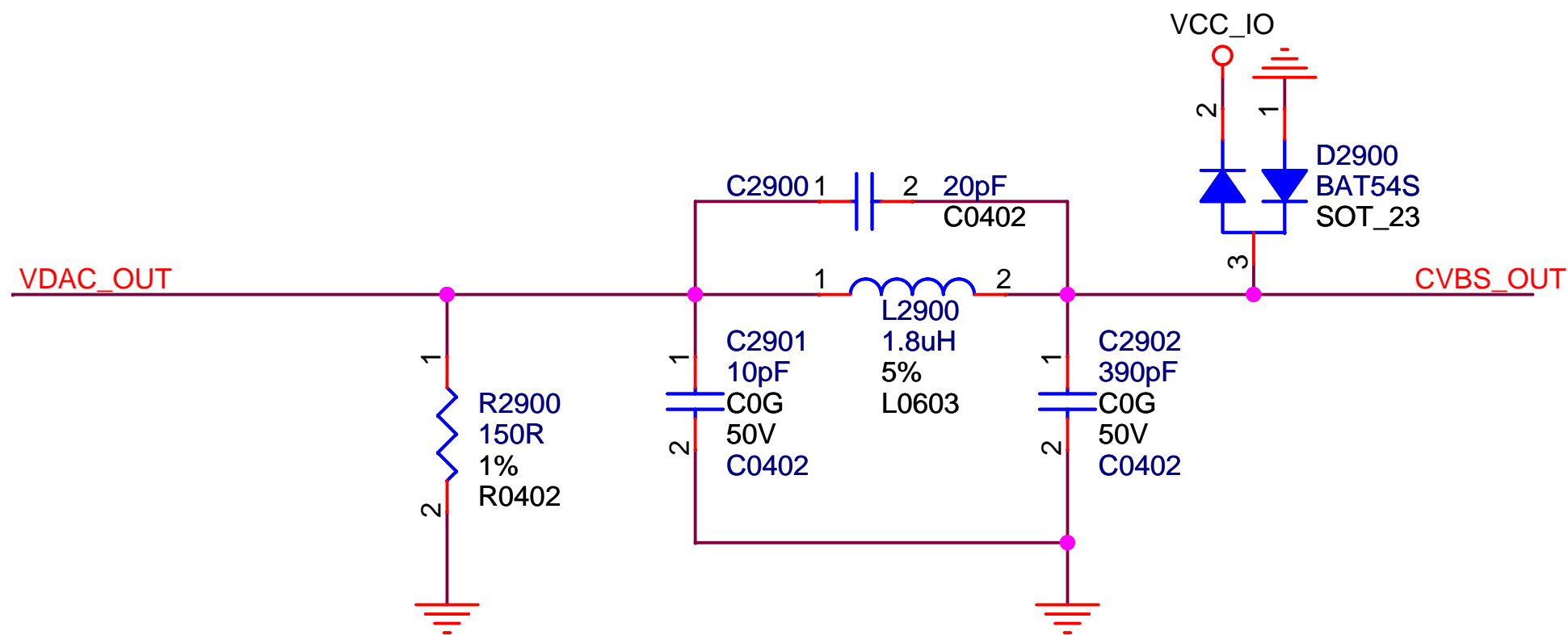
## IR Receiver


## IR Receiver

Note:  
WIFI天线不能太靠近IR接收头，  
WIFI会干扰IR接收头。  
发光二极管也有可能影响红外接收。

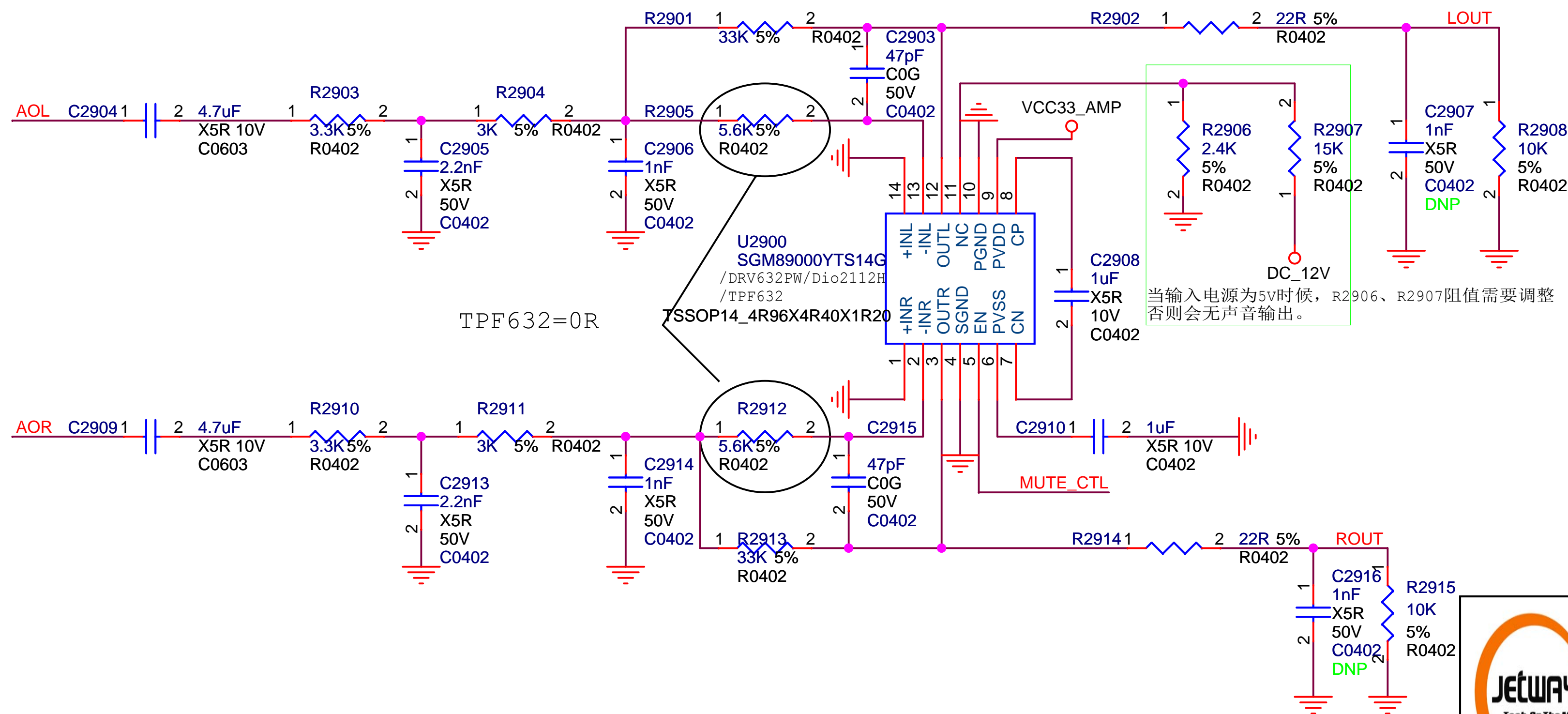






	<b>JETWAY INFORMATION CO.,LTD</b>				
	Title <b>AV OUT Port</b>				
	Size A4	Document Number <b>RK3328_BOX_Demo3</b>			Rev 1.0
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**AV OUT**

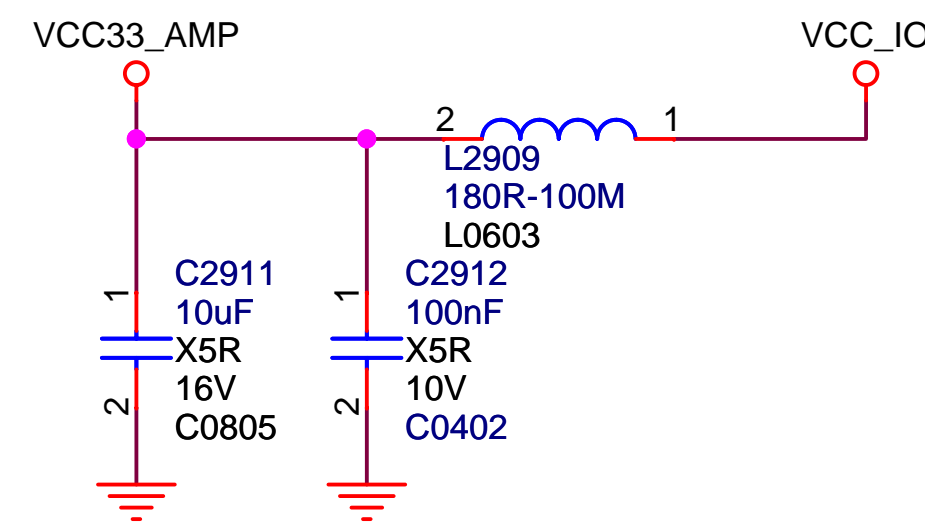


VDAC\_OUT

AOL


AOR

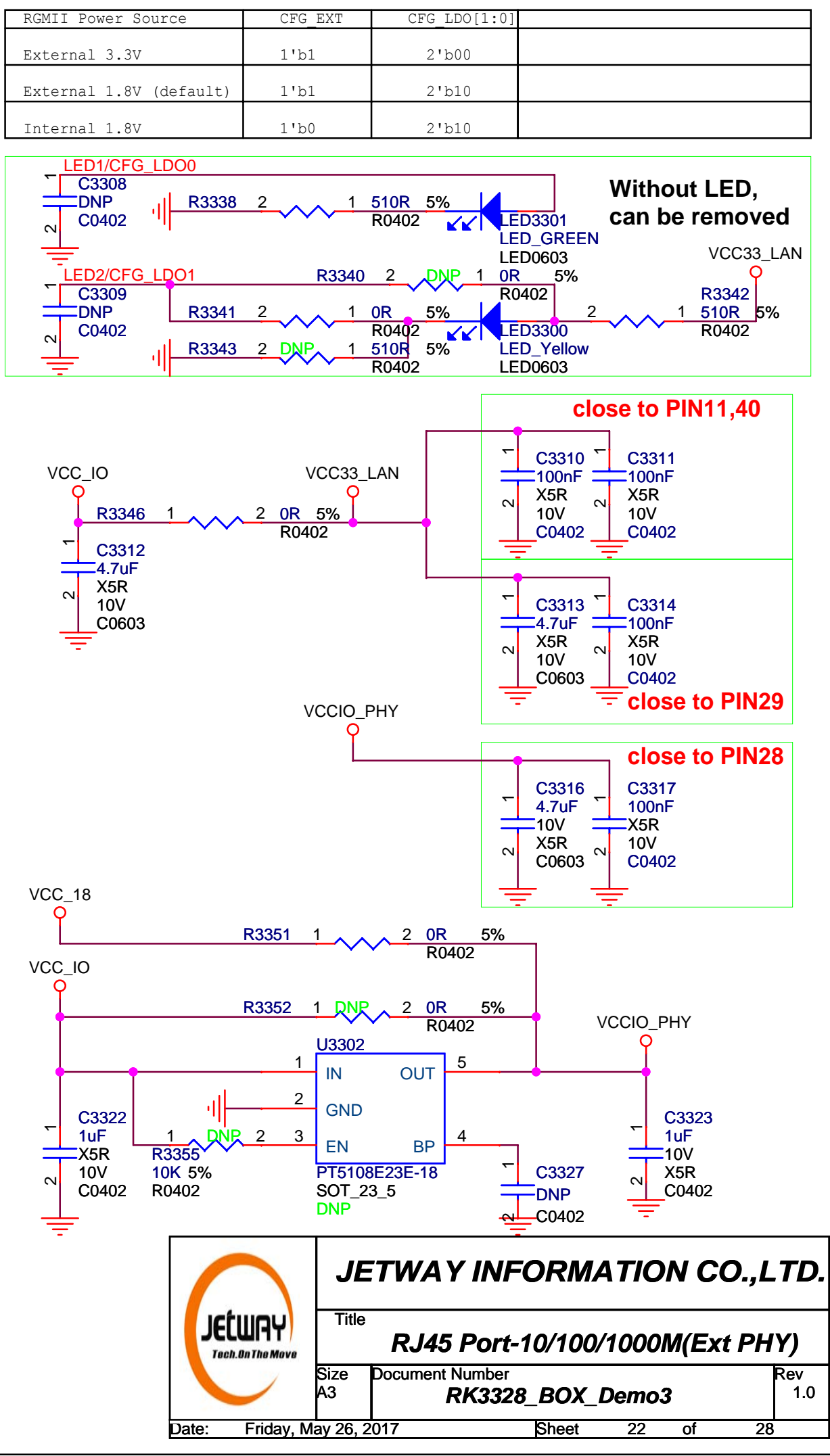
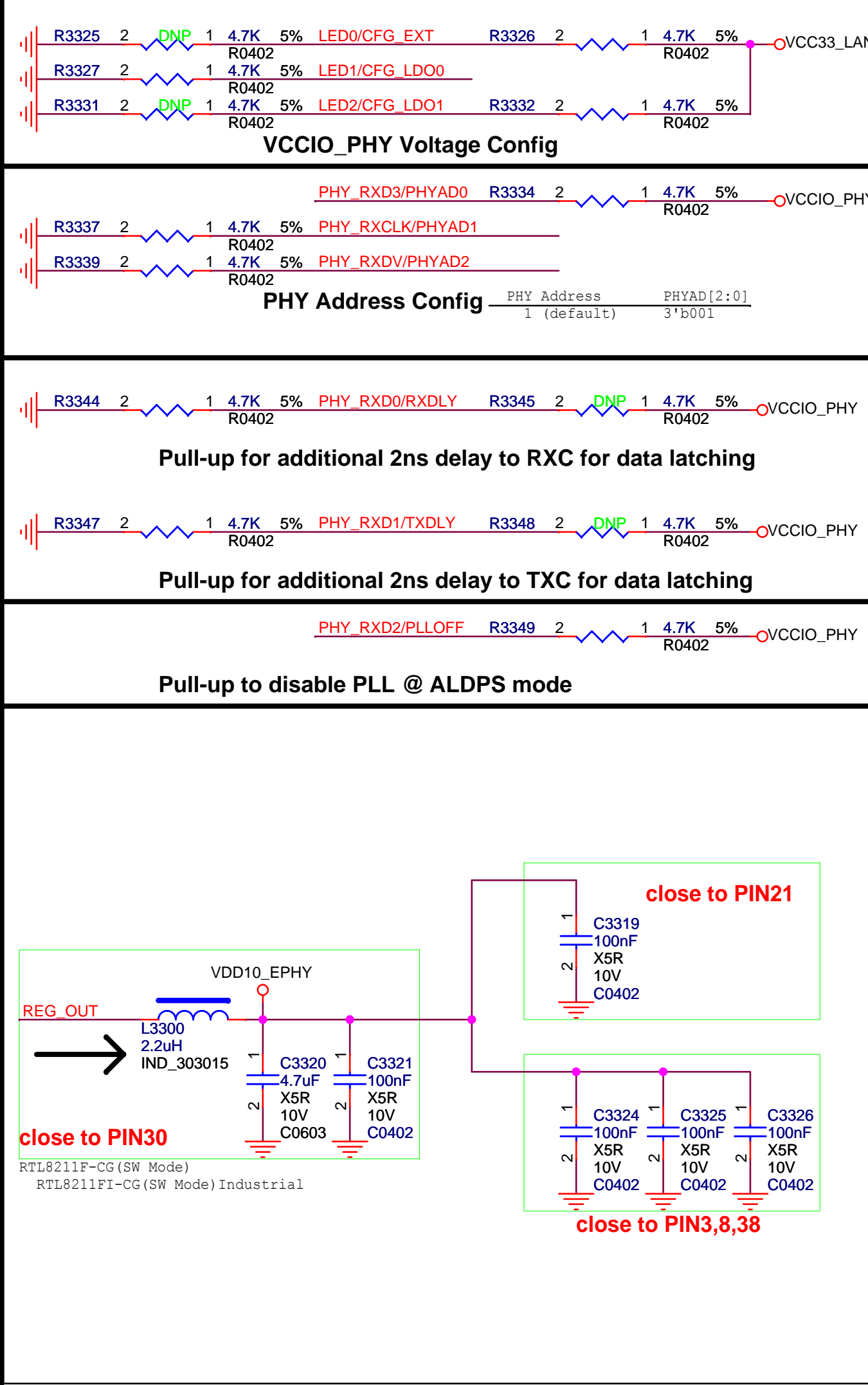
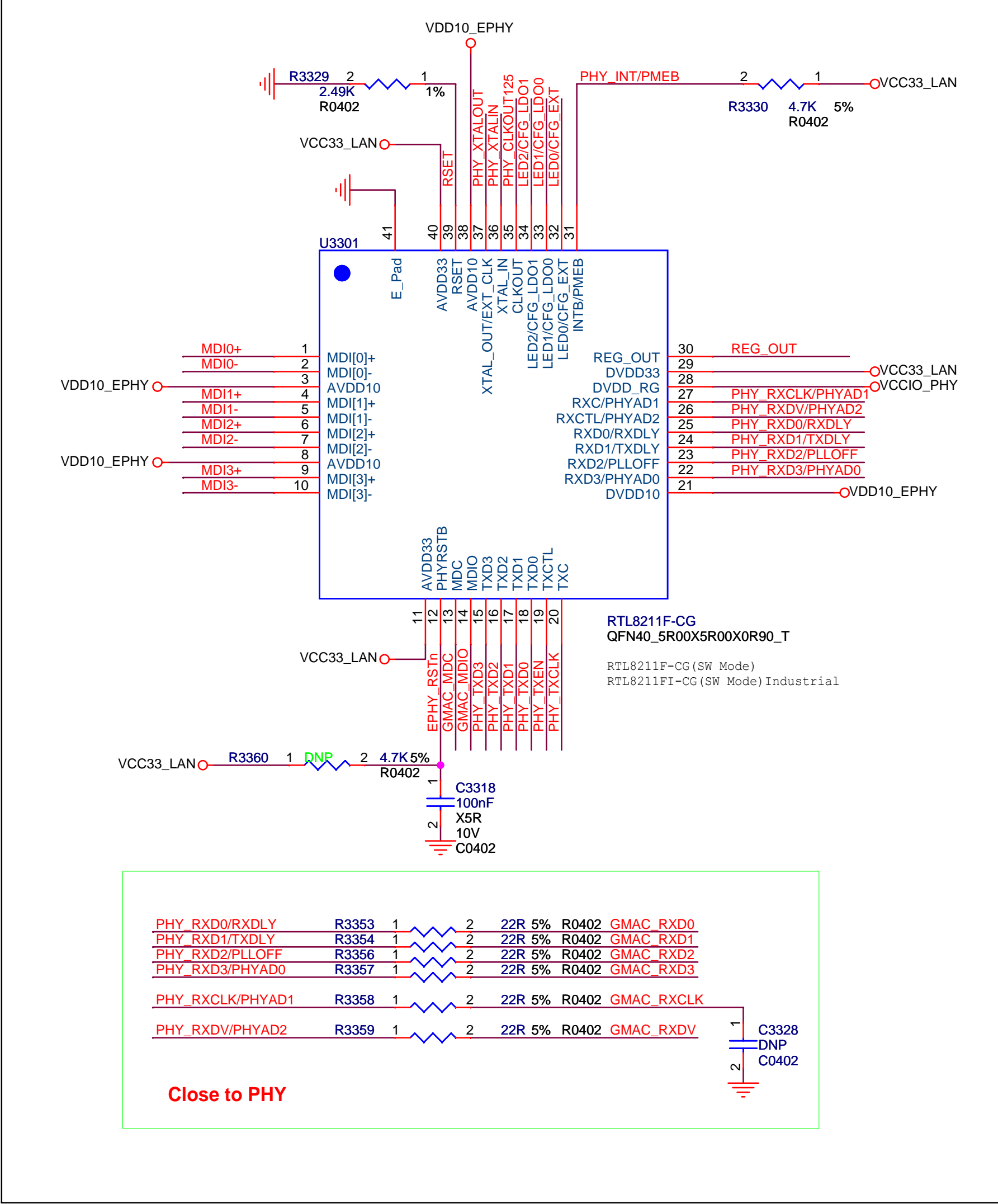
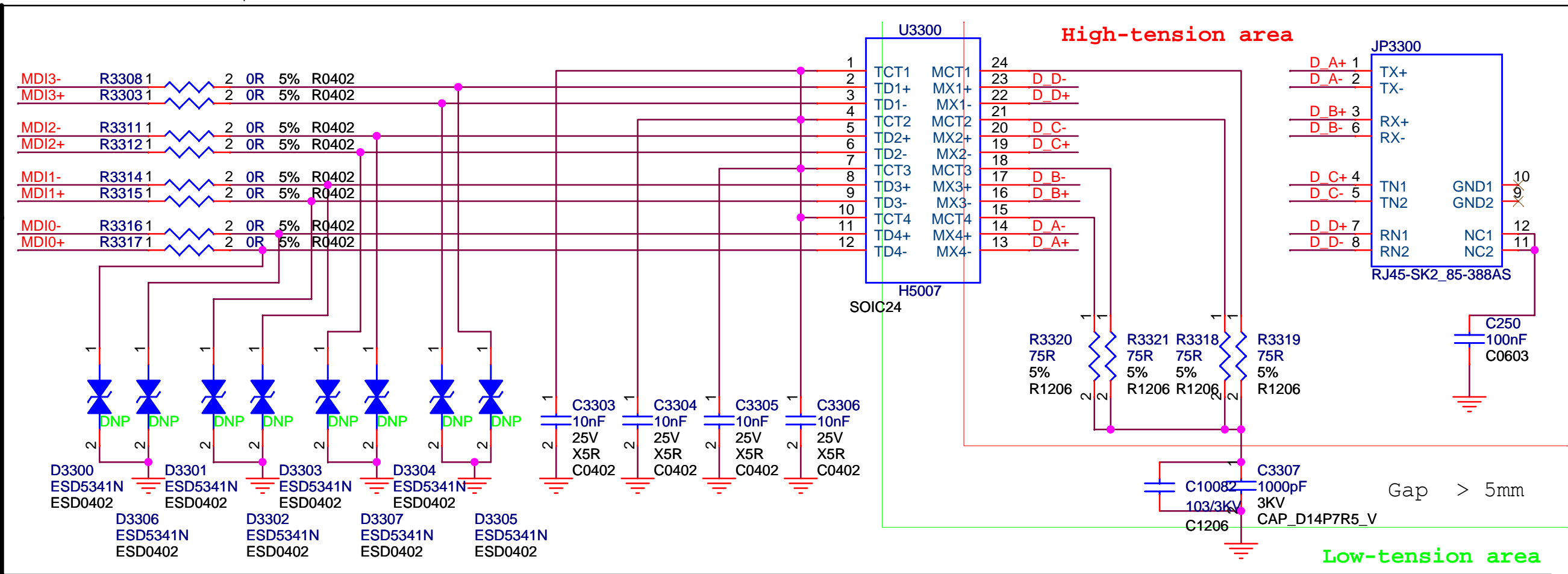
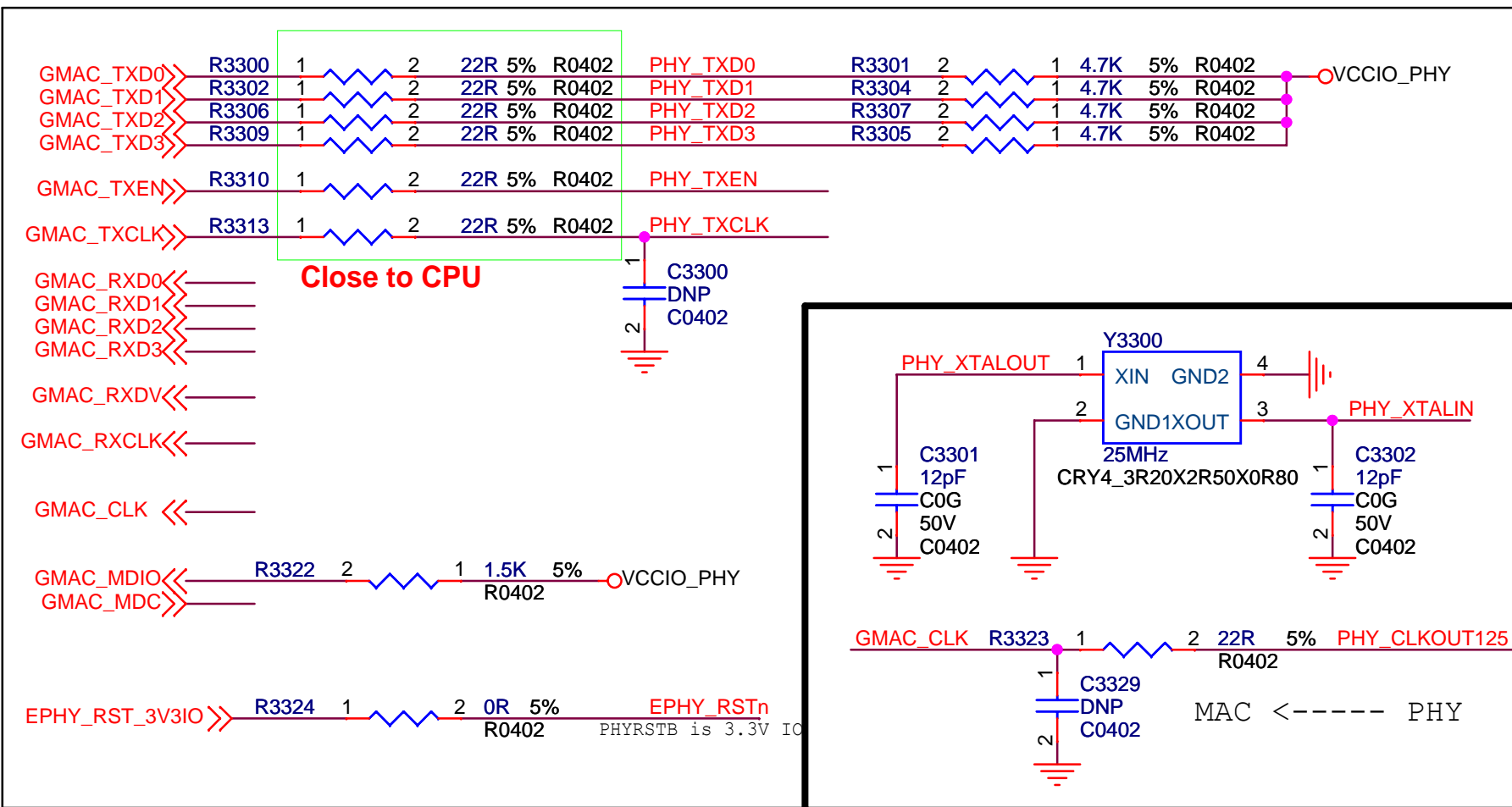
MUTE\_CTL

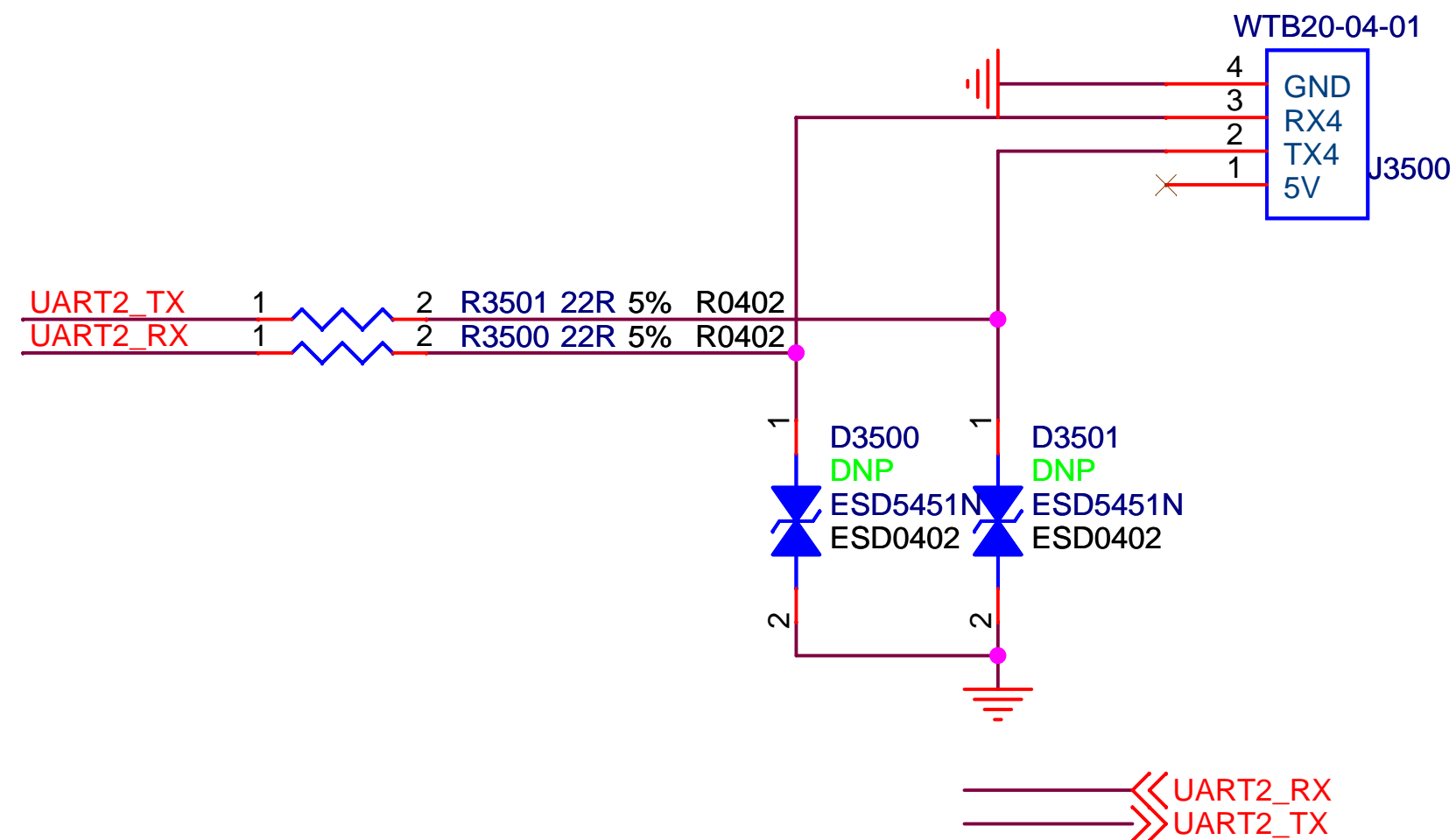


**2-Vrms Audio Line Driver**

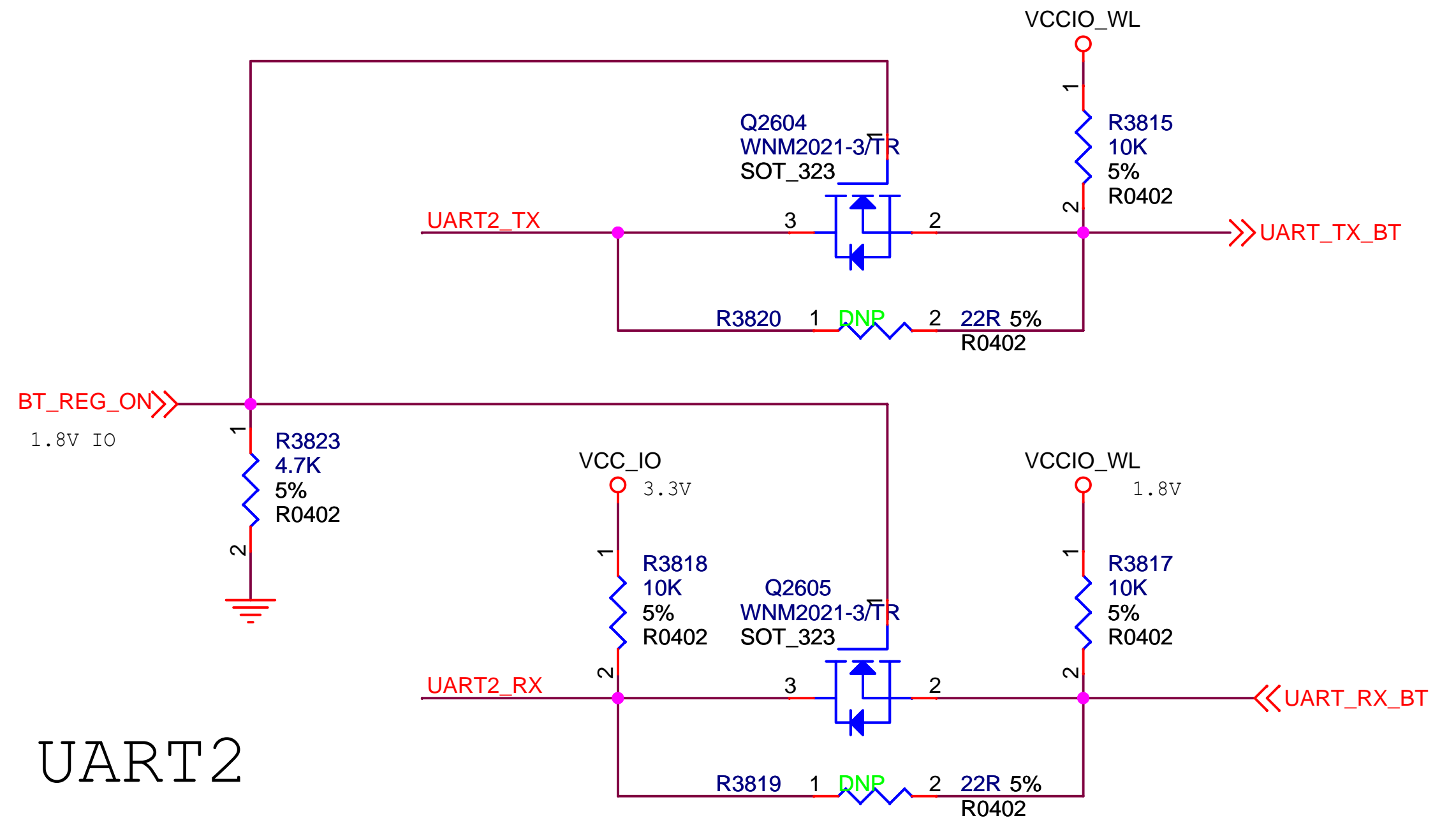
2

	<b>JETWAY INFORMATION CO.,LTD.</b>		
	Title <b>AV OUT Port</b>		
	Size A4	Document Number <b>RK3328_BOX_Demo3</b>	Rev 1.0
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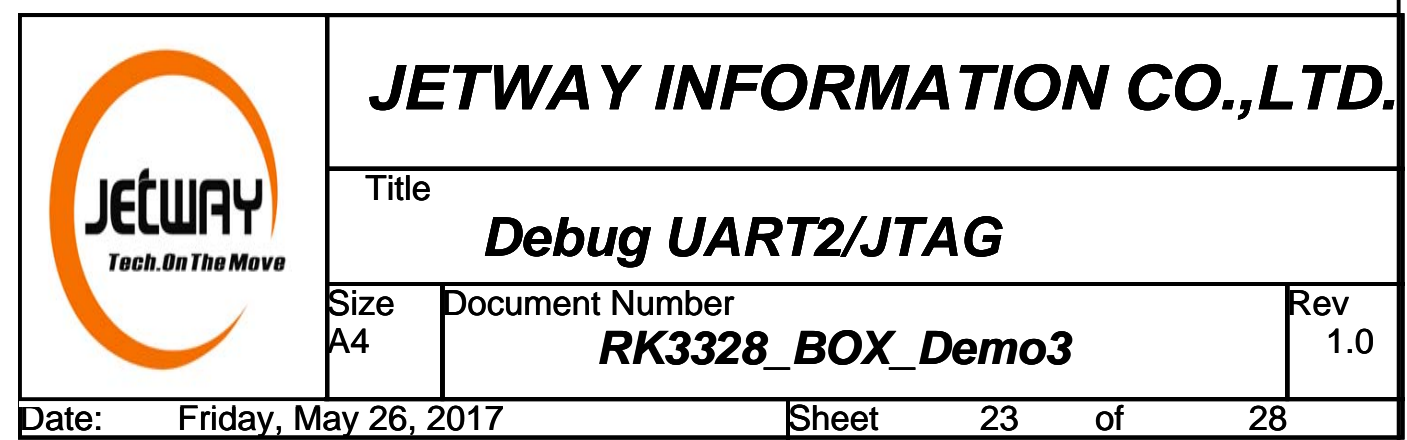
## Debug UART2



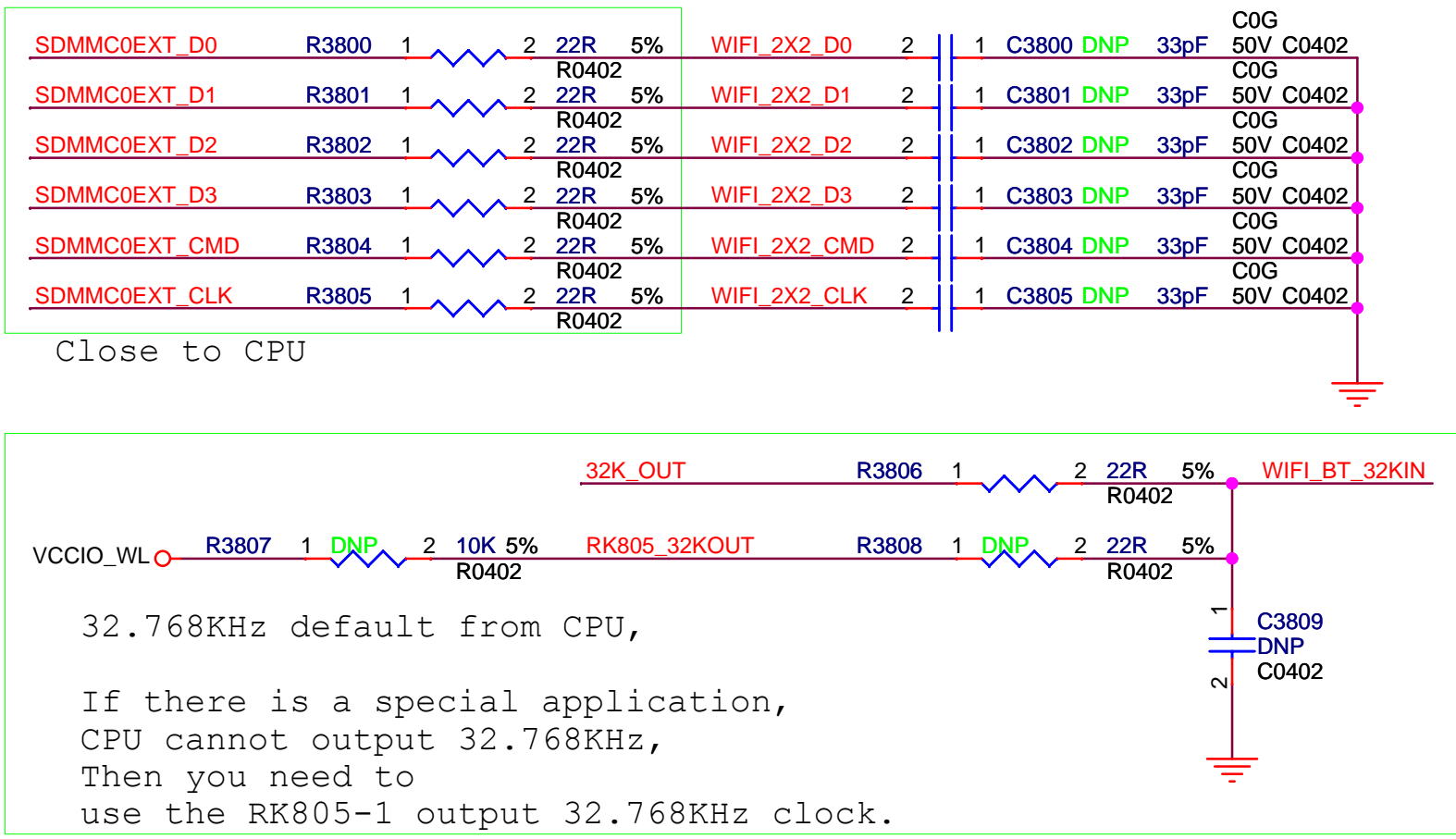
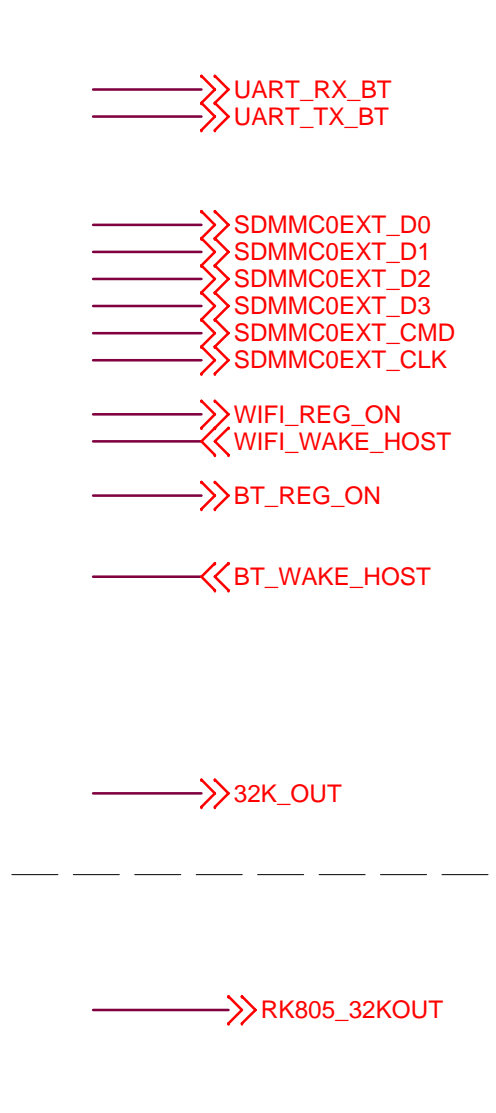
BT UART2

BT ON: BT UART, 需移除Debug uart小板

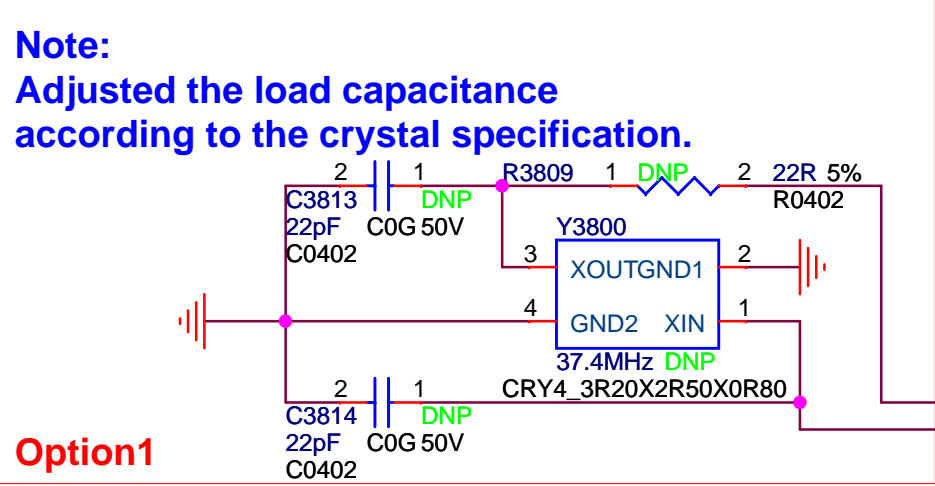
BT OFF: Debug UART2, 可接debug uart小板







Layout Note:  
Crystal away from antenna

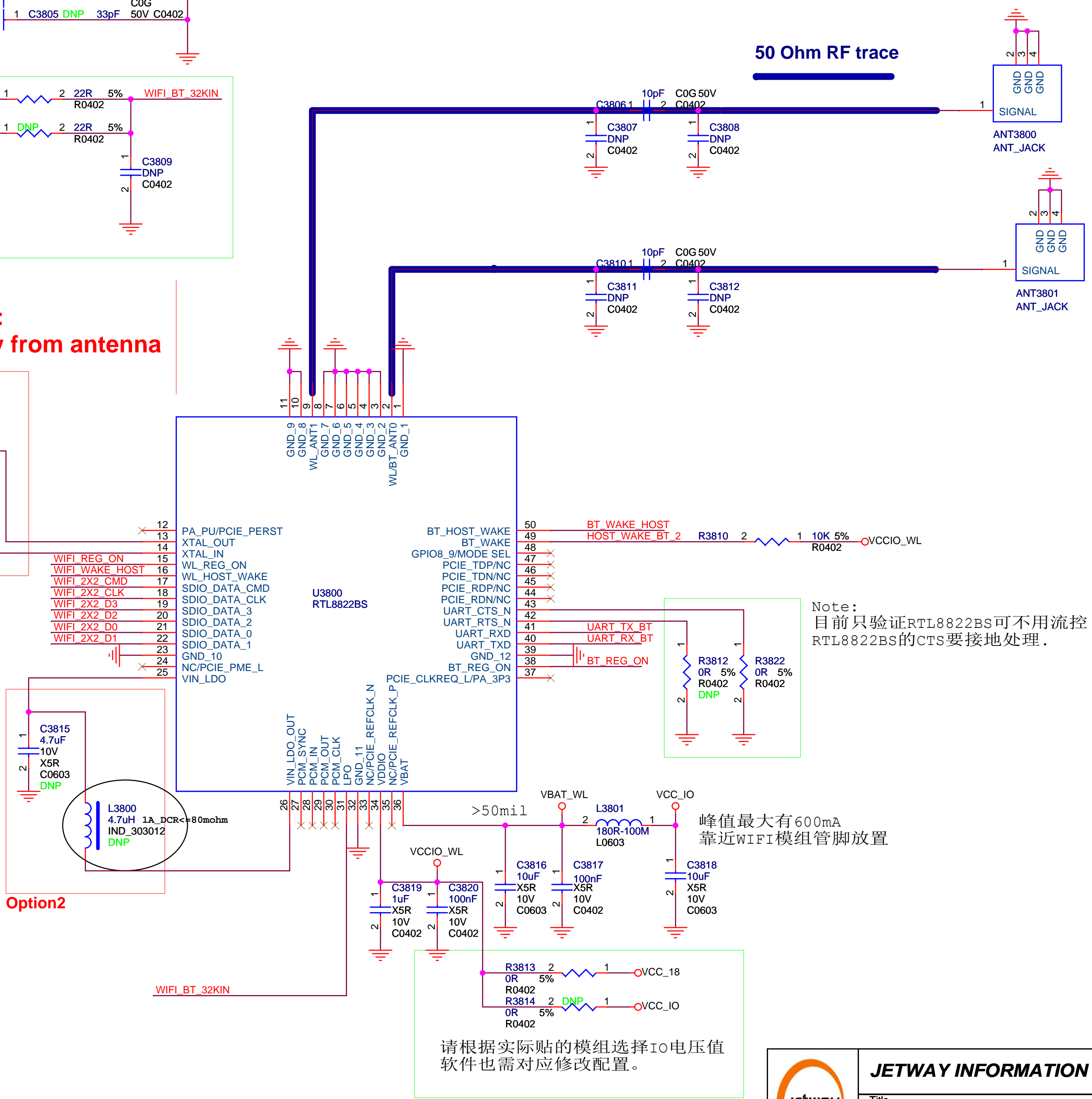


## 2T2R

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
RTL8822 模组	Yes	Yes	Yes	Yes	Yes		1.7-3.6V
RTL8192 模组	No	Yes	No	No	No		1.7-3.6V

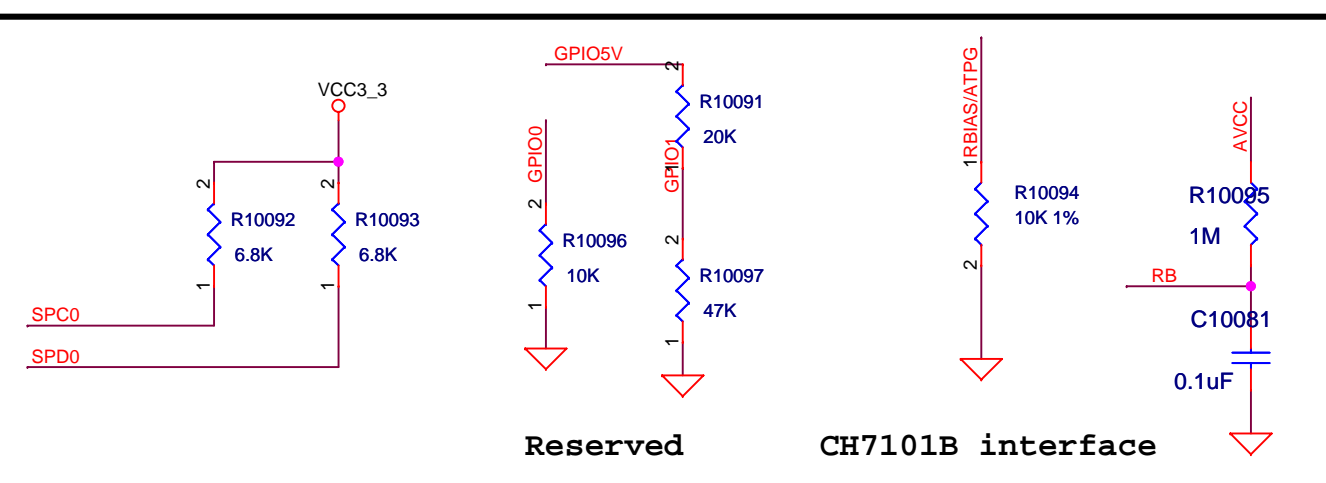
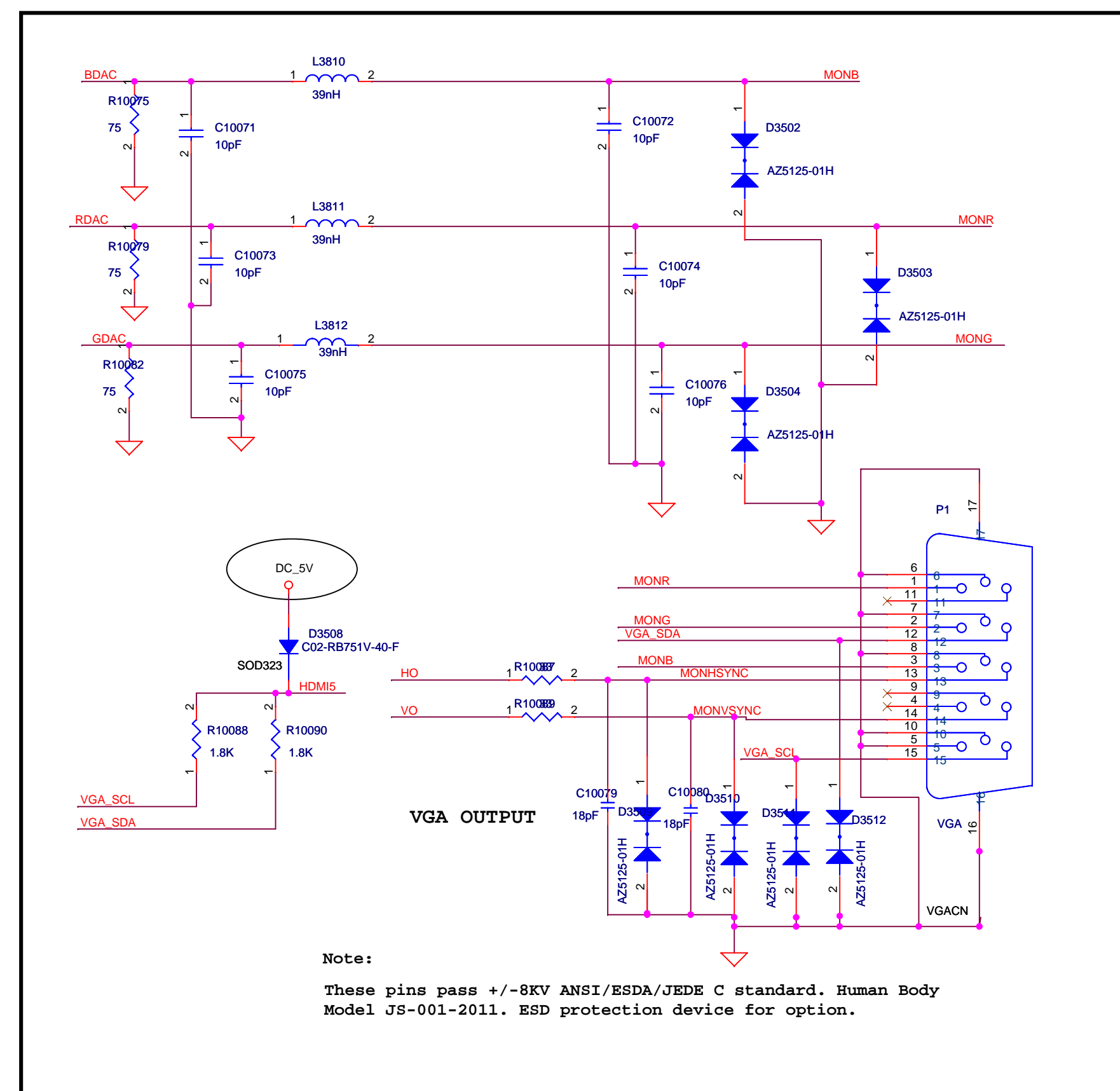
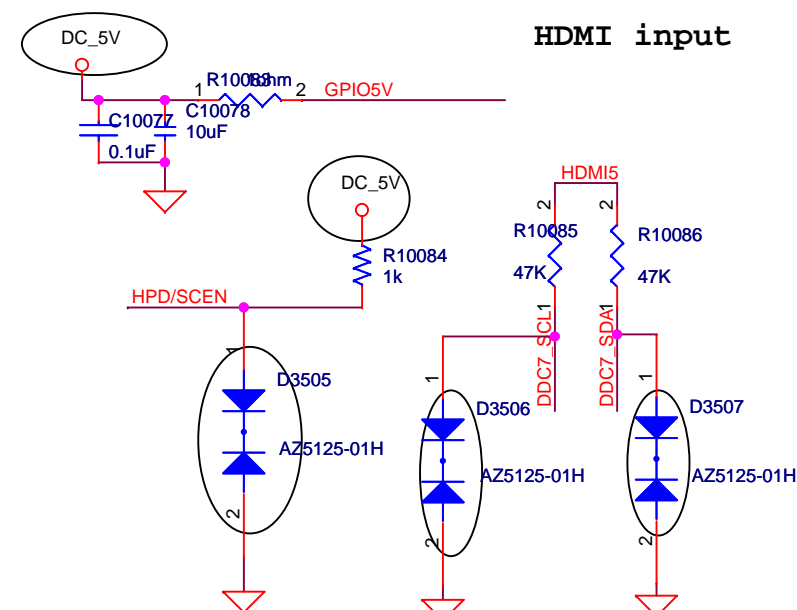
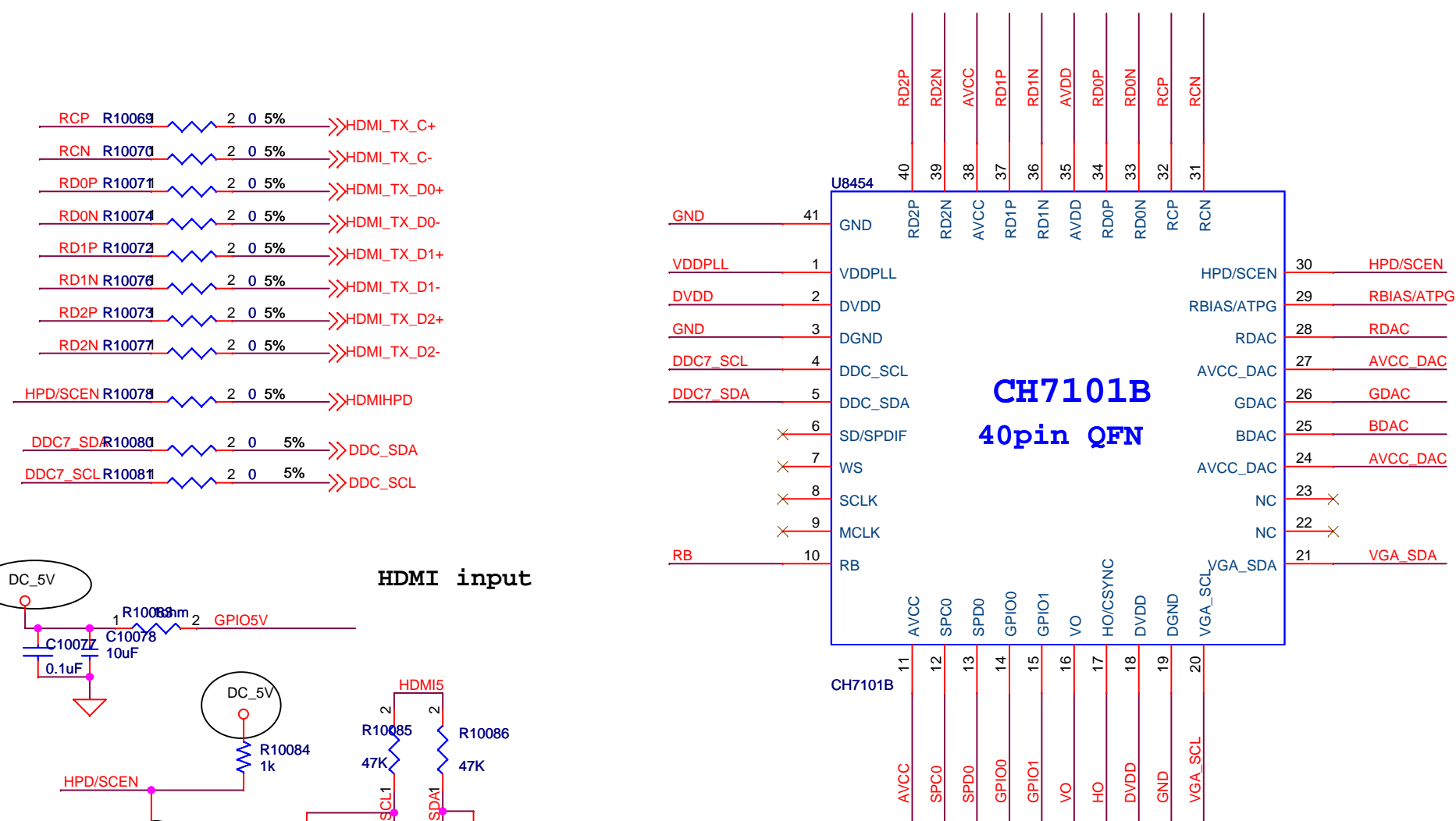
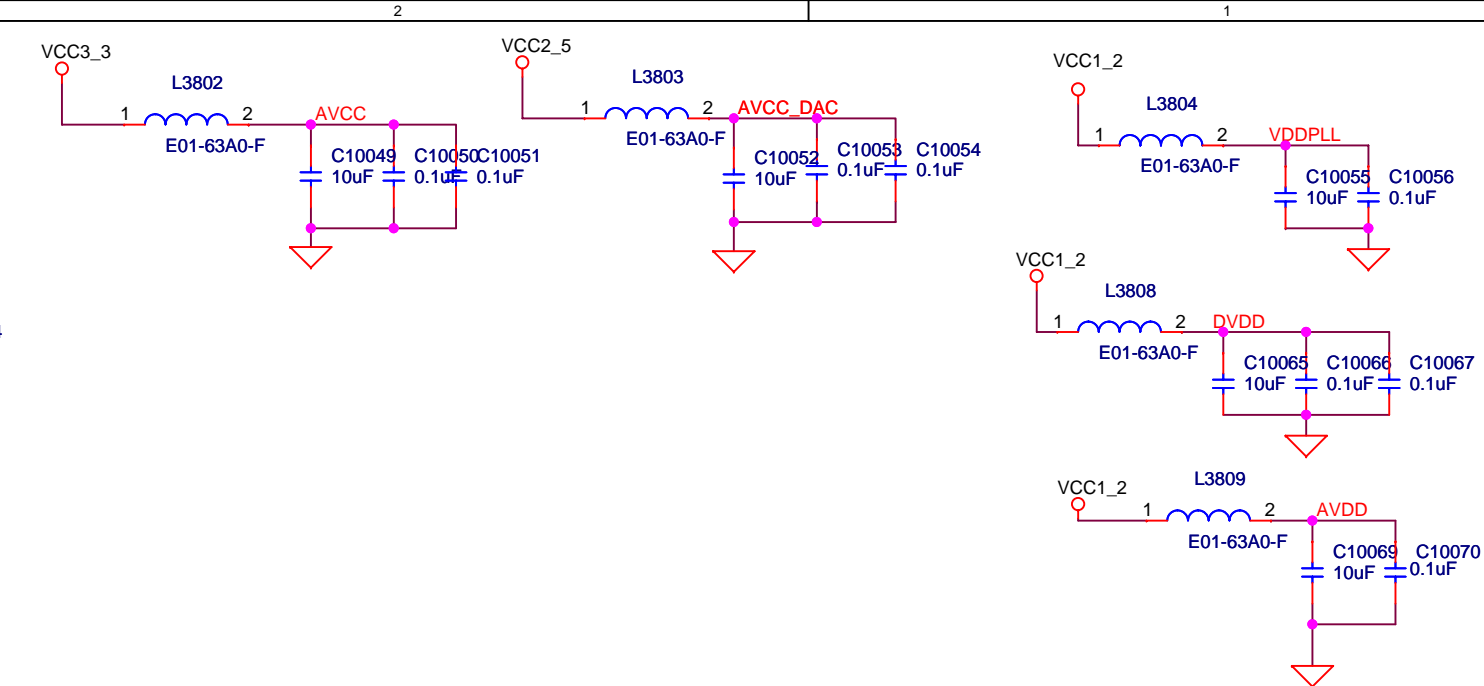
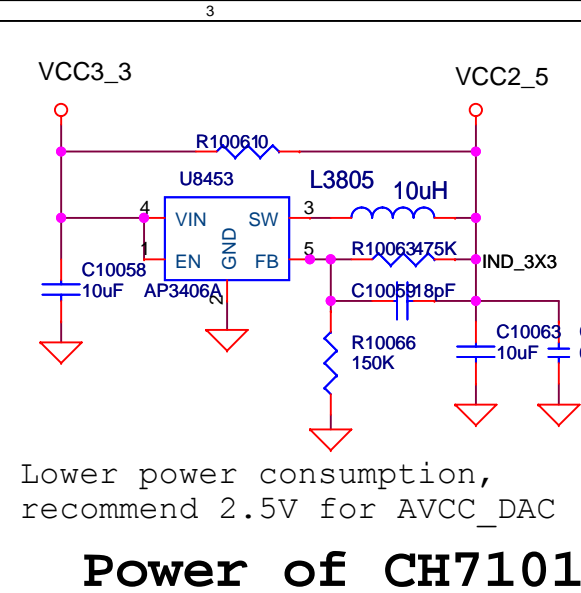
OPTION	1	2	3		
RTL8822 模组	No	No			
RTL8192 模组	No	No			

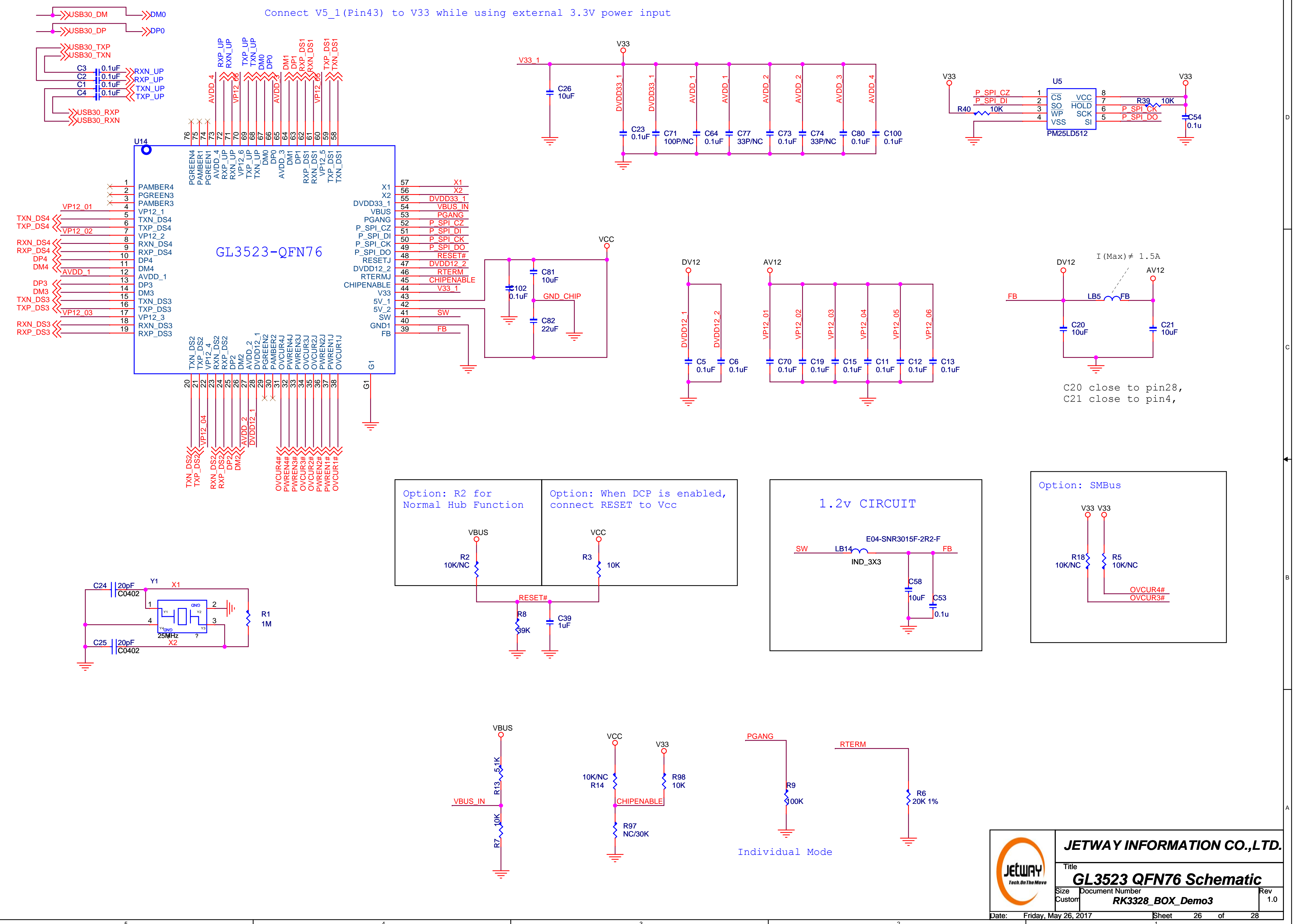
Note:  
Yes:框内要贴  
No:框内不贴



Note:  
目前只验证RTL8822BS可不用流控  
RTL8822BS的CTS要接地处理。



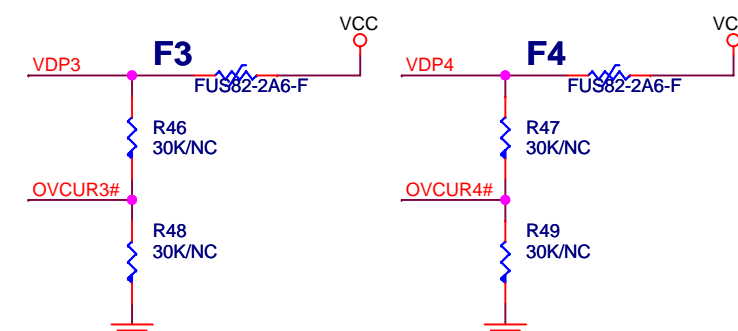
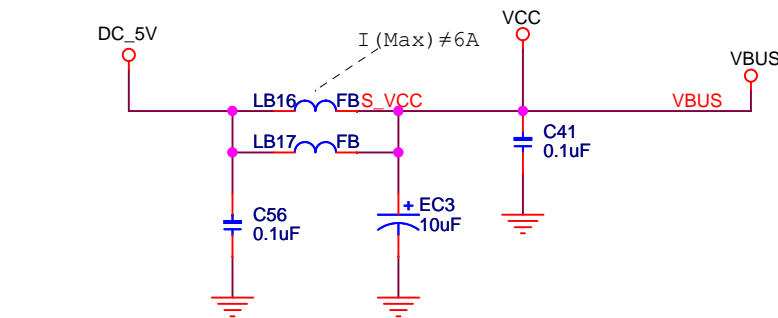




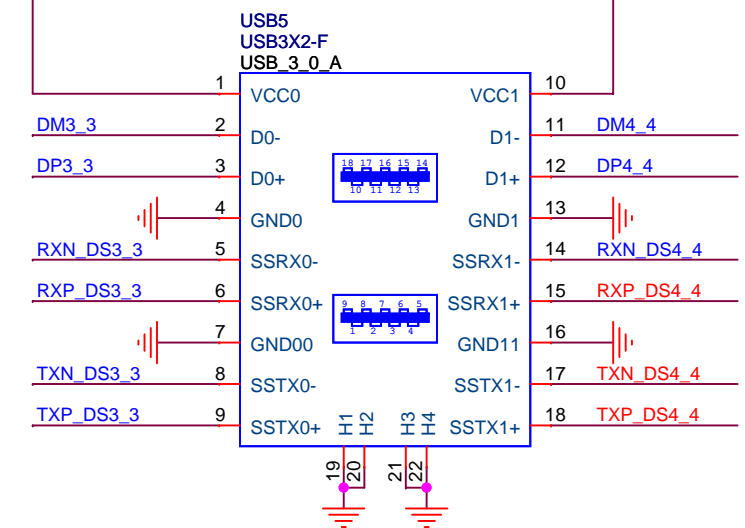
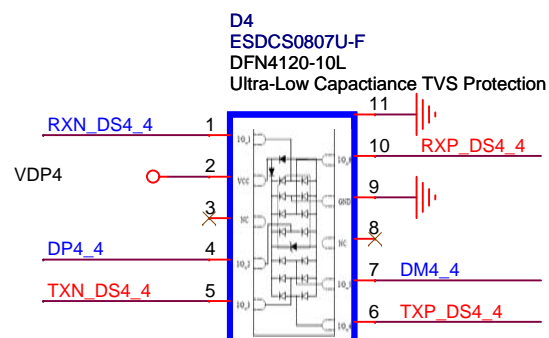
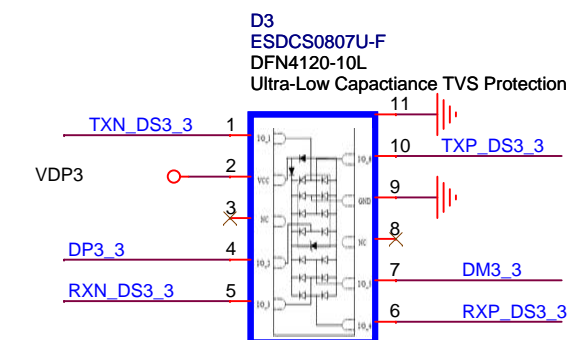
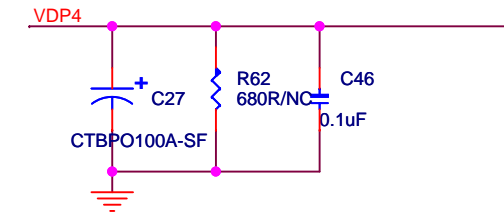
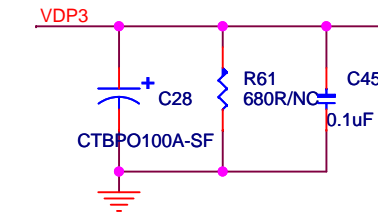
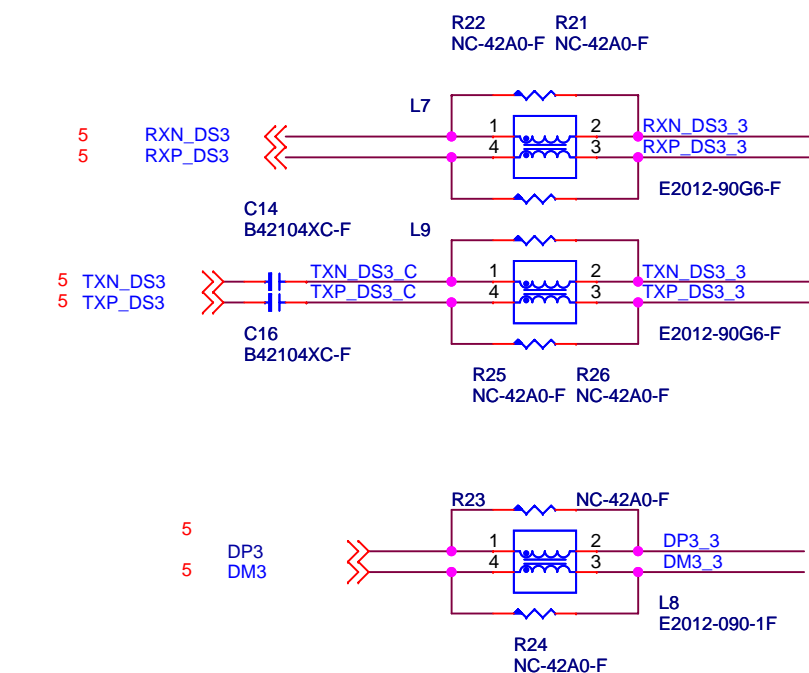
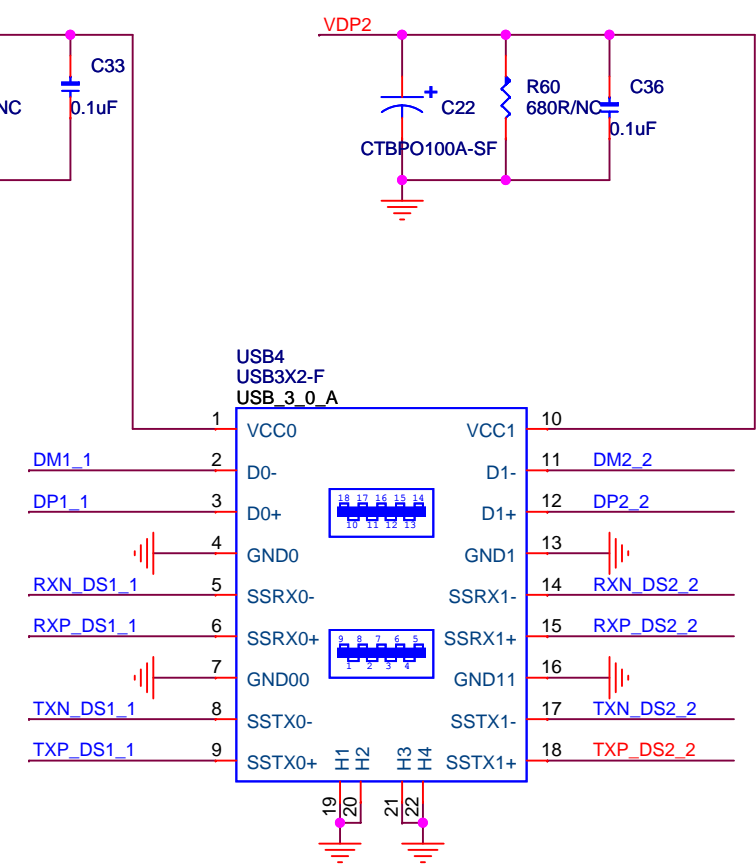
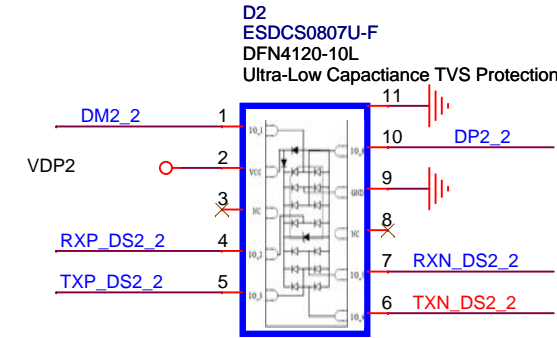
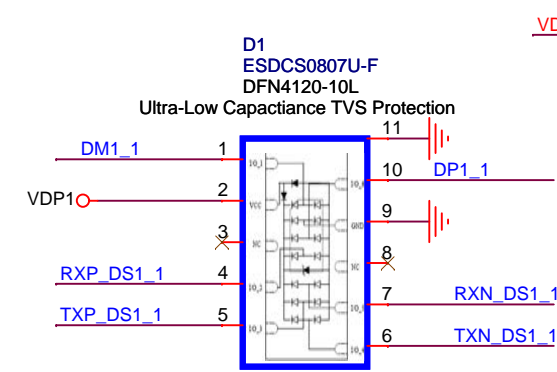
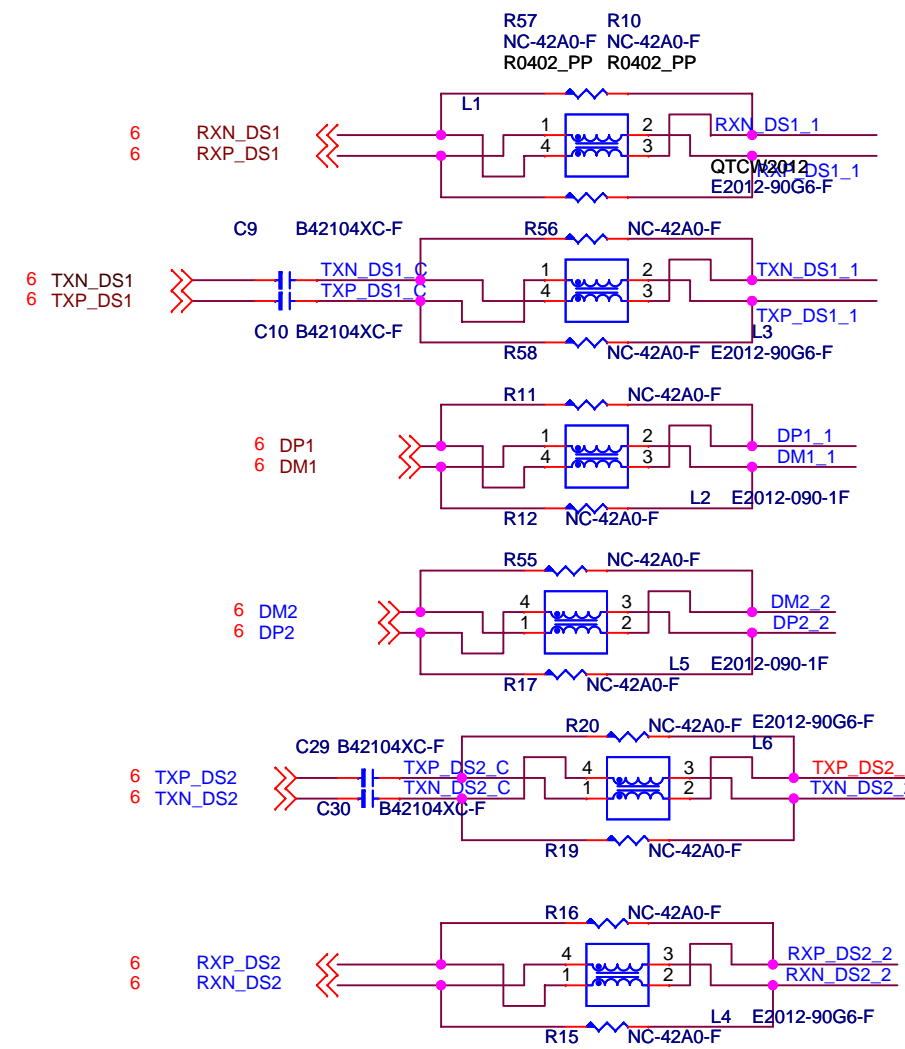
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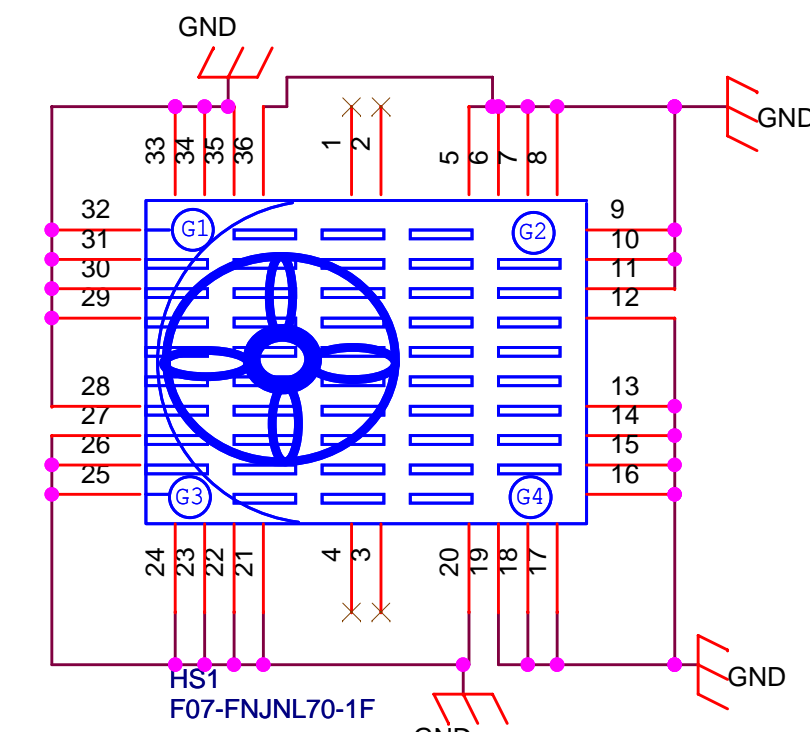
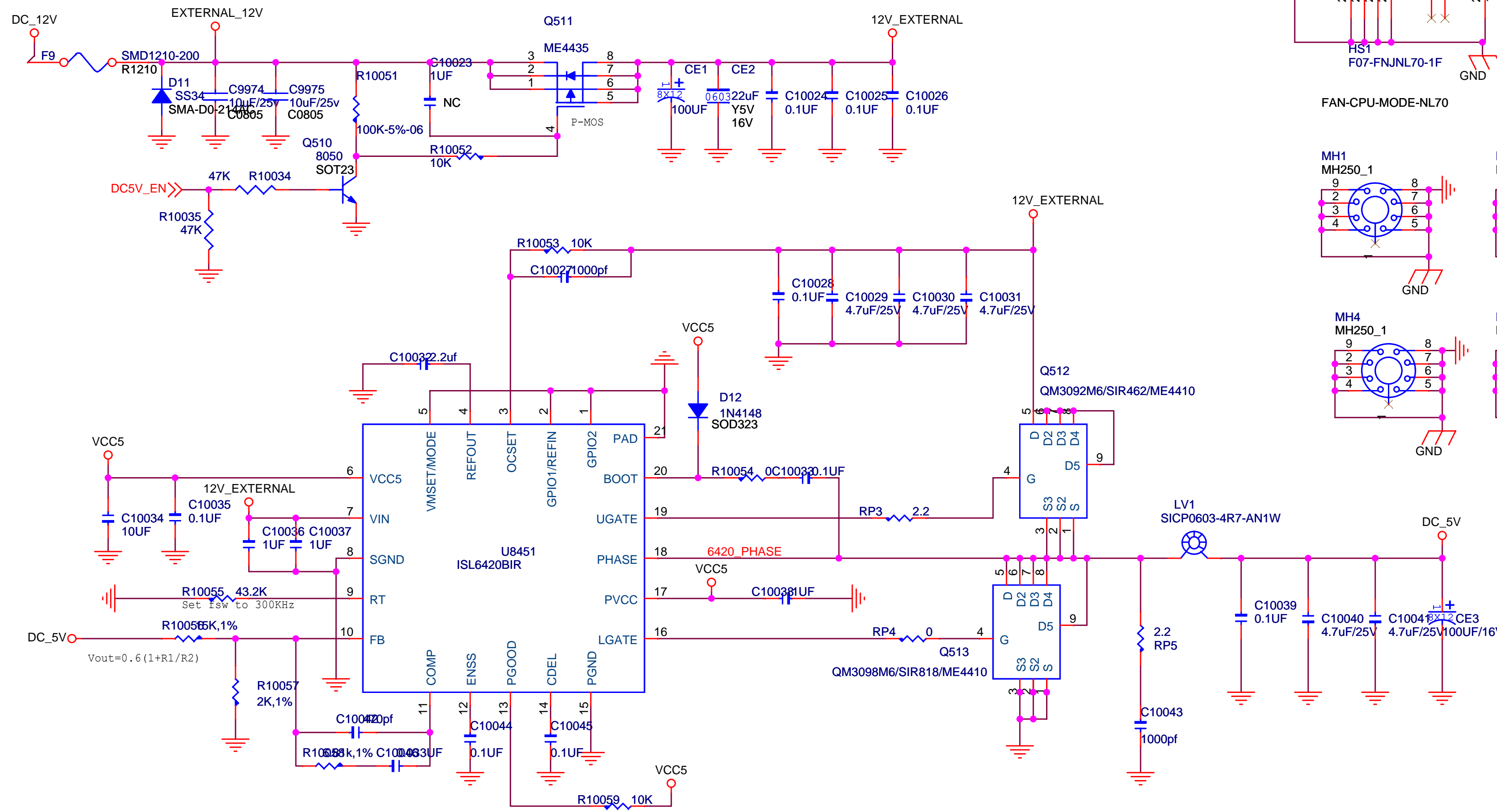
Schematic diagram of the AIC1519N-0 microcontroller. The chip is shown with pins 1 through 8. Pin 1 is CTLA OUTA, Pin 2 is FLGA IN, Pin 3 is FLGB GND, Pin 4 is CTLB OUTB, Pin 5 is FUS8-2A6-F, Pin 6 is FUS8-2A6-F, Pin 7 is VDP1, and Pin 8 is VDP4. The chip is connected to a V33 supply through a network of resistors (R42, R43, R44, R45) and to ground through resistors (R52, R51). The chip is also connected to a VCC supply through a network of capacitors (C57, C63) and resistors (F7, F8).

OVCUR1~4# has to be pulled high by 10K

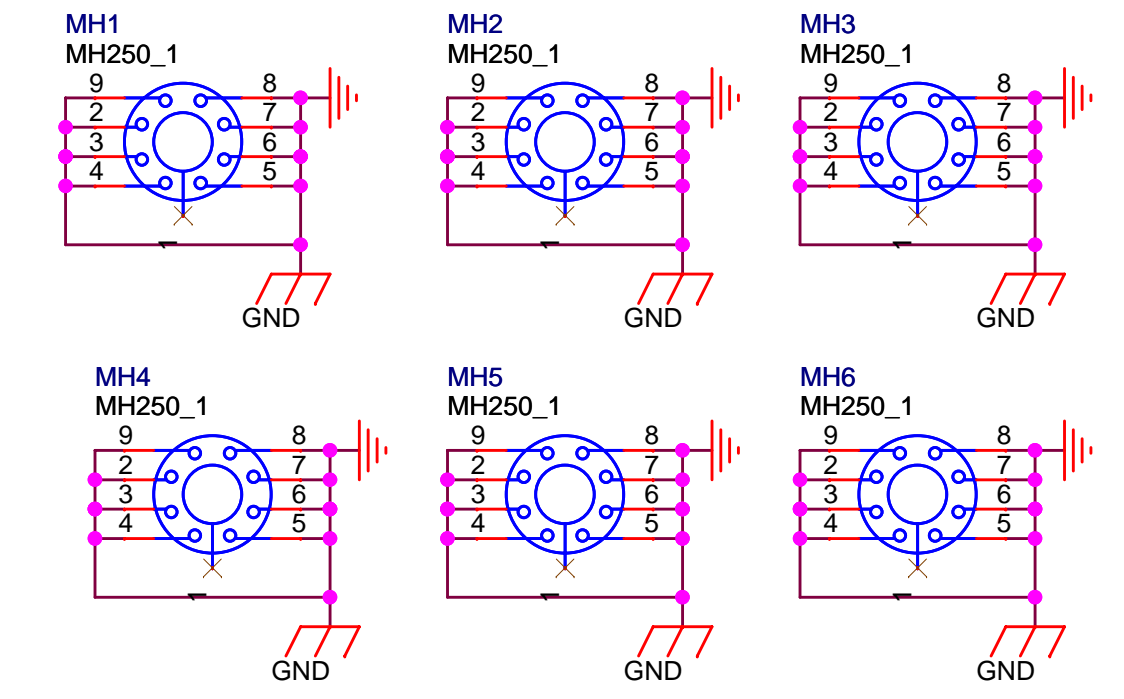



OVCUR1~4# has to be pulled high by 10K





FAN-CPU-MODE-NL70



	<b>JETWAY INFORMATION CO.,LTD.</b>		
	Title <b>POWER-HV</b>		
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