



正基科技股份有限公司

## **SPECIFICATION**

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PRODUCT NAME : AP62X2

|      | APPROVED | CHECKED | PREPARED | DCC ISSUE |
|------|----------|---------|----------|-----------|
| NAME |          |         |          |           |

# AMPAK

## AP62X2

2x2 WiFi+Bluetooth 4.0(HS)+FM Rx  
Module Spec Sheet

# Revision History

| Date       | Revision Content                   | Revised By | Version |
|------------|------------------------------------|------------|---------|
| 2012/12/25 | -Preliminary                       | Bart       | 1.0     |
| 2013/03/28 | -Modify WiFi RF Specification      | Bart       | 1.1     |
| 2013/05/06 | -Modify BT Frequency Band          | Brian      | 1.2     |
| 2013/07/08 | -Modify External Clock Description | Brian      | 1.3     |
| 2014/04/25 | -Modify Operating Temperature      | Brian      | 1.4     |
| 2014/05/26 | - Add Solder Paste definition      | Brian      | 1.5     |
|            |                                    |            |         |

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## 1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi, Bluetooth and FM functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets, FM radio functional applications and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11a/b/g/n 2x2 Access Points in the wireless LAN.

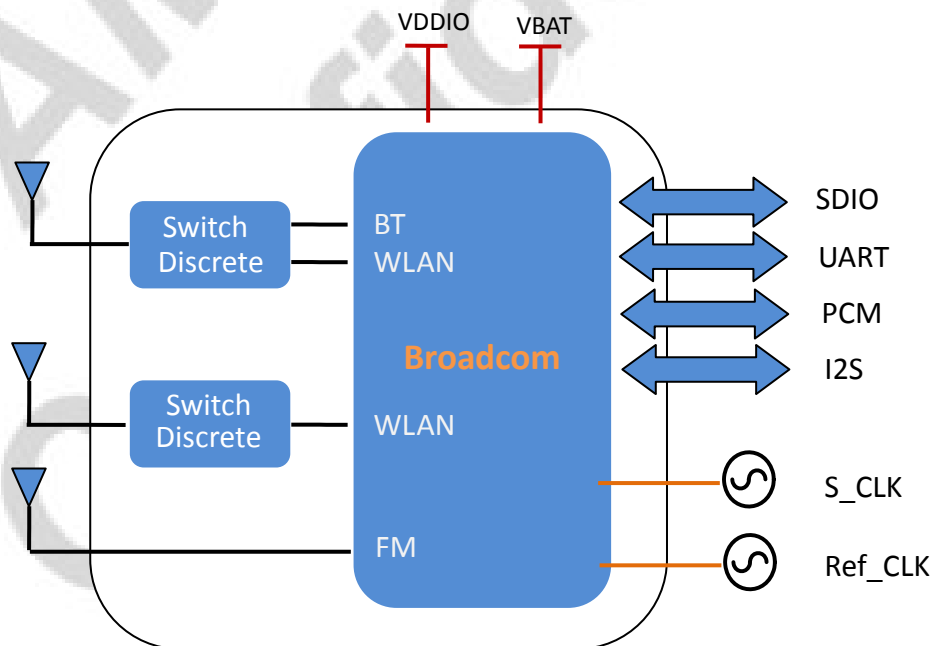
The wireless module complies with IEEE 802.11 a/b/g/n 2x2 standard and it can achieve up to a speed of 300Mbps with dual stream in 802.11n to connect the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / PCM / I2S interface for Bluetooth / FM.

This compact module is a total solution for a combination of WiFi + BT + FM technologies. The module is specifically developed for Smart phones and Portable devices.

## 2. Features

- 802.11a/b/g/n and 2x2 802.11n MAC/baseband/radio — virtual-simultaneous dual-band operation
- Dual-stream IEEE 802.11n support for 20MHz and 40MHz channels provides PHY layer rates up to 300Mbps for typical upper-layer throughput in excess of 200Mbps
- Bluetooth V4.0(HS) with integrated Class 1 PA and Low Energy (BLE) support
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- WLAN host interface options:
  - SDIO v3.0 — up to 208 MHz (4-bit) clock rate
- BT host digital interface:
  - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



## 3. Deliverables

### 3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

### 3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

## 4. General Specification

### 4.1 General Specification

|                       |  |
|-----------------------|--|
| Model Name            | AP62X2                                       |
| Product Description   | Support WiFi/Bluetooth/FM functionalities    |
| Dimension             | L x W x H: 15 x 13 x 1.5 (typical) mm        |
| WiFi Interface        | Support SDIO3.0/2.0                          |
| BT Interface          | UART / PCM                                   |
| FM Interface          | UART / I2S                                   |
| Operating temperature | -30°C to 65°C                                |
| Storage temperature   | -40°C to 85°C                                |
| Humidity              | Operating Humidity 10% to 95% Non-Condensing |

### 4.2 Voltages

#### 4.2.1 Absolute Maximum Ratings

| Symbol | Description                         | Min. | Max. | Unit |
|--------|-------------------------------------|------|------|------|
| VBAT   | Input supply Voltage                | -0.5 | 5.5  | V    |
| VDDIO  | Digital/Bluetooth/SDIO/ I/O Voltage | -0.5 | 3.8  | V    |

#### 4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

|                       | Min. | Typ. | Max. | Unit  |
|-----------------------|------|------|------|-------|
| Operating Temperature | -30  | 25   | 65   | deg.C |
| VBAT                  | 2.3  | 3.6  | 4.8  | V     |
| VDDIO                 | 1.8  | -    | 3.3  | V     |



## 5. WiFi RF Specification

### 5.1 2.4GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

| Feature  | Description   |
|--|---|
| WLAN Standard                                    | IEEE 802.11b/g/n 2x2, WiFi compliant  |
| Frequency Range                                  | 2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)                                    |
| Number of Channels                               | 2.4GHz : Ch1 ~ Ch14   |
| Modulation                                       | 802.11b : DQPSK, DBPSK, CCK<br>802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK |
| Output Power                                     | 802.11b /11Mbps : 16 dBm $\pm$ 1.5 dB @ EVM $\leq$ -9dB                     |
|  | 802.11g /54Mbps : 15 dBm $\pm$ 1.5 dB @ EVM $\leq$ -25dB                    |
|  | 802.11n /MCS7 : 14 dBm $\pm$ 1.5 dB @ EVM $\leq$ -28dB                      |
| SISO Receive Sensitivity<br>(11n,20MHz) @10% PER | - MCS=0 PER @ -89 dBm, typical  |
|  | - MCS=1 PER @ -87 dBm, typical  |
|  | - MCS=2 PER @ -85 dBm, typical  |
|  | - MCS=3 PER @ -81 dBm, typical  |
|  | - MCS=4 PER @ -78 dBm, typical  |
|  | - MCS=5 PER @ -74 dBm, typical  |
|  | - MCS=6 PER @ -72 dBm, typical  |
|  | - MCS=7 PER @ -71 dBm, typical  |
| MIMO Receive Sensitivity<br>(11n,20MHz) @10% PER | - MCS=0 PER @ -91 dBm, typical  |
|  | - MCS=1 PER @ -90 dBm, typical  |
|  | - MCS=2 PER @ -88 dBm, typical  |
|  | - MCS=3 PER @ -84 dBm, typical  |
|  | - MCS=4 PER @ -81 dBm, typical  |
|  | - MCS=5 PER @ -77 dBm, typical  |
|  | - MCS=6 PER @ -75 dBm, typical  |
|  | - MCS=7 PER @ -74 dBm, typical  |
|  | - MCS=8 PER @ -87 dBm, typical  |
| SISO Receive Sensitivity<br>(11g,20MHz) @10% PER | - MCS=15 PER @ -67 dBm, typical   |
|  | - 6Mbps PER @ -91 dBm, typical  |
|  | - 9Mbps PER @ -90 dBm, typical  |
|  | - 12Mbps PER @ -88 dBm, typical   |
|  | - 18Mbps PER @ -86 dBm, typical   |
|  | - 24Mbps PER @ -82 dBm, typical   |

|  |  |
|--|--|
|  | - 36Mbps PER @ -80 dBm, typical                                      |
|  | - 48Mbps PER @ -74 dBm, typical                                      |
|  | - 54Mbps PER @ -73 dBm, typical                                      |
| MIMO Receive Sensitivity<br>(11g,20MHz) @10% PER | - 6Mbps PER @ -92 dBm, typical                                       |
|  | - 9Mbps PER @ -91 dBm, typical                                       |
|  | - 12Mbps PER @ -90 dBm, typical                                      |
|  | - 18Mbps PER @ -89 dBm, typical                                      |
|  | - 24Mbps PER @ -85 dBm, typical                                      |
|  | - 36Mbps PER @ -83 dBm, typical                                      |
|  | - 48Mbps PER @ -77 dBm, typical                                      |
|  | - 54Mbps PER @ -76 dBm, typical                                      |
| SISO Receive Sensitivity<br>(11b,20MHz) @8% PER  | - 1Mbps PER @ -96 dBm, typical                                       |
|  | - 2Mbps PER @ -93 dBm, typical                                       |
|  | - 5.5Mbps PER @ -91 dBm, typical                                     |
|  | - 11Mbps PER @ -87 dBm, typical                                      |
| Data Rate  | 802.11b : 1, 2, 5.5, 11Mbps  |
|  | 802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps                           |
|  | 802.11n: MCS0, MCS1, MCS2, MCS3, MCS4, MCS5, MCS6, MCS7, MCS8, MCS15 |
| Maximum Input Level                              | 802.11b : -10 dBm  |
|  | 802.11g/n : -20 dBm  |
| Antenna Reference                                | Small antennas with 0~2 dBi peak gain                                |

## 5.2 5GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

| Feature  | Description  |
|--|--|
| WLAN Standard                                    | IEEE 802.11a/n 2x2, WiFi compliant   |
| Frequency Range                                  | 4.900 GHz ~ 5.845 GHz (5.0 GHz ISM Band)   |
| Number of Channels                               | 5.0GHz : Please see the table <sup>1</sup>   |
| Modulation                                       | 802.11a : OFDM /64-QAM, 16-QAM, QPSK, BPSK<br>802.11n : OFDM /64-QAM, 16-QAM, QPSK, BPSK |
| Output Power                                     | 802.11a /54Mbps : 13 dBm ± 1.5 dB @ EVM ≤ -25dB  |
|  | 802.11n /MCS7 : 12 dBm ± 1.5 dB @ EVM ≤ -28dB  |
| SISO Receive Sensitivity<br>(11a,20MHz) @10% PER | - 6Mbps PER @ -89 dBm, typical   |
|  | - 9Mbps PER @ -88 dBm, typical   |
|  | - 12Mbps PER @ -86 dBm, typical  |

|  |          |                        |
|--|----------|------------------------|
|  | - 18Mbps | PER @ -84 dBm, typical |
|  | - 24Mbps | PER @ -80 dBm, typical |
|  | - 36Mbps | PER @ -78 dBm, typical |
|  | - 48Mbps | PER @ -73 dBm, typical |
|  | - 54Mbps | PER @ -72 dBm, typical |
| MIMO Receive Sensitivity<br>(11a,20MHz) @10% PER | - 6Mbps  | PER @ -90 dBm, typical |
|  | - 9Mbps  | PER @ -89 dBm, typical |
|  | - 12Mbps | PER @ -88 dBm, typical |
|  | - 18Mbps | PER @ -87 dBm, typical |
|  | - 24Mbps | PER @ -83 dBm, typical |
|  | - 36Mbps | PER @ -81 dBm, typical |
|  | - 48Mbps | PER @ -76 dBm, typical |
| SISO Receive Sensitivity<br>(11n,20MHz) @10% PER | - 54Mbps | PER @ -75 dBm, typical |
|  | - MCS=0  | PER @ -88 dBm, typical |
|  | - MCS=1  | PER @ -86 dBm, typical |
|  | - MCS=2  | PER @ -83 dBm, typical |
|  | - MCS=3  | PER @ -79 dBm, typical |
|  | - MCS=4  | PER @ -76 dBm, typical |
|  | - MCS=5  | PER @ -72 dBm, typical |
| MIMO Receive Sensitivity<br>(11n,20MHz) @10% PER | - MCS=6  | PER @ -71 dBm, typical |
|  | - MCS=7  | PER @ -69 dBm, typical |
|  | - MCS=0  | PER @ -89 dBm, typical |
|  | - MCS=1  | PER @ -88 dBm, typical |
|  | - MCS=2  | PER @ -86 dBm, typical |
|  | - MCS=3  | PER @ -83 dBm, typical |
|  | - MCS=4  | PER @ -80 dBm, typical |
|  | - MCS=5  | PER @ -75 dBm, typical |
|  | - MCS=6  | PER @ -74 dBm, typical |
|  | - MCS=7  | PER @ -71 dBm, typical |
| SISO Receive Sensitivity<br>(11n,40MHz) @10% PER | - MCS=8  | PER @ -86 dBm, typical |
|  | - MCS=15 | PER @ -64 dBm, typical |
|  | - MCS=0  | PER @ -85 dBm, typical |
|  | - MCS=1  | PER @ -83 dBm, typical |
|  | - MCS=2  | PER @ -80 dBm, typical |
|  | - MCS=3  | PER @ -77 dBm, typical |
|  | - MCS=4  | PER @ -74 dBm, typical |
|  | - MCS=5  | PER @ -69 dBm, typical |

|  |  |
|--|--|
|  | - MCS=6 PER @ -68 dBm, typical                                       |
|  | - MCS=7 PER @ -66 dBm, typical                                       |
| MIMO Receive Sensitivity<br>(11n,40MHz) @10% PER | - MCS=0 PER @ -87 dBm, typical                                       |
|  | - MCS=1 PER @ -85 dBm, typical                                       |
|  | - MCS=2 PER @ -83 dBm, typical                                       |
|  | - MCS=3 PER @ -79 dBm, typical                                       |
|  | - MCS=4 PER @ -76 dBm, typical                                       |
|  | - MCS=5 PER @ -72 dBm, typical                                       |
|  | - MCS=6 PER @ -70 dBm, typical                                       |
|  | - MCS=7 PER @ -68 dBm, typical                                       |
|  | - MCS=8 PER @ -84 dBm, typical                                       |
|  | - MCS=15 PER @ -64 dBm, typical                                      |
| Data Rate  | 802.11a : 6, 9, 12, 18, 24, 36, 48, 54Mbps                           |
|  | 802.11n: MCS0, MCS1, MCS2, MCS3, MCS4, MCS5, MCS6, MCS7, MCS8, MCS15 |
| Maximum Input Level                              | 802.11a/n : -30 dBm  |
| Antenna Reference                                | Small antennas with 0~2 dBi peak gain                                |

<sup>1</sup>5GHz(20MHz) Channel table

| Band (GHz)        | Operating Channel Numbers | Channel center frequencies(MHz) |
|-------------------|---------------------------|---------------------------------|
| 5.15GHz~5.25GHz   | 36                        | 5180                            |
|                   | 40                        | 5200                            |
|                   | 44                        | 5220                            |
|                   | 48                        | 5240                            |
| 5.25GHz~5.35GHz   | 52                        | 5260                            |
|                   | 56                        | 5280                            |
|                   | 60                        | 5300                            |
|                   | 64                        | 5320                            |
| 5.5GHz~5.7GHz     | 100                       | 5500                            |
|                   | 104                       | 5520                            |
|                   | 108                       | 5540                            |
|                   | 112                       | 5560                            |
|                   | 116                       | 5580                            |
|                   | 120                       | 5600                            |
|                   | 124                       | 5620                            |
|                   | 128                       | 5640                            |
|                   | 132                       | 5660                            |
|                   | 136                       | 5680                            |
| 5.725GHz~5.825GHz | 140                       | 5700                            |
|                   | 149                       | 5745                            |
|                   | 153                       | 5765                            |
|                   | 157                       | 5785                            |
|                   | 161                       | 5805                            |

## 6. Bluetooth Specification

### 6.1 Bluetooth Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

| Feature   | Description                           |          |      |
|---|---------------------------------------|----------|------|
| <b>General Specification</b>                          |                                       |          |      |
| Bluetooth Standard                                    | Bluetooth V4.0 of 1, 2 and 3 Mbps.    |          |      |
| Host Interface  | UART                                  |          |      |
| Antenna Reference                                     | Small antennas with 0~2 dBi peak gain |          |      |
| Frequency Band  | 2402 MHz ~ 2480 MHz                   |          |      |
| Number of Channels                                    | 79 channels                           |          |      |
| Modulation  | FHSS, GFSK, DPSK, DQPSK               |          |      |
| <b>RF Specification</b>                               |                                       |          |      |
|   | Min.                                  | Typical. | Max. |
| Output Power (Class 1.5)                              |                                       | 10 dBm   |      |
| Output Power (Class 2)                                |                                       | 2 dBm    |      |
| Sensitivity @ BER=0.1%<br>for GFSK (1Mbps)            |                                       | -86 dBm  |      |
| Sensitivity @ BER=0.01%<br>for $\pi/4$ -DQPSK (2Mbps) |                                       | -86 dBm  |      |
| Sensitivity @ BER=0.01%<br>for 8DPSK (3Mbps)          |                                       | -80 dBm  |      |
| Maximum Input Level                                   | GFSK (1Mbps):-20dBm                   |          |      |
|   | $\pi/4$ -DQPSK (2Mbps) :-20dBm        |          |      |
|   | 8DPSK (3Mbps) :-20dBm                 |          |      |

## 7. FM Specification

### 7.1 FM Specification (TBD)

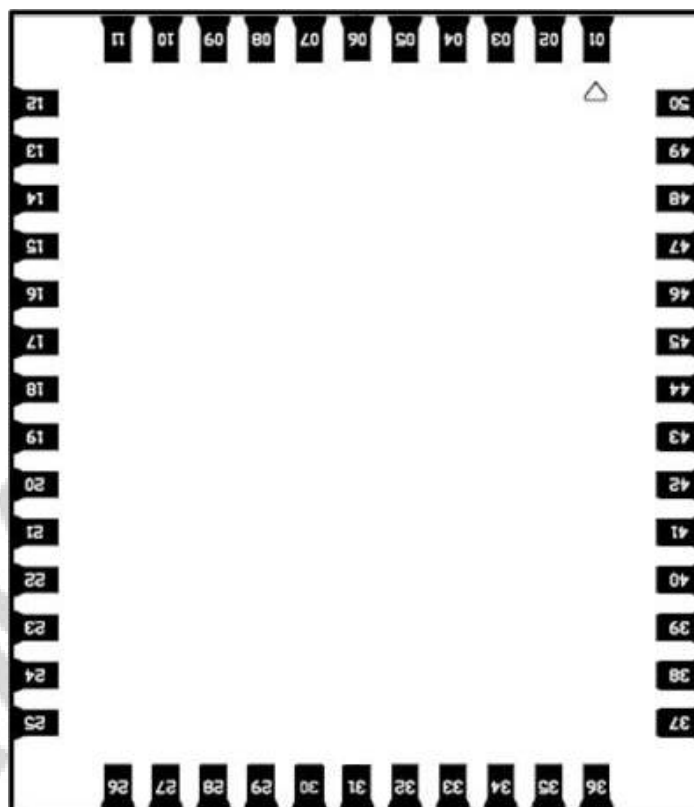
Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

| Feature                                      | Description  |           |     |     |     |      |
|--|--|-----------|-----|-----|-----|------|
| General Specification                        |  |           |     |     |     |      |
| Frequency Band                               | 76MHz-108MHz   |           |     |     |     |      |
| Host Interface                               | HCI UART, PCM  |           |     |     |     |      |
| Channel step                                 | 50 KHz   |           |     |     |     |      |
| Analog Audio output load                     | $R_L>30K\Omega$ , $C_L>20pF$                                       |           |     |     |     |      |
| Characteristics                              | Condition  |           | MIN | TYP | MAX | UNIT |
| Receiver<br>(FM Rx Antenna =<br>120nH, Q>30) | RDS Sensitivity  |           |     |     |     | dBm  |
|  | Audio harmonic distortion<br>( $V_{in}=1mV$ , $\Delta f=75KHz$ )   | fmod=1KHz |     |     |     | %    |
|  |  | fmod=3KHz |     |     |     |      |
|  | Maximum SNR<br>(fmod=1KHz, $\Delta f=22.5$ KHz, BW=300Hz to 15KHz) | MONO      |     |     |     | dB   |
|  |  | Stereo    |     |     |     |      |
|  | RF input power level   |           |     |     |     | dBuV |

## 8. Pin Assignments

### 8.1 Pin Outline

< TOP VIEW >



### 8.2 Pin Definition

| NO | Name       | Type | Description                           |
|----|------------|------|---------------------------------------|
| 1  | GND        | —    | Ground connections                    |
| 2  | WL/BT_ANT0 | I/O  | RF I/O port0                          |
| 3  | GND        | —    | Ground connections                    |
| 4  | GND        | —    | Ground connections                    |
| 5  | GND        | —    | Ground connections                    |
| 6  | GND        | —    | Ground connections                    |
| 7  | GND        | —    | Ground connections                    |
| 8  | GND        | —    | Ground connections                    |
| 9  | WL_ANT1    | I/O  | RF I/O port1                          |
| 10 | GND        | —    | Ground connections                    |
| 11 | GND        | —    | Ground connections                    |
| 12 | PA_PU      | O    | External LDO/switcher power-up signal |
| 13 | XTAL_OUT   | O    | External Crystal out                  |



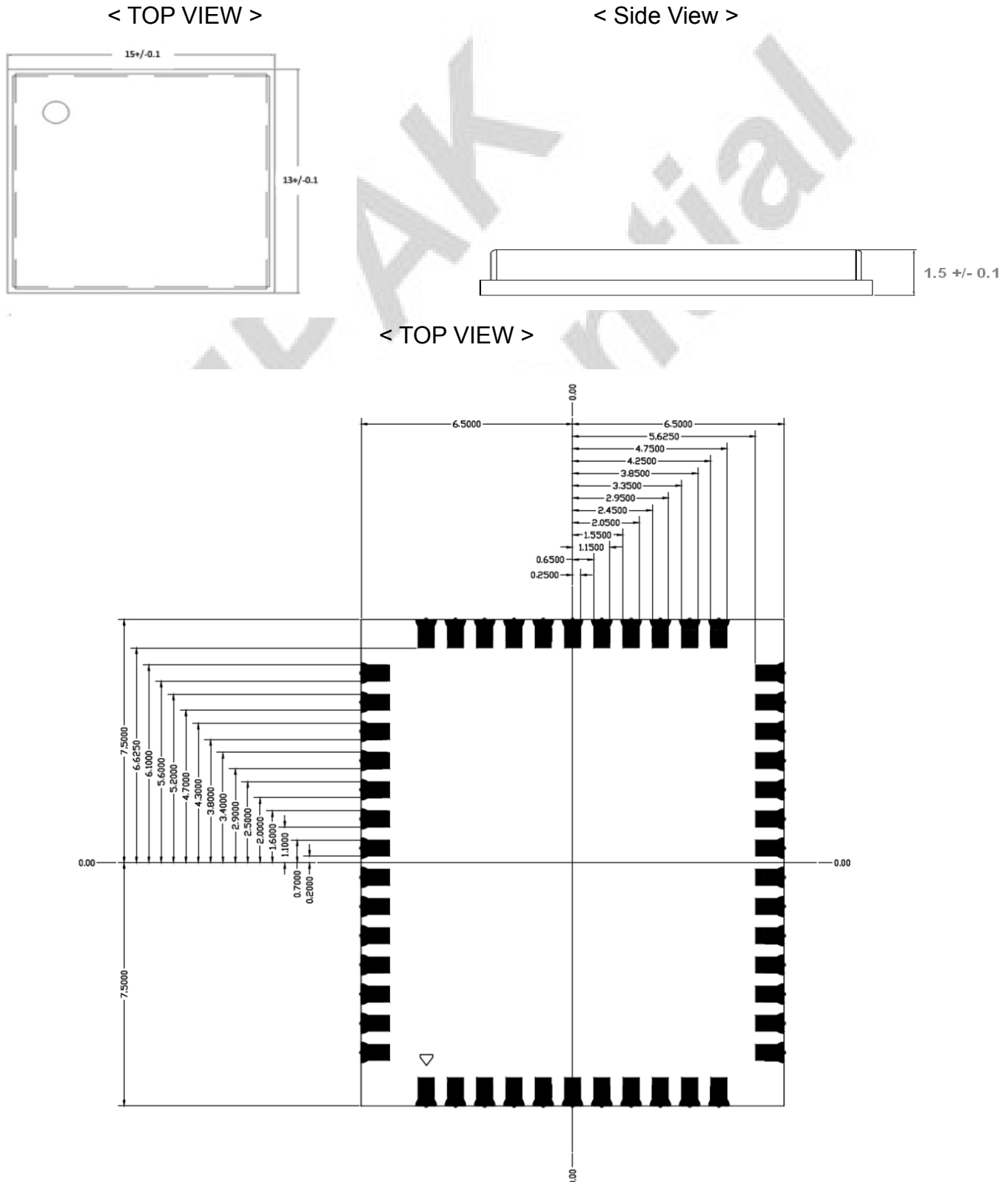
|    |               |     |  |
|----|---------------|-----|--|
| 14 | XTAL_IN       | I   | External Crystal in/ Single clock source in      |
| 15 | WL_REG_ON     | I   | Low asserting reset for WiFi core                |
| 16 | WL_HOST_WAKE  | O   | WLAN to wake-up HOST                             |
| 17 | SDIO_DATA_CMD | I/O | SDIO command line                                |
| 18 | SDIO_DATA_CLK | I/O | SDIO clock line                                  |
| 19 | SDIO_DATA_3   | I/O | SDIO data line 3                                 |
| 20 | SDIO_DATA_2   | I/O | SDIO data line 2                                 |
| 21 | SDIO_DATA_0   | I/O | SDIO data line 0                                 |
| 22 | SDIO_DATA_1   | I/O | SDIO data line 1                                 |
| 23 | GND           | —   | Ground connections                               |
| 24 | NC            | —   | Floating (Don't connected to ground)             |
| 25 | VIN_LDO       | P   | Internal Buck voltage generation pin             |
| 26 | VIN_LDO_OUT   | P   | Internal Buck voltage generation pin             |
| 27 | PCM_SYNC      | I/O | PCM sync signal                                  |
| 28 | PCM_IN        | I   | PCM data input                                   |
| 29 | PCM_OUT       | O   | PCM Data output                                  |
| 30 | PCM_CLK       | I/O | PCM clock  |
| 31 | LPO           | I   | External Low Power Clock input (32.768KHz)       |
| 32 | GND           | —   | Ground connections                               |
| 33 | NC            | —   | Floating (Don't connected to ground)             |
| 34 | VDDIO         | P   | I/O Voltage supply input                         |
| 35 | NC            | —   | Floating (Don't connected to ground)             |
| 36 | VBAT          | P   | Main power voltage source input                  |
| 37 | PA_3P3        | P   | Internal PA 3V3 voltage source input             |
| 38 | BT_REG_ON     | I   | Low asserting reset for Bluetooth/FM core        |
| 39 | GND           | —   | Ground connections                               |
| 40 | UART_TXD      | O   | Bluetooth/FM UART interface                      |
| 41 | UART_RXD      | I   | Bluetooth/FM UART interface                      |
| 42 | UART_RTS_N    | O   | Bluetooth/FM UART interface                      |
| 43 | UART_CTS_N    | I   | Bluetooth/FM UART interface                      |
| 44 | I2S_WS        | I/O | I2S WS: can be master(output) or slave(input)    |
| 45 | I2S_CLK       | I/O | I2S clock: can be master(output) or slave(input) |
| 46 | I2S_DO        | O   | I2S data output                                  |
| 47 | I2S_DI        | I   | I2S data input                                   |
| 48 | FM_RX         | I   | FM radio RF input antenna port                   |
| 49 | BT_WAKE       | I   | HOST wake-up Bluetooth device                    |
| 50 | BT_HOST_WAKE  | O   | Bluetooth device to wake-up HOST                 |



# 9. Dimensions

## 9.1 Physical Dimensions

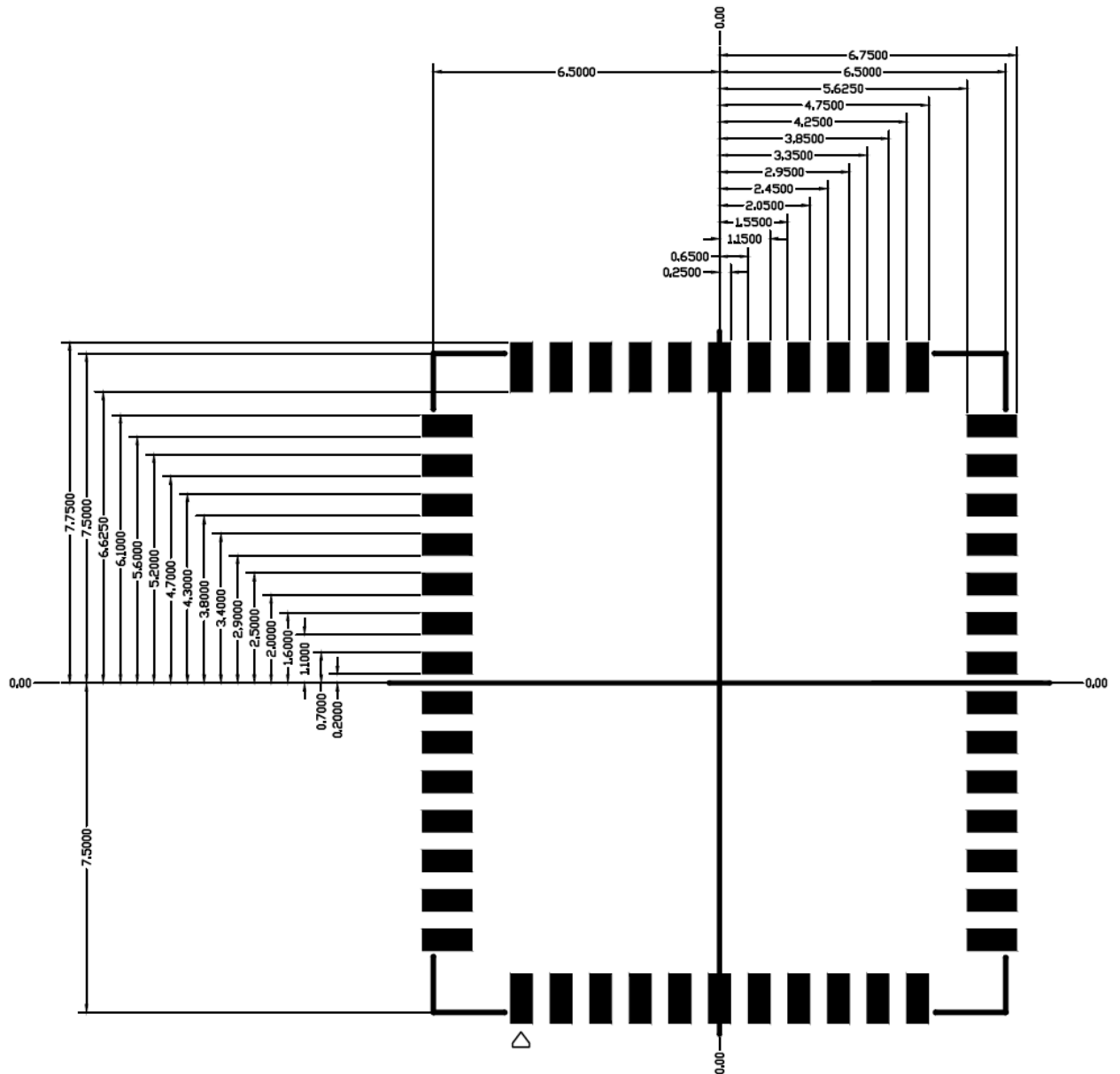
(Unit: mm)



## 9.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >



## 10. External clock reference

External LPO signal characteristics

| Parameter                                    | Specification            | Units          |
|--|--------------------------|----------------|
| Nominal input frequency                      | 32.768                   | kHz            |
| Frequency accuracy                           | $\pm 30$                 | ppm            |
| Duty cycle                                   | 30 - 70                  | %              |
| Input signal amplitude                       | 1600 to 3300             | mV, p-p        |
| Signal type                                  | Square-wave or sine-wave | -              |
| Input impedance                              | $>100k$<br>$<5$          | $\Omega$<br>pF |
| Clock jitter (integrated over 300Hz – 15KHz) | $<1$                     | Hz             |
| Output high voltage                          | $0.7V_{io} - V_{io}$     | V              |

### 10.1 SDIO Pin Description

The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps),SDR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

| SD 4-Bit Mode |                          |
|---------------|--------------------------|
| DATA0         | Data Line 0              |
| DATA1         | Data Line 1 or Interrupt |
| DATA2         | Data Line 2 or Read Wait |
| DATA3         | Data Line 3              |
| CLK           | Clock                    |
| CMD           | Command Line             |

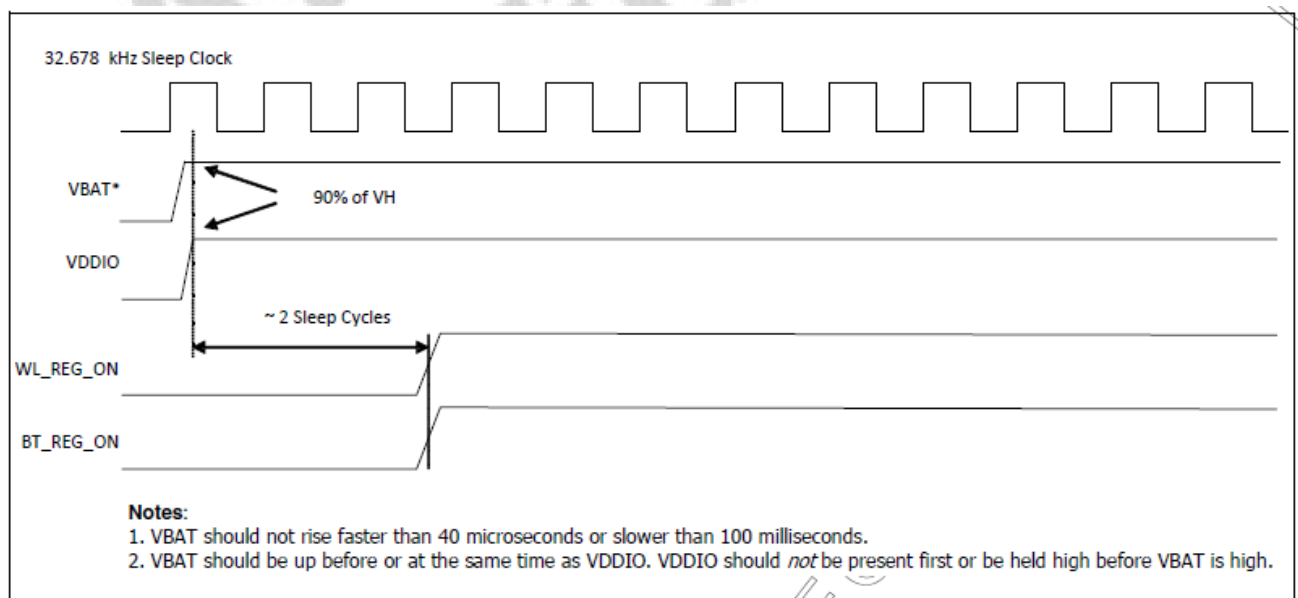
# 11. Host Interface Timing Diagram

## 11.1 Power-up Sequence Timing Diagram

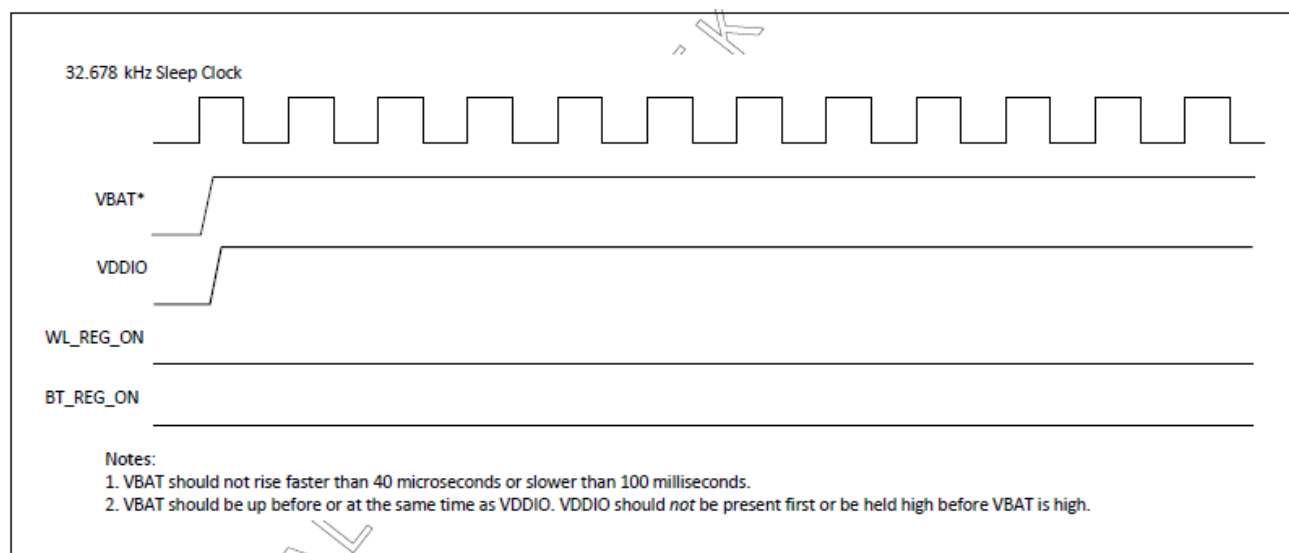
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, FM, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

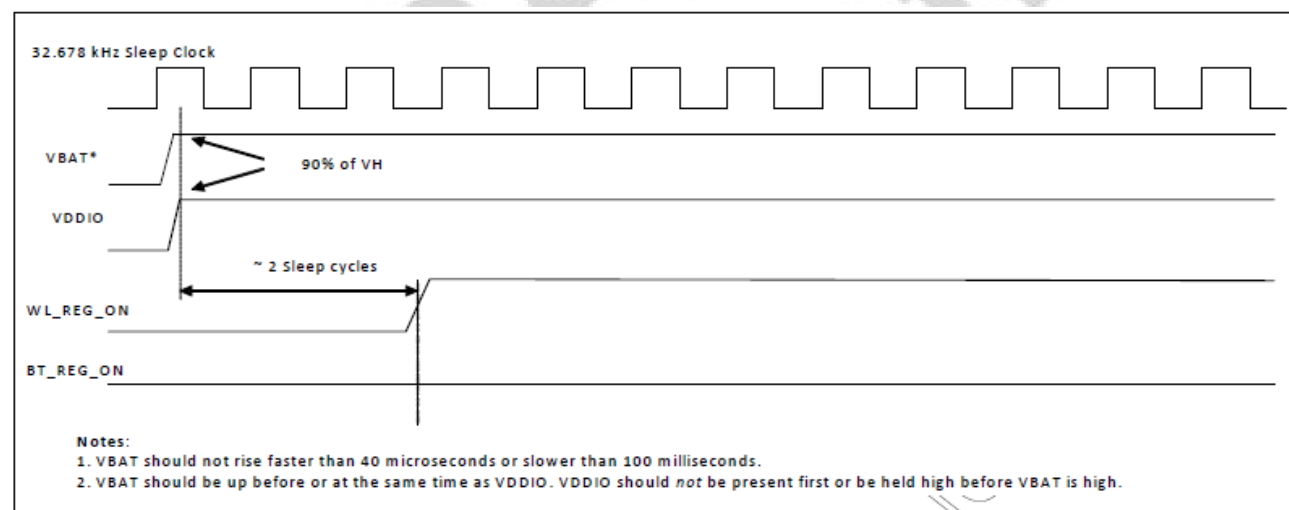
- ※ WL\_REG\_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT\_REG\_ON: Used by the PMU to power up or power down the internal regulators used by the BT/FM section. Low asserting reset for Bluetooth and FM. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



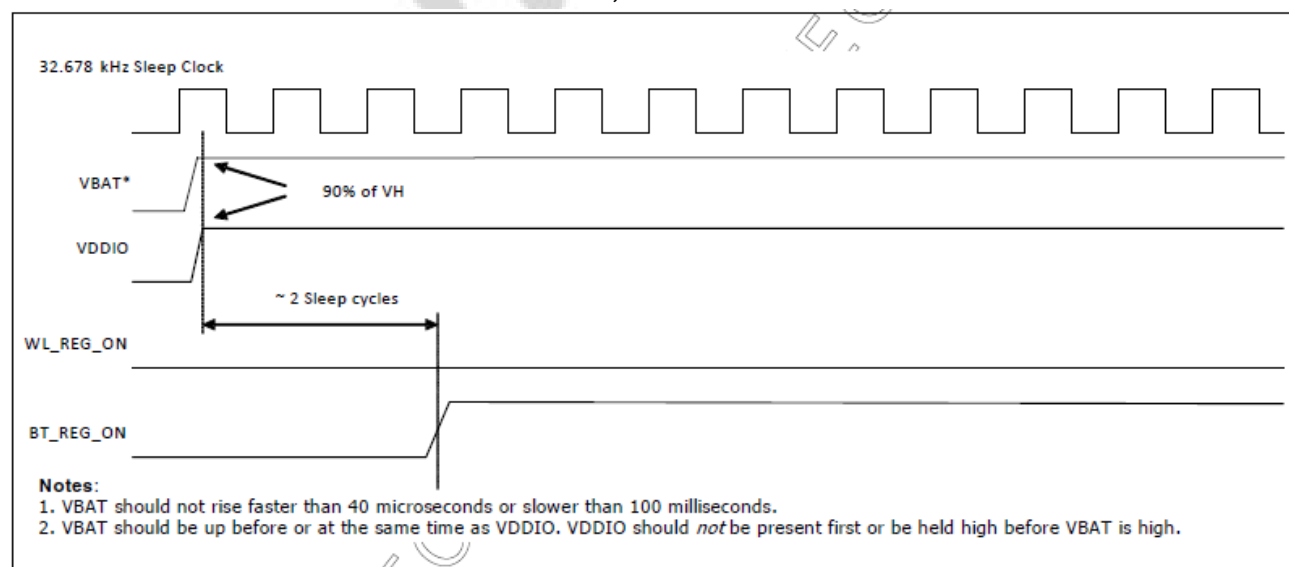
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

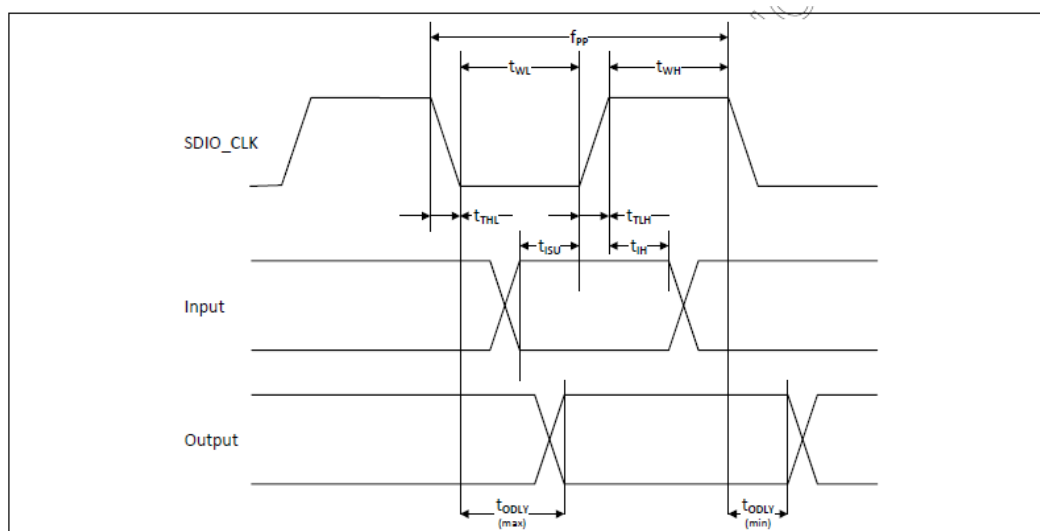


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

## 11.2 SDIO Default Mode Timing Diagram

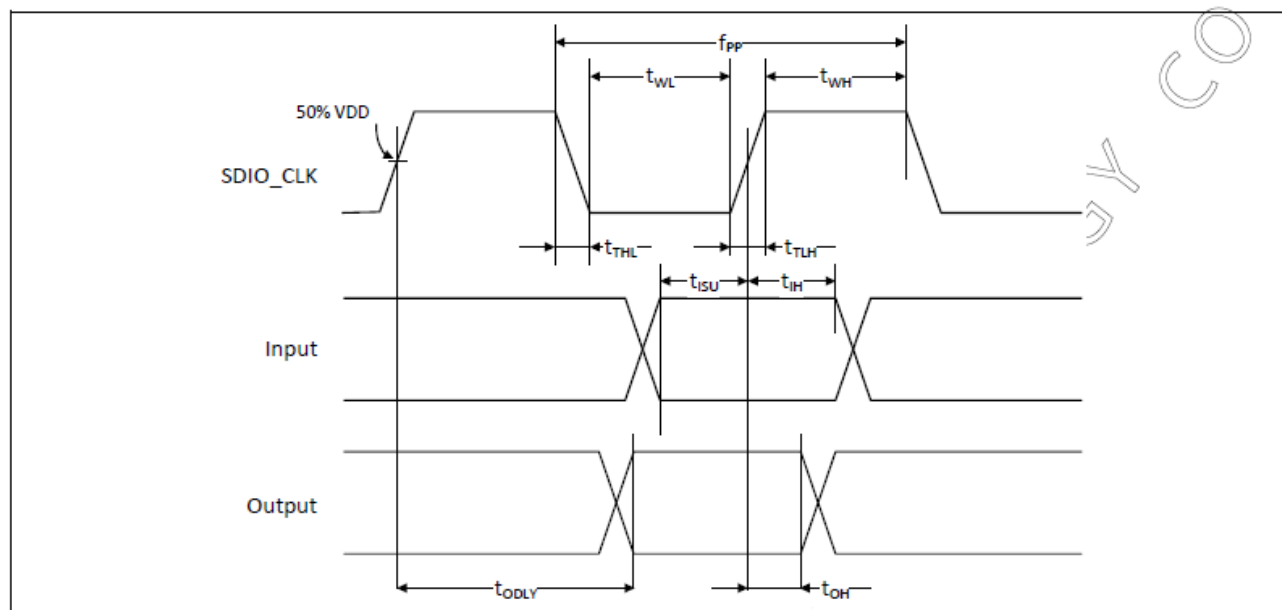


| Parameter  | Symbol            | Minimum | Typical | Maximum | Unit |
|--|-------------------|---------|---------|---------|------|
| <b>SDIO CLK (All values are referred to minimum VIH and maximum VIL<sup>b</sup>)</b> |                   |         |         |         |      |
| Frequency – Data Transfer mode   | f <sub>pp</sub>   | 0       | –       | 25      | MHz  |
| Frequency – Identification mode  | f <sub>OD</sub>   | 0       | –       | 400     | kHz  |
| Clock low time   | t <sub>WL</sub>   | 10      | –       | –       | ns   |
| Clock high time  | t <sub>WH</sub>   | 10      | –       | –       | ns   |
| Clock rise time  | t <sub>TLH</sub>  | –       | –       | 10      | ns   |
| Clock fall time  | t <sub>THL</sub>  | –       | –       | 10      | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>  |                   |         |         |         |      |
| Input setup time   | t <sub>ISU</sub>  | 5       | –       | –       | ns   |
| Input hold time  | t <sub>IH</sub>   | 5       | –       | –       | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>   |                   |         |         |         |      |
| Output delay time – Data Transfer mode   | t <sub>ODLY</sub> | 0       | –       | 14      | ns   |
| Output delay time – Identification mode  | t <sub>ODLY</sub> | 0       | –       | 50      | ns   |

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(V<sub>IH</sub>) = 0.7 × VDDIO and max(V<sub>IL</sub>) = 0.2 × VDDIO.

### 11.3 SDIO High Speed Mode Timing Diagram



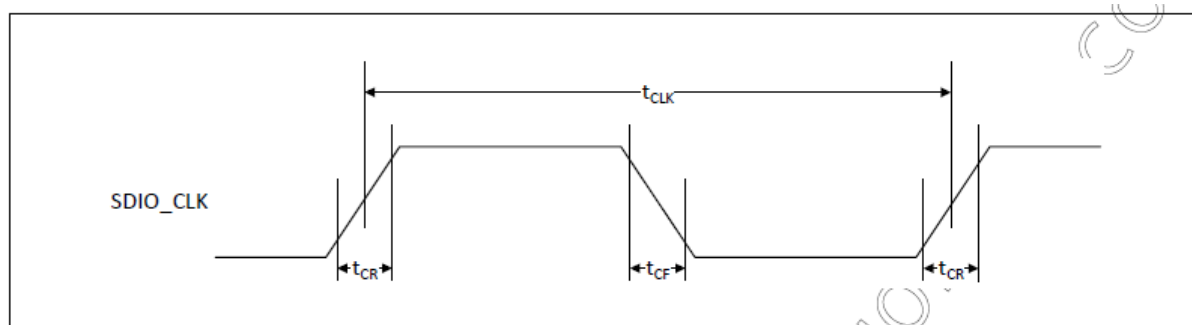
| Parameter  | Symbol     | Minimum | Typical | Maximum | Unit |
|--|------------|---------|---------|---------|------|
| <b>SDIO CLK (all values are referred to minimum <math>V_{IH}</math> and maximum <math>V_{IL}</math><sup>b</sup>)</b> |            |         |         |         |      |
| Frequency – Data Transfer Mode   | $f_{PP}$   | 0       | –       | 50      | MHz  |
| Frequency – Identification Mode  | $f_{OD}$   | 0       | –       | 400     | kHz  |
| Clock low time   | $t_{WL}$   | 7       | –       | –       | ns   |
| Clock high time  | $t_{WH}$   | 7       | –       | –       | ns   |
| Clock rise time  | $t_{TLH}$  | –       | –       | 3       | ns   |
| Clock low time   | $t_{THL}$  | –       | –       | 3       | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>  |            |         |         |         |      |
| Input setup Time   | $t_{ISU}$  | 6       | –       | –       | ns   |
| Input hold Time  | $t_{IH}$   | 2       | –       | –       | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>   |            |         |         |         |      |
| Output delay time – Data Transfer Mode   | $t_{ODLY}$ | –       | –       | 14      | ns   |
| Output hold time   | $t_{OH}$   | 2.5     | –       | –       | ns   |
| Total system capacitance (each line)   | CL         | –       | –       | 40      | pF   |

a. Timing is based on  $CL \leq 40$  pF load on CMD and Data.

b.  $\min(V_{ih}) = 0.7 \times V_{DDIO}$  and  $\max(V_{il}) = 0.2 \times V_{DDIO}$ .

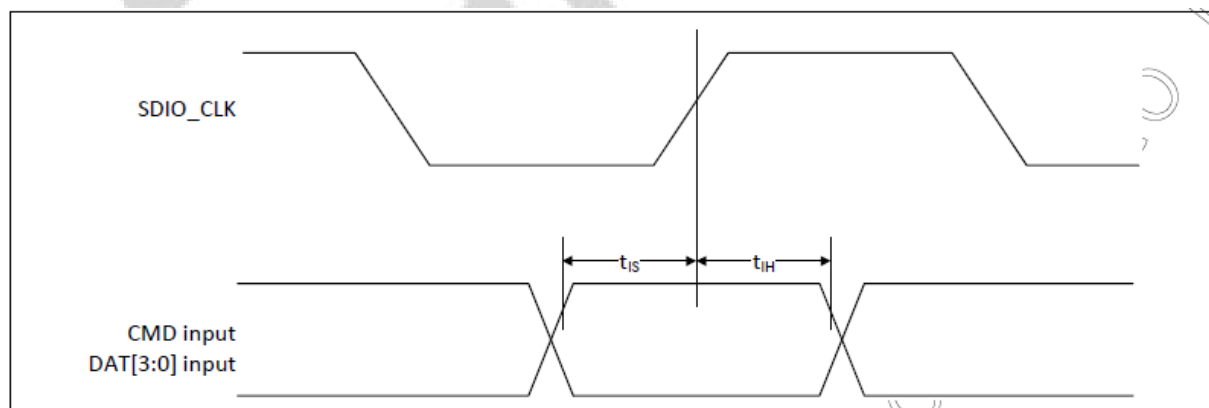
## 11.4 SDIO Bus Timing Specifications in SDR Modes

### Clock timing(SDR Modes)



| Parameter  | Symbol           | Minimum | Maximum              | Unit | Comments   |
|------------|------------------|---------|----------------------|------|--|
| –          | $t_{CLK}$        | 40      | –                    | ns   | SDR12 mode   |
|            |                  | 20      | –                    | ns   | SDR25 mode   |
|            |                  | 10      | –                    | ns   | SDR50 mode   |
|            |                  | 4.8     | –                    | ns   | SDR104 mode  |
| –          | $t_{CR}, t_{CF}$ | –       | $0.2 \times t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz,<br>$C_{CARD} = 10$ pF<br>$t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz,<br>$C_{CARD} = 10$ pF |
| Clock duty | –                | 30      | 70                   | %    | –  |

### Card Input timing (SDR Modes)

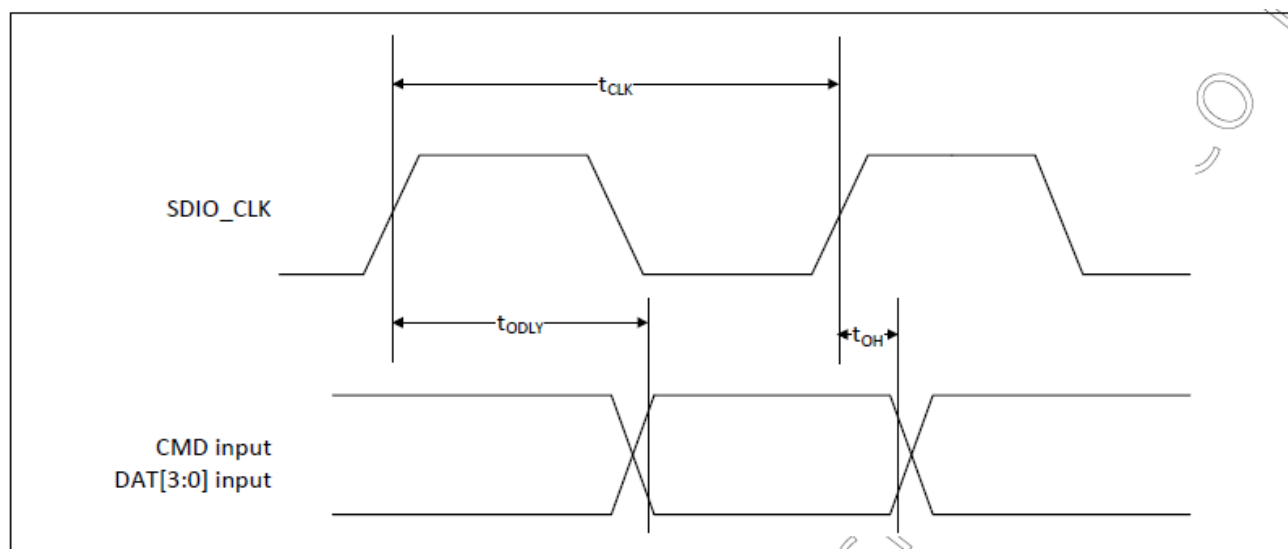


| Symbol             | Minimum           | Maximum | Unit | Comments                         |
|--------------------|-------------------|---------|------|----------------------------------|
| <b>SDR104 Mode</b> |                   |         |      |                                  |
| $t_{IS}$           | 1.70 <sup>a</sup> | –       | ns   | $C_{CARD} = 10$ pF, VCT = 0.975V |
| $t_{IH}$           | 0.80              | –       | ns   | $C_{CARD} = 5$ pF, VCT = 0.975V  |
| <b>SDR50 Mode</b>  |                   |         |      |                                  |
| $t_{IS}$           | 3.00              | –       | ns   | $C_{CARD} = 10$ pF, VCT = 0.975V |
| $t_{IH}$           | 0.80              | –       | ns   | $C_{CARD} = 5$ pF, VCT = 0.975V  |

a. SDIO 3.0 specification value is 1.40 ns.



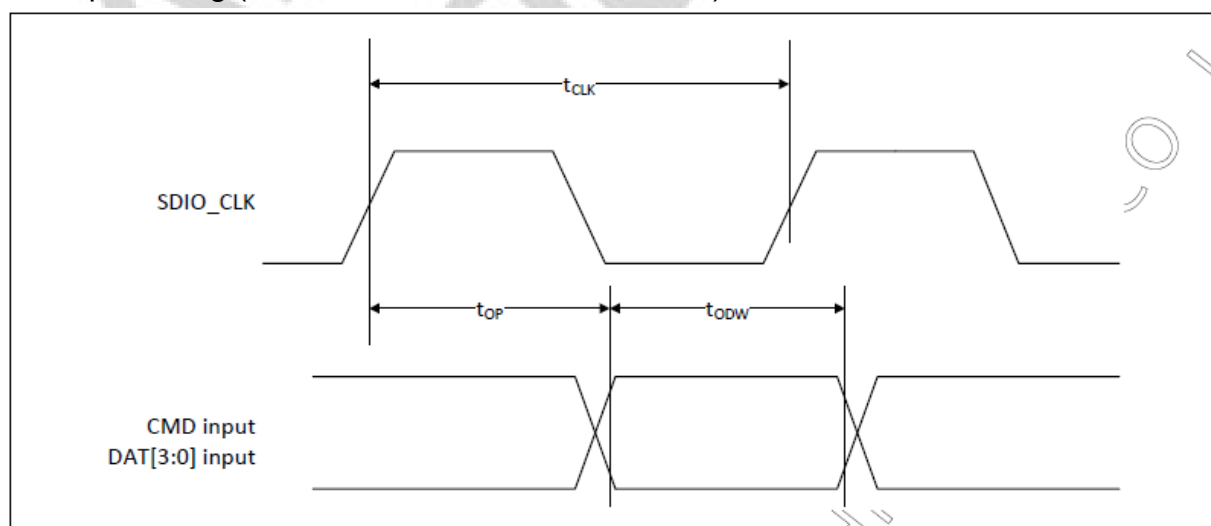
## Card output timing (SDR Modes up to 100MHz)



| Symbol     | Minimum | Maximum           | Unit | Comments   |
|------------|---------|-------------------|------|--|
| $t_{ODLY}$ | –       | 7.85 <sup>a</sup> | ns   | $t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50 |
| $t_{ODLY}$ | –       | 14.0              | ns   | $t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25        |
| $t_{OH}$   | 1.5     | –                 | ns   | Hold time at the $t_{ODLY}$ (min) $C_L = 15$ pF                  |

a. SDIO 3.0 specification value is 7.5 ns.

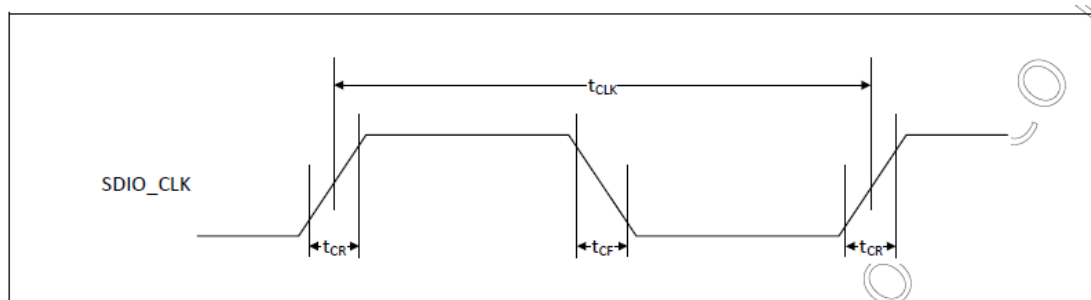
## Card output timing (SDR Modes 100MHz to 208MHz)



| Symbol          | Minimum | Maximum | Unit | Comments  |
|-----------------|---------|---------|------|---|
| $t_{OP}$        | 0       | 2       | UI   | Card output phase                               |
| $\Delta t_{OP}$ | –350    | +1550   | ps   | Delay variation due to temp change after tuning |
| $t_{ODW}$       | 0.60    | –       | UI   | $t_{ODW} = 2.88$ ns @ 208 MHz                   |

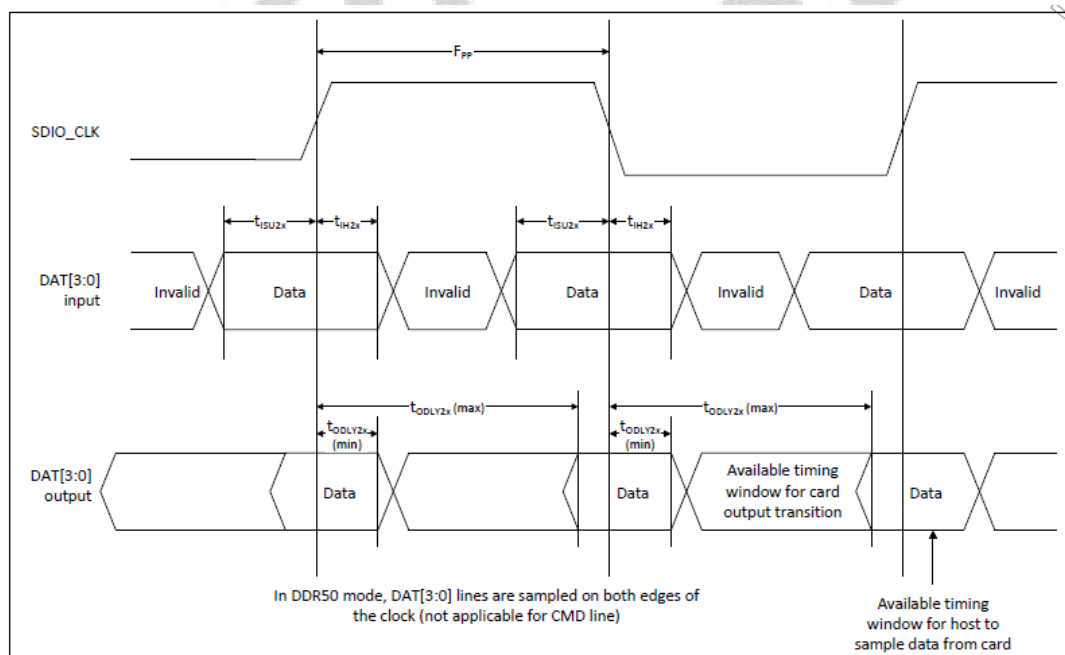
- $\Delta t_{OP} = +1550$  ps for junction temperature of  $\Delta t_{OP} = 90$  degrees during operation
- $\Delta t_{OP} = -350$  ps for junction temperature of  $\Delta t_{OP} = -20$  degrees during operation
- $\Delta t_{OP} = +2600$  ps for junction temperature of  $\Delta t_{OP} = -20$  to  $+125$  degrees during operation

## 11.5 SDIO Bus Timing Specifications in DDR50 Mode



| Parameter  | Symbol           | Minimum | Maximum              | Unit | Comments  |
|------------|------------------|---------|----------------------|------|---|
| –          | $t_{CLK}$        | 20      | –                    | ns   | DDR50 mode  |
| –          | $t_{CR}, t_{CF}$ | –       | $0.2 \times t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz,<br>$C_{CARD} = 10$ pF |
| Clock duty | –                | 45      | 55                   | %    | –   |

### Data Timing



| Parameter         | Symbol       | Minimum | Maximum           | Unit | Comments                    |
|-------------------|--------------|---------|-------------------|------|-----------------------------|
| <b>Input CMD</b>  |              |         |                   |      |                             |
| Input setup time  | $t_{ISU}$    | 6       | –                 | ns   | $C_{CARD} < 10$ pF (1 Card) |
| Input hold time   | $t_{IH}$     | 0.8     | –                 | ns   | $C_{CARD} < 10$ pF (1 Card) |
| <b>Output CMD</b> |              |         |                   |      |                             |
| Output delay time | $t_{ODLY}$   | –       | 13.7              | ns   | $C_{CARD} < 30$ pF (1 Card) |
| Output hold time  | $t_{OH}$     | 1.5     | –                 | ns   | $C_{CARD} < 15$ pF (1 Card) |
| <b>Input DAT</b>  |              |         |                   |      |                             |
| Input setup time  | $t_{ISU2x}$  | 3       | –                 | ns   | $C_{CARD} < 10$ pF (1 Card) |
| Input hold time   | $t_{IH2x}$   | 0.8     | –                 | ns   | $C_{CARD} < 10$ pF (1 Card) |
| <b>Output DAT</b> |              |         |                   |      |                             |
| Output delay time | $t_{ODLY2x}$ | –       | 7.85 <sup>a</sup> | ns   | $C_{CARD} < 25$ pF (1 Card) |
| Output hold time  | $t_{ODLY2x}$ | 1.5     | –                 | ns   | $C_{CARD} < 15$ pF (1 Card) |

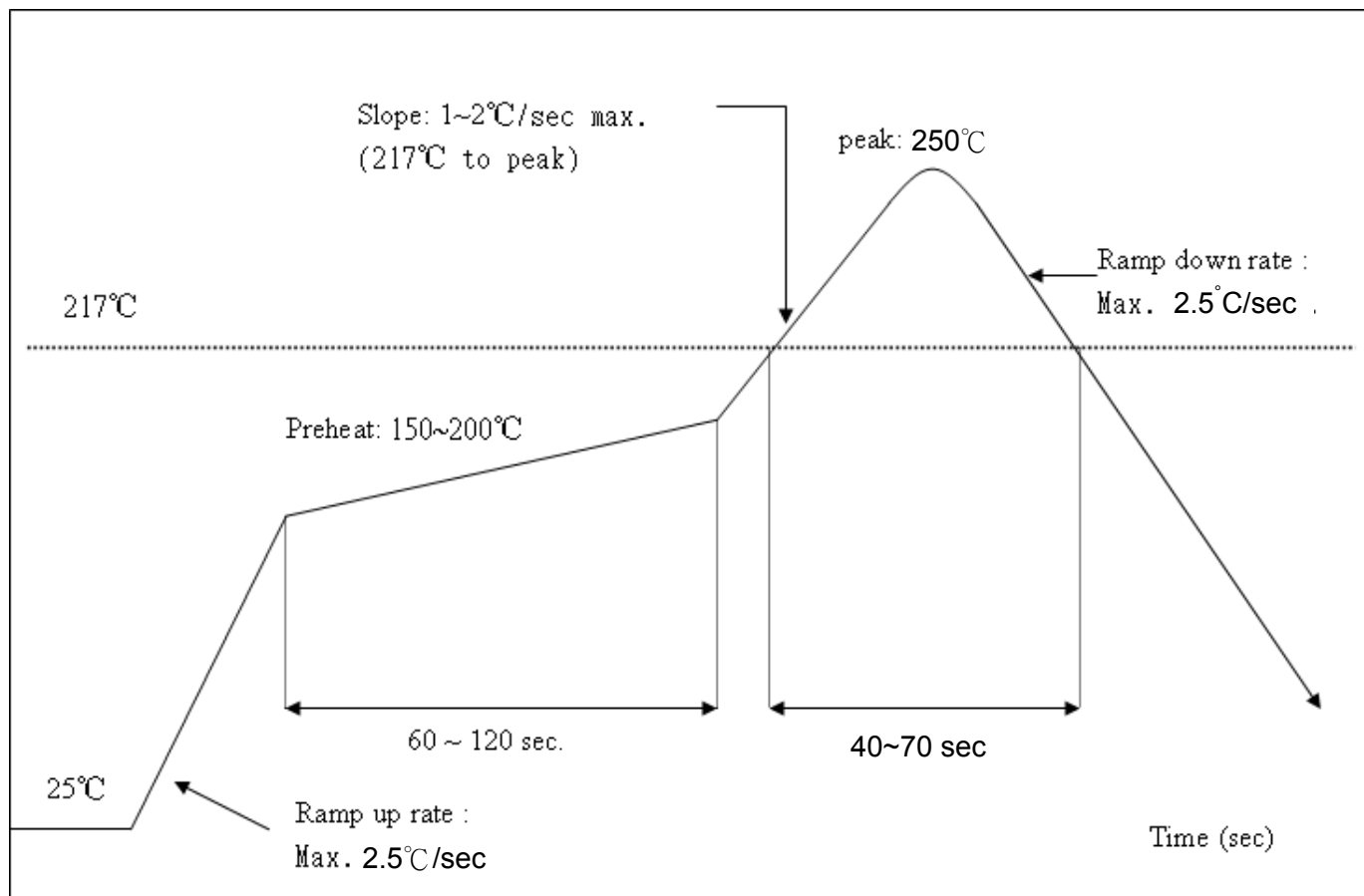
<sup>a</sup> SDIO 3.0 specification value is 7.0 ns.

## 12. Recommended Reflow Profile

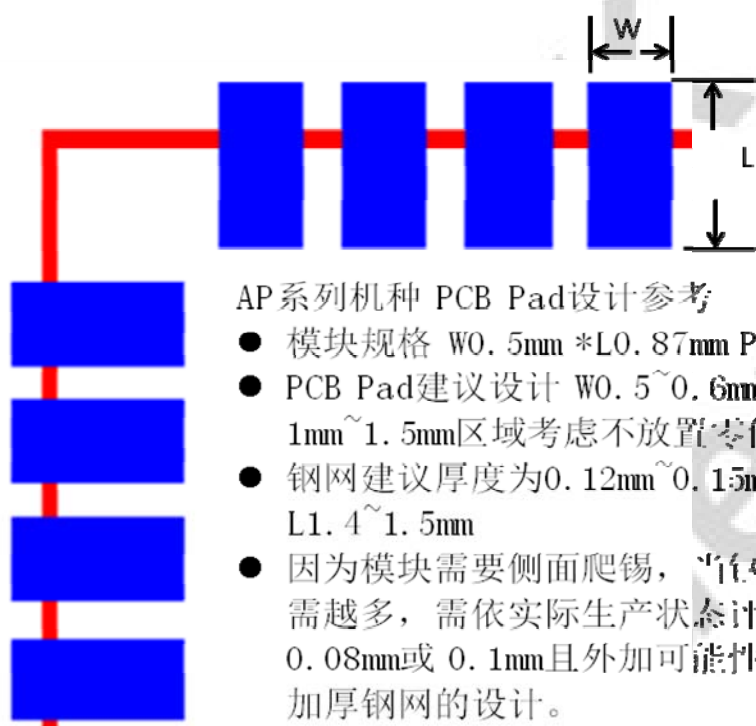
Referred to IPC/JEDEC standard.

Peak Temperature :  $<250^{\circ}\text{C}$

Number of Times :  $\leq 2$  times



# Solder Paste definition



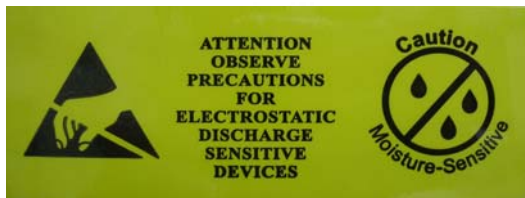
## AP系列机种 PCB Pad设计参考

- 模块规格 W0.5mm \* L0.87mm Pitch 0.9mm
- PCB Pad建议设计 W0.5~0.6mm \* L1.25mm, 且周边1mm~1.5mm区域考虑不放置零件以利外加锡量
- 钢网建议厚度为0.12mm~0.15mm, W0.15~0.5mm \* L1.4~1.5mm
- 因为模块需要侧面爬锡, 当钢网厚度越薄外加锡量需越多, 需依实际生产状态评估, 当使用钢网0.08mm或0.1mm且外加可能性低时则必须考虑局部加厚钢网的设计。
- 钢网设计主要以增加足锡的焊锡膏量考量
- 周边1mm~1.5mm区域考虑不放置零件以利SMT钢网外加锡量

# 13. Package Information

## 13.1 Label

Label A→ Anti-static and humidity notice








Label B→ MSL caution / Storage Condition

| Caution  |  | LEVEL  |
|--|--|--|
| This bag contains<br>MOISTURE-SENSITIVE DEVICES  |  | <input type="checkbox"/><br><small>If blank, see adjacent bar code label</small> |
| 1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)<br>2. Peak package body temperature: _____ °C<br><small>If blank, see adjacent bar code label</small><br>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be<br>a) Mounted within: _____ hours of factory conditions<br><small>If blank, see adjacent bar code label</small><br>≤30°C/60% RH, or<br>b) Stored per J-STD-033<br>4. Devices require bake, before mounting, if:<br>a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C<br>b) 3a or 3b are not met<br>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure<br>Bag Seal Date: _____<br><small>If blank, see adjacent bar code label</small><br><small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small> |  |  |

Label C→ Inner box label .

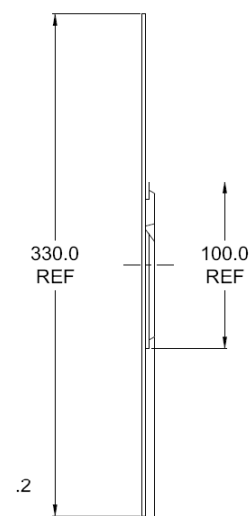
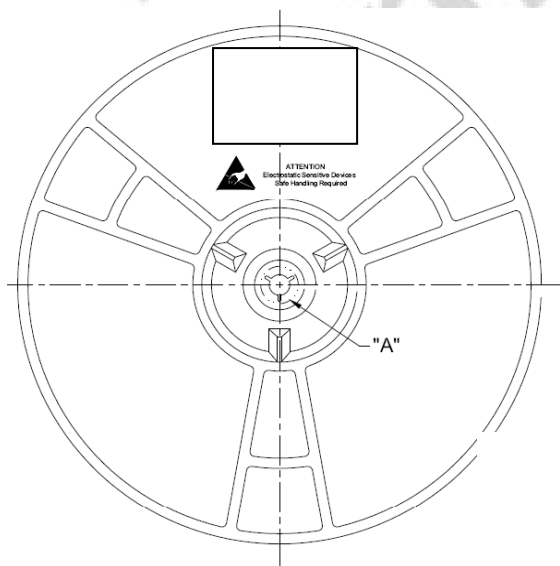
|             |  |
|-------------|--|
| PKG S/N :   | <br>9PKG12013100001 |
| Model:      | <br>XXXXXXXXXXXX   |
| P/N :       | <br>99P-W01-0048R  |
| Qty :       | <br>1500            |
| Date Code : | <br>1205            |
| Lot Code :  | <br>T0C102B         |

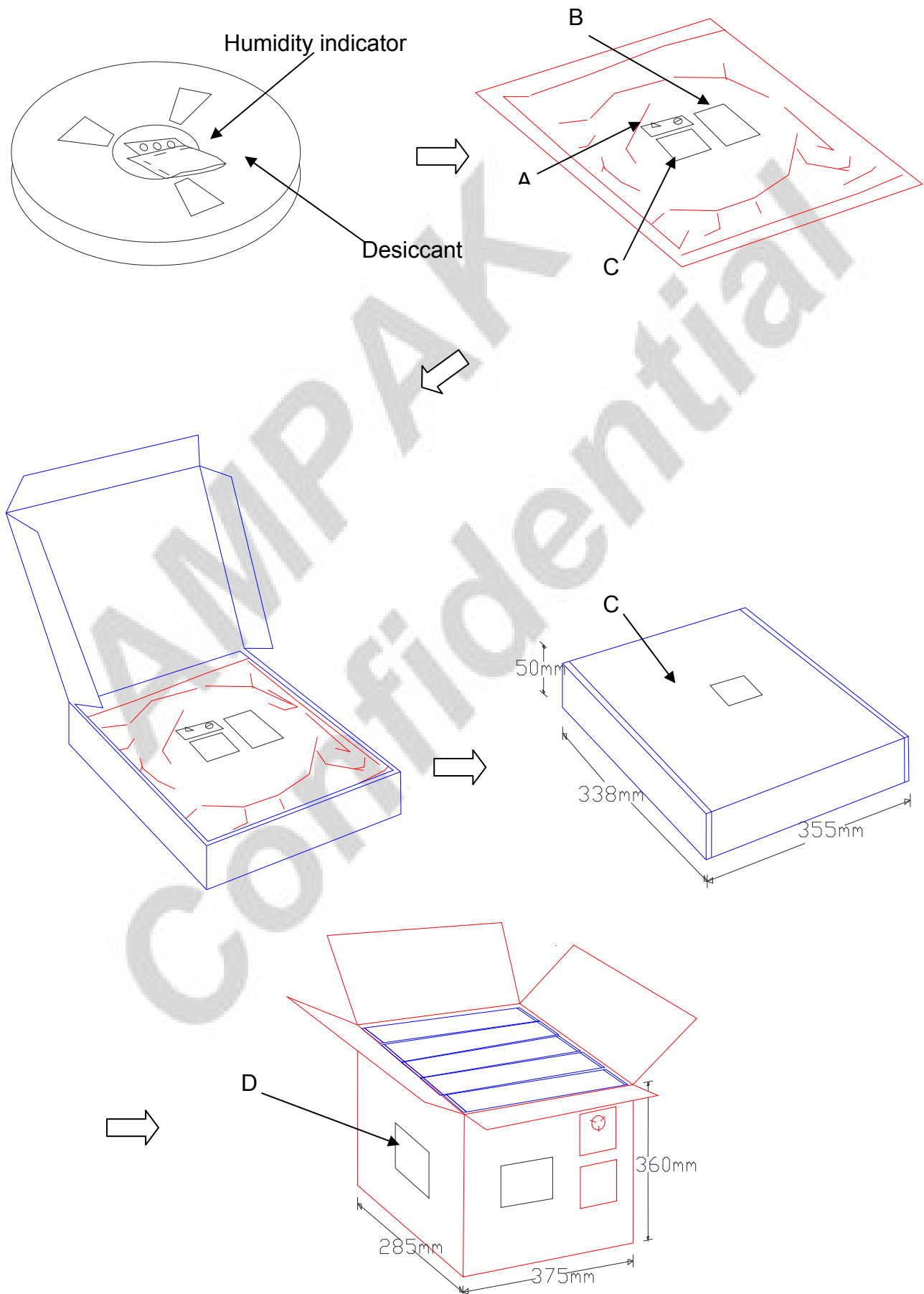
Label D→ Carton box label .

| AMPAK Technology |  |
|------------------|--|
| Model Name :     | <br>XXXXXXXXXXXX  |
| Part No :        | <br>99P-W01-0048R |
| Quantity :       | <br>7500 ea       |
| Lot D/C :        | <br>20081000033   |
| Manufacture :    | <br>2012/02/22    |


## 13.2 Dimension (TBD)

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness :  $0.30 \pm 0.05$  mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





### 13.3 MSL Level / Storage Condition

|   |  |  |
|---|--|--|
|  | <p><b>Caution</b></p> <p>This bag contains</p> <p><b>MOISTURE-SENSITIVE DEVICES</b></p> <p>Do not open except under controlled conditions</p> <p>1. Calculated shelf life in sealed bag: 12 months at <math>&lt; 40^{\circ}\text{C}</math> and <math>&lt; 90\%</math> relative humidity(RH)</p> <p>2. Peak package body temperature:      <math>225^{\circ}\text{C}</math>   <math>240^{\circ}\text{C}</math>   <math>250^{\circ}\text{C}</math>   <math>260^{\circ}\text{C}</math></p> <p style="margin-left: 100px;"> <input type="checkbox"/>    <input type="checkbox"/>    <input checked="" type="checkbox"/>    <input type="checkbox"/> </p> <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must</p> <p style="margin-left: 20px;">a) Mounted within: 48 hours of factory conditions</p> <p style="margin-left: 40px;"><math>&lt; 30^{\circ}\text{C}/60\% \text{ RH}</math>, OR</p> <p style="margin-left: 20px;">b) Stored at <math>&lt; 10\% \text{ RH}</math></p> <p>4. Devices require bake, before mounting, if:</p> <p style="margin-left: 20px;">a) Humidity Indicator Card is <math>&gt; 10\%</math> when read at <math>23 \pm 5^{\circ}\text{C}</math></p> <p style="margin-left: 20px;">b) 3a or 3b not met</p> <p>5. If baking is required, devices may be baked for 24 hours at <math>125 \pm 5^{\circ}\text{C}</math></p> <p>Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure</p> <p>Bag Seal Date:      <b>See-SEAL DATE LABEL</b></p> <p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p> | <p>LEVEL</p> <div style="border: 1px solid black; width: 60px; height: 60px; margin: 0 auto; display: flex; align-items: center; justify-content: center; font-size: 24px; font-weight: bold;">4</div> |
|---|--|--|

※NOTE : Accumulated baking time should not exceed 96hrs