Rockchip RV1107 Datasheet

Revision 1.1
Mar. 2017

Revision History

Date	Revision	Description
2017-3-20	1.1	Update
2017-3-16	1.0	Initial Release

Table of Content

Figure Index

Table Index

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Chapter 1 Introduction

RV1107 is a high performance low power application processor. It is designed for the HD IP camera It is embedded with a new generation DSP for digital process and an ARM Cortex-A7 single core processor for system and application. Especially, it is a high-integration and cost efficient SoC which can support H.264 video encoder up to 1440p.It has these features of low bit rate, high picture quality and low power consumption.

RV1107 package with 16bit DDR3 chip to meet a high-performance up to 800MHz and make cost lower.

1.1 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.1.1 Microprocessor

- Single-core ARM Cortex-A7 Core processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Separately integrated NEON and FPU
- 32KB/32KB L1 I-Cache/D-Cache
- Unified 128KB L2 Cache.
- Trustzone technology support

1.1.2 Video/Image Digital Signal Processor

- 32KB I-TCM and 32KB I-cache
- 128KB D-TCM

1.1.3 Memory Organization

- Internal on-chip memory
  - BootRom
  - Internal SRAM
- External off-chip memory$^{\circledR}$
  - DDR3/DDR3L
  - Async NAND Flash

1.1.4 Internal Memory

- Internal BootRom
  - Size : 10KB
  - Support system boot from the following device :
    - ◆ 8bits Async NAND Flash
    - ◆ SPI interface
    - ◆ eMMC interface
    - ◆ SDMMC interface
  - Support system code download by the following interface:
    - ◆ USB OTG interface
- Internal SRAM
  - Size : 12KB

1.1.5 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L)

- Compatible with JEDEC standard DDR3-1600/DDR3L-1600 SDRAM
- Supports 16 Bits data width, 1 ranks (chip selects), totally 512MB (max) address space.
- Programmable timing parameters to support DDR3/DDR3L SDRAM from various vendor
- Advanced command reordering and scheduling to maximize bus utilization
- Low power modes, such as power-down and self-refresh for DDR3 SDRAM; Compensation for board delays and variable latencies through programmable pipelines
- Programmable output and ODT impedance with dynamic PVT compensation

- NAND Flash Interface
  - Support 8bits async NAND flash
  - 16bits hardware ECC
  - For async NAND flash, support configurable interface timing,
  - maximum data rate is 8bit/cycle
  - Embedded AHB master interface to do data transfer by DMA method

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.51 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.1.6 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RV1107
  - One oscillator with 24MHz clock input and 3 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- Timer
  - 2 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Eight on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with one 128-bits AXI masters, one APB slaves
    - DSP interconnect with two 128-bits AXI masters, one 128-bits AXI slave, one 32-bits APB master and many 32-bits APB slaves
    - PERI interconnect with eight 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with two 128-bits AXI master, seven 64-bits AXI masters and lots 32-bits AHB/APB slave
    - VENC interconnect with two 128-bits AXI masters, and one 32-bits AHB slaves
    - VDEC interconnect also with two 64-bits AXI master and two 32-bits AHB slaves
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 128 SPI interrupt sources input from different components inside RV1107
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ)separately for each Cortex-A7, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
  - One non-maskable interrupt for DSP
  - Four hardware maskable interrupts for DSP
  - Four software maskable interrupts

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - One embedded DMA controller for system
  - DMAC features:
    - 8 channels totally
    - 16 hardware request from peripherals
    - 2 interrupt output
    - Dual APB slave interface for register configuration, designated as secure and

non-secure
◆ Support trustzone technology and programmable secure state for each DMA channel

- Security system
  - Embedded encryption and decryption engine
    ◆ Support AES 128/192/256 bits key mode, ECB/CBC/CTR chain mode, Slave/FIFO mode
    ◆ Support DES/3DES (ECB and CBC chain mode) , 3DES (EDE/ EEE key mode), Slave/FIFO mode
    ◆ Support SHA1/SHA256/MD5 (with hardware padding) HASH function, FIFO mode only
    ◆ Support 160 bit Pseudo Random Number Generator (PRNG)
    ◆ Support PKA 512/1024/2048 bit Exp Modulator

1.1.7 Camera interface

- ISP
  - Generic Sensor Interface with programmable polarity for synchronization signals
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12 bit camera interface
  - 12 bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - Flash light control
  - Mechanical shutter support
  - Windowing and frame synchronization
  - Frame skip support for video (e.g. MPEG-4) encoding
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Buffer in system memory organized as ring-buffer
  - Buffer overflow protection for raw data
  - Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
  - Interconnect test support
  - Semi planar storage format
  - Color processing (contrast, saturation, brightness, hue, offset, range)
  - Power management by software controlled clock disabling of currently not needed sub-modules
  - Read port provided to read back a picture from system memory
  - Black level compensation
  - Four channel Lens shade correction (Vignetting)
  - Auto focus measurement
  - White balancing and black level measurement
  - Auto exposure support by brightness measurement in 5x5 sub windows
  - Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
  - De-noising pre filter (DPF)
  - Enhanced color interpolation (RGB Bayer demosaic)
  - Chromatic aberration correction
  - Combined edge sensitive Sharpening / Blurring filter (Noise filter)
  - Color correction matrix (cross talk matrix)
  - Image Stabilization support and Video Stabilization Measurement
  - Flexible Histogram calculation
  - Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)

- Solarize effect through gamma correction
- AXI 64 bit interface 32Bit Address range (two DMA-write ports and one DMA-read port)
- Up to 16 Beat Bursts depending on configured FIFO size
- 32 bit AHB programming interface
- Maximum input resolution of 3264x2448 pixels
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 3264x2448 and 32x16 pixel in processing mode

- Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
- Support of semiplanar NV21 color storage format
- Support of image cropping
- Support Y12BIT and UV 8BIT path output after GAMMAOUT module
- Support RGB output after GAMMAOUT module
- Support hurry for latency FIFO
- Support Two-in-one RK-Tone-Mapping with wide dynamic range unit (Block/Global WDR)
- Support Video Stabilization Measurement (VSM) Programming update to 3264x2448

- CIF
  - Support YCbCr422 input
  - Support Raw 8bit input
  - Support CCIR656(PAL/NTSC) input
  - Support 1/2/4 channels mixed data of CCIR656 input
  - Support JPEG input
  - Support YCbCr422/420 output
  - Support UYVY/VYUY/YUYV/YVYU configurable
  - Support up to 8192x8192 resolution source
  - Support picture in picture
  - Support arbitrary size window crop
  - Support error/terminate interrupt and combined interrupt output
  - Support CLK/VSYNC/HREF polarity configurable
  - Support one frame stop/ping-pong mode

1.1.8 Video Encoder

- Support video encoder for H.264 UP to HP@level4.2
- Only support I and P slices ,not B slices
- Support CBR and VBR
- Support 8-area OSD insertion
- Support Link table configuration for high frame rate application
- Support ROI
- Support Slice split
- Support Low latency encoding
- Support Color domain conversion
- Support Cropping and mirror
- Support De-noise and enhancement
- Input data format:
  - YCbCr 4:2:0 planar
  - YCbCr 4:2:0 semi-planar
  - YCbCr 4:2:2 planar

- ◆ YCbCr 4:2:2 semi-planar
- ◆ YCbYCr 4:2:2 interleaved
- ◆ YCbCr 4:4:4 planar
- ◆ YCbCr 4:4:4 semi-planar
- ◆ RBG565
- ◆ RBG888
- ◆ ARBG8888
- ◼ Output Bit stream of H.264 "slice_layer_without_partitioning_rbsp()"
- ◼ Output ME results(SAD and MV) for each 16x16 block (optional)
- ◼ Image size is from 128x128 to 4096x2304
- ◼ Maximum frame rate is up to 2560x1440@30fps + 1280x720@30fps

1.1.9 JPEG CODEC

- ● JPEG codec
  - ◼ Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - ◼ Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - ◼ Support decode and encode from 48x48 to 8176x8176(66.8Mpixels), step size 8 pixels
  - ◼ Support JPEG ROI(region of image) decode
  - ◼ Maximum data rate® is up to 76million pixels per second

1.1.10 Image Enhancement (IEP module)

- ● Image format support
  - ◼ Input data: YUV420/YUV422
  - ◼ Output data: YUV420/YUV422
  - ◼ YUV swap
  - ◼ UV SP/P
  - ◼ BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - ◼ YUV up/down sampling
- ● De-interlace
  - ◼ 3x5 Y motion detection matrix
  - ◼ Source width up to 720x576, 720x480
  - ◼ Configured high frequency de-interlace
  - ◼ I4O2 (Input 4 field, output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode
- ● Interface
  - ◼ 32bit AHB bus slave
  - ◼ 64bit AXI bus master
  - ◼ Combined interrupt output

1.1.11 Graphics Engine

- ● 2D Graphics Engine(RGA module) :
  - ◼ Source formats :
    - ◆ ABGR8888, XBGR888, ARGB8888, XRGB888
    - ◆ RGB888, RGB565
    - ◆ RGBA5551, RGBA4444
    - ◆ YUV420 planar, YUV420 semi-planar
    - ◆ YUV422 planar, YUV422 semi-planar
    - ◆ YUV 10-bit for YUV420/422 semi-planar
    - ◆ BPP8, BPP4, BPP2, BPP1
  - ◼ Destination formats :
    - ◆ ABGR8888, XBGR888, ARGB8888, XRGB888

- ◆ RGB888, RGB565
- ◆ RGBA5551, RGBA4444
- ◆ YUV420 planar, YUV420 semi-planar
- ◆ YUV422 planar, YUV422 semi-planar
- Pixel Format conversion, BT.601/BT.709
- Max resolution: 8192x8192 source, 4096x4096 destination
- BitBLT
  - ◆ Two source BitBLT:
  - ◆ A+B=B only BitBLT, A support rotate & scale when B fixed
  - ◆ A+B=C second source (B) has same attribute with (C) plus rotation function
- Color fill with gradient fill, and pattern fill
- High-performance stretch and shrink
- Monochrome expansion for text rendering
- New comprehensive per-pixel alpha(color/alpha channel separately)
- Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, pattern mask, fading
- Dither operation
- 0, 90, 180, 270 degree rotation
- x-mirror, y-mirror & rotation operation

1.1.12 Video OUT

- Display Interface
  - Support HDMI 1.4 output up to 1080p@60Hz
  - TV Interface: TV encoder 10bit out for DAC
  - HDMI Interface : 24 bit(RGB888 YCbCr444),
  - Max output resolution 1080p for HDMI, 480i/576i for CVBS

1.1.13 HDMI

- Support RGB888 1080p @ 60fps
- HPD input analog comparator
- Compliance HDMI compliance Test specification 1.4
- Support multi-channels PCM or compressed audio transmission (32-192kHz Fs) from I2S, using IEC60958 and IEC 61937

1.1.14 Audio Interface

- I2S0 with 8ch
  - I2S0 supports up to 8 channels (8xTX, 8xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- I2S1/I2S2(PCM) with 2ch
  - Up to 2 channels (2xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time
  - I2S1 is connected to HDMI and internal Audio Codec
  - I2S2 is exposed for peripherals

- Audio CODEC
  - 24bit DAC
  - Support Line-out
  - Support Mono, Stereo, 5.1 HiFi channel performance
  - Integrated digital interpolation and decimation filter.
  - Sampling rate of 8kHz/12kHz/16kHz/24kHz/32kHz/44.1KHz/48KHz/96KHz
  - Optional fractional PLL available that support 6MHz to 20MHz clock input to any clock
  - Support PCM/I2S Mode
  - Support MIC single-ended/double-ended difference input

1.1.15 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- MAC 10/100M Ethernet Controller
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation
    - Supports IEEE 802.3x flow control for full-duplex operation
    - Optional forwarding of received pause control frames to the user application in full-duplex operation
    - Back-pressure support for half-duplex operation
    - Automatic transmission of zero-quanta pause frame on de-assertion of flow control input in full-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable Inter-Frame-Gap (40-96 bit times in steps of 8)
  - Supports a variety of flexible address filtering modes
  - Separate 32-bit status returned for transmission and reception packets
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagram
  - Comprehensive status reporting for normal operation and transfers with errors
  - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
  - Handles automatic retransmission of Collision frames for transmission
  - Discards frames on late collision, excessive collisions, excessive deferral and under-run conditions

- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- SFC
  - Support one chip select
  - Support x1,x2,x4 data bits mode
  - Support interrupt output, interrupt maskable

- ■ Support Spansion, MXIC ,Gigadevice …vendor's nor flash memory.

- ● UART Controller
    - ■ 3 on-chip UART controller inside RV1107
    - ■ DMA-based or interrupt-based operation
    - ■ UART1/1/2 Embedded two 64Bytes FIFO for TX and RX operation respectively
    - ■ Support 5bit,6bit,7bit,8bit serial data transmit or receive
    - ■ Standard asynchronous communication bits such as start, stop and parity
    - ■ Support different input clock for UART operation to get up to 4Mbps or other special baud rate
    - ■ Support non-integer clock divides for baud clock generation
    - ■ Support auto flow control mode

- ● I2C controller
    - ■ 4 on-chip I2C controller in RV1107
    - ■ Multi-master I2C operation
    - ■ Support 7bits and 10bits address mode
    - ■ Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
    - ■ Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- ● GPIO
    - ■ 4 groups of GPIO (GPIO0~GPIO3) , 32 GPIOs per group in GPIO0~GPIO3, totally have 128 GPIOs
    - ■ All of GPIOs can be used to generate interrupt to Cortex-A7
    - ■ All of pull-up GPIOs are software-programmable for pull-up resistor or not
    - ■ All of pull-down GPIOs are software-programmable for pull-down resistor
    - ■ or not
    - ■ All of GPIOs are always in input direction in default after power-on-reset

- ● USB Host2.0
    - ■ Embedded one USB Host 2.0 interfaces
    - ■ Compatible with USB Host2.0 specification
    - ■ Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
    - ■ Provides 16 host mode channels
    - ■ Support periodic out channel in host mode

- ● USB OTG2.0
    - ■ Compatible with USB OTG2.0 specification
    - ■ Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
    - ■ Support up to 9 device mode endpoints in addition to control endpoint 0
    - ■ Support up to 6 device mode IN endpoints including control endpoint 0
    - ■ Endpoints 1/3/5/7 can be used only as data IN endpoint
    - ■ Endpoints 2/4/6 can be used only as data OUT endpoint
    - ■ Endpoints 8/9 can be used as data OUT and IN endpoint
    - ■ Provides 9 host mode channels

1.1.16 Others

- ● Temperature Sensor(TS-ADC)
    - ■ 10-bits ADC up to 50KS/s sampling rate
    - ■ -40~125℃ temperature range and 5℃ temperature resolution

- ● Successive Approximation ADC (SARADC)
    - ■ 10-bit resolution
    - ■ Up to 1MS/s sampling rate
    - ■ 6 single-ended input channels

- Current consumption: 0.5mA @ 1MS/s

- eFuse
  - Two high-density electrical Fuse is integrated: two 256bits (32x8)
  - Support standby mode
  - Provide inactive mode, VP must be 0V or Floating in this mode.

- Package Type
  - BGA359 (body: 14mm x 14mm ; ball size : 0.3mm ; ball pitch : 0.65mm;)
  - Support MCP with 128M DDR3L-1600.

Notes :
① : DDR3 are not used simultaneously
② : Actual maximum frame rate will depend on the clock frequency and system bus performance
③ : Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2 Block Diagram

The following diagram shows the basic block diagram for RV1107
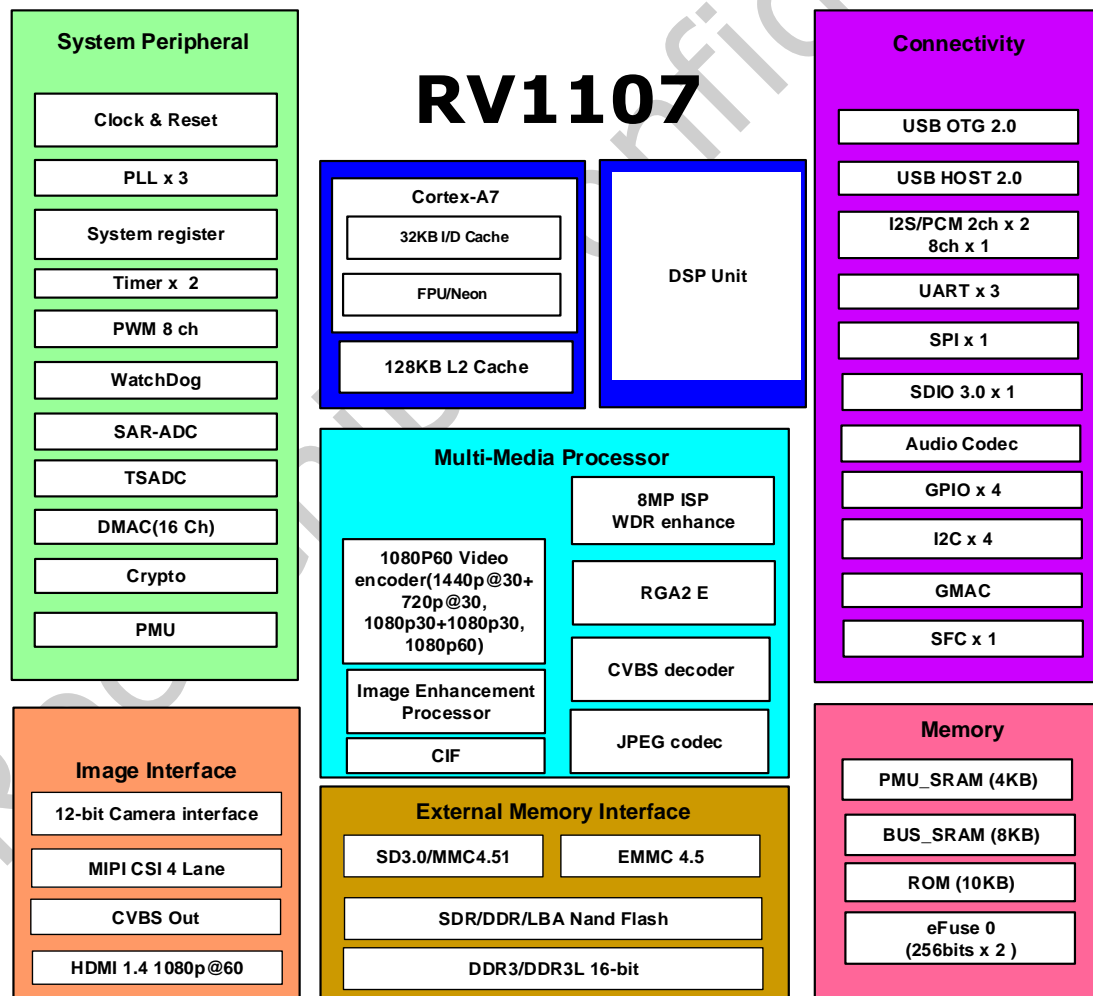
Fig. 1-1 RV1107 Block Diagram

Chapter 2 Package Information

2.1 Ordering information

Orderable Device	ROHS Status	Package	Package Qty	Device special feature
RV1107	ROHS	BGA359	1190	Cortex A7 + DSP + 128MB DDR3

2.2 Top Marking

Rockchip: Brand Name

RKXXXX: Chip Name

ABC: Subcontractor Code
XXXXXX: Die Lot NO#
DEFG: Date Code
● The first pin
NXXX.XXX: Production Line #

2.3 Dimension
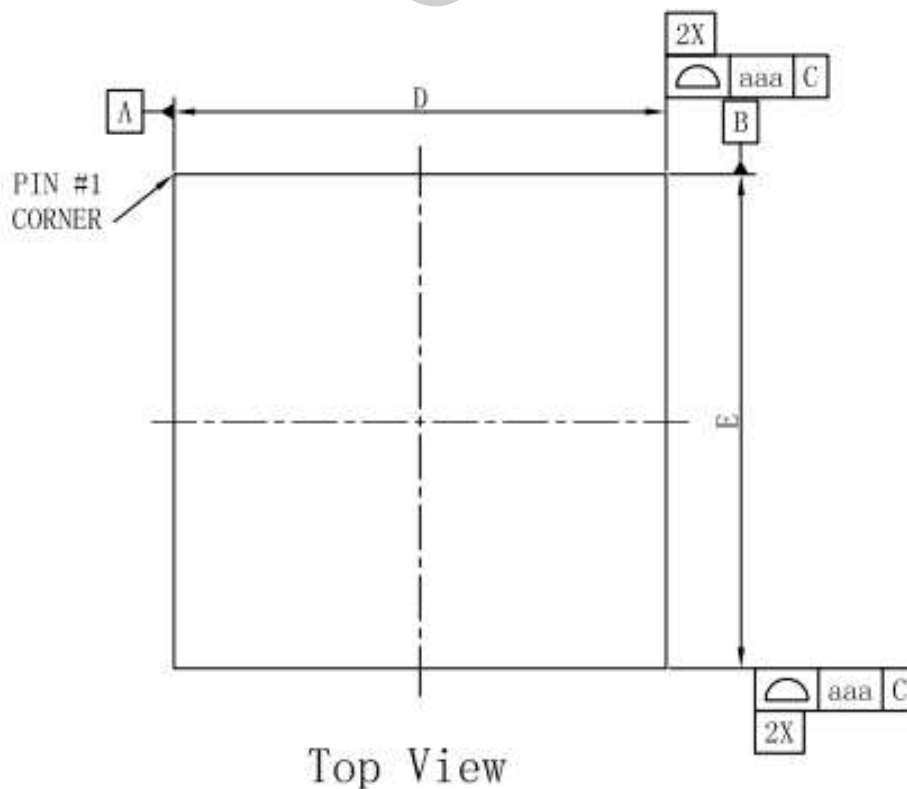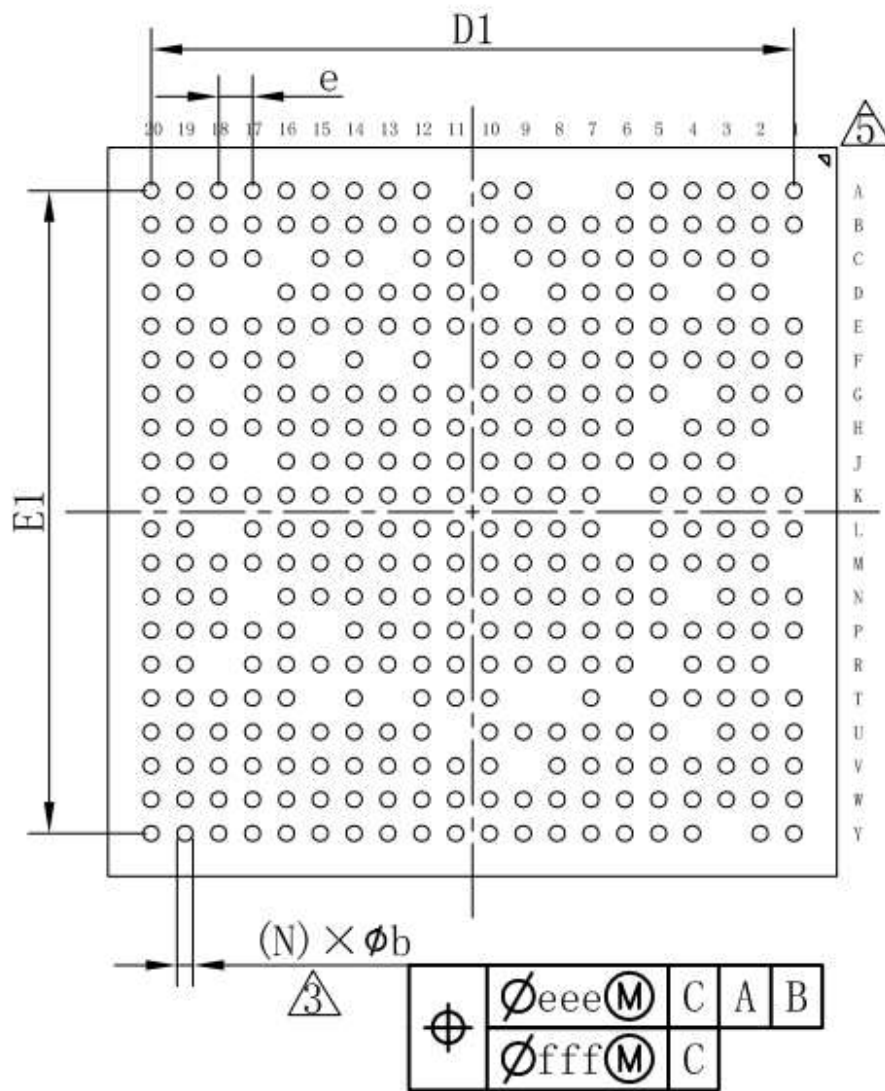
Top View

Fig. 2-1 RV1107 BGA359 Package Top View and bottom view
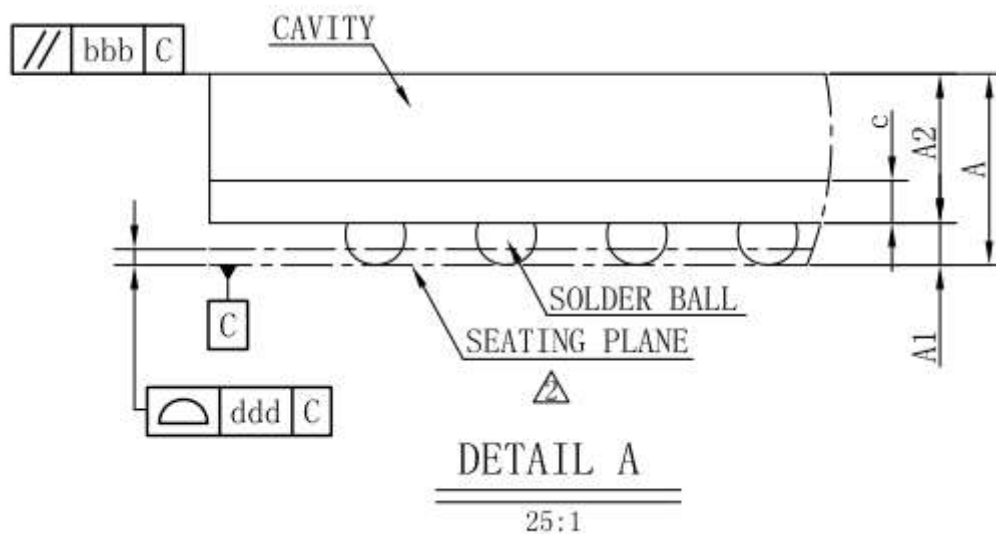
Side View

Fig. 2-2 RV1107 BGA359 Package Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.100	---	---	0.043
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.690	0.740	0.810	0.027	0.029	0.032
c	0.170	0.210	0.250	0.007	0.008	0.010
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	---	12.350	---	---	0.486	---
E1	---	12.350	---	---	0.486	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	359			359		
MD/ME	20/20			20/20		

Fig. 2-3 RV1107 BGA359 Package Dimension

2.4 Ball Map

	1	2	3	4	5	6	7	8	9	10	11
A	VSS_1	VSS_107	VSS_108	VSS_89	DDR_VDD_15	VSS_115	NP	NP	VSS_95	DDR_VDD_23	NP
B	VSS_109	VSS_110	VSS_111	VSS_112	DDR_VDD_16	VSS_113	VSS_114	VSS_98	VSS_116	DDR_VDD_24	SADC_AVDD_1V8
C	NP	DDR_VDD_12	DDR_VDD_13	VSS_97	DDR_VDD_17	VSS_90	VSS_96	DDR_VDD_22	VSS_117	NP	VSS_72
D	NP	VSS_88	DDR_VDD_14	NP	DDR_VDD_18	DDR_VDD_19	DDR_VDD_20	DDR_VDD_21	NP	ADC_IN3	GPIO3_B7/SDMMC0_PWR
E	VSS_85	VSS_122	VSS_123	PZQ	VSS_100	DDR_VDD_25	DDR_VDD_26	DDR_VDD_27	VSS_93	DDR_VDD_4	ADC_IN5
F	VSS_121	VSS_87	VSS_124	VSS_125	VSS_126	VREF	DDR_VDD_5	DDR_VDD_6	DDR_VDD_7	VSS_11	NP
G	VSS_118	VSS_119	VSS_86	NP	DDR_VDD_11	DDR_VDD_3	VSS_37	CORE_VDD_1	CORE_VDD_2	VSS_8	VSS_92
H	NP	DDR_VDD_8	DDR_VDD_9	DDR_VDD_10	NP	DDR_VDD_2	VSS_91	VSS_14	VSS_15	VSS_16	VSS_17
J	NP	NP	VSS_127	VSS_128	VSS_73	DDR_VDD_1	CORE_VDD_7	VSS_22	VSS_23	VSS_24	VSS_25
K	VSS_99	VSS_129	VSS_4	VSS_130	VSS_135	NP	VSS_29	VSS_30	VSS_31	VSS_32	VSS_33
L	VSS_131	VSS_132	VSS_133	VSS_120	VSS_13	NP	VSS_5	VSS_38	VSS_39	VSS_40	VSS_41

	12	13	14	15	16	17	18	19	20	
A	GPIO3_C2/SDMMC0_D1/UART2_RX	GPIO3_C5/SDMMC0_CMD	NC_2	CODEC_AOL	CODEC_AOR	CODEC_MICBIAS	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	GPIO1_D7/HDMI_CEC/DSP_RTCK	A
B	GPIO3_C3/SDMMC0_D0/UART2_TX	GPIO3_C4/SDMMC0_CLKO	NC_3	CODEC_MICR	CODEC_VCM	VSS_6	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	VSS_2	GPIO1_B3/I2S_SCLK/GMAC_TXD1	B
C	GPIO3_C0/SDMMC0_D3	NP	NC_1	CODEC_MICL	NP	5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	5VGPIO1_D6/HDMI_HPD0	GPIO1_B4/I2S_MCLK/GMAC_TXEN	GPIO1_B6/I2S_LRCLKTX/GMAC_RXD1	C
D	GPIO3_C1/SDMMC0_D2	ADC_IN0	VSS_69	CODEC_AVDD_1V8	VSS_60	NP	NP	GPIO1_D2/UART1_RX/SPI_RXD	GPIO1_C2/I2S_SDIO3/GMAC_RXER	D
E	ADC_IN2	ADC_IN1	NC_4	CODEC_AVSS	GPIO2_D2/UART2_TX/JTAG_TCK	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	GPIO1_C0/I2S_LRCLKRX	GPIO1_C1/I2S_SDI/PWM4	GPIO1_C3/GMAC_MDIO	E
F	ADC_IN4	NP	APIO3_VDD	NP	GPIO2_D1/UART2_RX/JTAG_TMS	GPIO1_B2/I2S_SDO/GMAC_TXD0	GPIO1_B5/I2S_SDIO1/GMAC_RXD0	GPIO1_C4/GMAC_MDC	GPIO2_B1/FLASH_CLE	F
G	VSS_102	VSS_7	VSS_10	CORE_VDD_4	GPIO1_B7/I2S_SDIO2/GMAC_RXDV	GPIO1_C5/GMAC_CLK	NP	GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	GPIO2_A4/FLASH_D4/EMMC_D4	G
H	VSS_18	VSS_19	VSS_20	VSS_105	APIO1_VDD	GPIO2_C2/FLASH_WP/EMMC_PWR	GPIO2_B0/FLASH_ALE	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	GPIO2_A7/FLASH_D7/EMMC_D7	H
J	VSS_26	VSS_27	VSS_103	CORE_VDD_3	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1	NP	GPIO2_B7/FLASH_CSN1/SFC_CLK	GPIO2_A5/FLASH_D5/EMMC_D5	GPIO2_B5/FLASH_CSN0	J
K	VSS_34	VSS_35	VSS_36	VSS_106	APIO6_VDD	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	GPIO2_B2/FLASH_WRN	GPIO2_B6/EMMC_CLKO	K
L	VSS_42	VSS_43	VSS_28	CORE_VDD_6	GPIO2_A6/FLASH_D6/EMMC_D6	GPIO2_B3/FLASH_RDN	NP	GPIO2_D7/SDIO_D0	GPIO2_D6/SDIO_CMD	L

	1	2	3	4	5	6	7	8	9	10	11
M	NP	VSS_134	GPIO0_A7/SPI_TXD	GPIO0_C0/PWM3/IR	GPIO0_B7/TSADC_SHUT	PLL_AVDD_1V0	VSS_45	VSS_46	VSS_47	VSS_48	VSS_49
N	GPIO0_B6/I2C3_SCL	VSS_74	EFUSE	NP	GPIO0_B5/PMIC_SLEEP	PLL_AVDD_1V8	VSS_53	VSS_54	VSS_55	VSS_56	VSS_57
P	XIN_24M	XOUT24M	VSS_61	GPIO0_A3/SPI_CLK	GPIO0_A4/SPI_CSN0	GPIO0_C3/PMU_DEBUG2	TEST	VSS_62	VSS_63	VSS_64	VSS_65
R	NP	GPIO0_B3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	GPIO0_B2/I2C0_SDA	NP	PMU_DVDD_1V0	CORE_VDD_8	PMUIO_VDD	VSS_71	VSS_44	VSS_101
T	NPOR	GPIO0_C5/PWM0/PMU_DEBUG3	GPIO0_C4/PWM1/I2C3_SDA	GPIO0_B1/I2C0_SCL	GPIO0_B4	NP	GPIO0_A1/SDMMC0_DET	NP	NP	USB_AVDD_1V8	USB_AVDD_3V3
U	GPIO0_A2/SDMMC1_PWR	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN	NP	GPIO0_B0/SPI_RXD	HDMI_EXTR	VDAC_AVDD_1V8	APO_AVDD_1V8	APO_VDD_3V3	USB_EXTR	NP
V	GPIO0_A6/PMU_DEBUG0	GPIO0_A5/CLK_WIFI_OUT	HDMI_AVDD_1V8	VSS_78	HDMI_AVDD_1V0	VSS_79	APO_VDD_1V0	VSS_80	NP	VSS_81	USB0_ID
W	HDMI_TXCP	HDMI_TX0N	HDMI_TX0P	HDMI_TX1N	HDMI_TX2P	VDAC_EXTR	GPIO1_B1/PWM7	GPIO1_A7/PWM5	GPIO1_A1	GPIO1_A4	GPIO1_A2
Y	HDMI_TXCN	VSS_77	NP	HDMI_TX1P	HDMI_TX2N	VDAC_OUT	GPIO1_B0/PWM6	GPIO1_A6	GPIO1_A0	GPIO1_A5	GPIO1_A3

12	13	14	15	16	17	18	19	20	
VSS_50	VSS_51	VSS_52	VSS_70	VSS_104	GPIO3_A2/SDIO_D3	GPIO3_A0/SDIO_D1	GPIO2_D5/SDIO_CLKO	GPIO3_A1/SDIO_D2	M
VSS_58	VSS_59	VSS_12	CORE_VDD_5	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT	NP	GPIO3_B2/PCM_IN/FLASH_TRIG_IN	GPIO3_B6	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	N
VSS_66	VSS_67	VSS_68	NP	APIO5_VDD	GPIO3_A6/UART0_TX	GPIO3_A4/UART0_CTSN	GPIO3_A7	GPIO3_B5/MIPI_CSI_MCLK	P
VSS_9	VSS_75	VSS_76	VSS_94	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	GPIO2_D4/I2C1_SCL	NP	GPIO3_B3/PCM_CLK	GPIO3_A3/UART0_RTSN	R
USB_VDD_1V0	NP	VSS_21	NP	APIO2_VDD	GPIO3_D1/CIF_PDN	GPIO3_C7/CIF_CLKIN	GPIO2_D3/I2C1_SDA	GPIO3_A5/UART0_RX	T
MIPI_CSI_EXTR	MIPI_CSI_AVDD_1V0	GPIO2_C1/CIF_D7/I2S_SDI	GPIO2_C5/CIF_D2/I2S_MCLK	GPIO2_C4/CIF_D1/I2S_SCLK	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	GPIO3_D0/CIF_HREF	GPIO1_C7/CIF_D5/I2S_SDIO2	GPIO3_B0	U
USB_VBUS	VSS_82	GPIO2_C6/CIF_D3/I2S_SDIO1	VSS_83	GPIO2_C3/CIF_D0/I2S_SDO	VSS_84	GPIO3_D2/CIF_CLKOUT	GPIO3_C6/CIF_VSYNC	GPIO1_C6/CIF_D4//I2S_LRCLKTX	V
USB0_DP	USB1_DP	MIPI_CSI_D0N	MIPI_CSI_D1N	MIPI_CSI_CLKP	MIPI_CSI_D2N	MIPI_CSI_D3P	VSS_3	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	W
USB0_DM	USB1_DM	MIPI_CSI_D0P	MIPI_CSI_D1P	MIPI_CSI_CLKN	MIPI_CSI_D2P	MIPI_CSI_D3N	GPIO2_C0/CIF_D6/I2S_LRCLKRX	GPIO3_D3/CIF_D8/I2S_SDIO3	Y
12	13	14	15	16	17	18	19	20	

Fig. 2-4 RV1107 BGA 359 Ball Map

2.5 Ball Pin Number Order

Table 2-1 RV1107 BGA359 Pin Number Order Information

Pin Number	Pin Name	Pin Number	Pin Name
A1	VSS_1	L1	VSS_131
A2	VSS_107	L2	VSS_132
A3	VSS_108	L3	VSS_133
A4	VSS_89	L4	VSS_120
A5	DDR_VDD_15	L5	VSS_13
A6	VSS_115	L6	NP
A7	NP	L7	VSS_5
A8	NP	L8	VSS_38
A9	VSS_95	L9	VSS_39
A10	DDR_VDD_23	L10	VSS_40
A11	NP	L11	VSS_41
A12	GPIO3_C2/SDMMC0_D1/UART2_RX	L12	VSS_42
A13	GPIO3_C5/SDMMC0_CMD	L13	VSS_43
A14	NC_2	L14	VSS_28
A15	CODEC_AOL	L15	CORE_VDD_6
A16	CODEC_AOR	L16	GPIO2_A6/FLASH_D6/EMMC_D6
A17	CODEC_MICBIAS	L17	GPIO2_B3/FLASH_RDN
A18	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	L18	NP
A19	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	L19	GPIO2_D7/SDIO_D0
A20	GPIO1_D7/HDMI_CEC/DSP_RTCK	L20	GPIO2_D6/SDIO_CMD
B1	VSS_109	M1	NP
B2	VSS_110	M2	VSS_134
B3	VSS_111	M3	GPIO0_A7/SPI_TXD
B4	VSS_112	M4	GPIO0_C0/PWM3/IR
B5	DDR_VDD_16	M5	GPIO0_B7/TSADC_SHUT
B6	VSS_113	M6	PLL_AVDD_1V0
B7	VSS_114	M7	VSS_45
B8	VSS_98	M8	VSS_46
B9	VSS_116	M9	VSS_47
B10	DDR_VDD_24	M10	VSS_48
B11	SADC_AVDD_1V8	M11	VSS_49
B12	GPIO3_C3/SDMMC0_D0/UART2_TX	M12	VSS_50
B13	GPIO3_C4/SDMMC0_CLKO	M13	VSS_51
B14	NC_3	M14	VSS_52
B15	CODEC_MICR	M15	VSS_70
B16	CODEC_VCM	M16	VSS_104
B17	VSS_6	M17	GPIO3_A2/SDIO_D3
B18	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	M18	GPIO3_A0/SDIO_D1
B19	VSS_2	M19	GPIO2_D5/SDIO_CLKO
B20	GPIO1_B3/I2S_SCLK/GMAC_TXD1	M20	GPIO3_A1/SDIO_D2
C1	NP	N1	GPIO0_B6/I2C3_SCL
C2	DDR_VDD_12	N2	VSS_74
C3	DDR_VDD_13	N3	EFUSE
C4	VSS_97	N4	NP

Pin Number	Pin Name	Pin Number	Pin Name
C5	DDR_VDD_17	N5	GPIO0_B5/PMIC_SLEEP
C6	VSS_90	N6	PLL_AVDD_1V8
C7	VSS_96	N7	VSS_53
C8	DDR_VDD_22	N8	VSS_54
C9	VSS_17	N9	VSS_55
C10	NP	N10	VSS_56
C11	VSS_72	N11	VSS_57
C12	GPIO3_C0/SDMMC0_D3	N12	VSS_58
C13	NP	N13	VSS_59
C14	NC_1	N14	VSS_12
C15	CODEC_MICL	N15	CORE_VDD_5
C16	NP	N16	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT
C17	5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	N17	NP
C18	5VGPIO1_D6/HDMI_HPD0	N18	GPIO3_B2/PCM_IN/FLASH_TRIG_IN
C19	GPIO1_B4/I2S_MCLK/GMAC_TXEN	N19	GPIO3_B6
C20	GPIO1_B6/I2S_LRCLKTX/GMAC_RXD1	N20	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT
D1	NP	P1	XIN_24M
D2	VSS_88	P2	XOUT24M
D3	DDR_VDD_14	P3	VSS_61
D4	NP	P4	GPIO0_A3/SPI_CLK
D5	DDR_VDD_18	P5	GPIO0_A4/SPI_CSN0
D6	DDR_VDD_19	P6	GPIO0_C3/PMU_DEBUG2
D7	DDR_VDD_20	P7	TEST
D8	DDR_VDD_21	P8	VSS_62
D9	NP	P9	VSS_63
D10	ADC_IN3	P10	VSS_64
D11	GPIO3_B7/SDMMC0_PWR	P11	VSS_65
D12	GPIO3_C1/SDMMC0_D2	P12	VSS_66
D13	ADC_IN0	P13	VSS_67
D14	VSS_69	P14	VSS_68
D15	CODEC_AVDD_1V8	P15	NP
D16	VSS_60	P16	APIO5_VDD
D17	NP	P17	GPIO3_A6/UART0_TX
D18	NP	P18	GPIO3_A4/UART0_CTSN
D19	GPIO1_D2/UART1_RX/SPI_RXD	P19	GPIO3_A7
D20	GPIO1_C2/I2S_SDIO3/GMAC_RXER	P20	GPIO3_B5/MIPI_CSI_MCLK
E1	VSS_85	R1	NP
E2	VSS_122	R2	GPIO0_B3
E3	VSS_123	R3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4
E4	PZQ	R4	GPIO0_B2/I2C0_SDA
E5	VSS_100	R5	NP
E6	DDR_VDD_25	R6	PMU_DVDD_1V0
E7	DDR_VDD_26	R7	CORE_VDD_8
E8	DDR_VDD_27	R8	PMUIO_VDD

Pin Number	Pin Name	Pin Number	Pin Name
E9	VSS_93	R9	VSS_71
E10	DDR_VDD_4	R10	VSS_44
E11	ADC_IN5	R11	VSS_101
E12	ADC_IN2	R12	VSS_9
E13	ADC_IN1	R13	VSS_75
E14	NC_4	R14	VSS_76
E15	CODEC_AVSS	R15	VSS_94
E16	GPIO2_D2/UART2_TX/JTAG_TCK	R16	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT
E17	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	R17	GPIO2_D4/I2C1_SCL
E18	GPIO1_C0/I2S_LRCLKRX	R18	NP
E19	GPIO1_C1/I2S_SDI/PWM4	R19	GPIO3_B3/PCM_CLK
E20	GPIO1_C3/GMAC_MDIO	R20	GPIO3_A3/UART0_RTSN
F1	DDR_121	T1	NPOR
F2	VSS_87	T2	GPIO0_C5/PWM0/PMU_DEBUG3
F3	VSS_124	T3	GPIO0_C4/PWM1/I2C3_SDA
F4	VSS_125	T4	GPIO0_B1/I2C0_SCL
F5	VSS_126	T5	GPIO0_B4
F6	VREF	T6	NP
F7	DDR_VDD_5	T7	GPIO0_A1/SDMMC0_DET
F8	DDR_VDD_6	T8	NP
F9	DDR_VDD_7	T9	NP
F10	VSS_11	T10	USB_AVDD_1V8
F11	NP	T11	USB_AVDD_3V3
F12	ADC_IN4	T12	USB_VDD_1V0
F13	NP	T13	NP
F14	APIO3_VDD	T14	VSS_21
F15	NP	T15	NP
F16	GPIO2_D1/UART2_RX/JTAG_TMS	T16	APIO2_VDD
F17	GPIO1_B2/I2S_SDO/GMAC_TXD0	T17	GPIO3_D1/CIF_PDN
F18	GPIO1_B5/I2S_SDIO1/GMAC_RXD0	T18	GPIO3_C7/CIF_CLKIN
F19	GPIO1_C4/GMAC_MDC	T19	GPIO2_D3/I2C1_SDA
F20	GPIO2_B1/FLASH_CLE	T20	GPIO3_A5/UART0_RX
G1	VSS_118	U1	GPIO0_A2/SDMMC1_PWR
G2	VSS_119	U2	GPIO0_C2/I2C2_SDA/PMU_DEBUG1
G3	VSS_86	U3	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN
G4	NP	U4	NP
G5	DDR_VDD_11	U5	GPIO0_B0/SPI_RXD
G6	DDR_VDD_3	U6	HDMI_EXTR
G7	VSS_37	U7	VDAC_AVDD_1V8
G8	CORE_VDD_1	U8	APO_VDD_1V8
G9	CORE_VDD_2	U9	APO_VDD_3V3
G10	VSS_8	U10	USB_EXTR
G11	VSS_92	U11	NP
G12	VSS_102	U12	MIPI_CSI_EXTR
G13	VSS_7	U13	MIPI_CSI_AVDD_1V0

Pin Number	Pin Name	Pin Number	Pin Name
G14	VSS_10	U14	GPIO2_C1/CIF_D7/I2S_SDI
G15	CORE_VDD_4	U15	GPIO2_C5/CIF_D2/I2S_MCLK
G16	GPIO1_B7/I2S_SDIO2/GMAC_RXDV	U16	GPIO2_C4/CIF_D1/I2S_SCLK
G17	GPIO1_C5/GMAC_CLK	U17	GPIO3_D4/CIF_D9/FLASH_TRIG_IN
G18	NP	U18	GPIO3_D0/CIF_HREF
G19	GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	U19	GPIO1_C7/CIF_D5/I2S_SDIO2
G20	GPIO2_A4/FLASH_D4/EMMC_D4	U20	GPIO3_B0
H1	NP	V1	GPIO0_A6/PMU_DEBUG0
H2	DDR_VDD_8	V2	GPIO0_A5/CLK_WIFI_OUT
H3	DDR_VDD_9	V3	HDMI_AVDD_1V8
H4	DDR_VDD_10	V4	VSS_78
H5	NP	V5	HDMI_AVDD_1V0
H6	DDR_VDD_2	V6	VSS_79
H7	VSS_91	V7	APO_VDD_1V0
H8	VSS_14	V8	VSS_80
H9	VSS_15	V9	NP
H10	VSS_16	V10	VSS_81
H11	VSS_17	V11	USB0_ID
H12	VSS_18	V12	USB_VBUS
H13	VSS_19	V13	VSS_82
H14	VSS_20	V14	GPIO2_C6/CIF_D3/I2S_SDIO1
H15	VSS_105	V15	VSS_83
H16	APIO1_VDD	V16	GPIO2_C3/CIF_D0/I2S_SDO
H17	GPIO2_C2/FLASH_WP/EMMC_PWR	V17	VSS_84
H18	GPIO2_B0/FLASH_ALE	V18	GPIO3_D2/CIF_CLKOUT
H19	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	V19	GPIO3_C6/CIF_VSYNC
H20	GPIO2_A7/FLASH_D7/EMMC_D7	V20	GPIO1_C6/CIF_D4//I2S_LRCLKTX
J1	NP	W1	HDMI_TXCP
J2	NP	W2	HDMI_TX0N
J3	VSS_127	W3	HDMI_TX0P
J4	VSS_128	W4	HDMI_TX1N
J5	VSS_73	W5	HDMI_TX2P
J6	DDR_VDD_1	W6	VDAC_EXTR
J7	CORE_VDD_7	W7	GPIO1_B1/PWM7
J8	VSS_22	W8	GPIO1_A7/PWM5
J9	VSS_23	W9	GPIO1_A1
J10	VSS_24	W10	GPIO1_A4
J11	VSS_25	W11	GPIO1_A2
J12	VSS_26	W12	USB0_DP
J13	VSS_27	W13	USB1_DP
J14	VSS_103	W14	MIPI_CSI_D0N
J15	CORE_VDD_3	W15	MIPI_CSI_D1N
J16	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1	W16	MIPI_CSI_CLKP
J17	NP	W17	MIPI_CSI_D2N

Pin Number	Pin Name	Pin Number	Pin Name
J18	GPIO2_B7/FLASH_CSN1/SFC_CLK	W18	MIPI_CSI_D3P
J19	GPIO2_A5/FLASH_D5/EMMC_D5	W19	VSS_3
J20	GPIO2_B5/FLASH_CSN0	W20	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT
K1	VSS_99	Y1	HDMI_TXCN
K2	VSS_129	Y2	VSS_77
K3	VSS_4	Y3	NP
K4	VSS_130	Y4	HDMI_TX1P
K5	VSS_135	Y5	HDMI_TX2N
K6	NP	Y6	VDAC_OUT
K7	VSS_29	Y7	GPIO1_B0/PWM6
K8	VSS_30	Y8	GPIO1_A6
K9	VSS_31	Y9	GPIO1_A0
K10	VSS_32	Y10	GPIO1_A5
K11	VSS_33	Y11	GPIO1_A3
K12	VSS_34	Y12	USB0_DM
K13	VSS_35	Y13	USB1_DM
K14	VSS_36	Y14	MIPI_CSI_D0P
K15	VSS_106	Y15	MIPI_CSI_D1P
K16	APIO6_VDD	Y16	MIPI_CSI_CLKN
K17	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	Y17	MIPI_CSI_D2P
K18	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	Y18	MIPI_CSI_D3N
K19	GPIO2_B2/FLASH_WRN	Y19	GPIO2_C0/CIF_D6/I2S_LRCLKRX
K20	GPIO2_B6/EMMC_CLKO	Y20	GPIO3_D3/CIF_D8//I2S_SDIO3

2.6 RV1107 Power/ground IO descriptions

Table 2-2 RV1107 Power/Ground IO information

Group	Ball#	Descriptions
GND	A1,A2,A3,A4,A6,A9 B1,B2,B3,B4,B6,B7,B8,B9,B17,B19 C4,C6,C7,C9,C11 D2,D14,D16 E1,E2,E3,E4,E5,E9,E10 F1,F2,F3,F4,F5,F6,F10 G1,G2,G3,G7,G10,G11,G12,G13,G14 H7,H8,H9,H10,H11,H12,H13,H14,H15 J3,J4,J5,J8,J9,J10,J11,J12,J13,J14 K1,K2,K3,K4,K5,K7,K8,K9,K10,K11,K12,K13,K14,K15 L1,L2,L3,L4,L5,L7,L8,L9,L10,L11,L12,L13,L14 M2,M7,M8,M9,M10,M11,M12,M13,M14,M15,M16 N2,N7,N8,N9,N10,N11,N12,N13,N14 P3,P8,P9,P10,P11,P12,P13,P14 R9,R10,R11,R12,R13,R14,R15 T14,V4,V6,V8,V10,V13,V15,V17,W19,Y2	Internal Core Ground Digital IO Ground
CODEC_AVSS	E15	Analog Codec Ground
PLL_AVDD_1V8	N6	PLL IO Power
PLL_AVDD_1V0	M6	General PLL Analog Power
CORE_VDD	G8,G9,J15,G15,N15,L15,J7,R7	ARM Core Power
PMU_DVDD_1V0	R6	PMU IO Domain(PowerDomain) Power
PMUIO_VDD	R8	PMU IO Power
APIO1_VDD	H16	APIO1 PowerDomain Power
APIO2_VDD	T16	APIO2 PowerDomain Power
APIO3_VDD	F14	APIO3 PowerDomain Power
APIO5_VDD	P16	APIO5 PowerDomain Power
APIO6_VDD	K16	APIO6 PowerDomain Power
DDR_VDD	A5,A10,B5,B10,C2,C3,C5,C8,D3,D6,D7,D8,E6,E7,G5,J6,H6,G6,E10,F7,F8,F9,H2,H3,H4	DDR PHY Power
USB_VDD_1V0	T12	USB OTG2.0/Host2.0 Digital Power
USB_AVDD_1V8	T10	USB OTG2.0/Host2.0 Analog Power
USB_AVDD_3V3	T11	USB OTG2.0/Host2.0 Analog Power
MIPI_CSI_AVDD_1V0	U13	MIPI_CSI PHY Analog Power
APO_VDD_1V0	V7	APO 1.0V Power
APO_VDD_1V8	U8	APO 1.8V Power
APO_VDD_3V3	U9	APO 3.3V Power
HDMI_AVDD_1V8	V3	HDMI PHY Analog Power
HDMI_AVDD_1V0	V5	HDMI PHY Analog Power
SADC_AVDD_1V8	B11	SADC Analog Power
CODEC_AVDD_1V8	D15	Audio Codec Analog Power
VDAC_AVDD_1V8	U7	VDAC Analog Power

2.7 RV1107 Function IO description

Table 2-3 RV1107 function IO description

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type ①	Def②	Pull	Drive Strength③	INT④	DIE Power domain
T7	GPIO0_A1/SDMMC0_DET	GPIO0_A1	SDMMC0_DET			I/O	I	up	4	√	PMUIO IO Voltage 3.3V
U1	GPIO0_A2/SDMMC1_PWR	GPIO0_A2	SDMMC1_PWR			I/O	I	down	4	√	
P4	GPIO0_A3/SPI_CLK	GPIO0_A3	SPI_CLK			I/O	I	down	4	√	
P5	GPIO0_A4/SPI_CSN0	GPIO0_A4	SPI_CSN0			I/O	I	down	4	√	
V2	GPIO0_A5/CLK_WIFI_OUT	GPIO0_A5	CLK_WIFI_OUT			I/O	I	up	4	√	
V1	GPIO0_A6/PMU_DEBUG0	GPIO0_A6	PMU_DEBUG0			I/O	I	down	4	√	
M3	GPIO0_A7/SPI_TXD	GPIO0_A7	SPI_TXD			I/O	I	down	4	√	
U5	GPIO0_B0/SPI_RXD	GPIO0_B0	SPI_RXD			I/O	I	down	4	√	
T4	GPIO0_B1/I2C0_SCL	GPIO0_B1	I2C0_SCL			I/O	I	up	4	√	
R4	GPIO0_B2/I2C0_SDA	GPIO0_B2	I2C0_SDA			I/O	I	up	4	√	
R2	GPIO0_B3	GPIO0_B3				I/O	I	up	4	√	
T5	GPIO0_B4	GPIO0_B4				I/O	I	up	4	√	
N5	GPIO0_B5/PMIC_SLEEP	GPIO0_B5	PMIC_SLEEP			I/O	I	down	4	√	
N1	GPIO0_B6/I2C3_SCL	GPIO0_B6	I2C3_SCL			I/O	I	up	4	√	
M5	GPIO0_B7/TSADC_SHUT	GPIO0_B7	TSADC_SHUT			I/O	I	up	4	√	
M4	GPIO0_C0/PWM3/IR	GPIO0_C0	PWM3	IR		I/O	I	down	4	√	
U3	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN	GPIO0_C1	HDMI_HPD1	CVBS_CLK_IN		I/O	I	down	4	√	
U2	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	GPIO0_C2	I2C4_SDA	PMU_DEBUG1		I/O	I	down	4	√	
P6	GPIO0_C3/PMU_DEBUG2	GPIO0_C3	PMU_DEBUG2			I/O	I	down	4	√	
T3	GPIO0_C4/PWM1/I2C3_SDA	GPIO0_C4	PWM1	I2C3_SDA		I/O	I	up	4	√	
T2	GPIO0_C5/PWM0/PMU_DEBUG3	GPIO0_C5	PWM0	PMU_DEBUG3		I/O	I	down	4	√	
R3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	GPIO0_C6	PWM2	I2C4_SCL	PMU_DEBUG4	I/O	I	down	4	√	
Y9	GPIO1_A0	GPIO1_A0		MIPI_CLKP		A		NA		√	APO
W9	GPIO1_A1	GPIO1_A1		MIPI_CLKN		A		NA		√	
W11	GPIO1_A2	GPIO1_A2		MIPI_D0P		A		NA		√	
Y11	GPIO1_A3	GPIO1_A3		MIPI_D0N		A		NA		√	
W10	GPIO1_A4	GPIO1_A4		MIPI_D1P		A		NA		√	
Y10	GPIO1_A5	GPIO1_A5		MIPI_D1N		A		NA		√	
Y8	GPIO1_A6	GPIO1_A6		MIPI_D2P		A		NA		√	
W8	GPIO1_A7/PWM5	GPIO1_A7		MIPI_D2N	PWM5	A		NA		√	
Y7	GPIO1_B0/PWM6	GPIO1_B0		MIPI_D3P	PWM6	A		NA		√	
W7	GPIO1_B1/PWM7	GPIO1_B1		MIPI_D3N	PWM7	A		NA		√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type ①	Def ②	Pull	Drive Strength ③	INT④	DIE Power domain
F17	GPIO1_B2/I2S_SDO/GMAC_TXD0	GPIO1_B2		I2S_SDO	GMAC_TXD0	I/O	I	down	8	√	
B20	GPIO1_B3/I2S_SCLK/GMAC_TXD1	GPIO1_B3		I2S_SCLK	GMAC_TXD1	I/O	I	down	8	√	
C19	GPIO1_B4/I2S_MCLK/GMAC_TXEN	GPIO1_B4		I2S_MCLK	GMAC_TXEN	I/O	I	down	8	√	
F18	GPIO1_B5/I2S_SDIO1/GMAC_RXD0	GPIO1_B5		I2S_SDIO1	GMAC_RXD0	I/O	I	down	8	√	
C20	GPIO1_B6/I2S_LRCLKTX/GMAC_RXD1	GPIO1_B6		I2S_LRCLKTX	GMAC_RXD1	I/O	I	down	8	√	
G16	GPIO1_B7/I2S_SDIO2/GMAC_RXDV	GPIO1_B7		I2S_SDIO2	GMAC_RXDV	I/O	I	down	8	√	
E18	GPIO1_C0/I2S_LRCLKRX	GPIO1_C0		I2S_LRCLKRX		I/O	I	down	8	√	
E19	GPIO1_C1/PWM4	GPIO1_C1		I2S_SDI	PWM4	I/O	I	down	8	√	
D20	GPIO1_C2/I2S_SDIO3/GMAC_RXER	GPIO1_C2		I2S_SDIO3	GMAC_RXER	I/O	I	down	8	√	
E20	GPIO1_C3/ GMAC_MDIO	GPIO1_C3		GMAC_MDIO		I/O	I	down	8	√	APIO1 IO Voltage 3.3V/1.8V
F19	GPIO1_C4/GMAC_MDC	GPIO1_C4		GMAC_MDC		I/O	I	down	8	√	
G17	GPIO1_C5 /GMAC_CLK	GPIO1_C5		GMAC_CLK		I/O	I	down	8	√	
A18	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	GPIO1_D0	UART1_CTSN	SPI_CLK	DSP_TCK	I/O	I	down	4	√	
A19	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	GPIO1_D1	UART1_RTSN	SPI_CSN0	DSP_TMS	I/O	I	up	4	√	
D19	GPIO1_D2/UART1_RX/SPI_RXD	GPIO1_D2	UART1_RX	SPI_RXD		I/O	I	up	4	√	
B18	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	GPIO1_D3	UART1_TX	SPI_TXD	DSP_TDO	I/O	I	down	4	√	
E17	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	5VGPIO1_D4	UART2_CTSN	HDMI_I2C0_SCL		I/O	I	up	4	√	
C17	5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	5VGPIO1_D5	UART2_RTSN	HDMI_I2C0_SDA		I/O	I	up	4	√	
C18	5VGPIO1_D6/HDMI_HPD0	5VGPIO1_D6	HDMI_HPD0			I/O	I	down	4	√	
A20	GPIO1_D7/HDMI_CEC/DSP_RTCK	GPIO1_D7	HDMI_CEC	DSP_RTCK		I/O	I	up	4	√	
F16	GPIO2_D1/UART2_RX/JTAG_TMS	GPIO2_D1	UART2_RX	JTAG_TMS		I/O	I	up	4	√	
E16	GPIO2_D2/UART2_TX/JTAG_TCK	GPIO2_D2	UART2_TX	JTAG_TCK		I/O	I	up	4	√	
T19	GPIO2_D3/I2C1_SDA	GPIO2_D3	I2C1_SDA			I/O	I	up	4	√	
R17	GPIO2_D4/I2C1_SCL	GPIO2_D4	I2C1_SCL			I/O	I	up	4	√	APIO2 IO Vlotage 3.3V/1.8V
M19	GPIO2_D5/SDIO_CLKO	GPIO2_D5	SDIO_CLKO			I/O	I	down	4	√	
L20	GPIO2_D6/SDIO_CMD	GPIO2_D6	SDIO_CMD			I/O	I	up	8	√	
L19	GPIO2_D7/SDIO_D0	GPIO2_D7	SDIO_D0			I/O	I	up	8	√	
M18	GPIO3_A0/SDIO_D1	GPIO3_A0	SDIO_D1			I/O	I	up	8	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type ①	Def②	Pull	Drive Strength③	INT④	DIE Power domain
M20	GPIO3_A1/SDIO_D2	GPIO3_A1	SDIO_D2			I/O	I	up	8	√	
M17	GPIO3_A2/SDIO_D3	GPIO3_A2	SDIO_D3			I/O	I	up	8	√	
R20	GPIO3_A3/UART0_RTSN	GPIO3_A3	UART0_RTSN			I/O	I	up	4	√	
P18	GPIO3_A4/UART0_CTSN	GPIO3_A4	UART0_CTSN			I/O	I	up	4	√	
T20	GPIO3_A5/UART0_RX	GPIO3_A5	UART0_RX			I/O	I	up	4	√	
P17	GPIO3_A6/UART0_TX	GPIO3_A6	UART0_TX			I/O	I	up	4	√	
P19	GPIO3_A7	GPIO3_A7				I/O	I	down	4	√	
U20	GPIO3_B0	GPIO3_B0				I/O	I	down	4	√	
N16	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT	GPIO3_B1	PCM_OUT	FLASH_TRIG_OUT		I/O	I	down	4	√	
N18	GPIO3_B2/PCM_IN/FLASH_TRIG_IN	GPIO3_B2	PCM_IN	FLASH_TRIG_IN		I/O	I	down	4	√	
R19	GPIO3_B3/PCM_CLK	GPIO3_B3	PCM_CLK			I/O	I	down	4	√	
N20	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	GPIO3_B4	PCM_SYNC	PRELIGHT_TRIG_OUT		I/O	I	down	4	√	
P20	GPIO3_B5/MIPI_CSI_MCLK	GPIO3_B5	MIPI_CSI_MCLK			I/O	I	down	4	√	
N19	GPIO3_B6	GPIO3_B6				I/O	I	down	4	√	
D11	GPIO3_B7/SDMMC0_PWR	GPIO3_B7	SDMMC0_PWR			I/O	I	up	8	√	APIO3 IO Voltage 3.3V/1.8V
C12	GPIO3_C0/SDMMC0_D3	GPIO3_C0	SDMMC0_D3			I/O	I	up	8	√	
D12	GPIO3_C1/SDMMC0_D2	GPIO3_C1	SDMMC0_D2	UART2_RX		I/O	I	up	8	√	
A12	GPIO3_C2/SDMMC0_D1/UART2_RX	GPIO3_C2	SDMMC0_D1	UART2_TX		I/O	I	up	8	√	
B12	GPIO3_C3/SDMMC0_D0/UART2_TX	GPIO3_C3	SDMMC0_D0			I/O	I	down	8	√	
B13	GPIO3_C4/SDMMC0_CLKO	GPIO3_C4	SDMMC0_CLKO			I/O	I	up	8	√	
A13	GPIO3_C5/SDMMC0_CMD	GPIO3_C5	SDMMC0_CMD			I/O	I	down	4	√	
V20	GPIO1_C6/CIF_D4/I2S_LRCLKTX	GPIO1_C6	CIF_D4	I2S_LRCLKTX		I/O	I	down	8	√	APIO5 IO Voltage 3.3V/1.8V
U19	GPIO1_C7/CIF_D5/I2S_SDIO2	GPIO1_C7	CIF_D5	I2S_SDIO2		I/O	I	down	8	√	
Y19	GPIO2_C0/CIF_D6/I2S_LRCLKRX	GPIO2_C0	CIF_D6	I2S_LRCLKRX		I/O	I	down	8	√	
U14	GPIO2_C1/CIF_D7/I2S_SDI	GPIO2_C1	CIF_D7	I2S_SDI		I/O	I	down	8	√	
V16	GPIO2_C3/CIF_D0/I2S_SDO	GPIO2_C3	CIF_D0	I2S_SDO		I/O	I	down	8	√	
U16	GPIO2_C4/CIF_D1/I2S_SCLK	GPIO2_C4	CIF_D1	I2S_SCLK		I/O	I	down	8	√	
U15	GPIO2_C5/CIF_D2/I2S_MCLK	GPIO2_C5	CIF_D2	I2S_MCLK		I/O	I	down	8	√	
V14	GPIO2_C6/CIF_D3/I2S_SDIO1	GPIO2_C6	CIF_D3	I2S_SDIO1		I/O	I	down	8	√	
V19	GPIO3_C6/CIF_VSYNC	GPIO3_C6	CIF_VSYNC			I/O	I	down	8	√	
T18	GPIO3_C7/CIF_CLKIN	GPIO3_C7	CIF_CLKIN			I/O	I	down	8	√	
U18	GPIO3_D0/CIF_HREF	GPIO3_D0	CIF_HREF			I/O	I	down	8	√	
T17	GPIO3_D1/CIF_PDN	GPIO3_D1	TCIF_PDN			I/O	I	down	8	√	
V18	GPIO3_D2/CIF_CLKOUT	GPIO3_D2	CIF_CLKOUT			I/O	I	down	8	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type ①	Def②	Pull	Drive Strength③	INT④	DIE Power domain
Y20	GPIO3_D3/CIF_D8/I2S_SDIO3	GPIO3_D3	CIF_D8	I2S_SDIO3		I/O	I	down	8	√	
U17	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	GPIO3_D4	CIF_D9	FLASH_TRIG_IN		I/O	I	down	8	√	
R16	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	GPIO3_D5	CIF_D10	FLASH_TRIG_OUT		I/O	I	down	8	√	
W20	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	GPIO3_D6	CIF_D11	PRELIGHT_TRIG_OUT		I/O	I	down	8	√	
K18	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	GPIO2_A0	FLASH_D0	EMMC_D0	SFC_SIO_IO0	I/O	I	up	8	√	
J16	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1	GPIO2_A1	FLASH_D1	EMMC_D1	SFC_SIO_IO1	I/O	I	up	8	√	
K17	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	GPIO2_A2	FLASH_D2	EMMC_D2	SFC_WP_IO2	I/O	I	up	8	√	
H19	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	GPIO2_A3	FLASH_D3	EMMC_D3	SFC_HOLD_IO3	I/O	I	up	8	√	
G20	GPIO2_A4/FLASH_D4/EMMC_D4	GPIO2_A4	FLASH_D4	EMMC_D4		I/O	I	up	8	√	
J19	GPIO2_A5/FLASH_D5/EMMC_D5	GPIO2_A5	FLASH_D5	EMMC_D5		I/O	I	up	8	√	
L16	GPIO2_A6/FLASH_D6/EMMC_D6	GPIO2_A6	FLASH_D6	EMMC_D6		I/O	I	up	8	√	APIO6
H20	GPIO2_A7/FLASH_D7/EMMC_D7	GPIO2_A7	FLASH_D7	EMMC_D7		I/O	I	up	8	√	IO Voltage
H18	GPIO2_B0/FLASH_ALE	GPIO2_B0	FLASH_ALE			I/O	I	down	8	√	3.3V/1.8V
F20	GPIO2_B1/FLASH_CLE	GPIO2_B1	FLASH_CLE			I/O	I	down	8	√	
K19	GPIO2_B2/FLASH_WRN	GPIO2_B2	FLASH_WRN			I/O	I	up	8	√	
L17	GPIO2_B3/FLASH_RDN	GPIO2_B3	FLASH_RDN			I/O	I	up	8	√	
G19	GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	GPIO2_B4	FLASH_RDY	EMMC_CMD	SFC_CSN0	I/O	I	up	8	√	
J20	GPIO2_B5/FLASH_CSN0	GPIO2_B5	FLASH_CSN0			I/O	I	up	8	√	
K20	GPIO2_B6/EMMC_CLKO	GPIO2_B6	EMMC_CLKO			I/O	I	down	8	√	
J18	GPIO2_B7/FLASH_CSN1/SFC_CLK	GPIO2_B7	FLASH_CSN1	SFC_CLK		I/O	I	up	8	√	
H17	GPIO2_C2/FLASH_WP/EMMC_PWR	GPIO2_C2	FLASH_WP	EMMC_PWR		I/O	I	down	8	√	
W14	MIPI_CSI_D0N	MIPI_CSI_D0N				A		NA			
Y14	MIPI_CSI_D0P	MIPI_CSI_D0P				A		NA			
W15	MIPI_CSI_D1N	MIPI_CSI_D1N				A		NA			
Y15	MIPI_CSI_D1P	MIPI_CSI_D1P				A		NA			
W17	MIPI_CSI_D2N	MIPI_CSI_D2N				A		NA			
Y17	MIPI_CSI_D2P	MIPI_CSI_D2P				A		NA			MIPI_CSI
Y18	MIPI_CSI_D3N	MIPI_CSI_D3N				A		NA			
W18	MIPI_CSI_D3P	MIPI_CSI_D3P				A		NA			
W16	MIPI_CSI_CLKP	MIPI_CSI_CLKP				A		NA			
Y16	MIPI_CSI_CLKN	MIPI_CSI_CLKN				A		NA			
U12	MIPI_CSI_EXTR	MIPI_CSI_EXTR				A		NA			
P7	TEST	TEST				I		down			PMUIO
T1	NPOR	NPOR				I		up			3.3V

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type ①	Def②	Pull	Drive Strength③	INT④	DIE Power domain
P2	XOUT_24M	XOUT_24M				O		NA			PLL_1V0
P1	XIN_24M	XIN_24M				I		NA			
Y1	HDMI_TXCN	HDMI_TXCN				A		NA			HDMI
W1	HDMI_TXCP	HDMI_TXCP				A		NA			
W2	HDMI_TX0N	HDMI_TX0N				A		NA			
W3	HDMI_TX0P	HDMI_TX0P				A		NA			
W4	HDMI_TX1N	HDMI_TX1N				A		NA			
Y4	HDMI_TX1P	HDMI_TX1P				A		NA			
Y5	HDMI_TX2N	HDMI_TX2N				A		NA			
W5	HDMI_TX2P	HDMI_TX2P				A		NA			
U6	HDMI_EXTR	HDMI_EXTR				A		NA			
W13	USB1_DP	USB1_DP				A		NA			USB
Y13	USB1_DM	USB1_DM				A		NA			
U10	USB_EXTR	USB_EXTR				A		NA			
V12	USB_VBUS	USB_VBUS				A		NA			
V11	USB0_ID	USB0_ID				A		NA			
Y12	USB0_DM	USB0_DM				A		NA			
W12	USB0_DP	USB0_DP				A		NA			
A17	CODEC_MICBIAS	CODEC_MICBIAS				A		NA			Audio Codec
C15	CODEC_MICL	CODEC_MICL				A		NA			
B15	CODEC_MICR	CODEC_MICR				A		NA			
B16	CODEC_VCM	CODEC_VCM				A		NA			
A15	CODEC_AOL	CODEC_AOL				A		NA			
A16	CODEC_AOR	CODEC_AOR				A		NA			
W6	VDAC_EXTR	VDAC_EXTR				P		NA			VDAC_AVDD
Y6	VDAC_OUT	VDAC_OUT				A		NA			
D13	ADC_IN0	ADC_IN0				A		NA			SAR_AVDD_18
E13	ADC_IN1	ADC_IN1				A		NA			
E12	ADC_IN2	ADC_IN2				A		NA			
D10	ADC_IN3	ADC_IN3				A		NA			
F12	ADC_IN4	ADC_IN4				A		NA			
E11	ADC_IN5	ADC_IN5				A		NA			
N3	EFUSE	EFUSE				P		NA			EFUSE
E4	PZQ	PZQ				A		NA			
F6	VREF	VREF				A		NA			
J6	DDR_VDD_1	DDR_VDD_1				A		NA			
H6	DDR_VDD_2	DDR_VDD_2				A		NA			
G6	DDR_VDD_3	DDR_VDD_3				A		NA			
E10	DDR_VDD_4	DDR_VDD_4				A		NA			
F7	DDR_VDD_5	DDR_VDD_5				A		NA			
F8	DDR_VDD_6	DDR_VDD_6				A		NA			
F9	DDR_VDD_7	DDR_VDD_7				A		NA			

Notes:

①:Type: I = input, O = output, I/O = input/output (bidirectional)

   AP = Analog Power, AG = Analog Ground

   DP = Digital Power, DG = Digital Ground

   A = Analog

②:Output Drive Unit is mA, only Digital IO has drive value;

③:Def: I = input without any pull resistor, O = output without any pull resistor;

④:INT: interrupt

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

2.8.1 MISC

Interface	Pin Name	Direction	Description
Misc	XIN_24M	I	Clock input of 24MHz crystal
	XOUT_24M	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset

2.8.2 JTAG

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_TMS	I/O	JTAG interface TMS input/SWD interface data out
	JTAG_TCK	I	JTAG interface clock input/SWD interface clock input

2.8.3 SDMMC

Interface	Pin Name	Direction	Description
SDMMC Host Controller	SDMMC0_Di(i=0~3)	I/O	sdmmc card data input and output
	SDMMC0_CLKO	O	sdmmc card clock
	SDMMC0_CMD	I/O	sdmmc card command output and response input
	SDMMC0_DET	I	sdmmc card detect signal, 0 represents presence of card

2.8.4 SDIO

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDIO_CLKO	O	sdio clock
	SDIO_CMD	I/O	sdio command output and response input
	SDIO_DATAi(i=0~3)		sdio data input and output

2.8.5 EMMC

Interface	Pin Name	Direction	Description
EMMC Interface	EMMC_CLKO	O	emmc card clock
	EMMC_CMD	I/O	emmc card command output and response input
	EMMC_DATAi(i=0~7)	I/O	emmc card data input and output

2.8.6 DDR3

Interface	Pin Name	Direction	Description
DMC	DDR_CLK	O	Active-high clock signal to the memory device.

Interface	Pin Name	Direction	Description
	DDR_CLKn	O	Active-low clock signal to the memory device.
	DDR_CKE	O	Active-high clock enable signal to the memory device
	DDR_CSN	O	Active-low chip select signal to the memory device. There are two chip select.
	DDR_RASN	O	Active-low row address strobe to the memory device.
	DDR_CASN	O	Active-low column address strobe to the memory device.
	DDR_WEN	O	Active-low write enable strobe to the memory device.
	DDR_RESET	O	DDR3 reset signal to the memory device
	DDR_Bai(i=0,1,2)	O	Bank address signal to the memory device.
	DDR_Ai(i=0~14)	O	Address signal to the memory device.
	DDR_ODT0	O	On-Die Termination output signal for two chip select.
	DDR_Dmi(i=0,1)	O	Active-low data mask signal to the memory device.
	DDR_DQS0/1	I/O	Active-high bidirectional data strobes to the memory device.
	DDR_DQS0n/1n	I/O	Active-low bidirectional data strobes to the memory device.
	DDR_Dqi(i=0~15)	I/O	Bidirectional data line to the memory device.

2.8.7 NAND FLASH

Interface	Pin Name	Direction	Description
	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRN	O	Flash write enable and clock signal
NAND	FLASH_RDN	O	Flash read enable and write/read signal
	FLASH_RDY	I	Flash ready/busy signal
	FLASH_Csi(i=0,1)	O	Flash chip enable signal for chip
	FLASH_WP	O	Flash write-protected signal
	FLASH_DATAi(i=0~7)	I/O	Flash data inputs/outputs signal

2.8.8 SPI FLASH

Interface	Pin Name	Direction	Description
	SFC_SIO_IO0	I/O	Data Input Output 0
	SFC_SIO_IO1	I/O	Data Input Output 1
SPI Flash	SFC_WP_IO2	I/O	Write Protect Output (Data Input Output 2)
	SFC_HOLD_IO3	I/O	Hold t Input (Data Input Output 3)
	SFC_CSN0	O	Chip Select
	SFC_CLK	O	Serial Clock Output

2.8.9 PCM

Interface	Pin Name	Direction	Description
PCM	PCM_OUT	O	PCM serial data output
	PCM_IN	I	PCM serial data input
	PCM_CLK	O	PCM clock source
	PCM_SYNC	I/O	PCM serial data synchronous

2.8.10 I2S

Interface	Pin Name	Direction	Description
I2S Controller	I2S_SCLK	I/O	I2S serial clock
	I2S_MCLK	O	I2S clock source
	I2S_LRCLKTX	I/O	I2S left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode
	I2S_SDIOi(i=0~3)	O	I2S serial data output
	I2S_LRCLKRX	I/O	I2S left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode
	I2S_SDI	I/O	I2S serial data input

2.8.11 SPI

Interface	Pin Name	Direction	Description
SPI Controller	SPI_CLK	I/O	SPI serial clock
	SPI_CSN0	I/O	SPI chip select signal ,low active
	SPI_TXD	O	SPI serial data output
	SPI_RXD	I	SPI serial data input

2.8.12 PWM

Interface	Pin Name	Direction	Description
PWM	PWM0	O	Pulse Width Modulation output
	PWM1	O	Pulse Width Modulation output
	PWM2	O	Pulse Width Modulation output
	PWM3	O	Pulse Width Modulation output
	PWM4	O	Pulse Width Modulation output
	PWM5	O	Pulse Width Modulation output
	PWM6	O	Pulse Width Modulation output
	PWM7	O	Pulse Width Modulation output

2.8.13 I2C

Interface	Pin Name	Direction	Description
I2C	I2C0_SDA	I/O	I2C0 data
	I2C0_SCL	I/O	I2C0 clock
	I2C1_SDA	I/O	I2C1 data
	I2C1_SCL	I/O	I2C1 clock
	I2C2_SDA	I/O	I2C2 data
	I2C2_SCL	I/O	I2C2 clock
	I2C3_SDA	I/O	I2C3_data
	I2C3_SCL	I/O	I2C3 clock

2.8.14 UART

Interface	Pin Name	Direction	Description
UART	UART1_CTSN	I	UART1 clear to send
	UART1_RTSN	O	UART1 request to send
	UART1_RX	I	UART1 serial data input
	UART1_TX	O	UART1 serial data output
	UART2_CTSN	I	UART2 clear to send
	UART2_RTSN	O	UART2 request to send
	UART2_RX	I	UART2 serial data input
	UART2_TX	O	UART2 serial data output
	UART0_CTSN	I	UART0 clear to send
	UART0_RTSN	O	UART0 request to send
	UART0_RTX	I	UART0 serial data input
	UART0_TX	O	UART0 serial data output

2.8.15 GMAC

Interface	Pin Name	Direction	Description
GMAC	GMAC_TXDi(i=0~1)	O	GMAC TX data
	GMAC_RXDi(i=0~1)	I	GMAC RX data
	GMAC_TXEN	O	GMAC TX data enable
	GMAC_RXDV	I	Collision and Data Valid
	GMAC_RXER	I	GMAC RX error signal
	GMAC_MDIO	I/O	GMAC management interface data
	GMAC_MDC	O	GMAC management interface clock
	GMAC_CLK	I/O	RMII REC_CLK output or GMAC external clock input

2.8.16 USB

Interface	Pin Name	Direction	Description
USB OTG 2.0	USB0_DM	I/O	USB OTG 2.0 Data signal DM
	USB0_DP	I/O	USB OTG 2.0 Data signal DP

Interface	Pin Name	Direction	Description
USB HOST 2.0	USB1_DP	I/O	USB HOST 2.0 Data signal DP
	USB1_DM	I/O	USB HOST 2.0 Data signal DM

2.8.17 EFUSE

Interface	Pin Name	Direction	Description
EFUSE	EFUSE	N/A	eFuse program and sense power

2.8.18 HDMI

Interface	Pin Name	Direction	Description
HDMI	HDMI_TX0N	O	TMDS channel 0 negative data line
	HDMI_TX0P	O	TMDS channel 0 positive data line
	HDMI_TX1N	O	TMDS channel 1 negative data line
	HDMI_TX1P	O	TMDS channel 1 positive data line
	HDMI_TX2N	O	TMDS channel 2 negative data line
	HDMI_TX2P	O	TMDS channel 2 positive data line

Interface	Pin Name	Direction	Description
	HDMI_EXTR	O	Connect 2.0Kohm resistor to ground to generate reference current
	HDMI_HPD0	I/O	HDMI hot plug detect signal
	HDMI_CEC	I/O	HDMI CEC signal

2.8.19 CODEC

Interface	Pin Name	Direction	Description
CODEC	CODEC_MICL	I	Left channel input
	CODEC_MICR	I	Right channel input
	CODEC_VCM	I	Reference voltage input
	CODEC_AOL	O	Left channel output
	CODEC_AOR	O	Right channel output

2.8.20 CVBSOUT

Interface	Pin Name	Direction	Description
CVBSOUT	VDAC_EXTR	I	Connect external resistor to generate current reference
	VDAC_OUT	O	Data signal output

2.8.21 SAR-ADC

Interface	Pin Name	Direction	Description
SAR-ADC	ADC_Ini($i=0\sim5$)	I	Analog input

2.8.22 ADC

Interface	Pin Name	Direction	Description
ADC	ADC_Ini($i=0\sim5$)	I	Analog input

2.8.23 CIF

Interface	Pin Name	Direction	Description
Camera IF	CIF_Di($i=0\sim11$)	I	Camera interface input pixel data
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_CLKIN	I	Camera interface input pixel clock
	CIF_HREF	I	Camera interface horizontial sync signal
	CIF_PDN	O	Camera power down control output
	CIF_CLKOUT	O	Camera interface output work clock

2.8.24 MIPI
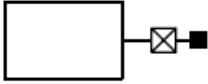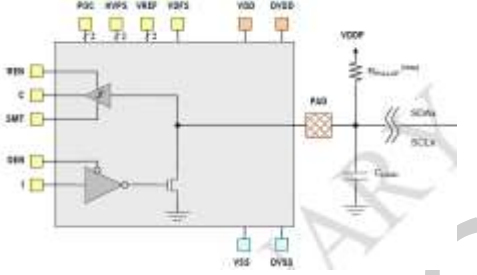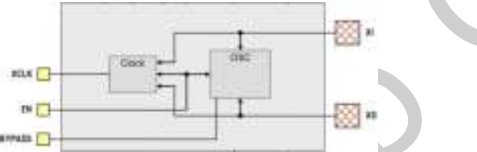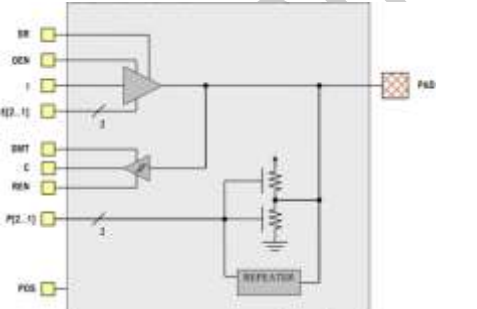
Interface	Pin Name	Direction	Description
MIPI_CSI	MIPI_CSI_DiN(i=0~3)	I/O	MIPI CSI negative differential data line transceiver output
	MIPI_CSI_DiP(i=0~3)	I/O	MIPI CSI positive differential data line transceiver output

Interface	Pin Name	Direction	Description
	MIPI_CSI_CLKP	I/O	MIPI CSI positive differential clock line transceiver output
	MIPI_CSI_CLKN	I/O	MIPI CSI negative differential clock line transceiver output
	MIPI_CSI_EXTR	I/O	MIPI CSI external resistor connection. Recommend to use a 2 KΩ E96 resistor.

2.9 RV1107 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-4 RV1107 IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Pad for 5V tolerance	hdmi_ddcscl hdmi_ddcsda hdmi_hpd
C		Crystal Oscillator with high enable	XIN24M/XOUT24M
D		Tri-state output pad with input, which pull-up/pull-down, slew rate and drive strength is configurable	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RV1107 absolute maximum ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	CORE_VDD PMU_VDD	1.4	V
DC supply voltage for Digital GPIO	APIO1_VDD APIO2_VDD APIO3_VDD PMUIO_VDD APIO5_VDD APIO6_VDD	3.6	V
DC supply voltage for DDR IO	DDR_VDD	1.65	V
DC supply voltage for digital part of PLL	PLL_AVDD_1V0	1.1	V
DC supply voltage for Analog part of PLL	PLL_AVDD_1V8	1.98	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD_1V0 USB_AVDD_1V8 USB_AVDD_3V3	1.1 1.98 3.63	V
DC supply voltage for Analog part of Audio Codec	CODEC_AVDD_1V8	1.98	V
DC supply voltage for Analog part of VDAC	VDAC_AVDD_1V8	1.98	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD_1V0 HDMI_AVDD_1V8	1.1 1.98	V
DC supply voltage for Analog part of SARADC and TSADC	SADC_AVDD_1V8	1.98	V
DC supply voltage for Analog part of DSI	APO_VDD_1V0 APO_VDD_1V8 APO_VDD_3V3	1.1 1.8	V
DC supply voltage for Analog part of CSI	MIPI_CSI_AVDD_1V0	1.1	V
DC supply voltage for Digital part of VIDEOADC	VIDEO_AVDD_1V0	1.1	V
DC supply voltage for Analog part of EFUSE	EFUSE	1.65	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIsO		3.6	V
Storage Temperature	Tstg	125	℃
Max Conjunction Temperature	Tj	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 RV1107 recommended operating condition

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power	CORE_VDD PMU_VDD	0.9	1.0	TBD	V
Digital GPIO Power(3.3V/2.5V/1.8V)	APIO1_VDD APIO2_VDD APIO3_VDD PMUIO_VDD APIO5_VDD APIO6_VDD	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V
DDR IO (DDR3 mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (DDR3L mode) Power	DDR_VDD	1.283	1.35	1.417	V
PLL Digital Power	PLL_AVDD_1V0	0.9	1.0	1.1	V
PLL Analog Power	PLL_AVDD_1V8	1.62	1.8	1.98	V
ACODEC Analog Power	CODEC_AVDD_1V8	1.62	1.8	1.98	V
VDAC Analog Power	VDAC_AVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Digital Power	USB_AVDD_1V0	0.9	1.0	1.1	V
USB OTG/Host2.0 Analog Power(1.8V)	USB_AVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD_3V3	3.069	3.3	3.63	V
HDMI Analog Power(1.0V)	HDMI_AVDD_1V0	0.9	1.0	1.1	V
HDMI Analog Power(1.8V)	HDMI_AVDD_1V8	1.62	1.8	1.98	V
SARADC Analog Power(1.8V)	SADC_AVDD_1V8	1.62	1.8	1.98	V
TSADC Analog Power(1.8V)	SADC_AVDD_1V8	1.62	1.8	1.98	V
MIPI CSI Analog Power(1.0V)	MIPI_CSI_AVDD_1V0	0.9	1.0	1.1	V
VIDEOADC Analog Power(1.0V)	VIDEO_AVDD_1V0	0.9	1.0	1.1	V
PLL input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature ②		-20	25	80	℃

Notes:

① Symbol name is same as the pin name in the io descriptions

3.3 DC Characteristics

Table 3-3 RV1107 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	3.6	V
	Threshold Point	Vtr+	1.53	1.46	1.43	V
		Vtr-	1.19	1.12	1.05	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	1.8+0.3	V
	Threshold Point	Vtr+	1.23	1.12	1.03	V
		Vtr-	0.91	0.82	0.73	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDD+0.4	V
	Input Low Voltage	Vil_ddr	-0.4	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	0.9xDDR_VDD	NA	N/A	V
	Output Low Voltage	Vol_ddr	N/A	NA	0.1*DDR_VDD	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	100 54 36	120 60 40	140 66 44	Ohm
HDMI	Single-ended standby voltage	Voff	avddtmds±10			mV
	Single-ended output swing voltage RT=50Ω	Vswing	400		600	mV
		Vswing_data	400		600	mV
		Vswing_clock	400		600	mV
	Single-ended output high voltage	Vh				mV
			avddtmds-400		avddtmds+10	mV
		Vh_data	avddtmds-400		avddtmds+10	mV
		Vh_clock	avddtmds-400		avddtmds+10	mV
	Single-ended output low voltage	Vl				mV
			avddtmds-1000		avddtmds-400	mV

Parameters		Symbol	Min	Typ	Max	Units
		Vl_data	avddtmds-1000		avddtmds-400	mV
		Vl_clock	avddtmds-1000		avddtmds-400	mV
	Differential source termination load	Rterm	75		150	Ω
MIPI CSI MIPI mode	Common-mode voltage HS receive mode	Vcmrx(dc)	70		300	mV
	Differential input high threshold	Vidth			70	mV
	Differential input low threshold	Vidtl	-70			mV
	Single-ended input high voltage	Vihhs			460	mV
	Single-ended input low voltage	Vilhs	-40			mV
	Single-ended threshold for HS termination enable	Vterm-en			450	mV
	Differential input impedance	Zid	80	100	125	Ω
MIPI CSI LP mode	Logic 1 input voltage	Vih	880			mV
	Logic 0 input voltage, not in ULP state	Vil			550	mV
	Logic 0 input voltage, ULP state	Vil-ulps			300	mV
	Input hysteresis	Vhyst	25			mV
SARADC	Effective Number of Bit	ENOB		9		Bit
	Differential Nonlinearity	DNL	-1		+1	LSB
	Integral Nonlinearity	INL	-2		+2	LSB
	Input Voltage Range	Vin	0		1	AVDD
	Input Capacitance	Cin		10		pF
	Sampling rate	fs			1	MS/s
	Spurious Free Dynamic Range	SFDR		61		dB
	Signal to Noise and Harmonic Ratio	SNDR		56		dB
CODEC	Microphone Bias	Vmicb	0.5 * AVDD		0.85 * AVDD	V
		Imicb			3	mA
	Microphone Gain Boost PGA	Gbst	0		20	dB
		Cin		10		pF
	ALC PGA	Galc	-18		28.5	dB
	ADC	SNR		92		dB
		THD		-81		dB
	DAC Output Driver	Gdrv	-39		6	dB
		Rout		1		Ω
		Cout		20		pF
		PSRR		70		

3.4 Electrical Characteristics for General IO

Table 3-4 RV1107 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 RV1107 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @3.3V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @3.3V/1.1V	10		800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/1.1V	800		3200	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/1.1V	16		3200	MHz
	Lock time	T_{lt}	@ 3.3V/1.1V, FREF=24M,REFDIV=1		250	500	Input clock cycles
	VDDHV current consumption		Fvco = 1000MHz, @3.3V *Current scale as (Fvco/1GHz)$^{1.5}$*		1.0	1.2	mA
	VDD Current consumption		VDD =1.1V		1.3	1.56	uA/MHz
	Power consumption (power-down mode)		PD=HIGH, @27 ℃		13		uA

Notes :
REFDIV is the input divider value;
FBDIV is the feedback divider value;
POSTDIV is the output divider value

3.6 Electrical Characteristics for USB Interface

Table 3-13 RV1107 Electrical Charactestics for USB Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Transmitter						
High input level	VIH		NA	1.0	NA	V
Low input level	VIL		NA	0	NA	V
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	0.3	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		+-250		mV
		HS mode		+-25		mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	VOH		NA	3.3	NA	V
Low output level	VOL		NA	0	NA	V

3.7 Electrical Characteristics for DDR IO

Table 3-6 RV1107 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0		uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	NA	0	NA	nA

3.8 Electrical Characteristics for eFuse

Table 3-7 RV1107 Electrical Characteristics for eFuse

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Active mode	VDD current in Read mode	Iread_vdd	nomal read	15	20	30	mA
	VDD current in PGM mode	Ipgm_vdd	STROBE high	0.5	1	2.5	mA
	VQPS current in PGM mode	Ipgm_vqps	STROBE high	5	10	15	mA
standby mode	VDD current in standby mode	Istandby_vdd	Standby	0.2	0.5	2	A

3.9 Electrical Characteristics for HDMI

Table 3-8 RV1107 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Trise and Tfall				<200		ps
Frequency Tolerance, max				-300 ~300		ppm
Clock duty cycle			40%		60%	
Power consumption		1080p		60		mA
Power consumption		2160p		100		mA

3.10 Electrical Characteristics for VDAC

Table 3-9 RV1107 Electrical Characteristics for VDAC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	VDD		0.9	1.0	1.1	V
Output Resistance	R_{OUT}			50		KΩ
Output Capacitance	C_{OUT}			10		pF
Full Scale Output Current	I_{OUT}		14.7		34.8	mA
Resistance Load	R_L			75		Ω
Clock Frequency	f_{CLK}				300	MHz
Analog Supply Current	I_{AVDD}	I_{OUT}=14.7mA		18		mA
		I_{OUT}=34.8mA		39		mA
		Power Down		10		uA
Digital Supply Current	I_{VDD}	f_{CLK}=100MHz		100		uA

Parameters	Symbol	Test condition	Min	Typ	Max	Units
		Power Down		1		uA

3.11 Electrical Characteristics for TSADC

Table 3-10 RV1107 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Temperature Resolution				5		℃
Temperature Range			-40		125	℃
Analog power	IAVDD	Fs= 50KS/s		190		uA
Digital power	IVDD	Fs= 50KS/s		10		uA
Clock Frequency	Fclk	Fclk			800	KHz
Power Down Current from Analog	IAVDD	Power down		1		uA
Power Down Current from Digital	IVDD	Power down		1		uA

3.12 Electrical Characteristics for MIPI CSI

Table 3-11 RV1107 Electrical Characteristics for MIPI CSI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode voltage HS receive mode	Vcmrx(dc)		70		300	mV
Differential input high threshold	Vidth				70	mV
Differential input low threshold	Vidtl		-70			mV
Single-ended input high voltage	Vihhs				460	mV
Single-ended input low voltage	Vilhs		-40			mV
Single-ended threshold for HS termination enable	Vterm-en				450	mV
Differential input impedance	Zid		80	100	125	Ω
Logic 1 input voltage	Vih		880			mV
Logic 0 input voltage, not in ULP state	Vil				550	mV
Logic 0 input voltage, ULP state	Vil-ulps				300	mV
Input hysteresis	Vhyst		25			mV
Common-mode interference beyond 450 MHz	ΔVcmrx(HF)				100	mV
Common-mode interference 50MHz-450MHz	ΔVcmrx(LF)		-50		50	mV
Common-mode termination	Ccm				60	pF
Input pulse rejection	Espike				300	V.ps
Minimum pulse width response	Tmin-rx		20			ns

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Peak interference amplitude	Vint				200	mV
Interference frequency	Fint		450			MHz

3.13 Electrical Characteristics for SARADC

Table 3-12 RV1107 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	VDD		0.9	1.0	1.1	V
Effective Number of Bit	ENOB			9		Bit
Differential Nonlinearity	DNL		-1		+1	LSB
Integral Nonlinearity	INL		-2		+2	LSB
Input Voltage Range	Vin		0		1	AVDD
Input Capacitance	Cin			10		pF
Sampling rate	fs				1	MS/s
Spurious Free Dynamic Range	SFDR	Fs=1MS/s Fout=1.17KHz		61		dB
Signal to Noise and Harmonic Ratio	SNDR			56		dB
Analog Supply Current	I$_{AVDD}$	Fs=1MS/s		450		uA
		Power Down		1		uA
Digital Supply Current	I$_{VDD}$	Fs=1MS/s		50		uA
		Power Down		1		uA

3.14 Electrical Characteristics for ACODEC

Table 3-13 RV1107 Electrical Characteristics for ACODEC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	DVDD		0.9	1.0	1.1	V
Bias Voltage	V$_{MICB}$		0.5 * AVDD		0.85 * AVDD	V
Bias Voltage	I$_{MICB}$				3	mA
Programmable Gain	G$_{BST}$		0		20	dB
Input Resistance	R$_{IN}$	G$_{BST}$=0dB		110		KΩ
		G$_{BST}$=20dB		20		KΩ
Input Capacitance	C$_{IN}$			10		pF
Programmable Gain	G$_{ALC}$		-18		28.5	dB
Signal to Noise Ratio	SNR	A-weighted		92		dB
Total Harmonic Distortion	THD	-3dBFS input		-81		dB
Programmable Gain	G$_{DRV}$		-39		6	dB

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output Resistance	R$_{OUT}$			1		Ω
Output Capacitance	C$_{OUT}$			20		pF
Power Supply Rejection	PSRR	1KHz		70		dB
Signal to Noise Ration	SNR	A-weighted		93		dB
Total Harmonic Distortion	THD	-3dBFS output 600Ω load		-80		dB

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RV1107 has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on RV1107. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 RV1107 Thermal Resistance Characteristics

Package (BGA359)	Power(W)	$\theta_{JA}(℃/W)$	$\theta_{JB}(℃/W)$	$\theta_{JC}(℃/W)$
RV1107	2.518	15.62	8.78	7.18

Note: The testing PCB is based on 4 layers, 14mmx 14mm, 1.1 mm Thickness, Ambient temperature is 25.3° C.