Integrated Monolithic GPS and GLONASS Receiver IC

GENERAL DESCRIPTION

The Broadcom® BCM4752 is a Global Navigation Satellite System (GNSS) single-die receiver IC, fabricated in low-power 40 nm CMOS technology.

The BCM4752 features a host-based architecture, where processing functions are split between the BCM4752 and the CPU on the host system. Demands on the host CPU are minimal and no real time requirements are imposed. Host communication can be implemented via UART (with optional hardware flow control) or a Broadcom Serial Control (BSC) slave.

The BCM4752 includes an internal low-dropout regulator to power both an external GNSS TCXO and an optional external low noise amplifier. It is available in a 0.4 mm ball pitch, 2.07 mm × 2.47 mm WLBGA package or a 5 mm × 5 mm FBGA package.

APPLICATIONS

- Designed for the fast-growing smartphone segment, where GNSS has become pervasive. The BCM4752 enables both navigation, a feature increasingly demanded by consumers, and location services, which are demanded by emergency services such as E911, network operators, location-aware services, as well as by consumers.
- Optimal for Portable Digital Assistants, Portable Media Players, and Portable Navigation Devices.

FEATURES

- Multi-constellation capability that simultaneously uses signals from four satellite constellations (GPS, GLONASS, QZSS and SBAS) to compute each position fix.
- Industry-breakthrough acquisition engine capability providing approximately 10× greater acquisition capability than the previous generation, resulting in unprecedented acquisition and re-acquisition performance in a variety of common user scenarios.
- Very low current consumption. As little as 8 mA average current in low power mode, which is made possible by a new and flexible internal signal processing architecture.
- The industry's smallest GNSS chip that features a low Bill of Materials (BOM) part count, which enables a very small PCB size of 16 mm^2, including external filter and TCXO.
- Proven firmware package with multiple advanced features:
  - Multi-Constellation Assistance Data — always maintains fresh multi-constellation assistance data thanks to Broadcom's Location Based Services (LBS) client/server solution.
  - Urban Navigation aided by sensors — provides industry leading urban navigation performance, due to the seamless integration of data from inertial and absolute sensors in the position engine.
  - Pedestrian Indoor Navigation aided by sensors and WLAN — provides an industry unique indoor pedestrian navigation capability, integrating sensor data and WLAN scans in the BCM4752 position engine.

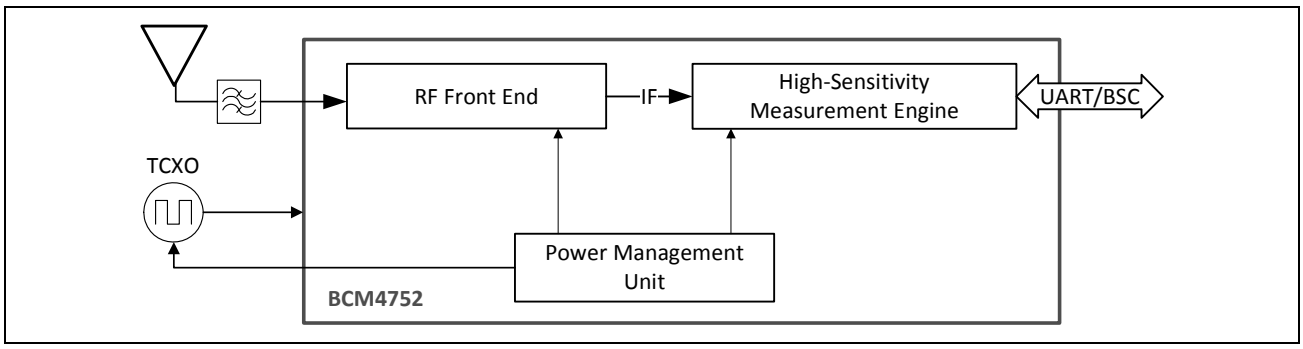

Figure 1: BCM4752 Top-Level Diagram

Revision History

Revision	*Date*	*Change Description*
4752-DS103-R	09/26/12	**Updated:** • The cover page to include the FBGA package. • Figure 5: "BCM4752 Power Management Unit," on page 14. • Table 11: "BCM4752 Pinouts," on page 29. • Table 16: "DC Characteristics—Current," on page 37. • Figure 18: "BCM4752 WLBGA Ballout Array (Top View)," on page 33. • Table 18: "Ordering Information," on page 42. **Added:** • Figure 19: "BCM4752 FBGA Ballout Array (Top View)," on page 33.
4752-DS102-R	06/07/12	**Updated:** • "Features" on page 8: added a bullet for the Power Management Unit (PMU). • Figure 2: "BCM4752 Functional Block Diagram," on page 9. • Section 6: "Pin-Outs and Signal Descriptions," on page 29. • Table 13: "Absolute Maximum Ratings," on page 33. • Table 15: "BCM4752 I/O Digital Specifications," on page 35. • Table 16: "DC Characteristics—Current," on page 36. • Table 17: "BSC Timing Specifications," on page 37. • Section 9: "Ordering Information," on page 40. **Added:** • Figure 1: "BCM4752 Top-Level Diagram," on page 2. • Section 2: "Hardware Description," on page 10. • Section 3: "Power Management," on page 14. • Section 4: "Clocking and Frequency References," on page 18. • Section 5: "Host Transport and Bus Interfaces," on page 24. **Removed:** • "I/O States" on page 32.
4752-DS101-R	12/05/11	Initial release.

Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM4752. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Overview

Features

The Broadcom BCM4752 is a monolithic, single-chip GPS and GLONASS receiver. The main features are listed below.

- Real-time, massively parallel correlator design
- Internal LNA; adjustable gain to support external LNA operation
- Supports industry aiding standards for AGPS applications, including GSM/UMTS (3GPP 44.031, 44.035 and 25.331).
- Excellent transmit blocker performance allowing for single filter on the external BOM
- Enhanced autonomous acquisition—multiday Long Term Orbit (LTO™) data accelerates the acquisition of satellite signals.
- Synchronization pulse input/output enables the BCM4752 to be synchronized to an external timing reference or to provide precise GNSS time to another device
- Support for Satellite-Based Augmentation Systems (WAAS, EGNOS, MSAS, GAGAN)
- GPS Location Library API includes protocol engines for control plane (RRLP, RRC) and user plane (SUPL) interfaces.
- Supports the Quasi Zenith Satellite System (QZSS).
- Autonomous, MS-based, MS-assisted, and Enhanced Autonomous GNSS operation
- Optimized software partition with approximately 4 MIPS host load
- Timestamped GNSS data and a multisecond data buffer
- Noise figure is better than 3.5 dB across Process-Voltage-Temperature (PVT).
- Integrated Power Management Unit (PMU) simplifies power supply requirements.

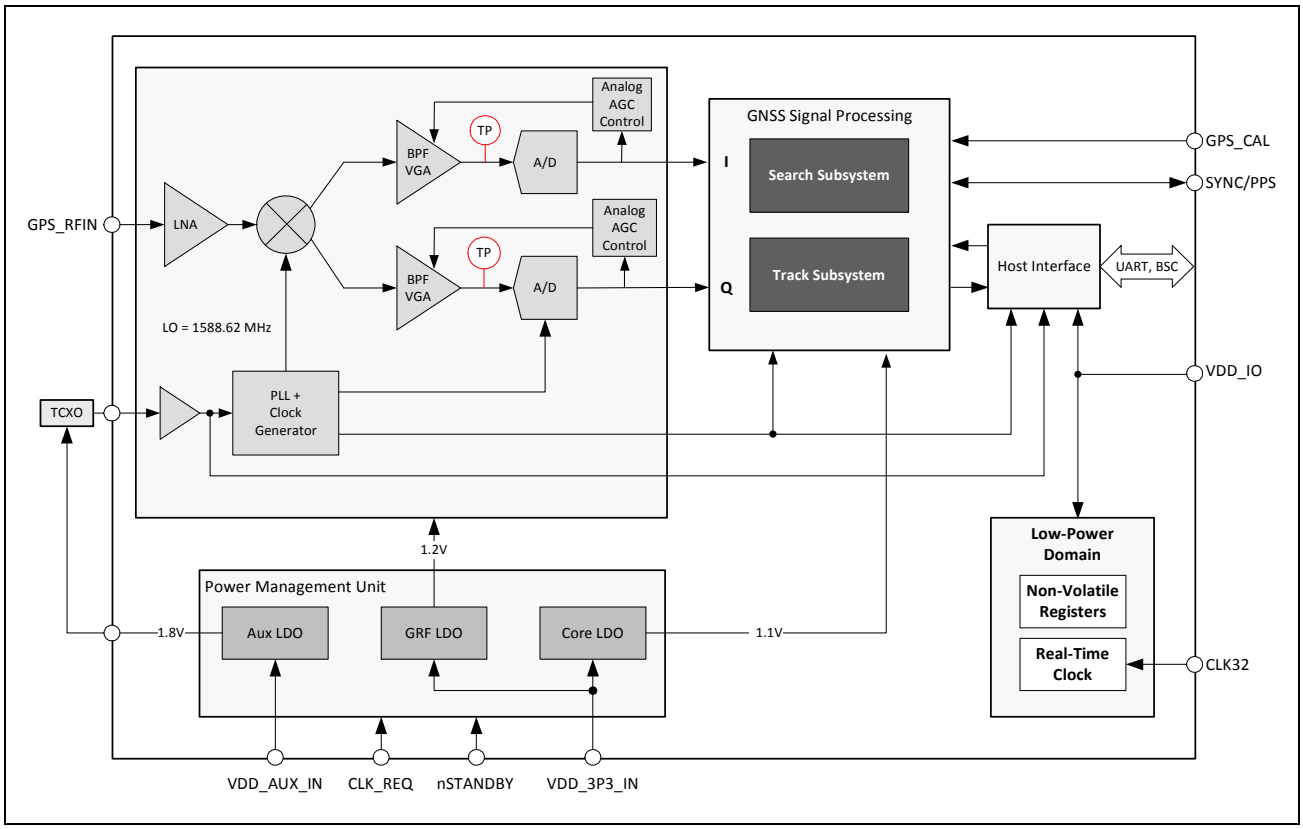


Figure 2: BCM4752 Functional Block Diagram

Section 2: Hardware Description

GNSS (GPS + GLONASS) Radio Architecture

The integrated RF front end of the BCM4752 amplifies, down-converts, filters, and digitizes GPS and GLONASS signals into I and Q streams that are sent to the Baseband Core for additional processing.

The GNSS radio of the BCM4752 is based on a low Intermediate Frequency (IF) down-conversion in-phase/quadrature (IQ) architecture as shown in Figure 2 on page 9. There are parallel and identical paths for the I and the Q channels from the complex mixer to the digital baseband.

Low Noise Amplifier/Mixer

The GNSS signal inputs to the BCM4752 are approximately –190 dBm/Hz for GPS and –188 dBm/Hz for GLONASS while thermal noise is –174 dBm/Hz. The GPS signal is roughly 1MHz wide and the total signal power for GPS is –130 dBm. The GLONASS signal is roughly 500 kHz wide and the total signal power for GLONASS is –131 dBm. Such low input signal power requires that the LNA have very low noise figure (NF).

The LNA amplifies the GPS and GLONASS signals, and the mixer uses the local oscillator to downconvert the 1575.42 MHz GPS and 1596–1607 MHz GLONASS signals to an intermediate frequency (IF). The input is single-ended and can easily be matched to a 50Ω source. The matching circuit should be adjusted on the final circuit board for optimum noise figure. To account for gain from an optional external LNA, the LNA/mixer gain is adjusted using configuration file settings. The output of the LNA and mixer is sent through the IF strip, which is composed of a series of high- and low-pass filters to provide jamming immunity and variable gain amplifier (VGA) stages to amplify the faint GNSS signals.

The GPS_RFIN pin is DC-coupled internally and must be AC-coupled externally.

Frequency Synthesizer

The BCM4752 uses a fractional-N phase-locked loop (PLL) frequency synthesizer to provide maximum flexibility in choosing a reference oscillator frequency. An external temperature-controlled crystal oscillator (TCXO) must be provided to serve as the frequency reference. The synthesizer drives a clock generator to provide the local oscillator for the mixer stage and all internal clocks required by the baseband processor.

A/D Converter

An oversampled A/D converter generates digital IF samples. The A/D converter runs at approximately 79 MHz.

Analog and Digital Automatic Gain Control

For coarse gain adjustment, the analog automatic gain control (AGC) loop optimizes the amplitude of the IF signal into the A/D converter. To accomplish this, the analog AGC digitally measures the power out of the A/D converter and optimally adjusts the analog VGAs. The digital AGC measures the power of the digitized IF and makes fine adjustments to the gain to further optimize the signal power and ensures uniform noise variance for baseband processing.

GNSS Baseband

The BCM4752 baseband processor performs GNSS pseudo-range measurements, Doppler measurements, navigation data bit decoding, carrier phase tracking, and proprietary signal processing tasks that optimize the detection of very low power GNSS signals.

Broadcom provides host software that works in conjunction with the baseband processor to acquire and track satellites, to perform satellite navigation calculations and to manage the satellite selection process. All of the low-level, satellite-specific signal processing occurs within the BCM4752.

The BCM4752 baseband processor uses an advanced search engine that processes the entire GNSS signal delay-space in one step. The correlation peak is detected and analyzed directly, enabling positions to be computed in a fraction of the time required by conventional GPS receivers. The phase and Doppler are transferred to the advanced tracking engine for pseudo-range measurements.

Baseband Architecture

The BCM4752 baseband is composed of two primary blocks. The GNSS Core block performs signal processing tasks. The Low Power (LP) block is used to maintain time-keeping. Most of the circuitry is contained in the GNSS Core block, including some digital RF circuitry. The RF/Synthesizer, and GNSS Core blocks are powered by separate regulators, allowing the Core and RF/Synthesizer blocks to be powered up or down as needed. The digital I/Os and the Low Power domain are powered by VDD_IO, which must be regulated externally and should match the I/O voltage used by the host interface.

Baseband Functional Description

The GNSS baseband section includes all the real-time signal processing needed to accomplish the tasks of signal detection, signal measurement, and navigation data decoding. The BCM4752 uses a proprietary architecture that segments GNSS processing into a hardware/software measurement engine and a software positioning engine. A key aspect of the interface is that the host software does not interact with the GNSS chip for any real-time signal processing operations. Thus, the system can deliver full performance operation without imposing latency requirements on the software running in the host.

The GNSS baseband section outputs measurement data at 1 Hz; this can be varied under software control to conserve power. The host software processes the measurements, outputs a navigation solution, and sends any necessary commands to the chip, after which the host platform can enter a sleep state or perform other tasks. The BCM4752 command and response FIFOs can hold several seconds of data, which allows the host software to process several seconds of measurements at once. This compensates for situations when the host software is busy with another task.

Unlike other firmware-based architectures, in the BCM4752 the carrier tracking loops, navigation data decoding, bit synchronization, and other algorithms are performed in a hardware-based correlation coprocessor, enabling a powerful and extremely power-efficient implementation. Parameters for coprocessor algorithms can be configured to ensure flexibility.

Time Transfer Interface

The Time Transfer Interface block is used in systems that are synchronized to an external source of GPS time. In such designs, a precise synchronization signal (SYNC) is input to the chip and a counter measures the time offset between the external time-source clock and the BCM4752 internal clock. The offset is measured with an accuracy of better than 500 ns and is then used by the navigation control software to establish a precise relationship between the internal clocks and the external clock. Figure 3 illustrates the time transfer process. The BCM4752 can also be configured to output a timing pulse (PPS) on the same pin. This software-enabled feature generates pulses synchronized with GPS time.

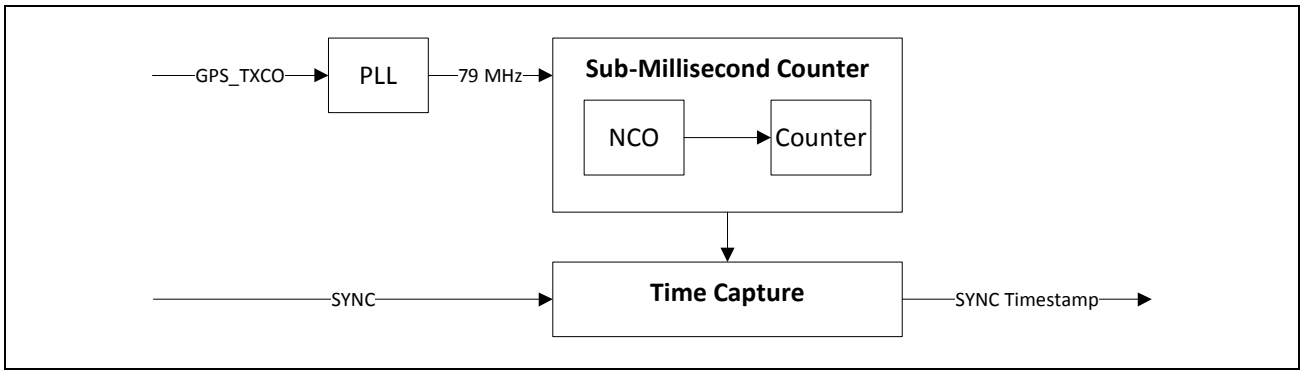


Figure 3: Precision Time Transfer

Frequency Counter

The frequency counter provides a means for measuring the reference clock frequency relative to a separate external reference. Figure 4 illustrates the frequency calibration process. Typical frequency measurement accuracy with respect to the reference clock is 10 parts per billion (ppb).

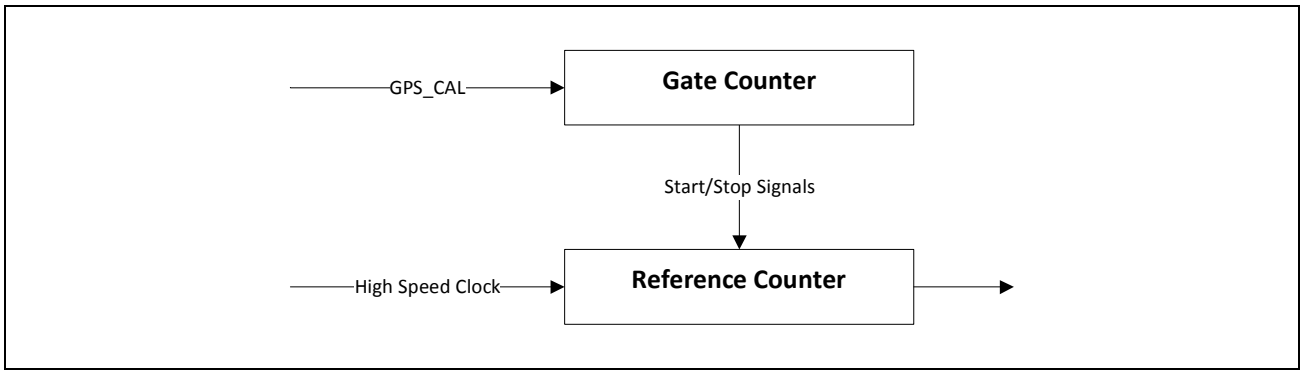


Figure 4: Frequency Calibration Process

Internal Microprocessor and Memory

The internal microprocessor runs all GNSS tasks with minimal latency. It is paired with a memory unit for program storage and ROM. Software patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or for adding features. These patches can be downloaded from the host to the BCM4752 through the host interface.

ROM, RAM, and Patch Memory

The BCM4752 has 92 KB of instruction ROM that is used for the lower layer protocol stack, test mode software, and boot ROM. To support firmware updates, the BCM4752 has 96 KB of patch RAM that allows code changes to be inserted for the purpose of fixing bugs and adding features to ROM memory. The BCM4752 has 48 KB of internal RAM that is used as general purpose scratch-pad memory.

Reset

Separate power-on reset (POR) signals are provided for the Core Logic domain and the Low Power domain. This allows the logic in the LP domain to keep time while the core logic is forced into a reset state during Deep-Sleep mode. The NSTANDBY signal can be used to force a reset to the entire chip, excluding the LP domain, by cycling the CORE_LDO regulator.

Section 3: Power Management

Power Management Unit

The BCM4752 has three on-chip power domains: I/O and low-power (VDD_IO), digital baseband core processing (VDD_CORE), and, finally, the analog radio (VDD_GPS_LNA and VDD_GPS_IF). The BCM4752 also has an auxiliary low-dropout regulator (AUX_LDO) which can supply regulated 1.8V power for the external TCXO and optionally an external LNA.

The PMU contains three low-dropout regulators: CORE_LDO for the digital baseband core, GRF_LDO for the analog radio and frequency synthesizer, and AUX_LDO for the TCXO and optional external LNA. The VDD_3P3_IN pin supplies current to the core and analog radio regulators, while the VDD_AUX_IN pin supplies current to the AUX_LDO. Using separate inputs allows the power consumption to the core and RF to be minimized while still meeting the higher input voltage required for the 1.8V AUX_LDO regulator.

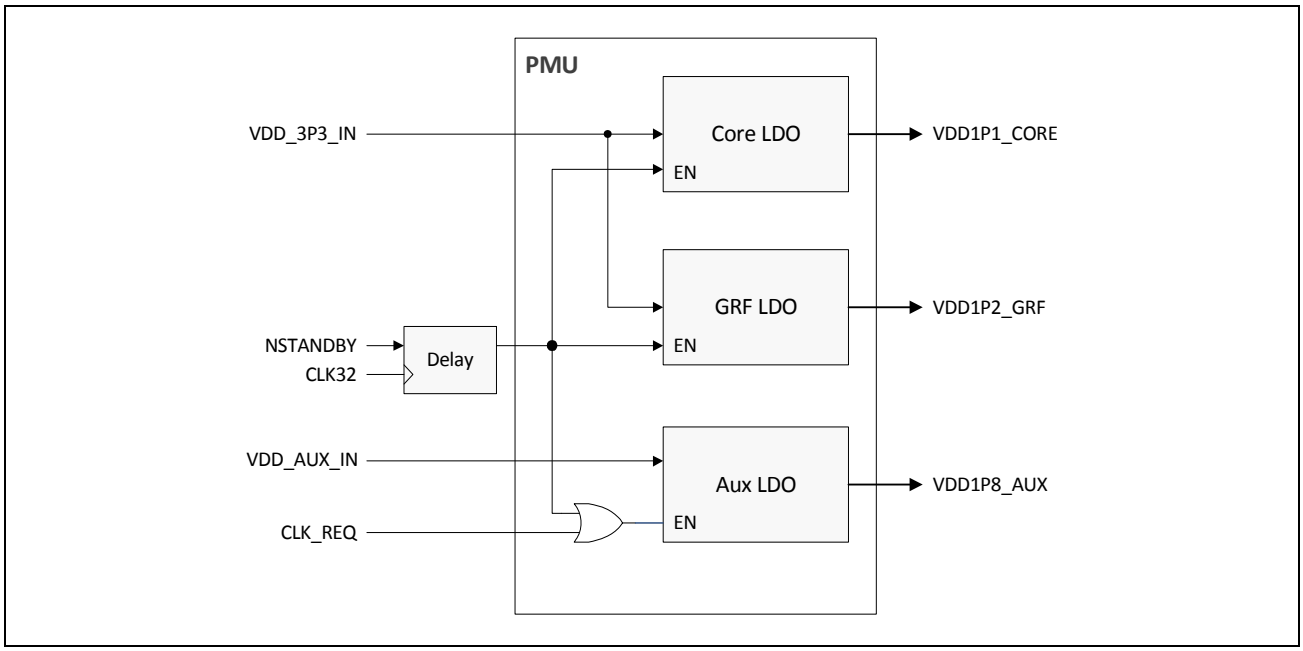


Figure 5: BCM4752 Power Management Unit

VDD_IO requires externally regulated power and provides power to the I/O cells and to the Low Power domain. External digital interfaces for the BCM4752 to the host CPU are referenced to VDD_IO. Power should always be applied to VDD_IO in order to retain nonvolatile configuration and timing data while the rest of the chip is powered down. The Low Power domain is designed for minimal power consumption to avoid unnecessary battery drain while in Standby mode. All three regulators turn on when the NSTANDBY pin is deasserted to power up the chip.

The NSTANDBY pin is used to power up the chip by enabling all three regulators. The CLK_REQ pin provides an additional way to turn on the AUX_LDO regulator. CLK_REQ is an active high input and is ORed with the NSTANDBY-controlled signal to enable the AUX_LDO. This allows a TCXO powered by the AUX_LDO to be shared with another subsystem without powering up the BCM4752.

Power Supplies

Table 1 defines the specifications for BCM4752 power supplies.

Note: Power supplies can be activated in any order.

Table 1: BCM4752 Required Power Supply Inputs

	Specification			
Required Parameter	***Minimum***	***Nominal***	***Maximum***	***Units***
Regulated supply (VDD_3P3_IN)	1.62	1.8	3.63	V
I/O voltage (VDD_IO)	1.65	1.8	3.63	V
Aux supply (VDD_AUX_IN)	2.3	–	5.5	V

Table 2 defines output characteristics for the CoreLDO, GRFLDO, and AuxLDO regulators.

Table 2: Regulator Output Characteristics

Regulator	***Minimum***	***Maximum***	***Rated Current***
CoreLDO	1.06V	1.18V	100 mA
GRFLDO	1.16V	1.28V	25 mA
AuxLDO	1.71V	1.89V	12 mA

A 1–2.2 µF capacitor is required at the output of each regulator. Ceramic capacitors with ESR of 0.005–0.3 Ω are required.

Input and output capacitors should be placed as close as possible to the associated pins to minimize trace inductance. The regulator output trace width should be at least 10 mils, and the trace length to the output capacitor should be less than 130 mils.

Power Modes

The BCM4752 has two externally controlled power modes: Active and Standby. In Active mode, all three regulators are powered up and the GPS Location Library (GLL) software performs GPS signal processing. In Standby mode, everything but the Low-Power domain and the I/O cells are powered down, and the LPO_IN clock is used to maintain time. Table 3 shows the state of the regulators as a function of the operating mode of the BCM4752.

Table 3: BCM4752 Power Modes

Mode	*VDD_IO*	*CoreLDO*	*GRFLDO*	*AuxLDO*
Active	Applied	ON	ON	ON
Standby	Applied	OFF	OFF	OFF or enabled by CLK_REQ

During VDD_IO power-up there is a VDD_IO-Only POR which is used to reset the Low Power domain to a known initial state. Power-up behavior is described in "Power-Up Sequence" below.

Power-Up Sequence

NSTANDBY is the main enable/power-up signal for the BCM4752. When NSTANDBY transitions from low to high, the BCM4752 is powered and the CORE_LDO, GRF_LDO, and AUX_LDO regulators are turned on. NSTANDBY should not be asserted until VDD_IO is on and CLK32 is running and stable. There is a safeguard delay after the AUX_LDO is enabled to ensure the TCXO is stable. A transition from high to low on NSTANDBY causes the BCM4752 to enter Standby mode with CORE_LDO, GRF_LDO, and AUX_LDO turned off. In Standby mode, time-keeping logic powered by VDD_IO uses the CLK32 clock to keep track of elapsed time.

The diagram below shows a first power-up when VDD_IO is initially ramped up. NSTANDBY (active low) is asserted until CLK32 is stable. Subsequently, NSTANDBY is deasserted to turn on the CORE_LDO, GRF_LDO, and AUX_LDO on-chip regulators.

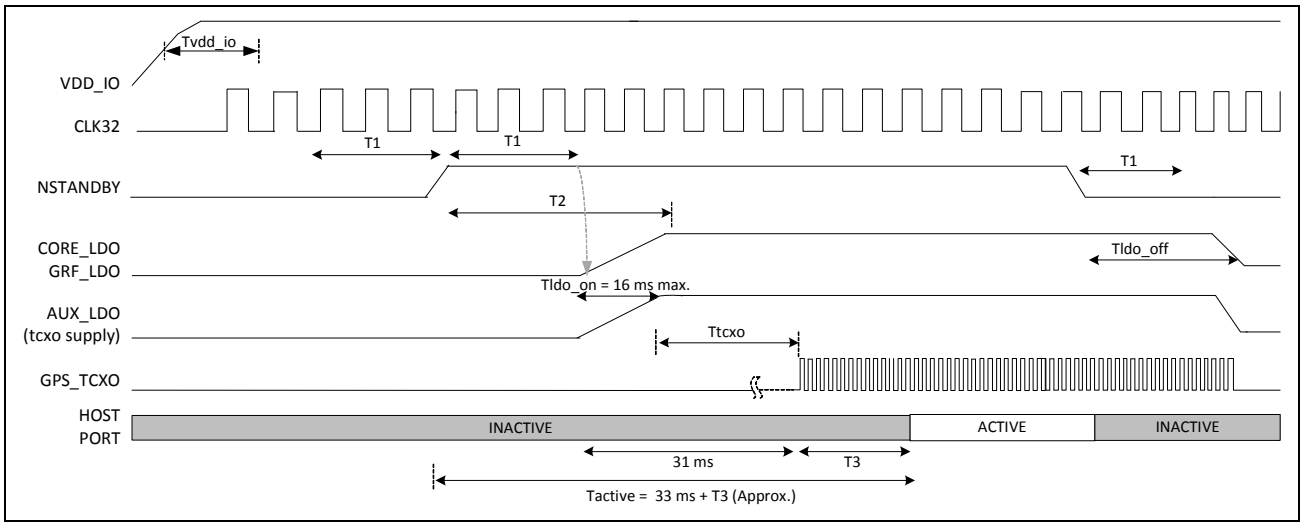


Figure 6: BCM4752 Power-Up Sequence

Note: The TCXO is powered by AUX_LDO; CLK32 is ON whenever VDD_IO is ON.

Power Sequence Timing Parameters

Power sequence timing parameters for the BCM4752 are defined in Table 4.

Table 4: Power Sequence Timing Parameters

Parameter	*Description*	*Min.*	*Typ.*	*Max.*	*Unit*
T_{VDD_IO}	VDD_IO power-up delay, starting from VDD_IO threshold of 0.7V. VDD_IO must settle within the recommended range by the end of this time-frame. The entire chip is in reset during this time	35	36	37	ms
T_0	Time from CLK32 stable to NSTANDBY negated	2	–	–	CLK32 period
T_1	Duration of NSTANDBY assertion/negation.	3	–	–	CLK32 period
T_{LDO_ON}	CORE_LDO/GRF_LDO/AUX_LDO ramp-up time	–	12	16	ms
T_2	NSTANDBY to regulator on time	–	13	17	ms
T_{TCXO}	TCXO delay from AUX_LDO on time	–	–	12	ms
T_3	Internal boot time	–	–	TBD	ms
T_{ACTIVE}	NSTANDBY negated to Device Active	32 ms + T3			ms
T_{COLD_START}	VDD_IO on to Device Active	75 ms + T3			ms

Section 4: Clocking and Frequency References

Overview

The BCM4752 uses a fractional-N synthesizer to generate all internal clocks based on the TCXO reference input clock. This enables the BCM4752 to operate from any of a multitude of frequencies ranging from 10–52 MHz. The synthesizer parameters are programmed by the software based on the supplied TCXO frequency.

In order for the system to boot up, an external 32.768 kHz clock must be connected to the CLK32 input.

Figure 7 shows the top-level diagram of the clocking configuration of the BCM4752, including the names of the relevant pins.

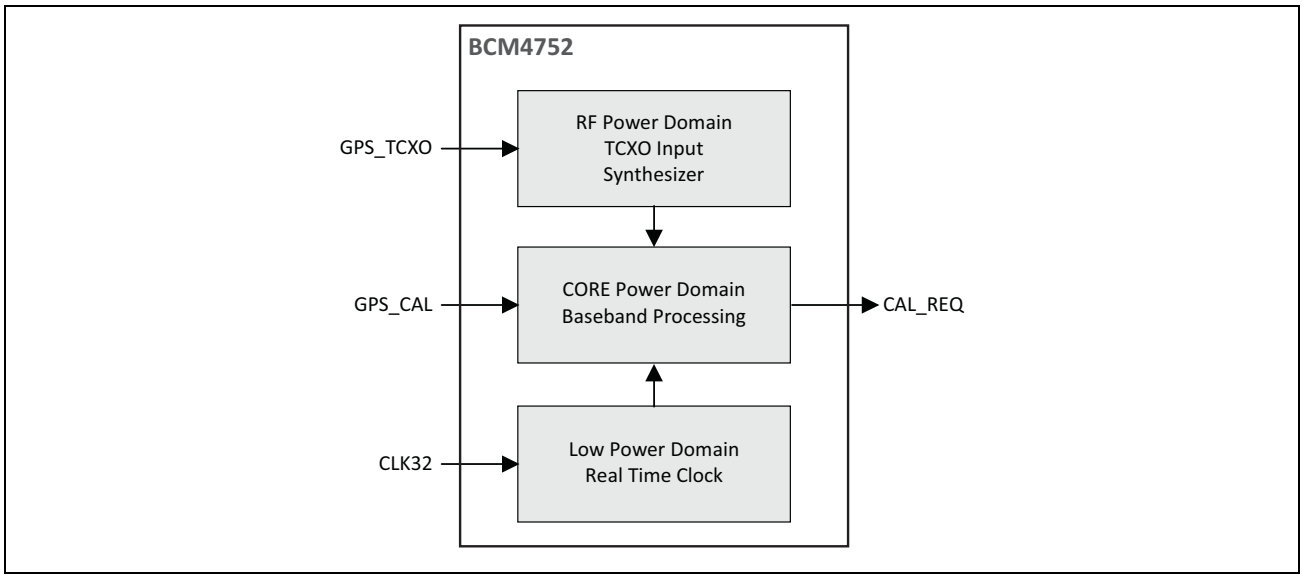


Figure 7: BCM4752 Top-Level Clocking Diagram

The main pins for the clocking subsystem are as follows:

- GPS_TCXO — AC coupled input from the TCXO.
- CAL_REQ — Output to enable a buffer for the GPS_CAL signal from the host system. This is an optional signal; GPS_CAL may also be controlled by software.
- GPS_CAL — Calibration clock input used to calibrate the TCXO.
- CLK32 — Input for the external 32 kHz clock coming from the host. This signal is used for time keeping while the BCM4752 is in the standby mode, as well as to control the startup timing during the transition to active mode.

The clocking subsystem in the BCM4752 supports different clocking configurations. The main supported configurations include:

- Local GPS TCXO — Hardware calibration against the calibration clock frequency.
- Shared TCXO with the host, software calibration — The frequency offset is provided as a parameter in the clock calibration request call by the host. The impedance seen by the TCXO must be stable; the buffers connected to the TCXO must not change the load seen by the TCXO output. Most buffers have input impedances that vary depending on whether the buffer is active or powered down. Broadcom engineers recommend that any buffer connected to the GPS TCXO not change state (active to or from powered down) while the GPS processing is active.

TCXO Requirements

A stable, low-noise reference oscillator is vital to a GNSS receiver. Figure 8 shows the waveform for the TCXO signal and Table 5 defines required characteristics. The phase noise requirements for the TCXO are given in Table 6. In addition, to avoid GNSS interference issues, frequencies that have harmonics which land within 3 MHz of the GPS L1 center frequency at 1575.42 MHz, or in the GLONASS band of 1597–1607 MHz, should be avoided. The GPS_TCXO input is AC-coupled, so it should be connected directly to the TCXO output.

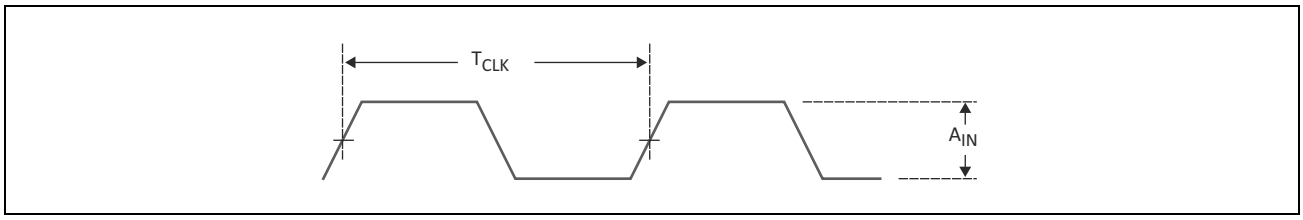


Figure 8: TCXO Waveform

Table 5: GPS_TCXO Requirements

Parameter	*Value*	*Units*
Supported frequency range	10–52	MHz
Signal type	Sine, square, or clipped sine wave	–
Amplitude (Ain)	400–2000	mVp-p
Minimum voltage	–0.3	V
Maximum voltage	3.63	V
Input impedance	100 (AC-coupled)	kΩ
Performance Requirements		
Frequency tolerance (initial accuracy)	±2	ppm
Frequency stability over temperature (–30°C to +85°C)	±0.5	ppm
Frequency slope (–30°C to 85°C)	±0.1	ppm/°C

Table 5: GPS_TCXO Requirements (Cont.)

Parameter	*Value*	*Units*
Short-term Stability		
First 10 sec after start-up	±40	ppb/10 sec
After 10 sec	±10	ppb/10 sec
AC duty cycle	40–60	%
Aging characteristics (per year)	±1	ppm

Table 6: Phase Noise Requirements for the BCM4752 Reference Frequency

	SSB Noise (dBc/Hz)		
Offset from Carrier	***10 MHz***	***26 MHz***	***52 MHz***
10 Hz	–88	–80	–74
100 Hz	–113	–105	–99
1 kHz	–138	–130	–124
10 kHz	–148	–140	–134
100 kHz	–153	–145	–141
1 MHz	–153	–145	–141

Calibration Procedures

The initial frequency configuration process provides a coarse reference frequency that is suitable for autonomous operation. A faster time-to-first-fix (TTFF) can be achieved by performing a calibration based on an additional precise clock signal.

Hardware Calibration

Hardware calibration means the TCXO frequency is calibrated against a known calibration signal coming from the platform into the GPS_CAL pin. In the BCM4752, GPS_CAL is connected to a counter that accumulates the cycles elapsed during the calibration interval. The TCXO is then calibrated using the known frequency value.

Figure 9 shows a block diagram of a typical implementation in which a local TCXO is used as the reference clock, and an external digital clock from the host is used for calibration. The signal driving GPS_CAL (see Figure 10 on page 21) must meet the digital input requirements in Section 7: "Electrical Characteristics," on page 34. The AC requirements are given Table 7 on page 22.

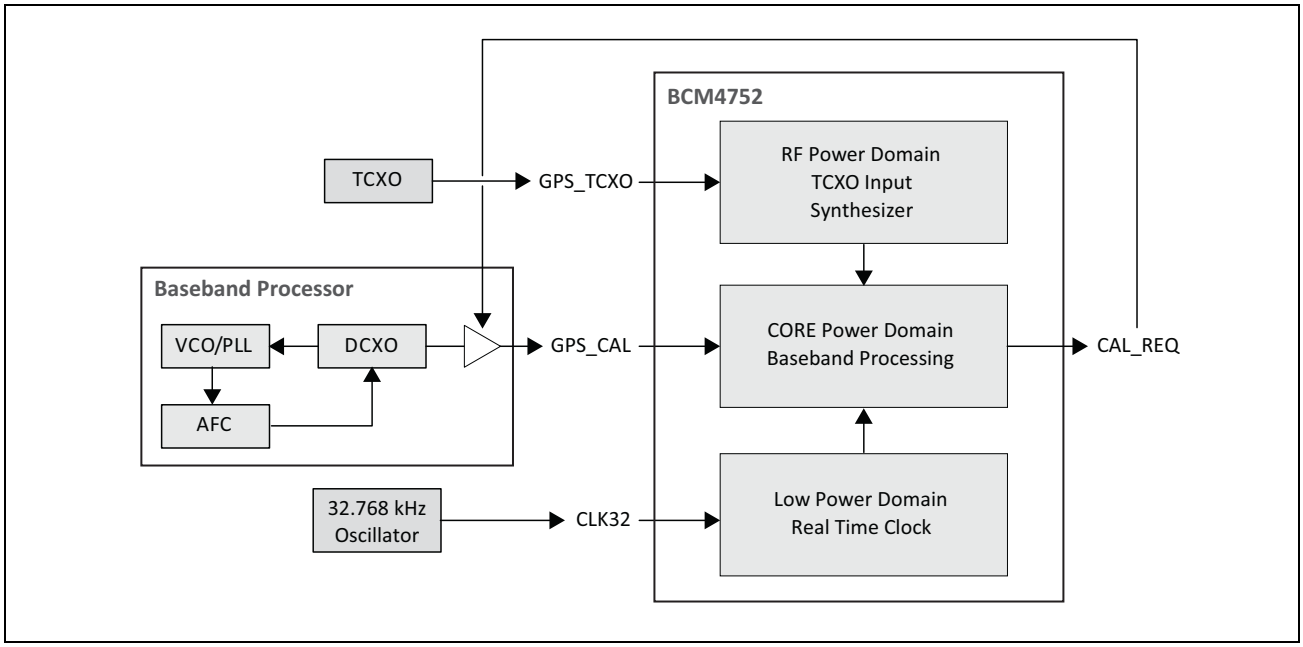


Figure 9: Local GPS TCXO with a Reference Clock for Calibration

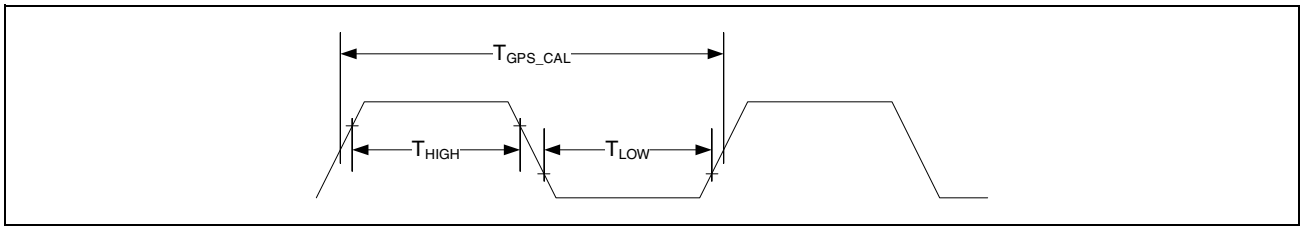


Figure 10: GPS_CAL Input Waveform

Table 7: GNSS Calibration Clock Requirements

Parameter		*Minimum*	*Maximum*	*Units*
Frequency		10	52	MHz
T_{GPS_CAL}	Period	19.2	100	ns
T_{High}	High time	7	–	ns
T_{Low}	Low time	7	–	ns
Frequency accuracy (at time of calibration)		–	±100	ppb

Software Calibration

Software calibration is typically used when the GPS subsystem shares the platform TCXO with the cellular host. GPS performance is closely related to the quality of the TCXO, so it is important that a TCXO of good quality is used. It is also important that the clock signal fed to the TXCO pin on the BCM4752 is free of abrupt AFC adjustments that can cause discontinuities in the frequency and phase of the clock signals. Such discontinuities affect the ability of the GPS receiver to decode navigation data from the GPS signals that use BPSK modulation.

Figure 11 shows a typical implementation of the software calibration configuration.

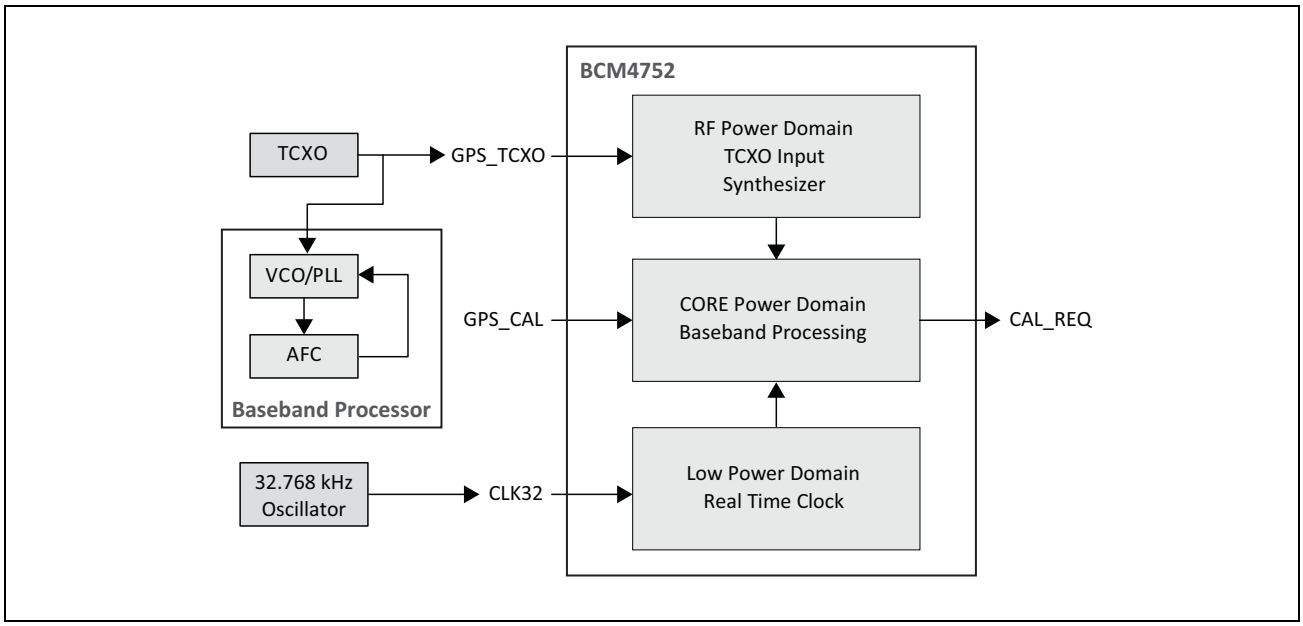


Figure 11: Shared TCXO with Software Calibration

In this mode, the TCXO is free-running, so it is not subject to AFC changes. The host, however, may have knowledge of the frequency offset of its TCXO with respect to a cellular base station. The TCXO offset can be provided to the BCM4752 through a software command. This mode saves the dedicated TCXO for the GPS subsystem, so it is very advantageous from a material cost point of view.

32 kHz Clock Interface

An external 32.768 kHz digital clock must be applied to the CLK32 pin of the BCM4752 at all times. This clock is used to keep track of elapsed time while Standby mode is in effect, and is used to establish the startup timing during the transition to Active mode. Figure 12 and Table 8 show the requirements for CLK32 clock. CLK32 signal levels must meet the digital I/O requirements (see page 36).

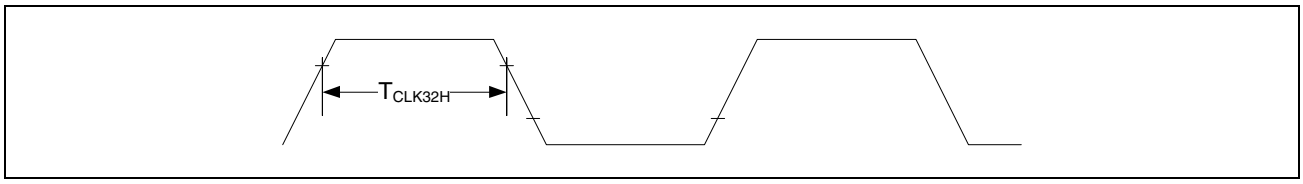


Figure 12: 32 kHz Clock Input Waveform

Table 8: External CLK32 Clock Requirements

Parameter	*Value*	*Units*
Nominal input frequency	32.768	kHz
Signal type	Square wave	–
Frequency tolerance	±100	ppm
High time T_{CLK32H}	100 minimum	ns

SYNC Input/PPS output

The SYNC input or pulse-per-second (PPS) output can be used to transfer precise time between the BCM4752 and an external system. A transition on the SYNC input will cause a precise time stamp to be captured inside the BCM4752 when instructed to do so by the GLL software. Alternatively, the PPS output can be instructed to output a timing pulse precisely aligned with GPS time. The polarity is programmable and the signal must meet the Digital I/O requirements.

Section 5: Host Transport and Bus Interfaces

Overview

The BCM4752 host interface can operate in either of two different modes: UART or Broadcom Serial Control (BSC) slave. The BSC slave is compatible with version 2.1 of the I^2C two-wire bus. The two interfaces are multiplexed onto the same four interface pins, and the interface selection is performed automatically by observing the activity the UART_RX/SDA and UART_TX/SCL pins during the first transmission from the host CPU after the BCM4752 is powered up.

UART/BSC Pins

Table 9 defines the states of the UART/BSC pins under different transport conditions.

Table 9: UART/BSC Pins

Pin	*Boot State (No Transport Selected)*	*BSC Transport Selected*	*UART Transport Selected*
UART_NRTS, HOST_REQ	Tristated with internal pull-down enabled. This means that nRTS is driven "ready for receiving" and a host using hardware flow control will be able to transmit data to the BCM4752.	Defaults to tristated GPIO with internal pull-down. Software will configure this to be used as the HOST_REQ output.	Defaults to tristated GPIO with internal pull-down. Software can configure this pin to output the UART RTS hardware handshake signal.
UART_NCTS, ANT_SEL	Tristated with internal pull-down to prevent the input from floating.	Defaults to tristated GPIO with internal pull-down.	Defaults to tristated GPIO with internal pull-down. Software can configure this pin to receive the UART CTS hardware handshake signal.
UART_RX, SDA	Tristated with internal pull-up.	Bi-directional data signal for the BSC interface.	Sent as input to BCM4752 UART.
UART_TX, SCL	Tristated with internal pull-up to prevent floating TX.	Clock input for the BSC interface	Output driven by BCM4752 UART.

Transport Detection

After power-up initialization, the BCM4752 will wait until the first data transmission from the host CPU before any processing can begin. By observing the activity on the UART_RX/SDA and UART_TX/SCL pins, it will automatically determine whether UART or BSC is in use, as shown in Figure 2.

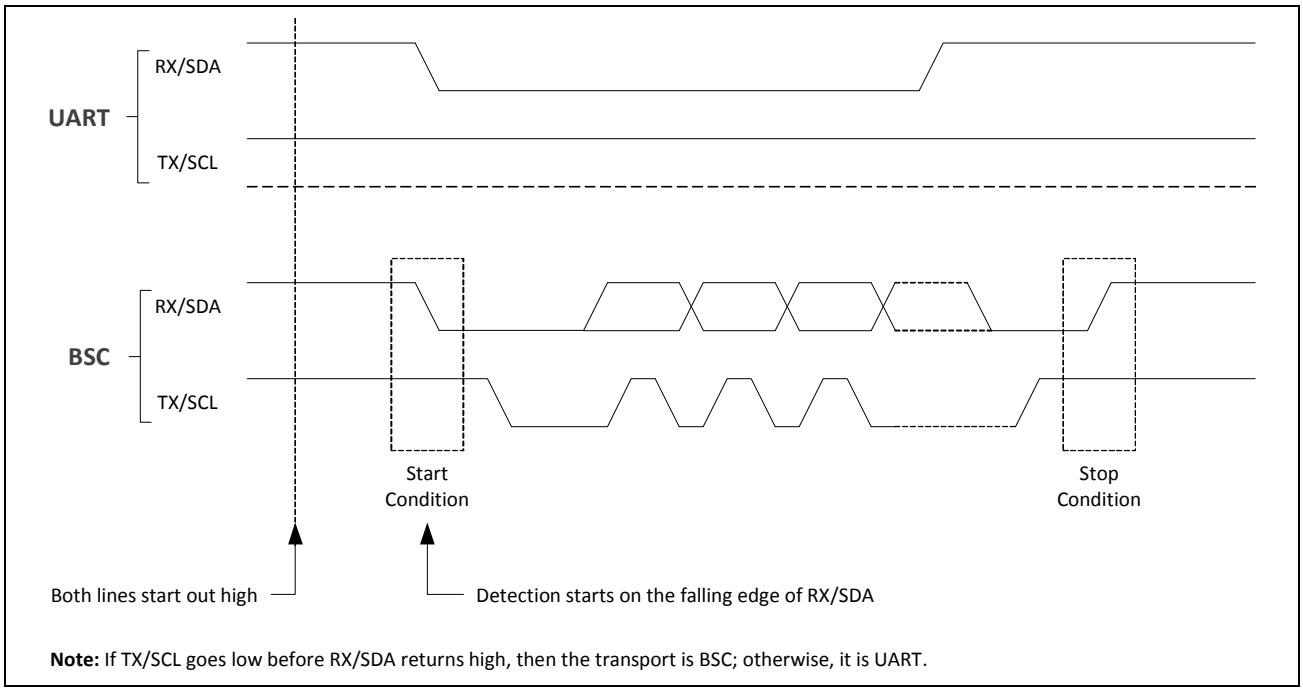


Figure 13: BCM4752 Transport Detection

If the UART interface is selected, an automatic baud rate detection process will begin immediately. The UART baud rate generator will match the baud rate observed during a special autobaud sequence transmitted by the host software.

If the BSC interface is used, the first attempt at communication will not be acknowledged by the BCM4752, and will be lost. This first packet will trigger the transport detection and the BSC slave will be connected. Subsequent BSC packets can then be used to configure the BSC interface.

UART Interface

The BCM4752 uses a standard 4-wire UART with optional hardware or software flow control. Any baud rate from 38,400 up to a maximum determined by the TCXO frequency can be used. The maximum baud rate is calculated as:

$$Max\ Baud\ Rate = \frac{F_{TCXO}}{16.25}$$

For a 26 MHz TCXO, the maximum is 1.6 Mbps.

The UART data format is fixed at 8 data bits, no parity, and 1 stop bit (8N1).

Flow control is required for reliable UART communications. The BCM4752 can be configured for either hardware or software flow control.

Hardware Flow Control

Hardware flow control is enabled by connecting the UART_nRTS and UART_nCTS signals to the host UART. When the BCM4752 is ready to receive data, the UART_nRTS (ready for receiving) pin will be asserted low. The external host may send data to the BCM4752 whenever UART_nRTS is asserted. When the BCM4752 cannot keep up with the incoming data, the UART_nRTS pin will be deasserted by raising it to the high state. The external host is allowed to send up to 16 additional bytes after NRTS is negated. This is allowed because the external host may not recognize the negation of NRTS immediately and may have queued up to 16 bytes in its transmitter FIFO. When the UART_nRTS pin is reasserted, the host may resume sending data.

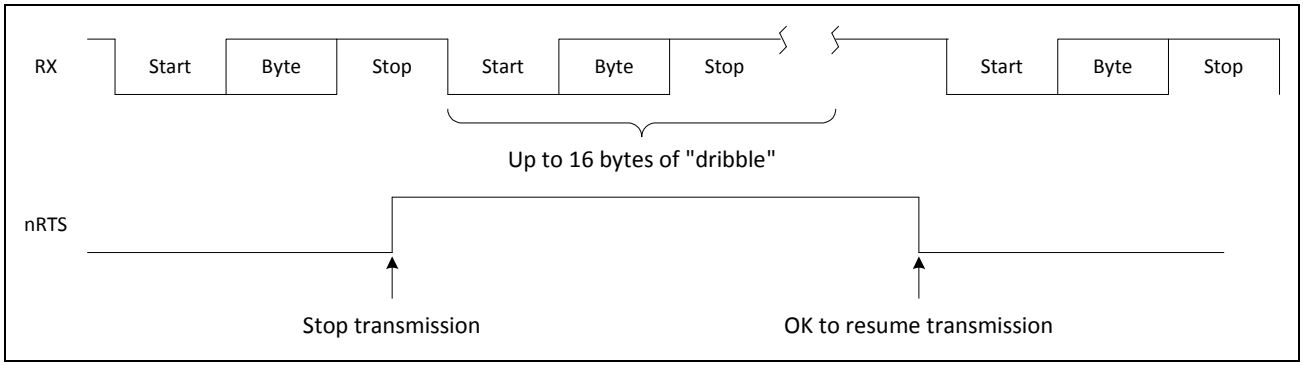


Figure 14: Receiver Flow Control

When the BCM4752 has a character ready to send, the transmitter state machine checks the state of the UART_nCTS pin. If UART_nCTS is asserted low by the external host, then the BCM4752 transmitter will send out the character. If UART_nCTS is not asserted, then the BCM4752 will wait until it is asserted. If UART_nCTS is deasserted in the middle of a character transmission, then the transmitter will complete the transmission of that character before idling. Depending upon the timing of NCTS versus the BCM4752 internal clocks, one additional character may be transmitted after UART_nCTS is asserted. As long as UART_nCTS is deasserted before the middle of the STOP bit, then no additional characters will be transmitted.

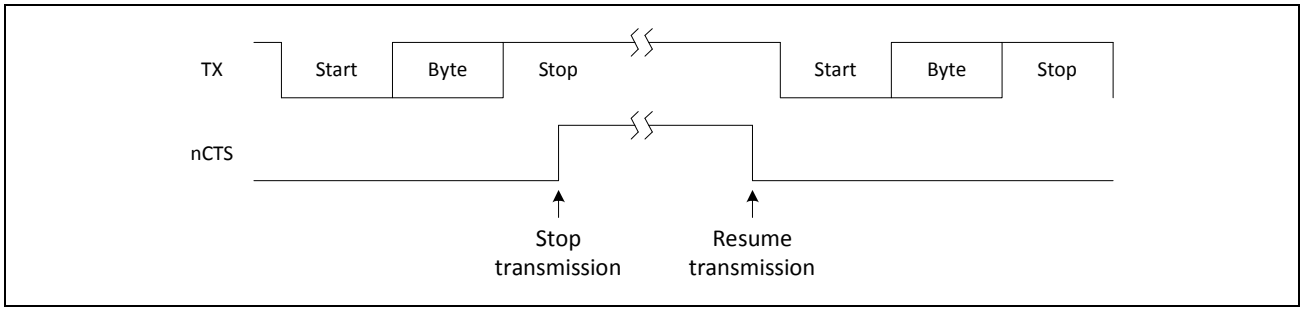


Figure 15: Transmitter Flow Control

Software Flow Control

Software flow control can be used when the hardware flow control signals are not available. In this mode, flow control characters are embedded into the data stream to stop the flow of data when the receiver is unable to keep up. The transmitter and receiver work together to manage the flow of data.

When the receiver receives a valid byte matching the XOFF code it disables the transmitter just like the deassertion of UART_nCTS would disable the transmitter. When the receiver receives a valid byte matching the XON code it enables the transmitter, just like the assertion of UART_nCTS would enable the transmitter. The receiver strips XON/XOFF bytes from the data stream, so they do not enter the receive FIFO. The GLL software will encode any XON or XOFF bytes that appear in the actual data so that they will never appear in the transmitted data.

When the receiver FIFO level changes from 1 byte to 2 bytes, the transmitter will transmit an XOFF byte. When the receiver FIFO level changes from 1 byte to 0 bytes the transmitter will transmit an XON byte. The transmitter will send outgoing XON/XOFF bytes for the purposes of flow control even if it has been disabled by the reception of an XOFF byte.

BSC Slave Interface

BSC is a 2-wire serial interface that allows several devices to reside and communicate on the same bus, in conformance with version 2.1 of the I^2C bus specification. The BCM4752 has a BSC slave controller that can be used for host communication instead of the UART interface. Table 10 describes the BSC controller in the BCM4752.

Table 10: BCM4752 BSC Controller

I^2C-Compatible Interface	*Supported Mode*	*Supported Data Rates*	*Supported Addressing*
BSC	Slave	Standard—100 kbps Fast—400 kbps	10-bit (default), and 7-bit

The two signals required by the BSC interface, SDA and SCL, are multiplexed with the UART_RX and UART_TX signals. One additional signal, HOST_REQ, is provided to enable the BSC slave to signal to the BSC master that it has data ready to be transferred, and that the master should initiate a read transfer. HOST_REQ is multiplexed with the UART_NRTS signal.

The BSC interface in the BCM4752 supports a clock rate of up to 400 kHz. The default BSC slave address after a reset is 10-bit address 0x1FA. This may be changed to an alternate 10-bit address or to a 7-bit address with a configuration message. External pull-ups are required in the system for the slave interface to operate with a master controller.

The BSC slave interface is designed to look similar to a UART to the host software, so it is referred to it as an emulated UART. Thus only two types of transfers are necessary:

- Reads from the emulated UART data register (includes transmit count)
- Writes to the emulated UART data register

The BSC slave interface does not need to know about anything other than the two operations listed above. Higher level transactions are managed by the firmware running on the embedded CPU. The two supported transfer types are shown in Figure 16 and Figure 17. For the sake of simplicity, all transfers are shown with 7-bit BSC addressing. Please see the NXP® I^2C Specification for information about 10-bit addressing.

BSC Emulated UART Data Register Reads

If the BSC master reads more bytes than the BCM4752 slave has available (what was returned in the byte count), then the slave will return zeroes for those bytes, and the host software will be able to discard those bytes. This allows the transfer size to be set before the byte count has been received, and may help improve efficiency.

The HOST_REQ pin should be used to indicate to the host when transmit data is available. A high output from HOST_REQ indicates that the transmit FIFO is not empty, and a low output indicates that the transmit FIFO is empty.

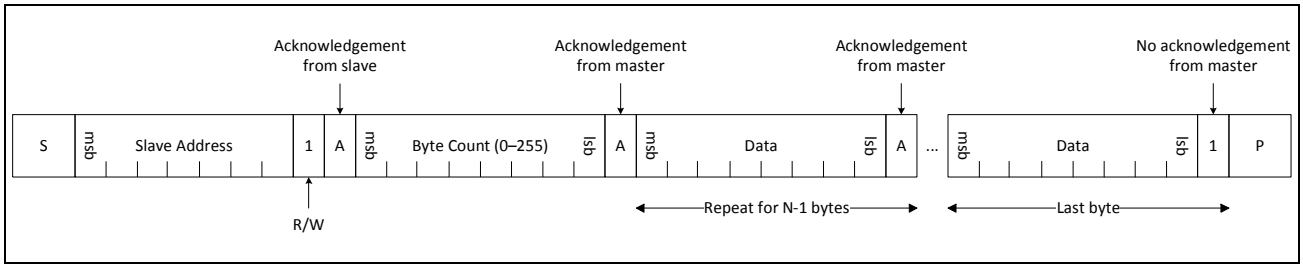


Figure 16: BSC Emulated UART Data Register Reads

BSC Emulated UART Data Register Writes

If the BSC master attempts to write more bytes than the BSC slave can accept, then the slave will NACK (negative acknowledgement) the bytes that it cannot accept. The BSC master should stop transmission after a NACK is received, and attempt to re-send the data starting with the byte that was NACKed. Although the receive FIFO is only 18 bytes deep, it is backed by a DMA engine, so it is not expected that the slave will ever NACK a byte. Nevertheless, since this is theoretically possible (for example, embedded firmware could disable RX DMA, or fall behind processing the DMA buffers) the NACK is included for completeness.

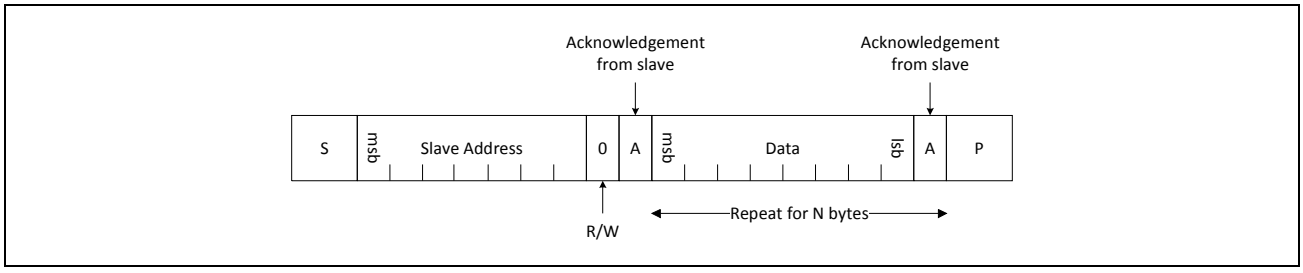


Figure 17: BSC Emulated UART Data Register Writes

Section 6: Pin-Outs and Signal Descriptions

Table 11 defines pin-outs and signals for the BCM4752. The Type column contains one or more of the following entries:

- **I** = Input signal
- **O** = Output signal
- **I/O** = Input/Output signal
- **G** = Ground
- **P** = Power
- **PD** = Pull-down
- **PU** = Pull-up
- **PMUPD** = PMU pull-down

Table 11: BCM4752 Pinouts

Pin							
WLBGA	***FBGA***	***Name***	***Description***	***Type***	***Standby State and Pull Resistor***	***Active Level***	***Comment***
Reset and Test Mode Pins							
C5	C1	TM0	Test mode	I	Hi-Z/PD	High	Connect to GND.
–	D7	NRESET	Reset	I	Hi-Z/PU	Low	Reset pin has an internal pull-up resistor. Leave this pin floating.
Clocking and Blanking Pins							
A5	A1	GPS_CAL	Calibration clock	I	Hi-Z/PD	–	–
E4	G3	GPS_TCXO	TCXO input	I	–	–	Analog input
A6	A2	CLK32	32768 Hz timekeeping input	I	Hi-Z	–	–
B5	B1	SYNC	Timestamp signal	I	Hi-Z/PD	Programmable	–
		PPS	Pulse-per-second output	O	Hi-Z/PD	Programmable	
A3	A4	IFVALID	Transmit blanking signal.	I	Hi-Z/PD	Programmable	–

Table 11: BCM4752 Pinouts (Cont.)

Pin					Standby State and Pull		
WLBGA	FBGA	Name	Description	Type	Resistor	Active Level	Comment
Communication Pins							
A1	A7	SDA	BSC data	I/O	Hi-Z/PU	High	Host BSC transport serial data
		UART_RXD	UART receive	I	Hi-Z/PU	High	Host UART transport data receive
A2	A5	SCL	BSC clock	I	Hi-Z/PU	High	Host BSC transport serial clock
		UART_TXD	UART transmit	I/O	Hi-Z/PU	High	Host UART transport data transmit. This pin is an input until UART transport detection completes, then it becomes an output.
B1	B6	UART_NRTS[a]	UART ready for receiving	O	Hi-Z/PD	Low	Used when UART is active.
		HOST_REQ	Host request	O	Hi-Z/PD	High	Used when BSC is active.
B2	A6	UART_nCTS[a]	UART clear to send	I	Hi-Z/PD	Low	Used when UART is active.
		ANT_SEL	Antenna select	O	Hi-Z/PD	–	Optional signal. Can be used to select between two antennas.
B6	B2	LNA_EN	LNA enable	O	Hi-Z/PD	High	External LNA enable.
		CAL_REQ	Calibration signal request	O	Hi-Z/PD	High	Optional signal. Can be used to enable a calibration clock buffer.
RF and Analog Pins							
D6	F1	GPS_RFIN	RF input	I	–	–	DC-coupled analog input
D4	E3	GPS_TEST_OUT	RF test output	O	–	–	–

Table 11: BCM4752 Pinouts (Cont.)

Pin					Standby State and Pull		
WLBGA	FBGA	Name	Description	Type	Resistor	Active Level	Comment
Power Management Pins							
B3	B5	NSTANDBY	Standby/power-on signal	I	Hi-Z	Low = Standby High = Power on	–
E1	G7	VDD_3P3_IN	Input to internal regulators	I, P	–	–	1.65–3.6V
E3	F4	VDD_AUX_IN	Aux LDO input	I, P	–	–	LDO to power TCXO or external LNA or both
D3	G4	VDD1P8_AUX	Aux LDO output	O, P	–	–	Requires 1–2.2 µF output capacitor.
D1	G6	VDD1P1_CORE	Output of core LDO	O, P	–	–	Requires 1–2.2 µF output capacitor.
E2	G5	VDD1P2_GRF	Output of RF LDO	O, P	–	–	Requires 1–2.2 µF output capacitor.
D2	F5	VSS_PMU	PMU ground	G	–	–	–
C2	F6	REF_CAP	Reference filter capacitor	–	–	–	Connect a 10 nF capacitor to GND
E5	E2	VDD_GPS_IF	IF supply	I, P	–	–	–
C6	E1	VSS_GPS_IF	IF ground	G	–	–	–
E6	F2	VDD_GPS_LNA	LNA supply	I, P	–	–	–
D5	G1	VSS_GPS_LNA	LNA ground	G	–	–	–
–	F3	VDD_GPS_PLL	–	–	–	–	–
–	G2	VSS_GPS_PLL	–	–	–	–	–
C1	C4, E7	VDD_CORE	Core supply	I, P	–	–	–
B4, C4	D5, D6, E4, E5	VSS_CORE	Core ground	G	–	–	–
A4	D4, E6	VDD_IO	I/O supply	I, P	–	–	–
C3	F7	CLK_REQ	External AUX LDO enable	I	Hi-Z/ PMUPD	High	–

Table 11: BCM4752 Pinouts (Cont.)

Pin		Name	Description	Type	Standby State and Pull Resistor	Active Level	Comment
WLBGA	FBGA						
Reserved							
–	B4	RESERVED10	–	–	–	–	Reserved. Leave reserved pins floating.
–	C7	RESERVED7	–	–	–	–	
–	C6	RESERVED9	–	–	–	–	
–	C5	RESERVED8	–	–	–	–	
–	B7	RESERVED11	–	–	–	–	
–	D3	RESERVED0	–	–	–	–	
–	D2	RESERVED1	–	–	–	–	
–	D1	RESERVED2	–	–	–	–	
–	C2	RESERVED3	–	–	–	–	
–	C3	RESERVED4	–	–	–	–	
–	B3	RESERVED5	–	–	–	–	
–	A3	RESERVED6	–	–	–	–	

a. Use of this pin is optional. This pin is not used in a 2-wire UART interface.

Table 12 lists the pull-up/pull-down values for the BCM4752 and the PMU.

Table 12: Pull-Up/Pull-Down Values

Pull-Up/Pull-Down	*Minimum*	*Typical*	*Maximum*	*Unit*
PD/PU	38	45	51.5	kΩ
PMUPD	–	5	–	MΩ

Ballout

Figure 18 shows a top view of the 30-pin WLBGA ballout.

	1	2	3	4	5	6	
A	UART_RXD/ SDA	UART_TXD SCL	IFVALID	VDD_IO	GPS_CAL	CLK32	A
B	UART_NRTS/ HOST_REQ	UART_NCTS/ ANT_SEL	NSTANDBY	VSS_CORE	SYNC/ PPS	LNA_EN/ CAL_REQ	B
C	VDD_CORE	REF_CAP	CLK_REQ	VSS_CORE	TM0	VSS_GPS_IF	C
D	VDD1P1_CORE	VSS_PMU	VDD1P8_AUX	GPS_TEST_OUT	VSS_GPS_LNA	GPS_RFIN	D
E	VDD_3P3_IN	VDD1P2_GRF	VDD_AUX_IN	GPS_TCXO	VDD_GPS_IF	VDD_GPS_LNA	E
	1	2	3	4	5	6	

Figure 18: BCM4752 WLBGA Ballout Array (Top View)

Figure 19 shows a top view of the 49-pin FBGA ballout.

	1	2	3	4	5	6	7	
A	GPS_CAL	CLK32	RESERVED6	IFVALID	UART_TXD/SCL	UART_NCTS/ ANT_SEL	UART_RXD/ SDA	A
B	SYNC/PPS	LNA_EN/CAL_REQ	RESERVED5	RESERVED10	NSTANDBY	UART_NRTS/ HOST_REQ	RESERVED11	B
C	TM0	RESERVED3	RESERVED4	VDD_CORE	RESERVED8	RESERVED9	RESERVED7	C
D	RESERVED2	RESERVED1	RESERVED0	VDD_IO	VSS_CORE	VSS_CORE	NRESET	D
E	VSS_GPS_IF	VDD_GPS_IF	GPS_TEST_OUT	VSS_CORE	VSS_CORE	VDD_IO	VDD_CORE	E
F	GPS_RFIN	VDD_GPS_LNA	VDD_GPS_PLL	VDD_AUX_IN	VSS_PMU	REF_CAP	CLK_REQ	F
G	VSS_GPS_LNA	VSS_GPS_PLL	GPS_TCXO	VDD1P8_AUX	VDD1P2_GRF	VDD1P1_CORE	VDD_3P3_IN	G
	1	2	3	4	5	6	7	

Figure 19: BCM4752 FBGA Ballout Array (Top View)

Section 7: Electrical Characteristics

Absolute Maximum Ratings

Absolute maximum ratings for the BCM4752 are defined in Table 13.

Table 13: Absolute Maximum Ratings

Description	*Signal/Parameter*	*Value*	*Unit*
PMU input voltage	VDD_3P3_IN	3.63	V
AUX LDO input voltage	VDD_AUX_IN	5.5	V
DC supply to core	VDD_CORE	1.26	V
DC supply to RF	VDD_GPS_LNA, VDD_GPS_IF, VDD_GPS_PLL	1.32	V
DC supply to I/O	VDD_IO	3.63	V
Maximum voltage on input or output pins (VDD_IO Domain)	VImax	VDD_IO + 0.3	V
Minimum voltage on input or output pins (VDD_IO Domain)	VImin	– 0.3	V
Maximum voltage on CLK_REQ input	CLK_REQ	3.63	V
Maximum RF input power	GPS_RFIN	–10	dBm
Maximum voltage on TCXO input	GPS_TCXO	4.1	V
Maximum voltage on RF input	GPS_RFIN	0.8	V
Operating Temperature	–	–35 to +85	°C
Storage temperature	–	–40 to +125	°C
ESD Human Body Model (HBM), EIA/JESD22-A114, VESDHBM (WLBGA)	–	±2000	V
ESD Machine Model (MM), EIA/JESD22-A115, VESDMM (WLBGA)	–	±100	V
ESD Charge Device Model (CDM), JESD22-C101, VESDCDM (WLBGA)	–	±300	V
ESD Human Body Model (HBM), EIA/JESD22-A114, VESDHBM (FBGA)	–	±2000	V
ESD Machine Model (MM), EIA/JESD22-A115, VESDMM (FBGA)	–	±100	V
ESD Charge Device Model (CDM), JESD22-C101, VESDCDM (FBGA)	–	±150	V

Recommended Operating Conditions

Recommended operating conditions for the BCM4752 are provided in Table 14.

Table 14: Recommended Operating Conditions

Signal/Parameter	*Minimum*	*Typical*	*Maximum*	*Unit*
VDD_3P3_IN	1.62	–	3.63	V
VDD_IO	1.65	–	3.63	V
Temp	–30	+25	+85	°C
VDD_AUX_IN	2.3	–	4.8	V

Digital I/O Specifications

I/O digital specifications for the BCM4752 are defined in Table 15. The I/O pins relevant for Table 15 are listed below:

- CLK_REQ
- GPS_CAL/CLK32
- IFVALID
- LNA_EN/CAL_REQ
- NSTANDBY
- SYNC/PPS
- TM0
- UART_NCTS/ANT_SEL
- UART_NRTS/HOST_REQ
- UART_RXD/SDA
- UART_TXD/SCL

Note: –30°C ≤ +$T_{AMBIENT}$ ≤ 85°C

Table 15: BCM4752 I/O Digital Specifications

			Value		
Symbol	***Parameter***	***Conditions***	***Min***	***Max***	***Unit***
V_{IL}	Input low voltage	1.65V ≤ VDD_IO ≤ 1.95V	–0.3	0.35 × VDD_IO	V
		2.3V ≤ VDD_IO ≤ 2.7V	–0.3	0.7	
		3.0V ≤ VDD_IO ≤ 3.63V	–0.3	0.8	
V_{IH}	Input high voltage	1.65V ≤ VDD_IO ≤ 1.95V	0.65 × VDD_IO	VDD_IO + 0.3	V
		2.3V ≤ VDD_IO ≤ 2.7V	1.7	VDD_IO + 0.3	
		3.0V ≤ VDD_IO ≤ 3.63V	2	VDD_IO + 0.3	
V_{OL}	Output low voltage	I_{OL} = 2 mA			V
		1.65V ≤ VDD_IO ≤ 1.95V	–	0.45	
		2.3V ≤ VDD_IO ≤ 2.7V	–	0.7	
		3.0V ≤ VDD_IO ≤ 3.63V	–	0.4	
V_{OH}	Output high voltage	I_{OH} = –2 mA			V
		1.65V ≤ VDD_IO ≤ 1.95V	VDD_IO – 0.45	–	
		2.3V ≤ VDD_IO ≤ 2.7V	1.7	–	
		3.0V ≤ VDD_IO ≤ 3.63V	2.4	–	
I_{IN}	Input current	VDD_IO = 3.63V, VIN = GND or VDD_IO	–	±5	µA
C_{IN}	Input capacitance	–	–	7	pf
–	CLK_REQ enable	1.62V ≤ VDD_IO ≤ 3.63V	0.65 × VDD_IO	3.63	V
–	CLK_REQ disable	1.62V ≤ VDD_IO ≤ 3.63V	–0.3	0.31	V

Maximum Current Consumption

The amount of power consumed by the BCM4752 depends on the operating environment, the power mode, and the associated number of correlation channels that are active at any time. A specific application note that details BCM4752 power consumption under typical use cases is being developed. For the purpose of this document, only the maximum current levels (peak and average) are specified in Table 16. These values are intended to help estimate the required size of the external regulators or power supplies.

Table 16: DC Characteristics—Current

Parameter [a]	*Conditions*		*Typical* [b]	*Maximum* [c]	*Units*
VDD_IO current	VDD_IO = 1.65V to 3.63V T_A = –30°C to +85°C	Active	80	440	µA
		Standby	1.3	3.1	
VDD_3P3_IN current	VDD_3P3_IN = 1.62V to 3.63V	Active	47 (Average)	55 (Peak)	mA
		Standby	0.03	1	µA

a. The information in this table is intended as a guide for sizing power supplies only, and should not be used for determining average power consumption.
b. Conditions for typical values: VDD_IO = 1.8V; TA = 25°C; TCXO frequency = 26 MHz; UART interface @ 115,200 baud.
c. Conditions for maximum values: VDD_IO = 3.6V; TA = 85°C; TCXO = 40 MHz; UART @ 921,600; GPS_CAL = 40 MHz.

BSC Host Interface Specifications

- Operates at up to 400 kHz
- Default address 0x1FA
- 10-bit (default) and 7-bit addressing modes
- Operates as a slave only

BSC timing specifications are defined in Table 17 and Figure 20 on page 39.

Note: The parameters in Table 17 are guaranteed by design, not characterization.

Table 17: BSC Timing Specifications

		Fast Mode[a]			
Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
SCL clock frequency	fSCL	0	–	400	kHz
Bus-free times between a stop and start condition	tBuf	1.3	–	–	µs
Hold time (repeated) start condition. After this period, the first clock pulse is generated.	tHD,STA	0.6	–	–	µs
Low period of the SCL clock	tLOW	1.3	–	–	µs
High period of the SCL clock	tHIGH	0.6	–	–	µs
Set-up time for a repeated start condition	tSU, STA	0.6	–	–	µs
Data hold time	tHD, DAT	0[b]	–	0.9[c]	µs
Data setup time	tSU, DAT	100[d]	–	–	ns
Setup time for stop condition	tSU, STOP	0.63	–	–	µs
Pulse width of spikes suppressed by the input filter	tSP	0	–	10	ns

a. All timing values are referenced to minimum (V_{IH}) and maximum (V_{IL}) levels, and were obtained over process, voltage, and temperature.

b. A device must internally provide a hold time of at least 300 ns for the serial data (SDA) signal to bridge the undefined region of serial clock line (SCL).

c. This must be met because the BCM4752 does not stretch the LOW period of the SCL signal.

d. A Fast-mode device can be used in Standard mode, but the requirement $T_{SU,DAT}$ > 250 ns must be met. This automatically applies because the BCM4752 does not stretch the LOW period of the SCL signal.

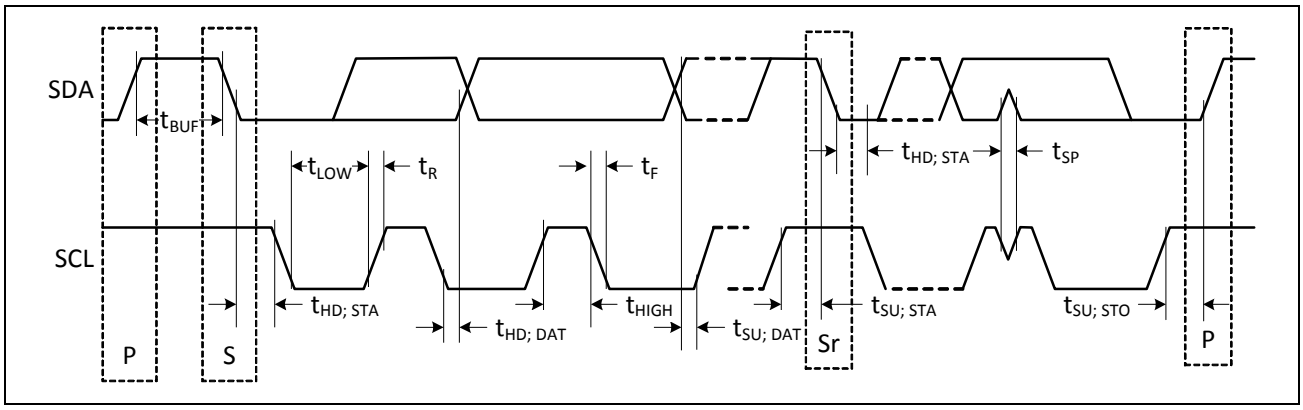
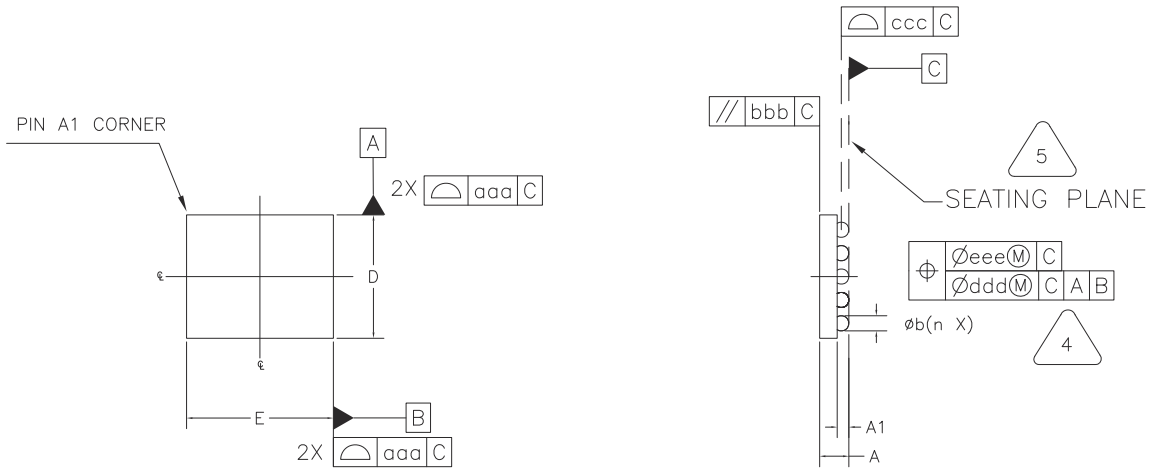
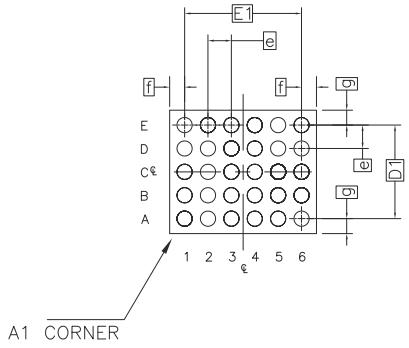


Figure 20: BSC Timing Diagram

Section 8: Mechanical Specifications





DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	2.02	2.07	2.12
D1		1.60 BSC	
E	2.42	2.47	2.52
E1		2.00 BSC	
b	0.200	0.250	0.300
e		0.40 BSC	
f		0.235 BSC	
g		0.235 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.05
n	–	30	–

Filename: MOD01594 Rev. 000

6. REFER TO BROADCOM APPLICATION NOTE "WAFER–LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5 PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

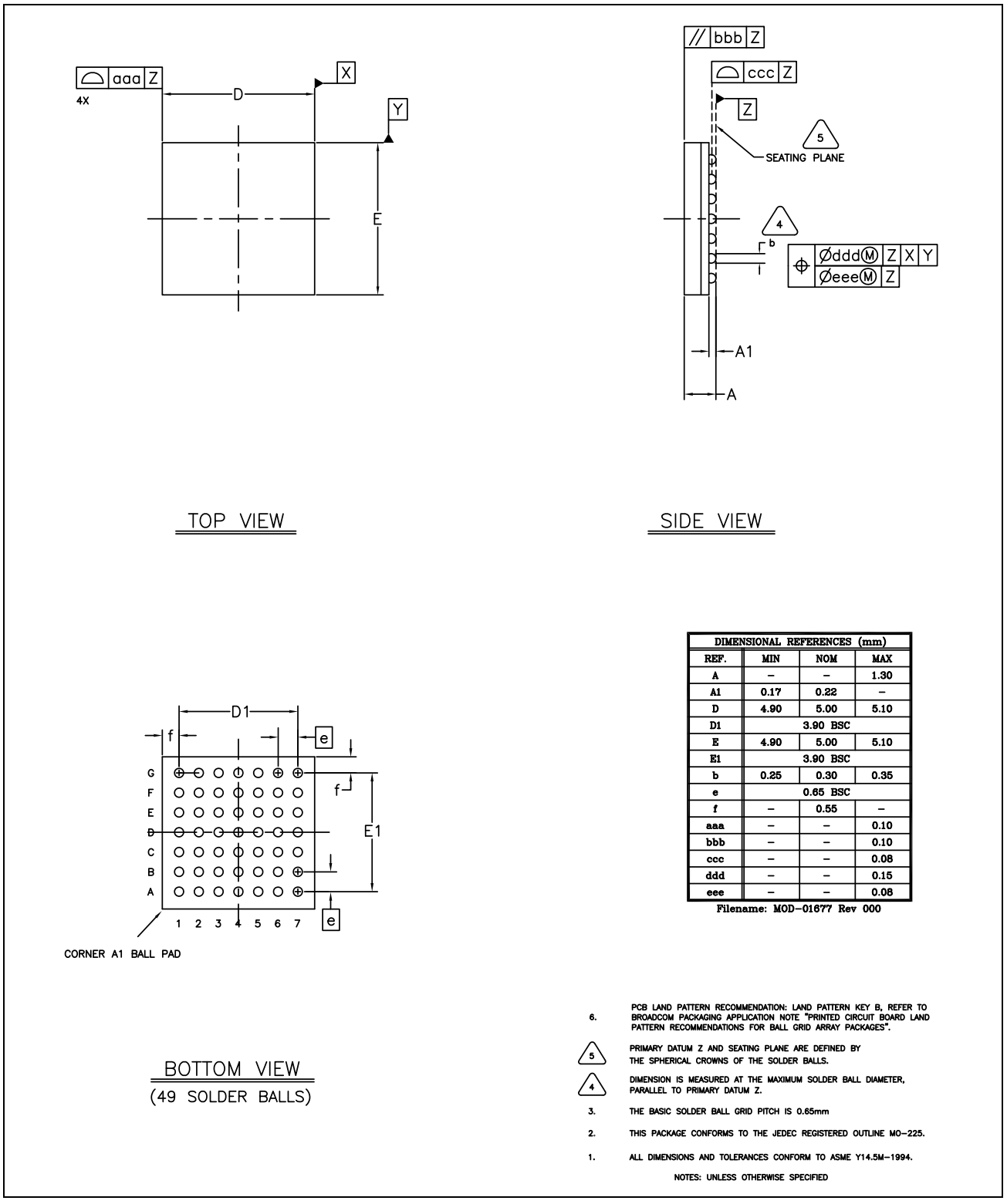
4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM C.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–211.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994 UNLESS OTHERWISE SPECIFIED

Figure 21: Outline Dimensions of the 30-Pin WLBGA Package



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.30
A1	0.17	0.22	–
D	4.90	5.00	5.10
D1		3.90 BSC	
E	4.90	5.00	5.10
E1		3.90 BSC	
b	0.25	0.30	0.35
e		0.65 BSC	
f	–	0.55	–
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD–01677 Rev 000

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY B, REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES".

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.65mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 22: Outline Dimensions of the 49-Pin FBGA Package

Section 9: Ordering Information

Table 18: Ordering Information

Part Number	*Package*	*Packing*	*Minimum Order Quantity*
BCM4752IUB2G[a]	30-pin WLBGA	Tape-and-reel	5000
BCM4752IFBG	49-pin FBGA	Tape-and-reel	2500

a. Backside lamination

Connecting everything®

BROADCOM CORPORATION
5300 California Avenue
Irvine, CA 92617

Phone: 949-926-5000
Fax: 949-926-5203
E-mail: info@broadcom.com
Web: www.broadcom.com

4752-DS103-R September 26, 2012