BCM4359

Single-Chip 5G WiFi IEEE 802.11ac 2 × 2 MAC/Baseband/ Radio with Integrated Bluetooth 4.2/RSDB

GENERAL DESCRIPTION

The Broadcom® BCM4359 is a dual-band (2.4 GHz and 5 GHz) IEEE 802.11ac 2×2 MIMO MAC/PHY/ Radio System-on-a-Chip. This single-chip device provides a high level of integration with dual-stream IEEE 802.11ac MAC/baseband/radio and Bluetooth 4.2. In IEEE 802.11ac mode, WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. In addition, all the rates specified in IEEE 802.11a/b/g/n are supported. External PAs, LNAs, and antenna diversity are also supported. The WLAN core supports two fully simultaneous SISO channels (real simultaneous dual-band, or RSDB).

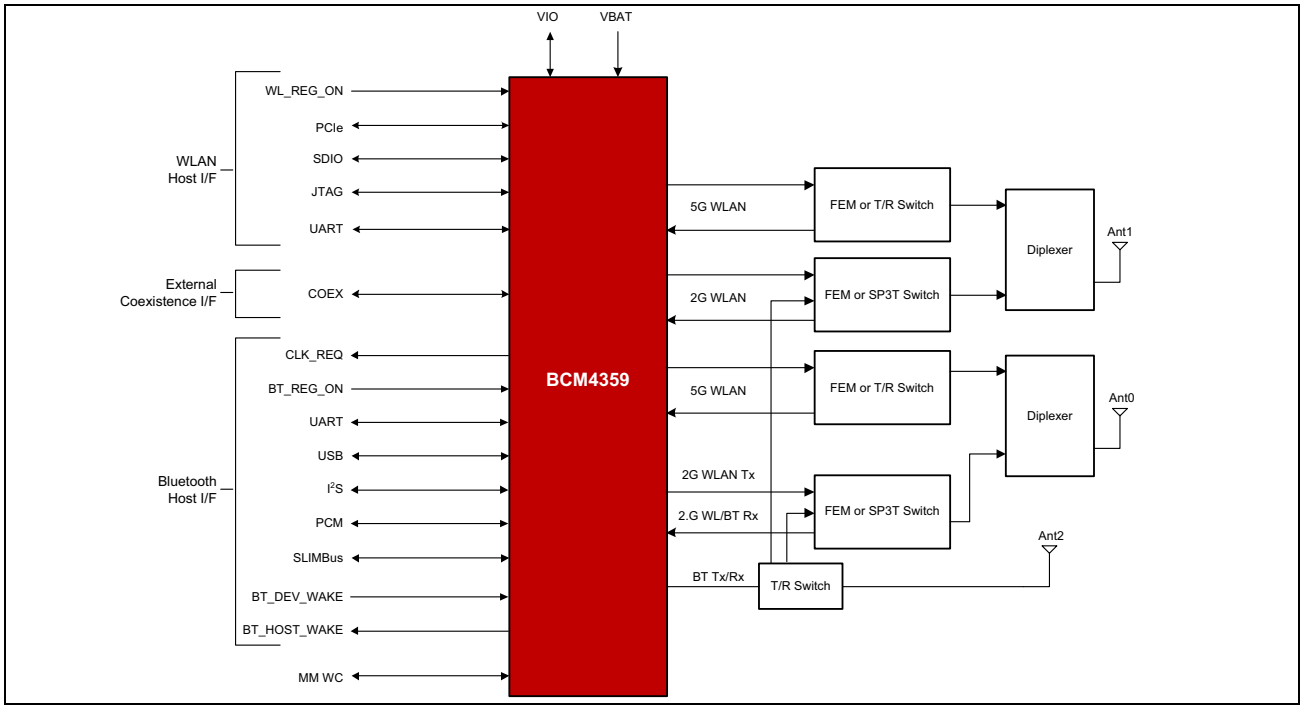
For the WLAN section, several host interface options are included: an SDIO v3.0 interface that can operate in 4b or 1b modes, high-speed 4-wire UART, and a PCIe v3.0-compliant interface running at Gen1 speeds. For the Bluetooth section, host interface options of a high-speed 4-wire UART and USB 2.0 full-speed (12 Mbps) are provided.

GENERAL DESCRIPTION

The BCM4359 uses advanced design techniques and process technology to reduce active and idle power, and includes an embedded power management unit that simplifies the system power topology.

In addition, the BCM4359 implements highly sophisticated enhanced collaborative coexistence mechanisms to optimize WLAN and Bluetooth coexistence. Coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface.

Figure 1: BCM4359 Functional Block Diagram



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FEATURES

IEEE 802.11X Key Features

- IEEE 802.11ac compliant.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- IEEE 802.11ac/n beamforming.
- Real simultaneous dual-band (RSDB).
- On-chip power amplifiers and low–noise amplifiers for both bands and support for external LNAs.
- Supports three antennas with one dedicated to Bluetooth and two to WLAN. Also, shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE and GPS.
- Supports standard SDIO v3.0 (up to SDR104 mode at 208 MHz, 4-bit and 1-bit) host interfaces.
- Backward compatible with SDIO v2.0 host interfaces.
- PCIe mode complies with PCI Express base specification revision 3.0 for ×1 lane and power management running at Gen1 speeds.
- Integrated ARMCR4 processor and memory minimizing the use of applications processor for standard WLAN functions. On-chip memory includes 768 KB SRAM and 768 KB ROM. This minimizes power consumption, while maintaining field upgrade capability.

Bluetooth Key Features

- Complies with Bluetooth Core Specification Version 4.2 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.

FEATURES

Bluetooth Key Features (Cont.)

- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support: host controller interface (HCI) using a USB or high-speed UART interface and PCM for audio data.
- USB 2.0 full-speed (12 Mbps) supported for Bluetooth.
- Low power consumption improves battery life of handheld devices.
- Automatic frequency detection for standard crystal and TCXO values.
- Supports serial flash interfaces.

General Features

- Supports battery range from 3.0V to 4.8V supplies with internal switching regulator.
- Programmable dynamic power management
- Supports 1410 bytes of user-accessible OTP, of which 256 bytes are allocated for BT and 1150 bytes are allocated for WLAN for storing board parameters.
- GPIOs: 20
- Security:
  - WPA and WPA2 (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0)
  - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Package:
  - 194-ball WLBGA (4.97 mm × 7.50 mm, 0.4 mm pitch)
- 397-bump WLCSP (4.97 mm × 7.50 mm, 0.2 mm pitch)
- Worldwide regulatory support: Global products supported with worldwide homologated design.

Revision History

Revision	*Date*	*Change Description*
4359-DS106-R	03/11/15	**Updated:** • The BCM4359 now supports Bluetooth 4.2. • "General Features" on page 2: WLAN OTP size. • Table 4: "External 32.768 kHz Sleep Clock Specifications," on page 26. • Table 21: "BCM4359 WLCSP Signal Descriptions," on page 103. • Table 30: "Environmental Ratings," on page 128. • Figure 32: "Port Locations (Applies to 2.4 GHz)," on page 139. • Figure 33: "Port Locations (Applies to 5 GHz)," on page 139. • Table 38: "WLAN 2.4 GHz Receiver Performance Specifications," on page 141. • Table 39: "WLAN 2.4 GHz Transmitter Performance Specifications," on page 145. • Table 40: "WLAN 5 GHz Receiver Performance Specifications," on page 147. • Table 41: "WLAN 5 GHz Transmitter Performance Specifications," on page 153. • Table 51: "Typical WLAN Power Consumption," on page 163. • Figure 53: "WLCSP Keep-Out Areas for PCB Layout (Top View, Balls Facing Down)," on page 188. • Table 64: "Ordering Information," on page 189. **Removed:** • Appendix A: "Pin Lists," on page 177: this information was consolidated in Section 12: "Pinout and Signal Descriptions," on page 71.

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Revision	*Date*	*Change Description*
4359-DS105-R	01/12/14	**Updated:** • "Standards Compliance" on page 27. • Figure 9: "Typical Power Topology (1.2V)," on page 29. • Figure 10: "Typical Power Topology (2.5V and 3.3V)," on page 30. • Table 5: "External 32.768 kHz Sleep Clock Specifications," on page 37. • "WLAN CPU and Memory Subsystem" on page 66. • "IEEE 802.11ac PHY" on page 79. • Table 69: "Part Ordering Information," on page 204.
4359-DS104-R	12/19/14	Refer to the release for revision history details.
4359-DS103-R	10/27/14	Refer to the release for revision history details.
4359-DS102-R	09/10/14	Refer to the release for revision history details.
4359-DS101-R	04/8/14	Refer to the release for revision history details.
4359-DS100-R	02/25/14	Initial release.

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About This Document

Purpose and Audience

This data sheet provides details on the functional, operational, and electrical characteristics for the Broadcom® BCM4359. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

References

The references in this section may be used in conjunction with this document.

Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	*Number*	*Source*
[1] Bluetooth MWS Coexistence 2–wire Transport Interface Specification	–	www.bluetooth.com

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads and Support site (http://www.broadcom.com/support/).

Section 1: Overview

Overview

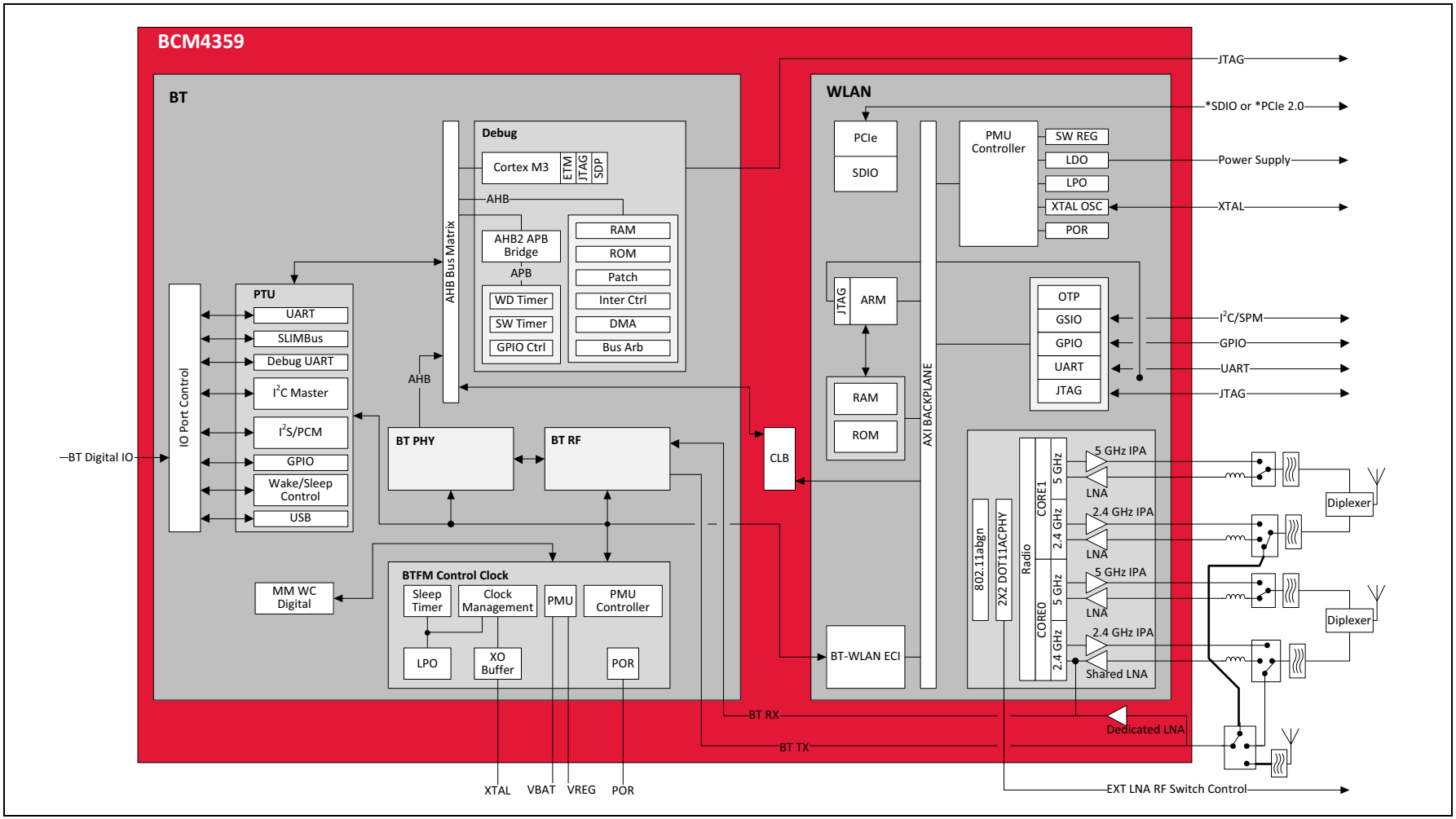
The Broadcom® BCM4359 single-chip device includes integrated IEEE 802.11 a/b/g/n/ac MAC/baseband/radio (dual-core 2×2 MIMO), Bluetooth 4.2+/BLE/multimode wireless charging (MM WC) with enhanced data rate (EDR). It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Table 1: Device Options and Features

Feature	*WLCSP*	*WLBGA*
Package ball count	397 bumps	194 balls
PCIe	Yes	Yes
USB 2.0 (Bluetooth)	Yes	Yes
I^2S	Yes	Yes
GPIO	20	20
SDIO 3.0	Yes	Yes

Figure 2 on page 16 shows the interconnect of all the major physical blocks in the BCM4359 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2: BCM4359 Block Diagram



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Standards Compliance

The BCM4359 supports the following standards:

- Bluetooth 2.1 + EDR, 3.0, Bluetooth 4.2
- IEEE 802.11ac mandatory and optional requirements for 20 MHz, 40 MHz, and 80 MHz channels
- IEEE 802.11a/b/g/n
- IEEE 802.11d/h
- IEEE 802.11i
- Security:
  - WEP, WPA/WPA2 personal, WMM, WMM-PS (U-APSD), WMM-SA, AES (hardware accelerator), TKIP (hardware accelerator), and CKIP (software support)
- Proprietary protocols:
  - CCXv2, CCXv3, and CCXv4

The BCM4359 will support the following future drafts/standards:

- IEEE 802.11r (fast roaming between APs)
- IEEE 802.11w (secure management frames)
- IEEE 802.11 extensions:
  - IEEE 802.11e QoS enhancements (In accordance with the WMM specification, QoS is already supported.)
  - IEEE 802.11h 5 GHz extensions
  - IEEE 802.11i MAC enhancements
  - IEEE 802.11k radio resource measurement

Section 2: Power Supplies and Power Management

Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the BCM4359. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

A single VBAT (3.0V to 4.8V DC max) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the BCM4359.

Three control signals, BT_REG_ON, WL_REG_ON, and WPT_REG_ON (that is, WPT_1P8), are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted and the wireless supplies (that is, WPT_1P8/WPT_3P3) are not available. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

The BCM4359 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, MEMLPLDO and LPLDO (which is a low-power linear regulator supplied by the system VIO supply) provide the BCM4359 with all the voltages it requires, further reducing leakage currents.

BCM4359 PMU Features

- VBAT to 1.35Vout (600 mA maximum) core-buck (CBUCK) switching regulator
- VBAT to 3.3Vout (650 mA maximum) PALDO3P3
- VBAT to 3.3Vout (200 mA maximum) LDO3P3
- VBAT to 2.5V out (70 mA maximum) BTLDO2P5
- 1.35V to 1.2Vout (150 mA maximum) LNLDO
- 1.35V to 1.2Vout (420 mA maximum) CLDO with bypass mode for deep-sleep
- 1.35V to 1.2Vout (100 mA maximum) HLDO
- VDDIO to 0.9Vout (10 mA maximum) MEMLPLDO
- VDDIO to 1.1Vout (3 mA maximum) LPLDO
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from extremely low power-consumption mode
- PMU input supplies automatic sensing and fast switching to support MM WC operations

Figure 3 and Figure 4 on page 20 illustrate the typical power topology for the BCM4359. The shaded areas are external to the BCM4359.

Figure 3: Typical Power Topology (1.2V)

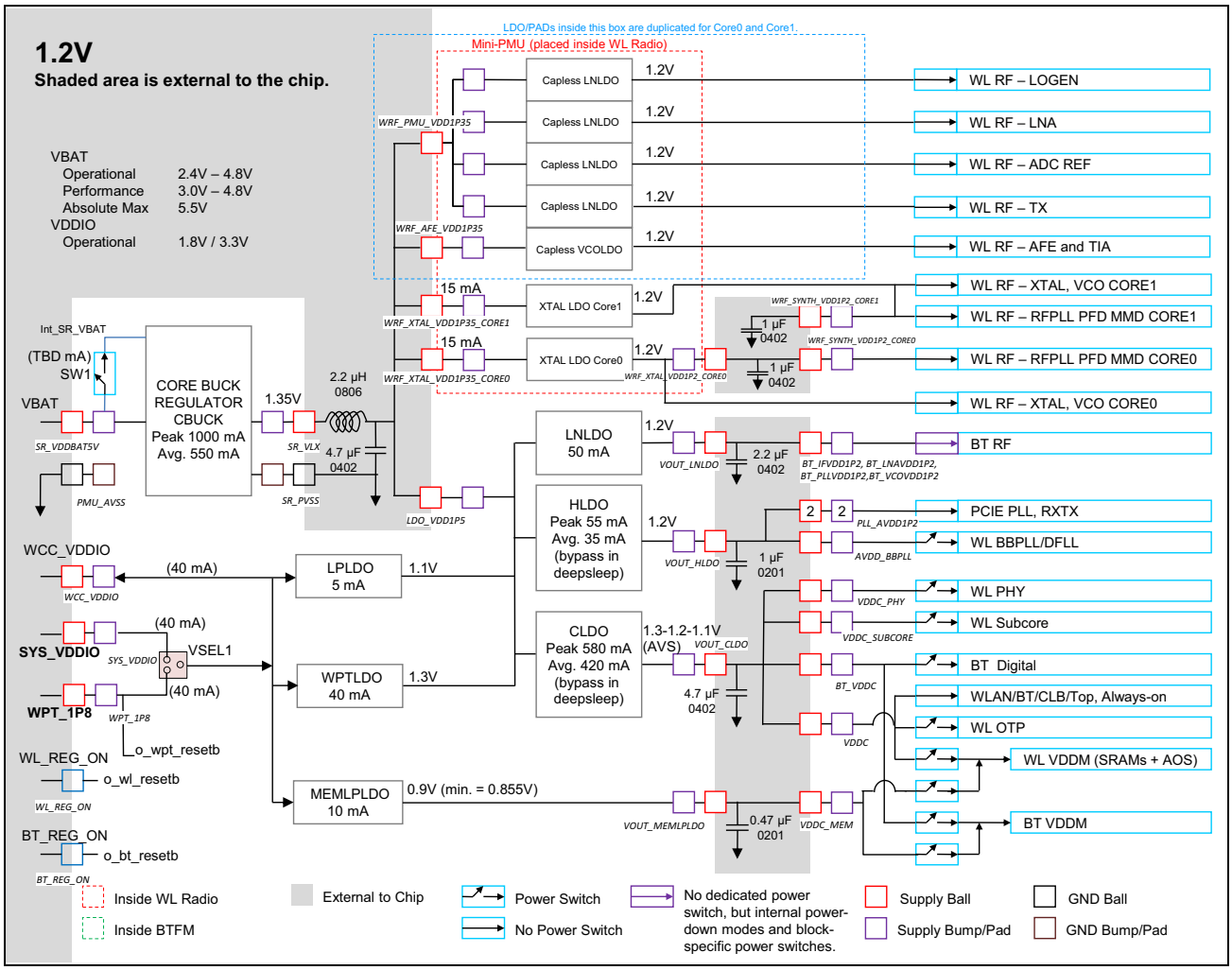
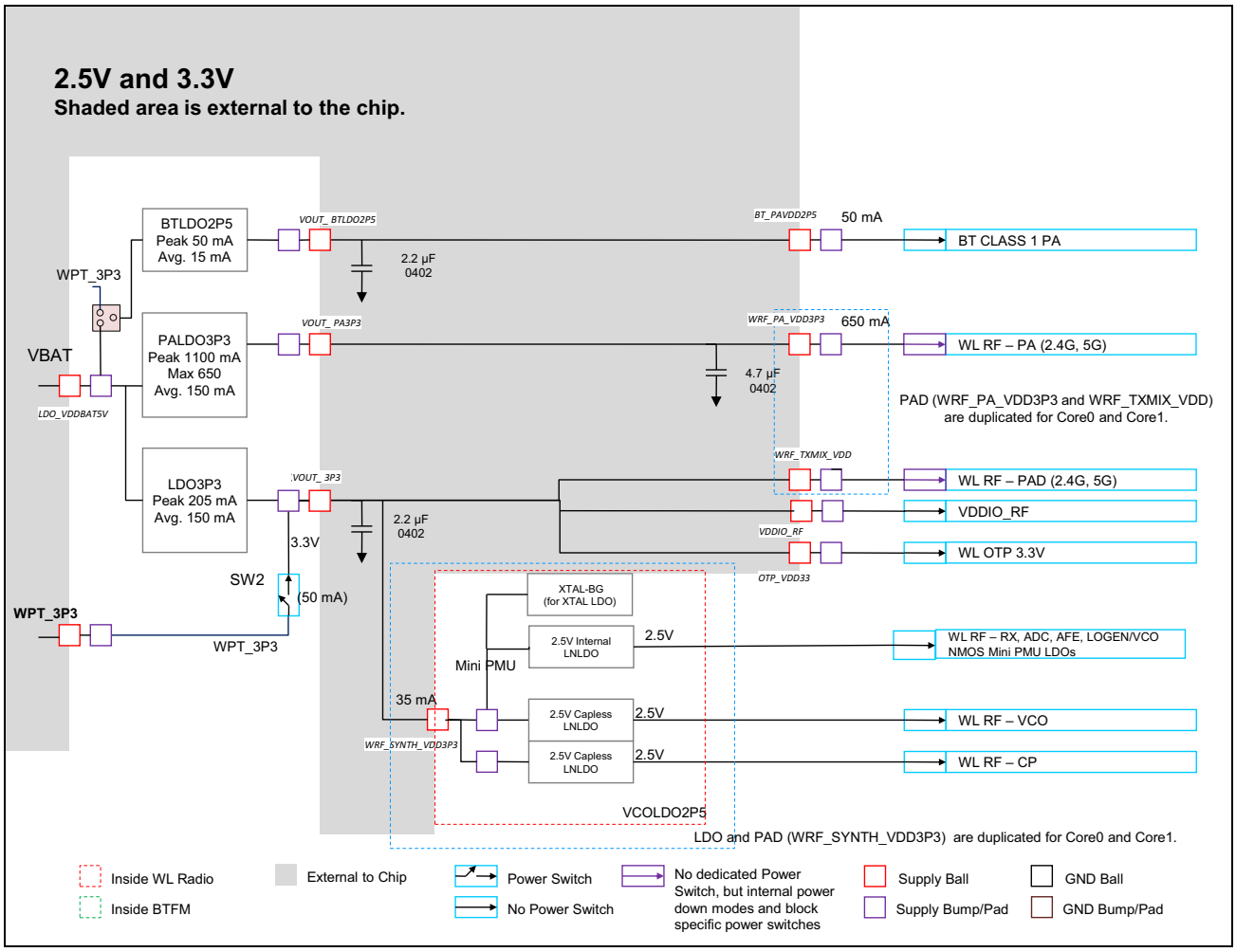


Figure 4: Typical Power Topology (2.5V and 3.3V)



WLAN Power Management

The BCM4359 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM4359 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the BCM4359 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM4359 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM4359 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the BCM4359 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Deep-sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization. In Deep-sleep mode, the primary source of power consumption is leakage current.
- Power-down mode—The BCM4359 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Power-Off Shutdown

The BCM4359 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the BCM4359 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the BCM4359 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to the BCM4359, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the BCM4359 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the BCM4359 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

Power-Up/Power-Down/Reset Circuits

The BCM4359 has two signals (see Table 2) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 19: “Power-Up Sequence and Timing,” on page 178.

Table 2: Power-Up/Power-Down/Reset Control Signals

Signal	*Description*
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM4359 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal BCM4359 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

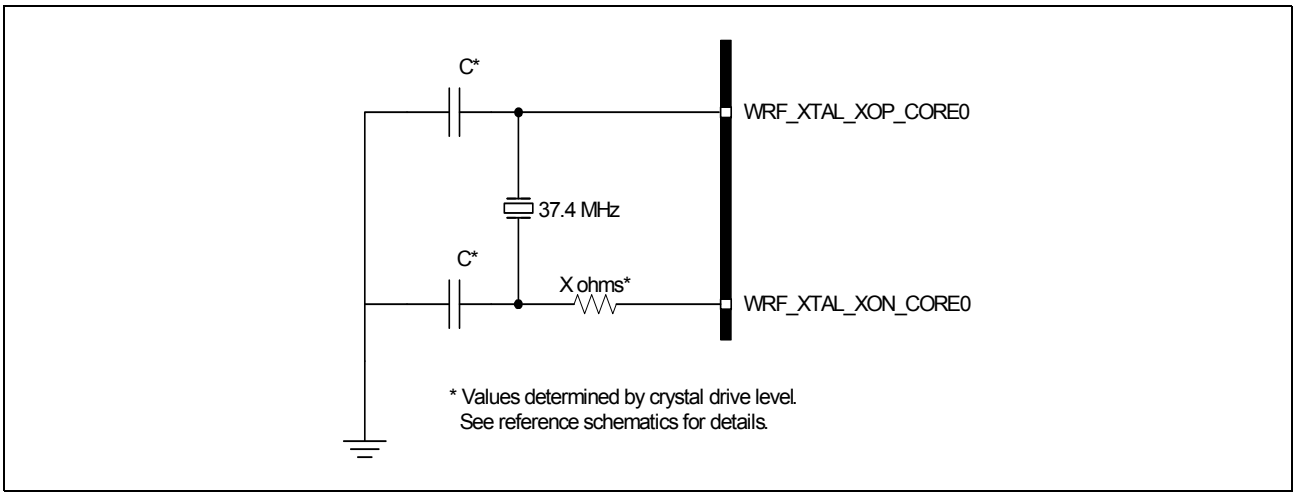
Section 3: Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Crystal Interface and Clock Generation

The BCM4359 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5: Recommended Oscillator Configuration



A fractional-N synthesizer in the BCM4359 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

For SDIO and PCIe WLAN host applications, the recommended default frequency reference is a 37.4 MHz crystal. For PCIe applications, see Table 3 on page 24 for details on alternatives for the external frequency reference. The signal characteristics for the crystal oscillator interface are also listed in Table 3.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Broadcom for further details.

External Frequency Reference

For operation in SDIO modes only, an alternative to a crystal (an external precision frequency reference) can be used. The recommended default frequency is 52 MHz ±10 ppm, and it must meet the phase noise requirements listed in Table 3.

If used, the external clock should be connected to the WRF_XTAL_XOP_CORE0 pin through an external 1000 pF coupling capacitor, as shown in Figure 6. The internal clock buffer connected to this pin will be turned OFF when the BCM4359 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P5 pin.

Figure 6: Recommended Circuit to Use with an External Reference Clock

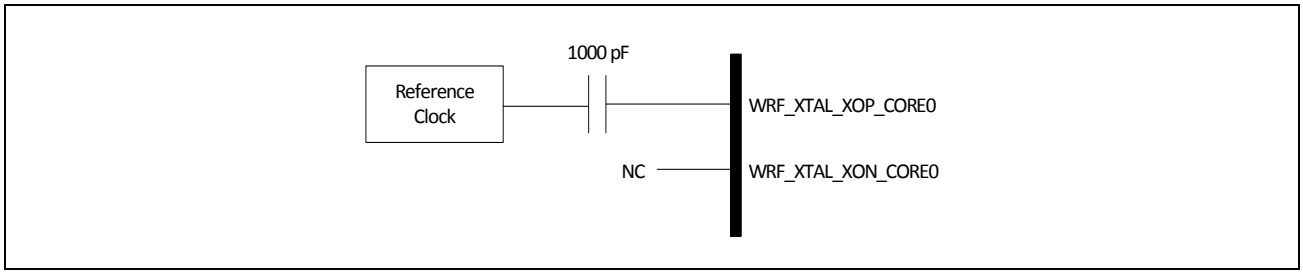


Table 3: Crystal Oscillator and External Clock—Requirements and Performance

		Crystal[a]			*External Frequency Reference*[b,c]			
Parameter	***Conditions/Notes***	***Min.***	***Typ.***	***Max.***	***Min.***	***Typ.***	***Max.***	***Units***
Frequency	2.4G and 5G bands: IEEE 802.11ac operation, SDIO3.0, and PCIe WLAN interfaces	35	37.4	–	–	52	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[d]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_XOP_CORE0)	Resistive	–	–	–	30	100	–	kΩ
	Capacitive	–	–	7.5	–	–	7.5	pF
WRF_XTAL_XOP_CORE0 Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_XOP_CORE0 Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V

Table 3: Crystal Oscillator and External Clock—Requirements and Performance (Cont.)

		Crystal[a]			External Frequency Reference[b,c]			
Parameter	**Conditions/Notes**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
WRF_XTAL_XOP_CORE0 input voltage (see Figure 6)	AC-coupled analog signal	–	–	–	400	–	1200	mV_{p-p}
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[e] (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase Noise[e] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–144	dBc/Hz
Phase Noise[e] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise[e,f] (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/Hz
Phase Noise[e] (IEEE 802.11ac, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–148	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–157	dBc/Hz

a. (Crystal) Use WRF_XTAL_XOP_CORE0 and WRF_XTAL_XON_CORE0.
b. See "External Frequency Reference" on page 24 for alternate connection methods.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
e. Assumes that external clock has a flat phase noise response above 100 kHz.
f. If the reference clock frequency is <35 MHz the phase noise requirements must be tightened by an additional 2 dB.

External 32.768 kHz Low-Power Oscillator

The BCM4359 uses a secondary low-frequency clock for Low-Power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz (± 30%) over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock which meets the requirements listed in Table 4.

Table 4: External 32.768 kHz Sleep Clock Specifications

Parameter	*LPO Clock*	*Unit*
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30 – 70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[a]	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	ppm

a. When power is applied or switched off.

Section 4: Bluetooth Subsystem Overview

The Broadcom BCM4359 is a Bluetooth 4.2 + EDR-compliant, baseband processor/2.4 GHz transceiver with an integrated dual-band radio. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth solution.

The BCM4359 is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high-speed UART and PCM for audio. The BCM4359 incorporates all Bluetooth 4.2 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume.

The BCM4359 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

Features

The major Bluetooth features include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.0 + EDR features:
  - Adaptive frequency hopping (AFH)
  - Quality of service (QoS)
  - Extended synchronous connections (eSCO)—Voice Connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure simple pairing (SSP)
  - Sniff subrating (SSR)
  - Encryption pause resume (EPR)
  - Extended inquiry response (EIR)
  - Link supervision timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.2 packet types
- Supports maximum Bluetooth data rates over HCI UART
- BT supports full-speed USB 2.0-compliant interface
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Broadcom fast connect (TBFC)

- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see “Host Controller Power Management” on page 33)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

Bluetooth Radio

The BCM4359 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmit

The BCM4359 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the BCM4359 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM4359 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM4359 uses an internal RF and IF loop filter.

Calibration

The BCM4359 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Section 5: Bluetooth Baseband Core

The Bluetooth baseband core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth 4.2 Features

The BBC supports all Bluetooth 4.2 features, with the following benefits:

- Dual-mode Bluetooth low energy (BT and BLE operation)
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision time out (LSTO): Additional commands added to HCI and link management protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

Bluetooth Low Energy

The BCM4359 supports the Bluetooth Low Energy operating mode.

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth link controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

Test Mode Support

The BCM4359 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test mode, the BCM4359 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Bluetooth Power Management Unit

The Bluetooth power management unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the BCM4359 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

Host Controller Power Management

When running in UART mode, the BCM4359 may be configured so that dedicated signals are used for power management hand-shaking between the BCM4359 and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation. Table 5 describes the power-control hand-shake signals used with the UART interface.

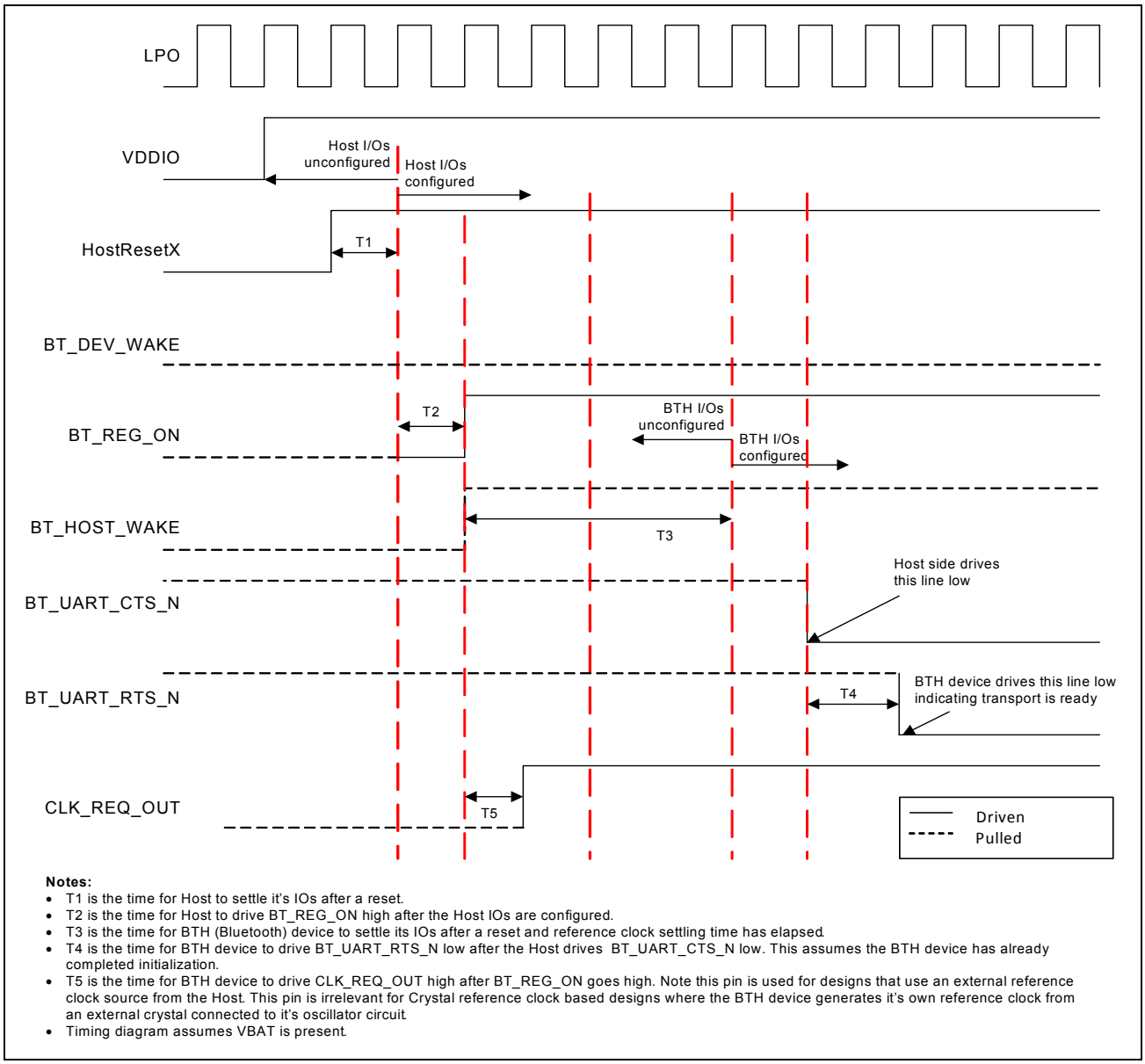
Table 5: Power Control Pin Description

Signal	*Mapped to Pin*	*Type*	*Description*
BT_DEV_WAKE	P5, 253	I	Bluetooth device wake-up: Signal from the host to the BCM4359 indicating that the host requires attention. • Asserted: The Bluetooth device must wake-up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	N4, 241	O	Host wake up. Signal from the BCM4359 to the host indicating that the BCM4359 requires attention. • Asserted: host device must wake-up or remain awake. • Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	N5, 233	O	The BCM4359 asserts CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The CLK_REQ polarity is active-high.

Note: Pad function Control Register is set to 0 for these pins. See "DC Characteristics" on page 127 for more details.

The timing for the startup sequence is defined in Figure 7.

Figure 7: Startup Signaling Sequence



Notes:

- T1 is the time for Host to settle it's IOs after a reset.
- T2 is the time for Host to drive BT_REG_ON high after the Host IOs are configured.
- T3 is the time for BTH (Bluetooth) device to settle its IOs after a reset and reference clock settling time has elapsed.
- T4 is the time for BTH device to drive BT_UART_RTS_N low after the Host drives BT_UART_CTS_N low. This assumes the BTH device has already completed initialization.
- T5 is the time for BTH device to drive CLK_REQ_OUT high after BT_REG_ON goes high. Note this pin is used for designs that use an external reference clock source from the Host. This pin is irrelevant for Crystal reference clock based designs where the BTH device generates it's own reference clock from an external crystal connected to it's oscillator circuit.
- Timing diagram assumes VBAT is present.

BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the BCM4359 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the BCM4359 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the BCM4359 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

  During the low-power shut-down state, provided VDDIO remains applied to the BCM4359, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the BCM4359 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

  Two BCM4359 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the BCM4359 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

Wideband Speech

The BCM4359 provides support for wideband speech (WBS) using on-chip SmartAudio® technology. The BCM4359 can perform subband codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The BCM4359 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 8 and Figure 9 show audio waveforms with and without Packet Loss Concealment. Broadcom PLC/BEC algorithms also support wide band speech.

Figure 8: CVSD Decoder Output Waveform Without PLC

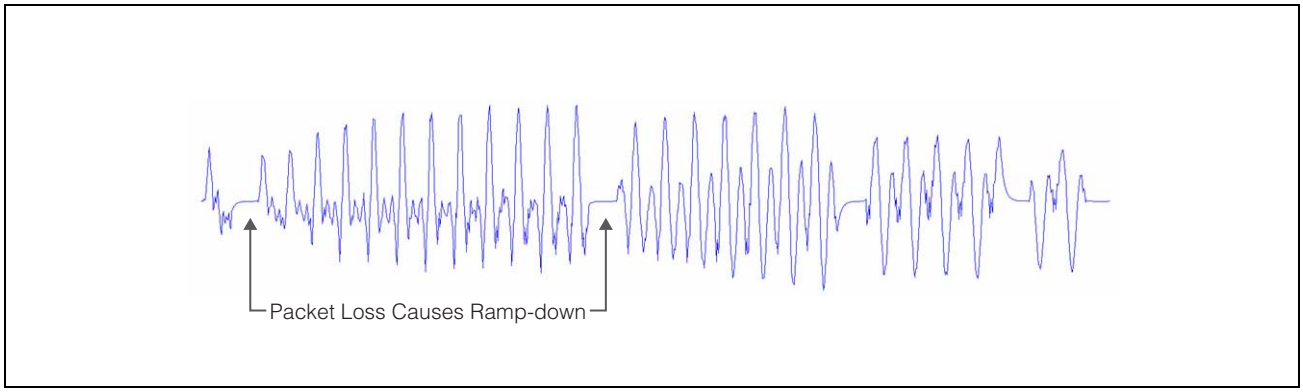
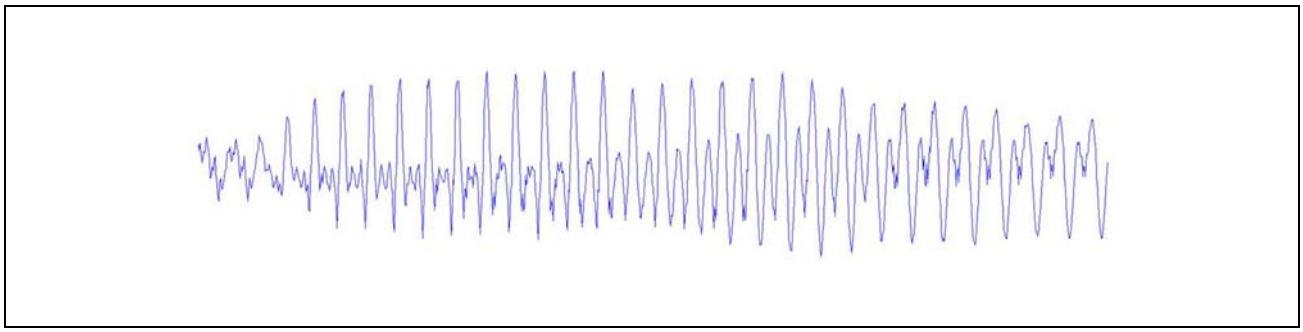


Figure 9: CVSD Decoder Output Waveform After Applying PLC



Audio Rate-Matching Algorithms

The BCM4359 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth data rates.

Codec Encoding

The BCM4359 can support SBC and mSBC encoding and decoding for wideband speech.

Multiple Simultaneous A2DP Audio Stream

The BCM4359 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

Burst Buffer Operation

The BCM4359 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

Adaptive Frequency Hopping

The BCM4359 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

Advanced Bluetooth/WLAN Coexistence

The BCM4359 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The BCM4359 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The BCM4359 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The BCM4359 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core’s channel information.

Fast Connection (Interlaced Page and Inquiry Scans)

The BCM4359 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

Section 6: Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 808 KB of ROM memory for program storage and boot ROM, 256 KB of RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the BCM4359 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the BCM4330 device.

RAM, ROM, and Patch Memory

The BCM4359 Bluetooth core has 256 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 808 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

Reset

The BCM4359 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

Section 7: Bluetooth Peripheral Transport Unit

PCM Interface

The BCM4359 supports two independent PCM interfaces that share the pins with the I^2S interfaces. The PCM Interface on the BCM4359 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM4359 generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM4359.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Slot Mapping

The BCM4359 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The BCM4359 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The BCM4359 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM4359 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

Wideband Speech Support

When the host encodes wideband speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The BCM4359 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

PCM Interface Timing

Short Frame Sync, Master Mode

Figure 10: PCM Timing Diagram (Short Frame Sync, Master Mode)

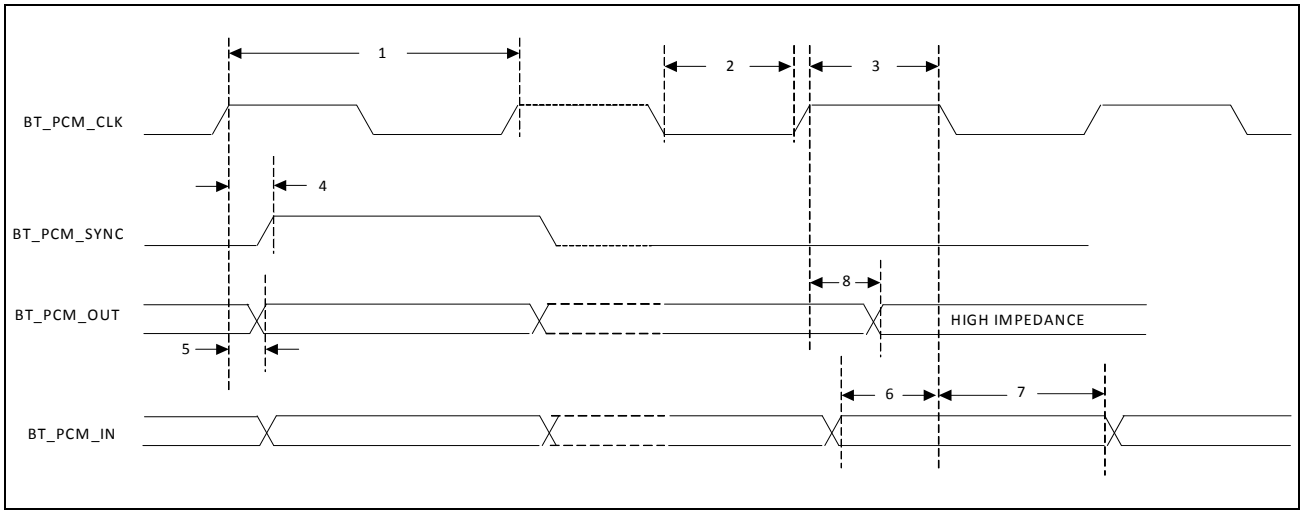


Table 6: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	BT_PCM_SYNC delay	0	–	25	ns
5	BT_PCM_OUT delay	0	–	25	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 11: PCM Timing Diagram (Short Frame Sync, Slave Mode)

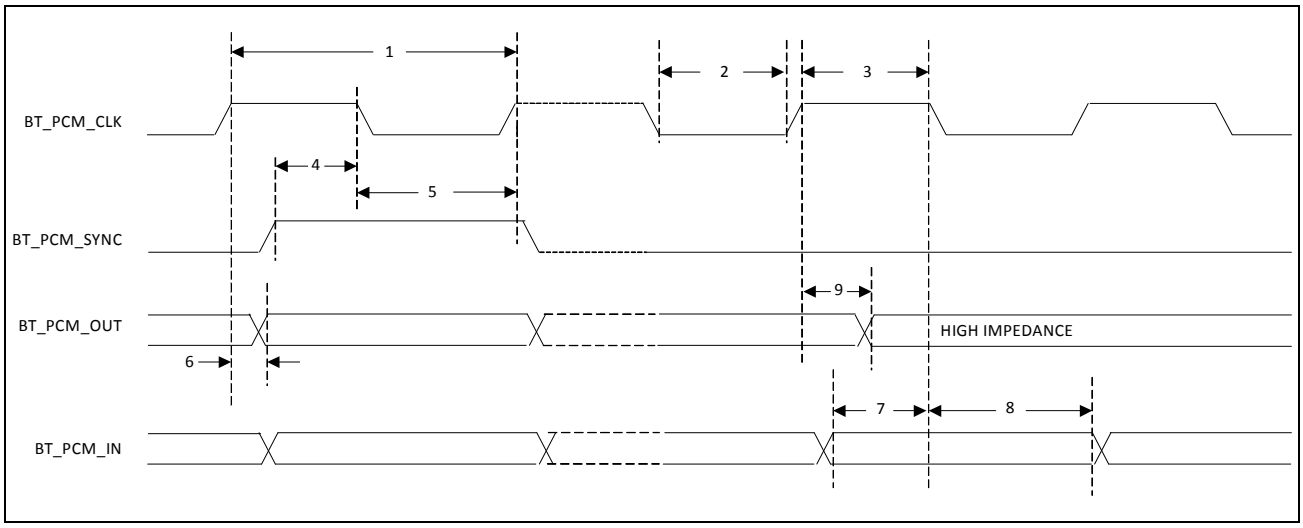


Table 7: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_OUT delay	0	–	25	ns
7	BT_PCM_IN setup	8	–	–	ns
8	BT_PCM_IN hold	8	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Long Frame Sync, Master Mode

Figure 12: PCM Timing Diagram (Long Frame Sync, Master Mode)

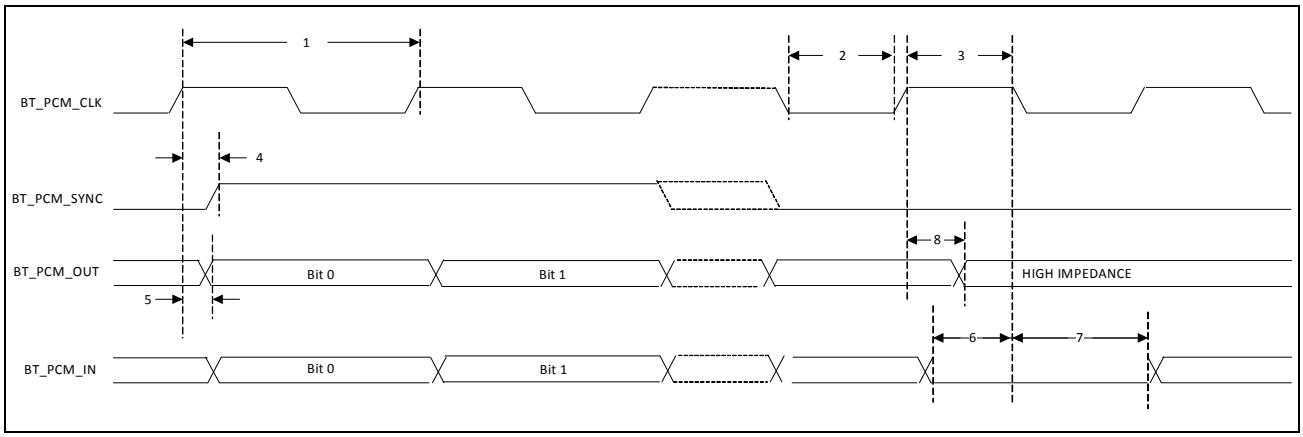


Table 8: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	BT_PCM_SYNC delay	0	–	25	ns
5	BT_PCM_OUT delay	0	–	25	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 13: PCM Timing Diagram (Long Frame Sync, Slave Mode)

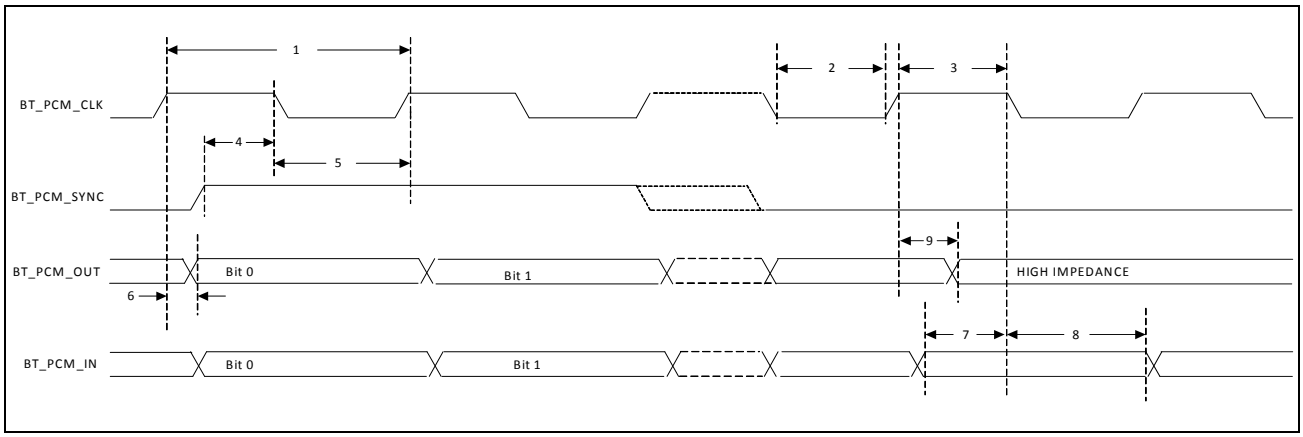


Table 9: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_OUT delay	0	–	25	ns
7	BT_PCM_IN setup	8	–	–	ns
8	BT_PCM_IN hold	8	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Short Frame Sync, Burst Mode

Figure 14: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

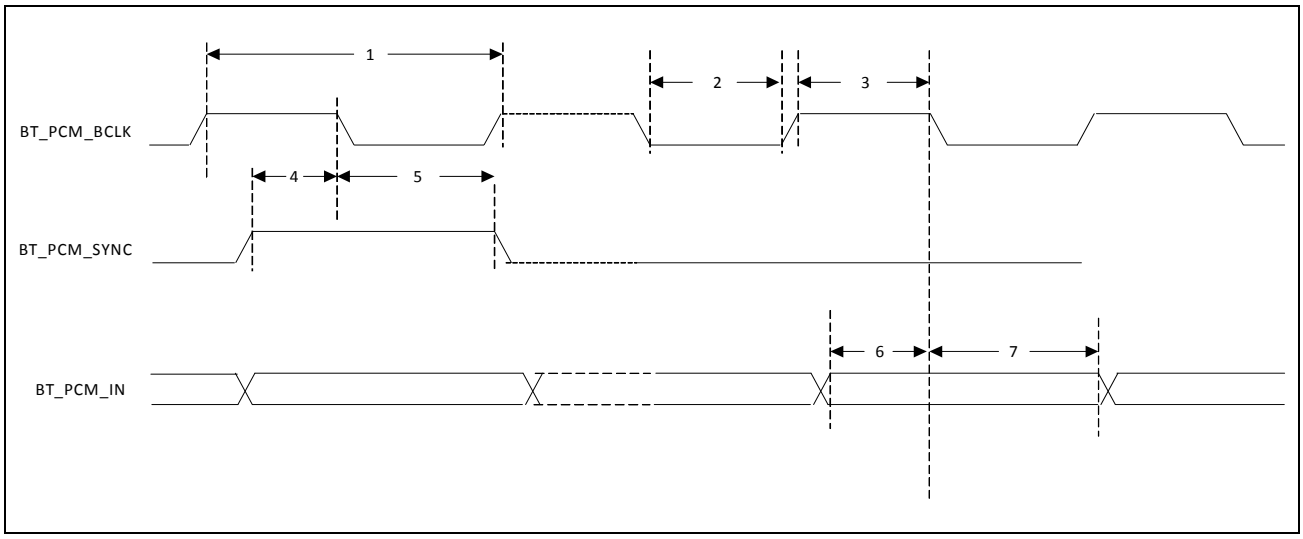


Table 10: PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

Figure 15: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

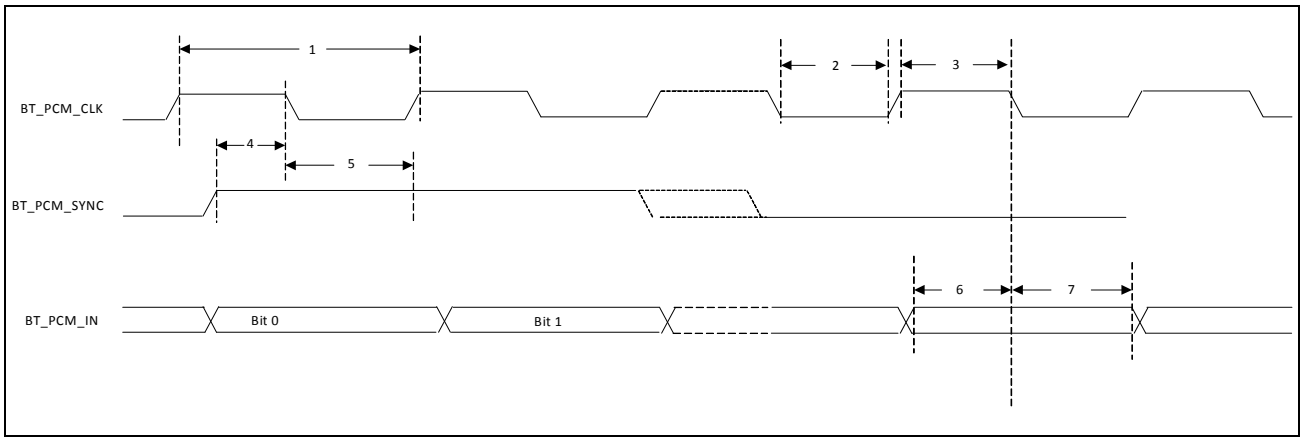


Table 11: PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns

USB Interface

Features

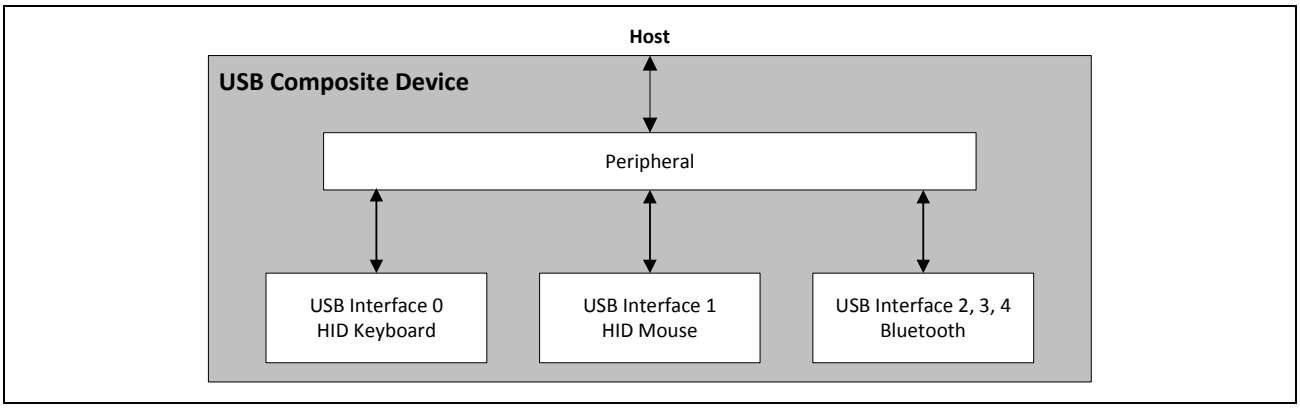
The following USB interface features are supported:

- USB Protocol, Revision 2.0, full-speed (12 Mbps) compliant
- Optional composite device with up to three functions internal to the device
- Global and selective suspend and resume with remote wake-up
- Link power management L1 state with remote wake-up
- HID, DFU, UHE (proprietary method to emulate an HID device at system bootup)
- Integrated detach resistor

Operation

The BCM4359 can be configured to boot up as either a single USB peripheral or USB composite device with multiple interfaces. As a single peripheral, the host detects a single USB Bluetooth device. In hub mode, the host detects a hub with one to three of the ports already connected to USB devices (see Figure 16).

Figure 16: USB Composite Device Configuration



Depending on the desired composite device configuration, the BCM4359 can boot up showing the three functions of logical USB devices internal to the BCM4359: a generic Bluetooth device, a mouse, and a keyboard. In this mode, the mouse and keyboard are emulated functions, since they connect to real HID devices via a Bluetooth link. The Bluetooth link to these HID functions is hidden from the USB host. To the host, the host, the mouse, and/or keyboard appear to be directly connected to the USB port. This Broadcom proprietary architecture is called USB HID Emulation (UHE).

The USB device, configuration, and string descriptors are fully programmable, allowing manufacturers to customize the descriptors, including vendor and product IDs, the BCM4359 uses to identify itself on the USB port. To make custom USB descriptor information available at boot time, stored it in external NVRAM.

Despite the mode of operation (single or composite device), the Bluetooth device is configured to include the following interfaces:

Interface 0 or 2	Contains a Control endpoint (Endpoint 0x00) for HCI commands, a Bulk In Endpoint (Endpoint 0x82) for receiving ACL data, a Bulk Out Endpoint (Endpoint 0x02) for transmitting ACL data, and an Interrupt Endpoint (Endpoint 0x81) for HCI events.
Interface 1 or 3	Contains Isochronous In and Out endpoints (Endpoints 0x83 and 0x03) for SCO traffic. Several alternate Interface 1 settings are available for reserving the proper bandwidth of isochronous data (depending on the application).
Interface 2 or 4	Contains Bulk In and Bulk Out endpoints (Endpoints 0x84 and 0x04) used for proprietary testing and debugging purposes. These endpoints can be ignored during normal operation.

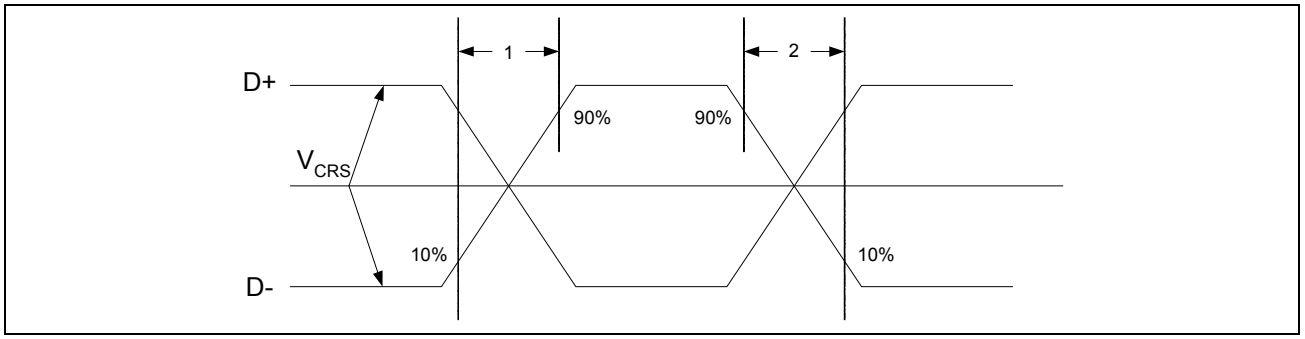
USB Full-Speed Timing

Table 12 shows timing specifications for the VDD_USB = 3.3V, V_{SS} = 0V, and T_A = 0°C to 85°C operating temperature range.

Table 12: USB Full-Speed Timing Specifications

Reference	*Characteristics*	*Minimum*	*Maximum*	*Unit*
1	Transition rise time	4	20	ns
2	Transition fall time	4	20	ns
3	Rise/fall timing matching	90	111	%
4	Full-speed data rate	12 – 0.25%	12 + 0.25%	Mbps

Figure 17: USB Full-Speed Timing



UART Interface

The BCM4359 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.2 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM4359 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM4359 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 13: Example of Common Baud Rates

Desired Rate	*Actual Rate*	*Error (%)*
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 18: UART Timing

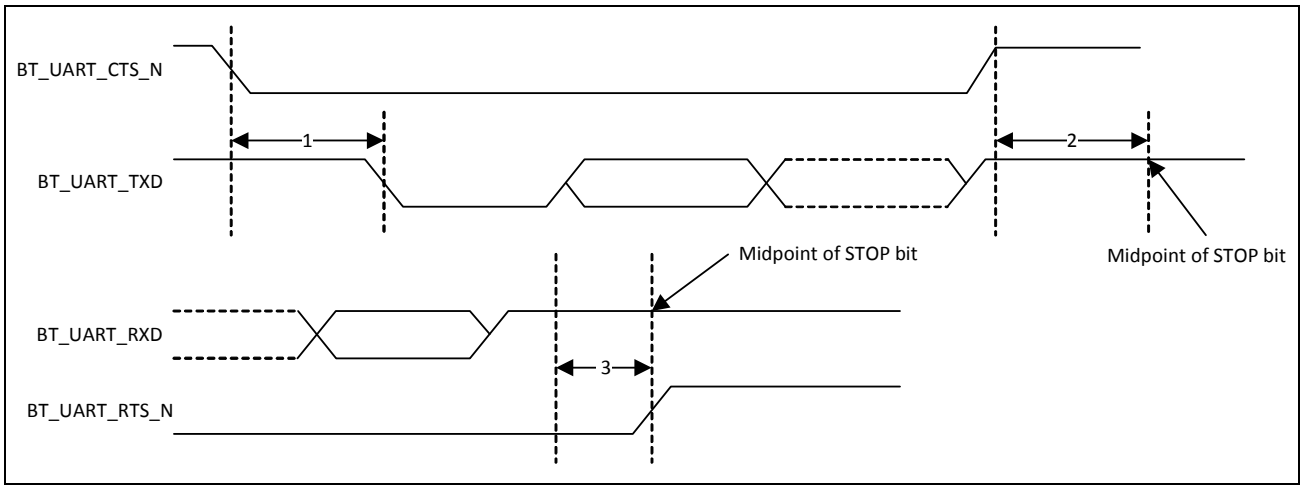


Table 14: UART Timing Specifications

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

I2S Interface

The BCM4359 supports I2S digital audio port for Bluetooth audio. The I2S signals are:

- I2S clock: BT_I2S_CLK
- I2S Word Select: BT_I2S_WS
- I2S Data Out: BT_I2S_DO
- I2S Data In: BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS become outputs in master mode and inputs in slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I2S bus, in accord with the I2S specification. The MSB of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT_I2S_WS is low, and right-channel data is transmitted when BT_I2S_WS is high. Data bits sent by the BCM4359 are synchronized with the falling edge of BT_I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

I²S Timing

Note: Timing values specified in Table 15 are relative to high and low threshold levels.

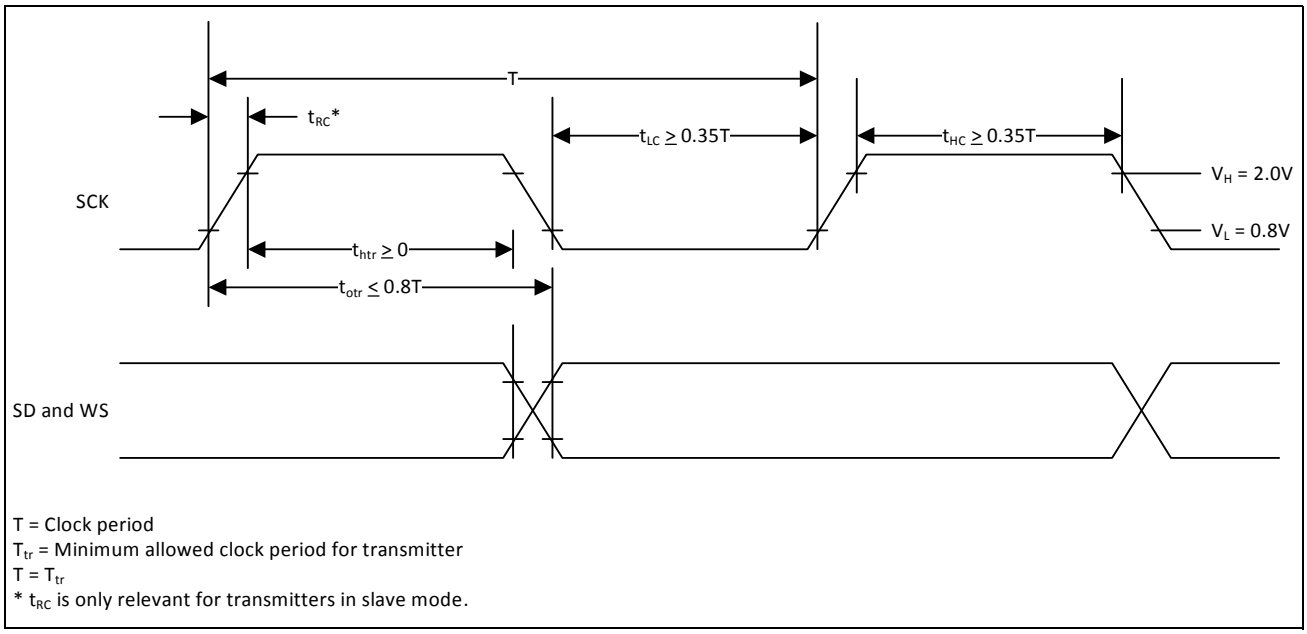
Table 15: Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–	–	–	d
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	e
Hold time t_{htr}	0	–	–	–	–	–	–	–	d
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	f
Hold time t_{hr}	–	–	–	–	–	0	–	–	f

a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
d. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

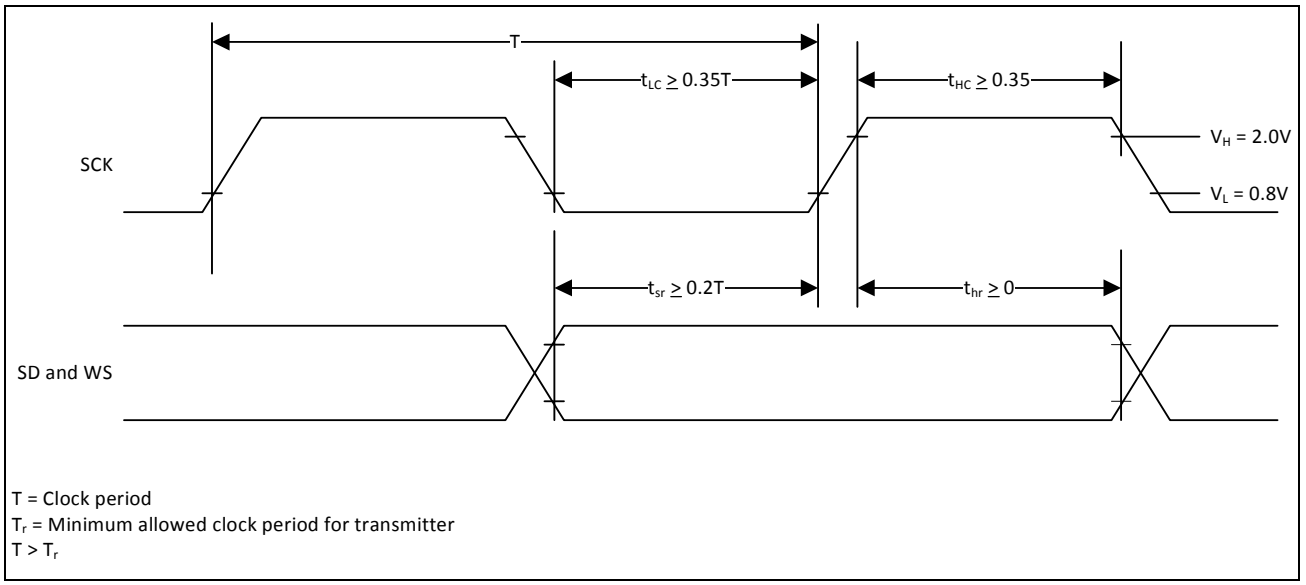
Note: The time periods specified in Figure 19 and Figure 20 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 19: I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
T = T_{tr}
* t_{RC} is only relevant for transmitters in slave mode.

Figure 20: I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
T > T_r

Section 8: WLAN Global Functions

WLAN CPU and Memory Subsystem

The BCM4359 WLAN section includes an integrated ARM Cortex-R4 32-bit processor with internal RAM and ROM. The on-chip memory for the CPU includes 768 KB SRAM and 768 KB ROM. The ARM Cortex-R4 processor implements the ARM v7-R architecture with support for the Thumb-2 instruction set.

Using multiple technologies to reduce cost, the ARM Cortex-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and System buses), integrated sleep modes, and extensive debug features including real time trace of program execution.

One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal one-time programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Up to 1150 bytes of user-accessible OTP are available.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

GPIO Interface

The BCM4359 has 20 general-purpose I/O (GPIO) pins in the WLAN section that can be used to connect to various external devices.

Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions, see Table 26: “GPIO Alternative Signal Functions,” on page 121.

External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as GPS, WiMAX, LTE, or UWB, to manage wireless medium sharing for optimal performance.

Figure 21 and Figure 22 on page 56 show the LTE/GPS coexistence interface (including UART) for each BCM4359 package type. See Table 26: “GPIO Alternative Signal Functions,” on page 121 for further details on multiplexed signals, such as the GPIO pins.

See Table 14: “UART Timing Specifications,” on page 51 for the UART baud rate.

Figure 21: Multipoint Global Coexistence Interface

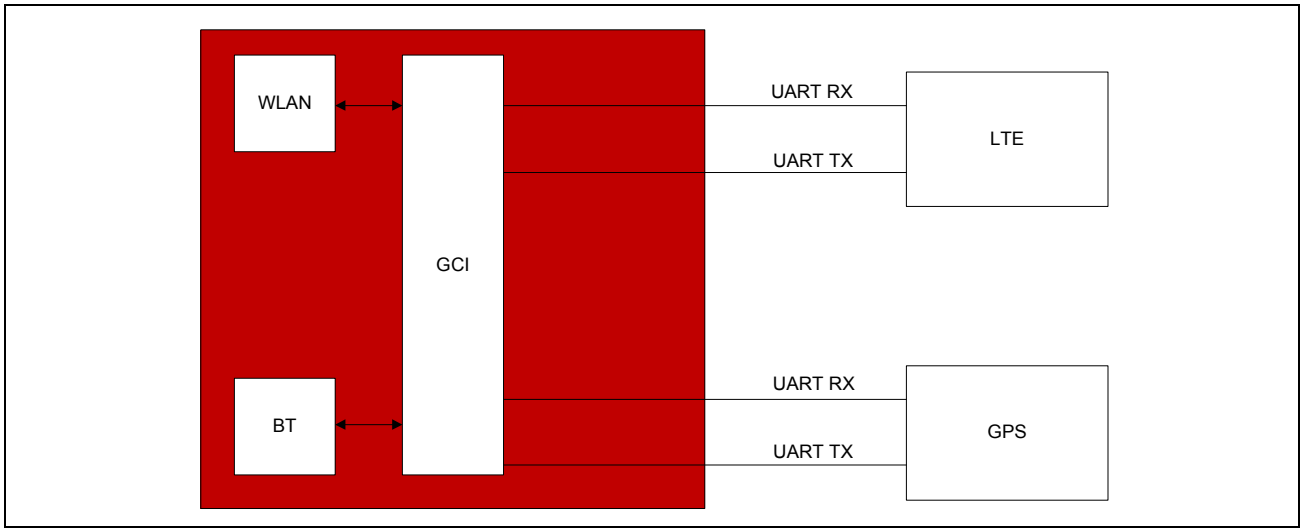
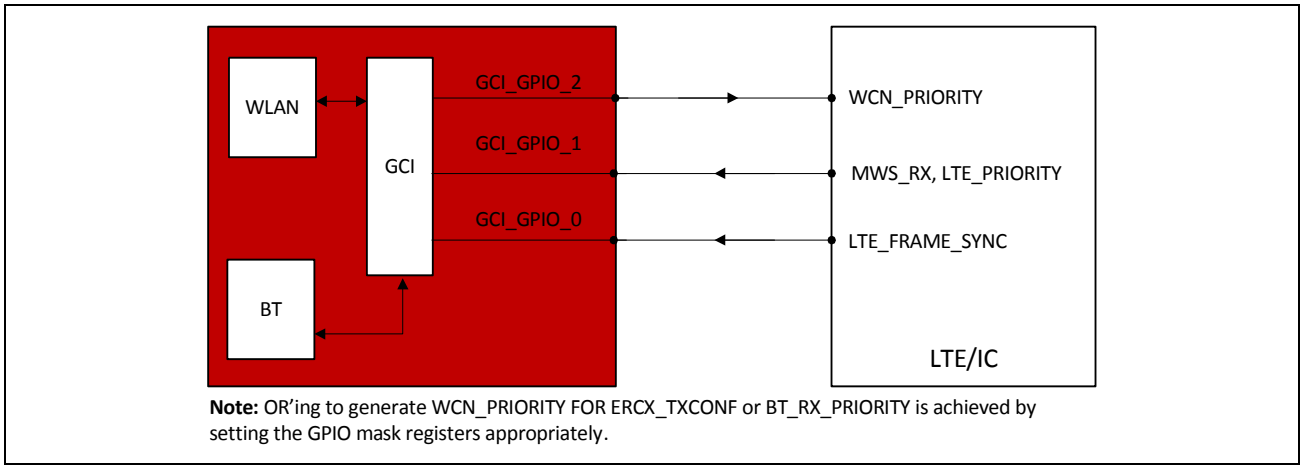


Figure 22: Legacy 3-Wire LTE Coexistence Interface



Note: OR’ing to generate WCN_PRIORITY FOR ERCX_TXCONF or BT_RX_PRIORITY is achieved by setting the GPIO mask registers appropriately.

Debug UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins. Refer to Table 26: “GPIO Alternative Signal Functions,” on page 121. Provided primarily for debugging during development, this UART enables the BCM4359 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

FAST UART Interface

A high-speed 4-wire CTS/RTS UART interface can be enabled by software as an alternate function on GPIO pins. Refer to Table 26: “GPIO Alternative Signal Functions,” on page 121. Provided primarily for control word exchange, this UART enables the chip to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

JTAG Interface

The BCM4359 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

Refer to Table 26: “GPIO Alternative Signal Functions,” on page 121 for JTAG pin assignments.

SPROM Interface

Various hardware configuration parameters may be stored in an external SPROM instead of the OTP. The SPROM is read by system software after device reset. In addition, depending on the board design, customer-specific parameters may be stored in SPROM.

The four SPROM control signals —SPROM_CS, SPROM_CLK, SPROM_MI, and SPROM_MO are multiplexed on the SDIO interface (see Table 26: “GPIO Alternative Signal Functions,” on page 121 for additional details). By default, the SPROM interface supports 2 kbit serial SPROMs, and it can also support 4 kbit and 16 kbit serial SPROMs by using the appropriate board parameters.

BSC Interface

A proprietary Broadcom Serial Control (BSC, an I^2C-compatible interface) slave interface is available, as an alternate function on the GPIO lines, which supports data transfer rates up to 3.4 Mbps in high-speed mode. This can be primarily used to transfer data to sensor hub in the host system. This interface also supports device addressing using both 7 bit or 10 bit and interrupt to the processor. Based on the device-address matching, a device can be brought out of low-power state using this interface. This interface provides an internal FIFO depth of 32 bytes for both TX and RX with ability to filter the glitches on both clock and data lines.

Section 9: WLAN Host Interfaces

SDIO v3.0

All three package options of the BCM4359 WLAN section provide support for SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).
- SDR50: SDR up to 100 MHz (1.8V signaling).
- SDR104: SDR up to 208 MHz (1.8V signaling)
- DDR50: DDR up to 50 MHz (1.8V signaling).

Note: The BCM4359 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options. Refer to Table 24 on page 119 WLAN GPIO Functions and Strapping Options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

SDIO Pins

Table 16: SDIO Pin Descriptions

SD 4-Bit Mode		*SD 1-Bit Mode*	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Figure 23: Signal Connections to SDIO Host (SD 4-Bit Mode)

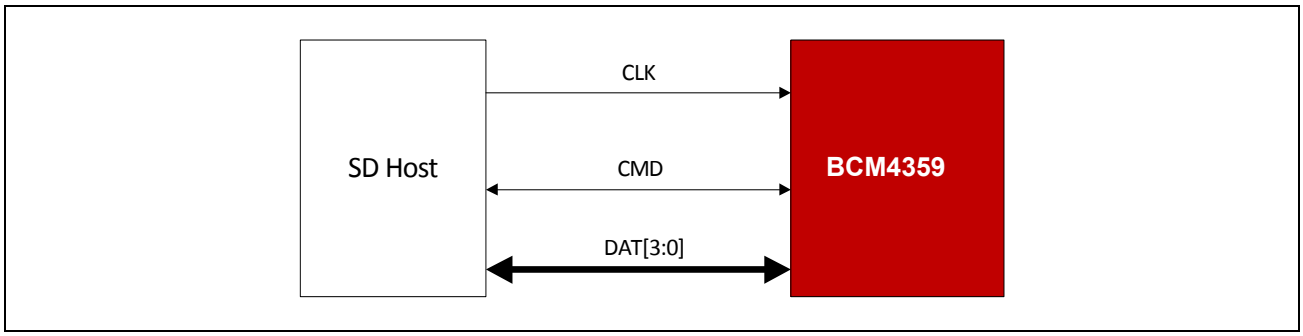
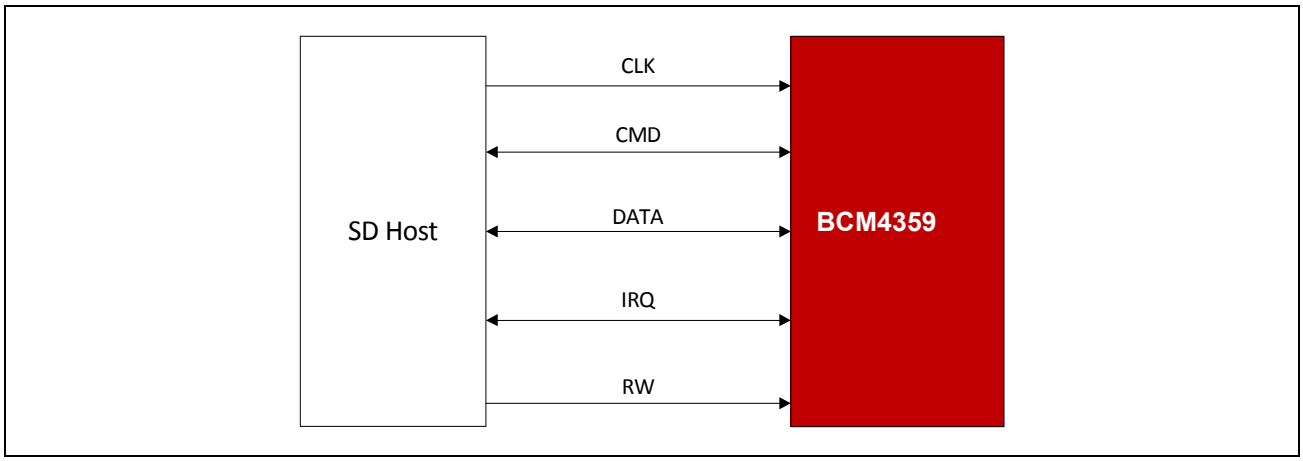


Figure 24: Signal Connections to SDIO Host (SD 1-Bit Mode)



Note: Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

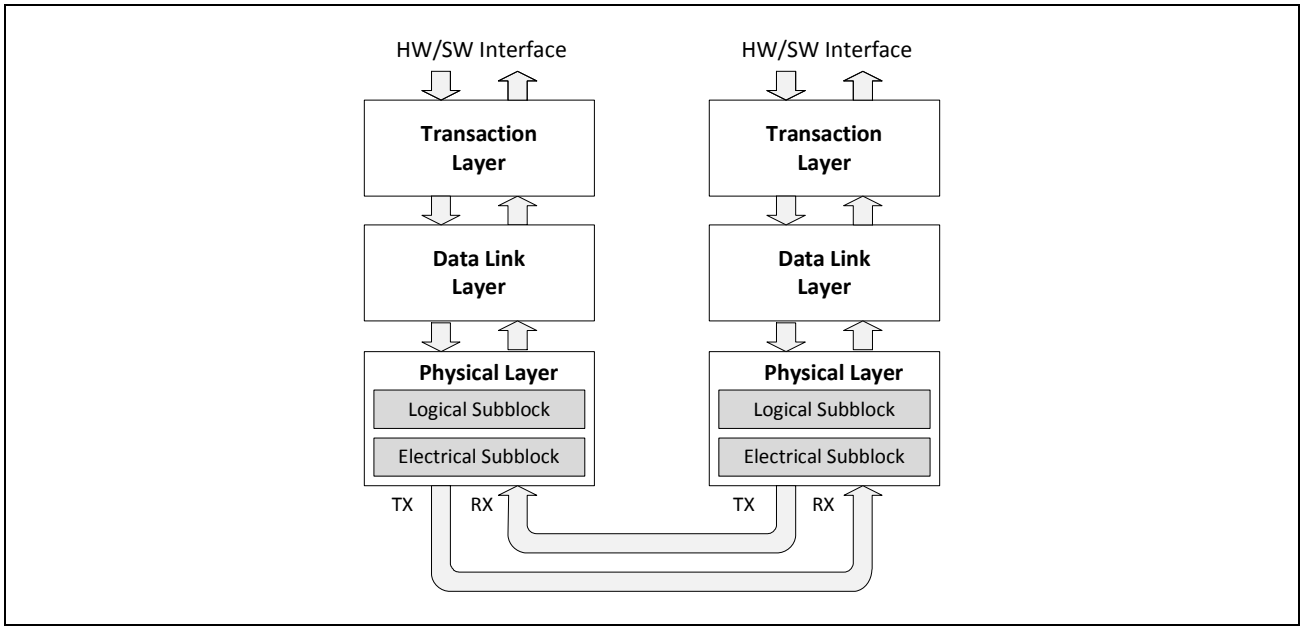
PCI Express Interface

The PCI Express (PCIe) core on the BCM4359 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification v3.0* running at Gen1 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 25. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and BCM4359 device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 25: PCI Express Layer Model



Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and BCM4359 device, delivering new levels of performance and features. The upper layer of the PCIe is the transaction layer. The transaction layer is primarily responsible for assembly and disassembly of transaction layer packets (TLPs). TLP structure contains header, data payload, and end-to-end CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

The data link layer packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and BCM4359 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

8B/10B Encoder/Decoder

The PCIe core on the BCM4359 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the 12 special symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. The special symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

Electrical Subblock

The high-speed signals utilize the common mode logic (CML) signaling interface with on-chip termination and de-emphasis for best-in-class signal integrity. A de-emphasis technique is employed to reduce the effects of intersymbol interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable bit-error rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are de-emphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the de-emphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

Configuration Space

The PCIe function in the BCM4359 implements the configuration space as defined in the *PCI Express Base Specification v3.0*.

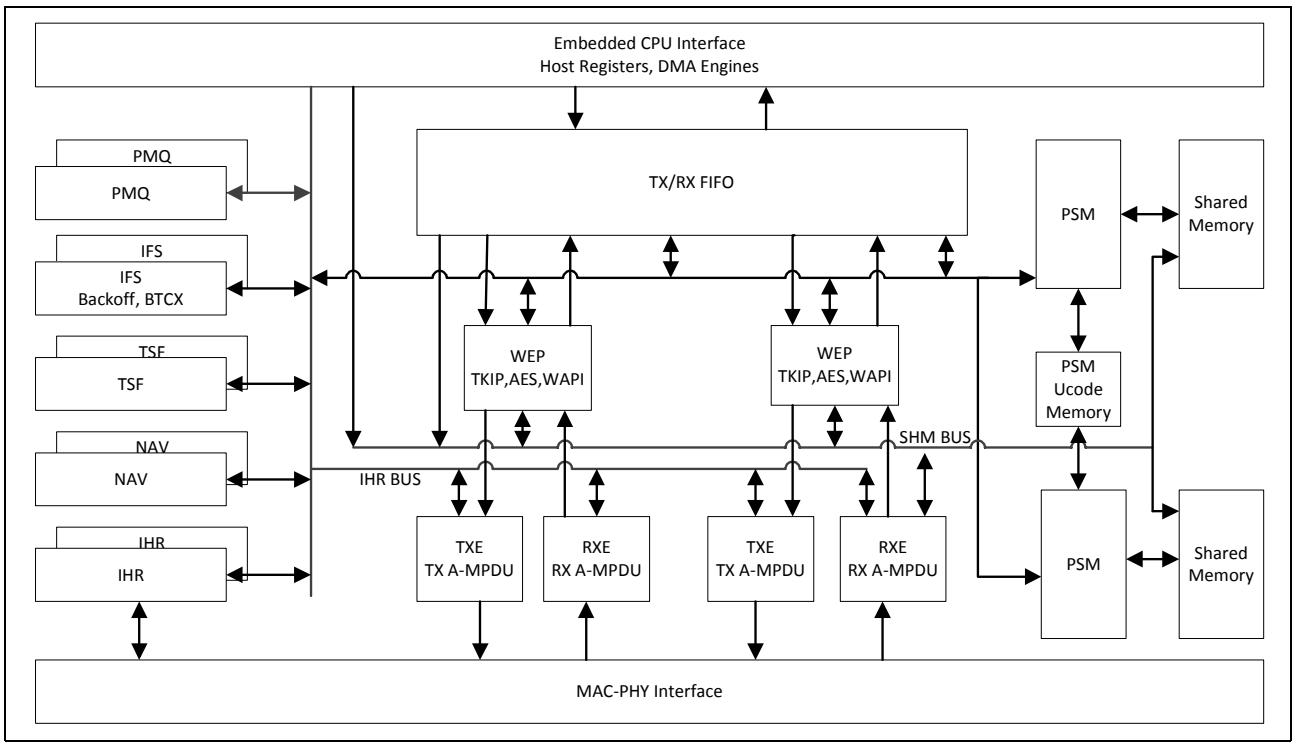
Section 10: Wireless LAN MAC and PHY

IEEE 802.11ac MAC

The BCM4359 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 26.

The following sections provide an overview of the important modules in the MAC.

Figure 26: WLAN MAC Architecture



The BCM4359 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11ac features.
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT).
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Hardware offload engine for IEEE 802.11 to IEEE 802.3 header conversion for receive packets.
- Support for coexistence with Bluetooth and other external radios.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality.
- Statistics counters for MIB support.
- RSDB-capable PHY and MAC support for 2 × 2 operation or two independent 1 × 1 operations.

PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

IEEE 802.11ac PHY

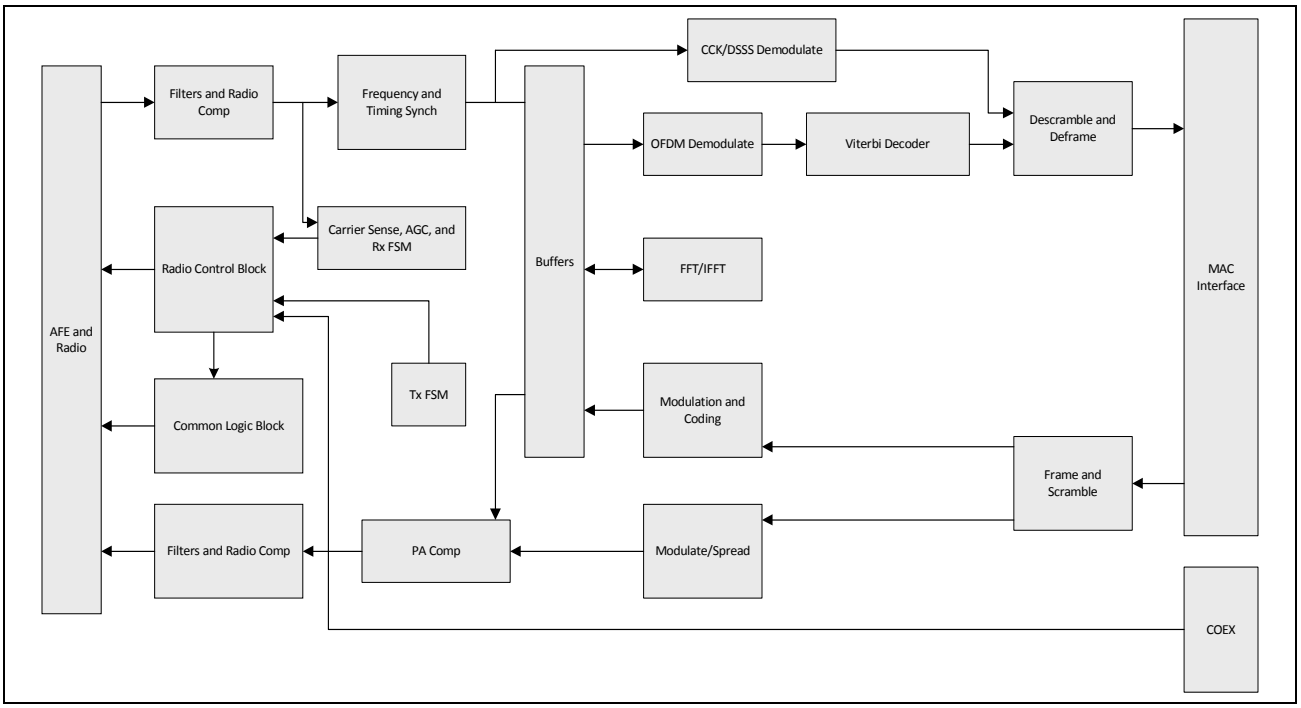
The BCM4359 WLAN Digital PHY PHY is designed to comply with IEEE 802.11ac and IEEE 802.11a/b/g/n specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 866.7 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT, and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for sharing an antenna between WL and BT to support simultaneous RX-RX.

The key PHY features include:

- Programmable data rates from MCS0–MCS9 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in IEEE 802.11ac
- Real simultaneous dual-band (RSDB), 2×2, and 80 + 80 MHz modes
- Improved performance with 2×2 channel smoothing support
- Short GI in TX and RX
- TX and RX LDPC for improved range and power efficiency
- Beamforming
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction
- Supports IEEE 802.11h/k for worldwide operation, designed to meet FCC and other worldwide regulatory requirements
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Closed loop-transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Available per-packet channel quality and signal strength measurements
- 5 MHz and 10 MHz modes of operation

Figure 27: WLAN PHY Block Diagram



Section 11:WLAN Radio Subsystem

The BCM4359 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Twenty RF control signals are available (10 per core) to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

The BCM4359 includes an integrated dual-band WLAN RF radio that follows an RSDB architecture, using two RFPLLs, where each core can operate independently. The same radio can be configured in MIMO mode, whereas one RFPLL is used to drive both of the cores and MIMO operation is achieved.

Receiver Path

The BCM4359 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. An on-chip low noise amplifier (LNA) in the 2.4 GHz path in CORE0 (can be optional) is shared between the Bluetooth and WLAN receivers, whereas the 5 GHz receive path and the CORE1 2.4 GHz receive path have dedicated on-chip LNAs. Control signals are available that can support the use of external LNAs for each band, which can increase the receive sensitivity by several dB.

Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output power while meeting IEEE 802.11ac and IEEE 802.11a/b/g/n specifications, and without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated.

Calibration

The BCM4359 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

Section 12: Pinout and Signal Descriptions

Ball Maps

Figure 28 and Figure 29 show the BCM4359 WLBGA ball map.

Figure 28: BCM4359 WLBGA Ball Map, A1–J12 (Package Bottom View—Balls Facing Up)

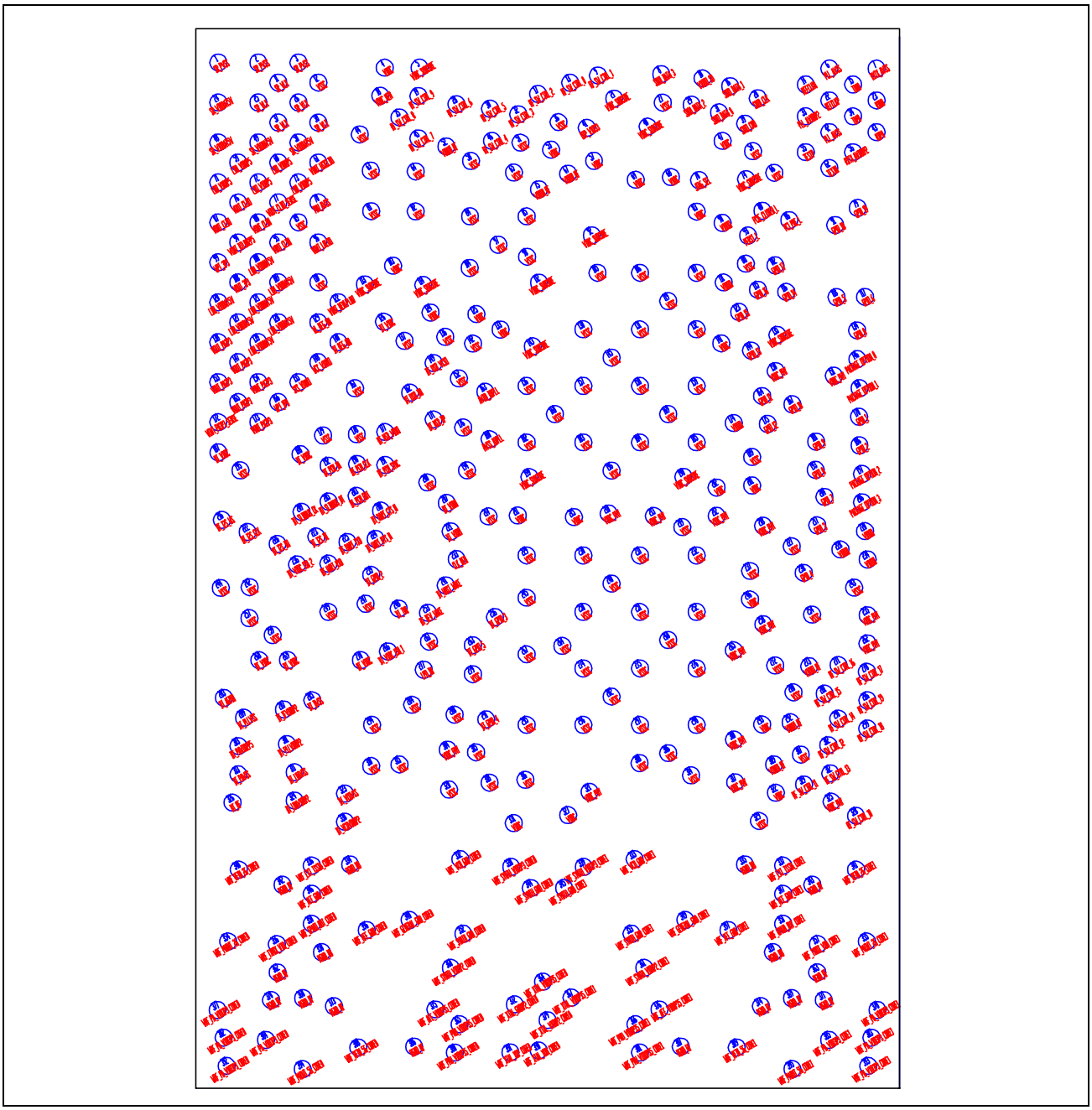
J	H	G	F	E	D	C	B	A	
	GPIO_6	GPIO_10	VDDC	PCIE_CLKREQ_L	PCIE_RDP0	PCIE_RDN0	PCIE_REFCLKP	PCIE_REFCLKN	12
GPIO_4	VDDC	GPIO_7	GPIO_9	PCIE_PERST_L	RXTX_AVDD1p2	PCIE_TESTN	PCIE_TESTP	PCIE_TDN0	11
GPIO_5	GPIO_8	GPIO_11	VDDIO	PCI_PME_L	PLL_AVSS	RXTX_AVSS	PLL_AVDD1p2	PCIE_TDP0	10
GPIO_3	VSSC		GPIO_13	JTAG_SEL	VSSC	VDDC			9
GPIO_14		AVSS_BBPLL	AVDD_BBPLL	GPIO_16	GPIO_12		SDIO_CMD	SDIO_CLK	8
VSSC	VDDC	HUSB_DP	HUSB_DN	VSSC	GPIO_15	GPIO_17	VDDIO_SD	SDIO__DATA_3	7
BT_UART_TXD	BT_PCM_SYNC	BT_PCM_CLK	RF_SW_CTRL_1	RF_SW_CTRL_0	VDDIO_RF		SDIO__DATA_0	SDIO__DATA_2	6
BT_SLIMBUS_DT	RF_SW_CTRL_4	RF_SW_CTRL_3	RF_SW_CTRL_2	GPIO_18	GPIO_19		VDDC	SDIO__DATA_1	5
BT_SLIMBUS_CK	RF_SW_CTRL_7	RF_SW_CTRL_6	RF_SW_CTRL_5	WL_REG_ON		VDDC_MEM			4
BT_VDDC	RF_SW_CTRL_8	WCC_VDDIO	BT_REG_ON	VOUT_MEMLPLDO	VSSC	VDDC	PMU_AVSS	VSSC	3
BT_PCM_IN	RF_SW_CTRL_9	WPT_1P8	SYS_VDDIO	VOUT_3P3	VOUT_LNLDO	VOUT_CLDO	VOUT_HLDO	SR_VLX	2
	VSSC	VOUT_PA3P3	LDO_VDDBAT5V	WPT_3P3	VOUT_BTLDO2P5	LDO_VDD1P5	SR_VDDBAT5V	SR_PVSS	1
J	H	G	F	E	D	C	B	A	

Figure 29: BCM4359 WLBGA Ball Map, K1–V12(Package Bottom View—Balls Facing Up)

	V	U	T	R	P	N	M	L	K
12	WRF_PA_VDD3P3_core1		WRF_PAOUT_2G_core1	WRF_RFIN_2G_core1	RF_SW_CTRL_12	RF_SW_CTRL_15		RF_SW_CTRL_19	GPIO_0
11	WRF_PAOUT_5G_core1	WRF_PA_GND3P3_core1	WRF_TXMIX_VDD_core1	WRF_RX2G_GND_core1		RF_SW_CTRL_11	RF_SW_CTRL_14	RF_SW_CTRL_18	GPIO_1
10	WRF_RFIN_5G_core1	WRF_GENERAL2_GND_core1	WRF_AFE_GND_core1	WRF_GPAIO_OUT_core1	VSSC	RF_SW_CTRL_10	RF_SW_CTRL_13	VDDC	GPIO_2
9	WRF_RX5G_GND_core1	WRF_AFE_VDD1P35_core1	WRF_GENERAL_GND_core1	WRF_EXT_TSSIA_core1		VDDC	VDDIO_RF	RF_SW_CTRL_17	RF_SW_CTRL_16
8	WRF_PMU_VDD1P35_core1	WRF_SYNTH_VDD1P2_core1	WRF_SYNTH_GND_core1	WRF_VCO_GND_core1		VSSC	BT_UART_RTS_N	BT_UART_CTS_N	VDDIO
7	WRF_XTAL_XOP_core0	WRF_XTAL_VDD1P2_core0	WRF_XTAL_VDD1P35_core1	WRF_SYNTH_VDD3P3_core1		VDDC		BT_I2S_WS	BT_I2S_CLK
6	WRF_XTAL_XON_core0	WRF_XTAL_GND1P2_core0	WRF_XTAL_VDD1P35_core0	WRF_SYNTH_VDD3P3_core0		LPO_IN	BT_I2S_DO	BT_GPIO_2	VDDC
5	WRF_PMU_VDD1P35_core0	WRF_SYNTH_VDD1P2_core0	WRF_SYNTH_GND_core0	WRF_VCO_GND_core0		CLK_REQ	BT_I2S_DI	BT_GPIO_3	BT_UART_RXD
4	WRF_RX5G_GND_core0	WRF_AFE_VDD1P35_core0	WRF_GENERAL_GND_core0	WRF_EXT_TSSIA_core0	BT_DEV_WAKE	BT_HOST_WAKE	VSSC	BT_VDDC	BT_VDDO
3	WRF_RFIN_5G_core0	WRF_GENERAL2_GND_core0	WRF_AFE_GND_core0	WRF_GPAIO_OUT_core0	BT_VCOVDD1p2	BT_VCOVSS	BT_IFVSS	BT_PCM_OUT	VSSC
2	WRF_PAOUT_5G_core0	WRF_PA_GND3P3_core0	WRF_TXMIX_VDD_core0	WRF_RX2G_GND_core0	BT_LNAVDD1p2	BT_LNAVSS	BT_PLLVSS	BT_GPIO_5	BT_VDDC
1	WRF_PA_VDD3P3_core0		WRF_PAOUT_2G_core0	WRF_RFIN_2G_core0	BT_RFOP	BT_PAVDD2p5	BT_PLLVDD1p2	BT_IFVDD1p2	BT_GPIO_4
	V	U	T	R	P	N	M	L	K

Figure 30 shows the BCM4359 397-bump WLCSP ball map.

Figure 30: BCM4359 WLCSP Package Top View (Bumps Facing Down)



Pin Lists

Table 17 lists the BCM4359 WLBGA pins by pin number. For a list of by BCM4359 WLBGA pins by pin name, see Table 18 on page 77.

Table 17: WLBGA Pin List by Pin Number

Ball No.	Name
A1	SR_PVSS
A2	SR_VLX
A3	VSSC
A5	SDIO_DATA_1
A6	SDIO_DATA_2
A7	SDIO_DATA_3
A8	SDIO_CLK
A10	PCIE_TDP0
A11	PCIE_TDN0
A12	PCIE_REFCLKN
B1	SR_VDDBAT5V
B2	VOUT_HLDO
B3	PMU_AVSS
B5	VDDC
B6	SDIO_DATA_0
B7	VDDIO_SD
B8	SDIO_CMD
B10	PLL_AVDD1P2
B11	PCIE_TESTP
B12	PCIE_REFCLKP
C1	LDO_VDD1P5
C2	VOUT_CLDO
C3	VDDC
C4	VDDC_MEM
C7	GPIO_17
C9	VDDC
C10	RXTX_AVSS
C11	PCIE_TESTN
C12	PCIE_RDN0
D1	VOUT_BTLDO2P5
D2	VOUT_LNLDO
D3	VSSC
D5	GPIO_19

Table 17: WLBGA Pin List by Pin Number (Cont.)

Ball No.	Name
D6	VDDIO_RF
D7	GPIO_15
D8	GPIO_12
D9	VSSC
D10	PLL_AVSS
D11	RXTX_AVDD1P2
D12	PCIE_RDP0
E1	WPT_3P3
E2	VOUT_3P3
E3	VOUT_MEMLPLDO
E4	WL_REG_ON
E5	GPIO_18
E6	RF_SW_CTRL_0
E7	VSSC
E8	GPIO_16
E9	JTAG_SEL
E10	PCI_PME_L
E11	PCIE_PERST_L
E12	PCIE_CLKREQ_L
F1	LDO_VDDBAT5V
F2	SYS_VDDIO
F3	BT_REG_ON
F4	RF_SW_CTRL_5
F5	RF_SW_CTRL_2
F6	RF_SW_CTRL_1
F7	HUSB_DN
F8	AVDD_BBPLL
F9	GPIO_13
F10	VDDIO
F11	GPIO_9
F12	VDDC
G1	VOUT_PA3P3
G2	WPT_1P8

Table 17: WLBGA Pin List by Pin Number (Cont.)

Ball No.	Name
G3	WCC_VDDIO
G4	RF_SW_CTRL_6
G5	RF_SW_CTRL_3
G6	BT_PCM_CLK
G7	HUSB_DP
G8	AVSS_BBPLL
G10	GPIO_11
G11	GPIO_7
G12	GPIO_10
H1	VSSC
H2	RF_SW_CTRL_9
H3	RF_SW_CTRL_8
H4	RF_SW_CTRL_7
H5	RF_SW_CTRL_4
H6	BT_PCM_SYNC
H7	VDDC
H9	VSSC
H10	GPIO_8
H11	VDDC
H12	GPIO_6
J2	BT_PCM_IN
J3	BT_VDDC
J4	BT_SLIMBUS_CK
J5	BT_SLIMBUS_DT
J6	BT_UART_TXD
J7	VSSC
J8	GPIO_14
J9	GPIO_3
J10	GPIO_5
J11	GPIO_4
K1	BT_GPIO_4
K2	BT_VDDC
K3	VSSC
K4	BT_VDDO
K5	BT_UART_RXD
K6	VDDC
K7	BT_I2S_CLK
K8	VDDIO
K9	RF_SW_CTRL_16

Table 17: WLBGA Pin List by Pin Number (Cont.)

Ball No.	Name
K10	GPIO_2
K11	GPIO_1
K12	GPIO_0
L1	BT_IFVDD1P2
L2	BT_GPIO_5
L3	BT_PCM_OUT
L4	BT_VDDC
L5	BT_GPIO_3
L6	BT_GPIO_2
L7	BT_I2S_WS
L8	BT_UART_CTS_N
L9	RF_SW_CTRL_17
L10	VDDC
L11	RF_SW_CTRL_18
L12	RF_SW_CTRL_19
M1	BT_PLLVDD1P2
M2	BT_PLLVSS
M3	BT_IFVSS
M4	VSSC
M5	BT_I2S_DI
M6	BT_I2S_DO
M8	BT_UART_RTS_N
M9	VDDIO_RF
M10	RF_SW_CTRL_13
M11	RF_SW_CTRL_14
N1	BT_PAVDD2P5
N2	BT_LNAVSS
N3	BT_VCOVSS
N4	BT_HOST_WAKE
N5	CLK_REQ
N6	LPO_IN
N7	VDDC
N8	VSSC
N9	VDDC
N10	RF_SW_CTRL_10
N11	RF_SW_CTRL_11
N12	RF_SW_CTRL_15
P1	BT_RFOP
P2	BT_LNAVDD1P2

Table 17: WLBGA Pin List by Pin Number (Cont.)

Ball No.	Name
P3	BT_VCOVDD1P2
P4	BT_DEV_WAKE
P10	VSSC
P12	RF_SW_CTRL_12
R1	WRF_RFIN_2G_CORE0
R2	WRF_RX2G_GND_CORE0
R3	WRF_GPAIO_OUT_CORE0
R4	WRF_EXT_TSSIA_CORE0
R5	WRF_VCO_GND_CORE0
R6	WRF_SYNTH_VDD3P3_CORE0
R7	WRF_SYNTH_VDD3P3_CORE1
R8	WRF_VCO_GND_CORE1
R9	WRF_EXT_TSSIA_CORE1
R10	WRF_GPAIO_OUT_CORE1
R11	WRF_RX2G_GND_CORE1
R12	WRF_RFIN_2G_CORE1
T1	WRF_PAOUT_2G_CORE0
T2	WRF_TXMIX_VDD_CORE0
T3	WRF_AFE_GND_CORE0
T4	WRF_GENERAL_GND_CORE0
T5	WRF_SYNTH_GND_CORE0
T6	WRF_XTAL_VDD1P35_CORE0
T7	WRF_XTAL_VDD1P35_CORE1
T8	WRF_SYNTH_GND_CORE1
T9	WRF_GENERAL_GND_CORE1
T10	WRF_AFE_GND_CORE1
T11	WRF_TXMIX_VDD_CORE1
T12	WRF_PAOUT_2G_CORE1
U2	WRF_PA_GND3P3_CORE0
U3	WRF_GENERAL2_GND_CORE0
U4	WRF_AFE_VDD1P35_CORE0
U5	WRF_SYNTH_VDD1P2_CORE0
U6	WRF_XTAL_GND1P2_CORE0
U7	WRF_XTAL_VDD1P2_CORE0
U8	WRF_SYNTH_VDD1P2_CORE1
U9	WRF_AFE_VDD1P35_CORE1
U10	WRF_GENERAL2_GND_CORE1
U11	WRF_PA_GND3P3_CORE1
V1	WRF_PA_VDD3P3_CORE0

Table 17: WLBGA Pin List by Pin Number (Cont.)

Ball No.	Name
V2	WRF_PAOUT_5G_CORE0
V3	WRF_RFIN_5G_CORE0
V4	WRF_RX5G_GND_CORE0
V5	WRF_PMU_VDD1P35_CORE0
V6	WRF_XTAL_XON_CORE0
V7	WRF_XTAL_XOP_CORE0
V8	WRF_PMU_VDD1P35_CORE1
V9	WRF_RX5G_GND_CORE1
V10	WRF_RFIN_5G_CORE1
V11	WRF_PAOUT_5G_CORE1
V12	WRF_PA_VDD3P3_CORE1

Table 18 lists the BCM4359 WLBGA pins by pin name. For a list of by BCM4359 WLBGA pins by pin number, see Table 17 on page 74.

Table 18: WLBGA Pins Listed by Pin Name

Name	Ball No.
AVDD_BBPLL	F8
AVSS_BBPLL	G8
BT_DEV_WAKE	P4
BT_GPIO_2	L6
BT_GPIO_3	L5
BT_GPIO_4	K1
BT_GPIO_5	L2
BT_HOST_WAKE	N4
BT_I2S_CLK	K7
BT_I2S_DI	M5
BT_I2S_DO	M6
BT_I2S_WS	L7
BT_IFVDD1P2	L1
BT_IFVSS	M3
BT_LNAVDD1P2	P2
BT_LNAVSS	N2
BT_PAVDD2P5	N1
BT_PCM_CLK	G6
BT_PCM_IN	J2
BT_PCM_OUT	L3
BT_PCM_SYNC	H6
BT_PLLVDD1P2	M1
BT_PLLVSS	M2
BT_REG_ON	F3
BT_RFOP	P1
BT_SLIMBUS_CK	J4
BT_SLIMBUS_DT	J5
BT_UART_CTS_N	L8
BT_UART_RTS_N	M8
BT_UART_RXD	K5
BT_UART_TXD	J6
BT_VCOVDD1P2	P3
BT_VCOVSS	N3
BT_VDDC	J3
BT_VDDC	K2
BT_VDDC	L4

Table 18: WLBGA Pins Listed by Pin Name (Cont.)

Name	Ball No.
BT_VDDO	K4
CLK_REQ	N5
GPIO_0	K12
GPIO_1	K11
GPIO_2	K10
GPIO_3	J9
GPIO_4	J11
GPIO_5	J10
GPIO_6	H12
GPIO_7	G11
GPIO_8	H10
GPIO_9	F11
GPIO_10	G12
GPIO_11	G10
GPIO_12	D8
GPIO_13	F9
GPIO_14	J8
GPIO_15	D7
GPIO_16	E8
GPIO_17	C7
GPIO_18	E5
GPIO_19	D5
HUSB_DN	F7
HUSB_DP	G7
JTAG_SEL	E9
LDO_VDD1P5	C1
LDO_VDDBAT5V	F1
LPO_IN	N6
PCIE_CLKREQ_L	E12
PCIE_PERST_L	E11
PCIE_RDN0	C12
PCIE_RDP0	D12
PCIE_REFCLKN	A12
PCIE_REFCLKP	B12
PCIE_TDN0	A11
PCIE_TDP0	A10

Table 18: WLBGA Pins Listed by Pin Name (Cont.)

Name	Ball No.
PCIE_TESTN	C11
PCIE_TESTP	B11
PCI_PME_L	E10
PLL_AVDD1P2	B10
PLL_AVSS	D10
PMU_AVSS	B3
RF_SW_CTRL_0	E6
RF_SW_CTRL_1	F6
RF_SW_CTRL_2	F5
RF_SW_CTRL_3	G5
RF_SW_CTRL_4	H5
RF_SW_CTRL_5	F4
RF_SW_CTRL_6	G4
RF_SW_CTRL_7	H4
RF_SW_CTRL_8	H3
RF_SW_CTRL_9	H2
RF_SW_CTRL_10	N10
RF_SW_CTRL_11	N11
RF_SW_CTRL_12	P12
RF_SW_CTRL_13	M10
RF_SW_CTRL_14	M11
RF_SW_CTRL_15	N12
RF_SW_CTRL_16	K9
RF_SW_CTRL_17	L9
RF_SW_CTRL_18	L11
RF_SW_CTRL_19	L12
RXTX_AVDD1P2	D11
RXTX_AVSS	C10
SDIO_CLK	A8
SDIO_CMD	B8
SDIO_DATA_0	B6
SDIO_DATA_1	A5
SDIO_DATA_2	A6
SDIO_DATA_3	A7
SR_PVSS	A1
SR_VDDBAT5V	B1
SR_VLX	A2
SYS_VDDIO	F2
VDDC	B5

Table 18: WLBGA Pins Listed by Pin Name (Cont.)

Name	Ball No.
VDDC	C3
VDDC	C9
VDDC	F12
VDDC	H7
VDDC	H11
VDDC	K6
VDDC	L10
VDDC	N7
VDDC	N9
VDDC_MEM	C4
VDDIO	F10
VDDIO	K8
VDDIO_RF	D6
VDDIO_RF	M9
VDDIO_SD	B7
VOUT_3P3	E2
VOUT_BTLDO2P5	D1
VOUT_CLDO	C2
VOUT_HLDO	B2
VOUT_LNLDO	D2
VOUT_MEMLPLDO	E3
VOUT_PA3P3	G1
VSSC	A3
VSSC	D3
VSSC	D9
VSSC	E7
VSSC	H1
VSSC	H9
VSSC	J7
VSSC	K3
VSSC	M4
VSSC	N8
VSSC	P10
WCC_VDDIO	G3
WL_REG_ON	E4
WPT_1P8	G2
WPT_3P3	E1
WRF_AFE_GND_CORE0	T3
WRF_AFE_GND_CORE1	T10

Table 18: WLBGA Pins Listed by Pin Name (Cont.)

Name	Ball No.
WRF_AFE_VDD1P35_CORE0	U4
WRF_AFE_VDD1P35_CORE1	U9
WRF_EXT_TSSIA_CORE0	R4
WRF_EXT_TSSIA_CORE1	R9
WRF_GENERAL2_GND_CORE0	U3
WRF_GENERAL2_GND_CORE1	U10
WRF_GENERAL_GND_CORE0	T4
WRF_GENERAL_GND_CORE1	T9
WRF_GPAIO_OUT_CORE0	R3
WRF_GPAIO_OUT_CORE1	R10
WRF_PAOUT_2G_CORE0	T1
WRF_PAOUT_2G_CORE1	T12
WRF_PAOUT_5G_CORE0	V2
WRF_PAOUT_5G_CORE1	V11
WRF_PA_GND3P3_CORE0	U2
WRF_PA_GND3P3_CORE1	U11
WRF_PA_VDD3P3_CORE0	V1
WRF_PA_VDD3P3_CORE1	V12
WRF_PMU_VDD1P35_CORE0	V5
WRF_PMU_VDD1P35_CORE1	V8
WRF_RFIN_2G_CORE0	R1
WRF_RFIN_2G_CORE1	R12
WRF_RFIN_5G_CORE0	V3
WRF_RFIN_5G_CORE1	V10
WRF_RX2G_GND_CORE0	R2
WRF_RX2G_GND_CORE1	R11
WRF_RX5G_GND_CORE0	V4
WRF_RX5G_GND_CORE1	V9
WRF_SYNTH_GND_CORE0	T5
WRF_SYNTH_GND_CORE1	T8
WRF_SYNTH_VDD1P2_CORE0	U5
WRF_SYNTH_VDD1P2_CORE1	U8
WRF_SYNTH_VDD3P3_CORE0	R6
WRF_SYNTH_VDD3P3_CORE1	R7
WRF_TXMIX_VDD_CORE0	T2
WRF_TXMIX_VDD_CORE1	T11
WRF_VCO_GND_CORE0	R5
WRF_VCO_GND_CORE1	R8
WRF_XTAL_GND1P2_CORE0	U6

Table 18: WLBGA Pins Listed by Pin Name (Cont.)

Name	Ball No.
WRF_XTAL_VDD1P2_CORE0	U7
WRF_XTAL_VDD1P35_CORE0	T6
WRF_XTAL_VDD1P35_CORE1	T7
WRF_XTAL_XON_CORE0	V6
WRF_XTAL_XOP_CORE0	V7

Table 19 lists the BCM43XX WLCSP coordinates by bump number. For a list of by BCM43XX WLCSP coordinates by bump name, see Table 20 on page 91.

Table 19: WLCSP Coordinates by Bump Number

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
1	SR_PVSS	–2324.9835	3510.958	2324.9835	3510.958
2	SR_PVSS	–2042.1405	3510.958	2042.1405	3510.958
3	SR_PVSS	–1759.2975	3510.958	1759.2975	3510.958
4	VDDC	–1149.3585	3474.373	1149.3585	3474.373
5	VDDC_SUBCORE	–902.9475	3474.373	902.9475	3474.373
6	PLL_AVSS	1990.998	3468.145	–1990.998	3468.145
7	RXTX_AVSS	2324.7	3468.145	–2324.7	3468.145
8	SDIO_DATA_3	803.1915	3429.553	–803.1915	3429.553
9	RF_SW_CTRL_1	355.8465	3419.266	–355.8465	3419.266
10	VDDIO_SD	1095.2325	3399.79	–1095.2325	3399.79
11	SR_VLX	–1900.719	3369.5365	1900.719	3369.5365
12	VSSC	–1617.876	3369.5365	1617.876	3369.5365
13	RF_SW_CTRL_0	159.7275	3368.416	–159.7275	3368.416
14	REFCLKN	1824.498	3355.645	–1824.498	3355.645
15	TDN0	2158.2	3355.645	–2158.2	3355.645
16	SDIO_DATA_1	1289.6775	3343.864	–1289.6775	3343.864
17	RF_SW_CTRL_2	–66.0645	3289.126	66.0645	3289.126
18	VDDC_MEM	–1180.7145	3276.517	1180.7145	3276.517
19	RF_SW_CTRL_9	–911.9385	3274.078	911.9385	3274.078
20	SDIO_CLK	1485.4365	3258.013	–1485.4365	3258.013
21	VDDC_SUBCORE	472.0725	3255.835	–472.0725	3255.835
22	REFCLKP	1990.998	3243.145	–1990.998	3243.145
23	RDN0	2324.7	3243.145	–2324.7	3243.145
24	SR_VDDBAT5V	–2324.9835	3228.115	2324.9835	3228.115
25	SR_VLX	–2042.1405	3228.115	2042.1405	3228.115
26	SR_VLX	–1759.2975	3228.115	1759.2975	3228.115
27	VSSC	814.0815	3227.386	–814.0815	3227.386
28	RF_SW_CTRL_6	–642.9285	3216.487	642.9285	3216.487
29	SDIO_DATA_2	1017.8325	3212.491	–1017.8325	3212.491
30	RF_SW_CTRL_5	–405.0315	3183.79	405.0315	3183.79
31	SDIO_DATA_0	1211.6385	3158.518	–1211.6385	3158.518
32	RF_SW_CTRL_3	–206.5005	3145.063	206.5005	3145.063
33	PLL_AVDD1P2	1824.498	3130.645	–1824.498	3130.645
34	TDP0	2158.2	3130.645	–2158.2	3130.645

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
35	RF_SW_CTRL_8	–1045.1835	3122.464	1045.1835	3122.464
36	VSSC	77.3955	3089.974	–77.3955	3089.974
37	SR_VLX	–1900.719	3086.6935	1900.719	3086.6935
38	SR_VLX	–1617.876	3086.6935	1617.876	3086.6935
39	SDIO_CMD	1395.6885	3078.517	–1395.6885	3078.517
40	VDDC_SUBCORE	706.9365	3057.898	–706.9365	3057.898
41	OTP_VDD33	277.1595	3048.817	–277.1595	3048.817
42	PLL_AVSS	1990.998	3018.145	–1990.998	3018.145
43	RDP0	2324.7	3018.145	–2324.7	3018.145
44	VSSC	–1325.7585	3002.125	1325.7585	3002.125
45	RF_SW_CTRL_7	–910.9575	2974.045	910.9575	2974.045
46	RF_SW_CTRL_4	–391.1085	2956.801	391.1085	2956.801
47	VDDC	1237.0005	2956.252	–1237.0005	2956.252
48	SR_VDDBAT5V	–2324.9835	2945.272	2324.9835	2945.272
49	SR_VDDBAT5V	–2042.1405	2945.272	2042.1405	2945.272
50	SR_VDDBAT5V	–1759.2975	2945.272	1759.2975	2945.272
51	VSSC	–190.7595	2944.084	190.7595	2944.084
52	VDDIO_RF	–714.3255	2917.912	714.3255	2917.912
53	VDDC	25.3485	2894.458	–25.3485	2894.458
54	VSSC	1450.9665	2883.415	–1450.9665	2883.415
55	TESTP	1824.498	2876.8045	–1824.498	2876.8045
56	RXTX_AVDD1P2	2158.2	2876.8045	–2158.2	2876.8045
57	VDDC	328.6215	2815.15	–328.6215	2815.15
58	VSSC	–540.5175	2814.538	540.5175	2814.538
59	LDO_VDD1P5	–2183.562	2803.8505	2183.562	2803.8505
60	LDO_VDD1P5	–1900.719	2803.8505	1900.719	2803.8505
61	VOUT_HLDO	–1617.876	2803.8505	1617.876	2803.8505
62	TESTN	1990.998	2764.309	–1990.998	2764.309
63	VSSC	–1248.2595	2746.156	1248.2595	2746.156
64	VSSC	–931.0725	2740.693	931.0725	2740.693
65	VSSC	–236.6415	2732.764	236.6415	2732.764
66	VSSC	1601.2125	2731.234	–1601.2125	2731.234
67	VDDIO_RF	146.3445	2724.07	–146.3445	2724.07
68	VDDC	871.3395	2699.986	–871.3395	2699.986
69	VDDC	623.8125	2681.014	–623.8125	2681.014
70	JTAG_SEL	1071.0855	2678.044	–1071.0855	2678.044

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
71	LDO_VDD1P5	–2324.9835	2662.429	2324.9835	2662.429
72	LDO_VDD1P5	–2042.1405	2662.429	2042.1405	2662.429
73	LDO_VDD1P5	–1759.2975	2662.429	1759.2975	2662.429
74	VDDC_SUBCORE	1402.9965	2684.884	–1402.9965	2684.884
75	VDDIO_RF	–59.1615	2613.514	59.1615	2613.514
76	VOUT_CLDO	–2183.562	2521.0075	2183.562	2521.0075
77	VOUT_CLDO_SENSE	–1900.719	2521.0075	1900.719	2521.0075
78	PMU_AVSS	–1617.876	2521.0075	1617.876	2521.0075
79	GPIO_19	2192.0085	2481.88	–2192.0085	2481.88
80	PCIE_CLKREQ_L	1517.3055	2461.972	–1517.3055	2461.972
81	VSSC	–1244.6235	2459.227	1244.6235	2459.227
82	VSSC	–931.0725	2457.4	931.0725	2457.4
83	VDDC	1053.5625	2455.663	–1053.5625	2455.663
84	VSSC	–547.1775	2422.228	547.1775	2422.228
85	VSSC	–147.1815	2422.228	147.1815	2422.228
86	PCI_PME_L	1707.2055	2395.642	–1707.2055	2395.642
87	VOUT_CLDO	–2324.9835	2379.586	2324.9835	2379.586
88	VOUT_CLDO	–2042.1405	2379.586	2042.1405	2379.586
89	VSSC	–1759.2975	2379.586	1759.2975	2379.586
90	VDDIO	1236.9825	2375.887	–1236.9825	2375.887
91	GPIO_18	2032.4205	2360.632	–2032.4205	2360.632
92	VDDC_SUBCORE	313.4925	2288.677	–313.4925	2288.677
93	PERST_L	1416.4965	2287.03	–1416.4965	2287.03
94	VOUT_BTLDO2P5	–2183.562	2238.1645	2183.562	2238.1645
95	VOUT_CLDO	–1900.719	2238.1645	1900.719	2238.1645
96	VOUT_LNLDO	–1617.876	2238.1645	1617.876	2238.1645
97	VSSC	–347.1795	2222.221	347.1795	2222.221
98	VSSC	–144.0675	2136.145	144.0675	2136.145
99	WPT_3P3	–2324.9835	2096.743	2324.9835	2096.743
100	LDO_VDDBAT5V	–2042.1405	2096.743	2042.1405	2096.743
101	VSSC	1401.5385	2087.374	–1401.5385	2087.374
102	GPIO_17	1609.0785	2075.647	–1609.0785	2075.647
103	VDDC	–1089.8325	2072.641	1089.8325	2072.641
104	VSSC	–549.5175	2057.926	549.5175	2057.926
105	VSSC	352.8225	2022.223	–352.8225	2022.223
106	VSSC	652.8195	2022.223	–652.8195	2022.223

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
107	VSSC	1052.8155	2022.223	–1052.8155	2022.223
108	VOUT_3P3	–2183.562	1955.3215	2183.562	1955.3215
109	LDO_VDDBAT5V	–1900.719	1955.3215	1900.719	1955.3215
110	VSSC	–1617.876	1955.3215	1617.876	1955.3215
111	VDDIO	1244.0385	1954.624	–1244.0385	1954.624
112	VDDC_SUBCORE	–59.5125	1953.508	59.5125	1953.508
113	VDDC_SUBCORE	–1289.5335	1940.872	1289.5335	1940.872
114	VDDC_SUBCORE	–877.2075	1936.552	877.2075	1936.552
115	GPIO_16	1486.6785	1902.847	–1486.6785	1902.847
116	GPIO_14	1686.5055	1887.637	–1686.5055	1887.637
117	GPIO_6	2242.8045	1851.484	–2242.8045	1851.484
118	GPIO_5	2041.6455	1850.575	–2041.6455	1850.575
119	VSSC	852.8175	1822.225	–852.8175	1822.225
120	LDO_VDDBAT5V	–2324.9835	1813.9	2324.9835	1813.9
121	LDO_VDDBAT5V	–2042.1405	1813.9	2042.1405	1813.9
122	VOUT_MEMLPLDO	–1476.4545	1813.9	1476.4545	1813.9
123	GPIO_15	1353.6405	1745.311	–1353.6405	1745.311
124	VDDC	–826.1055	1741.918	826.1055	1741.918
125	VDDC	–501.4755	1729.606	501.4755	1729.606
126	BT_VDDC	–1155.0825	1676.821	1155.0825	1676.821
127	LDO_VDDBAT5V	–2183.562	1672.4785	2183.562	1672.4785
128	LDO_VDDBAT5V	–1900.719	1672.4785	1900.719	1672.4785
129	WL_REG_ON	–1617.876	1672.4785	1617.876	1672.4785
130	VSSC	252.8145	1622.227	–252.8145	1622.227
131	VSSC	652.8195	1622.227	–652.8195	1622.227
132	VSSC	1052.8155	1622.227	–1052.8155	1622.227
133	VDDC	–332.0775	1621.264	332.0775	1621.264
134	GPIO_0	2186.0775	1615.27	–2186.0775	1615.27
135	VDDC_SUBCORE	1623.4065	1582.717	–1623.4065	1582.717
136	VSSC	–721.5615	1568.605	721.5615	1568.605
137	VSSC	–1008.9315	1539.877	1008.9315	1539.877
138	VOUT_PA3P3	–2324.9835	1531.057	2324.9835	1531.057
139	LDO_VDDBAT5V	–2042.1405	1531.057	2042.1405	1531.057
140	BT_REG_ON	–1476.4545	1531.057	1476.4545	1531.057
141	VDDC	1227.3885	1523.803	–1227.3885	1523.803
142	VSSC	–526.1625	1521.814	526.1625	1521.814

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
143	VDDC_SUBCORE	–103.5225	1502.455	103.5225	1502.455
144	GPIO_13	1436.9625	1473.142	–1436.9625	1473.142
145	VSSC	452.8215	1422.22	–452.8215	1422.22
146	PACKAGE OPTION_0	2189.0025	1411.834	–2189.0025	1411.834
147	VOUT_PA3P3	–2183.562	1389.6355	2183.562	1389.6355
148	WCC_VDDIO	–1617.876	1389.6355	1617.876	1389.6355
149	BT_USB_VSSO	–804.1275	1384.708	804.1275	1384.708
150	VDDC_PHY	1610.8245	1326.694	–1610.8245	1326.694
151	VDDC_PHY	2022.7275	1294.231	–2022.7275	1294.231
152	VSSC	–624.9645	1275.367	624.9645	1275.367
153	VOUT_PA3P3	–2324.9835	1248.214	2324.9835	1248.214
154	VOUT_PA3P3	–2042.1405	1248.214	2042.1405	1248.214
155	SYS_VDDIO	–1759.2975	1248.214	1759.2975	1248.214
156	VSSC	–147.1815	1222.222	147.1815	1222.222
157	VSSC	252.8145	1222.222	–252.8145	1222.222
158	VSSC	652.8195	1222.222	–652.8195	1222.222
159	VSSC	1052.8155	1222.222	–1052.8155	1222.222
160	PACKAGE OPTION_1	2203.5915	1205.86	–2203.5915	1205.86
161	VSSC	–1359.4185	1205.275	1359.4185	1205.275
162	BT_USB_DN	–970.3215	1173.973	970.3215	1173.973
163	AVDD_BBPLL	–439.6095	1180.606	439.6095	1180.606
164	GPIO_11	1515.6585	1150.177	–1515.6585	1150.177
165	VOUT_PA3P3	–2183.562	1106.7925	2183.562	1106.7925
166	WPT_1P8	–1900.719	1106.7925	1900.719	1106.7925
167	GPIO_10	1729.5615	1091.488	–1729.5615	1091.488
168	VSSC	52.8165	1022.224	–52.8165	1022.224
169	VSSC	852.8175	1022.224	–852.8175	1022.224
170	GPIO_1	2200.4415	1003.765	–2200.4415	1003.765
171	BT_USB_DP	–804.1275	984.703	804.1275	984.703
172	VOUT_PA3P3_SENSE	–2324.9835	965.371	2324.9835	965.371
173	VOUT_PA3P3	–2042.1405	965.371	2042.1405	965.371
174	VDDIO	1316.2095	959.107	–1316.2095	959.107
175	GPIO_12	1555.4745	952.276	–1555.4745	952.276
176	VSSC	–594.6975	927.337	594.6975	927.337
177	BT_USB_VDDO	–1146.1005	895.864	1146.1005	895.864
178	VSSC	–1347.0525	879.511	1347.0525	879.511

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
179	VSSC	–1584.3195	871.042	1584.3195	871.042
180	AVSS_BBPLL	–408.9015	845.671	408.9015	845.671
181	GPIO_9	1897.0065	828.481	–1897.0065	828.481
182	VSSC	–147.1815	822.226	147.1815	822.226
183	VSSC	252.8145	822.226	–252.8145	822.226
184	VSSC	652.8195	822.226	–652.8195	822.226
185	VSSC	1052.8155	822.226	–1052.8155	822.226
186	GPIO_2	2203.3755	801.364	–2203.3755	801.364
187	BT_VDDC	–2323.1835	751.306	2323.1835	751.306
188	BT_VDDC	–1743.7005	738.463	1743.7005	738.463
189	VSSC	1445.9265	718.717	–1445.9265	718.717
190	BT_PCM_CLK	–1344.9285	669.514	1344.9285	669.514
191	BT_PCM_SYNC	–1144.9395	662.26	1144.9395	662.26
192	BT_PCM_IN	–1545.6375	657.913	1545.6375	657.913
193	GPIO_8	1894.4145	627.853	–1894.4145	627.853
194	VSSC	–567.9315	624.361	567.9315	624.361
195	VSSC	–2168.8155	623.857	2168.8155	623.857
196	VSSC	452.8215	622.228	–452.8215	622.228
197	PACKAGE OPTION_2	2221.9155	598.09	–2221.9155	598.09
198	VDDC_SUBCORE	960.7005	578.227	–960.7005	578.227
199	VDDC_SUBCORE	–127.7415	576.841	127.7415	576.841
200	VSSC	–848.7585	539.032	848.7585	539.032
201	VDDC	1444.7205	517.135	–1444.7205	517.135
202	VDDC	1194.3945	502.897	–1194.3945	502.897
203	BT_PCM_OUT	–1348.1415	443.632	1348.1415	443.632
204	GPIO_7	1956.1455	436.603	–1956.1455	436.603
205	BT_SLIMBUS_DT	–1545.4035	403.222	1545.4035	403.222
206	PACKAGE OPTION_3	2221.9155	398.065	–2221.9155	398.065
207	BT_VDDO	–710.7705	393.178	710.7705	393.178
208	BT_UART_CTS_N	–1175.0355	339.097	1175.0355	339.097
209	BT_SLIMBUS_CK	–1736.1315	330.043	1736.1315	330.043
210	VDDC_PHY	432.5265	318.271	–432.5265	318.271
211	VDDC	–210.0195	304.6	210.0195	304.6
212	VDDC_PHY	1195.1595	302.395	–1195.1595	302.395
213	VDDC_PHY	750.9195	301.216	–750.9195	301.216
214	VSSC	–416.7045	297.931	416.7045	297.931

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
215	VDDC	187.4025	293.314	–187.4025	293.314
216	BT_I2S_WS	–2299.1535	272.317	2299.1535	272.317
217	GPIO_3	1905.3045	235.651	–1905.3045	235.651
218	VDDC_PHY	1523.5065	231.277	–1523.5065	231.277
219	VSSC	952.8165	222.223	–952.8165	222.223
220	VDDIO	2242.7595	194.035	–2242.7595	194.035
221	BT_VDDO	–683.4285	192.847	683.4285	192.847
222	BT_I2S_CLK	–2118.2175	187.006	2118.2175	187.006
223	BT_I2S_DI	–1632.9195	155.65	1632.9195	155.65
224	BT_UART_RTS_N	–1213.7805	138.37	1213.7805	138.37
225	BT_UART_TXD	–1413.0495	116.635	1413.0495	116.635
226	BT_I2S_DO	–1906.5915	102.757	1906.5915	102.757
227	VSSC	1725.0705	86.305	–1725.0705	86.305
228	VDDIO	2069.0415	63.76	–2069.0415	63.76
229	VSSC	–147.1815	22.225	147.1815	22.225
230	VSSC	252.8145	22.225	–252.8145	22.225
231	VSSC	652.8195	22.225	–652.8195	22.225
232	VSSC	1052.8155	22.225	–1052.8155	22.225
233	CLK_REQ	–641.2275	–4.262	641.2275	–4.262
234	VDDIO	2260.3995	–6.296	–2260.3995	–6.296
235	BT_UART_RXD	–1546.3755	–36.257	1546.3755	–36.257
236	BT_VDDC_ISO_2	–1768.0995	–42.053	1768.0995	–42.053
237	VSSC	1430.9865	–88.052	–1430.9865	–88.052
238	GPIO_4	1809.6885	–100.868	–1809.6885	–100.868
239	BT_GPIO_2	–1244.2005	–115.25	1244.2005	–115.25
240	VSSC	452.8215	–177.773	–452.8215	–177.773
241	BT_HOST_WAKE	–718.0335	–189.689	718.0335	–189.689
242	VSSC	–2103.8535	–202.928	2103.8535	–202.928
243	VSSC	2166.6915	–206.033	–2166.6915	–206.033
244	VSSC	–2307.6405	–208.157	2307.6405	–208.157
245	VSSC	–147.1815	–277.772	147.1815	–277.772
246	VDDC	1430.3925	–289.103	–1430.3925	–289.103
247	VSSC	–1284.5655	–320.306	1284.5655	–320.306
248	BT_TM1	–1051.1145	–354.803	1051.1145	–354.803
249	VSSC	–1547.1855	–377.78	1547.1855	–377.78
250	VSSC	252.8145	–377.78	–252.8145	–377.78

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
251	VSSC	652.8195	–377.78	–652.8195	–377.78
252	VSSC	1052.8155	–377.78	–1052.8155	–377.78
253	BT_DEV_WAKE	–843.3225	–383.972	843.3225	–383.972
254	VSSC	1869.3945	–397.013	–1869.3945	–397.013
255	VDDC_PHY	2260.4265	–401.018	–2260.4265	–401.018
256	BT_GPIO_3	–370.3275	–415.238	370.3275	–415.238
257	VSSC	–2105.0955	–422.852	2105.0955	–422.852
258	VDDC_PHY	1525.0275	–465.539	–1525.0275	–465.539
259	VSSC	–1940.4855	–541.679	1940.4855	–541.679
260	VSSC	852.8175	–577.778	–852.8175	–577.778
261	VSSC	–836.6625	–587.948	836.6625	–587.948
262	VDDC_PHY	2259.6165	–601.016	–2259.6165	–601.016
263	BT_GPIO_5	–526.5945	–612.914	526.5945	–612.914
264	VSSC	104.8725	–618.683	–104.8725	–618.683
265	VDDC_PHY	1316.4255	–649.859	–1316.4255	–649.859
266	BT_VDDC_ISO_1	–1126.1025	–657.257	1126.1025	–657.257
267	VSSC	–147.1815	–677.777	147.1815	–677.777
268	BT_VDDC	–2034.7605	–719.204	2034.7605	–719.204
269	BT_VDDC	–1833.7635	–719.204	1833.7635	–719.204
270	BT_VDDC	–1317.7575	–719.204	1317.7575	–719.204
271	RF_SW_CTRL_16	2055.5325	–753.665	–2055.5325	–753.665
272	VSSC	1608.2505	–757.58	–1608.2505	–757.58
273	VDDIO_RF	1848.8385	–762.872	–1848.8385	–762.872
274	VSSC	252.8145	–777.776	–252.8145	–777.776
275	VSSC	652.8195	–777.776	–652.8195	–777.776
276	VSSC	1052.8155	–777.776	–1052.8155	–777.776
277	LPO_IN	–872.9685	–787.064	872.9685	–787.064
278	RF_SW_CTRL_17	2255.8995	–802.22	–2255.8995	–802.22
279	VSSC	–526.5945	–818.699	526.5945	–818.699
280	VSSC	1737.2025	–946.94	–1737.2025	–946.94
281	RF_SW_CTRL_15	1957.5405	–956.624	–1957.5405	–956.624
282	VSSC	452.8215	–977.774	–452.8215	–977.774
283	BT_AGPIO	–2284.614	–985.5725	2284.614	–985.5725
284	VSSC	–956.0385	–1035.194	956.0385	–1035.194
285	BT_DVSS	–1661.112	–1003.4645	1661.112	–1003.4645
286	RF_SW_CTRL_19	2259.6165	–1004.198	–2259.6165	–1004.198

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
287	BT_IFVDD1P2	–1861.11	–1069.0385	1861.11	–1069.0385
288	VSSC	–656.1135	–1105.583	656.1135	–1105.583
289	BT_PLLVSS	–2143.332	–1127.7545	2143.332	–1127.7545
290	RF_SW_CTRL_14	2054.3715	–1133.006	–2054.3715	–1133.006
291	BT_GPIO_4	–431.9235	–1139.108	431.9235	–1139.108
292	VDDIO_RF	1716.7275	–1159.457	–1716.7275	–1159.457
293	VDDC	1515.9465	–1174.442	–1515.9465	–1174.442
294	VSSC	–1239.1785	–1177.772	1239.1785	–1177.772
295	VSSC	–147.1815	–1177.772	147.1815	–1177.772
296	VSSC	252.8145	–1177.772	–252.8145	–1177.772
297	VSSC	652.8195	–1177.772	–652.8195	–1177.772
298	VSSC	1052.8155	–1177.772	–1052.8155	–1177.772
299	RF_SW_CTRL_18	2259.6165	–1204.646	–2259.6165	–1204.646
300	VDDC_PHY	1317.7395	–1282.658	–1317.7395	–1282.658
301	BT_PLLVDD1P2	–1839.1095	–1313.375	1839.1095	–1313.375
302	RF_SW_CTRL_12	1983.6855	–1320.863	–1983.6855	–1320.863
303	BT_PAVDD2P5	–2183.022	–1327.7525	2183.022	–1327.7525
304	VDDC_PHY	–704.5875	–1353.767	704.5875	–1353.767
305	VSSC	–504.3915	–1371.704	504.3915	–1371.704
306	VSSC	852.8175	–1377.779	–852.8175	–1377.779
307	VSSC	1789.2315	–1388.264	–1789.2315	–1388.264
308	VSSC	650.4255	–1448.348	–650.4255	–1448.348
309	VDDIO_RF	1599.8985	–1457.708	–1599.8985	–1457.708
310	VSSC	–1244.9115	–1468.796	1244.9115	–1468.796
311	BT_LNAVSS	–1786.383	–1513.373	1786.383	–1513.373
312	RF_SW_CTRL_13	1997.1405	–1520.888	–1997.1405	–1520.888
313	BT_PAVSS	–2183.022	–1527.7505	2183.022	–1527.7505
314	VSSC	1014.1065	–1535.504	–1014.1065	–1535.504
315	VSSC	–1045.0755	–1458.194	1045.0755	–1458.194
316	VSSC	–155.2635	–1566.122	155.2635	–1566.122
317	VDDC_PHY	1326.0375	–1584.518	–1326.0375	–1584.518
318	VSSC	–409.3875	–1587.434	409.3875	–1587.434
319	RF_SW_CTRL_11	1812.5145	–1599.647	–1812.5145	–1599.647
320	VSSC	–695.5425	–1635.269	695.5425	–1635.269
321	VDDC_PHY	297.8595	–1651.856	–297.8595	–1651.856
322	VDDC	1612.9125	–1658.012	–1612.9125	–1658.012

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
323	BT_VCOVSS	–1429.875	–1664.3705	1429.875	–1664.3705
324	BT_LNAVDD1P2	–1786.383	–1713.371	1786.383	–1713.371
325	VDDC_PHY	2005.9605	–1721.453	–2005.9605	–1721.453
326	BT_RF	–2224.305	–1727.7485	2224.305	–1727.7485
327	VDDC	145.7775	–1816.043	–145.7775	–1816.043
328	RF_SW_CTRL_10	2179.4355	–1821.335	–2179.4355	–1821.335
329	VSSC	1493.8965	–1857.677	–1493.8965	–1857.677
330	BT_VCOVDD1P2	–1429.875	–1864.3685	1429.875	–1864.3685
331	VDDC	–238.1445	–1873.355	238.1445	–1873.355
332	WRF_VCO_GND_CORE0	–615.0735	–2128.406	615.0735	–2128.406
333	WRF_VCO_GND_CORE1	615.0735	–2128.406	–615.0735	–2128.406
334	WRF_TIA_GND_CORE0	–1394.2575	–2166.1205	1394.2575	–2166.1205
335	WRF_TIA_GND_CORE1	1394.2575	–2166.1205	–1394.2575	–2166.1205
336	WRF_EXT_TSSIA_CORE0	–1664.5005	–2173.5725	1664.5005	–2173.5725
337	WRF_EXT_TSSIA_CORE1	1664.5005	–2173.5725	–1664.5005	–2173.5725
338	WRF_SYNTH_VDD3P3_CORE0	–256.2705	–2183.5445	256.2705	–2183.5445
339	WRF_SYNTH_VDD3P3_CORE1	256.2705	–2183.5445	–256.2705	–2183.5445
340	WRF_RFIN_2G_CORE0	–2179.584	–2202.6515	2179.584	–2202.6515
341	WRF_RFIN_2G_CORE1	2179.584	–2202.6515	–2179.584	–2202.6515
342	WRF_RX2G_GND_CORE0	–1871.0415	–2310.1475	1871.0415	–2310.1475
343	WRF_RX2G_GND_CORE1	1871.0415	–2310.1475	–1871.0415	–2310.1475
344	WRF_SYNTH_GND_CORE0	–117.909	–2332.3685	117.909	–2332.3685
345	WRF_SYNTH_GND_CORE1	117.909	–2332.3685	–117.909	–2332.3685
346	WRF_AFE_GND_CORE0	–1664.5005	–2373.5705	1664.5005	–2373.5705
347	WRF_AFE_GND_CORE1	1664.5005	–2373.5705	–1664.5005	–2373.5705
348	WRF_GENERAL_GND_CORE0	–973.53	–2558.5565	973.53	–2558.5565
349	WRF_GENERAL_GND_CORE1	973.53	–2558.5565	–973.53	–2558.5565
350	WRF_GPAIO_OUT_CORE0	–1664.514	–2585.381	1664.514	–2585.381
351	WRF_GPAIO_OUT_CORE1	1664.514	–2585.381	–1664.514	–2585.381
352	WRF_SYNTH_GND_CORE0	–593.442	–2656.238	593.442	–2656.238
353	WRF_SYNTH_GND_CORE1	593.442	–2656.238	–593.442	–2656.238
354	WRF_PAOUT_2G_CORE0	–2255.4855	–2710.7285	2255.4855	–2710.7285
355	WRF_PAOUT_2G_CORE1	2255.4855	–2710.7285	–2255.4855	–2710.7285
356	WRF_TXMIX_VDD_CORE0	–1910.1375	–2730.1685	1910.1375	–2730.1685
357	WRF_TXMIX_VDD_CORE1	1910.1375	–2730.1685	–1910.1375	–2730.1685
359	WRF_GENERAL2_GND_CORE0	–1592.847	–2787.26	1592.847	–2787.26

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
359	WRF_GENERAL2_GND_CORE1	1592.847	–2787.26	–1592.847	–2787.26
360	WRF_SYNTH_VDD1P2_CORE0	–682.668	–2897.429	682.668	–2897.429
361	WRF_SYNTH_VDD1P2_CORE1	682.668	–2897.429	–682.668	–2897.429
362	WRF_PA_GND3P3_CORE0	–1905.1515	–2930.171	1905.1515	–2930.171
363	WRF_PA_GND3P3_CORE1	1905.1515	–2930.171	–1905.1515	–2930.171
364	WRF_XTAL_VDD1P35_CORE0	–30.6045	–2995.052	30.6045	–2995.052
365	WRF_PMU_VDD1P35_CORE0	–621.1395	–3297.425	621.1395	–3297.425
366	WRF_PMU_VDD1P35_CORE1	621.1395	–3297.425	–621.1395	–3297.425
367	WRF_XTAL_VDD1P35_CORE1	169.3935	–3108.3395	–169.3935	–3108.3395
368	WRF_PA_GND3P3_CORE0	–1726.011	–3112.493	1726.011	–3112.493
369	WRF_PA_GND3P3_CORE1	1726.011	–3112.493	–1726.011	–3112.493
370	WRF_PA_GND3P3_CORE0	–1951.7715	–3125.9165	1951.7715	–3125.9165
371	WRF_PA_GND3P3_CORE1	1951.7715	–3125.9165	–1951.7715	–3125.9165
372	WRF_XTAL_GND1P2_CORE0	–230.6025	–3157.277	230.6025	–3157.277
373	WRF_PA_GND3P3_CORE0	–1507.2705	–3168.824	1507.2705	–3168.824
374	WRF_PA_GND3P3_CORE1	1507.2705	–3168.824	–1507.2705	–3168.824
375	WRF_AFE_VDD1P35_CORE0	–791.217	–3192.0755	791.217	–3192.0755
376	WRF_AFE_VDD1P35_CORE1	791.217	–3192.0755	–791.217	–3192.0755
377	WRF_PA_VDD3P3_CORE0	–2330.0145	–3196.301	2330.0145	–3196.301
378	WRF_PA_VDD3P3_CORE1	2330.0145	–3196.301	–2330.0145	–3196.301
379	WRF_XTAL_VDD1P2_CORE0	0	–3268.031	0	–3268.031
380	WRF_PMU_VDD1P35_CORE0	–653.472	–3497.423	653.472	–3497.423
381	WRF_PMU_VDD1P35_CORE1	653.472	–3497.423	–653.472	–3497.423
382	WRF_PA_VDD3P3_CORE0	–2287.404	–3391.763	2287.404	–3391.763
383	WRF_PA_VDD3P3_CORE1	2287.404	–3391.763	–2287.404	–3391.763
384	WRF_PA_VDD3P3_CORE0	–1988.37	–3407.1665	1988.37	–3407.1665
385	WRF_PA_VDD3P3_CORE1	1988.37	–3407.1665	–1988.37	–3407.1665
386	WRF_RX5G_GND_CORE0	–941.4675	–3455.411	941.4675	–3455.411
387	WRF_RX5G_GND_CORE1	941.4675	–3455.411	–941.4675	–3455.411
388	WRF_RFIN_5G_CORE0	–1336.0365	–3462.0845	1336.0365	–3462.0845
389	WRF_RFIN_5G_CORE1	1336.0365	–3462.0845	–1336.0365	–3462.0845
390	WRF_XTAL_XON_CORE0	–61.704	–3483.752	61.704	–3483.752
391	WRF_XTAL_XOP_CORE0	–261.702	–3495.6455	261.702	–3495.6455
392	WRF_PA_VDD3P3_CORE0	–2265.4125	–3591.761	2265.4125	–3591.761
393	WRF_PA_VDD3P3_CORE1	2265.4125	–3591.761	–2265.4125	–3591.761
394	WRF_PAOUT_5G_CORE0	–1729.4715	–3614.351	1729.4715	–3614.351

Table 19: WLCSP Coordinates by Bump Number (Cont.)

Bump Number	Net Name	Package Top View (Bumps Facing Down) Package Center (0, 0)		Package Bottom View (Bumps Facing Up) Package Center (0, 0)	
		Bump X	Bump Y	Bump X	Bump Y
395	WRF_PAOUT_5G_CORE1	1729.4715	–3614.351	–1729.4715	–3614.351
396	WRF_AFE_GND_core0	–1277.3295	–2630.6105	1277.3295	–2630.6105
397	WRF_AFE_GND_core1	1277.33	–2630.61	–1277.3295	–2630.6105

Table 20 lists the BCM43XX WLCSP coordinates by bump name. For a list of by BCM43XX WLBGA coordinates by bump number, see Table 19 on page 80.

Table 20: WLCSP Coordinates Listed by Name

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
AVDD_BBPLL	163	–439.6095	1180.606	439.6095	1180.606
AVSS_BBPLL	180	–408.9015	845.671	408.9015	845.671
BT_AGPIO	283	–2284.614	–985.5725	2284.614	–985.5725
BT_DEV_WAKE	253	–843.3225	–383.972	843.3225	–383.972
BT_DVSS	285	–1661.112	–1003.4645	1661.112	–1003.4645
BT_GPIO_2	239	–1244.2005	–115.25	1244.2005	–115.25
BT_GPIO_3	256	–370.3275	–415.238	370.3275	–415.238
BT_GPIO_4	291	–431.9235	–1139.108	431.9235	–1139.108
BT_GPIO_5	263	–526.5945	–612.914	526.5945	–612.914
BT_HOST_WAKE	241	–718.0335	–189.689	718.0335	–189.689
BT_I2S_CLK	222	–2118.2175	187.006	2118.2175	187.006
BT_I2S_DI	223	–1632.9195	155.65	1632.9195	155.65
BT_I2S_DO	226	–1906.5915	102.757	1906.5915	102.757
BT_I2S_WS	216	–2299.1535	272.317	2299.1535	272.317
BT_IFVDD1P2	287	–1861.11	–1069.0385	1861.11	–1069.0385
BT_LNAVDD1P2	324	–1786.383	–1713.371	1786.383	–1713.371
BT_LNAVSS	311	–1786.383	–1513.373	1786.383	–1513.373
BT_PAVDD2P5	303	–2183.022	–1327.7525	2183.022	–1327.7525
BT_PAVSS	313	–2183.022	–1527.7505	2183.022	–1527.7505
BT_PCM_CLK	190	–1344.9285	669.514	1344.9285	669.514
BT_PCM_IN	192	–1545.6375	657.913	1545.6375	657.913
BT_PCM_OUT	203	–1348.1415	443.632	1348.1415	443.632
BT_PCM_SYNC	191	–1144.9395	662.26	1144.9395	662.26
BT_PLLVDD1P2	301	–1839.1095	–1313.375	1839.1095	–1313.375
BT_PLLVSS	289	–2143.332	–1127.7545	2143.332	–1127.7545

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
BT_REG_ON	140	–1476.4545	1531.057	1476.4545	1531.057
BT_RF	326	–2224.305	–1727.7485	2224.305	–1727.7485
BT_SLIMBUS_CK	209	–1736.1315	330.043	1736.1315	330.043
BT_SLIMBUS_DT	205	–1545.4035	403.222	1545.4035	403.222
BT_TM1	248	–1051.1145	–354.803	1051.1145	–354.803
BT_UART_CTS_N	208	–1175.0355	339.097	1175.0355	339.097
BT_UART_RTS_N	224	–1213.7805	138.37	1213.7805	138.37
BT_UART_RXD	235	–1546.3755	–36.257	1546.3755	–36.257
BT_UART_TXD	225	–1413.0495	116.635	1413.0495	116.635
BT_USB_DN	162	–970.3215	1173.973	970.3215	1173.973
BT_USB_DP	171	–804.1275	984.703	804.1275	984.703
BT_USB_VDDO	177	–1146.1005	895.864	1146.1005	895.864
BT_USB_VSSO	149	–804.1275	1384.708	804.1275	1384.708
BT_VCOVDD1P2	330	–1429.875	–1864.3685	1429.875	–1864.3685
BT_VCOVSS	323	–1429.875	–1664.3705	1429.875	–1664.3705
BT_VDDC	126	–1155.0825	1676.821	1155.0825	1676.821
BT_VDDC	187	–2323.1835	751.306	2323.1835	751.306
BT_VDDC	188	–1743.7005	738.463	1743.7005	738.463
BT_VDDC	268	–2034.7605	–719.204	2034.7605	–719.204
BT_VDDC	269	–1833.7635	–719.204	1833.7635	–719.204
BT_VDDC	270	–1317.7575	–719.204	1317.7575	–719.204
BT_VDDC_ISO_1	266	–1126.1025	–657.257	1126.1025	–657.257
BT_VDDC_ISO_2	236	–1768.0995	–42.053	1768.0995	–42.053
BT_VDDO	207	–710.7705	393.178	710.7705	393.178
BT_VDDO	221	–683.4285	192.847	683.4285	192.847
CLK_REQ	233	–641.2275	–4.262	641.2275	–4.262
GPIO_0	134	2186.0775	1615.27	–2186.0775	1615.27
GPIO_1	170	2200.4415	1003.765	–2200.4415	1003.765
GPIO_2	186	2203.3755	801.364	–2203.3755	801.364
GPIO_3	217	1905.3045	235.651	–1905.3045	235.651
GPIO_4	238	1809.6885	–100.868	–1809.6885	–100.868
GPIO_5	118	2041.6455	1850.575	–2041.6455	1850.575
GPIO_6	117	2242.8045	1851.484	–2242.8045	1851.484
GPIO_7	204	1956.1455	436.603	–1956.1455	436.603
GPIO_8	193	1894.4145	627.853	–1894.4145	627.853
GPIO_9	181	1897.0065	828.481	–1897.0065	828.481

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
GPIO_10	167	1729.5615	1091.488	–1729.5615	1091.488
GPIO_11	164	1515.6585	1150.177	–1515.6585	1150.177
GPIO_12	175	1555.4745	952.276	–1555.4745	952.276
GPIO_13	144	1436.9625	1473.142	–1436.9625	1473.142
GPIO_14	116	1686.5055	1887.637	–1686.5055	1887.637
GPIO_15	123	1353.6405	1745.311	–1353.6405	1745.311
GPIO_16	115	1486.6785	1902.847	–1486.6785	1902.847
GPIO_17	102	1609.0785	2075.647	–1609.0785	2075.647
GPIO_18	91	2032.4205	2360.632	–2032.4205	2360.632
GPIO_19	79	2192.0085	2481.88	–2192.0085	2481.88
JTAG_SEL	70	1071.0855	2678.044	–1071.0855	2678.044
LDO_VDD1P5	59	–2183.562	2803.8505	2183.562	2803.8505
LDO_VDD1P5	60	–1900.719	2803.8505	1900.719	2803.8505
LDO_VDD1P5	71	–2324.9835	2662.429	2324.9835	2662.429
LDO_VDD1P5	72	–2042.1405	2662.429	2042.1405	2662.429
LDO_VDD1P5	73	–1759.2975	2662.429	1759.2975	2662.429
LDO_VDDBAT5V	100	–2042.1405	2096.743	2042.1405	2096.743
LDO_VDDBAT5V	109	–1900.719	1955.3215	1900.719	1955.3215
LDO_VDDBAT5V	120	–2324.9835	1813.9	2324.9835	1813.9
LDO_VDDBAT5V	121	–2042.1405	1813.9	2042.1405	1813.9
LDO_VDDBAT5V	127	–2183.562	1672.4785	2183.562	1672.4785
LDO_VDDBAT5V	128	–1900.719	1672.4785	1900.719	1672.4785
LDO_VDDBAT5V	139	–2042.1405	1531.057	2042.1405	1531.057
LPO_IN	277	–872.9685	–787.064	872.9685	–787.064
OTP_VDD33	41	277.1595	3048.817	–277.1595	3048.817
PACKAGE OPTION_0	146	2189.0025	1411.834	–2189.0025	1411.834
PACKAGE OPTION_1	160	2203.5915	1205.86	–2203.5915	1205.86
PACKAGE OPTION_2	197	2221.9155	598.09	–2221.9155	598.09
PACKAGE OPTION_3	206	2221.9155	398.065	–2221.9155	398.065
PCIE_CLKREQ_L	80	1517.3055	2461.972	–1517.3055	2461.972
PCI_PME_L	86	1707.2055	2395.642	–1707.2055	2395.642
PERST_L	93	1416.4965	2287.03	–1416.4965	2287.03
PLL_AVDD1P2	33	1824.498	3130.645	–1824.498	3130.645
PLL_AVSS	6	1990.998	3468.145	–1990.998	3468.145
PLL_AVSS	42	1990.998	3018.145	–1990.998	3018.145
PMU_AVSS	78	–1617.876	2521.0075	1617.876	2521.0075

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
RDN0	23	2324.7	3243.145	–2324.7	3243.145
RDP0	43	2324.7	3018.145	–2324.7	3018.145
REFCLKN	14	1824.498	3355.645	–1824.498	3355.645
REFCLKP	22	1990.998	3243.145	–1990.998	3243.145
RF_SW_CTRL_0	13	159.7275	3368.416	–159.7275	3368.416
RF_SW_CTRL_1	9	355.8465	3419.266	–355.8465	3419.266
RF_SW_CTRL_2	17	–66.0645	3289.126	66.0645	3289.126
RF_SW_CTRL_3	32	–206.5005	3145.063	206.5005	3145.063
RF_SW_CTRL_4	46	–391.1085	2956.801	391.1085	2956.801
RF_SW_CTRL_5	30	–405.0315	3183.79	405.0315	3183.79
RF_SW_CTRL_6	28	–642.9285	3216.487	642.9285	3216.487
RF_SW_CTRL_7	45	–910.9575	2974.045	910.9575	2974.045
RF_SW_CTRL_8	35	–1045.1835	3122.464	1045.1835	3122.464
RF_SW_CTRL_9	19	–911.9385	3274.078	911.9385	3274.078
RF_SW_CTRL_10	328	2179.4355	–1821.335	–2179.4355	–1821.335
RF_SW_CTRL_11	319	1812.5145	–1599.647	–1812.5145	–1599.647
RF_SW_CTRL_12	302	1983.6855	–1320.863	–1983.6855	–1320.863
RF_SW_CTRL_13	312	1997.1405	–1520.888	–1997.1405	–1520.888
RF_SW_CTRL_14	290	2054.3715	–1133.006	–2054.3715	–1133.006
RF_SW_CTRL_15	281	1957.5405	–956.624	–1957.5405	–956.624
RF_SW_CTRL_16	271	2055.5325	–753.665	–2055.5325	–753.665
RF_SW_CTRL_17	278	2255.8995	–802.22	–2255.8995	–802.22
RF_SW_CTRL_18	299	2259.6165	–1204.646	–2259.6165	–1204.646
RF_SW_CTRL_19	286	2259.6165	–1004.198	–2259.6165	–1004.198
RXTX_AVDD1P2	56	2158.2	2876.8045	–2158.2	2876.8045
RXTX_AVSS	7	2324.7	3468.145	–2324.7	3468.145
SDIO_CLK	20	1485.4365	3258.013	–1485.4365	3258.013
SDIO_CMD	39	1395.6885	3078.517	–1395.6885	3078.517
SDIO_DATA_0	31	1211.6385	3158.518	–1211.6385	3158.518
SDIO_DATA_1	16	1289.6775	3343.864	–1289.6775	3343.864
SDIO_DATA_2	29	1017.8325	3212.491	–1017.8325	3212.491
SDIO_DATA_3	8	803.1915	3429.553	–803.1915	3429.553
SR_PVSS	1	–2324.9835	3510.958	2324.9835	3510.958
SR_PVSS	2	–2042.1405	3510.958	2042.1405	3510.958
SR_PVSS	3	–1759.2975	3510.958	1759.2975	3510.958
SR_VDDBAT5V	24	–2324.9835	3228.115	2324.9835	3228.115

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
SR_VDDBAT5V	48	–2324.9835	2945.272	2324.9835	2945.272
SR_VDDBAT5V	49	–2042.1405	2945.272	2042.1405	2945.272
SR_VDDBAT5V	50	–1759.2975	2945.272	1759.2975	2945.272
SR_VLX	11	–1900.719	3369.5365	1900.719	3369.5365
SR_VLX	25	–2042.1405	3228.115	2042.1405	3228.115
SR_VLX	26	–1759.2975	3228.115	1759.2975	3228.115
SR_VLX	37	–1900.719	3086.6935	1900.719	3086.6935
SR_VLX	38	–1617.876	3086.6935	1617.876	3086.6935
SYS_VDDIO	155	–1759.2975	1248.214	1759.2975	1248.214
TDN0	15	2158.2	3355.645	–2158.2	3355.645
TDP0	34	2158.2	3130.645	–2158.2	3130.645
TESTN	62	1990.998	2764.309	–1990.998	2764.309
TESTP	55	1824.498	2876.8045	–1824.498	2876.8045
VDDC	4	–1149.3585	3474.373	1149.3585	3474.373
VDDC	47	1237.0005	2956.252	–1237.0005	2956.252
VDDC	53	25.3485	2894.458	–25.3485	2894.458
VDDC	57	328.6215	2815.15	–328.6215	2815.15
VDDC	68	871.3395	2699.986	–871.3395	2699.986
VDDC	69	623.8125	2681.014	–623.8125	2681.014
VDDC	83	1053.5625	2455.663	–1053.5625	2455.663
VDDC	103	–1089.8325	2072.641	1089.8325	2072.641
VDDC	124	–826.1055	1741.918	826.1055	1741.918
VDDC	125	–501.4755	1729.606	501.4755	1729.606
VDDC	133	–332.0775	1621.264	332.0775	1621.264
VDDC	141	1227.3885	1523.803	–1227.3885	1523.803
VDDC	201	1444.7205	517.135	–1444.7205	517.135
VDDC	202	1194.3945	502.897	–1194.3945	502.897
VDDC	211	–210.0195	304.6	210.0195	304.6
VDDC	215	187.4025	293.314	–187.4025	293.314
VDDC	246	1430.3925	–289.103	–1430.3925	–289.103
VDDC	293	1515.9465	–1174.442	–1515.9465	–1174.442
VDDC	322	1612.9125	–1658.012	–1612.9125	–1658.012
VDDC	327	145.7775	–1816.043	–145.7775	–1816.043
VDDC	331	–238.1445	–1873.355	238.1445	–1873.355
VDDC_MEM	18	–1180.7145	3276.517	1180.7145	3276.517
VDDC_PHY	150	1610.8245	1326.694	–1610.8245	1326.694

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
VDDC_PHY	151	2022.7275	1294.231	–2022.7275	1294.231
VDDC_PHY	210	432.5265	318.271	–432.5265	318.271
VDDC_PHY	212	1195.1595	302.395	–1195.1595	302.395
VDDC_PHY	213	750.9195	301.216	–750.9195	301.216
VDDC_PHY	218	1523.5065	231.277	–1523.5065	231.277
VDDC_PHY	255	2260.4265	–401.018	–2260.4265	–401.018
VDDC_PHY	258	1525.0275	–465.539	–1525.0275	–465.539
VDDC_PHY	262	2259.6165	–601.016	–2259.6165	–601.016
VDDC_PHY	265	1316.4255	–649.859	–1316.4255	–649.859
VDDC_PHY	300	1317.7395	–1282.658	–1317.7395	–1282.658
VDDC_PHY	304	–704.5875	–1353.767	704.5875	–1353.767
VDDC_PHY	317	1326.0375	–1584.518	–1326.0375	–1584.518
VDDC_PHY	321	297.8595	–1651.856	–297.8595	–1651.856
VDDC_PHY	325	2005.9605	–1721.453	–2005.9605	–1721.453
VDDC_SUBCORE	5	–902.9475	3474.373	902.9475	3474.373
VDDC_SUBCORE	21	472.0725	3255.835	–472.0725	3255.835
VDDC_SUBCORE	40	706.9365	3057.898	–706.9365	3057.898
VDDC_SUBCORE	74	1402.9965	2684.884	–1402.9965	2684.884
VDDC_SUBCORE	92	313.4925	2288.677	–313.4925	2288.677
VDDC_SUBCORE	112	–59.5125	1953.508	59.5125	1953.508
VDDC_SUBCORE	113	–1289.5335	1940.872	1289.5335	1940.872
VDDC_SUBCORE	114	–877.2075	1936.552	877.2075	1936.552
VDDC_SUBCORE	135	1623.4065	1582.717	–1623.4065	1582.717
VDDC_SUBCORE	143	–103.5225	1502.455	103.5225	1502.455
VDDC_SUBCORE	198	960.7005	578.227	–960.7005	578.227
VDDC_SUBCORE	199	–127.7415	576.841	127.7415	576.841
VDDIO	90	1236.9825	2375.887	–1236.9825	2375.887
VDDIO	111	1244.0385	1954.624	–1244.0385	1954.624
VDDIO	174	1316.2095	959.107	–1316.2095	959.107
VDDIO	220	2242.7595	194.035	–2242.7595	194.035
VDDIO	228	2069.0415	63.76	–2069.0415	63.76
VDDIO	234	2260.3995	–6.296	–2260.3995	–6.296
VDDIO_RF	52	–714.3255	2917.912	714.3255	2917.912
VDDIO_RF	67	146.3445	2724.07	–146.3445	2724.07
VDDIO_RF	75	–59.1615	2613.514	59.1615	2613.514
VDDIO_RF	273	1848.8385	–762.872	–1848.8385	–762.872

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
VDDIO_RF	292	1716.7275	–1159.457	–1716.7275	–1159.457
VDDIO_RF	309	1599.8985	–1457.708	–1599.8985	–1457.708
VDDIO_SD	10	1095.2325	3399.79	–1095.2325	3399.79
VOUT_3P3	108	–2183.562	1955.3215	2183.562	1955.3215
VOUT_BTLDO2P5	94	–2183.562	2238.1645	2183.562	2238.1645
VOUT_CLDO	76	–2183.562	2521.0075	2183.562	2521.0075
VOUT_CLDO	87	–2324.9835	2379.586	2324.9835	2379.586
VOUT_CLDO	88	–2042.1405	2379.586	2042.1405	2379.586
VOUT_CLDO	95	–1900.719	2238.1645	1900.719	2238.1645
VOUT_CLDO_SENSE	77	–1900.719	2521.0075	1900.719	2521.0075
VOUT_HLDO	61	–1617.876	2803.8505	1617.876	2803.8505
VOUT_LNLDO	96	–1617.876	2238.1645	1617.876	2238.1645
VOUT_MEMLPLDO	122	–1476.4545	1813.9	1476.4545	1813.9
VOUT_PA3P3	138	–2324.9835	1531.057	2324.9835	1531.057
VOUT_PA3P3	147	–2183.562	1389.6355	2183.562	1389.6355
VOUT_PA3P3	153	–2324.9835	1248.214	2324.9835	1248.214
VOUT_PA3P3	154	–2042.1405	1248.214	2042.1405	1248.214
VOUT_PA3P3	165	–2183.562	1106.7925	2183.562	1106.7925
VOUT_PA3P3	173	–2042.1405	965.371	2042.1405	965.371
VOUT_PA3P3_SENSE	172	–2324.9835	965.371	2324.9835	965.371
VSSC	12	–1617.876	3369.5365	1617.876	3369.5365
VSSC	27	814.0815	3227.386	–814.0815	3227.386
VSSC	36	77.3955	3089.974	–77.3955	3089.974
VSSC	44	–1325.7585	3002.125	1325.7585	3002.125
VSSC	51	–190.7595	2944.084	190.7595	2944.084
VSSC	54	1450.9665	2883.415	–1450.9665	2883.415
VSSC	58	–540.5175	2814.538	540.5175	2814.538
VSSC	63	–1248.2595	2746.156	1248.2595	2746.156
VSSC	64	–931.0725	2740.693	931.0725	2740.693
VSSC	65	–236.6415	2732.764	236.6415	2732.764
VSSC	66	1601.2125	2731.234	–1601.2125	2731.234
VSSC	81	–1244.6235	2459.227	1244.6235	2459.227
VSSC	82	–931.0725	2457.4	931.0725	2457.4
VSSC	84	–547.1775	2422.228	547.1775	2422.228
VSSC	85	–147.1815	2422.228	147.1815	2422.228
VSSC	89	–1759.2975	2379.586	1759.2975	2379.586

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
VSSC	97	–347.1795	2222.221	347.1795	2222.221
VSSC	98	–144.0675	2136.145	144.0675	2136.145
VSSC	101	1401.5385	2087.374	–1401.5385	2087.374
VSSC	104	–549.5175	2057.926	549.5175	2057.926
VSSC	105	352.8225	2022.223	–352.8225	2022.223
VSSC	106	652.8195	2022.223	–652.8195	2022.223
VSSC	107	1052.8155	2022.223	–1052.8155	2022.223
VSSC	110	–1617.876	1955.3215	1617.876	1955.3215
VSSC	119	852.8175	1822.225	–852.8175	1822.225
VSSC	130	252.8145	1622.227	–252.8145	1622.227
VSSC	131	652.8195	1622.227	–652.8195	1622.227
VSSC	132	1052.8155	1622.227	–1052.8155	1622.227
VSSC	136	–721.5615	1568.605	721.5615	1568.605
VSSC	137	–1008.9315	1539.877	1008.9315	1539.877
VSSC	142	–526.1625	1521.814	526.1625	1521.814
VSSC	145	452.8215	1422.22	–452.8215	1422.22
VSSC	152	–624.9645	1275.367	624.9645	1275.367
VSSC	156	–147.1815	1222.222	147.1815	1222.222
VSSC	157	252.8145	1222.222	–252.8145	1222.222
VSSC	158	652.8195	1222.222	–652.8195	1222.222
VSSC	159	1052.8155	1222.222	–1052.8155	1222.222
VSSC	161	–1359.4185	1205.275	1359.4185	1205.275
VSSC	168	52.8165	1022.224	–52.8165	1022.224
VSSC	169	852.8175	1022.224	–852.8175	1022.224
VSSC	176	–594.6975	927.337	594.6975	927.337
VSSC	178	–1347.0525	879.511	1347.0525	879.511
VSSC	179	–1584.3195	871.042	1584.3195	871.042
VSSC	182	–147.1815	822.226	147.1815	822.226
VSSC	183	252.8145	822.226	–252.8145	822.226
VSSC	184	652.8195	822.226	–652.8195	822.226
VSSC	185	1052.8155	822.226	–1052.8155	822.226
VSSC	189	1445.9265	718.717	–1445.9265	718.717
VSSC	194	–567.9315	624.361	567.9315	624.361
VSSC	195	–2168.8155	623.857	2168.8155	623.857
VSSC	196	452.8215	622.228	–452.8215	622.228
VSSC	200	–848.7585	539.032	848.7585	539.032

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
VSSC	214	–416.7045	297.931	416.7045	297.931
VSSC	219	952.8165	222.223	–952.8165	222.223
VSSC	227	1725.0705	86.305	–1725.0705	86.305
VSSC	229	–147.1815	22.225	147.1815	22.225
VSSC	230	252.8145	22.225	–252.8145	22.225
VSSC	231	652.8195	22.225	–652.8195	22.225
VSSC	232	1052.8155	22.225	–1052.8155	22.225
VSSC	237	1430.9865	–88.052	–1430.9865	–88.052
VSSC	240	452.8215	–177.773	–452.8215	–177.773
VSSC	242	–2103.8535	–202.928	2103.8535	–202.928
VSSC	243	2166.6915	–206.033	–2166.6915	–206.033
VSSC	244	–2307.6405	–208.157	2307.6405	–208.157
VSSC	245	–147.1815	–277.772	147.1815	–277.772
VSSC	247	–1284.5655	–320.306	1284.5655	–320.306
VSSC	249	–1547.1855	–377.78	1547.1855	–377.78
VSSC	250	252.8145	–377.78	–252.8145	–377.78
VSSC	251	652.8195	–377.78	–652.8195	–377.78
VSSC	252	1052.8155	–377.78	–1052.8155	–377.78
VSSC	254	1869.3945	–397.013	–1869.3945	–397.013
VSSC	257	–2105.0955	–422.852	2105.0955	–422.852
VSSC	259	–1940.4855	–541.679	1940.4855	–541.679
VSSC	260	852.8175	–577.778	–852.8175	–577.778
VSSC	261	–836.6625	–587.948	836.6625	–587.948
VSSC	264	104.8725	–618.683	–104.8725	–618.683
VSSC	267	–147.1815	–677.777	147.1815	–677.777
VSSC	272	1608.2505	–757.58	–1608.2505	–757.58
VSSC	274	252.8145	–777.776	–252.8145	–777.776
VSSC	275	652.8195	–777.776	–652.8195	–777.776
VSSC	276	1052.8155	–777.776	–1052.8155	–777.776
VSSC	279	–526.5945	–818.699	526.5945	–818.699
VSSC	280	1737.2025	–946.94	–1737.2025	–946.94
VSSC	282	452.8215	–977.774	–452.8215	–977.774
VSSC	284	–956.0385	–1035.194	956.0385	–1035.194
VSSC	288	–656.1135	–1105.583	656.1135	–1105.583
VSSC	294	–1239.1785	–1177.772	1239.1785	–1177.772
VSSC	295	–147.1815	–1177.772	147.1815	–1177.772

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
VSSC	296	252.8145	–1177.772	–252.8145	–1177.772
VSSC	297	652.8195	–1177.772	–652.8195	–1177.772
VSSC	298	1052.8155	–1177.772	–1052.8155	–1177.772
VSSC	305	–504.3915	–1371.704	504.3915	–1371.704
VSSC	306	852.8175	–1377.779	–852.8175	–1377.779
VSSC	307	1789.2315	–1388.264	–1789.2315	–1388.264
VSSC	308	650.4255	–1448.348	–650.4255	–1448.348
VSSC	310	–1244.9115	–1468.796	1244.9115	–1468.796
VSSC	314	1014.1065	–1535.504	–1014.1065	–1535.504
VSSC	315	–1045.0755	–1458.194	1045.0755	–1458.194
VSSC	316	–155.2635	–1566.122	155.2635	–1566.122
VSSC	318	–409.3875	–1587.434	409.3875	–1587.434
VSSC	320	–695.5425	–1635.269	695.5425	–1635.269
VSSC	329	1493.8965	–1857.677	–1493.8965	–1857.677
WCC_VDDIO	148	–1617.876	1389.6355	1617.876	1389.6355
WL_REG_ON	129	–1617.876	1672.4785	1617.876	1672.4785
WPT_1P8	166	–1900.719	1106.7925	1900.719	1106.7925
WPT_3P3	99	–2324.9835	2096.743	2324.9835	2096.743
WRF_AFE_GND_CORE0	346	–1664.5005	–2373.5705	1664.5005	–2373.5705
WRF_AFE_GND_CORE1	347	1664.5005	–2373.5705	–1664.5005	–2373.5705
WRF_AFE_GND_core0	396	–1277.3295	–2630.6105	1277.3295	–2630.6105
WRF_AFE_GND_core1	397	1277.33	–2630.61	–1277.3295	–2630.6105
WRF_AFE_VDD1P35_CORE0	375	–791.217	–3192.0755	791.217	–3192.0755
WRF_AFE_VDD1P35_CORE1	376	791.217	–3192.0755	–791.217	–3192.0755
WRF_EXT_TSSIA_CORE0	336	–1664.5005	–2173.5725	1664.5005	–2173.5725
WRF_EXT_TSSIA_CORE1	337	1664.5005	–2173.5725	–1664.5005	–2173.5725
WRF_GENERAL2_GND_CORE0	359	–1592.847	–2787.26	1592.847	–2787.26
WRF_GENERAL2_GND_CORE1	359	1592.847	–2787.26	–1592.847	–2787.26
WRF_GENERAL_GND_CORE0	348	–973.53	–2558.5565	973.53	–2558.5565
WRF_GENERAL_GND_CORE1	349	973.53	–2558.5565	–973.53	–2558.5565
WRF_GPAIO_OUT_CORE0	350	–1664.514	–2585.381	1664.514	–2585.381
WRF_GPAIO_OUT_CORE1	351	1664.514	–2585.381	–1664.514	–2585.381
WRF_PAOUT_2G_CORE0	354	–2255.4855	–2710.7285	2255.4855	–2710.7285
WRF_PAOUT_2G_CORE1	355	2255.4855	–2710.7285	–2255.4855	–2710.7285
WRF_PAOUT_5G_CORE0	394	–1729.4715	–3614.351	1729.4715	–3614.351
WRF_PAOUT_5G_CORE1	395	1729.4715	–3614.351	–1729.4715	–3614.351

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
WRF_PA_GND3P3_CORE0	362	–1905.1515	–2930.171	1905.1515	–2930.171
WRF_PA_GND3P3_CORE0	368	–1726.011	–3112.493	1726.011	–3112.493
WRF_PA_GND3P3_CORE0	370	–1951.7715	–3125.9165	1951.7715	–3125.9165
WRF_PA_GND3P3_CORE0	373	–1507.2705	–3168.824	1507.2705	–3168.824
WRF_PA_GND3P3_CORE1	363	1905.1515	–2930.171	–1905.1515	–2930.171
WRF_PA_GND3P3_CORE1	369	1726.011	–3112.493	–1726.011	–3112.493
WRF_PA_GND3P3_CORE1	371	1951.7715	–3125.9165	–1951.7715	–3125.9165
WRF_PA_GND3P3_CORE1	374	1507.2705	–3168.824	–1507.2705	–3168.824
WRF_PA_VDD3P3_CORE0	377	–2330.0145	–3196.301	2330.0145	–3196.301
WRF_PA_VDD3P3_CORE0	382	–2287.404	–3391.763	2287.404	–3391.763
WRF_PA_VDD3P3_CORE0	384	–1988.37	–3407.1665	1988.37	–3407.1665
WRF_PA_VDD3P3_CORE0	392	–2265.4125	–3591.761	2265.4125	–3591.761
WRF_PA_VDD3P3_CORE1	378	2330.0145	–3196.301	–2330.0145	–3196.301
WRF_PA_VDD3P3_CORE1	383	2287.404	–3391.763	–2287.404	–3391.763
WRF_PA_VDD3P3_CORE1	385	1988.37	–3407.1665	–1988.37	–3407.1665
WRF_PA_VDD3P3_CORE1	393	2265.4125	–3591.761	–2265.4125	–3591.761
WRF_PMU_VDD1P35_CORE0	365	–621.1395	–3297.425	621.1395	–3297.425
WRF_PMU_VDD1P35_CORE0	380	–653.472	–3497.423	653.472	–3497.423
WRF_PMU_VDD1P35_CORE1	366	621.1395	–3297.425	–621.1395	–3297.425
WRF_PMU_VDD1P35_CORE1	381	653.472	–3497.423	–653.472	–3497.423
WRF_RFIN_2G_CORE0	340	–2179.584	–2202.6515	2179.584	–2202.6515
WRF_RFIN_2G_CORE1	341	2179.584	–2202.6515	–2179.584	–2202.6515
WRF_RFIN_5G_CORE0	388	–1336.0365	–3462.0845	1336.0365	–3462.0845
WRF_RFIN_5G_CORE1	389	1336.0365	–3462.0845	–1336.0365	–3462.0845
WRF_RX2G_GND_CORE0	342	–1871.0415	–2310.1475	1871.0415	–2310.1475
WRF_RX2G_GND_CORE1	343	1871.0415	–2310.1475	–1871.0415	–2310.1475
WRF_RX5G_GND_CORE0	386	–941.4675	–3455.411	941.4675	–3455.411
WRF_RX5G_GND_CORE1	387	941.4675	–3455.411	–941.4675	–3455.411
WRF_SYNTH_GND_CORE0	344	–117.909	–2332.3685	117.909	–2332.3685
WRF_SYNTH_GND_CORE0	352	–593.442	–2656.238	593.442	–2656.238
WRF_SYNTH_GND_CORE1	345	117.909	–2332.3685	–117.909	–2332.3685
WRF_SYNTH_GND_CORE1	353	593.442	–2656.238	–593.442	–2656.238
WRF_SYNTH_VDD1P2_CORE0	360	–682.668	–2897.429	682.668	–2897.429
WRF_SYNTH_VDD1P2_CORE1	361	682.668	–2897.429	–682.668	–2897.429
WRF_SYNTH_VDD3P3_CORE0	338	–256.2705	–2183.5445	256.2705	–2183.5445
WRF_SYNTH_VDD3P3_CORE1	339	256.2705	–2183.5445	–256.2705	–2183.5445

Table 20: WLCSP Coordinates Listed by Name (Cont.)

Net Name	Bump Number	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Bottom View (Bumps Facing Up) Package Center (0,0)	
		Bump X	Bump Y	Bump X	Bump Y
WRF_TIA_GND_CORE0	334	–1394.2575	–2166.1205	1394.2575	–2166.1205
WRF_TIA_GND_CORE1	335	1394.2575	–2166.1205	–1394.2575	–2166.1205
WRF_TXMIX_VDD_CORE0	356	–1910.1375	–2730.1685	1910.1375	–2730.1685
WRF_TXMIX_VDD_CORE1	357	1910.1375	–2730.1685	–1910.1375	–2730.1685
WRF_VCO_GND_CORE0	332	–615.0735	–2128.406	615.0735	–2128.406
WRF_VCO_GND_CORE1	333	615.0735	–2128.406	–615.0735	–2128.406
WRF_XTAL_GND1P2_CORE0	372	–230.6025	–3157.277	230.6025	–3157.277
WRF_XTAL_VDD1P2_CORE0	379	0	–3268.031	0	–3268.031
WRF_XTAL_VDD1P35_CORE0	364	–30.6045	–2995.052	30.6045	–2995.052
WRF_XTAL_VDD1P35_CORE1	367	169.3935	–3108.3395	–169.3935	–3108.3395
WRF_XTAL_XON_CORE0	390	–61.704	–3483.752	61.704	–3483.752
WRF_XTAL_XOP_CORE0	391	–261.702	–3495.6455	261.702	–3495.6455

Signal Descriptions

The signal name, type, and description of each pin in the BCM4359 is listed in Table 21 and Table 22. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 21: BCM4359 WLCSP Signal Descriptions

Bump	Signal Name	Type	Description
WLAN and Bluetooth Receive RF Signal Interface			
340	WRF_RFIN_2G_CORE0	I	2.4 GHz Bluetooth and WLAN CORE0 receiver shared input.
341	WRF_RFIN_2G_CORE1	I	2.4 GHz Bluetooth and WLAN CORE1 receiver shared input.
388	WRF_RFIN_5G_CORE0	I	5 GHz WLAN CORE0 receiver input.
389	WRF_RFIN_5G_CORE1	I	5 GHz WLAN CORE1 receiver input.
354	WRF_PAOUT_2G_CORE0	O	2.4 GHz WLAN CORE0 PA output.
355	WRF_PAOUT_2G_CORE1	O	2.4 GHz WLAN CORE1 PA output.
394	WRF_PAOUT_5G_CORE0	O	5 GHz WLAN CORE0 PA output.
395	WRF_PAOUT_5G_CORE1	O	5 GHz WLAN CORE1 PA output.
336	WRF_EXT_TSSIA_CORE0	I	5 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
337	WRF_EXT_TSSIA_CORE1	I	5 GHz TSSI CORE1 input from an optional external power amplifier/power detector.
350	WRF_GPAIO_OUT_CORE0	I	GPIO or 2.4 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
351	WRF_GPAIO_OUT_CORE1	I	GPIO or 2.4 GHz TSSI CORE1 input from an optional external power amplifier/power detector.

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
RF Switch Control Lines			
13	RF_SW_CTRL_0	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
9	RF_SW_CTRL_1	O	
17	RF_SW_CTRL_2	O	
32	RF_SW_CTRL_3	O	
46	RF_SW_CTRL_4	O	
30	RF_SW_CTRL_5	O	
28	RF_SW_CTRL_6	O	
45	RF_SW_CTRL_7	O	
35	RF_SW_CTRL_8	O	
19	RF_SW_CTRL_9	O	
328	RF_SW_CTRL_10	O	
319	RF_SW_CTRL_11	O	
302	RF_SW_CTRL_12	O	
312	RF_SW_CTRL_13	O	
290	RF_SW_CTRL_14	O	
281	RF_SW_CTRL_15	O	
271	RF_SW_CTRL_16	O	
278	RF_SW_CTRL_17	O	
299	RF_SW_CTRL_18	O	
286	RF_SW_CTRL_19	O	
WLAN PCI Express Interface			
80	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
93	PCIE_PERST_L	I (PU)	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1.
23	PCIE_RDN0	I	Receiver differential pair (×1 lane).
43	PCIE_RDP0	I	
14	PCIE_REFCLKN	I	PCIE Differential Clock inputs (negative and positive). 100 MHz differential.
22	PCIE_REFCLKP	I	
15	PCIE_TDN0	O	Transmitter differential pair (×1 lane).
34	PCIE_TDP0	O	
86	PCI_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
55	PCIE_TESTP	–	PCIe test pins.
62	PCIE_TESTN	–	
WLAN SDIO Bus Interface These signals can support alternate functionality depending on package and host interface mode. See Table 26: "GPIO Alternative Signal Functions," on page 121.			
20	SDIO_CLK	I	SDIO clock input.
39	SDIO_CMD	I/O	SDIO command line.
31	SDIO_DATA_0	I/O	SDIO data line 0.
16	SDIO_DATA_1	I/O	SDIO data line 1.
29	SDIO_DATA_2	I/O	SDIO data line 2.
8	SDIO_DATA_3	I/O	SDIO data line 3.
WLAN GPIO Interface The GPIO signals can be multiplexed via software and the JTAG_SEL pin to support other functions. See Table 24: "GPIO Strap Pins," on page 119 and Table 26: "GPIO Alternative Signal Functions," on page 121 for additional details.			
134	GPIO_0	I/O	Programmable GPIO pins.
170	GPIO_1	I/O	
186	GPIO_2	I/O	
217	GPIO_3	I/O	
238	GPIO_4	I/O	
118	GPIO_5	I/O	
117	GPIO_6	I/O	
204	GPIO_7	I/O	
193	GPIO_8	I/O	
181	GPIO_9	I/O	
167	GPIO_10	I/O	
164	GPIO_11	I/O	
175	GPIO_12	I/O	
144	GPIO_13	I/O	
116	GPIO_14	I/O	
123	GPIO_15	I/O	
115	GPIO_16	I/O	
102	GPIO_17	I/O	
91	GPIO_18	I/O	
79	GPIO_19	I/O	

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
JTAG Interface			
70	JTAG_SEL	I/O	JTAG select: pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground. ***Note:*** See Table 26: "GPIO Alternative Signal Functions," on page 121 for the JTAG signal pins.
Clocks			
390	WRF_XTAL_XON_CORE0	O	XTAL oscillator output.
391	WRF_XTAL_XOP_CORE0	I	XTAL oscillator input.
277	LPO_IN	I	External sleep clock input (32.768 kHz).
233	CLK_REQ	I/O	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.
Bluetooth Transceiver			
326	BT_RF	O	Bluetooth PA output
Bluetooth PCM			
190	BT_PCM_CLK	I/O	PCM clock; can be master (output) or slave (input).
192	BT_PCM_IN	I	PCM data input.
203	BT_PCM_OUT	O	PCM data output.
191	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input).
Bluetooth USB Interface			
162	BT_USB_DN	I/O	USB (Host) data negative. Negative terminal of the USB transceiver.
171	BT_USB_DP	I/O	USB (Host) data positive. Positive terminal of the USB transceiver.
Bluetooth UART			
208	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
224	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
235	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
225	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
Bluetooth I^2S			
222	BT_I2S_CLK	I/O	I^2S clock, can be master (output) or slave (input).
223	BT_I2S_DI	I/O	I^2S data input.
226	BT_I2S_DO	I/O	I^2S data output.
216	BT_I2S_WS	I/O	I^2S WS; can be master (output) or slave (input).
Bluetooth GPIOs			
239	BT_GPIO_2	I/O	Bluetooth general-purpose I/O.
256	BT_GPIO_3	I/O	Bluetooth general-purpose I/O.
291	BT_GPIO_4	I/O	Bluetooth general-purpose I/O.
263	BT_GPIO_5	I/O	Bluetooth general-purpose I/O.
283	BT_AGPIO	I/O	Bluetooth test pin.
Bluetooth SLIMbus			
209	BT_SLIMBUS_CK	I/O	Bluetooth SLIMbus clock.
205	BT_SLIMBUS_DT	I/O	Bluetooth SLIMbus data.
Miscellaneous			
129	WL_REG_ON	I	Used by PMU to power up or power down the internal BCM4359 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
140	BT_REG_ON	I	Used by PMU to power up or power down the internal BCM4359 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
253	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE.
241	BT_HOST_WAKE	I/O	Bluetooth HOST_WAKE.
248	BT_TM1	I/O	Bluetooth test mode pin.
Integrated Voltage Regulators			
24, 48, 49, 50	SR_VDDBAT5V	I	Power VBAT.
11, 25, 26, 37, 38	SR_VLX	O	CBUCK switching regulator output. Refer to Table 43 on page 155 for details of the inductor and capacitor required on this output.
59, 60, 71, 72, 73	LDO_VDD1P5	I	LNLDO input.
100, 109, 120, 121, 127, 128, 139	LDO_VDDBAT5V	I	LDO VBAT.

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
367	WRF_XTAL_VDD1P35_CORE1	I	XTAL LDO input CORE1 (1.35V).
364	WRF_XTAL_VDD1P35_CORE0	I	XTAL LDO input CORE0 (1.35V).
379	WRF_XTAL_VDD1P2_CORE0	O	XTAL LDO output CORE0 (1.2V).
96	VOUT_LNLDO	O	Output of low-noise LDO.
76, 87, 88, 95	VOUT_CLDO	O	Output of core LDO.
77	VOUT_CLDO_SENSE	I	Voltage sense pin for VOUT_CLDO 1.2V output.
94	VOUT_BTLDO2P5	O	Output of BT LDO.
61	VOUT_HLDO	O	Output of host system interface core LDO 1.2V supply.
108	VOUT_3P3	O	LDO 3.3V output.
122	VOUT_MEMLPLDO	O	Output of 1.2V LDO for low power memory.
138, 147, 153, 154, 165, 173	VOUT_PA3P3	O	Output of 3.3V LDO for PA.
172	VOUT_PA3P3_SENSE	I	Voltage sense pin for VOUT_PA3P3 output.
Bluetooth Supplies			
303	BT_PAVDD2P5	PWR	Bluetooth PA power supply.
324	BT_LNAVDD1P2	PWR	Bluetooth LNA power supply.
287	BT_IFVDD1P2	PWR	Bluetooth IF block power supply.
301	BT_PLLVDD1P2	PWR	Bluetooth RF PLL power supply.
266	BT_VDDC_ISO1	PWR	1.8V VIO supply for power-on/off island.
330	BT_VCOVDD1P2	PWR	Bluetooth RF power supply.
236	BT_VDDC_ISO2	PWR	1.8V VIO supply for power-on/off island.
207, 221	BT_VDDO	PWR	1.8V or 3.3V VIO supply.
WLAN Supplies			
338	WRF_SYNTH_VDD3P3_CORE0	PWR	SYNTH CORE0 VDD 3.3V supply.
339	WRF_SYNTH_VDD3P3_CORE1	PWR	SYNTH CORE1 VDD 3.3V supply.
360	WRF_SYNTH_VDD1P2_CORE0	PWR	SYNTH CORE0 VDD 1.2V supply.
361	WRF_SYNTH_VDD1P2_CORE1	PWR	SYNTH CORE1 VDD 1.2V supply.
138, 147, 153, 154	VOUT_PA3P3	PWR	PA 3.3V supply.
377, 382, 384, 392	WRF_PA_VDD3P3_CORE0	PWR	PA CORE0 3.3V VBAT supply.
378, 383, 385, 393	WRF_PA_VDD3P3_CORE1	PWR	PA CORE1 3.3V VBAT supply.
365, 380	WRF_PMU_VDD1P35_CORE0	PWR	PMU CORE0 1.35V supply.
366, 381	WRF_PMU_VDD1P35_CORE1	PWR	PMU CORE1 1.35V supply.
356	WRF_TXMIX_VDD_CORE0	PWR	TX mixer CORE0 supply.
357	WRF_TXMIX_VDD_CORE1	PWR	TX mixer CORE1 supply.

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
Miscellaneous Supplies			
41	OTP_VDD33	PWR	OTP 3.3V supply
4, 47, 53, 57, 68, 69, 83, 103, 124, 125, 133, 141, 201, 202, 211, 215, 246, 293, 322, 327, 331	VDDC	PWR	1.2V core supply for WLAN.
90, 111, 174, 220, 228, 234	VDDIO	PWR	1.8V or 3.3V supply for WLAN. Must be directly connected to PMU_VDDIO and BT_VDDO on the PCB.
5, 21, 40, 74, 92, 112, 113, 114, 135, 143, 198, 199	VDDC_SUBCORE	PWR	1.2V supply for subcore.
210. 212, 213, 218, 255, 258, 262, 265, 300, 304, 317, 321, 325	VDDC_PHY	PWR	PHY core supply.
126, 187, 188, 268, 269, 270	BT_VDDC	PWR	1.2V core supply for BT.
155	SYS_VDDIO	PWR	1.8V or 3.3V supply for system I/O.
148	WCC_VDDIO	PWR	1.8V or 3.3V supply for WCC I/O.
177	BT_USB_VDDO	PWR	Bluetooth USB supply.
18	VDDC_MEM	PWR	Memory core supply.
10	VDDIO_SD	PWR	1.8V–3.3V supply for SDIO pads.
166	WPT_1P8	PWR	Wireless charging 1.8V supply with internal switches.
99	WPT_3P3	PWR	Wireless charging 3.3V supply for BTLDO2P5 and VBAT_SEL with internal switches.
52, 67, 75, 273, 292, 309	VDDIO_RF	PWR	IO supply for RF switch control pads (3.3V).
163	AVDD_BBPLL	PWR	Baseband PLL supply.
33	PLL_AVDD1P2	PWR	1.2V supply for PCIe PLL.
56	PCIE_RXTX_AVDD1P2	PWR	1.2V supply for PCIE TX and RX.
Ground			
332	WRF_VCO_GND_CORE0	GND	VCO CORE0 ground.
333	WRF_VCO_GND_CORE1	GND	VCO CORE1 ground.
346	WRF_AFE_GND_CORE0	GND	CORE0 AFE ground.

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
347, 397	WRF_AFE_GND_CORE1	GND	CORE1 AFE ground.
334	WRF_TIA_GND_CORE0	GND	TX CORE0 ground.
335	WRF_TIA_GND_CORE1	GND	TX CORE1 ground.
344, 352	WRF_SYNTH_GND_CORE0	GND	SYNTH CORE0 ground.
345, 353	WRF_SYNTH_GND_CORE1	GND	SYNTH CORE1 ground.
373	WRF_XTAL_GND1P2_CORE0	GND	XTAL CORE0 ground.
342	WRF_RX2G_GND_CORE0	GND	RX 2 GHz CORE0 ground.
343	WRF_RX2G_GND_CORE1	GND	RX 2 GHz CORE1 ground.
386	WRF_RX5G_GND_CORE0	GND	RX 5 GHz CORE0 ground.
387	WRF_RX5G_GND_CORE1	GND	RX 5 GHz CORE1 ground.
348	WRF_GENERAL_GND_CORE0	GND	General CORE0 ground.
349	WRF_GENERAL_GND_CORE1	GND	General CORE1 ground.
358	WRF_GENERAL2_GND_CORE0	GND	General 2 CORE0 ground.
359	WRF_GENERAL2_GND_CORE1	GND	General 2 CORE1 ground.
362, 368, 370, 373	WRF_PA_GND3P3_CORE0	GND	PA CORE0 ground.
363, 369, 371, 374	WRF_PA_GND3P3_CORE1	GND	PA CORE1 ground.
396	WRF_AFE_GND_CORE0	GND	AFE CORE0 Ground.
397	WRF_AFE_GND_CORE1	GND	AFE CORE1 Ground.

Table 21: BCM4359 WLCSP Signal Descriptions (Cont.)

Bump	Signal Name	Type	Description
12, 27, 36, 44, 51, 54, 58, 63–66, 81, 82, 84, 85, 89, 97, 98, 101, 104–107, 110, 119, 130–132, 136, 137, 142, 145, 146, 152, 156–159, 160, 161, 168, 169, 176, 178, 179, 182–185, 189, 194–197, 200, 206 214, 219, 227, 229–232, 237, 240, 242–245, 247, 249–252, 254, 257, 259–261, 264, 267, 272, 274–276, 279, 280, 282, 284, 288, 294–298, 305–308, 310, 314–316, 318, 320	VSSC	GND	Core ground for WLAN and BT.
1–3	SR_PVSS	GND	Power ground.
78	PMU_AVSS	GND	Quiet ground.
313	BT_PAVSS	GND	Bluetooth PA ground.
285	BT_DVSS	GND	Bluetooth digital ground.
289	BT_PLLVSS	GND	Bluetooth PLL ground.
323	BT_VCOVSS	GND	Bluetooth VCO ground.
180	AVSS_BBPLL	GND	Baseband PLL ground.
311	BT_LNAVSS	GND	BT LNA ground.
7	PCIE_RXTX_AVSS	GND	PCIe RX/TX ground.
6, 42	PCIE_PLL_AVSS	GND	PCIe PLL ground.
311	BT_LNAVSS	GND	Bluetooth LNA ground.
149	BT_USB_VSSO	GND	Bluetooth USB ground.

Table 22: BCM4359 WLBGA Signal Descriptions

Ball	Signal Name	Type	Description
WLAN and Bluetooth Receive RF Signal Interface			
R1	WRF_RFIN_2G_CORE0	I	2.4 GHz Bluetooth and WLAN CORE0 receiver shared input.
R12	WRF_RFIN_2G_CORE1	I	2.4 GHz Bluetooth and WLAN CORE1 receiver shared input.
V3	WRF_RFIN_5G_CORE0	I	5 GHz WLAN CORE0 receiver input.
V10	WRF_RFIN_5G_CORE1	I	5 GHz WLAN CORE1 receiver input.
T1	WRF_PAOUT_2G_CORE0	O	2.4 GHz WLAN CORE0 PA output.
T12	WRF_PAOUT_2G_CORE1	O	2.4 GHz WLAN CORE1 PA output.
V2	WRF_PAOUT_5G_CORE0	O	5 GHz WLAN CORE0 PA output.
V11	WRF_PAOUT_5G_CORE1	O	5 GHz WLAN CORE1 PA output.
R4	WRF_EXT_TSSIA_CORE0	I	5 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
R9	WRF_EXT_TSSIA_CORE1	I	5 GHz TSSI CORE1 input from an optional external power amplifier/power detector.
R3	WRF_GPAIO_OUT_CORE0	I	GPIO or 2.4 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
R10	WRF_GPAIO_OUT_CORE1	I	GPIO or 2.4 GHz TSSI CORE1 input from an optional external power amplifier/power detector.
RF Switch Control Lines			
E6	RF_SW_CTRL_0	I/O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
F6	RF_SW_CTRL_1	I/O	
F5	RF_SW_CTRL_2	I/O	
G5	RF_SW_CTRL_3	I/O	
H5	RF_SW_CTRL_4	I/O	
F4	RF_SW_CTRL_5	I/O	
G4	RF_SW_CTRL_6	I/O	
H4	RF_SW_CTRL_7	I/O	
H3	RF_SW_CTRL_8	I/O	
H2	RF_SW_CTRL_9	I/O	
N10	RF_SW_CTRL_10	I/O	
N11	RF_SW_CTRL_11	I/O	
P12	RF_SW_CTRL_12	I/O	
M10	RF_SW_CTRL_13	I/O	
M11	RF_SW_CTRL_14	I/O	
N12	RF_SW_CTRL_15	I/O	
K9	RF_SW_CTRL_16	I/O	
L9	RF_SW_CTRL_17	I/O	
L11	RF_SW_CTRL_18	I/O	
L12	RF_SW_CTRL_19	I/O	

Table 22: BCM4359 WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
WLAN PCI Express Interface			
E12	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
E11	PCIE_PERST_L	I (PU)	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1.
C12	PCIE_RDN0	I	Receiver differential pair (×1 lane).
D12	PCIE_RDP0	I	
A12	PCIE_REFCLKN	I	PCIE Differential Clock inputs (negative and positive). 100 MHz differential.
B12	PCIE_REFCLKP	I	
A11	PCIE_TDN0	O	Transmitter differential pair (×1 lane).
A10	PCIE_TDP0	O	
E10	PCI_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.
B11	PCIE_TESTP	–	PCIe test pins.
C11	PCIE_TESTN	–	
WLAN SDIO Bus Interface ***Note:*** These signals can support alternate functionality depending on package and host interface mode. See Table 26: “GPIO Alternative Signal Functions,” on page 121 for additional details.			
A8	SDIO_CLK	I	SDIO clock input.
B8	SDIO_CMD	I/O	SDIO command line.
B6	SDIO_DATA_0	I/O	SDIO data line 0.
A5	SDIO_DATA_1	I/O	SDIO data line 1.
A6	SDIO_DATA_2	I/O	SDIO data line 2.
A7	SDIO_DATA_3	I/O	SDIO data line 3.

Table 22: BCM4359 WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
WLAN GPIO Interface			
Note: The GPIO signals can be multiplexed via software and the JTAG_SEL pin to support other functions. See Table 24: "GPIO Strap Pins," on page 119 and Table 26: "GPIO Alternative Signal Functions," on page 121 for additional details.			
K12	GPIO_0	I/O	Programmable GPIO pins.
K11	GPIO_1	I/O	
K10	GPIO_2	I/O	
J9	GPIO_3	I/O	
J11	GPIO_4	I/O	
J10	GPIO_5	I/O	
H12	GPIO_6	I/O	
G11	GPIO_7	I/O	
H10	GPIO_8	I/O	
F11	GPIO_9	I/O	
G12	GPIO_10	I/O	
G10	GPIO_11	I/O	
D8	GPIO_12	I/O	
F9	GPIO_13	I/O	
J8	GPIO_14	I/O	
D7	GPIO_15	I/O	
E8	GPIO_16	I/O	Programmable GPIO pins.
C7	GPIO_17	I/O	
E5	GPIO_18	I/O	
D5	GPIO_19	I/O	
JTAG Interface			
E9	JTAG_SEL	I/O	JTAG select: pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground. ***Note:*** See Table 26: "GPIO Alternative Signal Functions," on page 121 for the JTAG signal pins.
Clocks			
V6	WRF_XTAL_XON_CORE0	O	XTAL oscillator output.
V7	WRF_XTAL_XOP_CORE0	I	XTAL oscillator input.
N6	LPO_IN	I	External sleep clock input (32.768 kHz).
N5	CLK_REQ	I/O	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.
Bluetooth Transceiver			
P1	BT_RFOP	O	Bluetooth PA output.
Bluetooth PCM			

Table 22: BCM4359 WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
G6	BT_PCM_CLK	I/O	PCM clock; can be master (output) or slave (input).
J2	BT_PCM_IN	I	PCM data input.
L3	BT_PCM_OUT	O	PCM data output.
H6	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input).
Bluetooth USB Interface			
F7	HUSB_DN	I/O	USB (Host) data negative. Negative terminal of the USB transceiver.
G7	HUSB_DP	I/O	USB (Host) data positive. Positive terminal of the USB transceiver.
Bluetooth UART			
L8	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
M8	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
K5	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
J6	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
Bluetooth I^2S			
K7	BT_I2S_CLK	I/O	I^2S clock, can be master (output) or slave (input).
M6	BT_I2S_DO	I/O	I^2S data output.
M5	BT_I2S_DI	I/O	I^2S data input.
L7	BT_I2S_WS	I/O	I^2S WS; can be master (output) or slave (input).
Bluetooth SLIMbus			
J4	BT_SLIMBUS_CK	I/O	MIPI SLIMbus clock.
J5	BT_SLIMBUS_DT	I/O	MIPI SLIMbus data.
Bluetooth GPIOs			
L6	BT_GPIO_2	I/O	Bluetooth general-purpose I/O
L5	BT_GPIO_3	I/O	Bluetooth general-purpose I/O.
K1	BT_GPIO_4	I/O	Bluetooth general-purpose I/O.
L2	BT_GPIO_5	I/O	Bluetooth general-purpose I/O.
Miscellaneous			
E4	WL_REG_ON	I	Used by PMU to power up or power down the internal BCM4359 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Table 22: BCM4359 WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
F3	BT_REG_ON	I	Used by PMU to power up or power down the internal BCM4359 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
P4	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE.
N4	BT_HOST_WAKE	I/O	Bluetooth HOST_WAKE.
Integrated Voltage Regulators			
B1	SR_VDDBAT5V	I	Power VBAT.
A2	SR_VLX	O	CBUCK switching regulator output. Refer to Table 43 on page 155 for details of the inductor and capacitor required on this output.
C1	LDO_VDD1P5	I	LNLDO input.
F1	LDO_VDDBAT5V	I	LDO VBAT.
U7	WRF_XTAL_VDD1P2_CORE0	O	XTAL LDO CORE0 output (1.2V).
T6	WRF_XTAL_VDD1P35_CORE0	I	XTAL LDO CORE0 input (1.35V).
T7	WRF_XTAL_VDD1P35_CORE1	I	XTAL LDO CORE1 input (1.35V).
D2	VOUT_LNLDO	O	Output of LNLDO.
C2	VOUT_CLDO	O	Output of core LDO.
D1	VOUT_BTLDO2P5	O	Output of BT LDO.
E2	VOUT_3P3	O	LDO 3.3V output.
G1	VOUT_PA3P3	O	Voltage sense pin for PA LDO 3.3V output.
Bluetooth Supplies			
N1	BT_PAVDD2P5	PWR	Bluetooth PA power supply.
P2	BT_LNAVDD1P2	PWR	Bluetooth LNA power supply.
L1	BT_IFVDD1P2	PWR	Bluetooth IF block power supply.
M1	BT_PLLVDD1P2	PWR	Bluetooth RF PLL power supply.
P3	BT_VCOVDD1P2	PWR	Bluetooth RF power supply.
K4	BT_VDDO	PWR	1.8V or 3.3V VIO supply.
WLAN Supplies			
V5	WRF_PMU_VDD1P35_CORE0	PWR	PMU core0 1.35V supply.
V8	WRF_PMU_VDD1P35_CORE1	PWR	PMU core1 1.35V supply.
R7	WRF_SYNTH_VDD3P3_CORE1	PWR	SYNTH core1 VDD3.3V supply.
R6	WRF_SYNTH_VDD3P3_CORE0	PWR	SYNTH core0 VDD3.3V supply.
U4	WRF_AFE_VDD1P35_CORE0	PWR	AFE core0 1.35V supply.
U9	WRF_AFE_VDD1P35_CORE1	PWR	AFE core1 1.35V supply.
V1	WRF_PA_VDD3P3_CORE0	PWR	Core0 PA 3.3V VBAT supply.
V12	WRF_PA_VDD3P3_CORE1	PWR	Core1 PA 3.3V VBAT supply.
U5	WRF_SYNTH_VDD1P2_CORE0	PWR	SYNTH CORE0 VDD 1.2V supply.

Table 22: BCM4359 WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
U8	WRF_SYNTH_VDD1P2_CORE1	PWR	SYNTH CORE1 VDD 1.2V supply.
T2	WRF_TXMIX_VDD_CORE0	PWR	TX Mixer core0 VDD 3.3V supply.
T11	WRF_TXMIX_VDD_CORE1	PWR	TX Mixer core1 VDD 3.3V supply.
Miscellaneous Supplies			
B5, C3, C9, F12, H7, H11, K6, L10, N7, N9	VDDC	PWR	1.2V core supply for WLAN.
F10, K8	VDDIO	PWR	1.8V or 3.3V supply for WLAN. Must be directly connected to PMU_VDDIO and BT_VDDO on the PCB.
J3, K2, L4	BT_VDDC	PWR	1.2V core supply for BT.
B7	VDDIO_SD	PWR	1.8V–3.3V supply for SDIO pads.
D6, M9	VDDIO_RF	PWR	IO supply for RF switch control pads (3.3V).
F8	AVDD_BBPLL	PWR	Baseband PLL supply.
B10	PLL_AVDD1P2	PWR	1.2V supply for PCIe PLL.
D11	RXTX_AVDD1P2	PWR	1.2V supply for PCIE TX and RX.
B2	VOUT_HLDO	PWR	Output of host system interface core LDO 1.2V supply.
C4	VDDC_MEM	PWR	Input power supply for the memory.
E3	VOUT_MEMLPLDO	PWR	Memory LDO output.
E1	WPT_3P3	PWR	Wireless charging 3.3V supply for BTLDO2P5 and VBAT_SEL with internal switches.
G2	WPT_1P8	PWR	Wireless charging 1.8V supply with internal switches.
F2	SYS_VDDIO	PWR	1.8V or 3.3V input of VDDIO_SEL.
G3	WCC_VDDIO	PWR	1.8V or 3.3V input for LPLDO, WPTLDO, and chip VDDOP. Output of VDDIO_SEL.
Ground			
U6	WRF_XTAL_GND1P2_CORE0	GND	XTAL CORE0 ground.
R5	WRF_VCO_GND_CORE0	GND	CORE0 VCO ground.
R8	WRF_VCO_GND_CORE1	GND	CORE1 VCO ground.
T3	WRF_AFE_GND_CORE0	GND	CORE0 AFE ground.
T10	WRF_AFE_GND_CORE1	GND	CORE1 AFE ground.
T5	WRF_SYNTH_GND_CORE0	GND	SYNTH CORE0 ground.
T8	WRF_SYNTH_GND_CORE1	GND	SYNTH CORE1 ground.
T4	WRF_GENERAL_GND_CORE0	GND	General ground.
T9	WRF_GENERAL_GND_CORE1	GND	General ground.
U3	WRF_GENERAL2_GND_CORE0	GND	General ground.
U10	WRF_GENERAL2_GND_CORE1	GND	General ground.

Table 22: BCM4359 WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
R2	WRF_RX2G_GND_CORE0	GND	RX 2GHz CORE0 ground.
R11	WRF_RX2G_GND_CORE1	GND	RX 2GHz CORE1 ground.
V4	WRF_RX5G_GND_CORE0	GND	RX 5GHz CORE0 ground.
V9	WRF_RX5G_GND_CORE1	GND	RX 5GHz CORE1 ground.
U2	WRF_PA_GND3P3_CORE0	GND	PA CORE0 ground.
U11	WRF_PA_GND3P3_CORE1	GND	PA CORE1 ground.
A3, D3, D9, E7, H9, J7, N8, P10	VSSC	GND	Core ground for WLAN and BT.
A1	SR_PVSS	GND	Power ground.
B3	PMU_AVSS	GND	Quiet ground.
H1, K3, M4	VSSC	GND	Bluetooth core ground.
M3	BT_IFVSS	GND	Bluetooth IF block ground.
M2	BT_PLLVSS	GND	Bluetooth PLL ground.
N3	BT_VCOVSS	GND	Bluetooth VCO ground.
G8	AVSS_BBPLL	GND	Baseband PLL ground.
N2	BT_LNAVSS	GND	Bluetooth LNA ground.
C10	RXTX_AVSS	GND	PCIe ground.
D10	PLL_AVSS	GND	PCIe ground.

WLAN/BT GPIO Signals and Strapping Options

The pins listed in Table 23 and Table 24 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 23: BT GPIO Functions and Strapping Options

Pin Name	Default Function	Description
BT_GPIO2	0	1: BT Serial Flash is present. 0: BT Serial Flash is absent (default).

Note: Not valid on wireless charging platform.

Strapping Options

Table 24: GPIO Strap Pins

Pin Name	Default Pull During Strapping	All Packages
GPIO_7	0	JTAG_ENABLE
GPIO_14	0	RSRC_INIT_0
GPIO_15	1	RSRC_INIT_1
GPIO_16	1	VTRIM_EN
GPIO_17	1	SDIO_PADVDDIO: 0 ≥ 3.3V, 1 ≥ 1.8V; when SDIO is enabled (strap from GPIO_18 is 0). SPROM_ABSENT: 0 ≥ SPROM present, 1 ≥ SPROM absent; when SDIO is disabled (strap from GPIO_18 is 1).
GPIO_18	1	SDIO_DISABLE: 0 ≥ SDIO enabled, 1 ≥ SDIO disabled; either PCIe or SDIO or both have to be present.
GPIO_19	1	PCIE_ENABLE: 0 ≥ PCIe disabled, 1 ≥ PCIe enabled; either PCIe or SDIO or both have to be present.

Host Interface Selection

Note: The strapping options are defined in such a way that defaults have internal pull-ups, so that it is easy to configure the strap value in opposite manner on a board (put a pull-down on the board).

Table 25: Host Interface Selection

PCIe Enable	*SDIO Disable*	*SDIO PADVDDIO/ SPROM Absent*	*Mode*
1	1	1	PCIe
1	1	0	PCIe + SPROM
0	0	1	1.8V SDIO
0	0	0	3.3V SDIO
1	0	1	PCIe + SDIO(1.8V)
1	0	0	PCIe + SDIO (3.3V)

GPIO Alternative Signal Functions

Table 26: GPIO Alternative Signal Functions

Pin Names	WLBGA	WLCSP	HW Decided/Power ON Default	GPIO_0	FAST_UART/GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/ I^2C	SPROM	MISC-0	MISC-1	MISC-2	Additional Functionality
			Function Select											
			0	2	3	4	5	6	7	8	9	10	11	
GPIO_0	Y	Y	TRISTATE_PDN	GPIO_8	–	GCI_GPIO_0	GCI_GPIO_11	–	–	–	–	SDIO_SEP_INT	SDIO_SEP_INT_OD	WL_HOST_WAKE
GPIO_1	Y	Y	TRISTATE_IND	GPIO_9	–	GCI_GPIO_1	GCI_GPIO_12	–	–	–	RF_DISABLE_L	–	–	WL_DEV_WAKE
GPIO_2	Y	Y	JTAG_SEL? TCK: TRISTATE_IND	GPIO_10	FAST_UART_RX	GCI_GPIO_2	GCI_GPIO_13	–	–	–	TCK	–	–	–
GPIO_3	Y	Y	JTAG_SEL? TMS: TRISTATE_IIND	GPIO_11	FAST_UART_TX	GCI_GPIO_3	GCI_GPIO_14	–	–	–	TMS	–	–	–
GPIO_4	Y	Y	JTAG_SEL? TDI: TRISTATE_IND	GPIO_12	FAST_UART_CTS_IN	GCI_GPIO_4	GCI_GPIO_15	DBG_UART_RX	–	–	TDI	–	–	–
GPIO_5	Y	Y	JTAG_SEL? TDO: TRISTATE_IND	GPIO_13	FAST_UART_RTS_OUT	GCI_GPIO_0	GCI_GPIO_5	DBG_UART_TX	–	–	TDO	–	–	–
GPIO_6	Y	Y	JTAG_SEL? TRST_L: TRISTATE_IND	GPIO_14	–	GCI_GPIO_1	GCI_GPIO_6	DBG_UART_RX	–	–	TRST_L	–	–	–
GPIO_7	Y	Y	TRISTATE_IND	GPIO_15	–	GCI_GPIO_2	GCI_GPIO_7	DBG_UART_TX	–	–	PMU_TEST_O	–	–	–
GPIO_8	Y	Y	TRISTATE_IND	GPIO_0	FAST_UART_RX	GCI_GPIO_3	GCI_GPIO_8	–	GSIO_SDI	–	–	–	–	–
GPIO_9	Y	Y	TRISTATE_PUP	GPIO_1	FAST_UART_TX	GCI_GPIO_4	GCI_GPIO_9	–	GSIO_SDO	–	–	–	–	–
GPIO_10	Y	Y	TRISTATE_IND	GPIO_2	FAST_UART_CTS_IN	GCI_GPIO_0	GCI_GPIO_10	DBG_UART_RX	GSIO_CSN	–	–	–	–	–
GPIO_11	Y	Y	TRISTATE_PUP	GPIO_3	FAST_UART_RTS_OUT	GCI_GPIO_1	GCI_GPIO_11	DBG_UART_TX	GSIO_CLK	–	–	–	–	–
GPIO_12	Y	Y	TRISTATE_IND	GPIO_4	–	GCI_GPIO_2	GCI_GPIO_12	DBG_UART_RX	–	–	–	SDIO_SEP_INT	SDIO_SEP_INT_OD	WL_LED1
GPIO_13	Y	Y	TRISTATE_IND	GPIO_5	–	GCI_GPIO_3	GCI_GPIO_13	DBG_UART_TX	–	–	–	–	–	WL_LED0
GPIO_14	Y	Y	TRISTATE_IND	GPIO_6	–	GCI_GPIO_4	GCI_GPIO_14	–	–	–	–	–	–	–

Table 26: GPIO Alternative Signal Functions (Cont.)

Pin Names	WLBGA	WLCSP	HW Decided/Power ON Default	GPIO_0	FAST_UART/GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/ I^2C	SPROM	MISC-0	MISC-1	MISC-2	Additional Functionality
			Function Select											
			0	2	3	4	5	6	7	8	9	10	11	
GPIO_15	Y	Y	TRISTATE_IND	GPIO_7	–	–	GCI_GPIO_15	–	–	–	–	–	–	–
GPIO_16	Y	Y	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
GPIO_17	Y	Y	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
GPIO_18	Y	Y	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
GPIO_19	Y	Y	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
SDIO_CLK	Y	Y	SDIO_EN ? SDIO_CLK: TRISTATE_IND	–	–	–	–	–	–	–	SDIO_AOS_CLK	TEST_SDIO_CLK	–	–
SDIO_CMD	Y	Y	SDIO_EN ? SDIO_CMD: (SPROM_EN ? SPROM_CS: TRISTATE_IND)	GPIO_11	–	GCI_GPIO_0	–	–	–	SPROM_CS	SDIO_AOS_CMD	TEST_SDIO_CMD	–	–
SDIO_DATA_0	Y	Y	SDIO_EN ? SDIO_DATA_0: (SPROM_EN ? SPROM_CLK: TRISTATE_IND)	GPIO_12	–	GCI_GPIO_1	–	–	–	SPROM_CLK	SDIO_AOS_D0	TEST_SDIO_DATA_0	–	–
SDIO_DATA_1	Y	Y	SDIO_EN ? SDIO_DATA_1: (SPROM_EN ? SPROM_MISO: TRISTATE_IND)	GPIO_13	–	GCI_GPIO_2	–	–	–	SPROM_MISO	SDIO_AOS_D1	TEST_SDIO_DATA_1	–	–
SDIO_DATA_2	Y	Y	SDIO_EN ? SDIO_DATA_2: TRISTATE_IND	GPIO_14	–	GCI_GPIO_3	–	–	–	–	SDIO_AOS_D2	TEST_SDIO_DATA_2	–	–
SDIO_DATA_3	Y	Y	SDIO_EN ? SDIO_DATA_3: (SPROM_EN ? SPROM_MOSI: TRISTATE_IND)	GPIO_15	–	GCI_GPIO_4	–	–	–	SPROM_MOSI	SDIO_AOS_D3	TEST_SDIO_DATA_3	–	–
RF_SW_CTRL_0	Y	Y	RF_SW_CTRL_0	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_1	Y	Y	RF_SW_CTRL_1	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_2	Y	Y	RF_SW_CTRL_2	–	–	–	–	–	–	–	–	–	–	–

Table 26: GPIO Alternative Signal Functions (Cont.)

Pin Names	WLBGA	WLCSP	HW Decided/Power ON Default	GPIO_0	FAST_UART/GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/ I^2C	SPROM	MISC-0	MISC-1	MISC-2	Additional Functionality
			Function Select											
			0	2	3	4	5	6	7	8	9	10	11	
RF_SW_CTRL_3	Y	Y	RF_SW_CTRL_3	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_4	Y	Y	RF_SW_CTRL_4	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_5	Y	Y	RF_SW_CTRL_5	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_6	Y	Y	RF_SW_CTRL_6	GPIO_8	GPIO_0	–	GCI_GPIO_8	–	GSIO_SDI	–	–	–	–	–
RF_SW_CTRL_7	Y	Y	RF_SW_CTRL_7	GPIO_9	GPIO_1	–	GCI_GPIO_9	–	GSIO_SDO	–	–	–	–	–
RF_SW_CTRL_8	Y	Y	RF_SW_CTRL_8	GPIO_10	GPIO_2	–	GCI_GPIO_10	DBG_UART_RX	GSIO_CSN	–	–	–	–	–
RF_SW_CTRL_9	Y	Y	RF_SW_CTRL_9	GPIO_11	GPIO_3	–	GCI_GPIO_11	DBG_UART_TX	GSIO_CLK	–	PALDO_PU	–	–	–
RF_SW_CTRL_10	Y	Y	RF_SW_CTRL_10	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_11	Y	Y	RF_SW_CTRL_11	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_12	Y	Y	RF_SW_CTRL_12	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_13	Y	Y	RF_SW_CTRL_13	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_14	Y	Y	RF_SW_CTRL_14	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_15	Y	Y	RF_SW_CTRL_15	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_16	Y	Y	RF_SW_CTRL_16	GPIO_12	GPIO_4	–	GCI_GPIO_12	–	GSIO_CLK	–	–	–	–	–
RF_SW_CTRL_17	Y	Y	RF_SW_CTRL_17	GPIO_13	GPIO_5	–	GCI_GPIO_13	–	GSIO_CSN	–	–	–	–	–
RF_SW_CTRL_18	Y	Y	RF_SW_CTRL_18	GPIO_14	GPIO_6	–	GCI_GPIO_14	DBG_UART_TX	GSIO_SDO	–	–	–	–	–
RF_SW_CTRL_19	Y	Y	RF_SW_CTRL_19	GPIO_15	GPIO_7	–	GCI_GPIO_15	DBG_UART_RX	GSIO_SDI	–	PALDO_PD	–	–	–

Table 27 defines status for all BCM4359 GPIOs based on the tristate test mode.

Table 27: GPIO Status Versus Test Modes

Test Mode	*Function Select*	*Status of All GPIOs*
TRISTATE_IND	12	Input disable
TRISTATE_PDN	13	Pull down
TRISTATE_PUP	14	Pull up
TRISTATE	15	Tristate

I/O States

The following notations are used in Table 28:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down
- Where applicable, the default value is shown in bold brackets (for example, [default value])

Table 28: WLAN-Side of PMIO States

Name	*I/O*	*Keeper*	*Active Mode*	*Low-Power State/Sleep (All Power Present)*	*Power-down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)*	*(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present*	*Power Rail*
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down can be disabled	I: PD Pull-down can be disabled	I: PD (of 200K)	I: PD (of 200K)	I: PD (of 200K)	–
SDIO DATA[a]	I/O	N	I/O: PU	I/O: PU	High-Z, NoPull	I/O: PU	I/O: PU	VDDIO_SD
SDIO CMD[a]	I/O	N	I/O: PU	I/O: PU	High-Z, NoPull	I/O: PU	I/O: PU	VDDIO_SD
SDIO_CLK[a]	I	N	I: NoPull	I: NoPull	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO_SD
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	I: PD	I: PD	VDDIO
GPIO_1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[b]	I: NoPull	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[b]	I: NoPull	VDDIO
GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[b]	I: NoPull	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[b]	I: NoPull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[b]	I: NoPull	VDDIO

Table 28: WLAN-Side of PMIO States (Cont.)

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_9	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	High-Z, NoPull	I: PU	I:PU	VDDIO
GPIO_10	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_11	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	High-Z, NoPull	I: PU	I:PU	VDDIO
GPIO_12	I/O	N	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_13	I/O	N	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_14	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_15	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_16	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_18	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_19	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
RF_SW_CTRL_X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RF

a. In SDIO mode.
b. When JTAG is not enabled on the GPIO.

Section 13: DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 29 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 29: Absolute Maximum Ratings

Rating	*Symbol*	*Value*	*Unit*
DC supply for VBAT and PA driver supply	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O[a]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[a]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C
DC supply voltage for wireless charging	WPT_3p3	–0.5 to 3.9	V
DC supply voltage for wireless charging	WPT_1p8 V	–0.5 to 3.9	V
DC supply voltage for WCC I/O	WCC_VDDIO V	–0.5 to 3.9	V

a. Duration not to exceed 25% of the duty cycle.

Environmental Ratings

The environmental ratings are shown in Table 30.

Table 30: Environmental Ratings

Characteristic	*Value*	*Units*	*Conditions/Comments*
Ambient Temperature (T_A)	–30 to +85	°C	Functional operation[a]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed across this range of temperature. Optimal RF performance specified in the data sheet, however, is guaranteed only for –10°C to +55°C without derating performance.

Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 31, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 31: Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0[a]	–	5.25[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.62	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
DC supply voltage for wireless charging	WPT_1p8, WPT_3p3	1.62	–	3.63	V
DC supply voltage for WCC I/O	WCC_VDDIO	1.62	–	3.63	V
SDIO Interface I/O Pins and PCIe Out-of-Band Signals (PCIE_PERST_L, PCIE_PME_L, and PCIE_CLKREQ_L)					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V

Table 31: Recommended Operating Conditions and DC Characteristics (Cont.)

		Value			
Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:		–	–	–	
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage@ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[c]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

a. The BCM4359 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 4.8V.
b. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
c. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 32: ESD Specifications

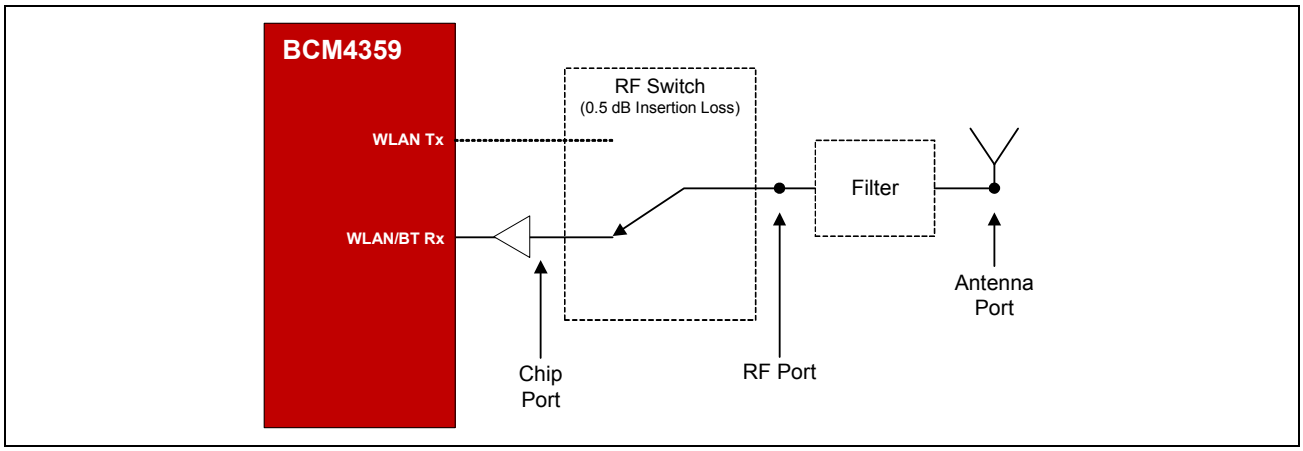
Pin Type	*Symbol*	*Condition*	*ESD Rating*	*Unit*
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/ JESD22-A114	TBD	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/ JESD22-C101	TBD	V

Section 14: Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 30: “Environmental Ratings,” on page 128 and Table 31: “Recommended Operating Conditions and DC Characteristics,” on page 129. Typical values apply for an ambient temperature of +25°C.

Figure 31: RF Port Location for Bluetooth Testing



Note: All Bluetooth specifications are measured at the chip port unless otherwise specified.

Table 33: Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm

Table 33: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
RX LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
Interference Performance[a]					
C/I co-channel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20	dB
C/I co-channel	π/4-DQPSK, 0.1% BER	–	–	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–40	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20	dB
C/I co-channel	8-DPSK, 0.1% BER	–	–	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer					
	GFSK (1 Mbps)[b]				
698–716 MHz	WCDMA	–	–13	–	dBm
776–849 MHz	WCDMA	–	–14	–	dBm
824–849 MHz	GSM850	–	–13	–	dBm
824–849 MHz	WCDMA	–	–14	–	dBm
880–915 MHz	E-GSM	–	–13	–	dBm
880–915 MHz	WCDMA	–	–13	–	dBm
1710–1785 MHz	GSM1800	–	–18	–	dBm

Table 33: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
1710–1785 MHz	WCDMA	–	–17	–	dBm
1850–1910 MHz	GSM1900	–	–19	–	dBm
1850–1910 MHz	WCDMA	–	–19	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20	–	dBm
1920–1980 MHz	WCDMA	–	–20	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20	–	dBm
2500–2570 MHz	WCDMA	–	–23	–	dBm
2510 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–26	–	dBm
2530 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–23	–	dBm
2550 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–22	–	dBm
2570 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–22	–	dBm
2310 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–22	–	dBm
2330 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–21	–	dBm
2350 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–22	–	dBm
2370 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–26	–	dBm
2570–2620 MHz[e]	Band 38	–	–22	–	dBm
2545–2575 MHz[f]	XGP Band	–	–23	–	dBm
	π/4-DPSK (2 Mbps)[b]				
698–716 MHz	WCDMA	–	–10	–	dBm
776–794 MHz	WCDMA	–	–10	–	dBm
824–849 MHz	GSM850	–	–11	–	dBm
824–849 MHz	WCDMA	–	–11	–	dBm
880–915 MHz	E-GSM	–	–10	–	dBm
880–915 MHz	WCDMA	–	–10	–	dBm
1710–1785 MHz	GSM1800	–	–16	–	dBm
1710–1785 MHz	WCDMA	–	–15	–	dBm
1850–1910 MHz	GSM1900	–	–17	–	dBm
1850–1910 MHz	WCDMA	–	–16	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18	–	dBm
1920–1980 MHz	WCDMA	–	–17	–	dBm
2010–2025 MHz	TD-SCDMA	–	–19	–	dBm
2500–2570 MHz	WCDMA	–	–23	–	dBm

Table 33: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
2510 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–26	–	dBm
2530 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–22	–	dBm
2550 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–22	–	dBm
2570 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–22	–	dBm
2310 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–22	–	dBm
2330 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–21	–	dBm
2350 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–22	–	dBm
2370 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–26	–	dBm
2570–2620 MHz[e]	Band 38	–	–22	–	dBm
2545–2575 MHz[f]	XGP Band	–	–25	–	dBm
	8-DPSK (3 Mbps)[g]				
698–716 MHz	WCDMA	–	–13	–	dBm
776–794 MHz	WCDMA	–	–13	–	dBm
824–849 MHz	GSM850	–	–13	–	dBm
824–849 MHz	WCDMA	–	–14	–	dBm
880–915 MHz	E-GSM	–	–13	–	dBm
880–915 MHz	WCDMA	–	–13	–	dBm
1710–1785 MHz	GSM1800	–	–18	–	dBm
1710–1785 MHz	WCDMA	–	–17	–	dBm
1850–1910 MHz	GSM1900	–	–19	–	dBm
1850–1910 MHz	WCDMA	–	–19	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19	–	dBm
1920–1980 MHz	WCDMA	–	–19	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20	–	dBm
2500–2570 MHz	WCDMA	–	–23	–	dBm
2510 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–26	–	dBm
2530 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–23	–	dBm
2550 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–22	–	dBm
2570 MHz[c]	LTE band 7 FDD 20 MHz BW	–	–22	–	dBm

Table 33: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
2310 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–23	–	dBm
2330 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–21	–	dBm
2350 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–22	–	dBm
2370 MHz[d]	LTE band 40 TDD 20 MHz BW	–	–26	–	dBm
2570–2620 MHz[e]	Band 38	–	–22	–	dBm
2545–2575 MHz[f]	XGP Band	–	–24	–	dBm
Spurious Emissions					
30 MHz–1 GHz		–	–95	–62	dBm
1–12.75 GHz		–	–70	–47	dBm
851–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
b. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = –84.5 dBm.
c. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
d. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
e. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
f. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
g. Bluetooth reference level for the wanted signal at the Bluetooth chip port = –79.5 dBm.

Table 34: Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		–	14.0	–	dBm
QPSK TX power at Bluetooth		–	10.0	–	dBm
8PSK TX power at Bluetooth		–	10.0	–	dBm
Power control step	–	–	4	–	dB
Note: Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31	–20.0	dBm
|M – N| ≥ 2.5 MHz[a]		–	–43	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[b, c]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[b, d, e]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm
Out-of-Band Noise Floor[f]					
65–108 MHz	FM RX	–	–177	–	dBm/Hz
776–794 MHz	CDMA2000	–	–177	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–177	–	dBm/Hz
925–960 MHz	E-GSM	–	–174	–	dBm/Hz
1570–1580 MHz	GPS	–	–164	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–160	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–152	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–145	–	dBm/Hz
2500–2570 MHz	Band 7	–	–135	–	dBm
2300–2400 MHz	Band 40	–	–135	–	dBm
2570–2620 MHz	Band 38	–	–135	–	dBm
2545–2575 MHz	XGP Band	–	–135	–	dBm

a. The typical number is measured at ± 3 MHz offset.
b. The maximum value represents the value required for Bluetooth qualification as defined in the v4.0 specification.

c. The spurious emissions during Idle mode are the same as specified in Table 34 on page 137.
d. Specified at the Bluetooth Antenna port.
e. Meets this specification using a front–end band–pass filter.
f. Transmitted power in cellular and FM bands at the Bluetooth Antenna port. See Figure 31 on page 132 for location of the port.

Table 35: Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	155	175	kHz
10101010 sequence in payload[b]	115	140	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 36: BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402	–	2480	MHz
RX sense[a]	GFSK, 0.1% BER, 1 Mbps	–	–95.5	–	dBm
TX power[b]	–	–	8.5	–	dBm
Mod Char: delta F1 average	–	225	255	275	kHz
Mod Char: delta F2 average	–	230	–	–	kHz
Mod Char: ratio	–	0.8	1.00	–	%

a. Dirty TX is off.
b. The BLE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.

Section 15: WLAN RF Specifications

Introduction

The BCM4359 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radios.

Note: Values in this section of the data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified inTable 30: “Environmental Ratings,” on page 128 and Table 31: “Recommended Operating Conditions and DC Characteristics,” on page 129. Typical values apply for an ambient temperature +25°C.

Figure 32: Port Locations (Applies to 2.4 GHz)

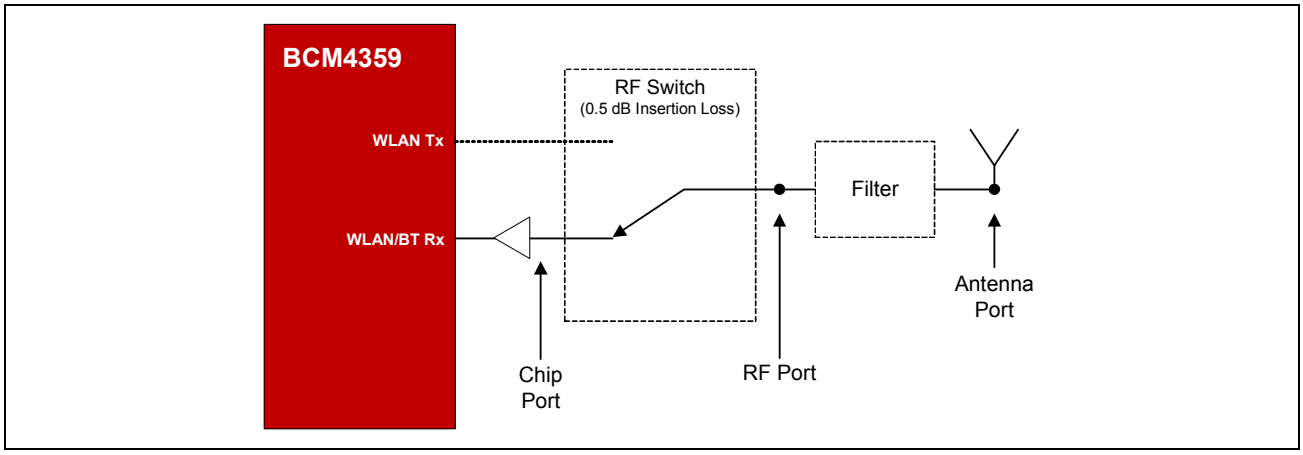
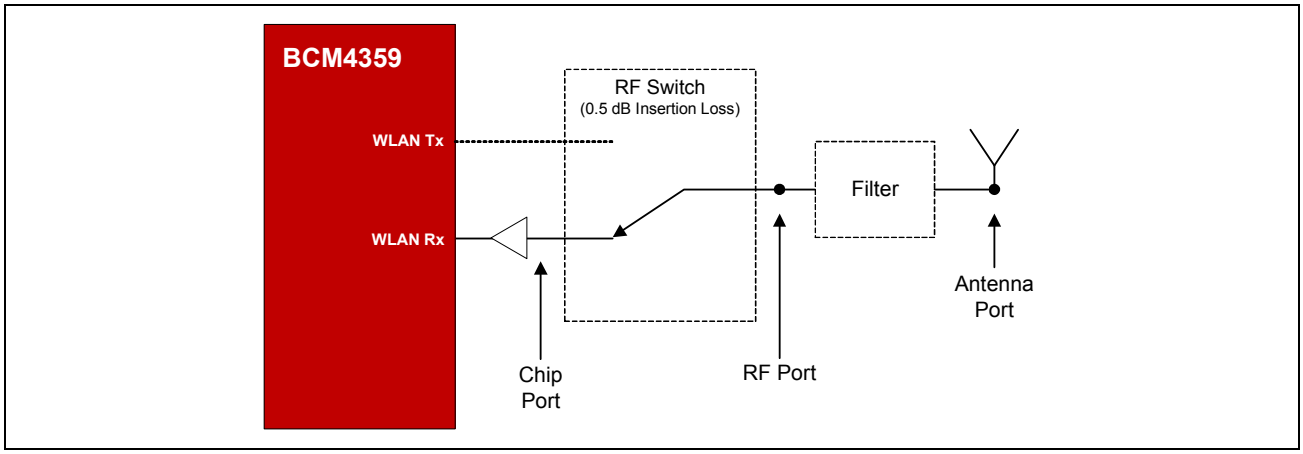


Figure 33: Port Locations (Applies to 5 GHz)



2.4 GHz Band General RF Specifications

Table 37: 2.4 GHz Band General RF Specifications

Item	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The values in Table 38 are specified at the RF port unless otherwise noted.

Table 38: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity IEEE 802.11b	1 Mbps DSSS	–	–98.4	–	dBm
	2 Mbps DSSS	–	–96.5	–	dBm
	5.5 Mbps DSSS	–	–93.7	–	dBm
	11 Mbps DSSS	–	–91.4	–	dBm
SISO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–95.5	–	dBm
	9 Mbps OFDM	–	–94.1	–	dBm
	12 Mbps OFDM	–	–93.2	–	dBm
	18 Mbps OFDM	–	–90.6	–	dBm
	24 Mbps OFDM	–	–87.3	–	dBm
	36 Mbps OFDM	–	–84	–	dBm
	48 Mbps OFDM	–	–79.3	–	dBm
	54 Mbps OFDM	–	–77.8	–	dBm
MIMO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–96.5	–	dBm/core
	9 Mbps OFDM	–	–96	–	dBm/core
	12 Mbps OFDM	–	–95.2	–	dBm/core
	18 Mbps OFDM	–	–93.6	–	dBm/core
	24 Mbps OFDM	–	–90.3	–	dBm/core
	36 Mbps OFDM	–	–87	–	dBm/core
	48 Mbps OFDM	–	–82.3	–	dBm/core
	54 Mbps OFDM	–	–80.8	–	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non–STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–95	–	dBm
	MCS1	–	–92.7	–	dBm
	MCS2	–	–90.2	–	dBm
	MCS3	–	–87.1	–	dBm
	MCS4	–	–83.5	–	dBm
	MCS5	–	–78.9	–	dBm
	MCS6	–	–77.3	–	dBm
	MCS7	–	–75.7	–	dBm

Table 38: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non–STBC.	20 MHz channel spacing for all MCS rates					
	MCS0		–	–96.5	–	dBm/core
	MCS1		–	–95.7	–	dBm/core
	MCS2		–	–93.2	–	dBm/core
	MCS3		–	–90.1	–	dBm/core
	MCS4		–	–86.5	–	dBm/core
	MCS5		–	–81.9	–	dBm/core
	MCS6		–	–80.3	–	dBm/core
	MCS7		–	–78.7	–	dBm/core
	MCS8		–	–95	–	dBm/core
	MCS15		–	–75.7	–	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non–STBC	20 MHz channel spacing for all MCS rates					
	MCS0, Nss 1		–	–94.3	–	dBm
	MCS1, Nss 1		–	–91.9	–	dBm
	MCS2, Nss 1		–	–90.1	–	dBm
	MCS3, Nss 1		–	–86.9	–	dBm
	MCS4, Nss 1		–	–83.4	–	dBm
	MCS5, Nss 1		–	–78.9	–	dBm
	MCS6, Nss 1		–	–77.3	–	dBm
	MCS7, Nss 1		–	–75.6	–	dBm
	MCS8, Nss 1		–	–71.2	–	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non–STBC	20 MHz channel spacing for all MCS rates					
	MCS0, Nss 1		–	–95.8	–	dBm/core
	MCS1, Nss 1		–	–94.9	–	dBm/core
	MCS2, Nss 1		–	–93.1	–	dBm/core
	MCS3, Nss 1		–	–89.9	–	dBm/core
	MCS4, Nss 1		–	–86.4	–	dBm/core
	MCS5, Nss 1		–	–81.9	–	dBm/core
	MCS6, Nss 1		–	–80.3	–	dBm/core
	MCS7, Nss 1		–	–78.6	–	dBm/core
	MCS8, Nss 1		–	–74.2	–	dBm/core
	MCS0, Nss 2		–	–94	–	dBm/core
	MCS8, Nss 2		–	–70.1	–	dBm/core
SISO RX sensitivity IEEE 802.11ac 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU)[a] at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 1	20 MHz	–	–77.4	–	dBm
	MCS8, Nss 1	20 MHz	–	–74.7	–	dBm
	MCS9, Nss 1	20 MHz	–	–71.4	–	dBm

Table 38: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11ac 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU)[a] at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 2	20 MHz	–	–76	–	dBm/core
	MCS8, Nss 2	20 MHz	–	–73.2	–	dBm/core
	MCS9, Nss 2	20 MHz	–	–70	–	dBm/core
Blocking level for 12 dB desense at the chip port (without external filtering)[b]	776–794 MHz	CDMA2000	–	–12.7	–	dBm
	824–849 MHz[c]	cdmaOne	–	–12.4	–	dBm
	824–849 MHz[c]	GSM850	–	–6.8	–	dBm
	880–915 MHz	E–GSM	–	–6.65	–	dBm
	1710–1785 MHz	GSM1800	–	–10.2	–	dBm
	1850–1910 MHz	GSM1800	–	–8.4	–	dBm
	1850–1910 MHz	cdmaOne	–	–13.2	–	dBm
	1850–1910 MHz	WCDMA	–	–9.4	–	dBm
	1920–1980 MHz	WCDMA	–	–10.8	–	dBm
	2500–2570 MHz	Band 7	–	–23.1	–	dBm
	2300–2400 MHz	Band 40	–	–17.8	–	dBm
	2570-2620 MHz	Band 38	–	–13.95	–	dBm
	2545-2575 MHz	XGP band	–	–15.325	–	dBm
In-band static CW jammer immunity (fc - 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSense + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Input In–Band IP3	Maximum LNA gain		–	–10	–	dBm
	Minimum LNA gain		–	11	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–9.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–9.5	–	–	dBm
	@ MCS8–9 rates (10% PER, 4095 octets)		–11.5	–	–	dBm
LPF 3 dB Bandwidth	–		9	–	36	MHz
Adjacent channel rejection–DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	Desired and interfering signal 30 MHz apart					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB

Table 38: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Adjacent channel rejection–OFDM (difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–9 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
	MCS8	–59 dBm	–4	–	–	dB
	MCS9	–57 dBm	–6	–	–	dB
IEEE 802.11ac Adjacent channel rejection MCS0–9 (Difference between interfering and desired signal at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–82 dBm	–	–	–	dB
	MCS1	–80 dBm	–	–	–	dB
	MCS2	–77 dBm	–	–	–	dB
	MCS3	–74 dBm	–	–	–	dB
	MCS4	–70 dBm	–	–	–	dB
	MCS5	–66 dBm	–	–	–	dB
	MCS6	–65 dBm	–	–	–	dB
	MCS7	–64 dBm	–	–	–	dB
	MCS8	–59 dBm	–	–	–	dB
	MCS9	–57 dBm	–	–	–	dB
Maximum receiver gain	–	–	–	66	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[d]	Range –90 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Zo = 50Ω, across the dynamic range		10	11.5	13	dB
Receiver cascaded noise figure	At maximum gain		–	3.2	–	dB

a. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
d. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The values in Table 39 are specified at the RF port unless otherwise noted.

Table 39: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands (at 18 dBm, 100% duty cycle, 1 Mbps CCK)[a]	76–108 MHz	FM RX	–	–149	–	dBm/Hz
	776–794 MHz	–	–	–165	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–155	–	dBm/Hz
	925–960 MHz	E-GSM	–	–160	–	dBm/Hz
	1570–1580 MHz	GPS	–	–150	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–145	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–143	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–135	–	dBm/Hz
	2500–2570 MHz	Band 7	–	–107	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–100	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–125	–	dBm/Hz
	2545–2575 MHz	XGP Band	–	–117	–	dBm/Hz
Harmonic level (at 18 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–29	–	dBm/1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–18	–	dBm/1 MHz
		EVM Does Not Exceed				
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance	802.11b (DSSS/CCK)	–9 dB	18	19.5	–	dBm
	OFDM, BPSK	–8 dB	18	19	–	dBm
	OFDM, QPSK	–13 dB	18	19	–	dBm
	OFDM, 16-QAM	–19 dB	16.5	18	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	15.5	17	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	14.5	16	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	–30 dB	13.5	15	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT20)	–32 dB	12	13.5	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees

Table 39: WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
TX power control dynamic range	–	10	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies across 10 dBm to 20 dBm output power range.	–	–	±1.5	dB
Carrier suppression	–	15	–	–	dBc
Gain control step	–	–	0.25	–	dB
Return loss at chip port TX	Zo = 50Ω	–	6	–	dB

a. The cellular standards listed only indicate the typical usages of that band in some countries: other standards may also be used within those bands.

WLAN 5 GHz Receiver Performance Specifications

Note: The values in Table 40 are specified at the RF port unless otherwise noted.

Table 40: WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency range	–	4900	–	5845	MHz
SISO RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps OFDM	–	–94.5	–	dBm
	9 Mbps OFDM	–	–93.1	–	dBm
	12 Mbps OFDM	–	–92.2	–	dBm
	18 Mbps OFDM	–	–89.6	–	dBm
	24 Mbps OFDM	–	–86.3	–	dBm
	36 Mbps OFDM	–	–83	–	dBm
	48 Mbps OFDM	–	–78.3	–	dBm
	54 Mbps OFDM	–	–76.8	–	dBm
MIMO RX sensitivity IEEE 802.11a (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–95.5	–	dBm/core
	9 Mbps OFDM	–	–95	–	dBm/core
	12 Mbps OFDM	–	–94.2	–	dBm/core
	18 Mbps OFDM	–	–92.6	–	dBm/core
	24 Mbps OFDM	–	–89.3	–	dBm/core
	36 Mbps OFDM	–	–86	–	dBm/core
	48 Mbps OFDM	–	–81.3	–	dBm/core
	54 Mbps OFDM	–	–77.8	–	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94	–	dBm
	MCS1	–	–91.7	–	dBm
	MCS2	–	–89.2	–	dBm
	MCS3	–	–86.1	–	dBm
	MCS4	–	–82.5	–	dBm
	MCS5	–	–77.9	–	dBm
	MCS6	–	–76.3	–	dBm
	MCS7	–	–74.7	–	dBm

Table 40: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–95.5	–	dBm/core
	MCS1	–	–94.7	–	dBm/core
	MCS2	–	–92.2	–	dBm/core
	MCS3	–	–89.1	–	dBm/core
	MCS4	–	–85.5	–	dBm/core
	MCS5	–	–80.9	–	dBm/core
	MCS6	–	–79.3	–	dBm/core
	MCS7	–	–77.7	–	dBm/core
	MCS8	–	–94	–	dBm/core
	MCS15	–	–74.7	–	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–91.8	–	dBm
	MCS1	–	–88.9	–	dBm
	MCS2	–	–86.5	–	dBm
	MCS3	–	–83	–	dBm
	MCS4	–	–79.9	–	dBm
	MCS5	–	–75.2	–	dBm
	MCS6	–	–73.7	–	dBm
	MCS7	–	–72.3	–	dBm
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–93.3	–	dBm/core
	MCS1	–	–91.9	–	dBm/core
	MCS2	–	–89.5	–	dBm/core
	MCS3	–	–86	–	dBm/core
	MCS4	–	–82.9	–	dBm/core
	MCS5	–	–78.2	–	dBm/core
	MCS6	–	–76.7	–	dBm/core
	MCS7	–	–75.3	–	dBm/core
	MCS8	–	–91.8	–	dBm/core
	MCS15	–	–72.3	–	dBm/core

Table 40: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–93.3	–	dBm
	MCS1, Nss 1	–	–90.3	–	dBm
	MCS2, Nss 1	–	–88	–	dBm
	MCS3, Nss 1	–	–85	–	dBm
	MCS4, Nss 1	–	–81.4	–	dBm
	MCS5, Nss 1	–	–76.9	–	dBm
	MCS6, Nss 1	–	–75.3	–	dBm
	MCS7, Nss 1	–	–74.6	–	dBm
	MCS8, Nss 1	–	–70.2	–	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–94.8	–	dBm/core
	MCS1, Nss 1	–	–93.3	–	dBm/core
	MCS2, Nss 1	–	–91	–	dBm/core
	MCS3, Nss 1	–	–88	–	dBm/core
	MCS4, Nss 1	–	–84.4	–	dBm/core
	MCS5, Nss 1	–	–79.9	–	dBm/core
	MCS6, Nss 1	–	–78.3	–	dBm/core
	MCS7, Nss 1	–	–77.6	–	dBm/core
	MCS8, Nss 1	–	–73.2	–	dBm/core
	MCS0, Nss 2	–	–93	–	dBm/core
	MCS8, Nss 2	–	–69.1	–	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–90.5	–	dBm
	MCS1, Nss 1	–	–87.5	–	dBm
	MCS2, Nss 1	–	–85.7	–	dBm
	MCS3, Nss 1	–	–82.5	–	dBm
	MCS4, Nss 1	–	–79.5	–	dBm
	MCS5, Nss 1	–	–74.5	–	dBm
	MCS6, Nss 1	–	–73.7	–	dBm
	MCS7, Nss 1	–	–72.3	–	dBm
	MCS8, Nss 1	–	–67.9	–	dBm
	MCS9, Nss 1	–	–66.6	–	dBm

Table 40: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–92	–	dBm/core
	MCS1, Nss 1	–	–90.5	–	dBm/core
	MCS2, Nss 1	–	–88.7	–	dBm/core
	MCS3, Nss 1	–	–85.5	–	dBm/core
	MCS4, Nss 1	–	–82.5	–	dBm/core
	MCS5, Nss 1	–	–77.5	–	dBm/core
	MCS6, Nss 1	–	–76.7	–	dBm/core
	MCS7, Nss 1	–	–75.3	–	dBm/core
	MCS8, Nss 1	–	–70.9	–	dBm/core
	MCS9, Nss 1	–	–69.6	–	dBm/core
	MCS0, Nss 2	–	–90	–	dBm/core
	MCS9, Nss 2	–	–65.2	–	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	80 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–87	–	dBm
	MCS1, Nss 1	–	–84	–	dBm
	MCS2, Nss 1	–	–82	–	dBm
	MCS3, Nss 1	–	–78.7	–	dBm
	MCS4, Nss 1	–	–75.7	–	dBm
	MCS5, Nss 1	–	–72.5	–	dBm
	MCS6, Nss 1	–	–70	–	dBm
	MCS7, Nss 1	–	–68.5	–	dBm
	MCS8, Nss 1	–	–64.3	–	dBm
	MCS9, Nss 1	–	–62.5	–	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	80 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–88.5	–	dBm/core
	MCS1, Nss 1	–	–87	–	dBm/core
	MCS2, Nss 1	–	–85	–	dBm/core
	MCS3, Nss 1	–	–81.7	–	dBm/core
	MCS4, Nss 1	–	–78.7	–	dBm/core
	MCS5, Nss 1	–	–75.5	–	dBm/core
	MCS6, Nss 1	–	–73	–	dBm/core
	MCS7, Nss 1	–	–71.5	–	dBm/core
	MCS8, Nss 1	–	–67.3	–	dBm/core
	MCS9, Nss 1	–	–65.5	–	dBm/core
	MCS0, Nss 2	–	–86.3	–	dBm/core
	MCS9, Nss 2	–	–61.5	–	dBm/core

Table 40: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*		*Min.*	*Typ.*	*Max.*	*Unit*
SISO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU)[a] at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 1	20 MHz	–	–76.4	–	dBm
	MCS8, Nss 1	20 MHz	–	–73.7	–	dBm
	MCS9, Nss 1	20 MHz	–	–70.4	–	dBm
	MCS7, Nss 1	40 MHz	–	–73.8	–	dBm
	MCS8, Nss 1	40 MHz	–	–69.5	–	dBm
	MCS9, Nss 1	40 MHz	–	–68.5	–	dBm
	MCS7, Nss 1	80 MHz	–	–70	–	dBm
	MCS8, Nss 1	80 MHz	–	–66.3	–	dBm
	MCS9, Nss 1	80 MHz	–	–64.5	–	dBm
MIMO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU)[a] at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 2	20 MHz	–	–75	–	dBm/core
	MCS8, Nss 2	20 MHz	–	–72.2	–	dBm/core
	MCS9, Nss 2	20 MHz	–	–68.5	–	dBm/core
	MCS7, Nss 2	40 MHz	–	–72.8	–	dBm/core
	MCS8, Nss 2	40 MHz	–	–68	–	dBm/core
	MCS9, Nss 2	40 MHz	–	–66.7	–	dBm/core
	MCS7, Nss 2	80 MHz	–	–69	–	dBm/core
	MCS8, Nss 2	80 MHz	–	–64.8	–	dBm/core
	MCS9, Nss 2	80 MHz	–	–62.5	–	dBm/core
Alternate adjacent channel rejection Blocking level for 12 dB desense at the chip port (without external filtering)[b]	776–794 MHz	CDMA2000	–11.2	–	–	dBm
	824–849 MHz[c]	cdmaOne	–10.8	–	–	dBm
	824–849 MHz[c]	GSM850	0.35	–	–	dBm
	880–915 MHz	E-GSM	–3.9	–	–	dBm
	1710–1785 MHz	GSM1800	–0.6	–	–	dBm
	1850–1910 MHz	GSM1800	–1.9	–	–	dBm
	1850–1910 MHz	cdmaOne	–8.7	–	–	dBm
	1850–1910 MHz	WCDMA	–3.4	–	–	dBm
	1920–1980 MHz	WCDMA	–4.4	–	–	dBm
	2500–2570 MHz	Band 7	–9.9	–	–	dBm
	2300–2400 MHz	Band 40	–11.2	–	–	dBm
	2570–2620 MHz	Band 38	–10.4	–	–	dBm
	2545–2575 MHz	XGP Band	–10.5	–	–	dBm
Input In-Band IP3	Maximum LNA gain		–	–12	–	dBm
	Minimum LNA gain		–	4	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps		–9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps		–14.5	–	–	dBm
LPF 3 dB bandwidth	–		9	–	36	MHz

Table 40: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
(Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[d] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	66	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[e]	Range –90 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Zo = 50Ω, across the dynamic range		10	–	13	dB
Receiver cascaded noise figure	At maximum gain		–	4	–	dB

a. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
d. For 65 Mbps, the size is 4096.
e. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Transmitter Performance Specifications

Note: The values in Table 41 are specified at the RF port unless otherwise noted.

Table 41: WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands (at 18 dBm)[a]	76–108 MHz	FM RX	–	–162	–	dBm/Hz
	776–794 MHz	–	–	–162	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–162	–	dBm/Hz
	925–960 MHz	E-GSM	–	–162	–	dBm/Hz
	1570–1580 MHz	GPS	–	–159	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–150	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–142	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–148	–	dBm/Hz
	2400–2483 MHz	BT/WLAN	–	–157	–	dBm/Hz
	2500–2570 MHz	Band 7	–	–157	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–157	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–157	–	dBm/Hz
	2545–2575 MHz	XGP Band	–	–140	–	dBm/Hz
Harmonic level (at 17 dBm)	9.8–11.570 GHz	2nd harmonic	–	–30	–	dBm/MHz
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance	802.11b (DSSS/CCK)	–9 dB	18	19.5	–	dBm
	OFDM, BPSK	–8 dB	18	19	–	dBm
	OFDM, QPSK	–13 dB	18	19	–	dBm
	OFDM, 16-QAM	–19 dB	16.5	18	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	15.5	17	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	14.5	16	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	–30 dB	13.5	15	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT20)	–32 dB	12	13.5	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees

Table 41: WLAN 5 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
TX power control dynamic range	–	10	–	–	dB
Closed loop TX power variation at highest power level setting	Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range.	–	–	±2.0	dB
Carrier suppression	–	15	–	–	dBc
Gain control step	–	–	0.25	–	dB
Return loss	Zo = 50Ω	–	6	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

General Spurious Emissions Specifications

Table 42: General Spurious Emissions Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–85	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–31	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–81	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–86	–	dBm
RX/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–100	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–60	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–87	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–87	–	dBm

Section 16: Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Note: Functional operation is not guaranteed outside of the specification limits provided in this section.

Core Buck Switching Regulator

Table 43: Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.6	4.8[a]	V
PWM mode switching frequency	CCM, Load > 100 mA VBAT = 3.6V	2.8	4	5.2	MHz
PWM output current	–	–	–	600	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps Default = 1.35V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode	–4	–	4	% ±2 with trim
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max Ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load	78	86	–	%
PFM mode efficiency	10 mA load current	–	80	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	–	500	µs
External inductor	0806 size, ± 30%, 0.11 ± 25% Ohms	0.67[b]	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, ± 20%, 6.3V	2.0[c]	4.7	10[d]	µF

Table 43: Core Buck Switching Regulator (CBUCK) Specifications (Cont.)

Specification	Notes	Min.	Typ.	Max.	Units
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 10V, 4.7 µF	0.67[c]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

a. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Effective inductance under current-bias and part-to-part tolerance.
c. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
d. Total capacitance includes those connected at the far end of the active load.

3.3V LDO (PALDO3P3)

Table 44: PALDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min = V_o + 0.2V = 3.1V (for V_o = 2.9V) dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[a]	V
Output current	–	0.2	–	650	mA
Nominal output voltage, V_o	Default = 3.3V	–	3.3	–	V
Dropout voltage	At max load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	100	120	µA
	Maximum load (600 mA)	–	5.8	6	mA
Leakage current	Power-Down mode, junction temperature = 85°C	–	1.5	5	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.25	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 3.3V, C_o = 4.7 µF, Max load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	C_o = 4.7 µF (plus other board capacitor max 4.7 µF)	–	160	210	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	1.0[b]	4.7	–	µF

Table 44: PALDO3P3 Specifications (Cont.)

Specification	Notes	Min.	Typ.	Max.	Units
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

3.3V LDO (LDO3P3)

Table 45: LDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min = V_o + 0.2V = 3.1V (for V_o = 2.9V) Dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[a]	V
Output current	–	0.1	–	200	mA
Nominal output voltage, V_o	Default = 3.3V	–	3.3	–	V
Dropout voltage	At max load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	35	40	µA
	Maximum load	–	1.94	1.97	mA
Leakage current	Power-Down mode, junction temperature = 85°C	–	1.5	5	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 3.3V, C_o = 4.7 µF, Max load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	0.7[b]	2.2	–	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402	–	4.7	–	µF

a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part–to–part tolerance, DC–bias, temperature, and aging.

2.5V LDO (BTLDO2P5)

Table 46: BTLDO2P5 Specifications

Specification	*Notes*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage	Min = 2.8V + 0.3V = 3.1V (for V_o = 2.8V) Dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[a]	V
Nominal output voltage	Default = 2.5V.	–	2.5	–	V
Output voltage programmability	Range	2.2	2.5	2.8	V
	Accuracy at any step (including line/load regulation), load > 0.1 mA.	–5	–	5	%
Dropout voltage	At maximum load.	–	–	300	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load.	–	8	16	µA
	Maximum load at 70 mA.	–	660	700	µA
Leakage current	Power-down mode.	–	1.5	5	µA
Line regulation	V_{in} from (V_o + 0.3V) to 4.8V, maximum load.	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, V_{in} = 3.6V.	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.3V, V_o = 2.5V, C_o = 2.2 µF, maximum load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	150	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5–240 mΩ), ±10%, 10V	0.7[b]	2.2	2.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V. Not needed if sharing VBAT 4.7 µF capacitor with SR_VDDBATP5V.	–	4.7	–	µF

a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

CLDO

Table 47: CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.3	–	420	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	% ±2 with trim
Quiescent current	No load	–	36	51	µA
	420 mA load	–	2.65	2.71	mA
Line Regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 420 mA	–	0.025	0.045	mV/mA
Leakage Current	Power down	–	–	20	µA
	Bypass mode	–	1	3	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF	20	–	–	dB
Start-up Time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO Turn-on Time	LDO turn-on time when rest of the chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	2.2[a]	4.7	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part–to–part tolerance, DC–bias, temperature, and aging.

LNLDO

Table 48: LNLDO Specifications

Specification	*Notes*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage, Vin	Min = $1.2V_o$ + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	–	0.1	–	150	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout Voltage	At maximum load	–	–	150	mV
Output Voltage DC Accuracy	Includes line/load regulation	–4	–	+4	% ±2 with trim
Quiescent current	No load	–	44	–	µA
	Max load	–	970	990	µA
Line Regulation	V_{in} from (V_o + 0.1V) to 1.5V, max load	–	–	5.5	mV/V
Load Regulation	Load from 1 mA to 150 mA	–	0.025	0.045	mV/mA
Leakage Current	Power-down	–	–	10	µA
Output Noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO Turn-on Time	LDO turn-on time when rest of chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[a]	2.2	4.7	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part–to–part tolerance, DC–bias, temperature, and aging.

HLDO

Table 49: HLDO Specifications

Parameter	*Conditions*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage, V_{in}	Min V_{in} = V_o + 0.15V = 1.35V (for V_o = 1.2V) dropout voltage requirement must be met under max load.	1.3	1.35	1.5	V
Output current	Peak load = 80 mA, average = 35 mA	0.1	–	100	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4 ±2 with trim	%
Quiescent current	No-load	–	11	13	µA
	100 mA load		633	650	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V; 100 mA load	–	–	5	mV/V
Load regulation	load from 1 mA to 100 mA; V_{in} ≥ (V_o + 0.15V)	–	0.025	0.045	mV/mA
Leakage current	Power-down mode	–	5	20	µA
	Bypass mode		0.2	1.5	µA
PSRR	At 1 kHz, V_{in} ≥ 1.35V, C_o= 1 µF	20	–	–	dB
Start-up time of PMU	V_{IO} up and steady. Time from REG_ON rise edge to CLDO reaching 99% of V_o.	–	530	700	µs
LDO turn-on time	LDO turn-on time when rest of the chip is up.	–	140	180	µs
External output capacitor, C_o	0201 size capacitor 6.3V.	0.5[a]	1	–	µF
External input capacitor	Only use an external input capacitor at VDD_LDO pin if it is not supplied from CBUCK output.	–	1	–	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

MEMLPLDO

Table 50: MEMLPLDO Specifications

Parameter	*Conditions*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage, V_{in}	Taken from VDDIO input	1.6	1.8	3.64	V
Nominal output voltage, V_o	Default = 0.9V	0.825	0.9	1.237	V
Output voltage DC accuracy	including line/load regulation.	–5	–	+5	%
Output current	–	0	–	10	mA
Quiescent current	No load includes LP-B Gap. Excludes other PMU peripherals.	–	3	–	µA
Leakage current	Power-down mode. At junction temperature 85°C.	–	–	1	µA
LDO turn-on time	LDO turn-on time when rest of the chip is up.	–	18	40	us
External output capacitor, C_o	–	–	0.47	–	µF
External input capacitor	VDDIO input pin capacitor.	0.06	0.22	0.47	µF

Section 17: System Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.
Unless otherwise stated, these values apply for the conditions specified in Table 31: “Recommended Operating Conditions and DC Characteristics,” on page 129.

WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 51.

All values in Table 51 are with the Bluetooth core in reset (that is, Bluetooth is OFF).

Table 51: Typical WLAN Power Consumption

Mode	*Bandwidth (MHz)*	*Band (GHz)*	*V_{bat} = 3.6V mA*	*V_{io} = 1.8V µA[a]*
Sleep Modes				
OFF[b]	–	–	TBD	TBD
Sleep[c]	–	–	0.007	250
IEEE power save, DTIM 1 1 RX core[d]	20	2.4	1.7	TBD
IEEE power save, DTIM 3 1 RX core[d]	20	2.4	0.510	TBD
IEEE power save, DTIM 1 1 RX core[d]	20	5	1.150	TBD
IEEE power save, DTIM 3 1 RX core[d]	20	5	0.430	TBD
IEEE power save, DTIM 1 1 RX core[d]	40	5	1.375	TBD
IEEE power save, DTIM 3 1 RX core[d]	40	5	0.514	TBD
IEEE power save, DTIM 1 1 RX core[d]	80	5	1.700	TBD
IEEE power save, DTIM 3 1 RX core[d]	80	5	0.753	TBD
Active Modes				
Transmit				
CCK 1 chain[e]	20	2.4	423	TBD
MCS8, Nss 1, HT20, SGI[f, g, h]	20	2.4	324	TBD
MCS7, SGI[f, g, i]	20	5	312	TBD
MCS15, SGI[f, g, i]	20	5	543	TBD
MCS7[f, g, i]	40	5	343	TBD
MCS9, Nss 1, SGI[f, g, j]	40	5	316	TBD

Table 51: Typical WLAN Power Consumption (Cont.)

Mode	*Bandwidth (MHz)*	*Band (GHz)*	*V_{bat} = 3.6V mA*	*V_{io} = 1.8V µA[a]*
MCS9, Nss 1, SGI[f, g, j]	80	5	338	TBD
Receive				
1 Mbps, 1 RX core	20	2.4	69.5	TBD
MCS7, HT20 1 RX core[k]	20	2.4	70	TBD
MCS15, HT20[k]	20	2.4	115	TBD
CRS 1 RX core[l]	20	2.4	60	TBD
Receive MCS7, SGI 1 RX core[k]	20	5	93	TBD
Receiver MCS15, SGI[k]	20	5	123	TBD
CRS 1 RX core[l]	20	5	77	TBD
Receive MCS 7, SGI 1 RX core[k]	40	5	115	TBD
Receive MCS 15, SGI[k]	40	5	140	TBD
CRS 1 RX core[l]	40	5	87	TBD
Receive MCS9, Nss 1, SGI[k]	80	5	155	TBD
CRS 1 RX core[l]	80	5	113	TBD

a. Specified with all pins idle (not switching) and not driving any loads.
b. WL_REG_ON, BT_REG_ON low, no VDDIO.
c. Idle, not associated, or inter-beacon.
d. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over three DTIM intervals.
e. Output power per core at RF port = 21 dBm.
f. Duty cycle is 100%.
g. Measured using packet engine test mode.
h. Output power per core at RF port = 17 dBm.
i. Output power per core at RF port = 17.5 dBm.
j. Output power per core at RF port = 14 dBm.
k. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
l. Carrier sense (CCA) when no carrier is present.

Bluetooth Current Consumption

The Bluetooth and BLE current consumption measurements are shown in Table 52.

Note:

- The WLAN core is in reset (WL_REG_ON = low) for all measurements provided in Table 52.
- The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm.

Table 52: Bluetooth and BLE Current Consumption

Operating Mode	*VBAT (VBAT = 3.6V) Typical*	*VDDIO (VDDIO = 1.8V) Typical*	*Units*
Sleep	8	185	µA
Standard 1.28s inquiry scan	273	187	µA
500 ms sniff master	214	220	µA
DM1/DH1	25.17	0.018	mA
DM3/DH3	28	0.031	mA
DM5/DH5	28.7	0.034	mA
3DH5/3DH1 master	24.8	0.072	mA
SCO HV3 master	11.5	0.055	mA
BLE scan	170	190	µA
BLE adv. unconnectable 1 sec	85	190	µA
BLE connected 1 sec	101	189	µA

Section 18: Interface Timing and AC Characteristics

SDIO Timing

SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 34 and Table 53.

Figure 34: SDIO Bus Timing (Default Mode)

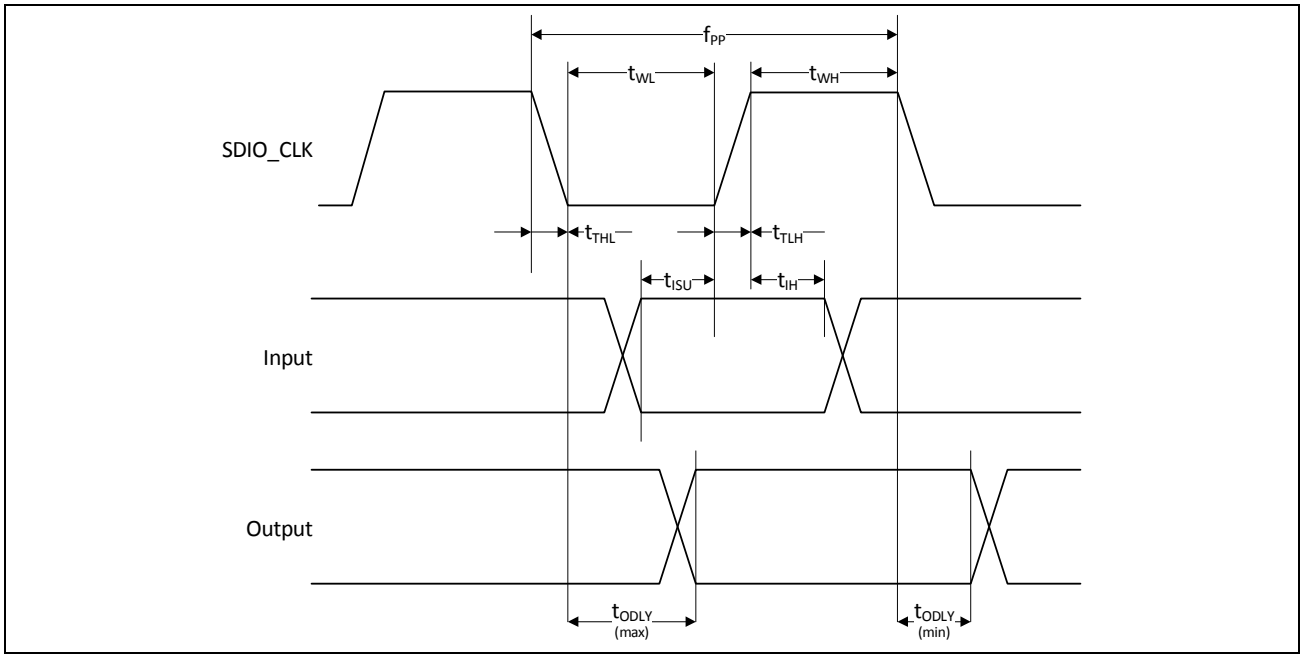


Table 53: SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns

Table 53: SDIO Bus Timing[a] Parameters (Default Mode) (Cont.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 35 and Table 54.

Figure 35: SDIO Bus Timing (High-Speed Mode)

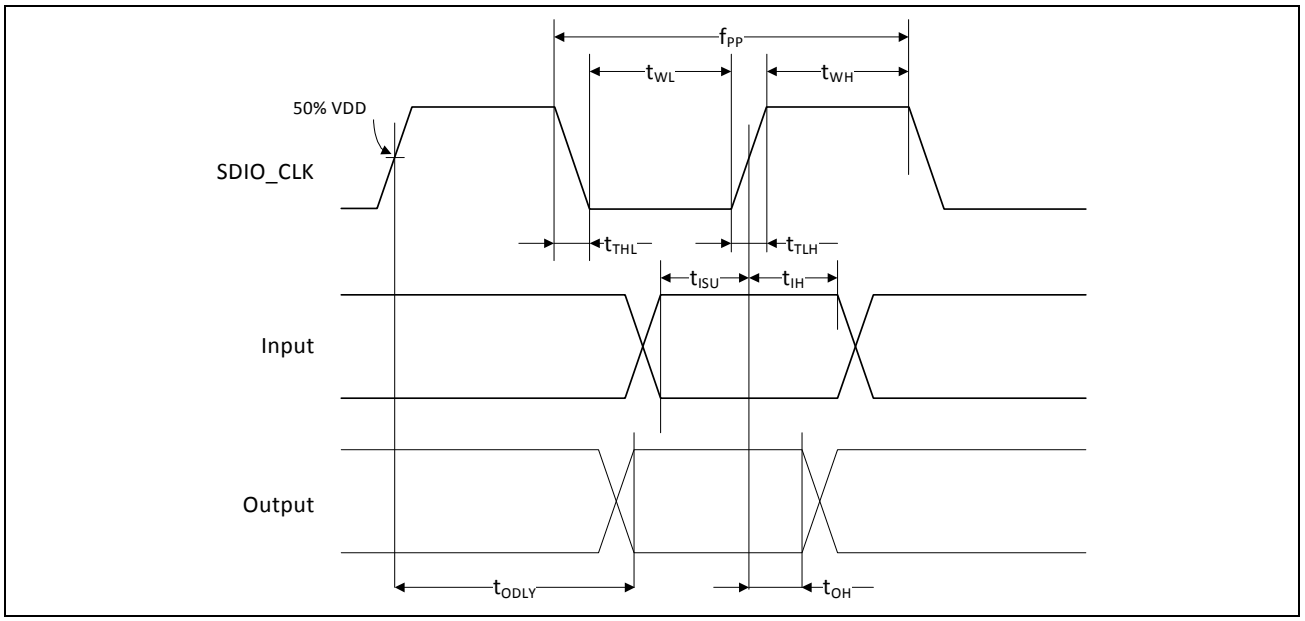


Table 54: SDIO Bus Timing[a] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

SDIO Bus Timing Specifications in SDR Modes

Clock Timing

Figure 36: SDIO Clock Timing (SDR Modes)

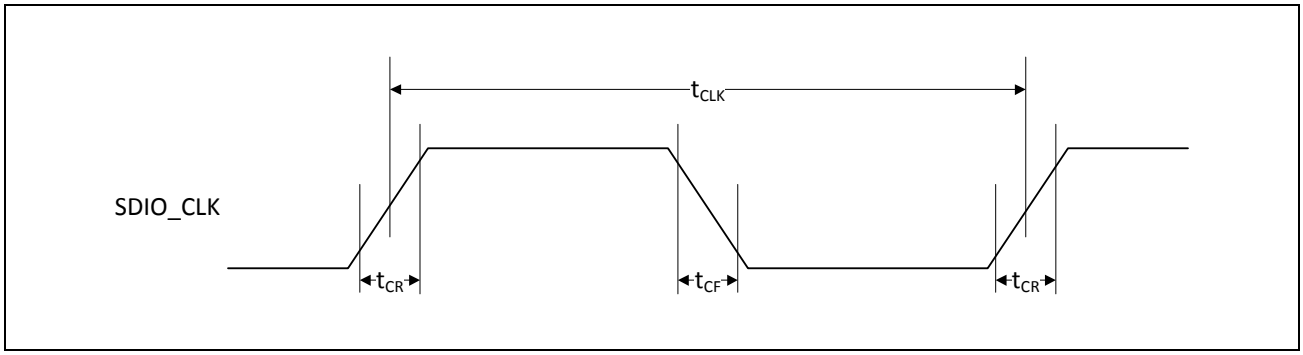


Table 55: SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30	70	%	–

Device Input Timing

Figure 37: SDIO Bus Input Timing (SDR Modes)

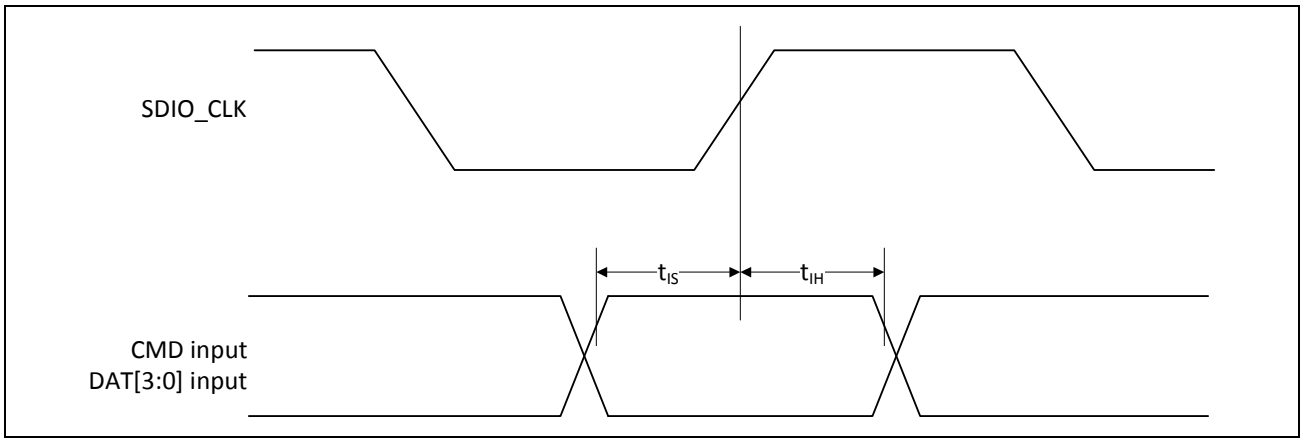


Table 56: SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Device Output Timing

Figure 38: SDIO Bus Output Timing (SDR Modes up to 100 MHz)

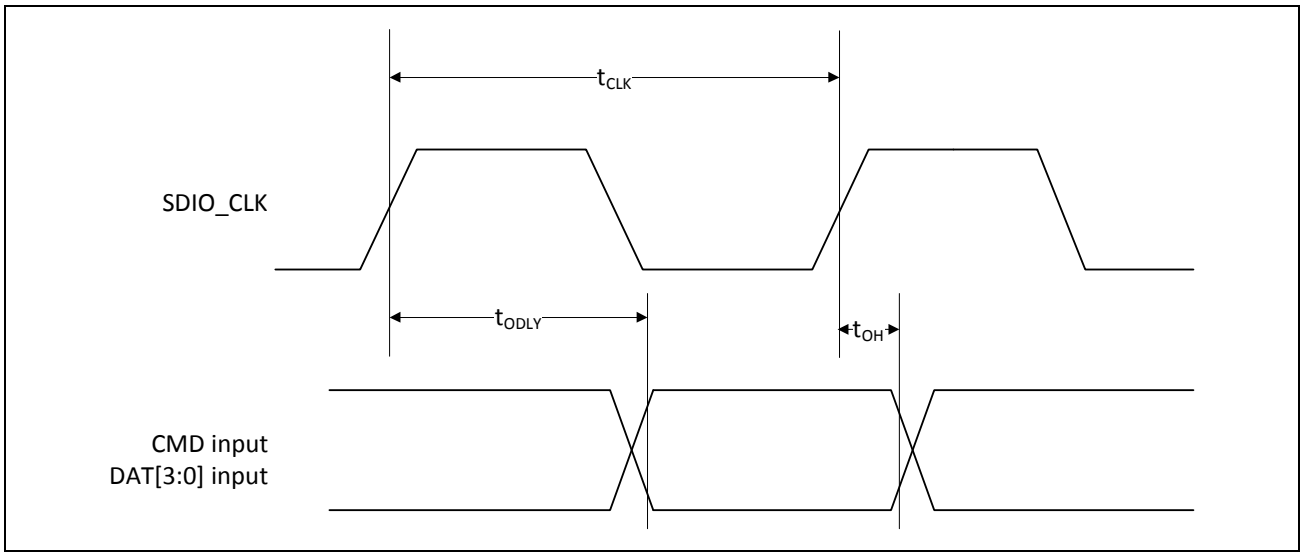


Table 57: SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

Figure 39: SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

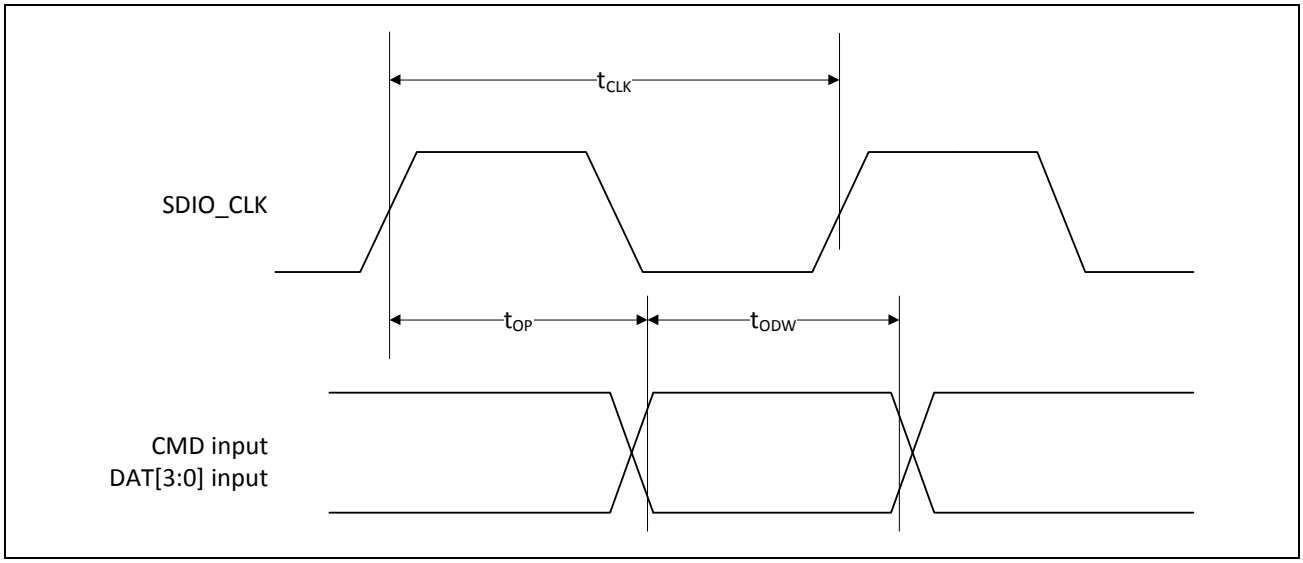
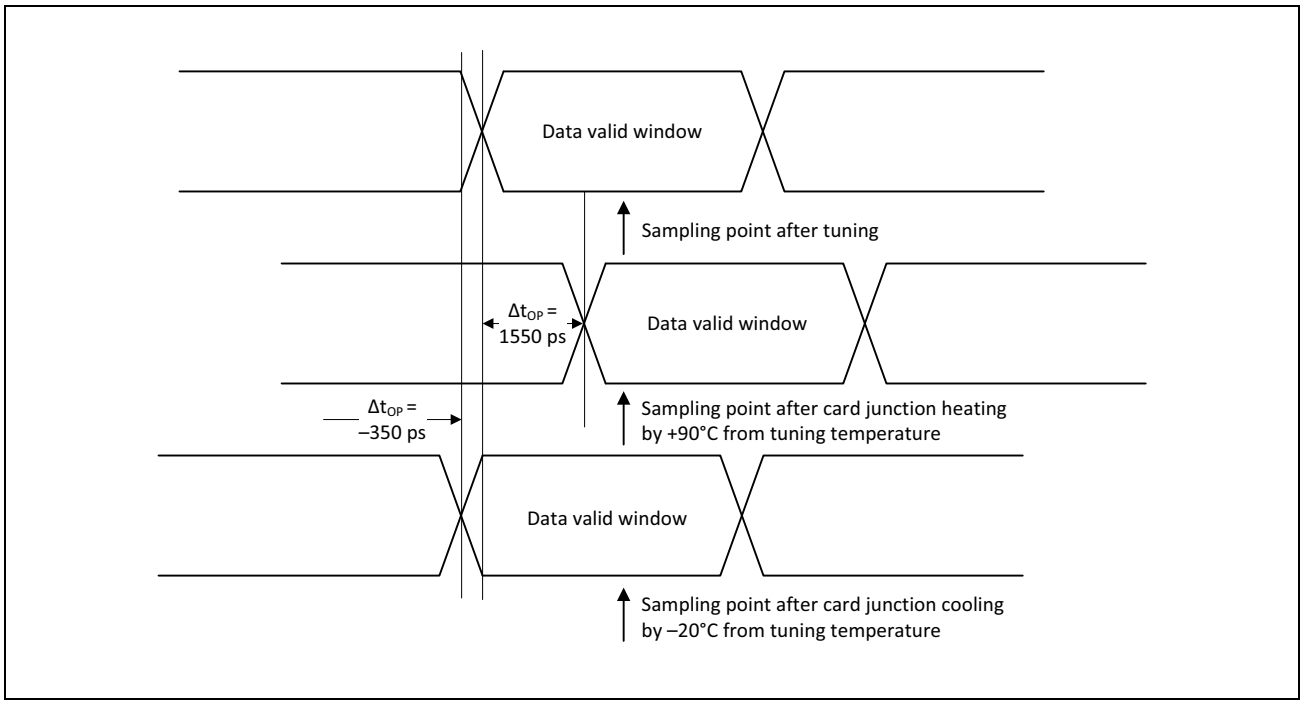


Table 58: SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20 to +125 degrees during operation

Figure 40: Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)



SDIO Bus Timing Specifications in DDR50 Mode

Figure 41: SDIO Clock Timing (DDR50 Mode)

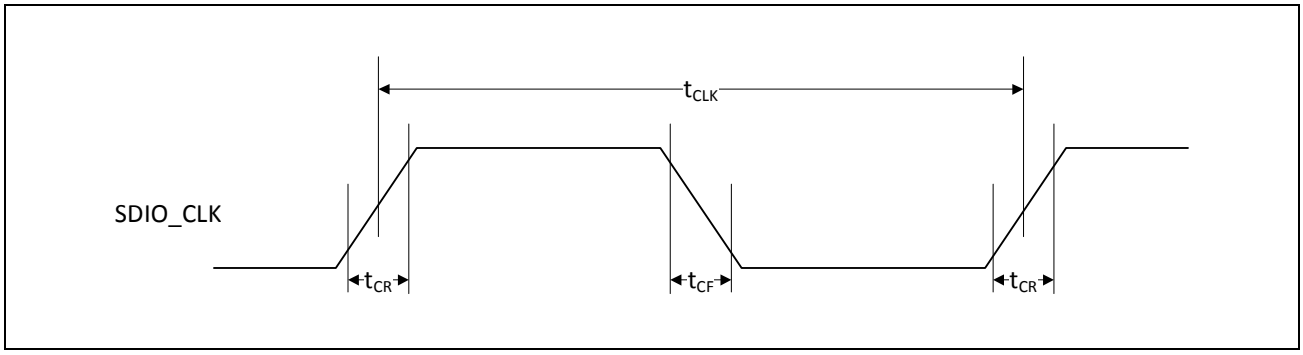


Table 59: SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @ 50 MHz, C_{CARD} = 10 pF
Clock duty	–	45	55	%	–

Data Timing, DDR50 Mode

Figure 42: SDIO Data Timing (DDR50 Mode)

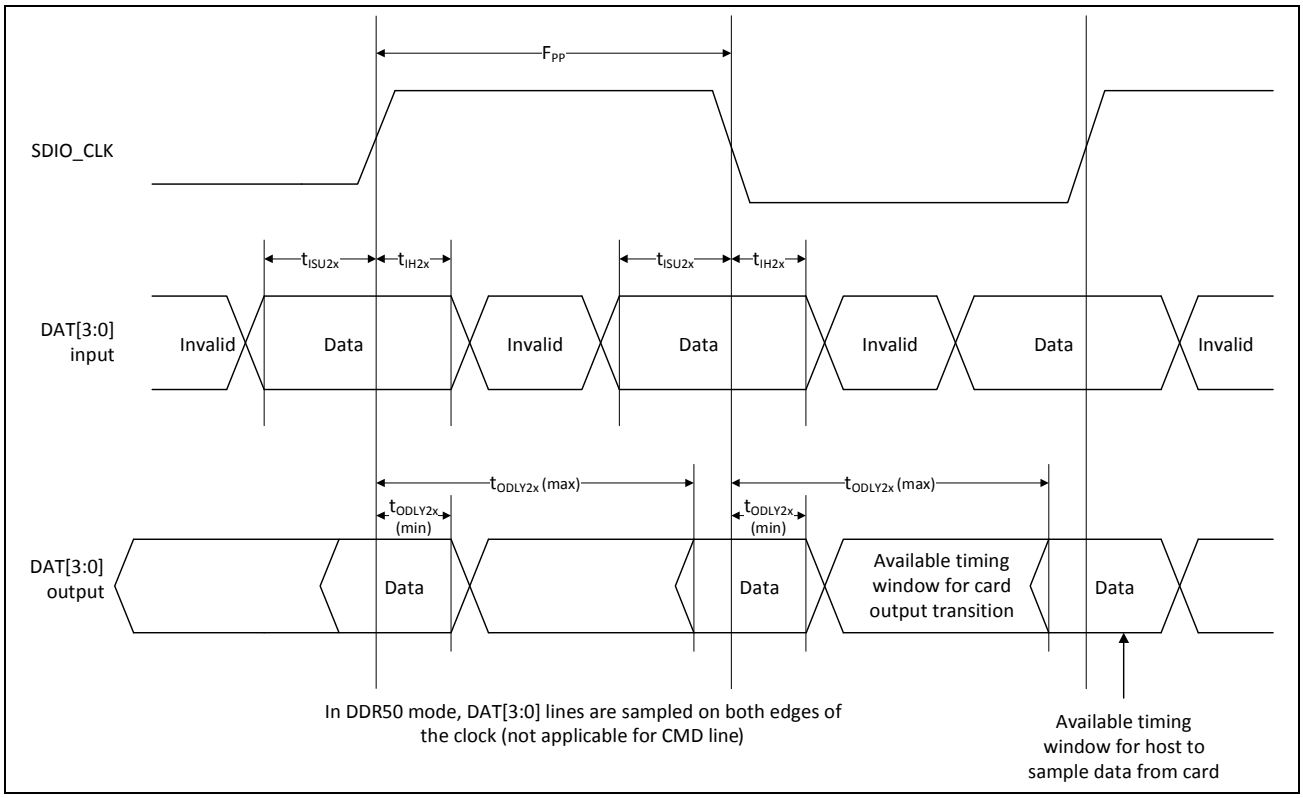


Table 60: SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

PCI Express Interface Parameters

Table 61: PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General[a]						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock peak-to-peak differential[b]	Vref	LVPECL, AC coupled	0.95	–	–	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI

Table 61: PCI Express Interface Parameters (Cont.)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20	mV
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	–	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

a. For out-of-band PCIe signal specification, refer to Table 31: “Recommended Operating Conditions and DC Characteristics,” on page 129.
b. The reference clock inputs comply with the requirements of the *PCI Express CEM v2.0 Specification*.

JTAG Timing

Table 62: JTAG Timing Characteristics

Signal Name	*Period*	*Output Maximum*	*Output Minimum*	*Setup*	*Hold*
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

Section 19: Power-Up Sequence and Timing

Sequencing of Reset and Regulator Control Signals

The BCM4359 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 43, Figure 44 on page 179, and Figure 45 and Figure 46 on page 180). The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

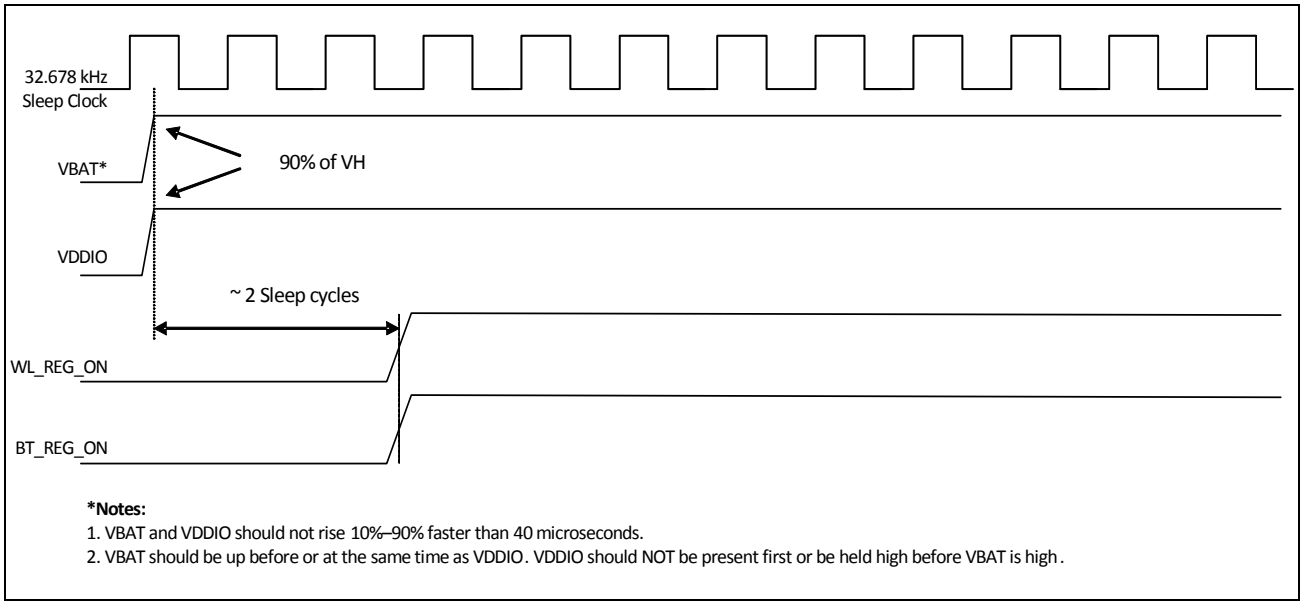
- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM4359 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal BCM4359 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note:

- The BCM4359 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO and PCIe accesses.
- VBAT, VDDIO, WPT_1P8, and WPT_3P3 should not rise 10%–90% faster than 40 microseconds.

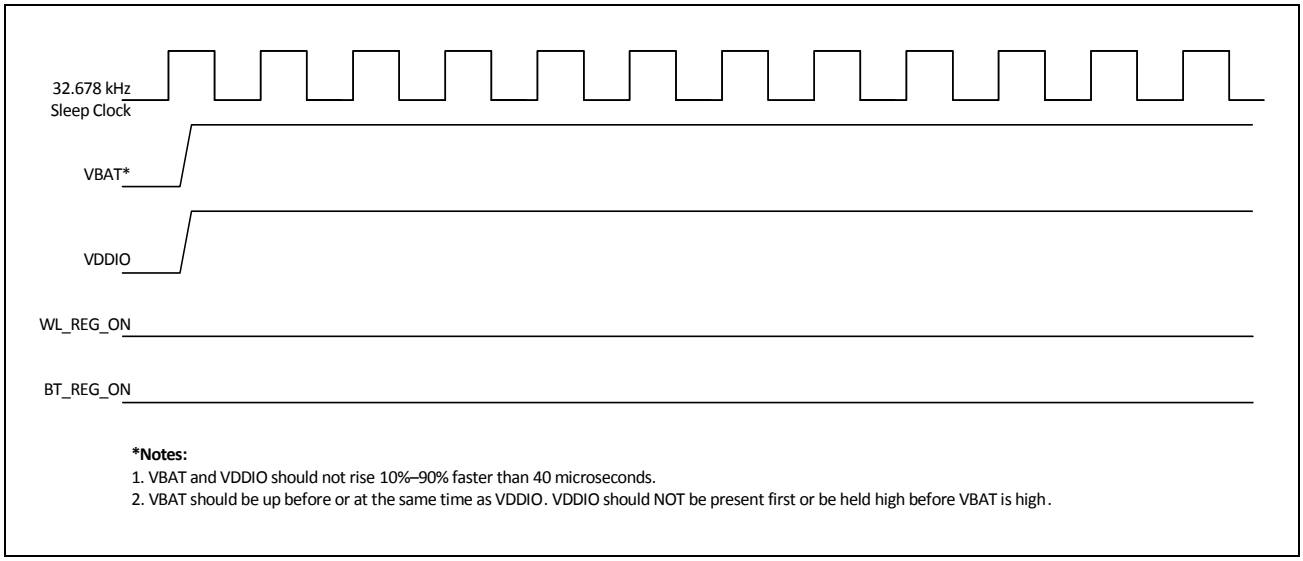
Control Signal Timing Diagrams

Figure 43: WLAN = ON, Bluetooth = ON



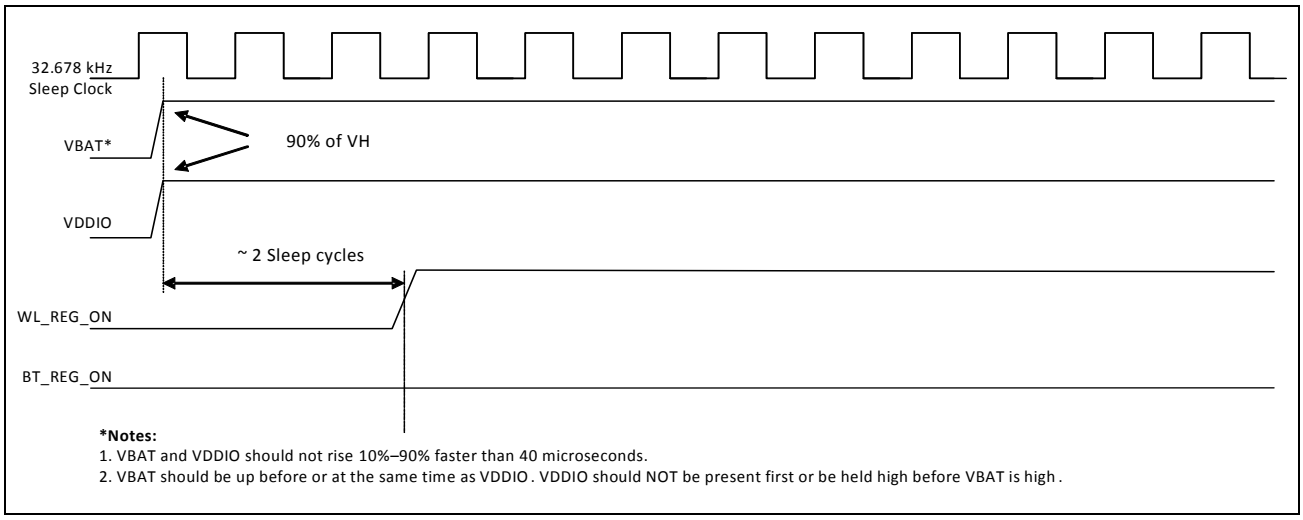
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 44: WLAN = OFF, Bluetooth = OFF



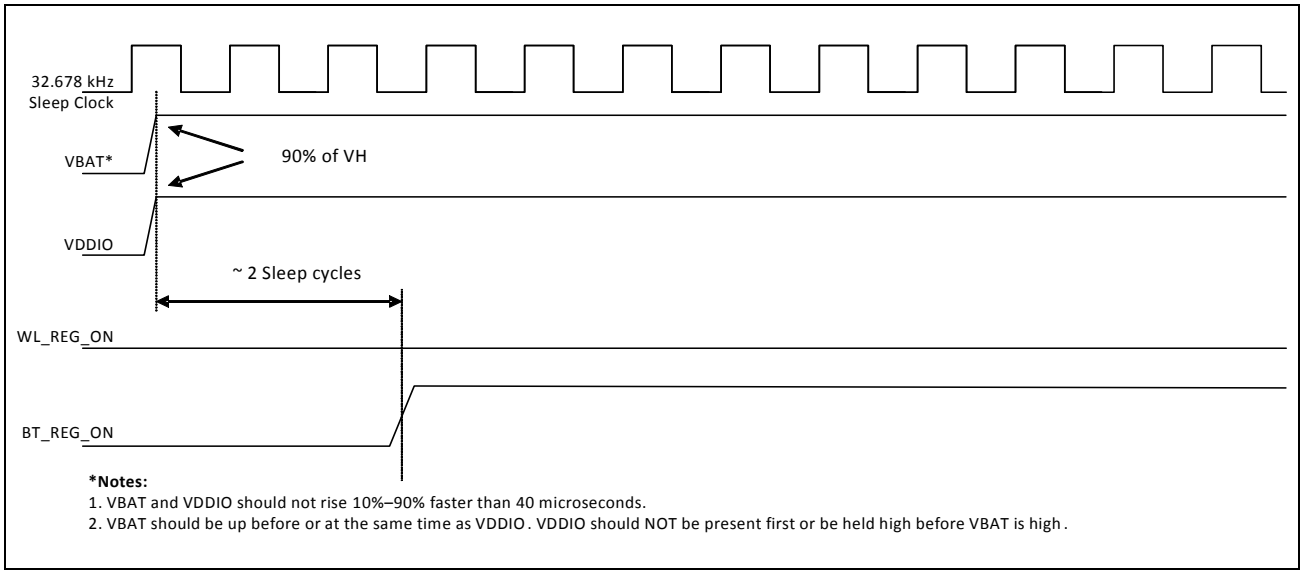
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 45: WLAN = ON, Bluetooth = OFF



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

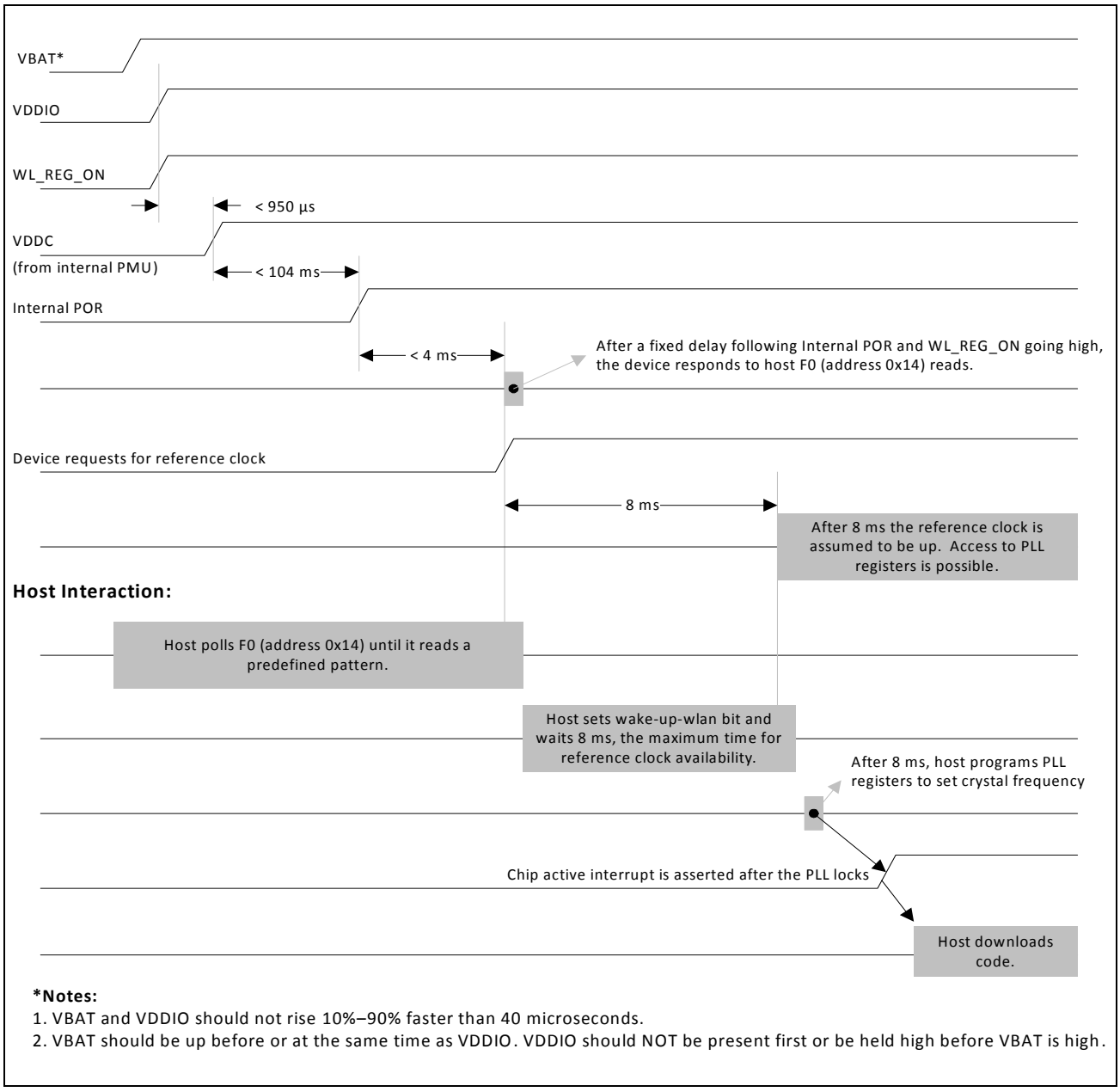
Figure 46: WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

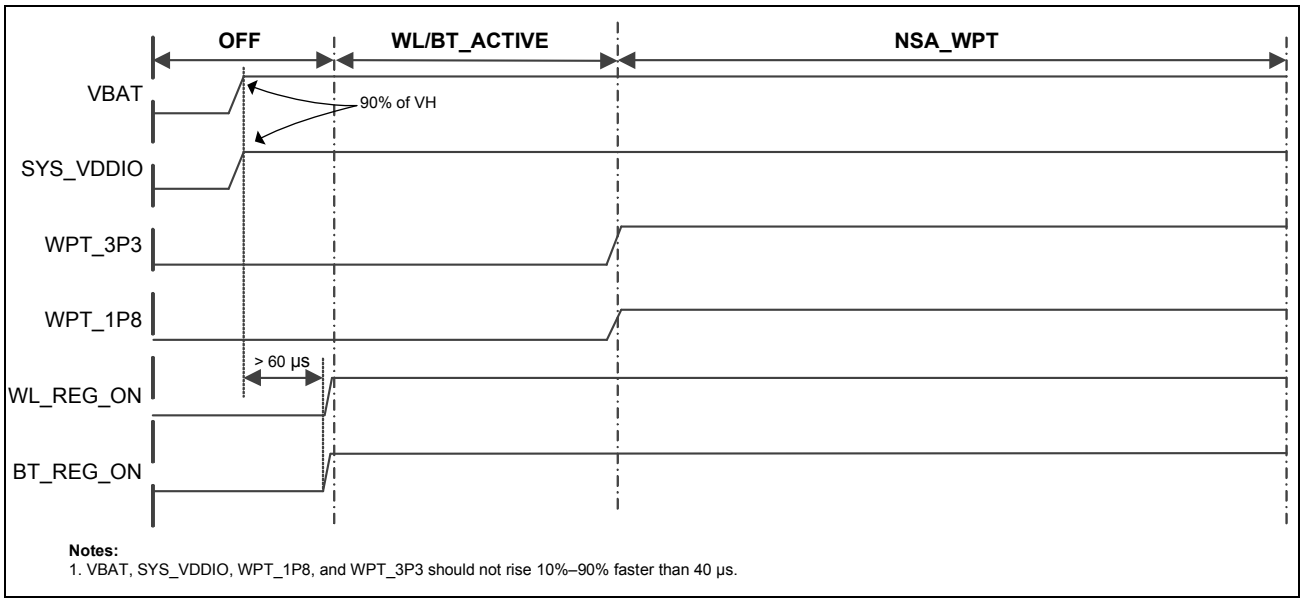
Figure 47 shows the WLAN boot-up sequence from power-up to firmware download.

Figure 47: WLAN Boot-Up Sequence



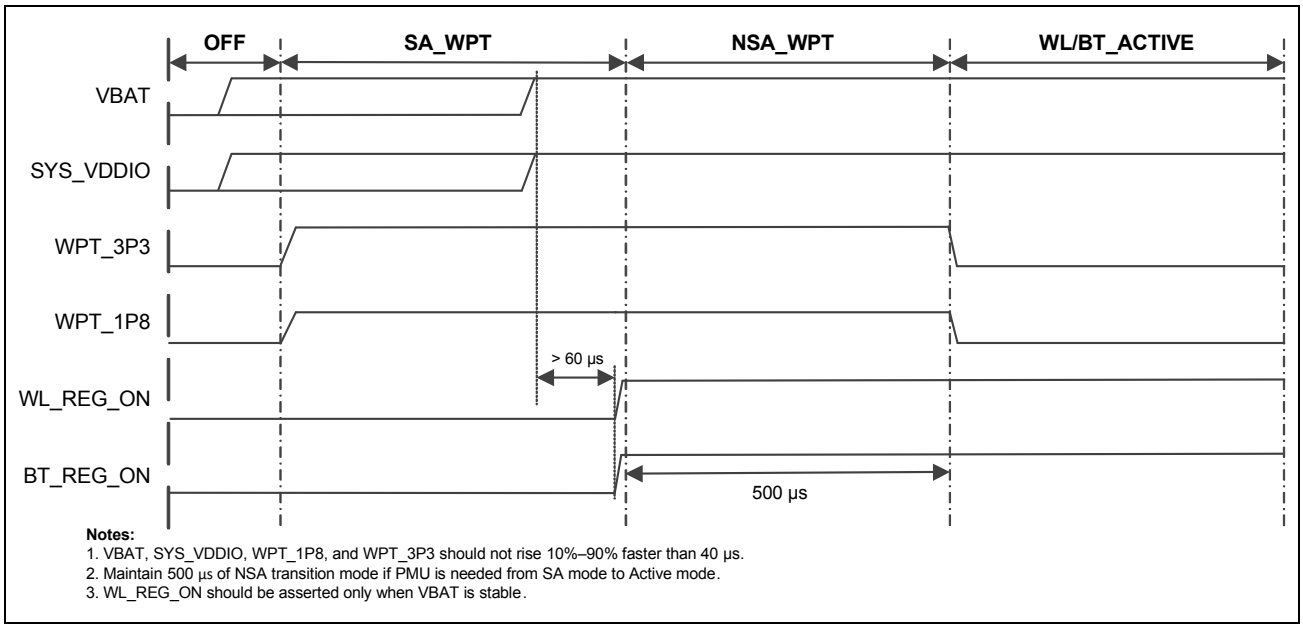
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 48: VBAT to WPT



Notes:
1. VBAT, SYS_VDDIO, WPT_1P8, and WPT_3P3 should not rise 10%–90% faster than 40 µs.

Figure 49: WPT to VBAT



Notes:
1. VBAT, SYS_VDDIO, WPT_1P8, and WPT_3P3 should not rise 10%–90% faster than 40 µs.
2. Maintain 500 µs of NSA transition mode if PMU is needed from SA mode to Active mode.
3. WL_REG_ON should be asserted only when VBAT is stable.

Section 20: Package Information

Package Thermal Characteristics

The information in Table 63 is based on the following conditions:

- No heat sink, T_A = 70°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 101.6 mm × 1.6 mm) and P = 2.65W continuous dissipation.
- Absolute junction temperature limits are maintained through active thermal monitoring or turning off one of the TX chains, or both.

Table 63: WLCSP Package Thermal Characteristics

Characteristic	*WLCSP*	*WLBGA*
θ_{JA} (°C/W) (value in still air)	39.62	39.1
θ_{JB} (°C/W)	4.56	4.51
θ_{JC} (°C/W)	1.65	1.24
Ψ_{JT} (°C/W)	7.23	6.53
Ψ_{JB} (°C/W)	12.01	11.6
Maximum Junction Temperature T_j (°C)	125	125
Maximum Power Dissipation (W)	2.65	2.65

Junction Temperature Estimation and PSI_{JT} Versus $Theta_{JC}$

The package thermal characterization parameter PSI_{JT} (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) than using the junction-to-case thermal resistance parameter $Theta_{JC}$ (θ_{JC}). The reason for this is that θ_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

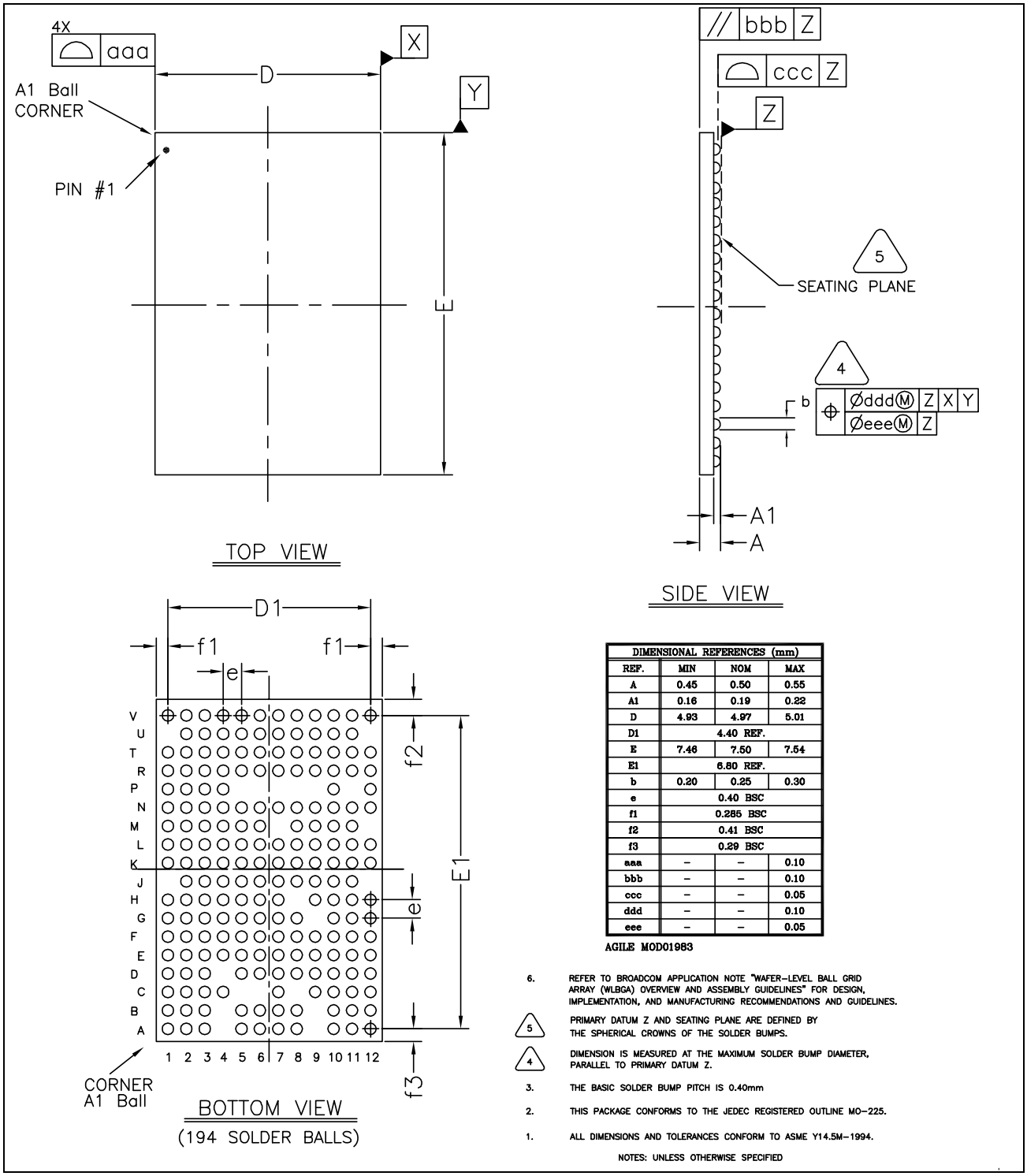
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

Environmental Characteristics

For environmental characteristics data, see Table 30: “Environmental Ratings,” on page 128.

Section 21: Mechanical Information

Figure 50: BCM4359 WLBGA Package Dimensions



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.16	0.19	0.22
D	4.93	4.97	5.01
D1		4.40 REF.	
E	7.46	7.50	7.54
E1		6.80 REF.	
b	0.20	0.25	0.30
e		0.40 BSC	
f1		0.285 BSC	
f2		0.41 BSC	
f3		0.29 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

AGILE MOD01983

6. REFER TO BROADCOM APPLICATION NOTE "WAFER-LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 51: WLBGA Keep-Out Areas for PCB Layout (Top View, Balls Facing Down)

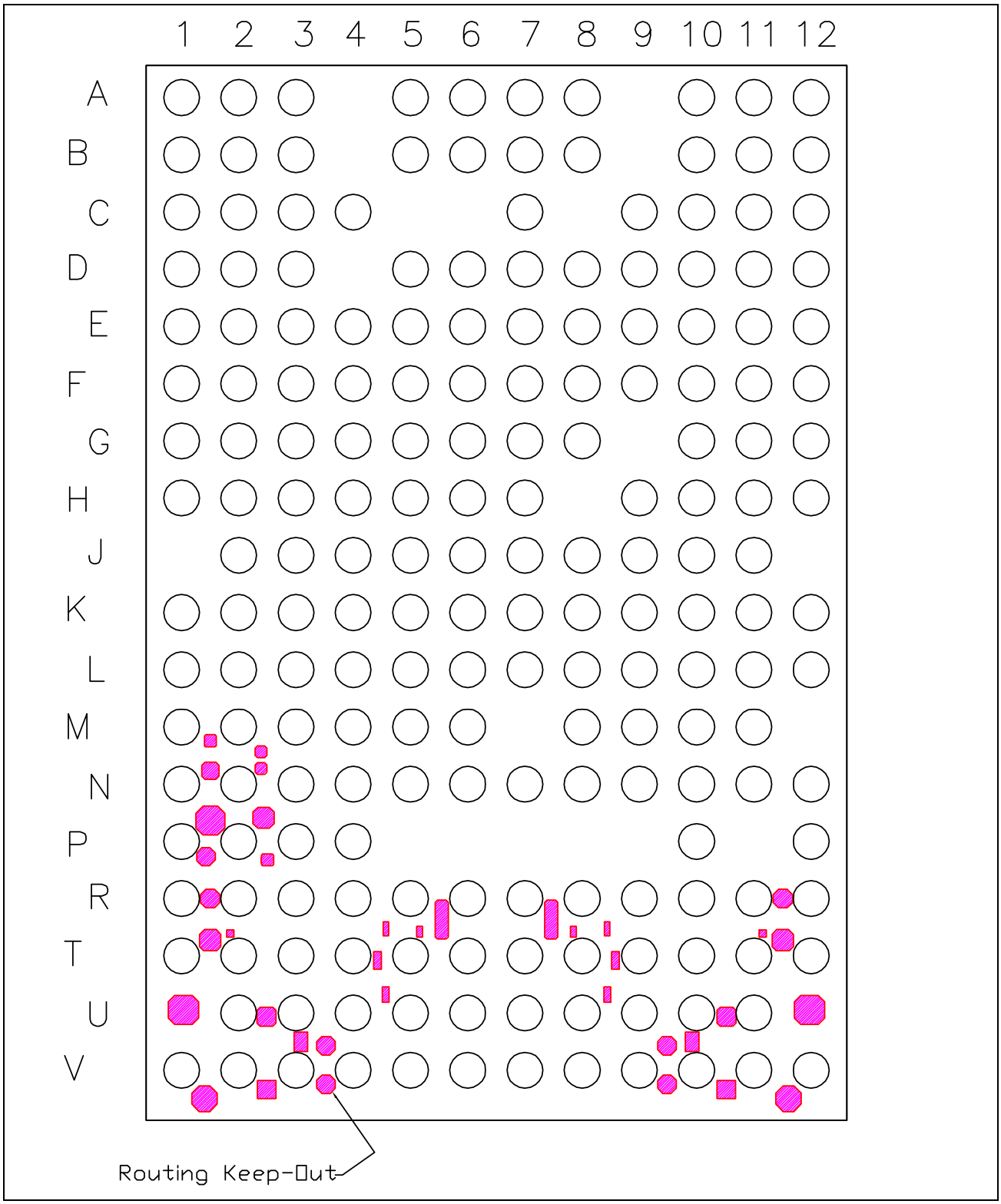
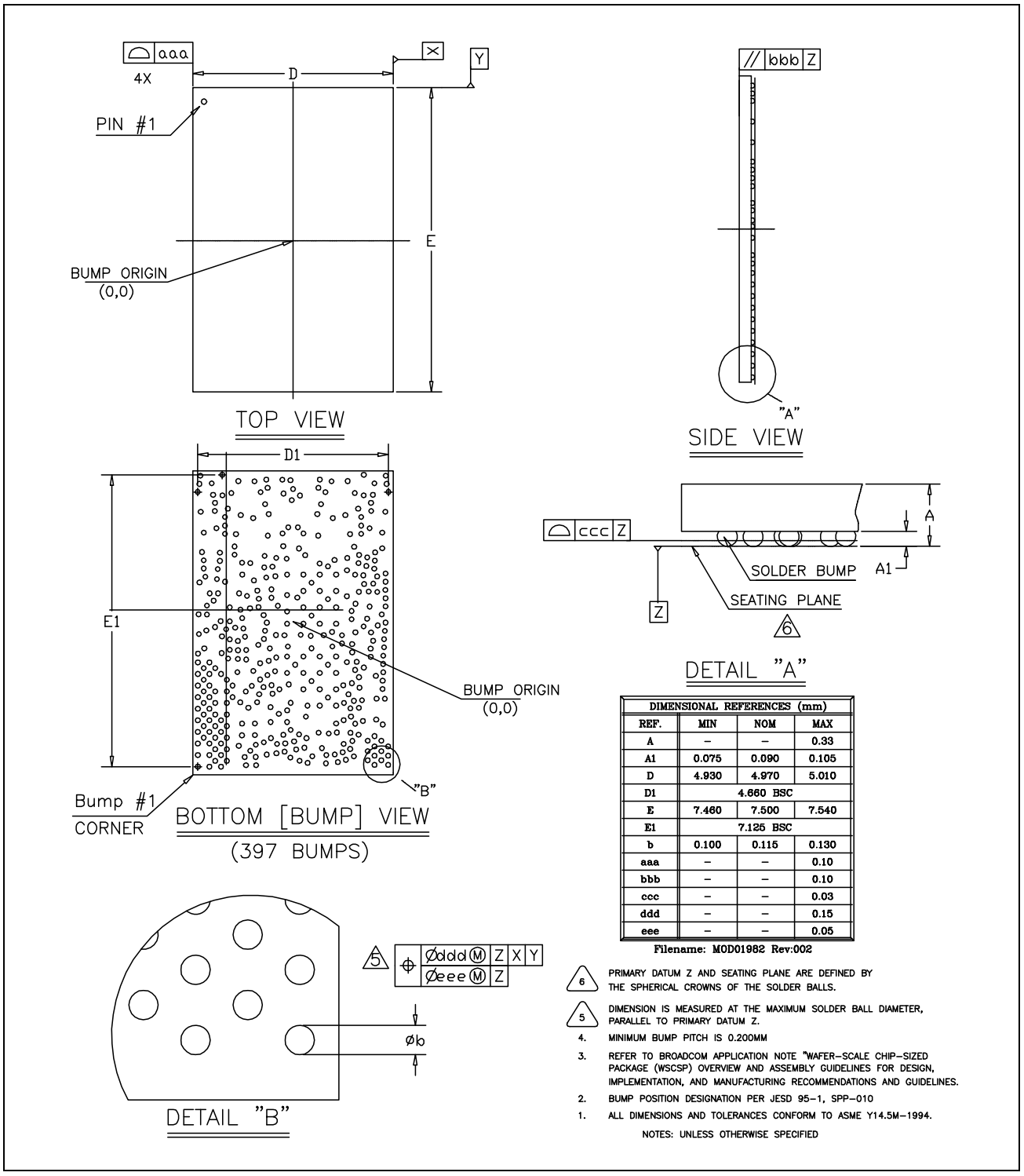


Figure 52: BCM4359 WLCSP Package Dimensions



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.33
A1	0.075	0.090	0.105
D	4.930	4.970	5.010
D1		4.660 BSC	
E	7.460	7.500	7.540
E1		7.125 BSC	
b	0.100	0.115	0.130
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

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6 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

4. MINIMUM BUMP PITCH IS 0.200MM

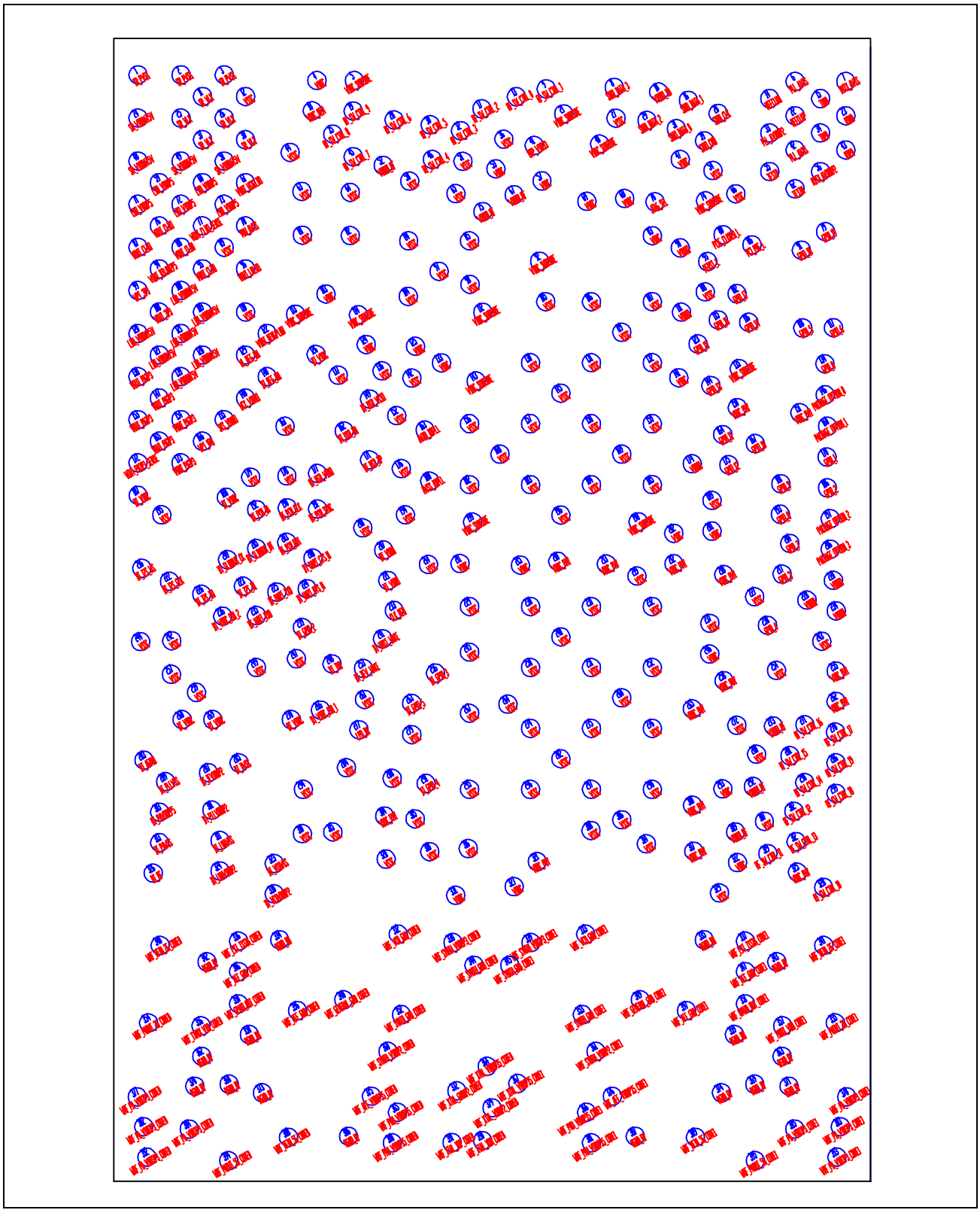
3. REFER TO BROADCOM APPLICATION NOTE "WAFER–SCALE CHIP–SIZED PACKAGE (WSCSP) OVERVIEW AND ASSEMBLY GUIDELINES FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

2. BUMP POSITION DESIGNATION PER JESD 95–1, SPP–010

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 53: WLCSP Keep-Out Areas for PCB Layout (Top View, Balls Facing Down)



Section 22: Ordering Information

Table 64: Ordering Information

Part Number	*Package*	*Description*	*Ambient Operating Temperature*
BCM4359X1KWBG	397-bump WLCSP (4.97 mm × 7.50 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN and Bluetooth 4.2	–30°C to +85°C (–22°F to 185°F)
BCM4359X1KUBG	194-ball WLBGA (4.97 mm × 7.50 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN and Bluetooth 4.2	–30°C to +85°C (–22°F to 185°F)

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