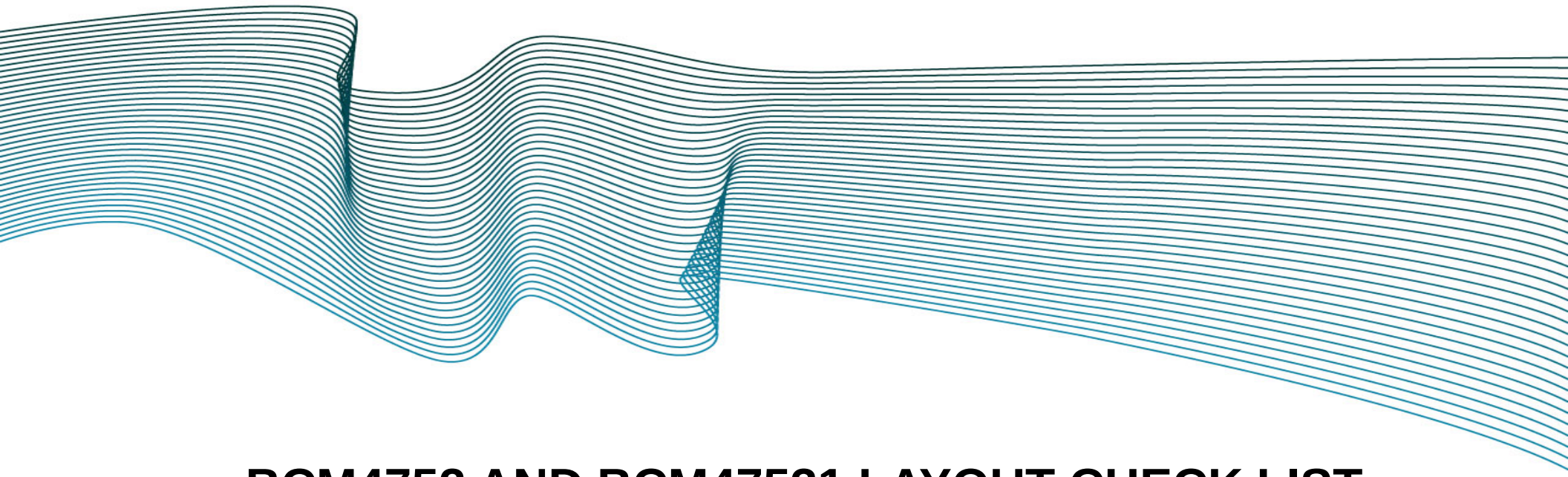


BCM4752 AND BCM47531 LAYOUT CHECK LIST

CHECK LIST – ANTENNA/RF PART

- Antenna expect to be high efficiency(enough ground keep out under antenna, no shielding for antenna such as metal, and hand will not cover antenna when using the device) , efficiency more than 40% and gain pattern face to sky.
- No noisy components near GPS antenna(camera and its FPC, WiFi/modem antenna, LCD FPC, CPU,Memory, DC/DC inductor)
- The RF trace should be short, no stub. There is ground keep out under RF trace to make its width>10mils(it can only use this ground keep out between antenna and external LNA for external LNA design), the RF trace impedance should be 50ohm, make sure there are enough ground vias along RF trace at both sides
- Put pre-LNA SAW and external LNA near the antenna, put after-LNA SAW close to GNSS chip when GNSS chip is away from antenna,
- External LNA input/output matching circuits near the pin.
- BCM4752/BCM47531 matching circuits near the pin
- Keep all digital traces away from GNSS chip's RF input circuits

CHECK LIST - POWER PART(INPUT)

- Put 100nF near VDD_IO pin and 4mils width trace is fine for VDD_IO pin.
- Put 1uF capacitor near VDD_PMU_IN(BCM47531)/VDD_3P3_IN(BCM4752) and 8mils width trace is fine for this pin
- Put 1uF capacitor near VDD_AUX_IN and 4mils width trace is fine for this pin
- TCXO bypass capacitor should be put near TCXO VCC pin
- External LNA bypass capacitor should be put near external LNA VCC pin

CHECK LIST - POWER PART(OUTPUT)

- Power supply bypass capacitor should be near the pin.
- 47pF capacitor near pin VDD_GPS_LNA/VDD_GPS_IF, connect VDD_GPS_LNA and VDD_GPS_IF to 47pF capacitor using star connection with 4mils width trace
- 1uF capacitor close to VDD1P2_GRF and 4mils width trace is fine for this power supply. VDD1P2_GRF first route to 1uF capacitor and then route to 47pF capacitor.
- Route traces of net VDD1P2_GRF/VDD_GPS_IF/VDD_GPS_LNA with ground on all sides since it powers RF part. Don't route traces of this net in parallel with other traces if meet ground on all sides requirements
- Put 1uF capacitor close to VDD1P1_CORE/VDD_CORE, connect these two pins to 1uF capacitor using star connection with 8mils width trace
- Put 1uF capacitor close to VDD1P8_AUX, 4mils is fine for this net traces. All the traces of this net should be routed with ground on all sides since it powers external LNA and tcxo. VDD1P8_AUX first route to 1uF capacitor and then route to external LNA and tcxo.
- Put capacitor near REF_CAP using 6mils width trace
- VSS_GPS_LNA connect to ground separately.

CHECK LIST – TCXO PART(I)

- Longer distance between heat source and tcxo is the gold key to improve the tcxo clock drift. Heat source affection is similar when it put on the same side or opposite side of tcxo.

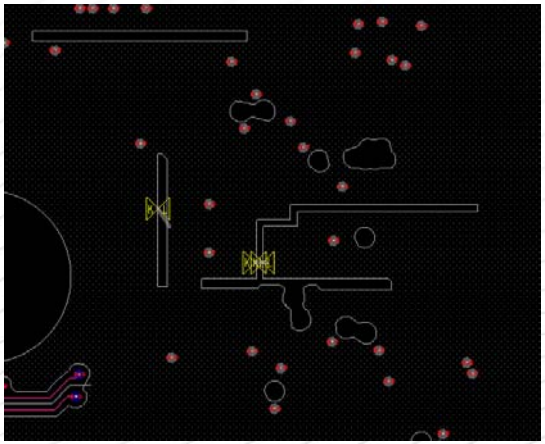
- TCXO output pin should not be too close to BCM4752 and tcxo should not be put at the opposite position of BCM4752 since BCM4752 also can act as heat source. 2mm length trace looks fine.

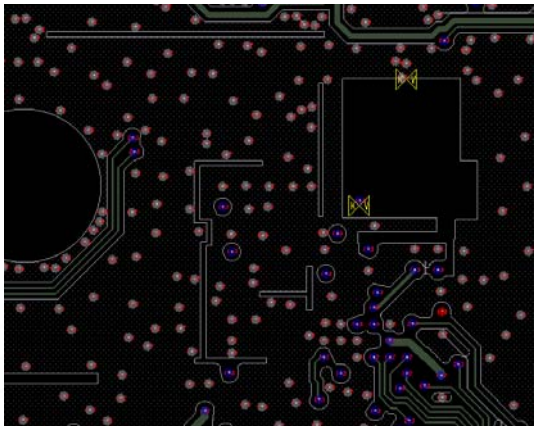
- TCXO ground pin need to connect main ground using long and thin trace(around 3mils width) to reduce thermal affection, more than 4mm length looks fine . The connection point of tcxo ground trace and main ground should be away from heat source. Rotate TCXO and select the position which ground pins are more away from heat source

TCXO recommend distance away from heat source	
WiFi	15mm
AP/CPU	20mm
Modem transceiver/PA	20mm

CHECK LIST – TCXO PART(II)

- Recommend to cut all ground planes underneath tcxo to reduce the thermal affection. Cut as many as possible if can't cut all the planes, at least cut 6 layers when using 10 layers PCB.
- Ground gap between tcxo and heat source on all ground planes will greatly help if can't cut all the ground planes underneath tcxo. Especially pay attention to the heat source "main" ground plane which there're lot of ground vias between this ground plane and heat source ground pad. Heat will goes quickly from heat source ground pad to this ground plane through vias and affect tcxo clock drift. It should use ground gap on this plane to reduce the thermal affection.
- Recommend route VCC/GND/OUTPUT traces on top/bottom layer to easier debug
- Reduce the ground vias around tcxo since these ground vias act as thermal vias





CHECK LIST – DIGITAL /CLOCK PART

- RTC clock at pin clk32 route in inner layer to avoid RFI to GNSS. This is digital signal and no need to control trace impedance
- Calibrated clock at pin GPS_CAL/GNSS_CAL route in inner layer to avoid RFI to GNSS. This is digital signal and no need to control trace impedance
- Route TCXO output clock with ground on all sides and route it in inner layer if the trace is long

CHECK LIST – EMI PART

- For display backlight DC/DC, it recommend connect to ground using single point
- Make sure there are EMI filter for camera interface to reduce risk of RFI to GPS. The camera module, related connectors and the PCB layout should be kept short and shielded; the traces should go in inner layer. The camera module should be shielded as well as it can be to reduce RFI. And also flex connected to the camera and display should be shielded on top as well as bottom
- Make sure there are EMI filter for LCD interface and LCD FPC are shielded to reduce risk of RFI to GPS
- High speed digital components and their traces should be shielded
- T-flash/SD card traces should be routed in inner layer, and T-flash/SD card need to be away from GPS antenna
- Shielding case for high speed signals should be complete with multiple ground connection points and no hole on the shielding case
- Make sure multi ground connection points between LCD back and main board to reduce noise radiated from LCD back