正基科技股份有限公司

SPECIFICATION

SPEC. NO.： _____ REV： 1.0

DATE： 10. 01. 2012

PRODUCT NAME： **AP6181**

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

AMPAK

AP6181

Wi-Fi 802.11b/g/n

SIP Module Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2012/10/01	- Initial released	Joe	1.0

Contents

1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, headsets and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

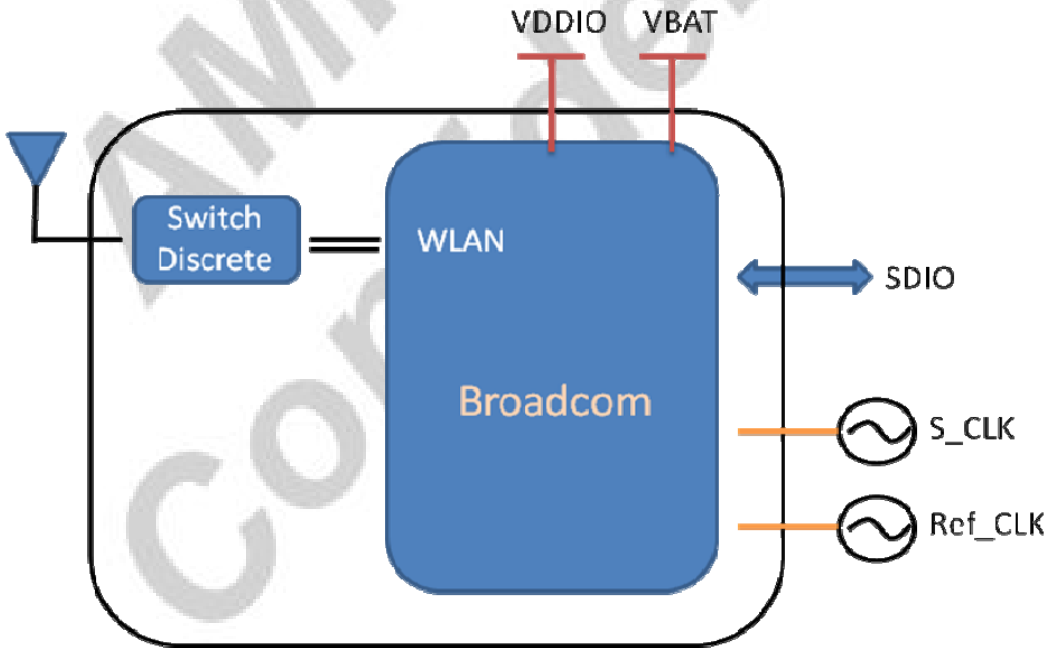
This wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi.

This compact module is a total solution for Wi-Fi technologies. The module is specifically developed for Tablet, Smart phones and Portable devices.

2. Features

- Single-band 2.4GHz IEEE 802.11b/g/n
- Supports standard interfaces SDIO v2.0(50MHz, 4-bit and 1-bit)
- Integrated ARM Cortex-M3™ CPU with on-chip memory enables running IEEE802.11 firmware that can be field-upgraded with future features.
- Security:
  i. Hardware WAPI acceleration engine
  ii. AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  iii. WPA™ – and WPA2™ - (Personal) support for powerful encryption and authentication

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 Wi-Fi RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
Model Name	AP6181
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Host Interface	SDIO
Dimension	L x W x H: 12 x 12 x 1.5 (typical) mm
Frequency Range	2.412 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
Number of Channels	11 for North America, 13 for Europe, and 14 for Japan
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 ± 1dBm, typical
	- MCS=1 PER @ -84 ± 1dBm, typical
	- MCS=2 PER @ -82 ± 1dBm, typical
	- MCS=3 PER @ -80 ± 1dBm, typical
	- MCS=4 PER @ -77 ± 1dBm, typical
	- MCS=5 PER @ -73 ± 1dBm, typical
	- MCS=6 PER @ -71 ± 1dBm, typical
	- MCS=7 PER @ -69 ± 1dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -87 ± 1dBm, typical
	- 9Mbps PER @ -86 ± 1dBm, typical
	- 12Mbps PER @ -85 ± 1dBm, typical
	- 18Mbps PER @ -83 ± 1dBm, typical
	- 24Mbps PER @ -81 ± 1dBm, typical
	- 36Mbps PER @ -78 ± 1dBm, typical
	- 48Mbps PER @ -74 ± 1dBm, typical
	- 54Mbps PER @ -72 ± 1dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -90 ± 1dBm, typical
	- 2Mbps PER @ -89 ± 1dBm, typical
	- 5.5Mbps PER @ -87 ± 1dBm, typical
	- 11Mbps PER @ -84 ± 1dBm, typical

Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	6.5	V
VDDIO	Digital/Bluetooth/SDIO Voltage	-0.5	4.1	V

4.2.2 Recommended Operating Ratings

Test conditions: At room temperature 25°C				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBAT	3.0	3.6	4.8	V
VDDIO	1.71	-	3.6	V

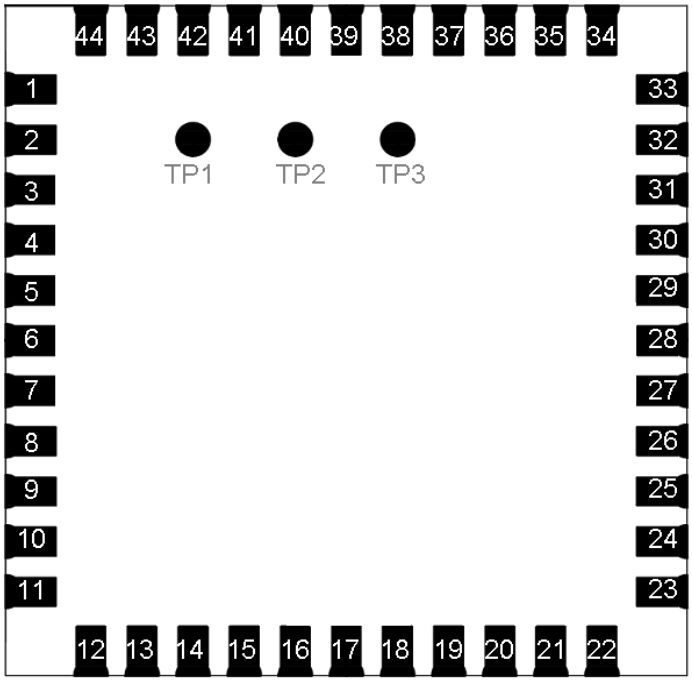
Note: The voltage of VDDIO is depended on system I/O voltage.

Test conditions: At operating temperature -10°C ~65°C				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBAT	3.0	3.6	4.8	V
VDDIO	1.71	-	3.6	V

Note: VDDIO operating voltage range from 1.71V to 3.63V at operating temperature is guaranteed.

5. Pin Assignments

5.1 PCB Pin Outline



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5.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	NC	—	Floating (Don't connected to ground)
6	NC	—	Floating (Don't connected to ground)
7	NC	—	Floating (Don't connected to ground)
8	NC	—	Floating (Don't connected to ground)
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	XTAL oscillator input
11	XTAL_OUT	O	XTAL oscillator output
12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN wake-up HOST
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line3

16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO CLK line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	NC	—	Floating (Don't connected to ground)
26	NC	—	Floating (Don't connected to ground)
27	NC	—	Floating (Don't connected to ground)
28	NC	—	Floating (Don't connected to ground)
29	WL_VDD_TCXO	P	1.7V to 3.3V supply for the TCXO driver
30	TCXO_IN	I	Reference clock input
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	NC	—	Floating (Don't connected to ground)
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	NC	—	Floating (Don't connected to ground)
38	NC	—	Floating (Don't connected to ground)
39	NC	—	Floating (Don't connected to ground)
40	NC	—	Floating (Don't connected to ground)
41	NC	—	Floating (Don't connected to ground)
42	NC	—	Floating (Don't connected to ground)
43	NC	—	Floating (Don't connected to ground)
44	NC	—	Floating (Don't connected to ground)
45	TP1 (NC)	—	Floating (Don't connected to ground)
46	TP2 (NC)	—	Floating (Don't connected to ground)
47	TP3 (NC)	—	Floating (Don't connected to ground)

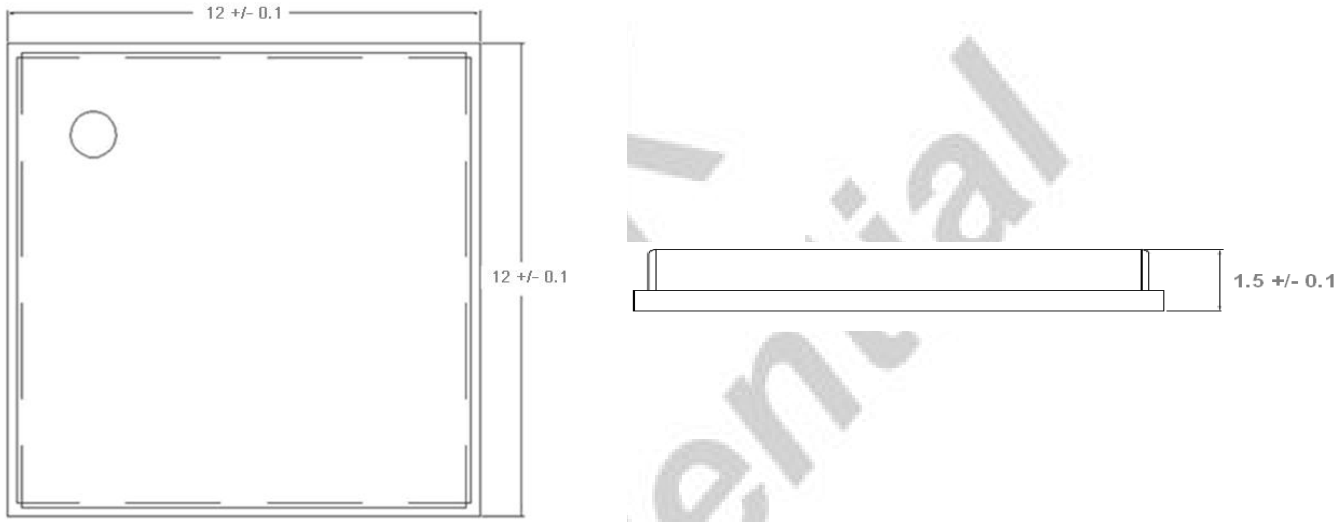
6. Dimensions

6.1 Physical Dimensions

(Unit: mm)

< TOP VIEW >

< Side View >



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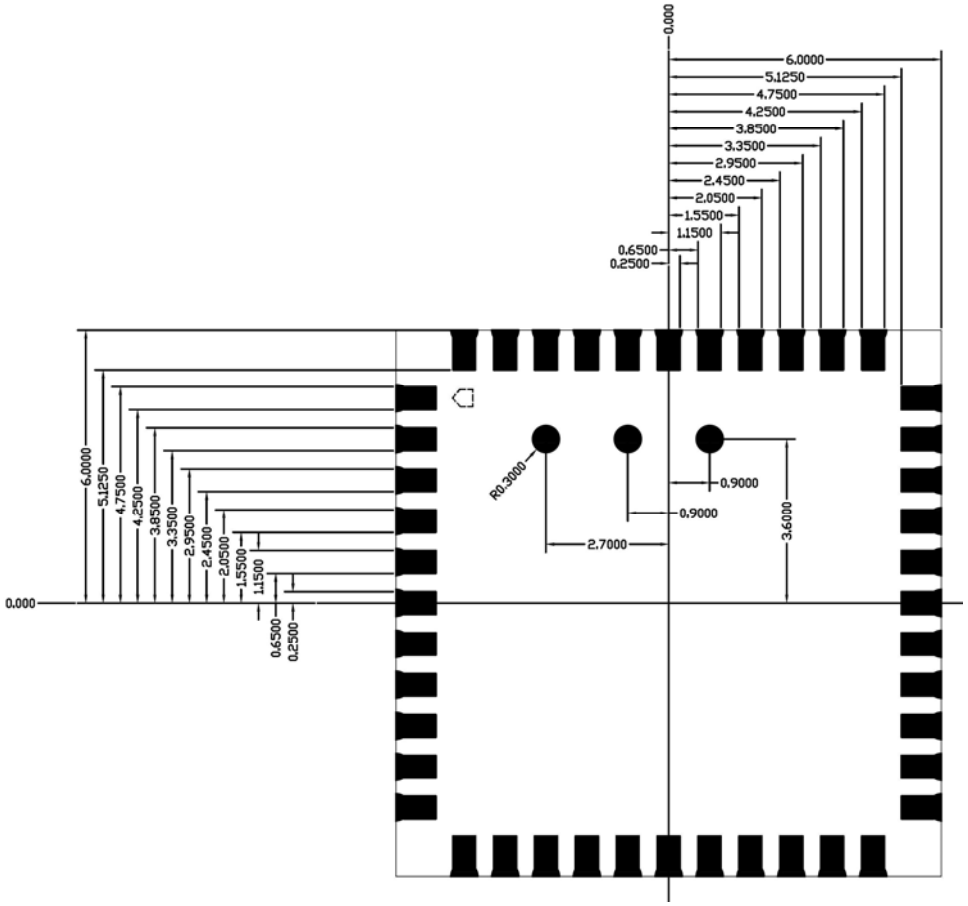

6.2 Recommended Footprint

(Unit: mm)

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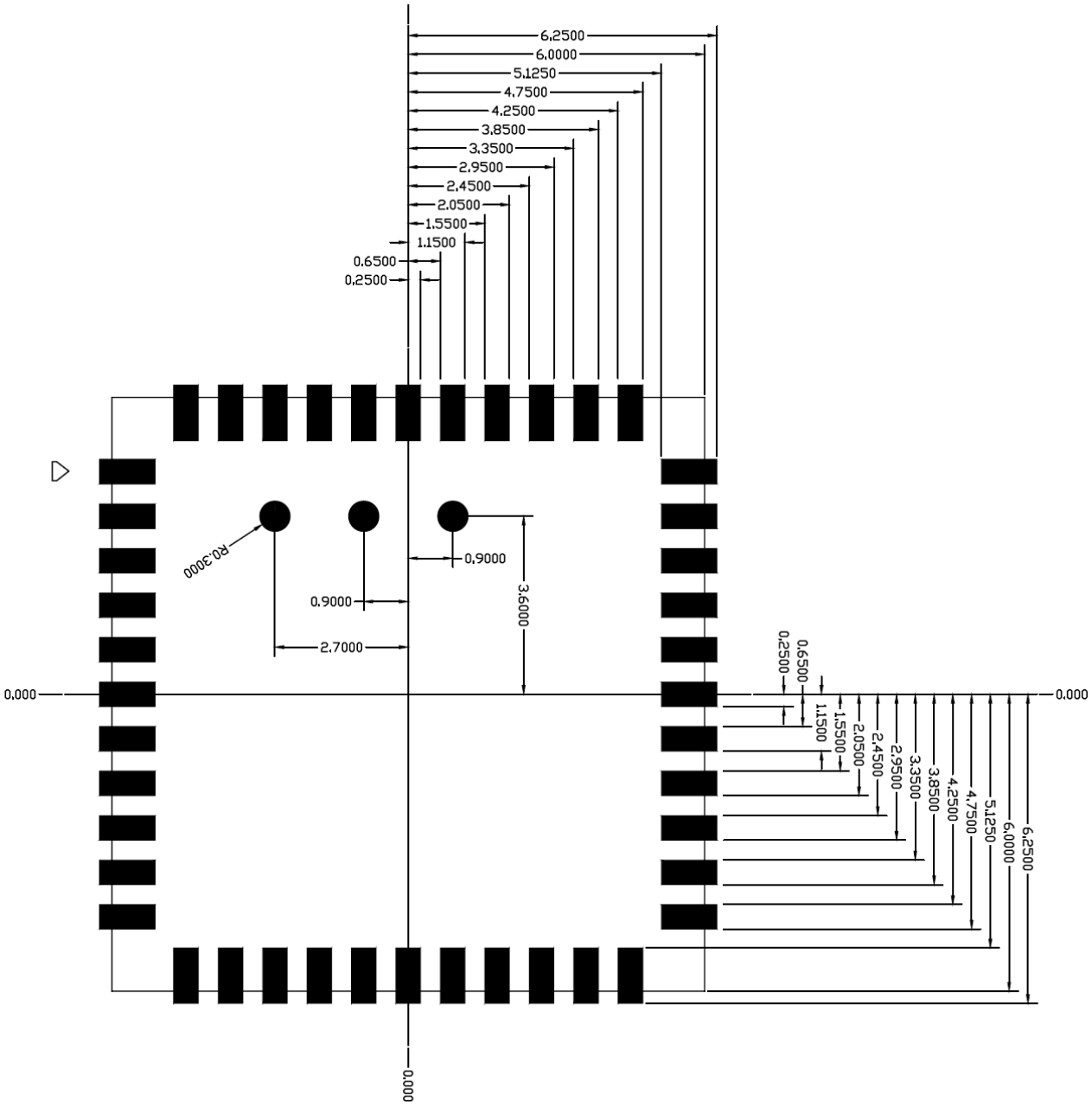


7. External clock reference

External LPO signal characteristics

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1600 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz

External Ref_CLK signal characteristics

No.	Item	Symb.	Electrical Specification				Remark
			Min.	Type	Max.	Units	
1	Nominal Frequency	F0	26.00000			MHz	
2	Mode of Vibration		Fundamental				
3	Frequency Tolerance	ΔF/F0	-10	-	10	ppm	at 25℃±3℃
4	Operating Temperature Range	T_{OPR}	-30	-	85	℃	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T_{STG}	-55	-	125	℃	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	μW	
10	Insulation Resistance	IR	500	-	-	MΩ	At 100V_{DC}
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

7.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

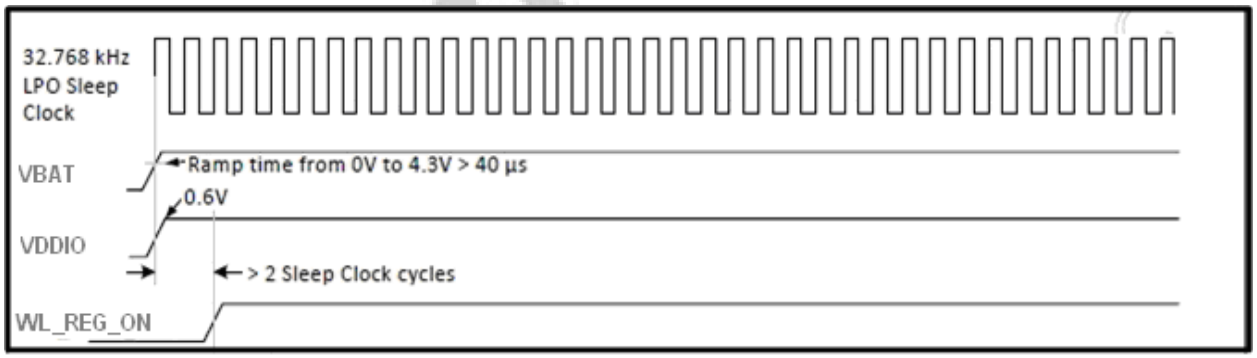
- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

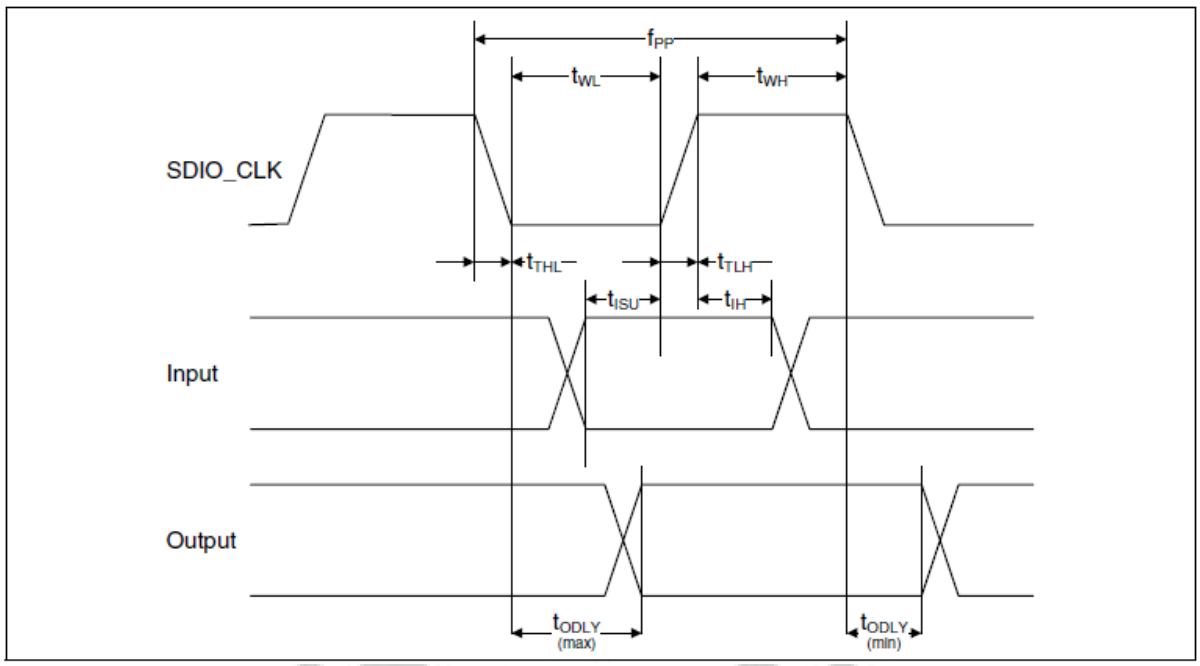
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram



※ WL_REG_ON: Internal regulators power enable/disable.
This pin must be driven high or low (not left floating).

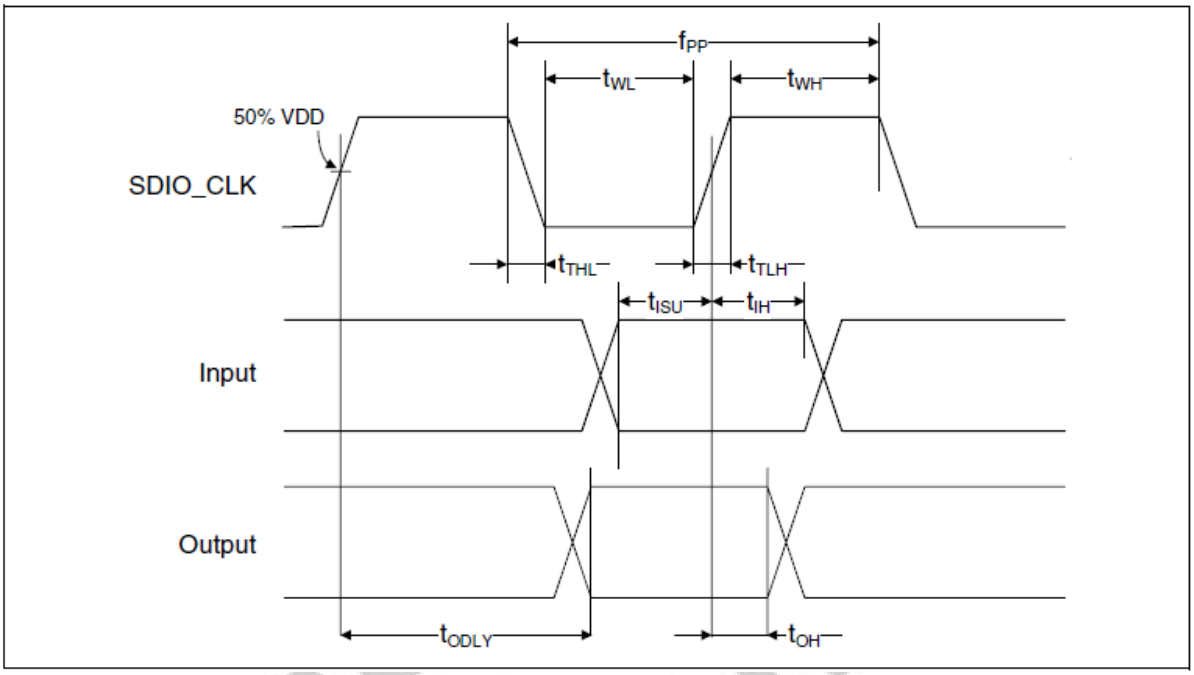
8.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

8.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

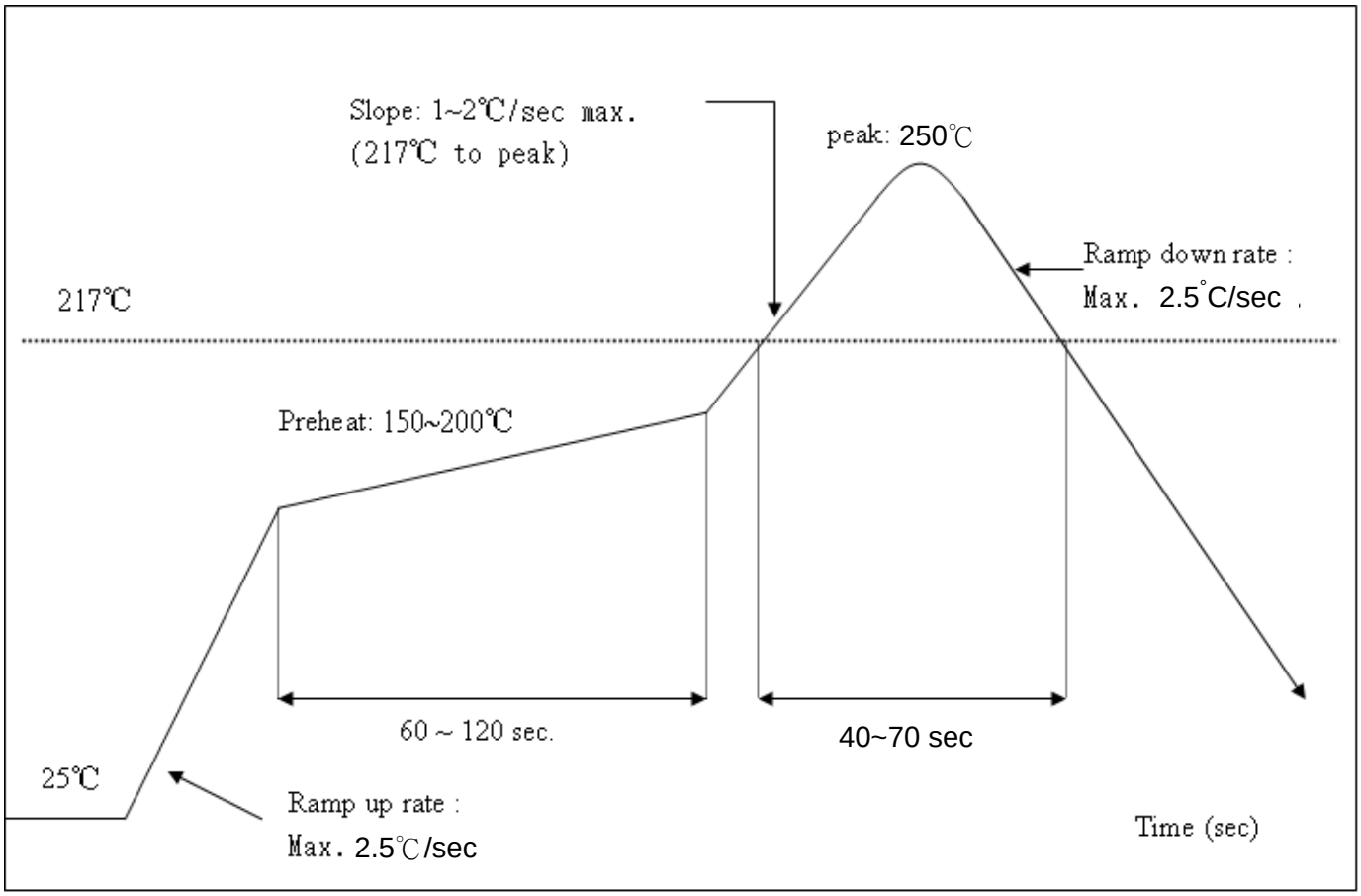
a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

9. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times

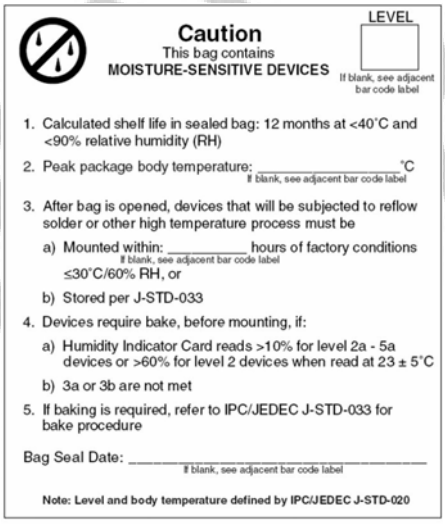


10. Packing Information

10.1 Label

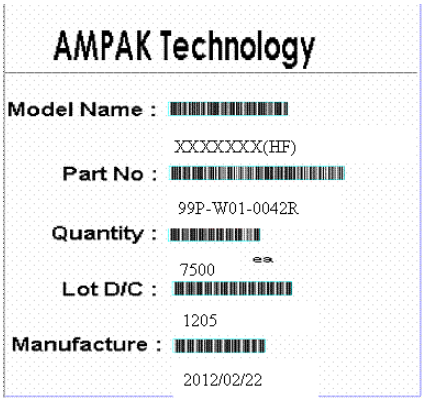
Label A → Anti-static and humidity notice

Label B → MSL caution / Storage Condition

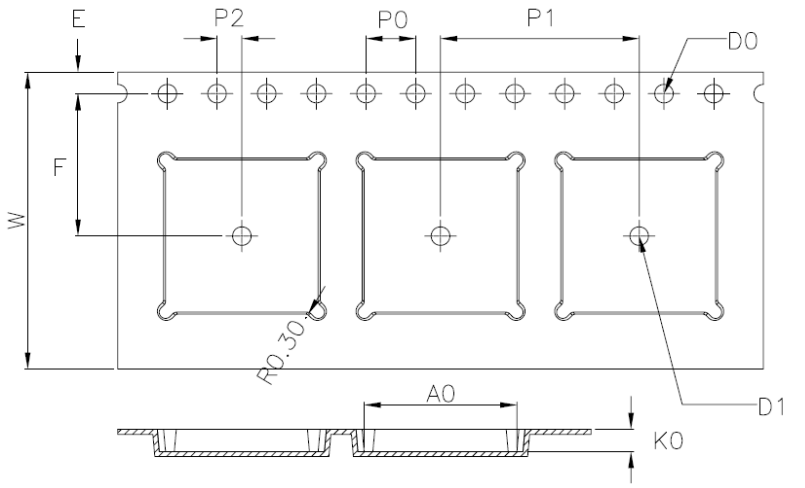


Label C → Inner box label .

Label D → Carton box label .

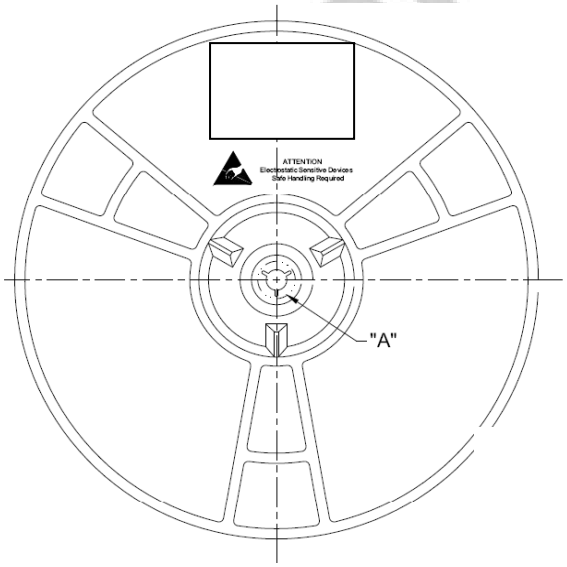


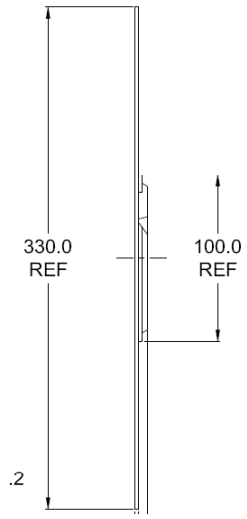
10.2 Dimension

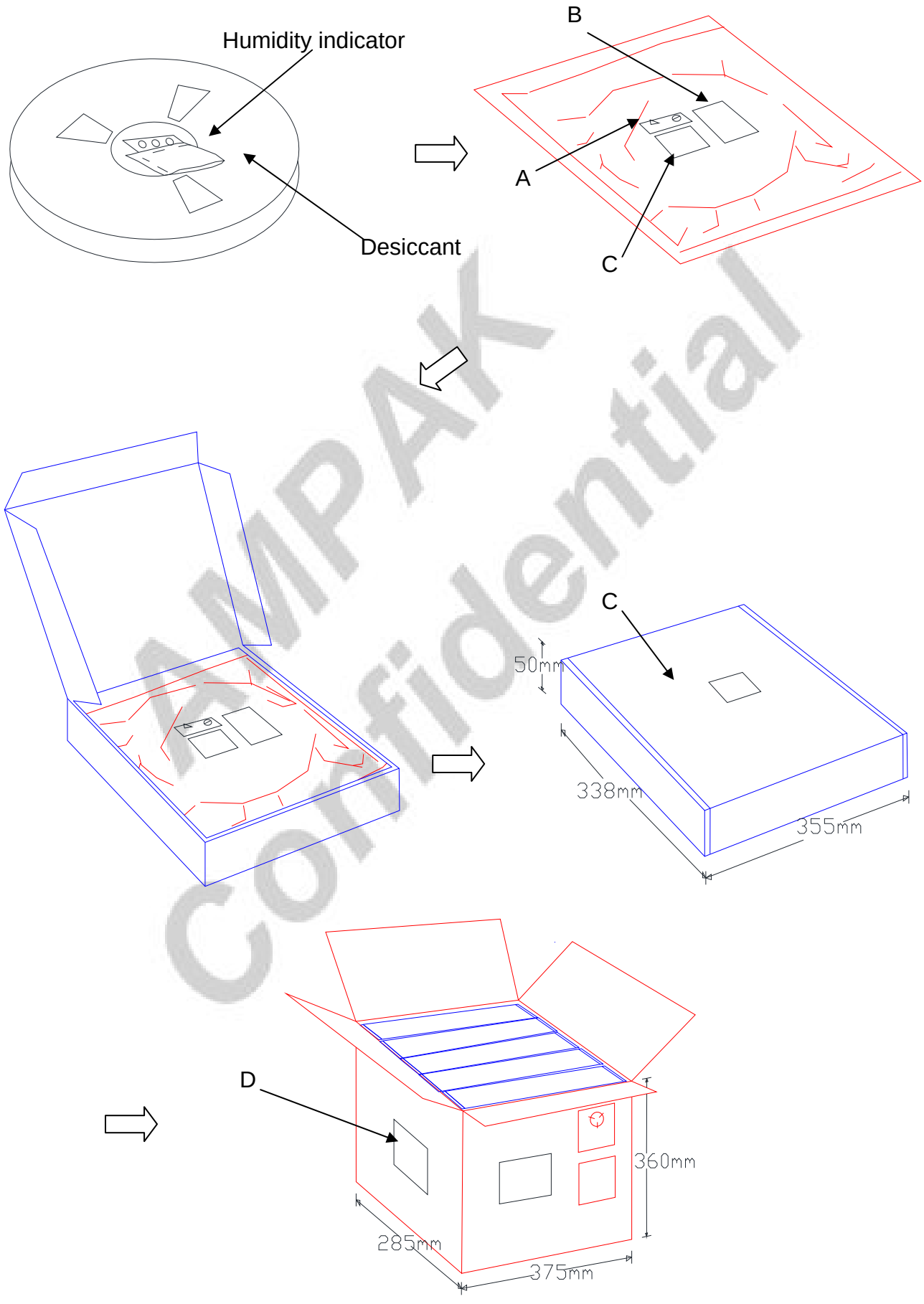


W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $^{+0.10}_{-0.00}$
D1	ø1.50MIN

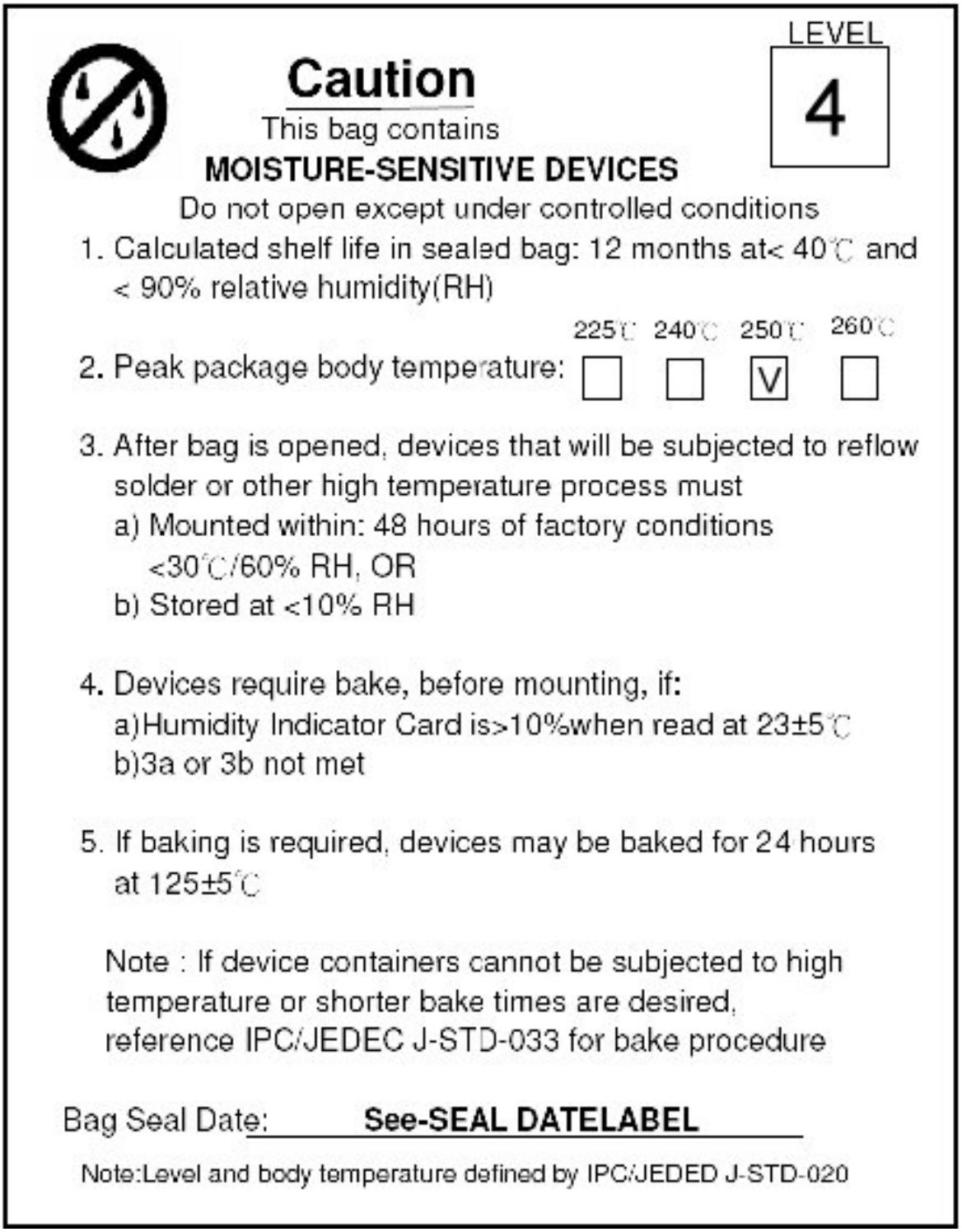
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.







10.3 MSL Level / Storage Condition



LEVEL 4

Caution

This bag contains

MOISTURE-SENSITIVE DEVICES

Do not open except under controlled conditions

1. Calculated shelf life in sealed bag: 12 months at< 40℃ and < 90% relative humidity(RH)

2. Peak package body temperature: 225℃ ☐ 240℃ ☐ 250℃ ☑ 260℃ ☐

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 48 hours of factory conditions <30℃/60% RH, OR
   b) Stored at <10% RH

4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is>10%when read at 23±5℃
   b) 3a or 3b not met

5. If baking is required, devices may be baked for 24 hours at 125±5℃

Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: **See-SEAL DATELABEL**

Note:Level and body temperature defined by IPC/JEDED J-STD-020

※NOTE : Accumulated baking time should not exceed 96hrs