正基科技股份有限公司

SPECIFICATION

SPEC. NO.：＿＿＿＿＿＿＿＿＿＿＿　REV：＿＿1.2＿＿＿

DATE：＿＿＿10. 30. 2012＿＿＿

PRODUCT　NAME：＿＿＿＿＿AP6493＿＿＿＿＿＿＿

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

AMPAK

AP6493

WiFi+Bluetooth 4.0+FM RX +NFC
SIP Module Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2012/10/05	- Preliminary	Joe	1.0
2012/10/26	- Modify pin define	Joe	1.1
2012/10/30	- Modify pin define	Joe	1.2

Contents

1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module, which has all of the WiFi, Bluetooth, FM and NFC functionalities. The highly integrated AP6493 module makes the possibilities of web browsing, VoIP, Bluetooth headsets, FM radio functional applications and other applications. With seamless roaming capabilities and advanced security, AP6493 can also interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO (4bit/1bit) interface for WiFi, UART / PCM interface for Bluetooth and UART / PCM interface for FM.

This compact module is a total solution for a combination of WiFi + BT + FM + NFC technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- 802.11b/g/n single-band radio
- Bluetooth V4.0(HS) with integrated Class 1 PA and Low Energy (BLE) support
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
    - SDIO v2.0 — up to 50 MHz clock rate
- BT host digital interface:
    - UART (up to 4 Mbps)
- FM multiple audio routing options:PCM, eSCO, A2DP
- IEEE Co-existence technologies are integrated die solution
- ECI - enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- NFC - Support for the ISO/IEC 18092, ISO/IEC 21481, ISO/IEC 14443 Types A, B and B', Japanese Industrial Standard (JIS) (X) 6319-4, and ISO/IEC 15693 standards, Support Reader/Writer (R/W) mode, Active and Passive Peer (P2P) mode.

A simplified block diagram of the module is depicted in the figure below.
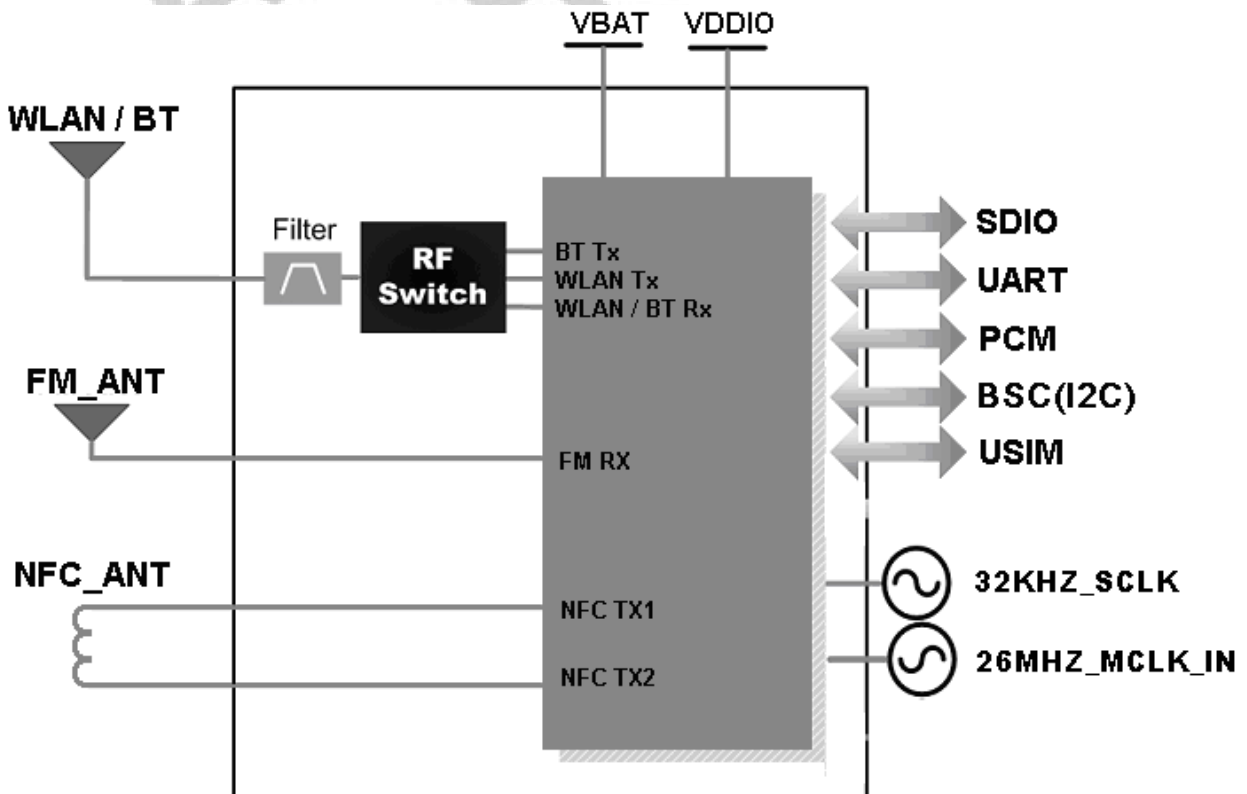
3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	AP6493
Product Description	Support WiFi/Bluetooth/FM/NFC functionalities
Dimension	L x W x H: 12.0 x 12.0 x 1.5 (typical) mm
WiFi Interface	SDIOV2.0 (4bit/1bit)
BT Interface	UART/ PCM
FM Interface	UART /PCM
NFC Interface	BSC
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	6	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	2.98	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.6	4.8	V
VDDIO	1.62	1.8	2.9+/-3%	V
VDDSWP_IN ETSI compliant to power class C	1.78	1.88	1.98	V
VDDSWP_IN ETSI compliant to power class B	2.9	3.1	3.3	V

5. WiFi RF Specification

5.1 2.4GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=2.9V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz：Ch1 ~ Ch14
Modulation	802.11b : DQPSK, DBPSK, CCK
	802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM $\leq$ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM $\leq$ -25dB
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM $\leq$ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 dBm, typical
	- MCS=1 PER @ -84 dBm, typical
	- MCS=2 PER @ -82 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -73 dBm, typical
	- MCS=6 PER @ -71 dBm, typical
	- MCS=7 PER @ -69 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -86 dBm, typical
	- 9Mbps PER @ -85 dBm, typical
	- 12Mbps PER @ -85 dBm, typical
	- 18Mbps PER @ -83 dBm, typical
	- 24Mbps PER @ -81 dBm, typical
	- 36Mbps PER @ -78 dBm, typical
	- 48Mbps PER @ -73 dBm, typical
	- 54Mbps PER @ -72 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -90 dBm, typical
	- 2Mbps PER @ -89 dBm, typical
	- 5.5Mbps PER @ -88 dBm, typical
	- 11Mbps PER @ -85 dBm, typical
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps

Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

6. Bluetooth Specification

6.1 Bluetooth Specification

Conditions : VBAT=3.6V ; VDDIO=2.9V ; Temp:25°C

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.0 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2.400 GHz ~ 2483.5 GHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power (Class 1.5)		10 dBm	
Output Power (Class 2)		2 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

7. FM Specification

7.1 FM Specification (TBD)

Conditions : VBAT=3.6V ; VDDIO=2.9V ; Temp:25°C

Feature	Description					
General Specification						
Frequency Band	76MHz-108MHz					
Host Interface	HCI UART, PCM					
Channel step	50 KHz					
Analog Audio output load	R_L>30KΩ, C_L>20pF					
Characteristics	**Condition**		**MIN**	**TYP**	**MAX**	**UNIT**
Receiver (FM Rx Antenna = 120nH, Q>30)	RDS Sensitivity					dBm
	Audio harmonic distortion (Vin=1mV, △f=75KHz)	fmod=1KHz				%
		fmod=3KHz				
	Maximum SNR (fmod=1KHz,△f=22.5 KHz, BW=300Hz to 15KHz)	MONO				dB
		Stereo				
	RF input power level					dBuV

8. Pin Assignments

8.1 Pin Outline

< TOP VIEW >
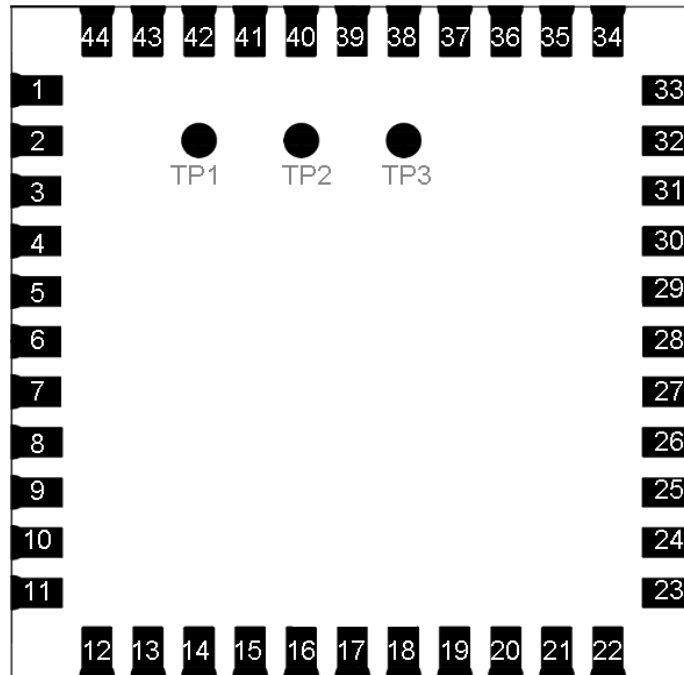
8.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	FM_RX	I	FM radio RF input antenna port
5	N_WAKE	I	HOST wake-up NFC device
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	N_HOST_WAKE	O	NFC device to wake-up HOST
9	VBAT	P	Main power voltage source input
10	NC	—	Floating (Don't connected to ground)
11	NC	—	Floating (Don't connected to ground)
12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN to wake-up HOST

14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	Low power oscillator clock input (32.768KHz)
25	PCM_OUT	I/O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I/O	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	VDD_TCXO	P	1.8V supply for internal buffer driving
30	TCXO_IN	I	26MHz TCXO 1.8V level input
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	N_I2C_SDA	I	BSC Serial Data Line
36	GND	—	Ground connections
37	N_I2C_SCL	I	BSC Serial Clock
38	N_REG_PU	I	NFC Internal regulators power enable/disable
39	TX2	O	NFC Tx coil output 2
40	TX1	O	NFC Tx coil output 1
41	UART_RTS_N	O	Bluetooth/FM UART interface
42	UART_TXD	O	Bluetooth/FM UART interface
43	UART_RXD	I	Bluetooth/FM UART interface
44	UART_CTS_N	I	Bluetooth/FM UART interface
45	TP1	I/O	NFC_VDDSWPIO(SWP I/O)
46	TP2	O	NFC_VDDSWP_OUT(UICC support out)
47	TP3	I	NFC_VDDSWP_IN(Platform UICC supply in)

9. Dimensions

9.1 Physical Dimensions

(Unit: mm)
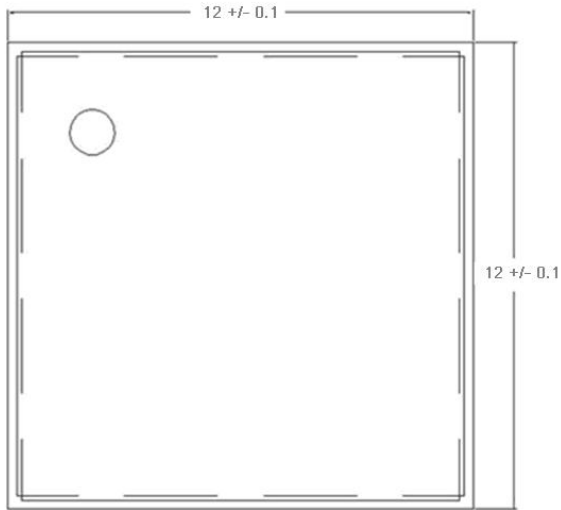
< TOP VIEW >   < Side View >
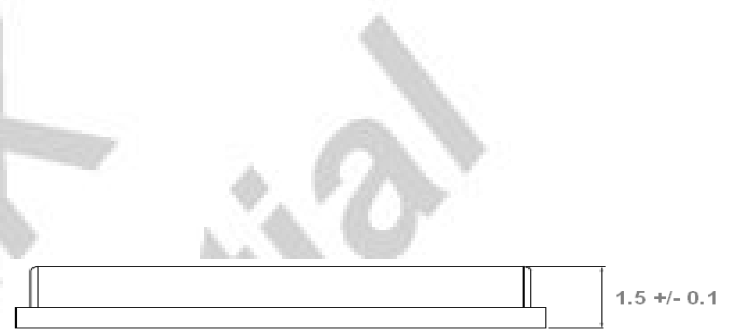
< TOP VIEW >
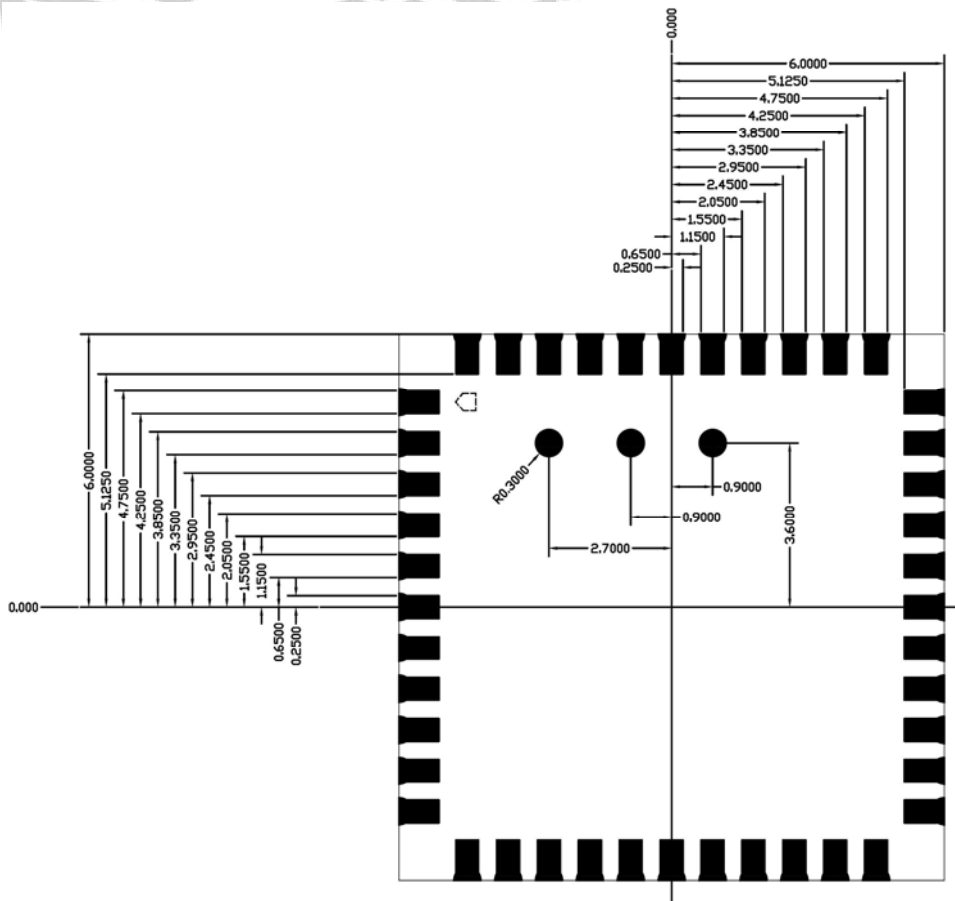
9.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >
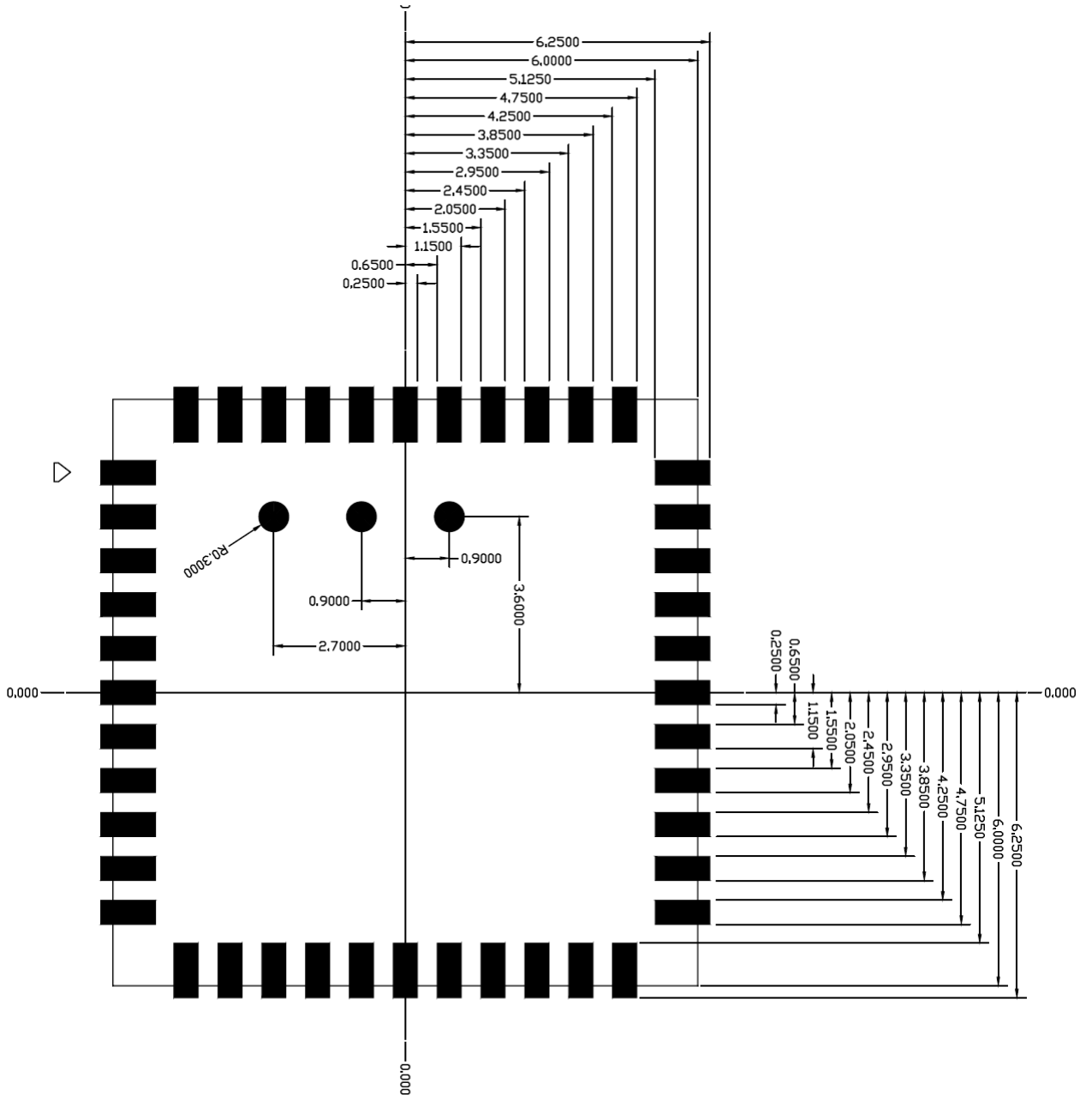
10. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	± 30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

External Ref_CLK signal characteristics

No.	Item	Symb.	Min.	Type	Max.	Units	Remark
				Electrical Specification			
1	Nominal Frequency	F0		26.00000		MHz	
2	Mode of Vibration			Fundamental			
3	Frequency Tolerance	△F/F0	-10	-	10	ppm	at 25℃±3℃
4	Operating Temperature Range	T_{OPR}	-30	-	85	℃	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T_{STG}	-55	-	125	℃	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	μW	
10	Insulation Resistance	IR	500	-	-	MΩ	At 100V$_{DC}$
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

10.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

11. Host Interface Timing Diagram

11.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.

※ BT_RST_N: Low asserting reset for Bluetooth and FM only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).
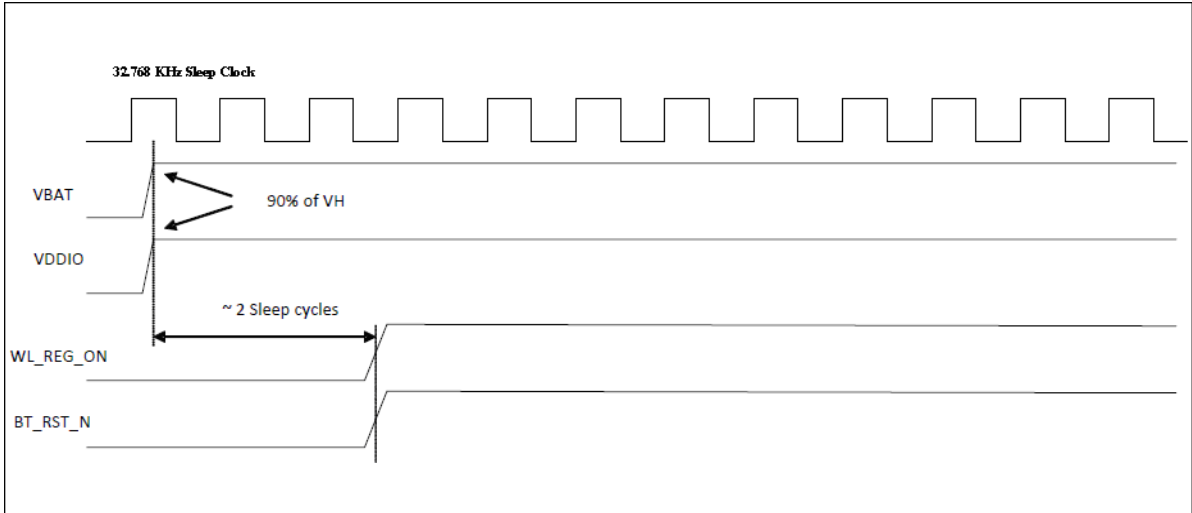
WLAN=ON, Bluetooth=ON
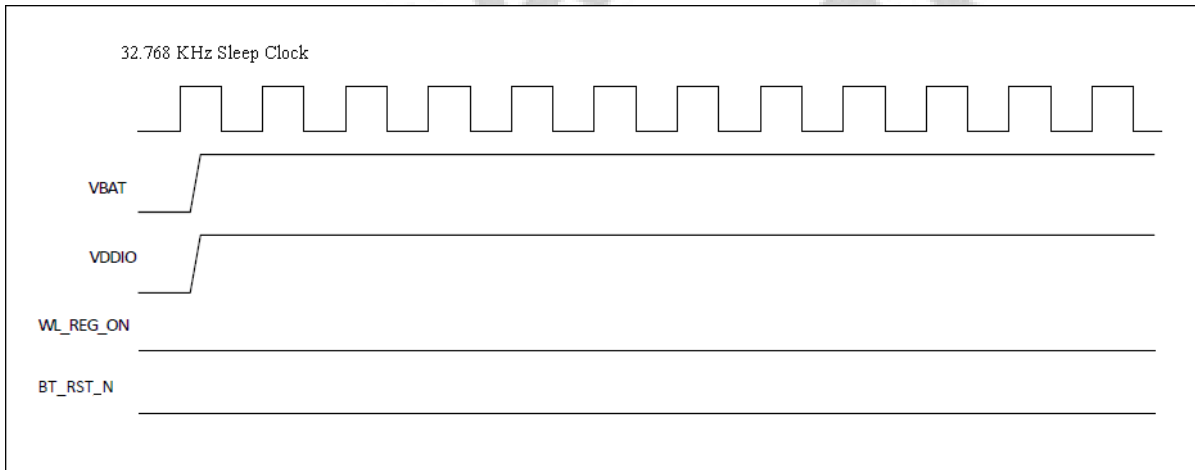
WLAN=OFF, Bluetooth=OFF
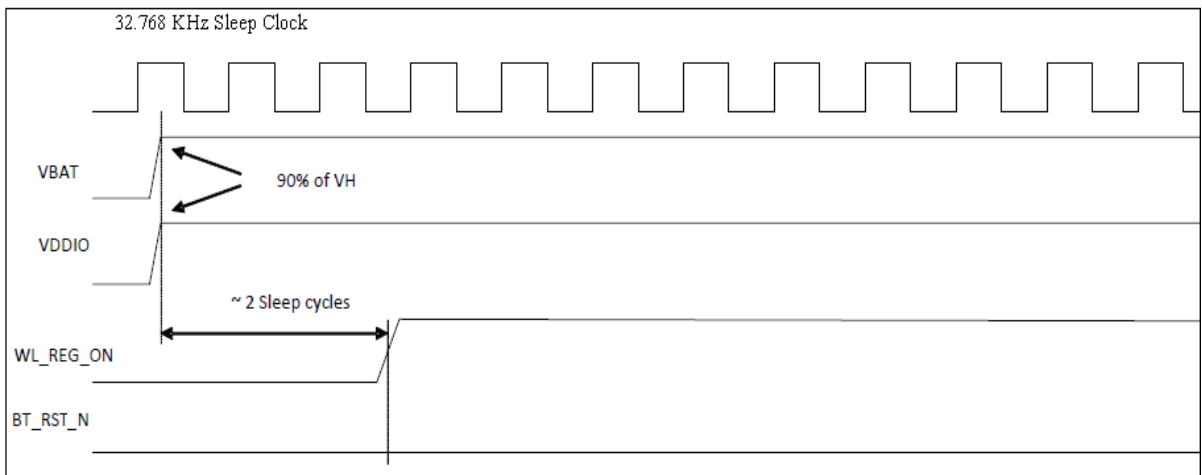
WLAN=ON, Bluetooth=OFF
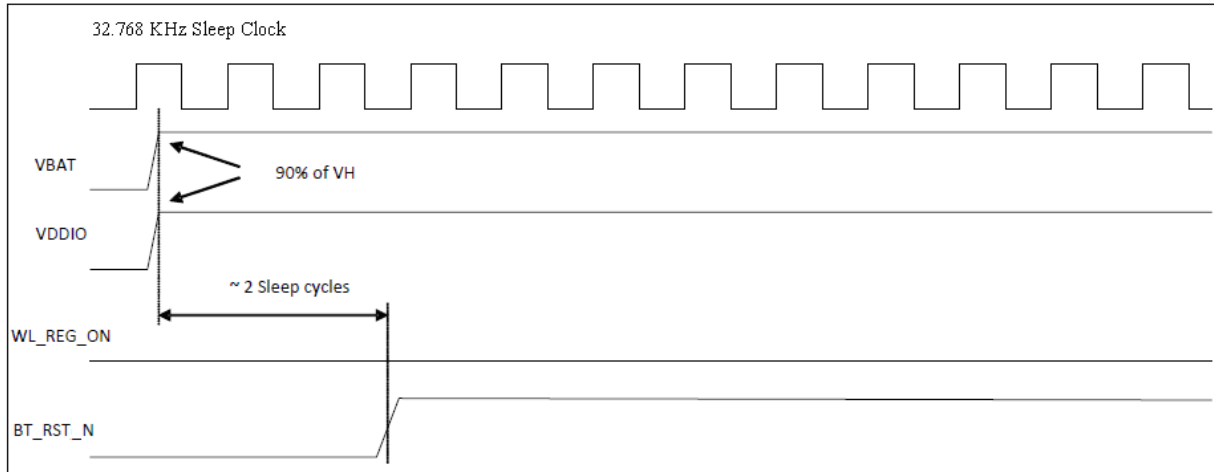
WLAN=OFF, Bluetooth=ON
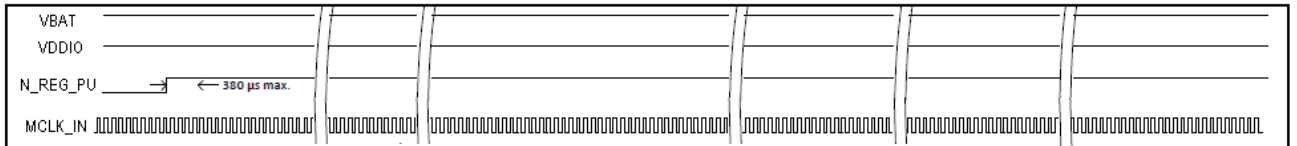
NFC ON

11.2 SDIO Default Mode Timing Diagram
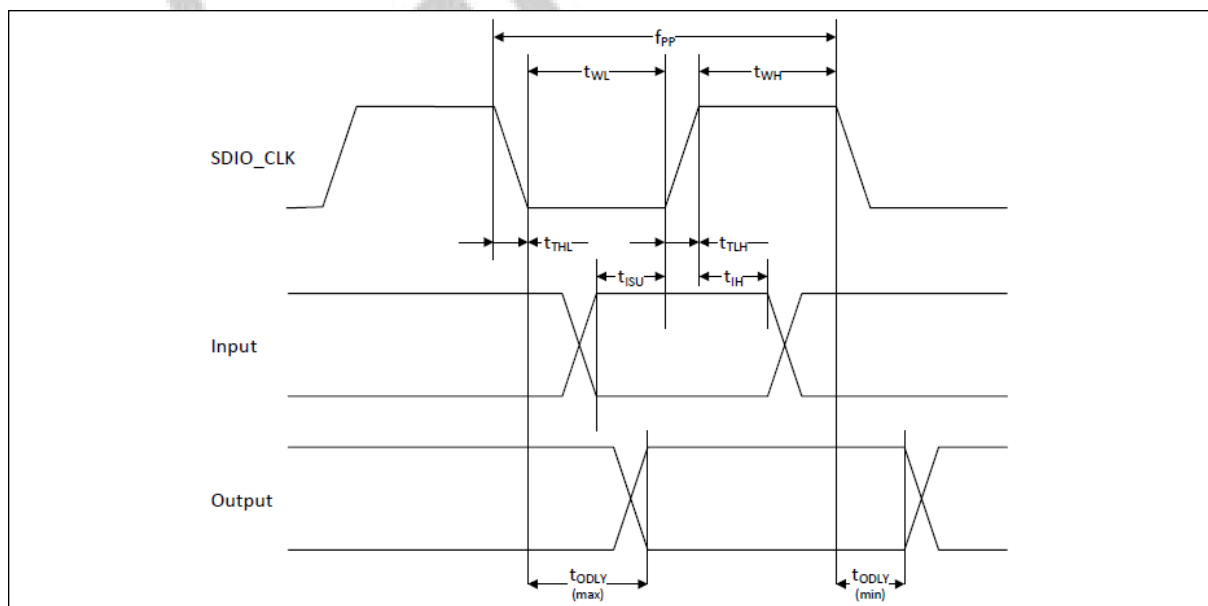
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

11.3 SDIO High Speed Mode Timing Diagram
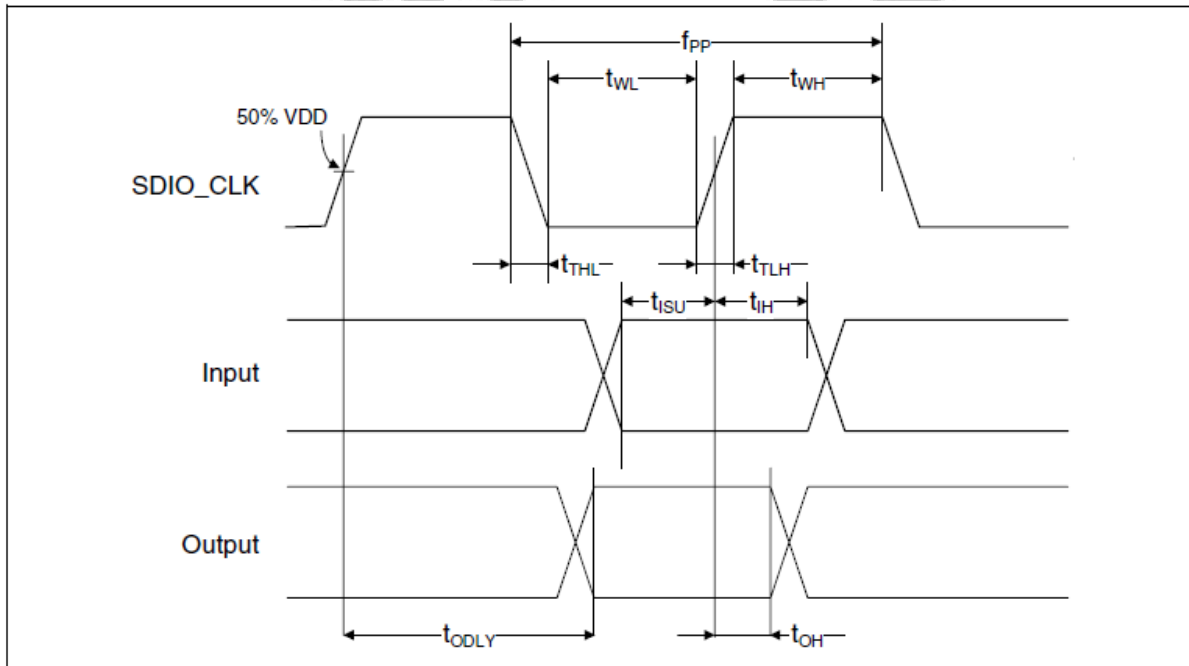
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

11.4 BSC (I2C-Compatible)

Following are the main features of the BSC host interface:

• Slave mode

• Low-speed mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps)
 upported. Due topractical constraints imposed by parasitic capacitance and pull-up resistor
 values, especially in a multidrop system, recommend that this be limited to 1.7 Mbps.

• 7-bit or 10-bit addressing mode; default boot-up of fixed 10-bit address (0x1FA), thereafter
 configurable to 7-bit or 10-bit addresses

• Dedicated TX and RX FIFOs, 272 bytes each.

• Digital deglitching filter implemented. Uses simple majority of 3 and will filter spikes up to
 42 ns.

• High-speed reference not required for operation. (Certain accesses in sleep mode will
initiate the wakeup function.)

The BSC timing waveform is shown in
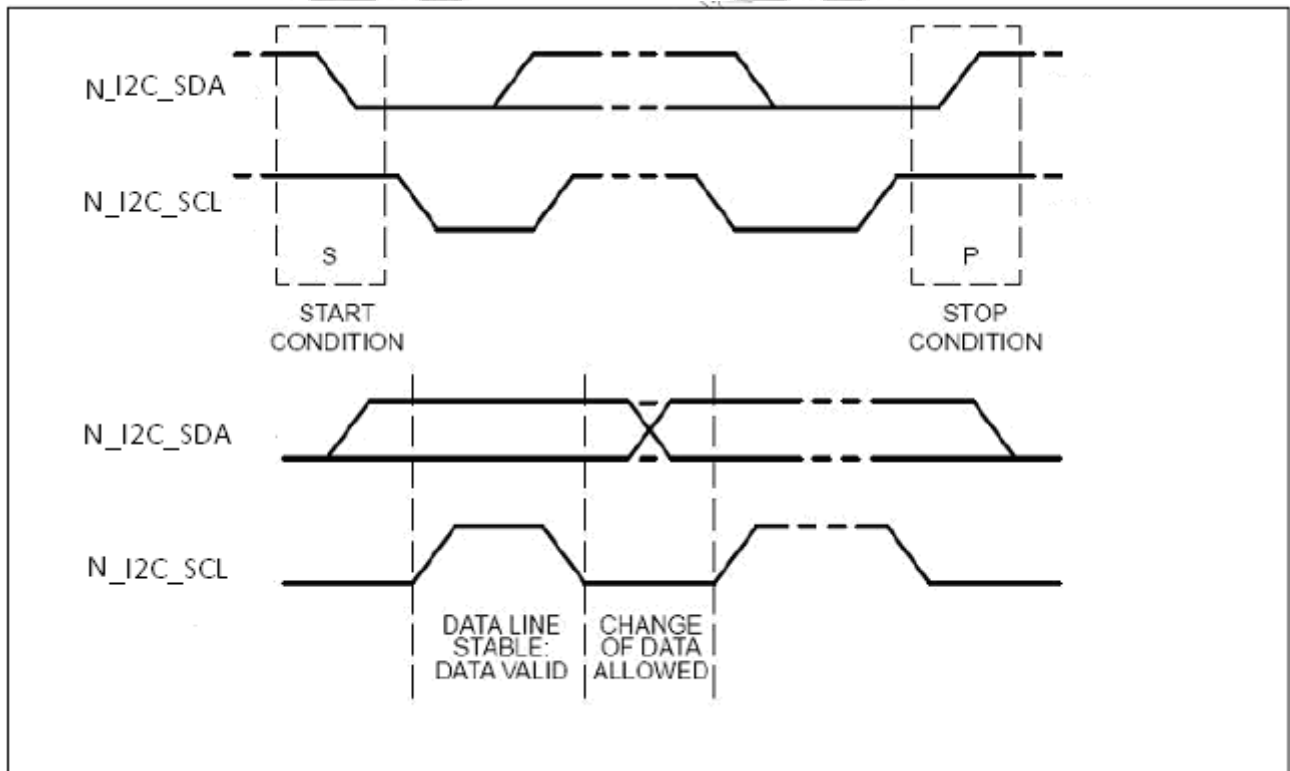
BSC Timing Waveform

NFC_HOST_WAKE is an output signal from the BCM20793S to the host that it wishes to communicate. The timing diagram shows NFC_HOST_WAKE as active high. The NFC_HOST_WAKE signal stays high until after the first byte has been read by the host.
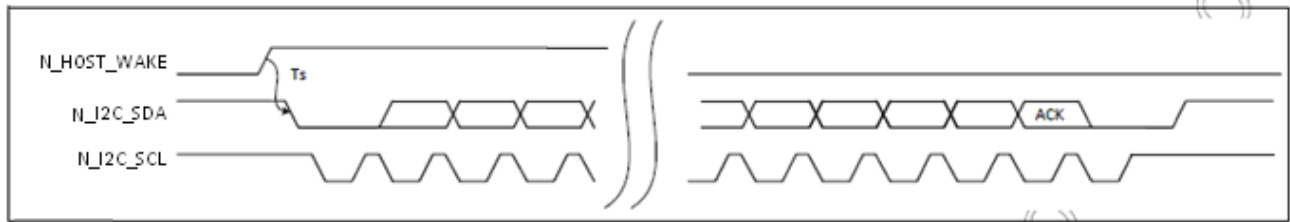
N_HOST_WAKE Timing Waveform

12. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times
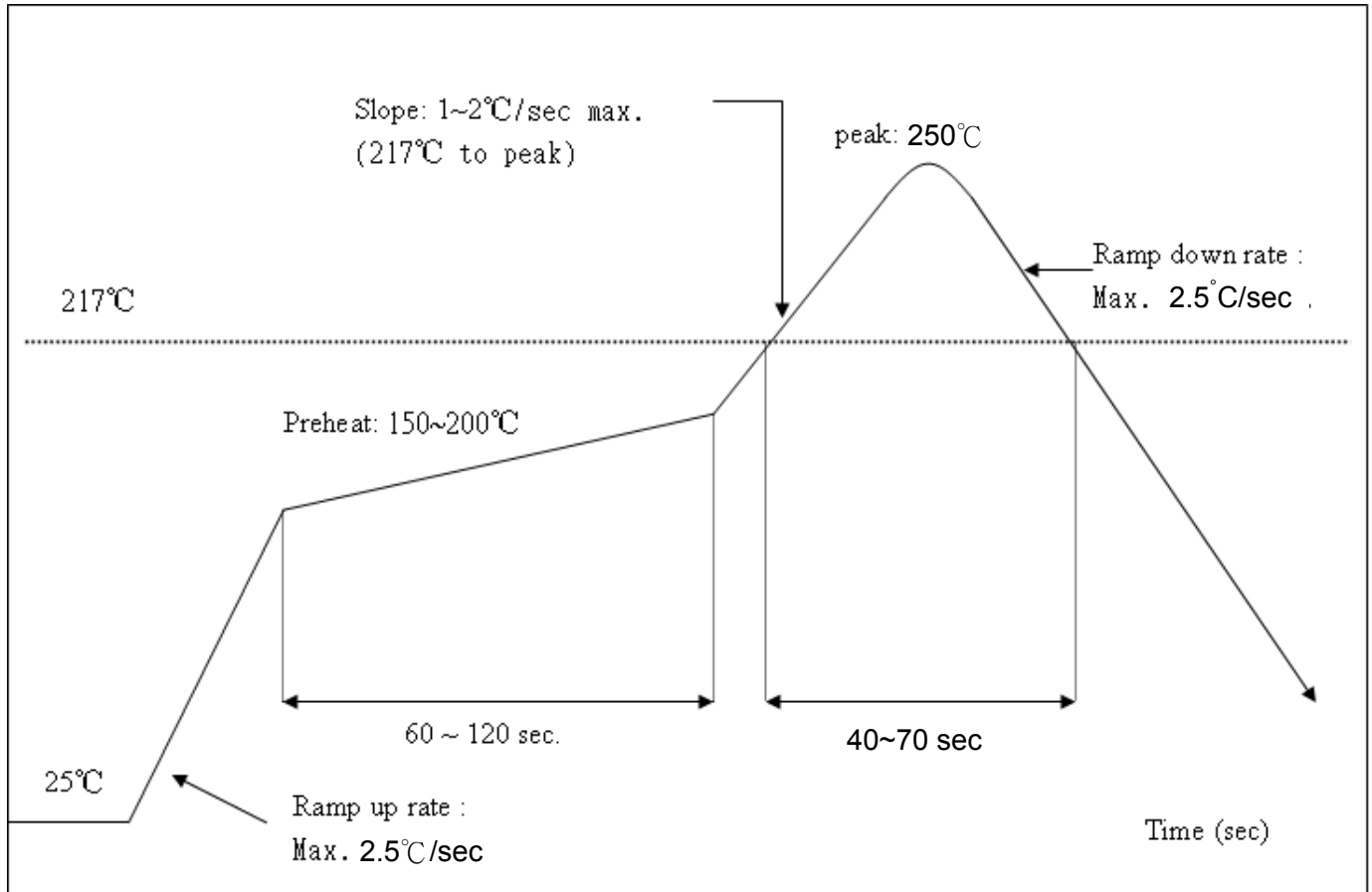
13. Package Information

13.1 Label

Label A→ Anti-static and humidity notice

Label B→ MSL caution / Storage Condition

Label C→ Inner box label .

PKG S/N :	9PKG12013100001
Model:	XXXXXXXXXXX
P/N :	99P-W01-0048R
Qty :	1500
Date Code :	1205
Lot Code :	T0C102B

Label D→ Carton box label .

AMPAK Technology

Model Name :	XXXXXXXXXXX
Part No :	99P-W01-0048R
Quantity :	7500 ea
Lot D/C :	20081000033
Manufacture :	2012/02/22

13.2 Dimension

W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $^{+0.10}_{-0.00}$
D1	⌀1.50MIN
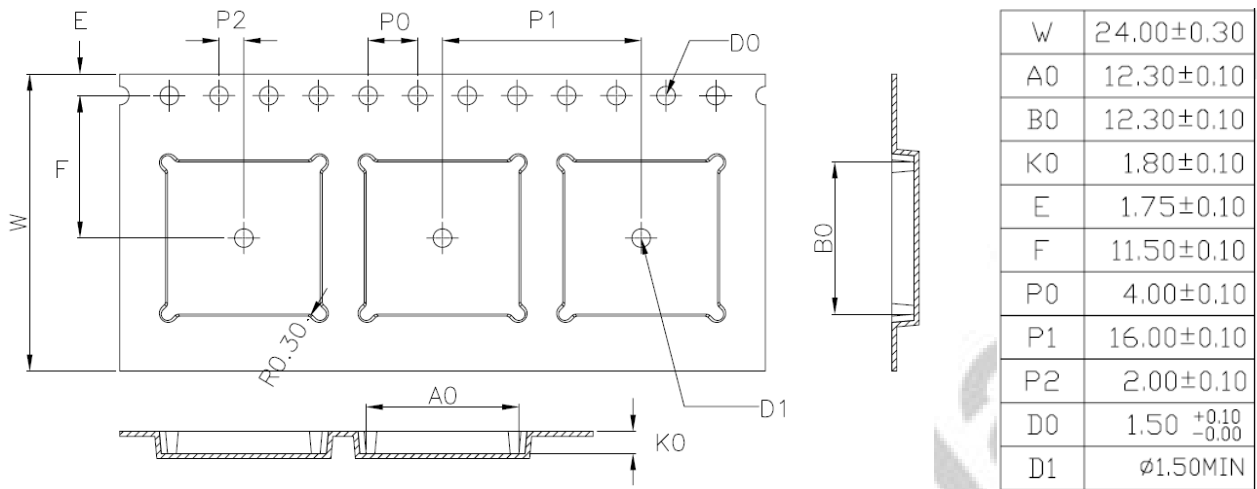
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.

Humidity indicator

Desiccant

B

A

C

C

50mm

338mm

355mm

D

360mm

285mm

375mm
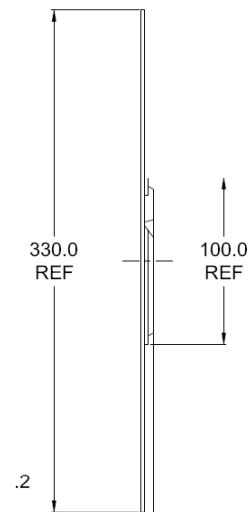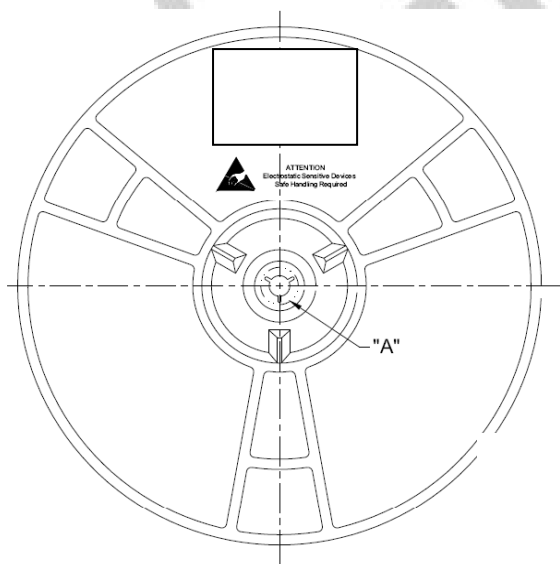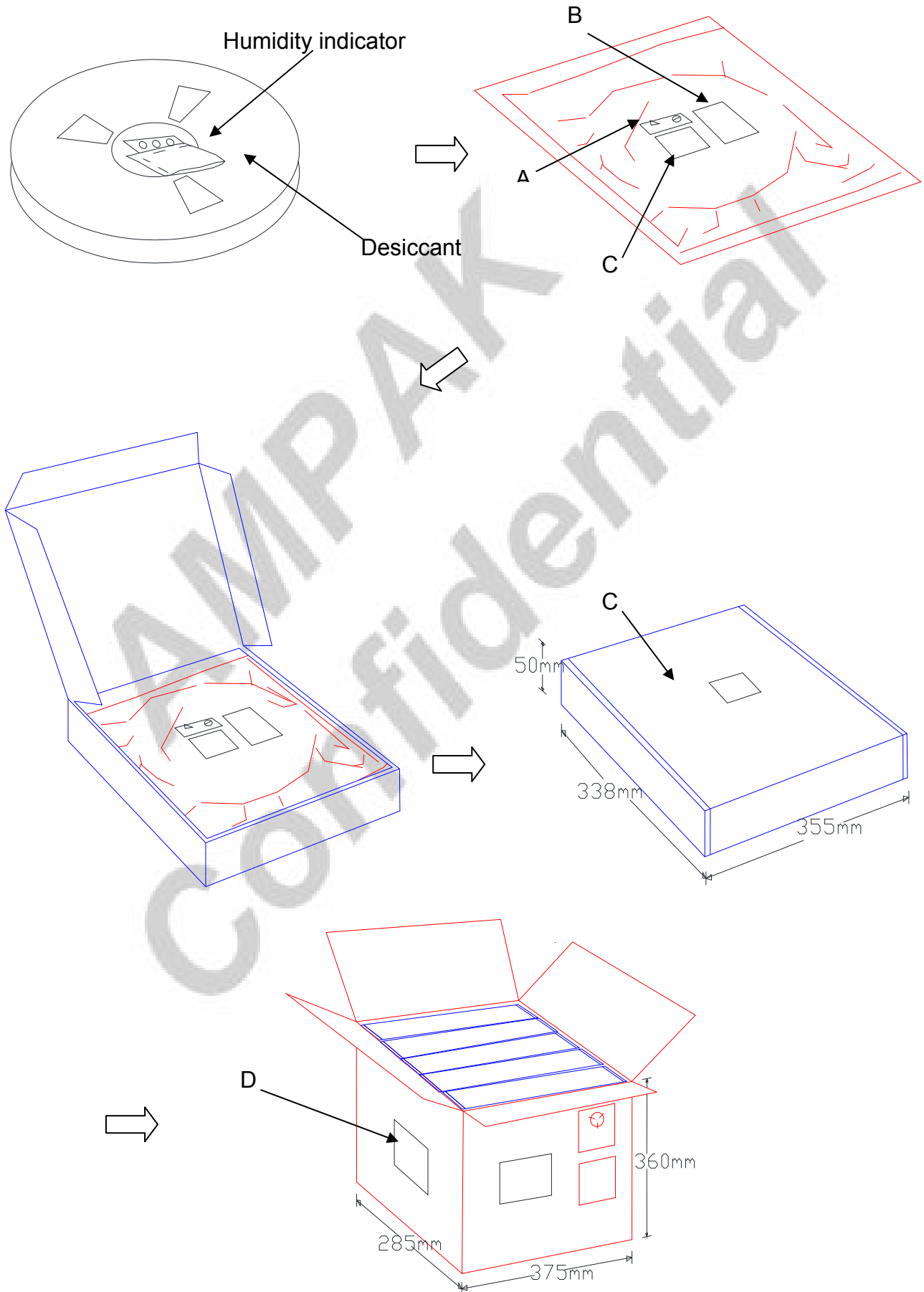
13.3 MSL Level / Storage Condition

LEVEL

4

⊘ **Caution**
This bag contains
MOISTURE-SENSITIVE DEVICES
Do not open except under controlled conditions

1. Calculated shelf life in sealed bag: 12 months at< 40℃ and
   < 90% relative humidity(RH)

   225℃ 240℃ 250℃ 260℃
2. Peak package body temperature: ☐ ☐ ☑ ☐

3. After bag is opened, devices that will be subjected to reflow
   solder or other high temperature process must
   a) Mounted within: 48 hours of factory conditions
      <30℃/60% RH, OR
   b) Stored at <10% RH

4. Devices require bake, before mounting, if:
   a)Humidity Indicator Card is>10%when read at 23±5℃
   b)3a or 3b not met

5. If baking is required, devices may be baked for 24 hours
   at 125±5℃

   Note : If device containers cannot be subjected to high
   temperature or shorter bake times are desired,
   reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: **See-SEAL DATELABEL**

Note:Level and body temperature defined by IPC/JEDED J-STD-020

※NOTE : Accumulated baking time should not exceed 96hrs