RTL8723BS EEPROM Content

Date: 2013/06/04
Version: 02

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Lists of Tables

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Modification History

Version	Data	Author	Change
V001	2013/05/22	Isaac	1. Initial Release
V002	2013/06/04	Jerry Chou	1. Update some RF default values.

1. EEPROM (eFuse) Contents

The RTL8723BS is embedded an internal non-volatile memory called eFuse. Values in the eFuse allow default fields in PCI configuration space and I/O space to be overridden following an internal power on reset, or software eFuse auto-load command. The RTL8723BS will auto-load values from the eFuse to these fields in configuration space and I/O space.

The eFuse emulates the structure of a usual EEPROM such as 93C46. We will describe the content and its addressing of the eFuse as we did in 93C46 and will mix the terms of EEPROM and eFuse in the following text,. After the initial power on or auto-load command to the eFuse, the RTL8723BS performs a series of EEPROM read operations from the EEPROM addresses 00h to 7Fh. The definition of each EEPROM byte is shown as the below.

Note: It is suggested to obtain Realtek approval before any change on the default settings of the EEPROM.

1.1 WLAN Controller EEPROM Contents Spec

Table 1.1 WLAN Controller EEPROM (eFuse) Contents

Bytes	Contents	Description	Value
00h	29h	These 2 bytes contain the ID code word for the RTL8723BS. The RTL8723BS will load the contents of the EEPROM into the corresponding location if the ID word is correct.	8129h
01h	81h		
02h ~ 0Fh	Reserved	Reserved for Realtek. Do not change this field without Realtek's approval.	-
10h	Path A 2.4G CCK-1TX Power Index (Absolute Value)	Path A CCK Power Index for Ch 1,2, Range 0~63.	2Dh
11h		Path A CCK Power Index for Ch 3, 4, 5, Range 0~63.	2Dh
12h		Path A CCK Power Index for Ch 6, 7, 8, Range 0~63.	2Dh
13h		Path A CCK Power Index for Ch 9, 10, 11, Range 0~63.	2Dh
14h		Path A CCK Power Index for Ch 12, 13, Range 0~63.	2Dh
15h		Path A CCK Power Index for Ch 14, Range 0~63.	2Dh
16h	Path A 2.4G BW40-1S TX Power Index (Absolute Value)	Path A 2G BW40-1S Power Index for Ch 1, 2, Range 0~63.	2Dh
17h		Path A 2G BW40-1S Power Index for Ch 3, 4, 5, Range 0~63.	2Dh
18h		Path A 2G BW40-1S Power Index for Ch 6, 7, 8, Range 0~63.	2Dh
19h		Path A 2G BW40-1S Power Index for Ch 9, 10, 11, Range 0~63.	2Dh
1Ah		Path A 2G BW40-1S Power Index for Ch 12, 13, 14 Range 0~63.	2Dh

<table>
<tr><th>Bytes</th><th>Contents</th><th>Description</th><th>Value</th></tr>
<tr><td>1Bh</td><td>Path A 2.4G BW20-1S TX Power Index Difference
OFDM-1 TX Power Index Difference</td><td>Power Index Difference between BW20-1S and BW40-1S.
Bit[7:4] : Path A 2G Offset, Range –8~7.
Power Index Difference between OFDM-1Tx and BW40-1S.
Bit[3:0] : Path A 2G Offset, Range –8~7.</td><td>E0h</td></tr>
<tr><td>1Ch~39h</td><td>Reserved</td><td>Reserved for Realtek.</td><td>-</td></tr>
<tr><td>3Ah</td><td rowspan="6">Path B 2.4G CCK-1TX Power Index (Absolute Value)</td><td>Path B CCK Power Index for Ch 1,2, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>3Bh</td><td>Path B CCK Power Index for Ch 3, 4, 5, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>3Ch</td><td>Path B CCK Power Index for Ch 6, 7 ,8, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>3Dh</td><td>Path B CCK Power Index for Ch 9, 10, 11, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>3Eh</td><td>Path B CCK Power Index for Ch 12, 13, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>3Fh</td><td>Path B CCK Power Index for Ch 14, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>40h</td><td rowspan="5">Path B 2.4G BW40-1S Tx Power Index (Absolute Value)</td><td>Path B 2G BW40-1S Power Index for Ch 1, 2, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>41h</td><td>Path B 2G BW40-1S Power Index for Ch 3, 4, 5, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>42h</td><td>Path B 2G BW40-1S Power Index for Ch 6, 7 ,8, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>43h</td><td>Path B 2G BW40-1S Power Index for Ch 9, 10, 11, Range 0~63.</td><td>2Dh</td></tr>
<tr><td>44h</td><td>Path B 2G BW40-1S Power Index for Ch 12, 13, 14 Range 0~63.</td><td>2Dh</td></tr>
<tr><td>45h</td><td>Path B 2.4G BW20-1S Tx Power Index Difference
Path B 2.4G OFDM-1Tx Power Index Difference</td><td>Pwower Index Difference between BW20-1S and BW40-1S.
Bit[7:4]: Path B 2G Offset, Range –8~7.
Pwower Index Difference between OFDM-1Tx and BW40-1S.
Bit[3:0]: Path B 2G Offset, Range –8~7.</td><td>E0h</td></tr>
<tr><td>37h~B7h</td><td>Reserved</td><td>Reserved for Realtek.</td><td>-</td></tr>
<tr><td>B8h</td><td>Channel Plan</td><td>Bit[7]: Software configure mode
0h: Enable software configure(refer to Channel Plane Domain Code)
1h: Disable software configure(can't change Channel Plan Setting)
Bit[6:0]: Channel Plan
<table>
<tr><th>Domain Code</th><th>eFuse Value</th><th>Channels</th><th>Descriptio</th></tr>
<tr><td>2G_WORLD</td><td>20h</td><td>1~13</td><td>Worldwird 13</td></tr>
<tr><td>2G_ETSI1</td><td>21h</td><td>1~13</td><td>Europe 2G</td></tr>
<tr><td>2G_FCC1</td><td>22h</td><td>1~11</td><td>US 2G</td></tr>
<tr><td>2G_MKK1</td><td>23h</td><td>1~13, 14</td><td>Japan 2G</td></tr>
<tr><td>2G_ETSI2</td><td>24h</td><td>10~13</td><td>France 2G</td></tr>
<tr><td>2G_Global</td><td>41h</td><td>1~13, 14</td><td>Global domain</td></tr>
</table></td><td>20h</td></tr>
<tr><td>B9h</td><td>Crystal Calibration</td><td>XTAL_K Value
Bit[5:0], Xi=Xo Range 0~3F h.
Bit[7:6]: reserved
FF h = 00 h</td><td>20h</td></tr>
</table>

Bytes	Contents	Description	Value
BAh	Thermal Meter	Thermal Meter Default Value System maker will calibrate a value and save it in EEPROM. Bit[7:0]: Thermal Meter Value	1Eh
BBh	Reserved	Reserved for Realtek.	00h
BCh	2G and 5G PA Type	2G PA Bit[7]: Path-D Internal/External PA 0h: Internal PA 1 h: External PA Bit[6]: Path-C Internal/External PA 0h: Internal PA 1h: External PA Bit[5]: Path-B Internal/External PA 0h: Internal PA 1h: External PA Bit[4]: Path-A Internal/External PA 0h: Internal PA 1h: External PA 5G PA Bit[3]: Path-D Internal/External PA 0h: Internal PA 1 h: External PA Bit[2]: Path-C Internal/External PA 0h: Internal PA 1h: External PA Bit[1]: Path-B Internal/External PA 0h: Internal PA 1h: External PA Bit[0]: Path-A Internal/External PA 0h: Internal PA 1h: External PA	00h
BDh	2G LNA Type and Gain Selection	Bit[2:0]: 2G path-A external LNA Gain, used to modify DIG mechanism 0h~7h: External LNA, 8~22dB with 2dB/step Bit[3]: 2G Path-A Internal/External LNA 0h: Internal LNA 1h: External LNA Bit[6:4]: 2G path-B external LNA Gain, used to modify DIG mechanism 0h~7h: External LNA, 8~22dB with 2dB/step Bit[7]: 2G Path-B Internal/External LNA 0h: Internal LNA 1h: External LNA	00h
BEh~C0h	Reserved	Reserved for Realtek.	FFh

Bytes	Contents	Description	Value
C1h	Board Options	Bit[2:0]: Regulatory selection. 0h: driver-defined maximum power offset for longer communication range. (refer to Power by rate table) 1h: Power limit table-defined maximum power offset range (refer to Power by rate table and Power limit table to take the smaler index value) 2h: not support power offset by rate (Don't refer to Power by rate table) 3h~7h: reserved Bit[3]: Non-interrupt Antenna Diversity 0: disable 1: enable Bit[4]: reserved Bit[7:5]: Board Type 0h: WiFi solo module 1h: WiFi+BT combo module 2h: PCIe Card 3h~7h: reserved.	29h
C2h	Feature Options	Bit[1:0]: function configuration of pin_LED0 and pin_LED1 Bit[3:2]: Link Speed shown in OS 0h: Current Tx PHY Rate 1h: Current Rx PHY Rate 2h: Maximum RX PHY Rate 3h: reserved Bit[4]: power down mode selection 0: radio off 1: power down Bit[5]: Enable bluetooth coexistence 0: Disable 1: Enable Bit[6]: Enable WoWLAN 0: Disable 1: Enable Bit[7]: Enable WAPI support 0: Disable 1: Enable	20h
C3h	BT Setting	Bit[0]: Total antenna number 0: 2-Antenna (default) 1: 1-Antenna Bit[7:3]: reserved	10h
C4h	Version	The EEPROM content version.	00h
C5h	Customer ID	Customer ID (0x00 and 0xFF are reserved for Realtek)	00h

Bytes	Contents	Description	Value
C6h	2G Tx BB Swing Setting	Bit[1:0]: 2G PathA OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB Bit[3:2]: 2G PathB OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB Bit[5:4]: 2G PathC OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB Bit[7:6]: 2G PathD OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB	00h
C7h	Reserved	Reserved for Realtek.	FFh
C8h	Tx Power Calibratior Rate	Bit[0]: 2G 40M Tx Power Calibrator Rate. 0h : HT40, MCS7 64QAM (default) 1h : VHT40, MCS9 256QAM Bit[1]: 5G 40M Tx Power Calibrator Rate. 0h : HT40, MCS7 64QAM (default) 1h : VHT40, MCS9 256QAM Bit[7:2]: reserved	00h
C9h	Reserved	Reserved for Realtek.	FFh
CAh	RFE Type	Bit[6:0]: RF Front-end Type 0h~Fh: reserved 10h: Fix-path with two antenna. (default) 11h: DPDT with two antenna. 12h: SPDT with single antenna. 13h: Coupler with single antenna. 14h~7Fh: reserved	10h
CBh~CFh	Reserved	Reserved for Realtek.	FFh

<table>
<tr><th>Bytes</th><th>Contents</th><th>Description</th><th>Value</th></tr>
<tr><td>D0h</td><td>CCCR</td><td>Bit[0]: SCSI ,CCCR 0x07[6]
Bit[1]:SDC , CCCR 0x08[0]
Bit[2]:SMB , CCCR 0x08[1]
Bit[3]:S4MI , CCCR 0x08[4]
Bit[4]:SMPC , CCCR 0x12[0]
Bit[5]:SHS , CCCR 0x13[0]
Bit[6]:SSDR50 , CCCR 0x14[0]
Bit[7]:SSDR104 , CCCR 0x14[1]</td><td>3Eh</td></tr>
<tr><td>D1h</td><td>CCCR&FBR</td><td>Bit[0]:SDDR50 , CCCR 0x14[2]
Bit[1]:SDTA , CCCR 0x15[0]
Bit[2]:SDTC , CCCR 0x15[1]
Bit[3]:SDTD , CCCR 0x15[2]
Bit[4]:SAI , CCCR 0x16[0]
Bit[5]: Init_skip, 0:need cmd 0 5 5 3 7 to enable Wifi ,(default)
1:skip
Bit[6~7]:reserve</td><td>10h</td></tr>
<tr><td>D2h</td><td></td><td>Bit[0]: SPS ,FBR 0x102[0]
Bit[1~3]:reserved
Bit[4~7]:PS3 ,FBR 0x102[4~7]</td><td>01h</td></tr>
<tr><td>D3h</td><td>CCCR</td><td><table><tr><th>Bit</th><th>Description</th></tr><tr><td>7:4</td><td>Reserved</td></tr><tr><td>3:0</td><td>CCCR Format Version number
0x02: CCCR/FBR Version 2.00</td></tr></table></td><td>02h</td></tr>
<tr><td>D4h</td><td>SDIO_MODE</td><td><table><tr><th>Bit</th><th>Description</th></tr><tr><td>7:4</td><td>SDx: SD Format Version number
0x02: SD physical Specification Version 2.00</td></tr><tr><td>3:0</td><td>SDIOx: SDIO Format Version number
0x03: SDIO physical Specification Version 2.00</td></tr></table>Note: SDIOx and SDx are in CCCR register.</td><td>23h</td></tr>
<tr><td>D5h~D7h</td><td>OCR</td><td>OCR value. Little Endian order.（This value must be consistent with CIS tuple value）</td><td>FF0000h</td></tr>
<tr><td>0xD8~0xE8</td><td>Common CIS dadta</td><td>Offset 68h~6Dh: CISTPL_MANFID
Value :0x20 04 4C 02 23 B7
Offset 6Eh~71h: CISTPL_FUNCID
Value :21 02 0C 00
Offset 72h~78h: CISTPL_FUNCE
Value :22 04 00 08 00 32 FF</td><td></td></tr>
</table>

Bytes	Contents	Description	Value
0xE9~0x119	Function 1 CIS Data	Offset 79h~7Ch: CISTPL_FUNCID Value :21 02 0C 00 Offset 7Dh~7Eh:CISTPL_FUNCE Value :22 2A Offset 7Fh~A9h: Value : 01 01 00 00 00 00 00 00 - 00 00 00 00 00 02 00 FF FF 00 00 00 00 00 00 00 - 00 00 00 00 00 00 00 00 00 00 EB 00 6E 01 00 00 - 00 00 FF	
0x11A~0x11F	Function 1 CIS Data MAC Address	MAC Address: After the auto-load command or hardware reset, the RTL8723AS loads MAC Addresses to MACID of the I/O registers of the RTL8723AS.	0123874C E000h

1.2 Bluetooth Controller EEPROM Contents Spec

Table 1.2 Bluetooth Controller EEPROM (eFuse) Contents

Bytes	Contents	Description	Value
00h	EFUSE_parameter	Reserved	00h
01h		Reserved	01h
02h		Reserved	00h
03h		Signature Field. 0xA5, fw uses efuse value. Otherwise, fw uses default value of Rom Code	A5h
04h ~ 07h	crystal_clk	Crystal clock	02625A00h
08h ~ 0Bh	SYS_log_uart_baudrate	Baud rate of system uart0 for debug log	0001C200h
0Ch ~ 0Fh	SYS_hci_uart_baudrate	Bit[31:21]: pll_sel Bit[20:16]: pll_d Bit[15:12]: ovsr Bit[11:0]: divisor Baud Rate : 1200, set 0x00009823 Baud Rate: 9600, set 0x00009104 Baud Rate : 57600, set 0x0000603F **Baud Rate : 115200, set 0x0000701D** Baud Rate : 230400, set 0x0000B00B Baud Rate : 460800, set 0x00006008 Baud Rate : 921600, set 0x00006004 Baud Rate : 3000000, set 0x00008001	0000701Dh

Bytes	Contents	Description	Value
10h ~ 13h	Rtl8723_data_uart_settings	Bit[0]: chk_bton_en use bton/baudrate_record if bton / baudrate_record!=0 Bit[1]: wr_bton_en enable write to bton/baudrate_record Bit[2]: baud_det_en enable baud rate detection funcation Bit[3]: baud_default_en 1: use default(RTL8723:115200), 0: use efuse baudrate Bit[8:4]: baud_det_timeout timeout_loops = 2^x, depends on host requirements Bit[9]: baud_det_timeout_en depends on host requirements Bit[10]: baud_est_use_original_buad_det_once Bit[11]: baud_record_at_rx_vendor_sync Bit[12]: hci_uart_mcr_rtsn Bit[13]: baud_est_baud_det_trial_redet_en Bit[14]: baud_est_delay_before_h5_state_check Bit[15]: buad_est_bypass_mon_valid_check Bit[16]: baud_record_at_h5_link_est Bit[17]: baud_est_baud_det_fail_redet_en Bit[18]: baud_est_use_original_buad_det_only Bit[19]: h5_sign_linkrst_signature Bit[20]: h5_linkrst_sign_fw_trig_wdg Bit[21]: h5_set_g_host_state set g_host_state when setting sleep_msg_state (to enable HCI C2H gating function) Bit[22]: tune_pll_sel_en	19EAC550h
		enable pll_sel tuning at SPI mode	

Bytes	Contents	Description	Value
		Bit[23]: h4_err_intr_en Bit[24]: en0_before_set_en 1(recommended): disable uart before UART initialization setting in uart_set_baud_clk_RTL8723(); to avoid glitch effects Bit[25]: err_recov_en 1: call hci_uart_reset_init_RTL8723 (re_init_flag = 1) when uart error Bit[26]: baud_redet_en valid when baud_det_en = 1, (when re_init_flag = 1) 1: detect baudrate 0: no re-detection Bit[27]: det_wait_en (when re_init_flag = 0) 1: wait for detection results, 0: bypass the waiting loops Bit[28]: redet_wait_en (when re_init_flag = 1) 1: wait for detection results, 0: bypass the waiting loops; valid when g_hci_uart_baud_redet_en = 1 Bit[29]: uart_h5_go_sleep_backup_en 1: enable h5 status backup when H5 go sleep Bit[30]: err_event_err_code_opt 1: error code = HARDWARE_FAILURE_ERROR_RTK_H4 to distinguish with other Hardware Error Codes Bit[31]: h5_linkfail_clr_unack	

Bytes	Contents	Description	Value
14h ~ 17h	Rtl8723_data_uart_settings2	Bit[0] : h5_en If set to 1, enable UART H5 transport. If set to 0, enable UART H4 transport Bit[1] : h5_active_sync If set to 1, do not wait HOST SYNC message before sending the first SYNC in UNINITIALIZED STATE Bit[2] : h5_ignore_sync If set to 1, ignore SYNC at ACTIVE STATE Bit[3] : h5_force_oof_ctrl If set to 1, force out-of-frame software flow control ON Bit[4] : h5_force_no_oof if set to 1, force out-of-frame software flow control OFF Bit[7:5] : h5_retry_limit LinkFailure: 2^(x+1) retries; LinkAlarm: 2^(x) retries Bit[10:8] : h5_resend_to_val 0~5; resend(retry) period: 2^(x+9) T_char; 115200: T_char ~ 95.5us; 921600: T_char ~ 11.9us Bit[13:11] : h5_sync_to_val 0~4; link establishment period; 2^(2x+6) T_char; 115200: T_char ~ 95.5us; 921600: T_char ~ 11.9us Bit[15:14] : h5_ack_to_val 0~3; pure ACK wait time: 2^(2x+2) T_char; 115200: T_char ~ 95.5us; 921600: T_char ~ 11.9us Bit[17:16] : h5_wake_to_val WAKEUP period; 2^(2x+2) T_char; 115200: T_char ~ 95.5us; 921600: T_char ~ 11.9us	AFF11BE0h

Bytes	Contents	Description	Value
		Bit[19:18] : h5_host_to_val HCI TX abort timeout(to avoid hangup bugs); 2^(2x+10) characters; 3: never timeout Bit[29:20] : h5_int_en Bit[30] : h5_lowpow_sleep_msg_wait_en, valid when h5_lowpow_sleep_msg_en = 1; 0: exit hci_uart_h5_send_sleep_msg_wait_done() without waiting done Bit[31] : h5_retry_state_clr_when_trx 1: clear h5_retry_alarm_state and h5_retry_fail_state when HCI DMA TRX is active	
18h ~ 1Bh	Rtl8723_data_uart_settings3	Bit[0] : parity_en Bit[1] : parity_even Bit[2] : hw_fctrl_on Bit[5:3] : long_break_duration 2^(x)*10ms Bit[8:6] : h5_poll_wake_duration 7: persistent poll; else: 2^(2x)*10ms Bit[10:9] : h5_retry_alarm_opt 0: nothing, 1: sent short break, 2: send long break; 3: poll_wake Bit[12:11] : h5_retry_fail_opt 0: nothing, 1: sent short break, 2: send long break; 3: poll_wake Bit[14:13] : h5_lowpow_wakeup_opt if (sleep_msg_state==1 && RX is to be send to HCI DMA), 0: nothing, 1: sent short break, 2: send long break; 3: poll_wake	0BA40158h

Bytes	Contents	Description	Value
		Bit[15] : h5_lowpow_sleep_msg_en 1: send_sleep_msg_and_wait_done() before go to sleep // TODO: need extra efuse for LPS mode? Bit[16] : h5_scounrel_force_en Bit[17] : h5_scounrel_force_value valid when force_en = 1, 0: reliable, 1: unreliable Bit[18] : h5_resend_time_adapt_en enable retry_limit adaption according to baudrate and resend_target; Should not be enabled when "baud_det_en & (det_wait_en = 0 | det_timeout_en)" ==> Baudrate may be strange Bit[20:19] : h5_resend_target valid when resend_time_adapt_en = 1; target resend timing for adaption = 250ms/2^x Bit[23:21] : h5_resend_time_adapt_max the maximum adapted resend_to_val; Bit[26:24] : h5_resend_time_adapt_min the minimum adapted resend_to_val Bit[27] : h5_retry_limit_adapt_en valid when resend_time_adapt_en = 1; enable retry_limit adaption according baud and resend_to_val Bit[28] : h5_trx_active_mask_opt to clear sleep_mst_state: 0: CMD/ACL/EVT, 1: CMD/ACL/EVT + SCO TX Bit[31:29] : err_send_event_delayw1c_opt 0: no HW Err Event + N0 delayed W1C, 1: HW Err Event +	

Bytes	Contents	Description	Value
		N0 delayed W1C, else: HW Err Event + delayed W1C with delay = 2^(x)*2.5ms	
1Ch ~ 1Fh	efuse_lps_setting_1_d32	Bit[2:0] : dsm_guard_interval // 7: 16; else: 2+x Bit[4:3] : sm_guard_interval // 3: 16; else: 2+x Bit[6:5] : min_sm_interval // 2^(x+1) Bit[8:7] : min_dsm_interval // 2^(x+1) Bit[10:9] : dsm_drift_scaling // DSM_DRIFT/2^x Bit[11] : delay625us_before_bton_lps_req Bit[12] : new_tol_cal Bit[13] : sniff_tol_adjust Bit[15:14] : min_sniff_int_for_xtol // 10*2^x slots Bit[31:16] : lps_task_mask	01FFE8B2h
20h ~ 23h	efuse_lps_setting_2_d32	Bit[1:0] : lps_pri //0: CH_AS_TASK_PRI, else: LC_RX_TASK_PRI Bit[2] : timer2_lps_on Bit[3] : sniff_lps_on Bit[4] : timer2_mode_sel // (0) orig (1) enable cch function Bit[5] : timer2_scan_en Bit[6] : lps_enable_hci_dma_wakeup_isr Bit[8:7] : sniff_xtol_scaling Bit[9] : sniff_xtol_scaling_for_park_hold Bit[11:10] : timer2_kill_scan_delay_ms // (2^(x+1)) msec Bit[12] : timer2_mode0_opt // (0) orig (1) chris timer2 with yilin function Bit[13] : sniff_mode_sel // (0) orig (1) enable cch function Bit[14] : sniff_scan_en Bit[18:15] : sm_scan_per	8B136430h

Bytes	Contents	Description	Value

		// (sniff interval >>x) as period
		Bit[20:19] : sm_scan_per_min
		// (2^x) period
		Bit[24:21] : dsm_scan_per
		// (sniff interval >>x) as period
		Bit[26:25] : dsm_scan_per_min
		// (2^x) period
		Bit[27] : force_exit_sm_en
		Bit[28] : issc_nope_en
		Bit[30:29] : issc_nope_num
		// return (x+1)
		Bit[31] : timer2_no_scan_wakeup_en
		//timer2 with no scan enable need to wakeup enable	

24h ~ 27h	efuse_lps_setting_3_d32	Bit[15:0] : timer2_lps_isr_mask Bit[16] : timer2_reset_at_uart_isr_en Bit[17] : sniff_lps_lmp_to Bit[18] : sniff_lps_sup_to Bit[19] : iot_sco_can_overlap // sco slot can overlap to sniff Bit[20] : lc_init_radio_osc_delay_opt Bit[22:21] : sniff_wakeup_xtol_opt // 0: original, 1: wakeup_inst -= tol, 2(recommended): wakeup_inst -= (tol-tol_prev) Bit[23] : iot_ralink_tid_no_check Bit[24] : iot_ralink_donot_feature_req Bit[25] : iot_sco_noise_pcm_send0: Bit[27:26] : iot_sco_noise_no_sco_count Bit[28] : iot_issc_inq_rssi Bit[29] : iot_issc_rmr_par Bit[30] : esco_nego_by_other Bit[31] : use_ext_32k	67DF030Ch
28h ~ 2Bh	lps_mode_max_time	Unit:10 ms	00000258h
2Ch ~ 2Dh	power_option	Bit[15:13]: Reserved Bit[12]: EF_SOP_ERCK Bit[11]: EF_SOP_ACKF Bit[10]: EF_LOP_ACKF	02B5h

Bytes	Contents	Description	Value
		Bit[9]: SOP_ESWR Bit[8]: SOP_PWMM Bit[7]: SOP_EECK Bit[6]: SOP_EXTL Bit[5]: SOP_EBNG Bit[4]: LOP_ESWR Bit[3]: LOP_PWMM Bit[2]: LOP_EECK Bit[1]: LOP_EXTL Bit[0]: LOP_EBNG	
2Eh ~ 2Fh	power_seq_param	Bit[15]: EF_PCM_PULL_LOW_PDN_SUS_3 Bit[14]: EF_PCM_PULL_LOW_PDN_SUS_2 Bit[13]: EF_PCM_PULL_LOW_PDN_SUS_1 Bit[12]: EF_PCM_PULL_LOW_PDN_SUS_0 Bit[11]: EF_PCM_PULL_LOW_ACT_3 Bit[10]: EF_PCM_PULL_LOW_ACT_2 Bit[9]: EF_PCM_PULL_LOW_ACT_1 Bit[8]: EF_PCM_PULL_LOW_ACT_0 Bit[7]: EF_PCM_PULL_LOW_EN Bit[6]: UART_HCI_RESET_EN Bit[5]: PTA_ANTENNA_STATUS Bit[4]: FORCE_MASK_WIFI_CH Bit[3]: EFUSE_POWER_OPTION_EN Bit[2]: USB_SIE_NY Bit[1]: BT_CORE_LDO_STANDYBY (EXPIRED) Bit[0]: LPS_TIMER	0020h
30h ~ 31h	general_control	Bit[15:13]: pdn_sus_fa_recov_delay default 0, (2 is recommended), delay = 5us * 2^x Bit[12]: pdn_sus_fa_recov_en default 0 (1 is recommended), 1: recovery after execute power-down for false-alarm case) Bit[11]: PDN_DELAY_TIME_UNIT 0 means MS, 1 means US Bit[10]: LOG_UART_RX_EN Bit[9]: AFE_LDO_HW_EN (EXPIRED) Bit[8]: LED_VENDOR_EN	5240h

Bytes	Contents	Description	Value
		Bit[7]: LED_IDLE_GLITTER_EN Bit[6]: LED_POLARITY Bit[5]: UART_H5_WAKEUP_EN Bit[4]: WAKE_UP_GPIO_POLARITY Bit[3]: GPIO_FOR_LED_FUN_EN Bit[2:1]: WAKE_UP_GPIO_TYPE 0: undefined 1: BT_WAKE_HOST (P_GPIO14) 2: LED0 (DesignWare GPIO4) 3: LED1 (DesignWare GPIO4) Bit[0]: GPIO_FOR_WAKE_UP_EN	
32h ~ 33h	default_max_flush_time		0064h
34h	mailbox_max_timeout		1Eh
35h	gpio_wake_up_time		01h
36h	pta_pkt_unit		03h
37h	control_time_parameter	Bit[7:4]: Wakeup Poll Time Bit[3:0]: retry index	24h
38h	pre_detect_pkt_num		03h
39h	pdn_delay_tim_byte0	Delay Time to exit Power Down state	03h
3Ah	pdn_delay_tim_byte1	Delay Time of GPIO Software Debouncing (unit: ms)	02h
3Bh	efuse_pow_setting_2_d8	[0]: hci_reset_init_power_var 1: initialize power-related variable at HCI_RESET [1]: power_on_check_init_power_var 1: initialize power-related variable at REBOOT gpio_power_on_check [2]: gpio_host_wake_bt_en 1: enable GPIO output [3]: gpio_host_wake_bt_polarity 1: active high, 0: active low **[4]: disable_force_usb_r_lop_extl_en** valid when lop_sop_low_power_setting_en = 0 0: force r_LOP_EXTL = 1 for USB interface **[5]: bt_wake_host_init_opt** 1: initialized as g_host_state; 0: (!g_host_state) **[6]: gpiointr_ignore_sus** 1: ignore GpioIntrHandler() bt_sus_en	80h

Bytes	Contents	Description	Value
		[7]: avoid_pdn_with_sus 1: ignore GpioIntrHandler() bt_sus_en when bt_pdn_en	
3Ch ~ 41h	bt_bd_addr[6]	BT BD address (unique in each device)	xxh, xxh, xxh, 4Ch, E0h, 00h
42h ~ 81h	bt_local_name[64]	BT local name	'R', 'T', 'K, '_', 'B', 'T', '_', '4', '.', '0', , '\0', FFh (x 53)
82h ~ 89h	bt_master_piconet_fea[8]	BT piconet feature mask (depend on supported Bluetooth spec)	FFh, FFh, FFh, FEh, DBh, FFh, 7Bh, 87h
8Ah ~ 99h	bt_security_key[16]	Security Key. To use with our Bluetooth driver in Realtek's authentication procedure	FFh (x16)
9Ah	bt_country_code	BT country code	00h
9Bh	efuse_lps_setting_4_d8	Bit[0] : lps_chk_g_host_wake_bt:1 // default = 0 Bit[1] : lps_use_state:1 // default = 1 Bit[2] : whql_test_2sco:1 // default = 0 Bit[3] : lps_stop_afh_timer:1 // default = 0 Bit[4] : lps_use_state_fast_lps:1 // default = 1 Bit[5] : lps_use_intr:1 // default = 0 Bit[6] : lps_isr_mask_check_isr_switch:1 // default = 0 Bit[7] : lps_pow_ctrl_intr_check_isr_switch:1 // default=0	12h
9Ch	efuse_pow_setting_1_d8	Bit[0]: bt_pdn_power_on_check_dis default 0, 0: check GPIO11(BT_DIS_N) in gpio_power_on_check(); Bit[1]: bt_suspend_power_on_check_dis:1 default 0, 0: check and execute SUSPEND Status in gpio_power_on_check() Bit[2]: init_bt_never_close_sram_pwr default 0, 1: Never close sram power fpr some reason Bit[3]: bt_fun_sts_power_on_check_en	00h

Bytes	Contents	Description	Value
		default 0, 1: check BT Functioin Status (OFF==>POWER-DOWN) in gpio_power_on_check() Bit[4] force_hw_pdn_en default 0, To assume EFUSE_HW_PDN_EN is 1 regardless Vendor0x44[26] Vendor 0x44[27]: 0/1: GPIO11 acts as HWPDN/RFOFF Function **Bit[5]: turn_off_ck120m_at_lps** default 0, 1: ck120m off when entering LPS, ck120m on when exiting from LPS **Bit[6]: lop_sop_low_power_setting_en** default 0, 1 is preferred; 1: init r_SOP_xxx and r_LOP_xxx for LOW POWER CONSUMPTION, then dynamically change the setting Bit[7]: bt_sus_power_on_check_execute default 0, 1: execulte bt_sus_en at gpio_power_on_check()	
9Dh	bt_default_tx_power_index_minus	BT default tx power index = BT maximum tx power index – bt_default_tx_power_index_minus	02h
9Eh ~ 9Fh	bt_manufacturer_name	BT manufacture name	005Dh
A0h ~ A1h	bt_sleep_mode_threshold	BT sleep mode threshold	FFFEh
A2h ~ A3h	bt_deep_sleep_mode_threshold	BT deep sleep mode threshold	0120h
A4h ~ A5h	bt_def_link_policy_settings	Default Link Policy Settings (refer HCI spec)	0000h
A6h ~ A7h	bt_t_poll_slave	Common Tpoll value	0024h
A8h ~ A9h	bt_t_poll	Qos Tpoll value	0024h
AAh ~ ABh	bt_supervision_timeout	BT supervision timeout value	7D00h
ACh ~ ADh	bt_page_timeout	BT page timeout value	2000h
AEh ~ AFh	bt_conn_accept_timeout	BT connection accept timeout value	1F40h
B0h ~ B1h	bt_read_buffer_size	BT read buffer size	0334h
B2h ~ B3h	bt_page_scan_interval	BT page scan interval value	0800h
B4h ~ B5h	bt_page_scan_window	BT page scan window value	0012h
B6h ~ B7h	bt_inquiry_scan_interval	BT inquiry scan interval value	1000h

Bytes	Contents	Description	Value
B8h ~ B9h	bt_inquiry_scan_window	BT inquiry scan window value	0012h
BAh ~ BBh	bt_hold_max_interval	BT hold maximum interval value	FFFFh
BCh ~ BDh	bt_hold_min_interval	Bt hold minimum interval value	0001h
BEh ~ BFh	bt_sniff_max_interval	BT sniff maximum interval value	FFFFh
C0h ~ C1h	bt_sniff_min_interval	BT sniff minimum interval value	0001h
C2h ~ C3h	bt_beacon_max_interval	BT beacon maximum interval value	2000h
C4h ~ C5h	bt_beacon_min_interval	BT beacon minimum interval value	00C0h
C6h ~ C7h	bt_priority_low	The Bluewiz Priority Low Register	0000h
C8h ~ C9h	bt_priority_high	The Bluewiz Priority High Register	0000h
CAh ~ CBh	bt_priority_3	The Bluewiz Priority 3 Register Bit[7:0]: The Bluewiz Priority 3 Register Default Setting Bit[8]: IS_HARDWARE_ERR_EVENT_TO_HOST_WHEN_HOST_ACL ? Bit[9]: IS_EARLY_TX_TOGGLE ? Bit[11:10]: NUM_RETX_TO_PAUSE_ESCO Bit[13:12]: PAUSE_ESCO_INTERVAL Bit[14]: test with MUTE ? Bit[15]: EN_FW_FIX_SCO_NAK_HID	1A00h
CCh ~ CFh	bt_class_of_device	BT class of device	00000000h
D0h ~ D3h	bt_func_support_policy	bit[0]: support BT3.0 bit[1]: support BT4.0 (if bit[0] and bit[1] both are 0, we will support BT2.1/EDR only) bit[2]: support scatternet bit[3]: allow inq scan after conn bit[4]: power saving enable bit[5]: BQB mode bit[6]: support hci log packet bit[7]: support WPAN LED (Mini-Card Spec) bit[8]: decide 2Mbps packet type first ? bit[14:9]: max log event packet length (4 byte unit) bit[15]: no output uart log message ? bit[29:16]: max log acl packet length (4 byte unit) bit[30]: use pta meter ? bit[31]: allow aggressive hci rx dma	C0807FDFh

Bytes	Contents	Description	Value
D4h ~ D7h	bt_le_multistate_bm_ldw	BT LE supported multiple states by bitmap (refer the BT4.0 spec)	1FFFFFFFh
D8h ~ DBh	bt_le_fw_policy	BT LE supported fw policy Bit[0]: g_le_conn_interval_auto_update_en Bit[1]: g_le_conn_interval_default_en Bit[13:2]: g_le_conn_interval_default Bit[14]: g_le_auto_cal_bw_en = 1 Bit[17:15]: g_le_slot_avoid_for_sco = 0 Bit[18]: IS_DAPE_TEST_MODIFY_AFH = 1 Bit[19]: LE_LEGACY_COMPENSATE_SLOT Bit[20]: BLOCK_LEGACY_WHEN_LE Bit[23:21]: BLOCK_SLOT_NUM_5SLOT Bit[26:24]: BLOCK_SLOT_NUM_3SLOT Bit[28:27]: LE_MAX_NUM_OF_ADV_REPORT_OPTION Bit[31:29]: LEGACY_INQUIRY_RESERVED_12SLOT	5A904018h
DCh ~ DFh	bt_func_support_policy_ext	bit[0]: ignore wifi alive detect bit[1]: support 3dg ? bit[2]: support enhanced cpu sleep mode ? bit[3]: support dual bzdma hci cmds to handle race condition when two le connection events are overlap bit[4]: do not block legacy retransmitted packet for le bit[5]: do not block legacy slave traffic for le bit[8:6]: PAUSE_LE_INTERVAL bit[10:9]: BLOCK_NUM_OF_LEGACY_WHEN_BR bit[11]: PAUSE_SCO_FOR_LE ? bit[12]: IS_NO_LE_TX_THRESHOLD_FOR_MULTI_CE bit[13]: IS_NO_LE_RX_THRESHOLD_FOR_MULTI_CE bit[14]: IS_NO_AFH_SCO_SIMULATE_ACL_PKT bit[15]: SHORTEN_MASTER_SNIFF_TIMEOUT_VAL bit[16]: IS_EVENT_REORDER_FOR_ANY_INTERFACE bit[17]: LE_AUTO_UPDT_WHEN_SLOT_CONFLICT_AFTER_CONN_UPDT bit[21:18]: g_le_use_interval_slot_pair bit[31:22]: reserved	00168E08h

Bytes	Contents	Description	Value
E0h ~ E1h	pta_default_setting	pta register default setting	0220h
E2h	bt_global_slot_min_sniff_int v		1Eh
E3h ~ EDh	-	Reserved	FFh (x11)
EEh	HCI_DMA_EnhanCtrl	Bit[0]: Enable Bit[1]: HCI Hardware Error Event Return Enable Bit[2]: HCI DMA Enhancement Function Interrupt Enable Bit[3]: HCI DMA Enhancement Function(CMD) Interrupt Enable Bit[4]: HCI Hardware_Reset Event(CMD) return Enable Bit[7:5]: reserved	03h
EFh	HCI_DMA_EnhanRsvd0	reserved	FFh
F0h	USB_LPM_Allow	Bit[0]: USB LPM Disable:0x0, Enable:0x1 Bit[1]: Control by F/W: 0, Control by Driver: 1	00h
F1h	USB_LPM_HIRDBESL_Th rd	HIRD/BESL Threshold Value. HIRD: bit7~4, BESL: bit3~0	FFh
F2h	USB_LPM_Rsvd0	USB LPM Reserved Parameter0	FFh
F3h	USB_LPM_Rsvd1	USB LPM Reserved Parameter1	FFh
F4h	hci_excodec_state	HCI:0x0 PCM External CODEC:0x1 I2 External CODEC:0x2	00h
F5h	pcm_ex_codec_format	Linear: 0x00, u-Law: 0x01, A-Law: 0x02, CVSD: 0x03	00h
F6h	pcm_ex_codec_format_8bit	Codec 8-bit enable. Disable: 0x00, Enable: 0x01	00h
F7h	Scoconv	Sco Data format	00h
F8h ~ F9h	pcm_if_ctrl1	PCM I/F Ctrl1	70C5h
FAh ~ FBh	pcm_if_ctrl2	PCM I/F Ctrl2	0000h
FCh	bw_rf_radio_sys_clk_sel	Select sys clock	09h
FDh	bw_rf_osc_delay	Oscillator Start up delay	08h
FEh	bw_rf_low_clk_frac	Select low power clock (1:32KHz, 0:32.768KHz)	01h
FFh ~ 101h	Bw_rf_reserved[3]	Reserved	FFFFFFh
102h ~ 103h	bw_rf_min_rssi_dbm	The lower limit of Golden Receive Power Range (signed integer, units: dBm)	FFD8h
104h ~ 105h	bw_rf_max_rssi_dbm	The upper limit of Golden Receive Power Range (signed integer, units: dBm)	FFE2h
106h ~ 107h	bw_rf_delay_vals_0	Initiate Bluewiz Register (0xC6):	D5C8h

Bytes	Contents	Description	Value
		Half-slot TX/RX radio processing delays: bit[15:8] for Tx and bit[7:0] for Rx	
108h ~ 109h	bw_rf_delay_vals_1	Initiate Bluewiz Register (0xC8): Full-slot TX/RX radio processing delays: bit[15:8] for Tx and bit[7:0] for Rx	D5C8h
10Ah ~ 10Bh	bw_rf_delay_vals_2	Initiate Bluewiz Register (0xCA): Half-slot TX/RX PLL lock delays: bit[15:8] for Tx and bit[7:0] for Rx	8989h
10Ch ~ 10Dh	bw_rf_delay_vals_3	Initiate Bluewiz Register (0xCC): Full-slot TX/RX PLL lock delays: bit[15:8] for Tx and bit[7:0] for Rx	8989h
10Eh ~ 10Fh	bw_rf_delay_vals_4	Initiate Bluewiz Register (0xCE): Correlator disable time for half-slot timing:bit[10:0]	0536h
110h ~ 111h	bw_rf_delay_vals_5	Initiate Bluewiz Register (0xD0): FHS/1st ID resp delay for INQ SCAN/PAGE SCAN: bit[8:0]	214Dh
112h ~ 113h	bw_rf_delay_vals_6	Initiate Bluewiz Register (0xD2): FHS listening delay for slave PAGE RESPONSE: bit[8:0]	2144h
114h ~ 115h	bw_rf_delay_vals_7	Initiate Bluewiz Register (0xD4): 2nd ID response delay adjustment for slave: bit[14:10] load_value2 and bit[9:0] slave response delay	014Ah
116h ~ 117h	bw_rf_delay_vals_8	Initiate Bluewiz Register (0xC2): Correlator threshold register: bit[15:8] sync sequence threshold and bit[6:0] access code threshold	933Ch
118h ~ 119h	bw_rf_delay_vals_9	Reserved	FFFFh
11Ah ~ 11Bh	Le_ce_early_int_time	To set the duration before the instant of the connection event and hw can trigger early interrupt at this time. Bit[9:0]: micro second (valid : 0 ~ 624 us) Bit[15:10]: 625 us slot number	0168h
11Ch ~ 11Dh	Le_trx_on_delay	Bit[15:8] rxon_delay (us) Bit[7:0] txon_delay (us)	DCDCh
11Eh ~ 11Fh	Le_rx_turnaround_delay	Bit[15:8] rx2rx_delay (us) Bit[7:0] rx2tx_delay (us)	3286h
120h ~ 121h	Le_tx_turnaround_delay	Bit[13:8] txon_early (us) Bit[7:0] tx2rx_delay (us)	1083h
122h ~ 123h	Le_ce_rx_timeout_delay	Bit[11:8] txon_ext (us) Bit[7:0] rx_timeout_delay (us)	0164h

Bytes	Contents	Description	Value
124h ~ 125h	le_rx_search_timeout_value		01F0h
126h ~ 127h	le_clock_compensate		0147h
128h	rtk_afh_mechanism_enable	To enable RTK AFH mechanism or not, 1: enable	01h
129h	rtk_afh_bt_psd_enable	To enable BT PSD mechanism or not. 1 : enable	00h
12Ah	min_channels_by_rtk	Minimum good channels requirement for AFH normal state.	1Ch
12Bh	rtk_afh_using_slave_report	To use the slave channel classification information or not, 1: enable	00h
12Ch	rtk_afh_wlan_psd_enable	To use WLAN PSD report to generate AFH map (In BT only, must set to 0)	00h
12Dh	max_afh_execute_times	Max execute times for normal state	64h
12Eh	afh_execute_times_I	Execute times I for normal state	32h
12Fh	afh_execute_times_II	Execute times II for normal state	19h
130h	afh_execute_times_III	Execute times III for normal state	0Ch
131h	afh_execute_times_IV	Execute times IV for normal state	05h
132h	min_afh_execute_times	Min Execute times for normal state	03h
133h	wlan_gap_threshold	To check wlan interference or not	0Ah
134h ~ 135h	score_threshold	The criterion to decide the channel as good channel by step1 of AFH normal state	0000h
136h	afh_check_wifi_alive_count	If BT feels WiFi is not alive, it can try to check WiFi is alive or not periodically. This field can set the period value (unit: 10ms). Note: If the scenario is BT only, this field can set to zero.	0Ah
137h	trk_afh_score_thres_sco	signed char. The score of sco threshold (x 4)	E7h
138h	trk_afh_score_thres_sco_i	signed char. The score of sco threshold I (x 16)	EDh
139h	trk_afh_score_thres_sco_ii	signed char. The score of sco threshold II (x 16)	DAh
13Ah ~ 159h	EFuse_PHYInit_ TxGainTable[32]	RF Tx Gain Table One unit is in 8-bit width	02h, 03h, 04h, 05h, 06h, 0Dh, 0Eh, 15h, 16h, 1Dh, 1Eh, 2Eh, 37h, 3Fh, FFh, FFh, FFh, FFh, FFh, FFh,

Bytes	Contents	Description	Value
			FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh
15Ah	EFuse_PHYInit_ MaxTxIndex	Bit[4:0]: Tx Gain Table Length, Max Tx Gain index of each rate can't exceed this value Bit[7:5]:reserved	08h
15Bh	EFuse_PHYInit_ MaxTxGain1M	Max Tx Gain Index for 1M	07h
15Ch	EFuse_PHYInit_ MaxTxGain2M	Max Tx Gain Index for 2M	07h
15Dh	EFuse_PHYInit_ MaxTxGain3M	Max Tx Gain Index for 3M	07h
15Eh	EFuse_PHYInit_ MaxTxGainLE	Max Tx Gain Index for LE	07h
15Fh	EFuse_PHYInit_ TxGainStep	Bit[2:0]: the Gain Step difference Bit[7:3]: reserved	01h
160h	EFuse_PHYInit_ TxScaleFactor	Tx Scaling Factor: 0 ~ 15	0Ah
161h	EFuse_PHYInit_ TxDACCurrent	DAC Current: 0 ~ 31	15h
162h – 163h	EFuse_PHYInit_Gain0Stop	LNA group 0 gain and stop index	2034h
164h – 165h	EFuse_PHYInit_Gain0Start	LNA group 0 gain and start index	361Eh
166h – 167h	EFuse_PHYInit_Gain1Start	LNA group 1 gain and start index	7517h
168h – 169h	EFuse_PHYInit_Gain2Start	LNA group 2 gain and start index	9510h
16Ah – 16Bh	EFuse_PHYInit_Gain3Start	LNA group 3 gain and start index [15:13]: LNA Gain Setting [12:8]: PGA Gain Setting [7:0]: Start Index	B60Ch
16Ch	EFuse_IQK_Settings (EFuse_IQK_Enable / EFuse_IQK_TxIQKEn / EFuse_IQK_RxIQKEn / EFuse_IQK_Modified/	Bit[0]: EFuse_IQK_Enable. Enable IQK ? (1/0: Enable/Disable) Bit[1]: EFuse_IQK_TxIQKEn. Enable Tx IQK and LOK ? (1/0: Enable/Disable) Bit[2]: EFuse_IQK_RxIQKEn.	00h

Bytes	Contents	Description	Value
	EFuse_IQK_Delay)	Enable Rx IQK ? (1/0: Enable/Disable) Bit[3]: EFuse_IQK_Modified. IQK result modified ? (1/0: YES/NO) Bit[7:4]: EFuse_IQK_Delay IQK delay in 10ms unit	
16Dh	EFuse_IQK_RFChL	Which Low-Channel ? (value: 0~78)	0Ah
16Eh	EFuse_IQK_RFChH	Which High-Channel ? (value: 0~78)	46h
16Fh	EFuse_IQK_TxGainL	Low-Channel Tx Gain (value:0x00~0xFF)	71h
170h	EFuse_IQK_TxGainH	High-Channel Tx Gain (value:0x00~0xFF)	71h
171h	EFuse_IQK_RxGain	Rx Gain (Value: 0x00~0xff)	8Bh
172h	EFuse_IQK_ErrorTh	Error threshold for Tx IMR result validation (Value: 0 ~ 15)	03h
173h	EFuse_IQK_LoadExtSetup	Do code patch in IQK setup (1/0: YES/NO)	00h
174h - 175h	EFuse_IQK_TxIMRDefault	Default TxIMR if IQK fail	0040h
176h – 177h	EFuse_IQK_RxIMRDefault	Default RxIMR if IQK fail	E08Bh
178h – 179h	EFuse_IQK_LOKLDfault	Default Low-Ch LOK if IQK fail	9200h
17Ah – 17Bh	EFuse_IQK_LOKHDefault	Default High-Ch LOK if IQK fail	9200h
17Ch – 17Dh	EFuse_IQK_RxAGC	Rx IQK AGC code	0000h
17Eh – 17Fh	EFuse_IQK_IQKPara	IQK setup parameters	108Ah
180h	EFuse_TxPowerTrack_En	Enable Tx Power Tracking ? (1/0: Enable/Disable)	00h
181h	EFuse_ThermalDefault	Bit[5:0]: Default thermal meter value Bit[7:6]: reserved	0Ch
182h	EFuse_Thermal_ UpdateInterval	Thermal meter timer interval:1 ~ 63 second, 0→disable timer update	05h
183h	EFuse_TxPowerTrack_ ThermalDelta	Thermal meter value delta	03h
184h – 190h	EFuse_TxPowerTrack_ TxGain [13]	Tx Power compensation table	F9h, FAh, FCh, 06h, 07h, 09h, 0Ah, 0Ch, 0Eh, 17h, 19h, 1Bh, 1Dh
191h	EFuse_CFOTrack_En	Enable CFO Tracking ? (1/0: Enable/Disable)	00h
192h	EFuse_CFOTrack_ ThermalDelta	Bit[5:0]: Thermal meter value delta Bit[7:6]: reserved	03h
193h – 19Fh	EFuse_CFOTrack_Cap[13]	Bit[5:0]: Cap offset table Bit[7:6]: reserved	74h, 00h, 00h, 00h, 00h, 00h,

Bytes	Contents	Description	Value
			00h, 00h, 00h, 00h, 07h, 10h, 1Fh
1A0h	EFuse_RxGainTrack_En	Enable Rx Gain Tracking ? (1/0: Enable/Disable)	00h
1A1h	EFuse_RxGainTrack_ ThermalDelta	Bit[5:0]: Thermal meter value delta Bit[7:6]: reserved	03h
1A2h ~1BBh	EFuse_RxGainTrack_ Para[13]	Bit[5:0]: Mixer para, mapping to RF register 0x16[13:8] Bit[8:6]: LNA para-1, mapping to RF register 0x17[7:5] Bit[10:9]: LNA para, mapping to RF register 0x17[15:14] Bit[15:11]: reserved	04C1h, 0441h, 0401h, 02C1h, 0241h, 0201h, 04C1h, 0441h, 0401h, 02C1h, 0241h, 0201h, 04C1h
1BCh	EFuse_ReRFCal_ ThermalDelta	Bit[5:0]: The difference of Thermal value for RF Re-Calibration Bit[7:6]: reserved	0Ah
1BDh	EFuse_ReRFCal_Settings (EFuse_ReRFCal_LCKEn / EFuse_ReRFCal_RCKEn / EFuse_ReRFCal_PDKEn / EFuse_ReRFCal_IQKEn)	Bit[0]: EFuse_ReRFCal_LCKEn Enable Re-LCK ? (1/0 means Enable/Disable) Bit[1]: EFuse_ReRFCal_RCKEn Enable Re-RCK ? (1/0 means Enable/Disable) Bit[2]: EFuse_ReRFCal_PDKEn Enable Re-PDK ? (1/0 means Enable/Disable) Bit[3]: EFuse_ReRFCal_IQKEn Enable Re-IQK ? (1/0 means Enable/Disable) Bit[7:4]: reserved	00h
1BEh	-	Reserved	FFh
1BFh	-	Reserved	FFh
1C0h ~ 1C1h	EFuse_TxPowerTrack_ TxGain_Lbond[2]	Tx Power compensation table	F8h, F9h
1C2h ~ 1C3h	EFuse_TxPowerTrack_ TxGain_Hbond[2]	Tx Power compensation table	1Fh, 1Fh
1C4h ~ 1C5h	EFuse_CFOTrack_Cap_	Bit[5:0]: Cap offset table	6Eh, 74h

Bytes	Contents	Description	Value
	Lbond[2]	Bit[7:6]: reserved	
1C6h ~ 1C7h	EFuse_CFOTrack_Cap_ Hbond[2]	Bit[5:0]: Cap offset table Bit[7:6]: reserved	1Fh, 1Fh
1C8h ~ 1C9h	EFuse_PHYInit_Gain4Start	LNA group 4 gain and start index	DC00h
1CAh ~ 1CBh	EFuse_PHYInit_Gain5Start	LNA group 5 gain and start index	0000h
1CCh ~ 1CDh	EFuse_PHYInit_Gain6Start	LNA group 6 gain and start index	0000h
1CEh ~ 1CFh	EFuse_PHYInit_Gain7Start	LNA group 7 gain and start index	0000h
1D0h	efuse_modem_setting_1_d8	[7:0]: reserved	0Ch
1D1h	efuse_pow_setting_3_d8	Bit[0] gpio_pdn_intr_lvl_trig_en 1: set as BT_DIS_N as level trigger, 0: edge trigger Bit[1] gpio_sus_intr_lvl_trig_en 1: set as USB/PCI SUS as level trigger, 0: edge trigger Bit[2] gpiointr_bypass_debunce 1: do NOT debunce, process_power_gpio_set() always return TRUE Bit[3] gpiointr_no_break 1: do NOT "break" after debunce check; to solve the problem of lossing PDN-signal, valid when gpiointr_no_break = 0 Bit[4] fast_gpio_power_on_check 1: move gpio_power_on_check for power-down as fast as possible Bit[5] record_bton_pre_boot_state 1: record the bton pre-boot state; (0) just power-on (1) from bt_hwpdn_en (2) from bt_sus_en (3) bt_hwpdn_en+bt_sus_en Bit[7:6] rsvd	36h
1D2h~1D3h	efuse_baud_est_setting_1_d16	Bit[0] baud_mon_en Bit[1] baud_est_en Bit[2] baud_recov_at_fw_trig_wdg Bit[3] baud_recov_at_h5_linkreset Bit[4] baud_recov_at_reinit Bit[5] baud_recov_at_other_wdg Bit[6] baud_recov_at_state_stop_postset Bit[7] baud_recov_at_state_stop_preset	8E4Ch

Bytes	Contents	Description	Value
		Bit[8] baud_est_restart_at_h5_linkreset Bit[9] exec_baud_est_init_post_at_reinit Bit[10] baud_est_update_at_h5_initialized Bit[11] baud_est_restart_at_baud_sram_recov Bit[13:12] baud_est_ovsrx8_grid ovsr search grid = 2^(x)/8; 1/4 or 1/8 is preferred Bit[15:14] min_low_falling_udfl_th_opt	
1D4h~1D5h	efuse_baud_est_setting_2_d 16	Bit[3:0] baud_est_falling_cnt_th_1st uart_falling_cnt_th = (baud_est_toggle_th*4) Bit[5:4] baud_est_combine_opt 0: by min_low_period, 1: by min_falling_space, 2: by average, ... Bit[7:6] baud_est_combine_opt_both_udfl Bit[8] min_falling_ovfl_chg_to_min_low Bit[9] min_low_udfl_chg_to_min_falling Bit[10] ignore_invalid_falling_low_ratio Bit[13 :11] est_bias_value Unit: 1/4 ovsr_div Bit[14] est_bias_sign 0: add, 1: sub Bit[15] baud_det_finetune_by_exhaust_est	0353h
1D6h~1D7h	efuse_baud_est_setting_3_d 16	Bit[11:0] det_allow_table Bit[14:12] baud_est_ovsr_low_bound Estimation OVSR Lower Bound = x+5 Bit[15] w1c_at_fallint_cnt_intr_end	CFFFh
1D8h~1D9h	efuse_baud_est_setting_4_d 16	Bit[1:0] baud_est_opt 0: exhaustive search, 1: detection, 2: detection, if err>(est/2^(1+x)) ==> exhaustive search Bit[4:2] det_err_chg_to_est_th valid when baud_est_opt = 2, if(err/ovsr_div_x8_est >= 1/2^x){ use exhaustive search } Bit[7:5] baud_est_delay 0: no delay, 1~7: delay 2^(x-1)ms; It should not affect the normal reception by changing baudrate during charcter	E34Dh

Bytes	Contents	Description	Value
		Bit[10:8] hci_uart_baud_est_h5init_retry_th intr_cnt_th for update baud rate at "H5 INIT State" or "R8723A-Det Mode Idle State" Bit[11] baud_est_by_low_period_at_h5_initialized Bit[15:12] baud_est_falling_cnt_th_2nd TRAIL State uart_falling_cnt_th = (baud_est_toggle_th*4)	
1DAh~1DBh	efuse_modem_psd_setting_1_d16	Bit[0] rtk_afh_modem_psd_enable Bit[1] afh_map_gen_instant_opt Bit[3:2] psd_timers_start_opt 0: no start, 1: as old afh, 2: if any active link with AFH Bit[4] psd_scan_3ch_mode 0: 1-channel mode, 1: 3-channel mode (need also to set EN_BPF_PSD related registers) Bit[5] rom_code_init_en Bit[6] force_channel_classify_on Bit[7] lmp_gen_afh_map_use_modem_psd_only Bit[8] lmp_gen_afh_map_at_other_case Bit[15:9] reserved	00B7h
1DCh~1DDh	efuse_modem_psd_setting_2_d16	Reserved	0000h
1DEh	efuse_pow_setting_4_d8	Bit[1:0] fast_gpio_power_on_check2b 1: move gpio_power_on_check for power-down as fast as possible; 2: after lc_init_radio() (for execute EFUSE Register Write(PHY_Init)) Bit[7:2] reserved	01h
1DFh	efuse_pow_setting_5_d8	Reserved	00h
1E0h	efuse_modem_rssi0_pin_dBm		A0h
1E1h	efuse_lps_setting_5_d8	Bit[0] lps_check_ext_32k_exist Bit[1] lps_use_new_cal Bit[2] lps_use_new_cal_fw_mode 1: use new calibration fw manual mode Bit[3] reserved	00h

<table>
<tr><th>Bytes</th><th>Contents</th><th>Description</th><th>Value</th></tr>
<tr><td></td><td></td><td>Bit[4] disable_never_enter_lps_when_usb_active
1: disable_never_enter_lps_when_usb_active = 0
Bit[7:5] lps_scan_protect_time
lps_scan_protect_time = 0; // (x + 2)*10msec</td><td></td></tr>
<tr><td>1E2h</td><td>efuse_rf_setting_1_d8</td><td>Bit[0] execute_lok_at_boot
Bit[3:1] execute_lok_at_boot_avg_num
average times = 2^x
Bit[4] execute_lok_at_boot_dummy_lok
Bit[5] lok_dont_set_rf_off
Bit[6] lok_force_adda_idle_on
Bit[7] reserved</td><td>00h</td></tr>
<tr><td>1E3h ~1F3h</td><td>reserved</td><td>Reserved</td><td>FFh (x 17)</td></tr>
<tr><td>1F4h ~ 3F3h</td><td>wPHYInit_RegVal[128]</td><td>(uints:4 bytes)
The structure of wPHYInit_RegVal :
Bit[31:16] The Register Value to be written
Bit[15:13] Register Type
➢ 0: RF
➢ 1: Modem
➢ 3: Delay
➢ 4: Vendor
➢ 6: Data UART
➢ 7: LE
➢ 2/5: Bluewiz
Bit[12]: Reserved
Bit[11:0]: The Definition is depended on Register Type
<table>
<tr><th></th><th>Modem</th><th>Delay</th><th>Others</th></tr>
<tr><td>Bit[31:16]</td><td>The value to be written</td><td>Delay Time (Units:ms)</td><td>The value to be written</td></tr>
<tr><td>Bit[15:13]</td><td>1</td><td>3</td><td>0/2/4/5/6/7</td></tr>
<tr><td>Bit[12]</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit[11:0]</td><td>Bit[9:8]: Page Number
Bit[7:0]: Word Address</td><td>NC</td><td>Register Offset</td></tr>
</table></td><td>-</td></tr>
</table>

Bytes	Contents	Description	Value
		Note: wPHYInit_RegVal [x] = 0x1234FFFF means “End of Script”	