正基科技股份有限公司

SPECIFICATION

SPEC. NO.： _____ REV： 1.0

DATE： 12. 25.2014

PRODUCT NAME： AP6452

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

AMPAK

AP6452

WiFi+BT4.0+GPS
SIP ModuleSpec Sheet

Revision History

Date	Revision Content	Revised By	Version
2014/12/25	- **Preliminary**	Brian	**1.0**

Contents

1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi, Bluetooth, and GPS functionalities. The highly integrated tiny module makes the possibilities of web browsing, VoIP, Bluetooth headsets, and portable navigation applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

The module complies with IEEE 802.11 b/g/n standard and it could achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in 802.11g, or 11Mbps for 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / PCM / Audio interface for Bluetooth and GPS.

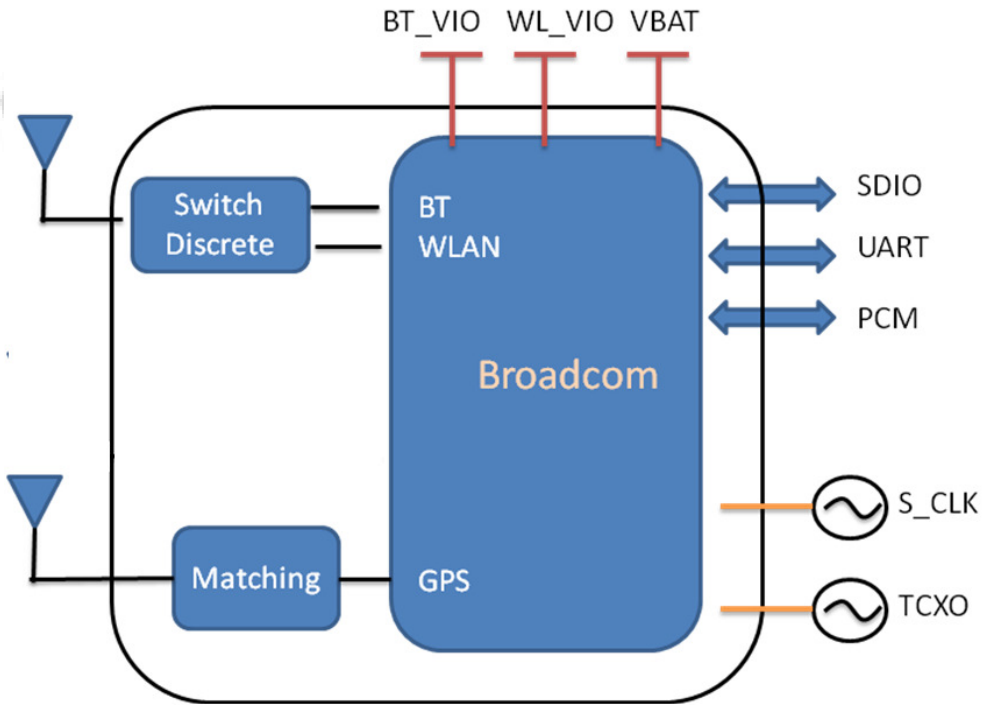
The module introduces dual-constellation support for both GPS and GLONASS with the same receiver chain. The GPS core host-based in the module splits processing functions between the GPS device and the CPU on the host system.

This compact module is a total solution for a combination of WiFi + BT + GPS technologies. The module is specifically developed for Tablet, Smart phones and Portable devices.

2. Features

- 802.11b/g/n single-band radio
- Bluetooth V4.0 with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - SDIO v2.0x — up to 50 MHz clock rate
- BT host digital interface:
  - UART (up to 4 Mbps)
- GPS able to track up to 12 satellites.
- IEEE Co-existence technologies are integrated die solution
- SECI — serial enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	AP6452
Product Description	Support WiFi/Bluetooth/ GPS functionalities
Dimension	L x W x H: 12.0 x 12.0 x 1.5 (typical)mm
WiFi Interface	SDIOV2.0
BT/GPS Interface	UART1/ PCM / UART2
Operating temperature	-30℃ to 85℃
Storage temperature	-40℃ to 85℃
Humidity	Operating Humidity 10% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	6	V
VDDIO	Voltage source for I/O Voltage	-0.5	3.6	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.6	4.8	V
VDDIO	1.7	3.3	3.6	V

5. WiFi RF Specification

5.1 2.4GHz RF Specification

Feature	Description
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
FrequencyRange	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz：Ch1 ~ Ch14
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n/65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 dBm, typical
	- MCS=1 PER @ -84 dBm, typical
	- MCS=2 PER @ -82 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -73dBm, typical
	- MCS=6 PER @ -71dBm, typical
	- MCS=7 PER @ -69dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -86 dBm, typical
	- 9Mbps PER @ -85 dBm, typical
	- 12Mbps PER @ -85 dBm, typical
	- 18Mbps PER @ -83 dBm, typical
	- 24Mbps PER @ -81 dBm, typical
	- 36Mbps PER @ -78 dBm, typical
	- 48Mbps PER @ -73 dBm, typical
	- 54Mbps PER @ -72 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -90 dBm, typical
	- 2Mbps PER @ -89 dBm, typical
	- 5.5Mbps PER @ -88dBm, typical
	- 11Mbps PER @ -85dBm, typical
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48,54Mbps
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps

Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

6. Bluetooth Specification

6.1 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	BluetoothV4.0 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power (Class 1.5)		10	
Output Power (Class 2)		2	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

7. GPS Specification

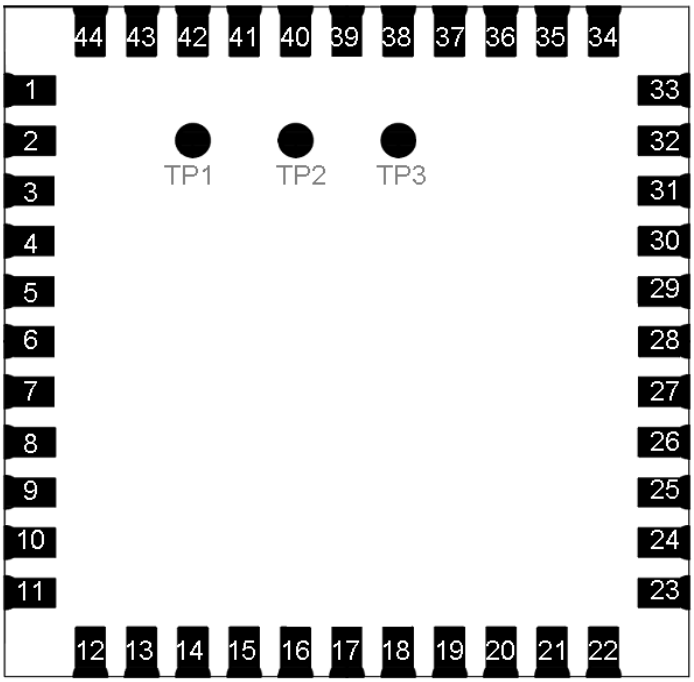
7.1 GPS Specification

Feature	Description				
General Specification					
Frequency Band	1575.42 MHz				
Host Interface	HCI UART				
Number of Channels	12 Channels				
Antenna Gain	1.5~5 dBi				
Sensitivity	Cold Start -140dBm, Hot Start -150dBm,Tracking -155dBm				
Characteristics	**Condition**	**Min**	**TYP**	**MAX**	**UNIT**
C/N	w/o LNA @ -130 dBm	35			
Autonomous Cold Start	Average TTFF@ -130 dBm			50	s
Autonomous Warm Start	Average TTFF@ -130 dBm			45	s
Autonomous Hot Start	Average TTFF@ -130 dBm			3	s

8. Pin Assignments

8.1 Pin Outline

<TOP VIEW >



8.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	GPIO4	I/O	GPIO
5	GPIO3	I/O	GPIO
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	GPS_REG_ON	I	GPS enable/disable pin
9	VBAT	P	Main power voltage source input
10	GPIO2	I/O	GPIO
11	GPIO1	I/O	GPIO
12	WL_REG_ON	I	WiFi enable/disable pin
13	WL_HOST_WAKE	O	WLAN to wake-up HOST
14	SDIO_D2	I/O	SDIO data line 2

15	SDIO_D3	I/O	SDIO data line 3
16	SDIO_CMD	I/O	SDIO command line
17	SDIO_CLK	I/O	SDIO CLK line
18	SDIO_D0	I/O	SDIO data line 0
19	SDIO_D1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage support 1.8V or 3.3V
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM Clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	VDD_TCXO	O	1.8V/3.3V supply for the external TCXO voltage
30	TCXO_IN	I	26MHz TCXO input
31	GND	—	Ground connections
32	GPS_RF	I	GPS RF input antenna port
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	LNA_EN	O	Enable output for external LNA
36	GND	—	Ground connections
37	GPS_UART_RTS	O	GPS UART interface
38	GPS_UART_TXD	O	GPS UART interface
39	GPS_UART_RXD	I	GPS UART interface
40	GPS_UART_CTS	I	GPS UART interface
41	BT_UART_RTS	O	Bluetooth UART interface
42	BT_UART_TXD	O	Bluetooth UART interface
43	BT_UART_RXD	I	Bluetooth UART interface
44	BT_UART_CTS	I	Bluetooth UART interface
45	NC	—	Floating (Don't connected to ground)
46	NC	—	Floating (Don't connected to ground)
47	NC	—	Floating (Don't connected to ground)

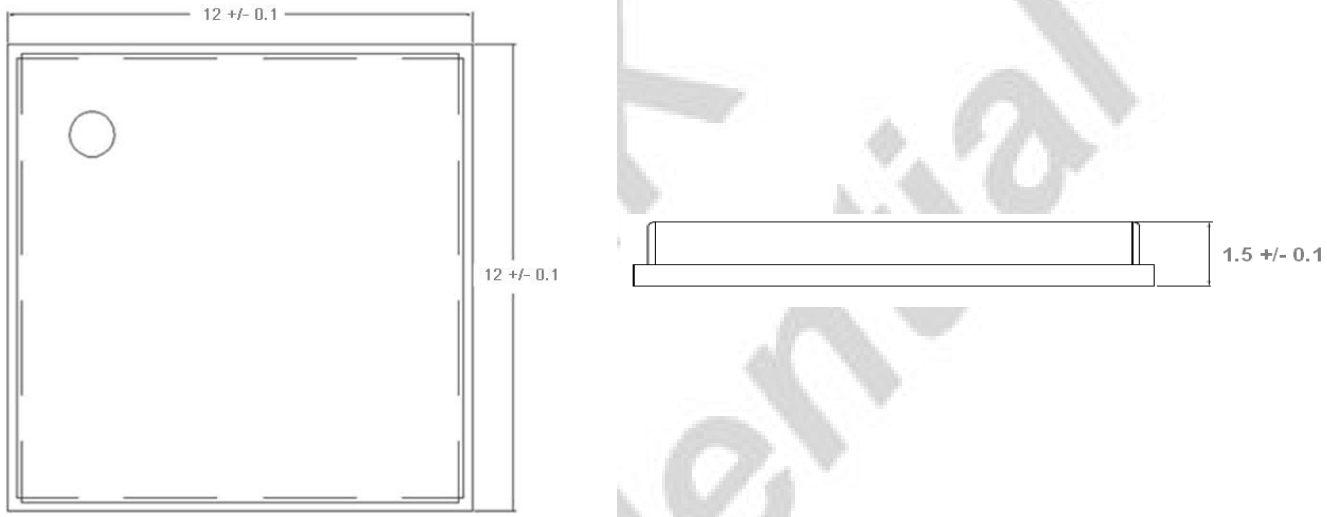
9. Dimensions

9.1 Physical Dimensions

(Unit: mm)

< TOP VIEW >

< Side View >



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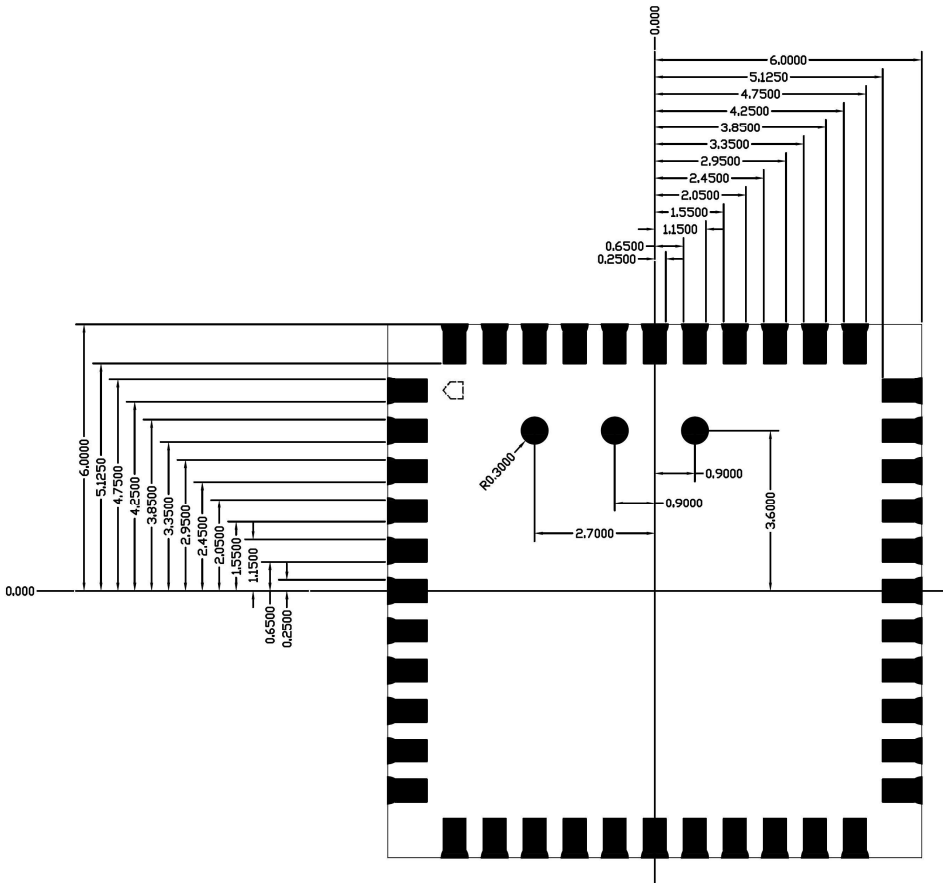
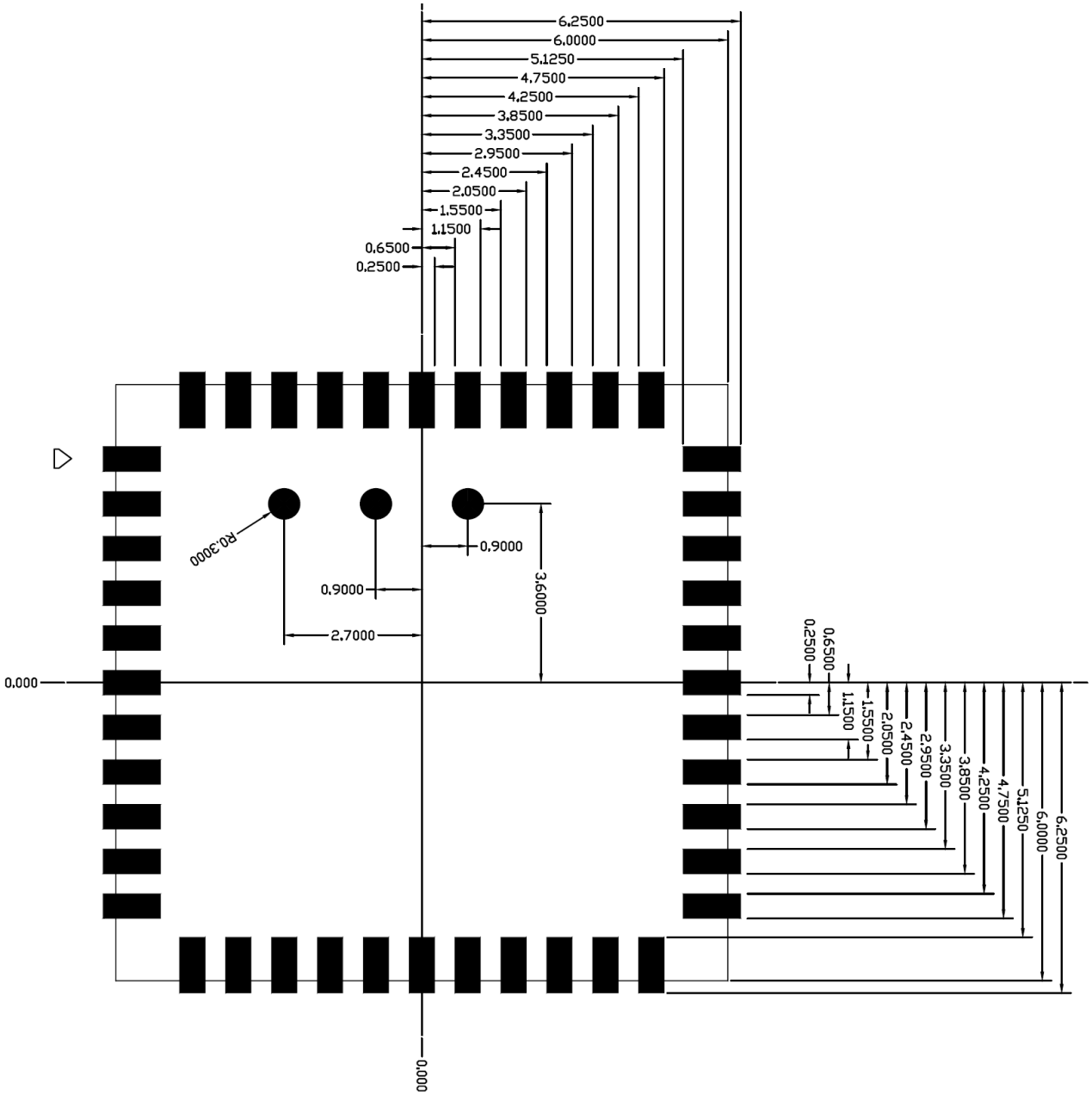


9.2 Layout Recommendation

(Unit: mm)

<TOP VIEW >



10. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

External TCXO signal characteristics

Parameter	Specification	Units
Nominal input frequency	26	MHz
Signal type	Sine-wave	-
Input Voltage Swing	400-1900	mVp-p
Input Voltage	0-1800	mV
Input capacitance	6(max)	pF
Input Low	0-0.1VDD	V
Input High	0.9VDD-VDD	V
Duty cycle	40 - 60	%
Frequency Tolerance(initial accuracy)	±2	ppm
Frequency Stability	±0.5	ppm
Aging	±1	Ppm/year
Phase Noise(26Mhz@1KHz carrier offset)	-130(max)	dBc/Hz

10.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function1 Backplane Function to access the internal System On Chip (SOC) address space(Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)
- ❖

SDIO Pin Description

SDIO 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

11. Host Interface Timing Diagram

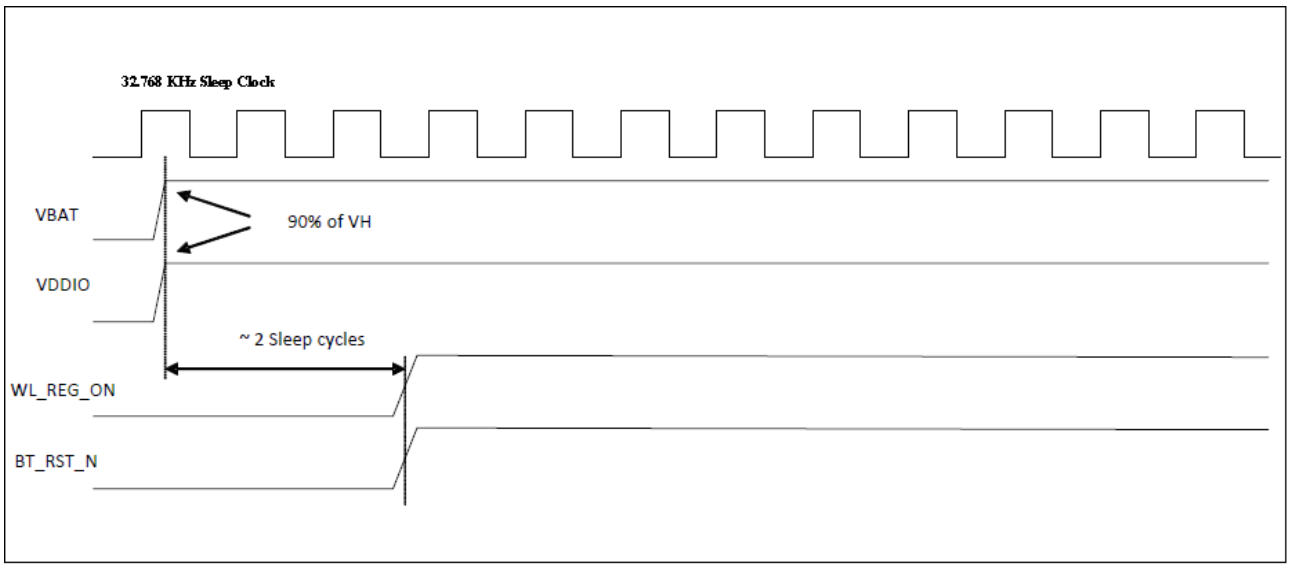
11.1 Power-up Sequence Timing Diagram

The module has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

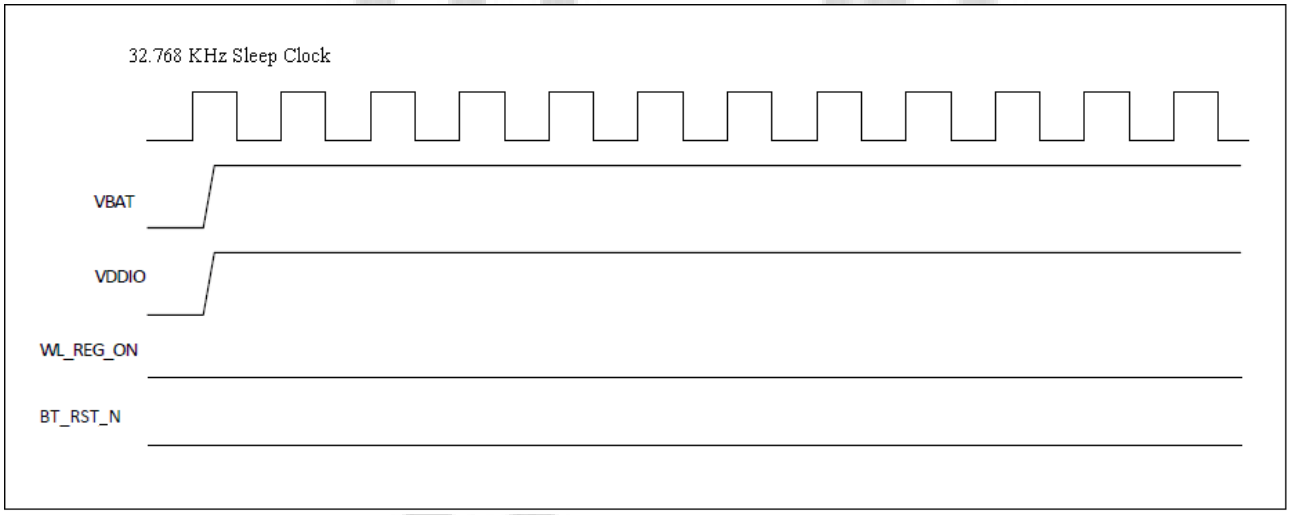
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

Note that the WL_REG_ON and BT_RST_ON are in the module. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (on for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the internal regulators.

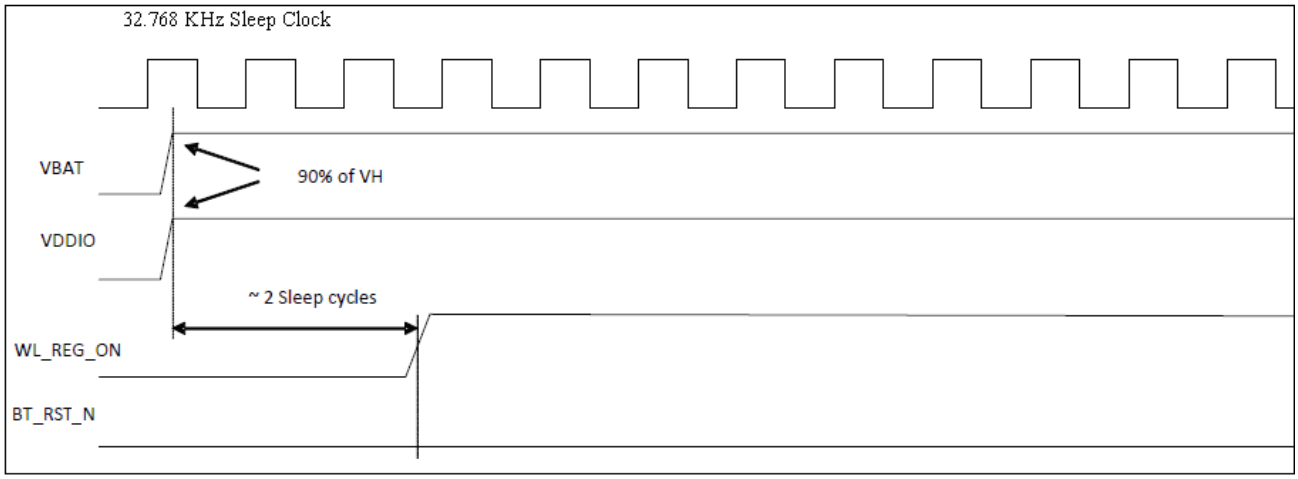
- ※ WL_REG_ON: Used by the PMU to power up the WLAN section. It is input to control the internal WLAN regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT_RST_ON: Used by the PMU to power up the internal Bluetooth regulators. If the BT_RST_ON pins are low, the regulators are disabled.



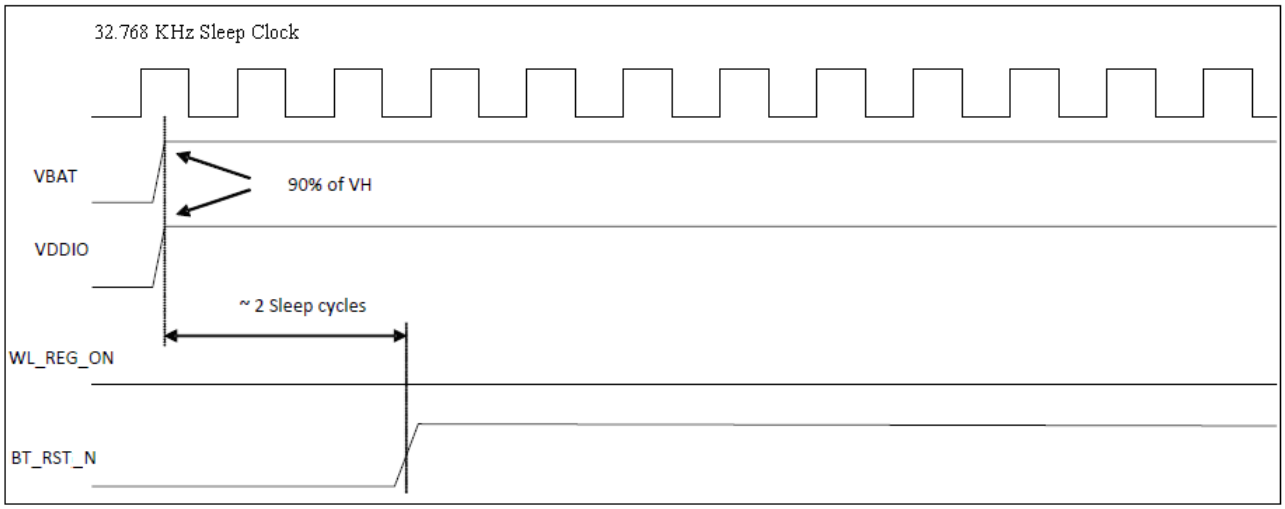
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

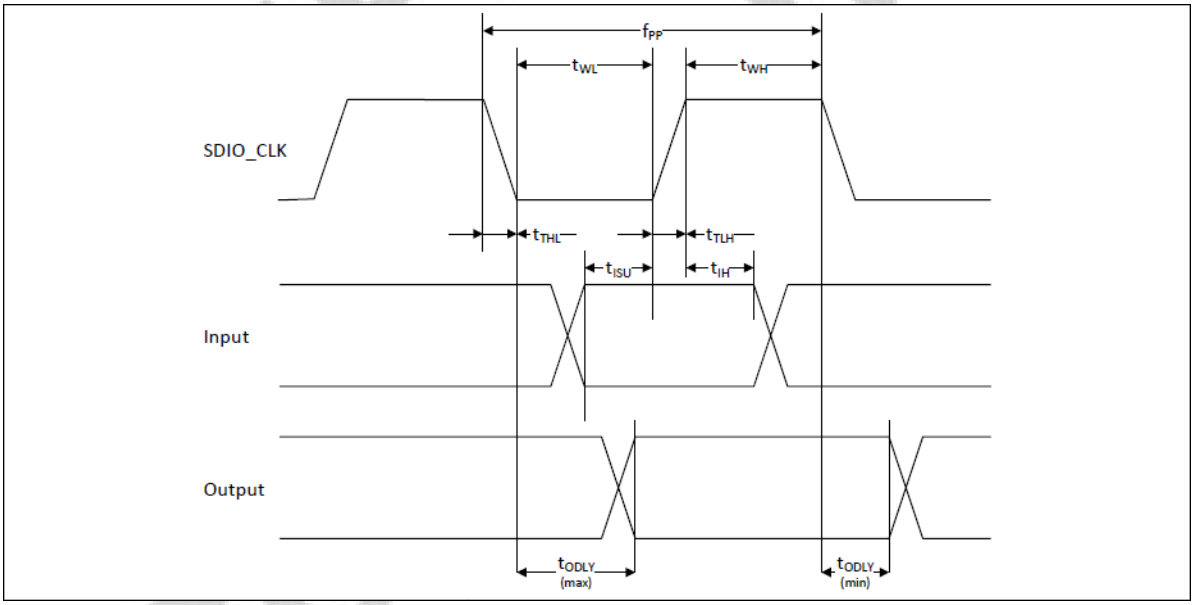


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

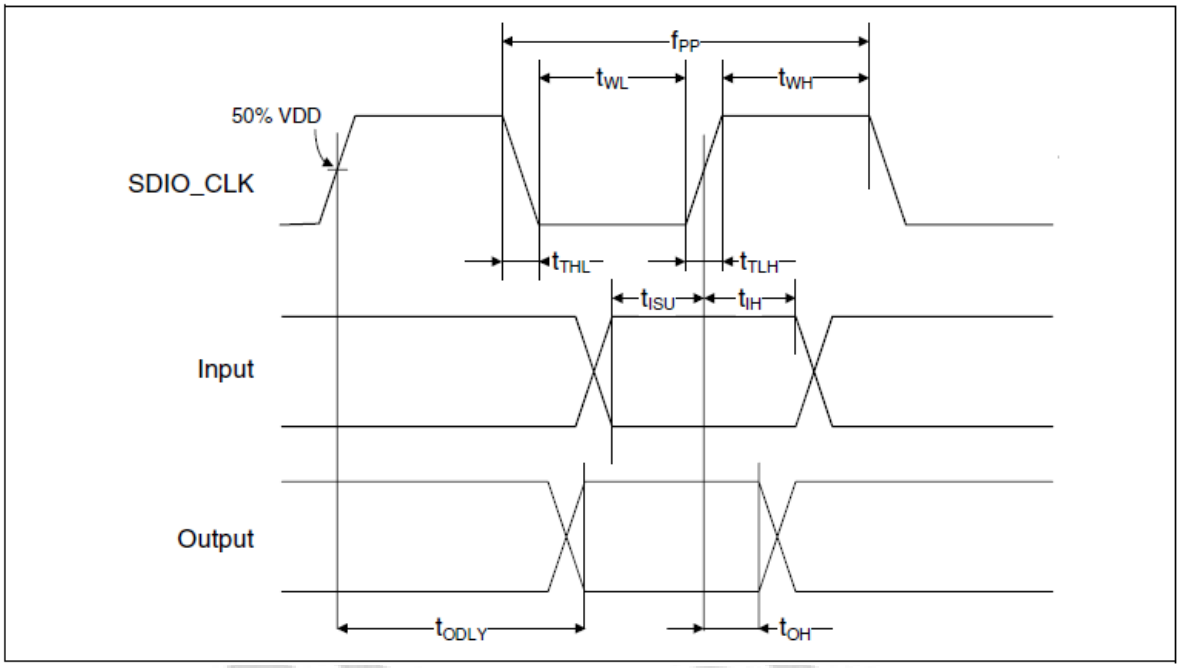
11.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

11.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

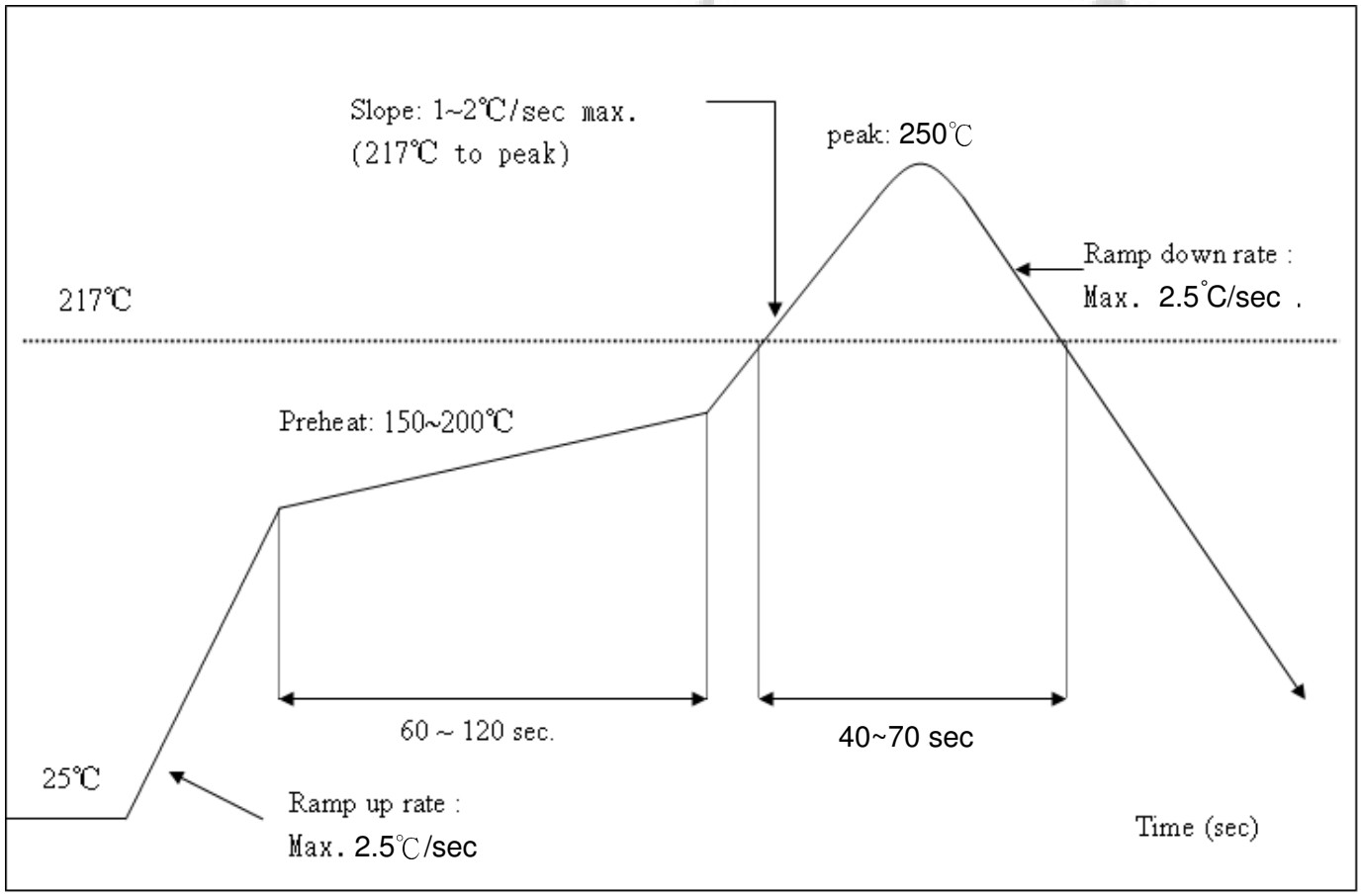
a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

12. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250℃

Number of Times : ≤2 times

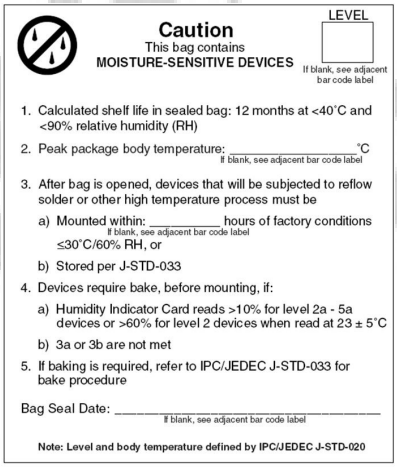


13. Package Information

13.1Label

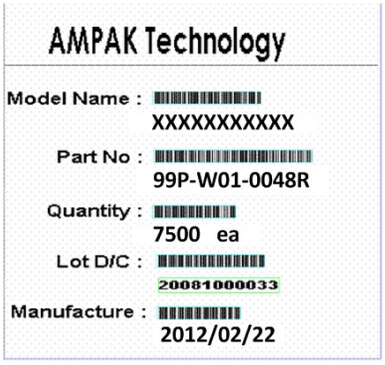
Label A→ Anti-static and humidity notice

Label B→ MSL caution / Storage Condition

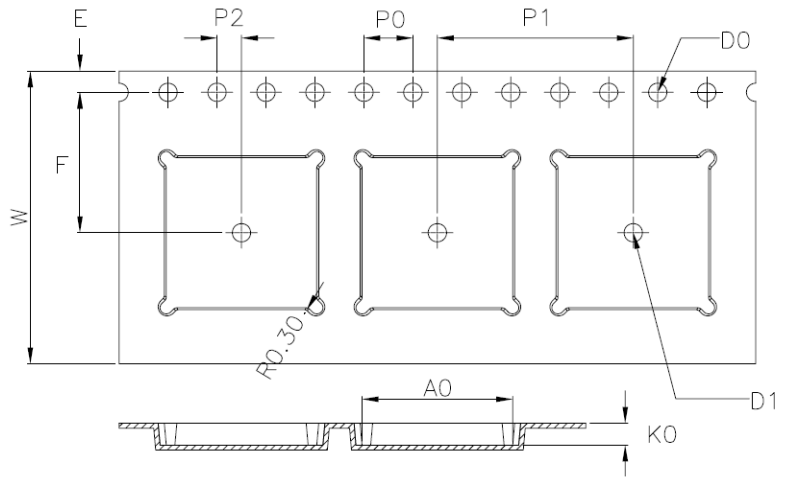


Label C→ Inner box label .

Label D→ Carton box label .

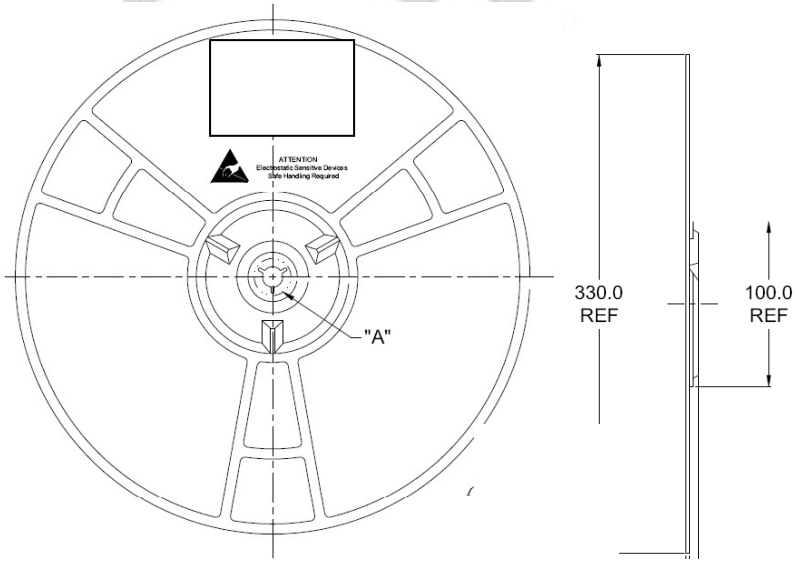


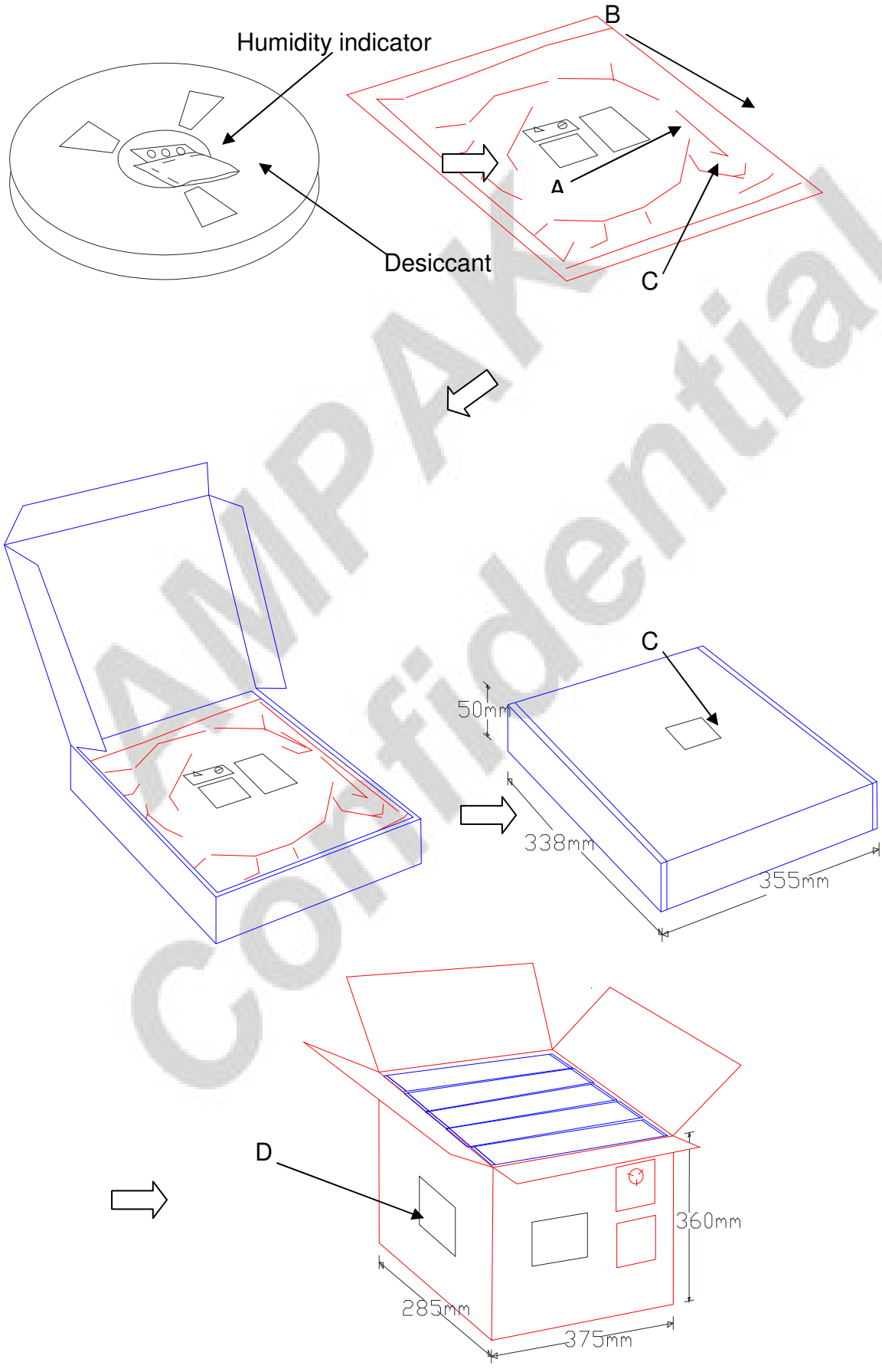
13.2Dimension



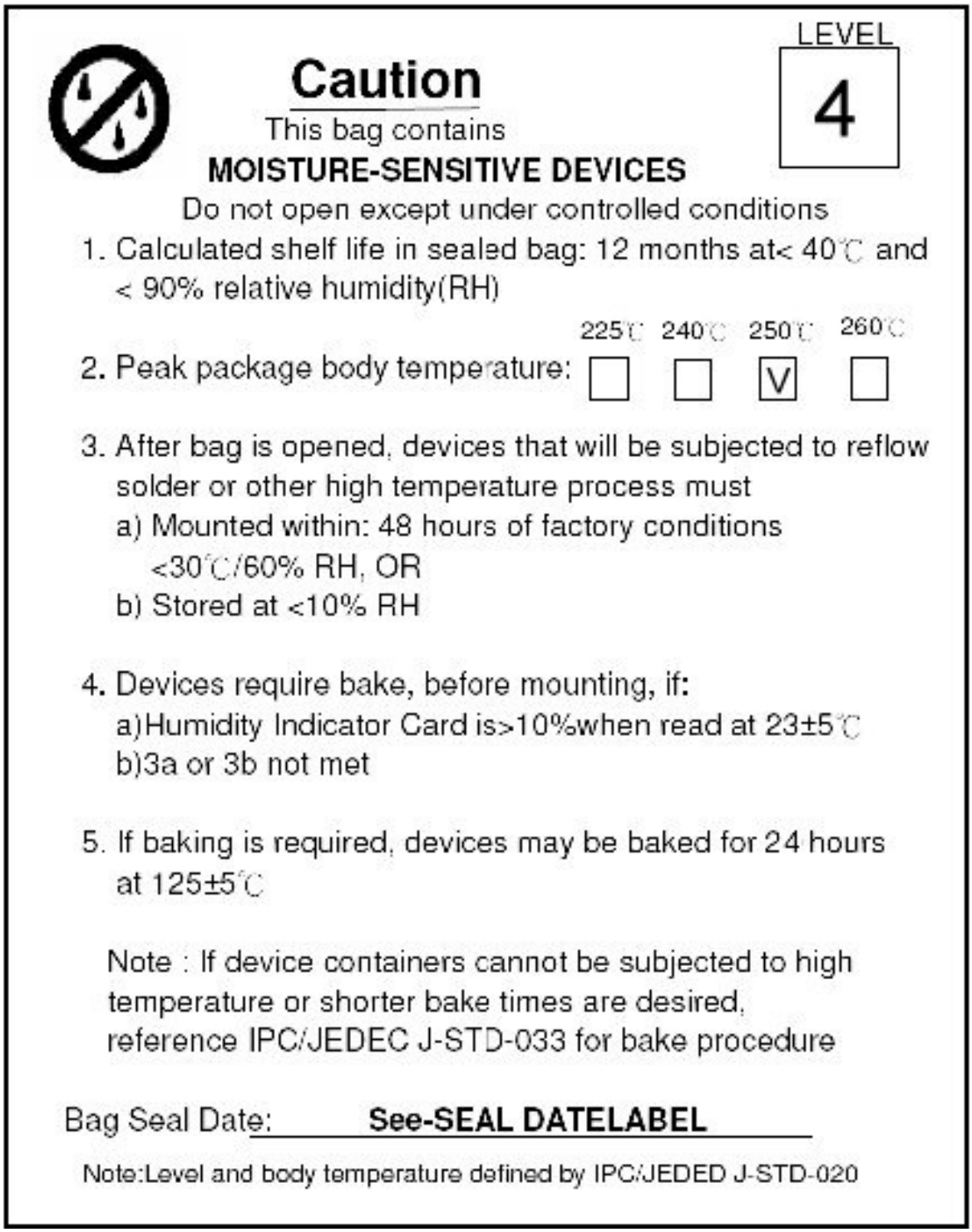
W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $^{+0.10}_{-0.00}$
D1	ø1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





13.3 MSL Level / Storage Condition



LEVEL 4

Caution

This bag contains

MOISTURE-SENSITIVE DEVICES

Do not open except under controlled conditions

1. Calculated shelf life in sealed bag: 12 months at< 40℃ and < 90% relative humidity(RH)
2. Peak package body temperature: 225℃ ☐ 240℃ ☐ 250℃ ☑ 260℃ ☐
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 48 hours of factory conditions <30℃/60% RH, OR
   b) Stored at <10% RH
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is>10%when read at 23±5℃
   b) 3a or 3b not met
5. If baking is required, devices may be baked for 24 hours at 125±5℃

Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: **See-SEAL DATELABEL**

Note:Level and body temperature defined by IPC/JEDED J-STD-020

※NOTE : Accumulated baking time should not exceed 96hrs