正基科技股份有限公司

SPECIFICATION

SPEC. NO.： _____ REV： 1.1

DATE： 03. 26.2015

PRODUCT NAME： AP6214A

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

AMPAK

AP6214A

WiFi + Bluetooth 4.0
SIP Module Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2015/01/13	- Preliminary	Brian	1.0
2015/03/26	- Pin Definition Modified	Brian	1.1

Contents

1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi and Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

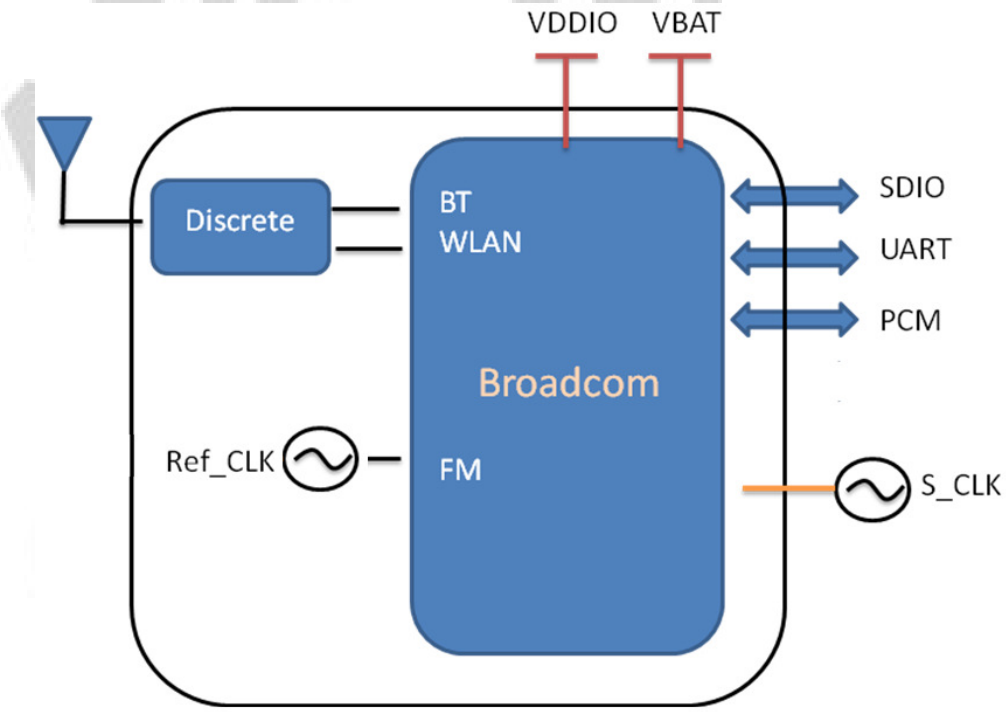
The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / PCM interface for Bluetooth.

This compact module is a total solution for a combination of WiFi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- 802.11b/g/n single-band radio
- Bluetooth V4.0(HS) with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - SDIO v2.0 — up to 50 MHz clock rate
- BT host digital interface:
  - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	AP6214A
Product Description	Support WiFi/Bluetooth functionalities
Dimension	L x W x H: 7 x 7 x 1.5 (typical) mm
WiFi Interface	SDIOV2.0
BT Interface	UART / PCM
Operating temperature	-30℃ to 85℃
Storage temperature	-40℃ to 85℃
Humidity	Operating Humidity 10% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.6	4.8	V
VDDIO	1.7	3.3	3.6	V

5. WiFi RF Specification

5.1 2.4GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25℃

Feature	Description
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz：Ch1 ~ Ch14
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 dBm, typical
	- MCS=1 PER @ -84 dBm, typical
	- MCS=2 PER @ -82 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -73 dBm, typical
	- MCS=6 PER @ -71 dBm, typical
	- MCS=7 PER @ -68 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -86 dBm, typical
	- 9Mbps PER @ -85 dBm, typical
	- 12Mbps PER @ -85 dBm, typical
	- 18Mbps PER @ -83 dBm, typical
	- 24Mbps PER @ -81 dBm, typical
	- 36Mbps PER @ -78 dBm, typical
	- 48Mbps PER @ -73 dBm, typical
	- 54Mbps PER @ -71 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -90 dBm, typical
	- 2Mbps PER @ -88 dBm, typical
	- 5.5Mbps PER @ -87 dBm, typical
	- 11Mbps PER @ -84 dBm, typical
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps

Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

6. Bluetooth Specification

6.1 Bluetooth Specification

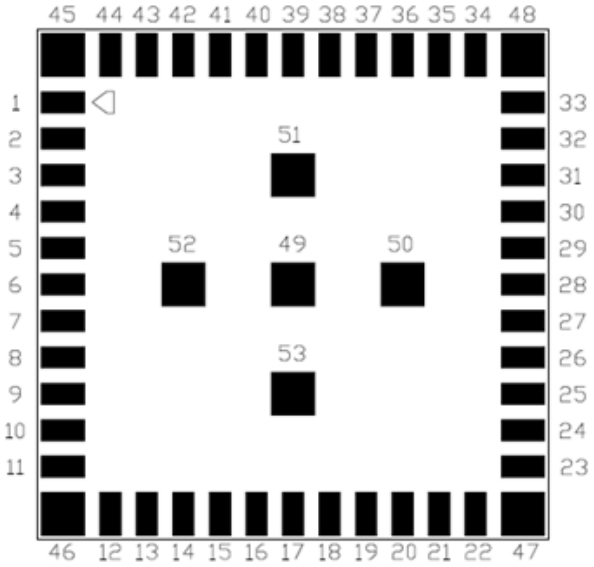
Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25℃

Feature	**Description**		
General Specification			
Bluetooth Standard	Bluetooth V4.0 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402MHz ~ 2480MHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power (Class 1.5)		8 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

7. Pin Assignments

7.1 Pin Outline

< TOP VIEW >



7.2 Pin Definition

NO	Name	Type	Description
1	WL_BT_ANT	I/O	RF I/O port
2	GND	—	Ground connections
3	BT_WAKE	I	HOST wake-up Bluetooth device
4	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
5	BT_REG_ON	I	Bluetooth device enable/disable pin
6	BT_GPIO3	I/O	BLUETOOTH GPIO
7	BT_GPIO4	I/O	BLUETOOTH GPIO
8	BT_GPIO5	I/O	BLUETOOTH GPIO
9	GND	—	Ground connections
10	NC	—	Floating (Don't connected to ground)
11	NC	—	Floating (Don't connected to ground)
12	NC	—	Floating (Don't connected to ground)
13	NC	—	Floating (Don't connected to ground)
14	GND	—	Ground connections
15	WL_GPIO3	I/O	WLAN GPIO
16	WL_GPIO4	I/O	WLAN GPIO

17	WL_GPIO2	I/O	WLAN GPIO
18	WL_GPIO1	I/O	WLAN GPIO
19	WL_HOST_WAKE	O	WLAN device to wake-up HOST
20	WL_REG_ON	I	WLAN device enable/disable pin
21	GND	—	Ground connections
22	NC	—	Floating (Don't connected to ground)
23	SDIO_DATA_CMD	I/O	SDIO command line
24	SDIO_DATA_CLK	I/O	SDIO clock line
25	SDIO_DATA_2	I/O	SDIO data line 2
26	SDIO_DATA_0	I/O	SDIO data line 0
27	SDIO_DATA_3	I/O	SDIO data line 3
28	SDIO_DATA_1	I/O	SDIO data line 1
29	GND	—	Ground connections
30	VDDIO	P	I/O Voltage supply input
31	LPO	I	External Low Power Clock input (32.768KHz)
32	VIN_LDO	P	Internal Buck voltage generation pin
33	VBAT	P	Main power voltage source input
34	VIN_LDO_OUT	P	Internal Buck voltage generation pin
35	GND	—	Ground connections
36	PCM_CLK	I/O	PCM clock
37	PCM_SYNC	I/O	PCM sync signal
38	PCM_OUT	O	PCM Data output
39	PCM_IN	I	PCM data input
40	UART_TXD	O	Bluetooth UART interface
41	UART_RXD	I	Bluetooth UART interface
42	UART_CTS_N	I	Bluetooth UART interface
43	UART_RTS_N	O	Bluetooth UART interface
44	GND	—	Ground connections
45	GND	—	Ground connections
46	GND	—	Ground connections
47	GND	—	Ground connections
48	GND	—	Ground connections
49	GND	—	Ground connections
50	GND	—	Ground connections
51	GND	—	Ground connections
52	GND	—	Ground connections
53	GND	—	Ground connections

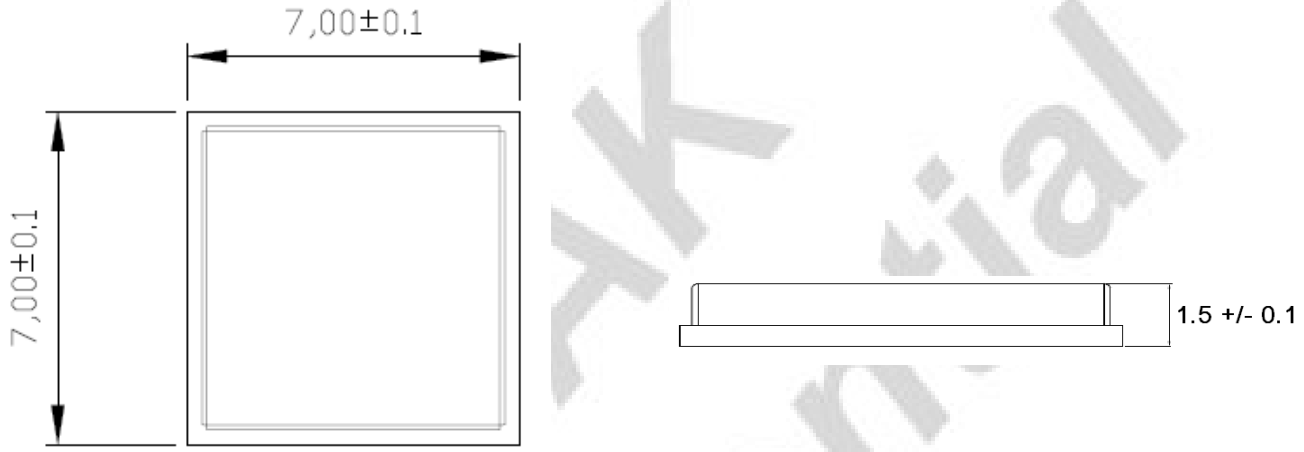
8. Dimensions

8.1 Physical Dimensions

(Unit: mm)

< TOP VIEW >

< Side View >



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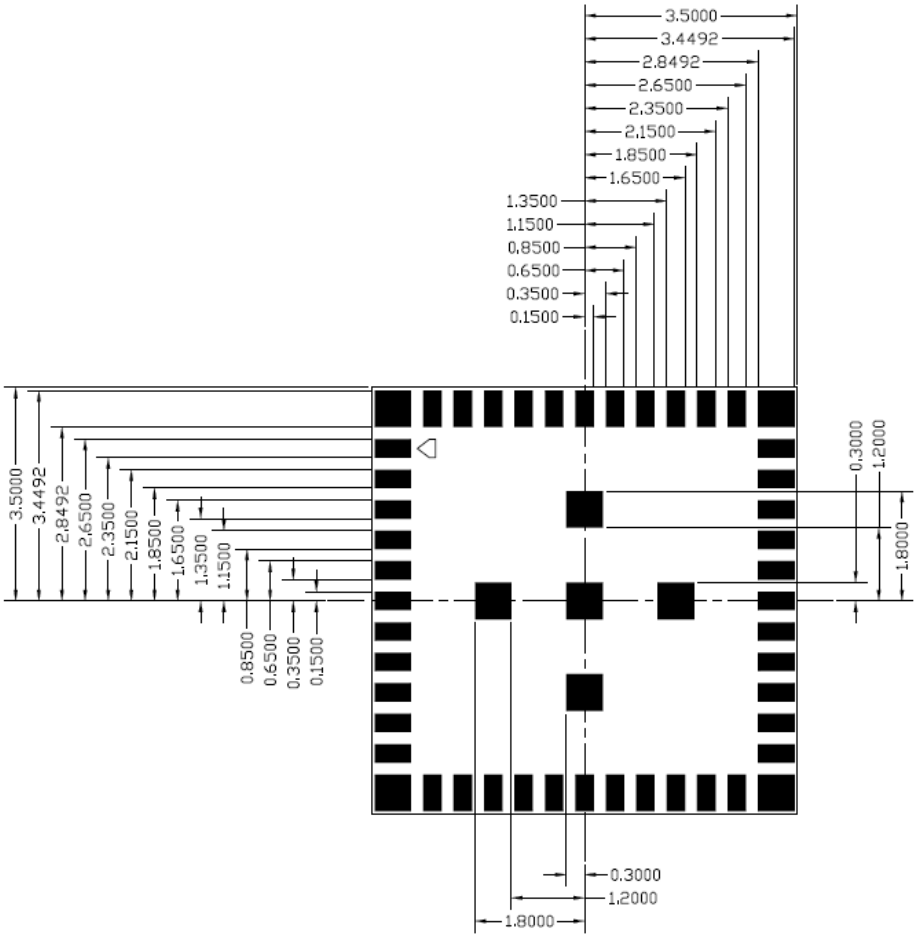
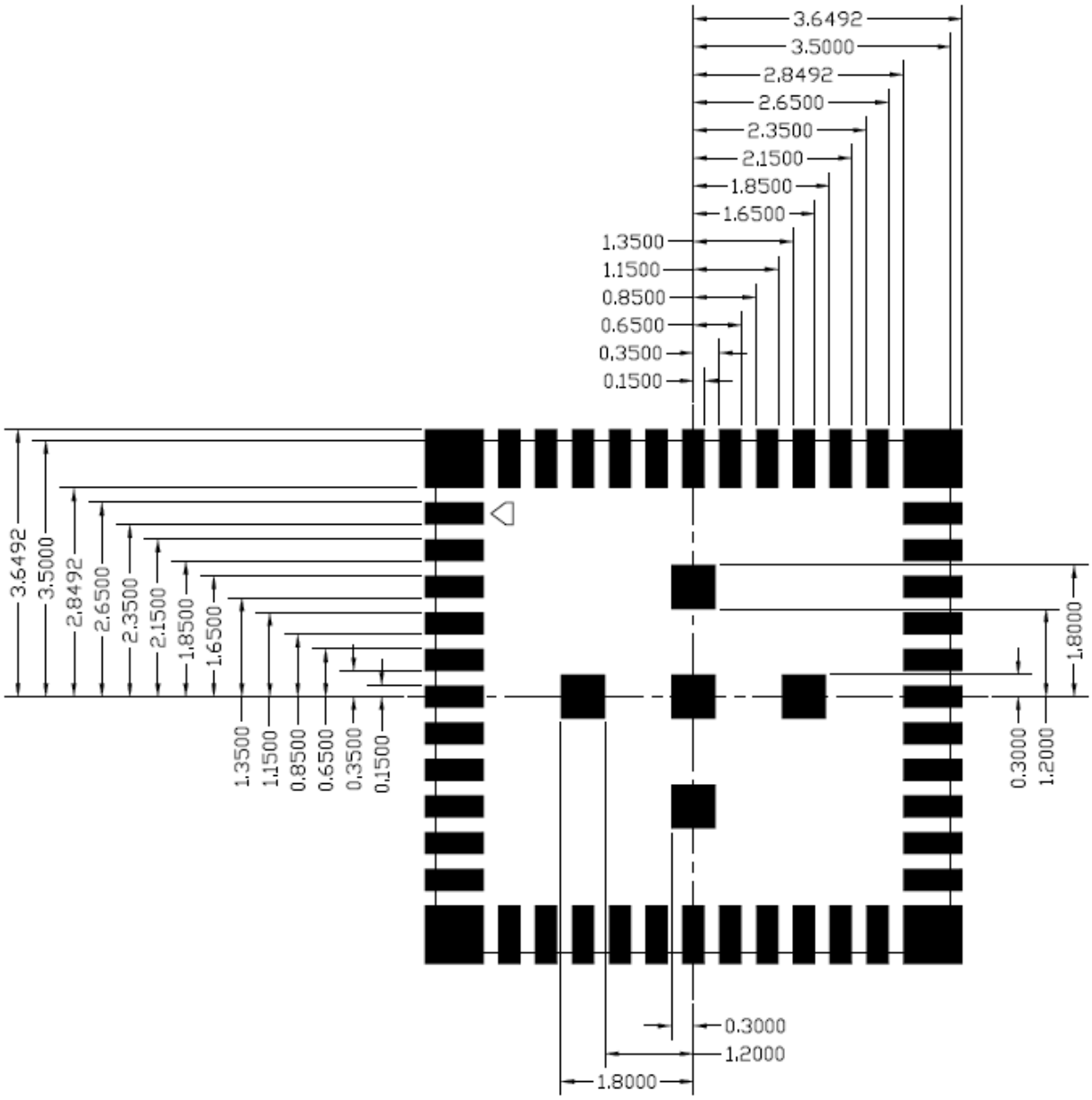


8.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >



9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

9.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

10. Host Interface Timing Diagram

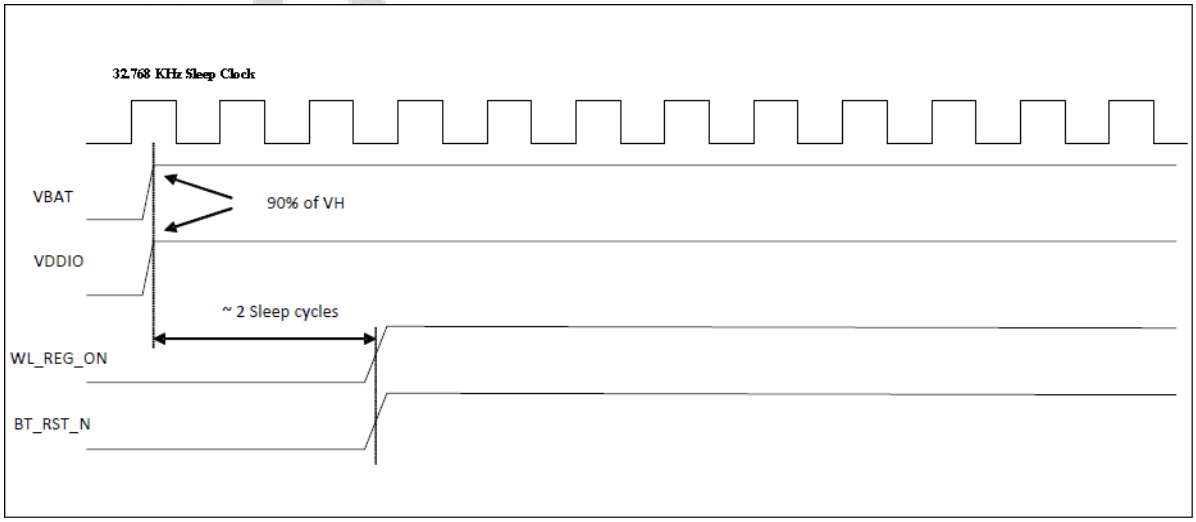
10.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

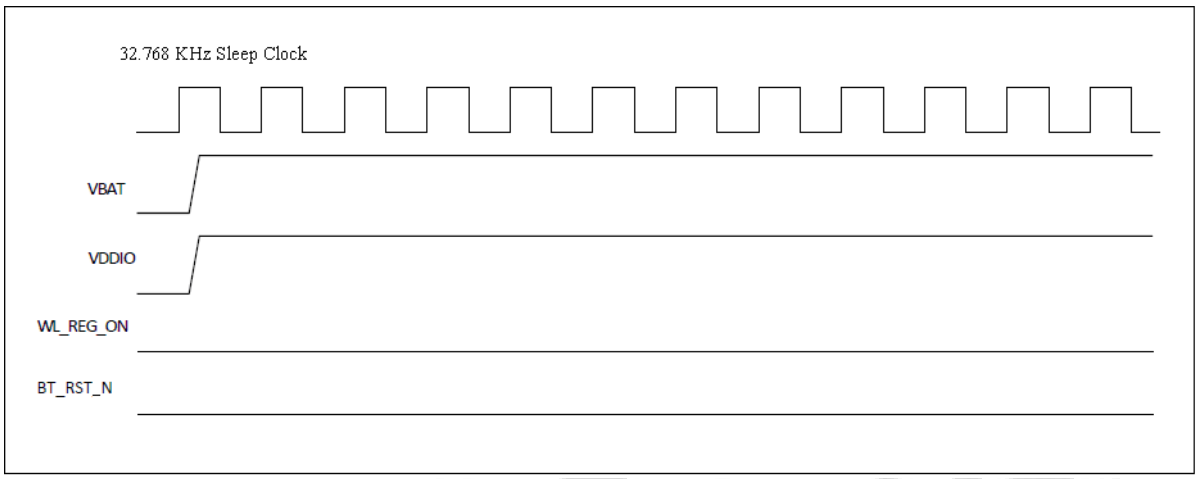
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.

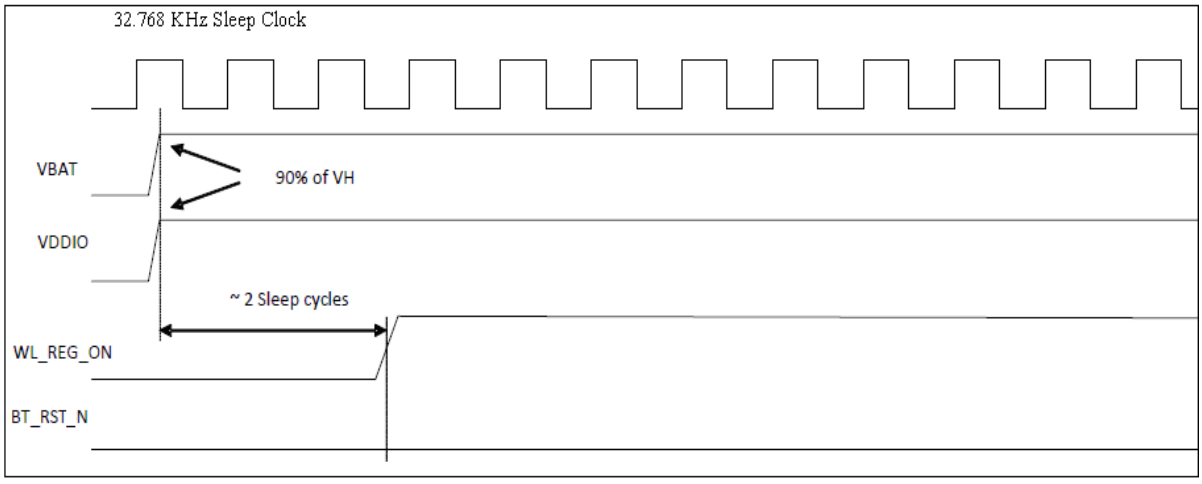
※ BT_RST_N: Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



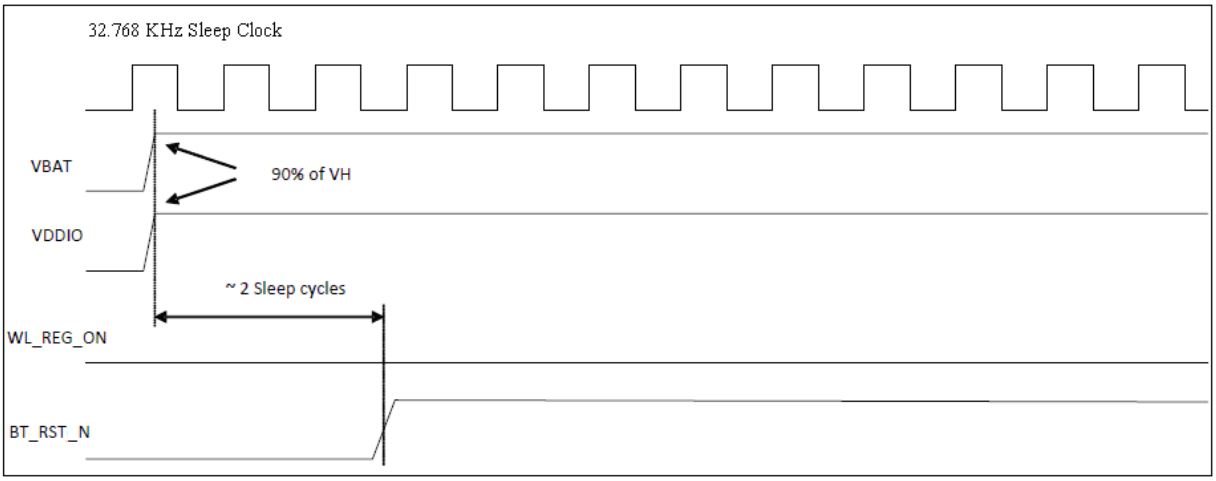
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

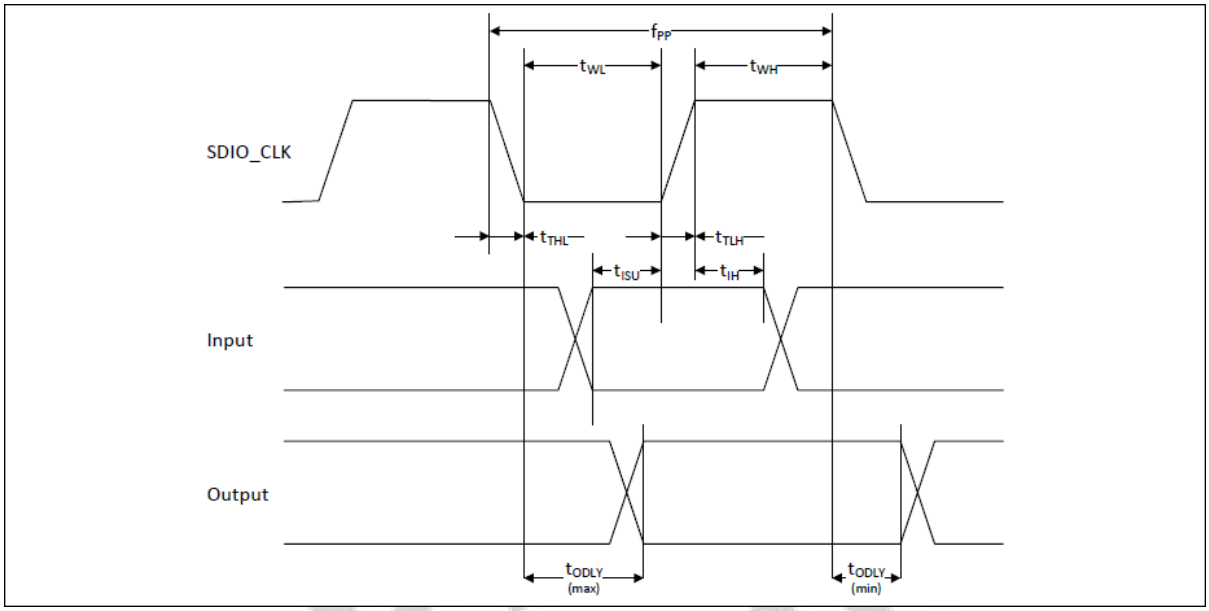


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

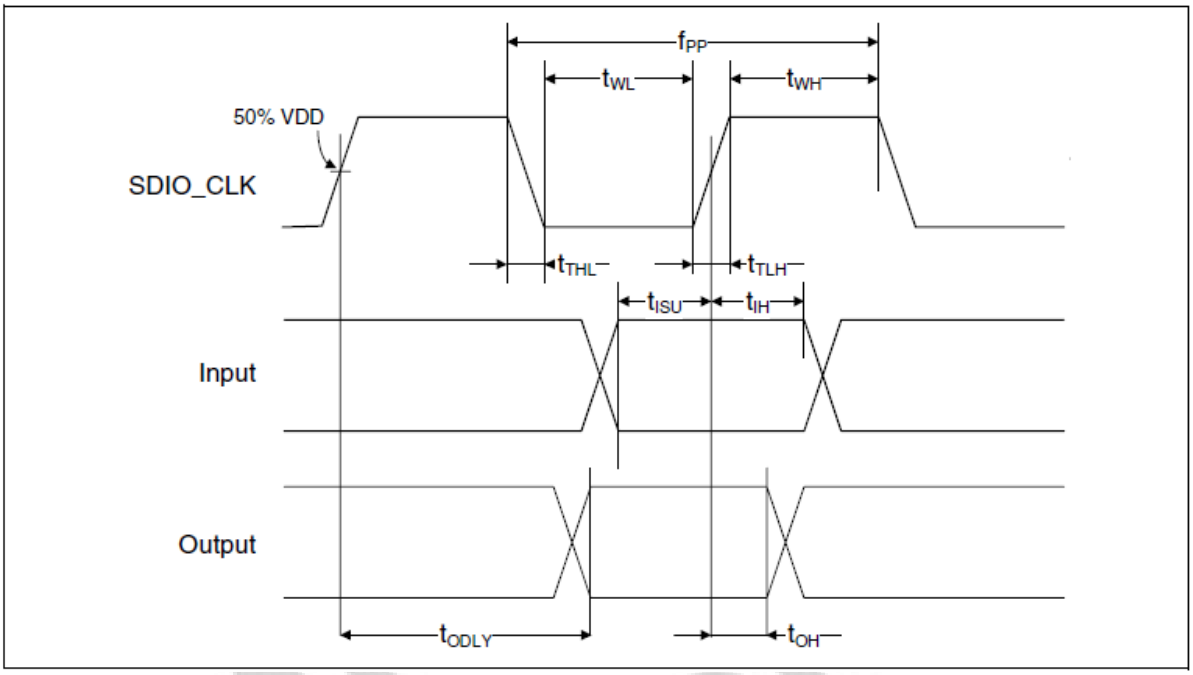
10.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

10.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

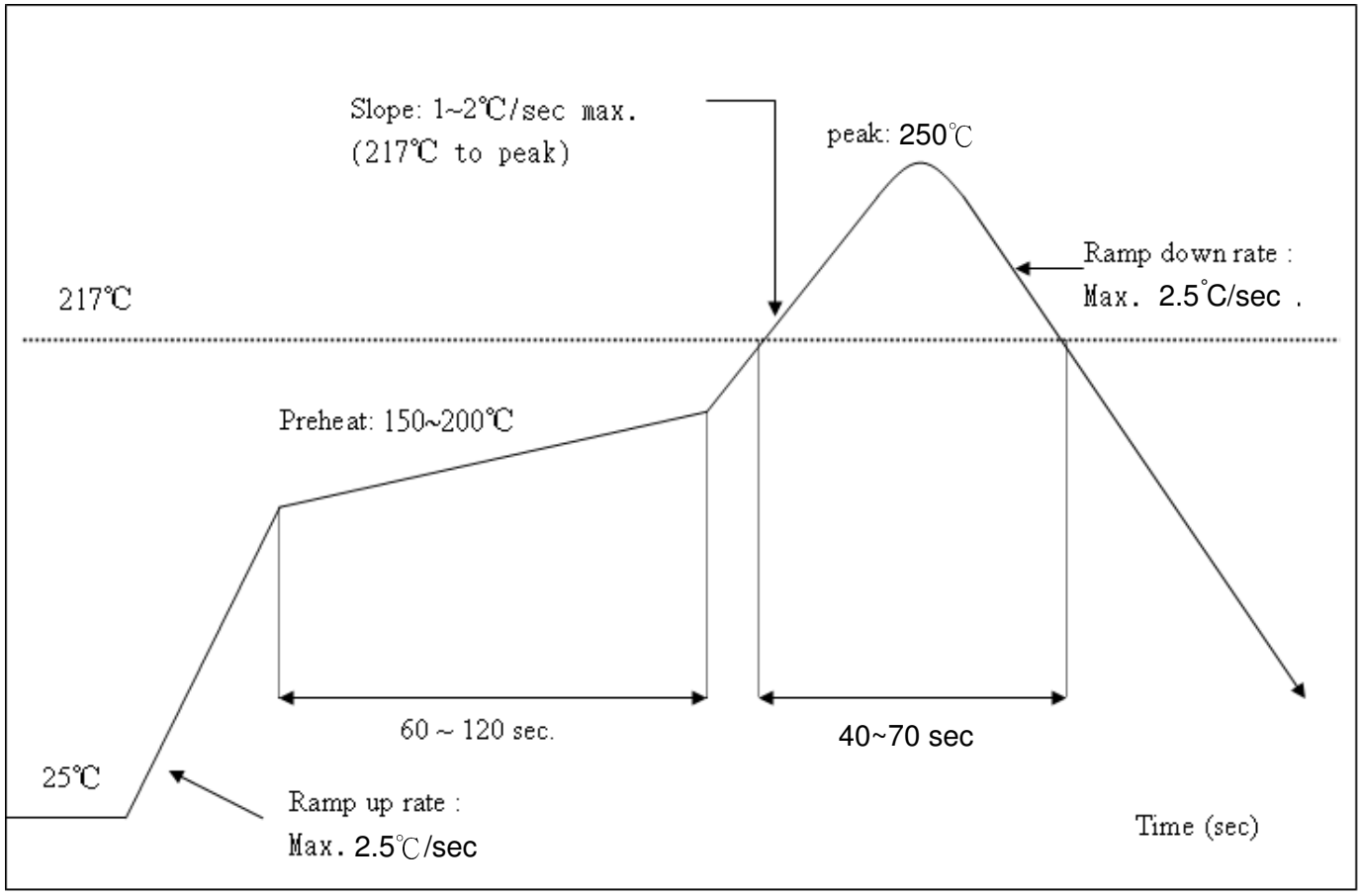
a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

11. Recommended Reflow Profile

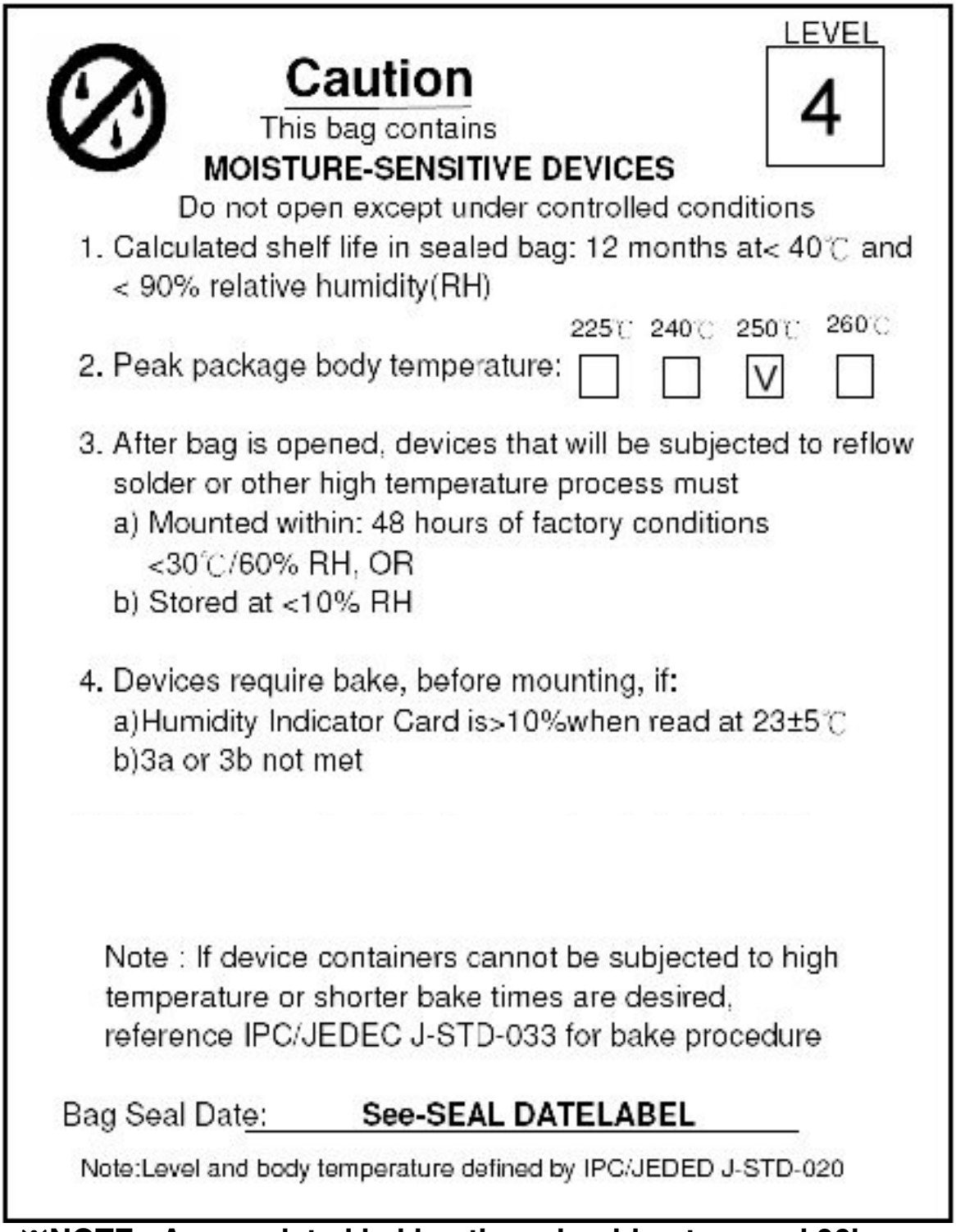
Referred to IPC/JEDEC standard.

Peak Temperature : <250℃

Number of Times : ≤2 times



12 MSL Level / Storage Condition



LEVEL 4

Caution

This bag contains

MOISTURE-SENSITIVE DEVICES

Do not open except under controlled conditions

1. Calculated shelf life in sealed bag: 12 months at< 40℃ and < 90% relative humidity(RH)

2. Peak package body temperature:

225℃	240℃	250℃	260℃
☐	☐	V	☐

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 48 hours of factory conditions <30℃/60% RH, OR
   b) Stored at <10% RH

4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is>10%when read at 23±5℃
   b) 3a or 3b not met

Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: **See-SEAL DATELABEL**

Note:Level and body temperature defined by IPC/JEDED J-STD-020

※NOTE : Accumulated baking time should not exceed 96hrs