Rockchip
RK3036
Technical Reference Manual
Graphic and Multi-media

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Revision History

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Chapter 1 GPU (Graphics Process Unit)

1.1 Overview

The GPU is a hardware accelerator for 2D and 3D graphics systems. Its triangle rate can be 30 Mtris/s, pixel rate can be 300Mpix/s@300MHz.
The GPU supports the following graphics standards:

- OpenGL ES 2.0
- OpenGL ES 1.1
- OpenVG 1.1

The GPU consists of:

- 1 Pixel Processors (PPs)
- 1 geometry Processor (GP)
- 1 Level2 Cache controller (L2)
- 1 Memory Management Unit (MMU) for each GP and PP included in the GPU

The GPU contains a 64-bit APB bus and a 64-bit AXI bus. CPU configures GPU through APB bus, GPU read and write data through AXI bus.

1.2 Block Diagram

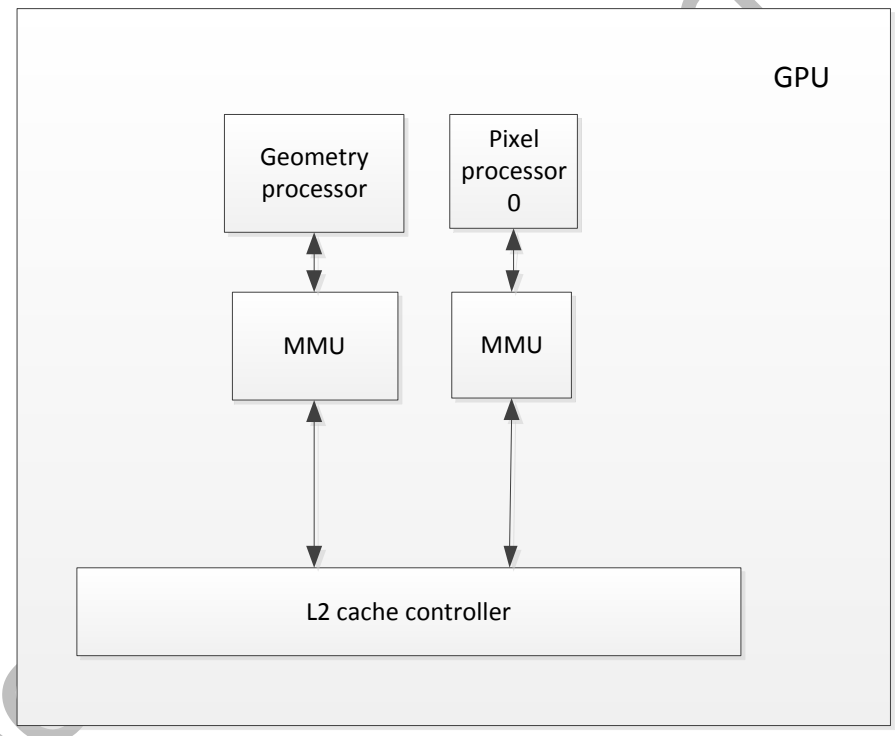


Fig. 1-1 GPU block diagram

The GPU contains one geometry processor, 1 pixel processors, 3 MMU and a L2 cache controller.
The pixel processor features are:

- Each pixel processor used processes a different tile, enabling a faster turnaround.
- Programmable fragment shader
- Alpha blending
- Complete non-power-of-2 texture support
- Cube mapping
- Fast dynamic branching
- Fast trigonometric functions, including arctangent
- Full floating-point arithmetic
- Framebuffer blend with destination alpha
- Indexable texture samplers
- Line, quad, triangle and point sprites

- No limit on program length
- Perspective correct texturing
- Point sampling, bilinear and trilinear filtering
- Programmable mipmap level-of-detail biasing and replacement
- Stencil buffering, 8-bit
- Two-sided stencil
- Unlimited dependent texture reads
- 4-level hierarchical Z and stencil operations
- Up to 512 times Full scene Anti-Aliasing (FSAA). 4x multisampling times 128x supersampling
- 4-bit per texel compressed texture format

The geometry processor features are:
- Programmable vertex shader
- Flexible input and output formats
- Autonomous operation tile list generation
- Indexed and no-indexed geometry input
- Primitive constructions with points, lines, triangles and quads

The L2 cache controller features are:
- 32KB size
- 4-way set-associative
- Supports up to 32 outstanding AXI transactions
- Implements a standard pseudo-LRU algorithm
- Cache line and line fill burst size is 64 bytes
- Support eight to 64 bytes uncached read bursts and write bursts
- 64-bit interface to memory sub-system
- Support for hit-under-miss and miss-under-miss with the only limitation of AXI ordering rules.

The MMU features are:
- Accesses control registers through the bus infrastructure to configure the memory system
- Each processor has its own MMU to control and translate memory access that the GPU initiates

1.3 Register Description

The GPU base address is 0x1009_0000.

1.4 Timing Diagram

The GPU only has a clock input, which is called gpu_aclk. Gpu_aclk is generated from the CRU module as shows below

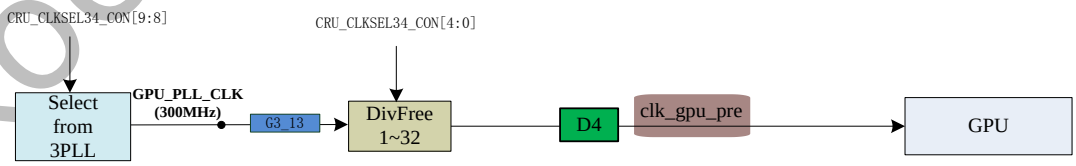


Fig. 1-2 GPU_ACLK generate block diagram

We can configure CPLL, GPLL and CRU register CRU_CLKSEL34_CON to control the gpu_aclk frequency.

1.5 Interface Description

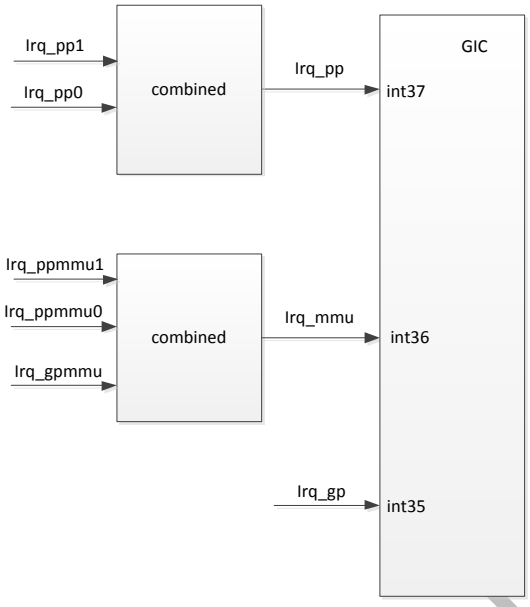


Fig. 1-3 GPU interrupt connection

The GPU now has three interrupt output. irq_ppmmu and irq_gpmmu is combined to irq_mmu.

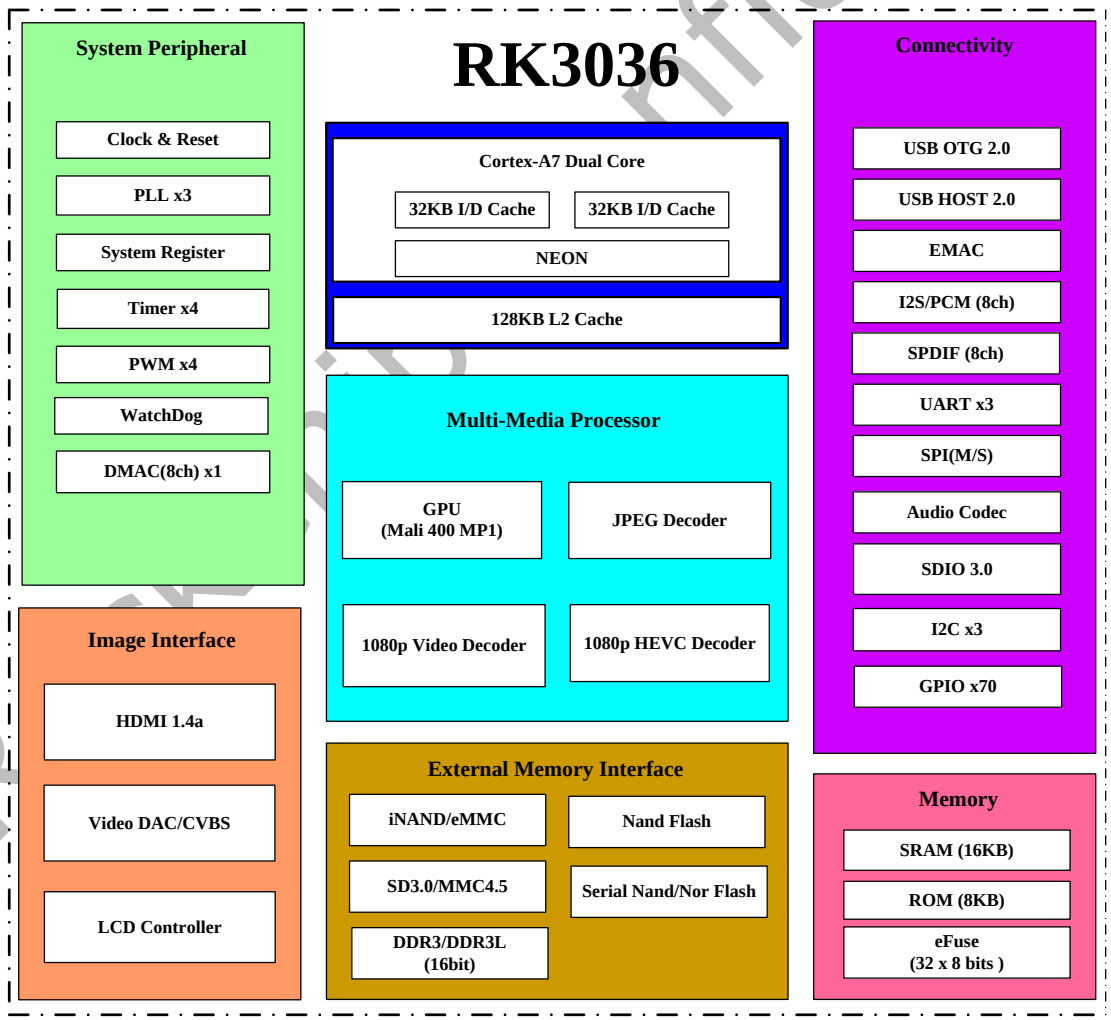


Fig. 1-4 RK3036 Block Diagram

Chapter 2 Video Output Processor (VOP)

2.1 Overview

Video Output Processor is a video process engine and a display interface from memory frame buffer to display device (HDMI or CVBS). VOP is connected to an AHB bus through an AHB slave and AXI bus through an AXI master. The register setting is configured through the AHB slave interface and the display frame data is read through the AXI master interface.

2.1.1 Features

- Interrupt
  - One combined interrupt
    - high active
    - raw status readable
    - combinational with interrupt sources
- Display interface
  - TV Interface
    - RGB2YUV, 8bit
    - TV encoder 10bit out for DAC
    - RGB888+1080i for HDMI
    - Parallel RGB HDMI Interface: 24-bit(RGB888)
  - Max output resolution
    - 1920x1080 for HDMI
    - 480i/576i for CVBS
- Display process
  - Background layer
    - programmable 24-bit color
  - Win0 layer
    - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - 1/8 to 8 scaling-down and scaling-up engine
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - De-flicker support for interlace output
  - Win1 layer
    - RGB888, ARGB888, RGB565
    - 1/8 to 8 scaling-down and scaling-up engine
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - support alpha scale
    - max input 720P UI
  - Hardware cursor
    - 8BPP(ARGB888 LUT)
    - Support two size: 32x32 and 64x64
    - 256 level alpha blending
    - Support hwc over panel at right and below side
- Others
  - Win0 layer and Win1 layer overlay exchangeable
  - YcbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
  - RGB2YcbCr(BT601)
  - Brightness, Contrast, Saturation, Hue adjustment
  - Blank and black display
  - Standby mode
  - Support MMU
  - Support QoS for higher bus priority for win0/win1/hwc
  - Support DMA stop mode

2.2 Block Diagram

The architecture is shown in the following figure.

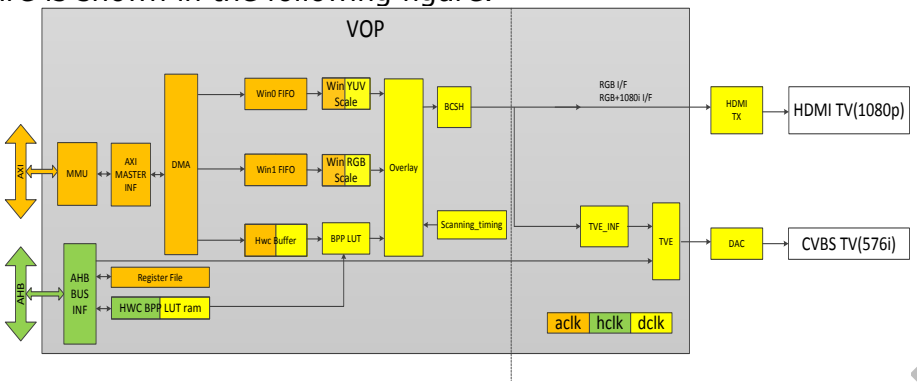


Fig. 2-1 VOP Block Diagram

2.3 Function Description

2.3.1 Pixel format

1. RGB

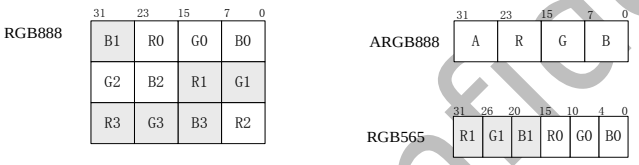


Fig. 2-2 RGB data format

2. YCbCr/YUV(8bit)

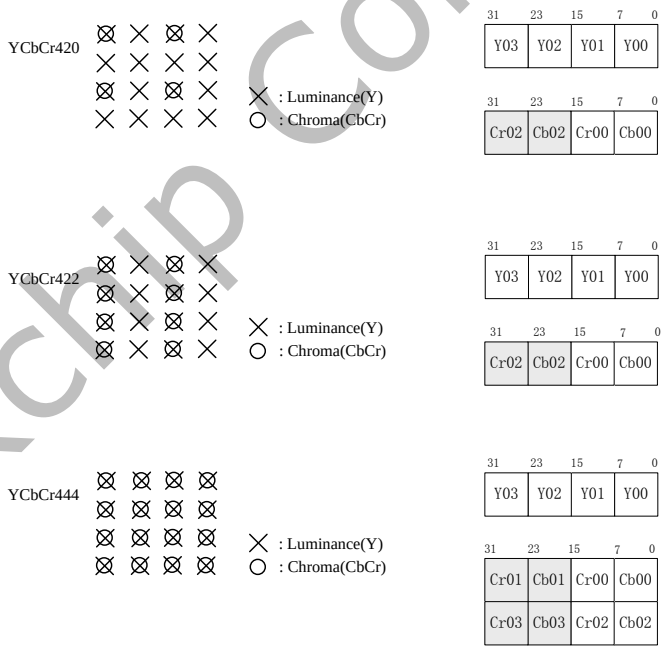


Fig. 2-3 YUV data format

YUV just support SP
YUV-8bit 32bit align

3. BPP

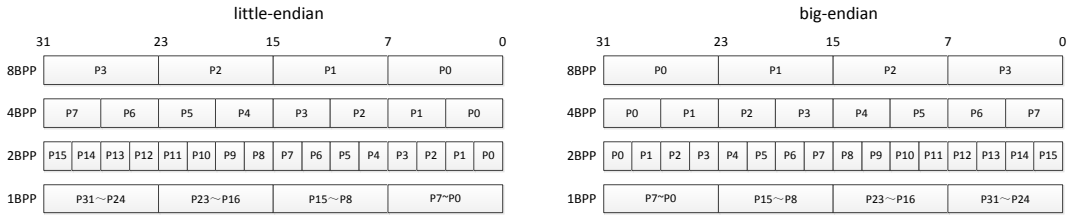


Fig. 2-4 BPP little/big endian data format

2.3.2 Pixel Data Path

Internal DMA can fetch the pixel data through AXI bus from system memory (DDR) for all the display layers. Data fetching is driven by display output requirement.

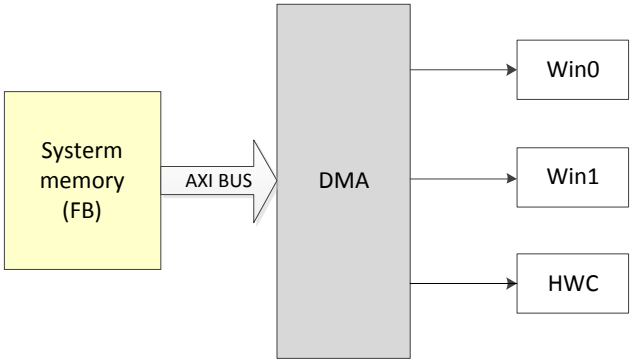


Fig. 2-5 VOP Internal DMA

2.3.3 Win Scaling

The scaling operation is the image resizing process of data transfer from the frame buffer memory to LCD panel or TV set.
Horizontal and vertical scaling factor should be set according the window scaling ratio.
Both win0 and win1 support scale, so they have the same register group.The differences are that win0 supports YUV data format (which means win1 doesn't have UV related registers)and that win1 supports alpha scale. So we take calculating win0 scaling factor and scaling start point offset for example.

1. Scaling factor

Because the Chroma data may have different sampling rate with Luma data in the memory format of YCbCr422/YCbCr420. The scaling factor of Win0 has two couples of factor registers: VOP_WIN0_SCL_FACTOR_Y/VOP_WIN0_SCL_FACTOR_CBR
Software calculates the scaling factor value using the following equations:

$$y\_rgb\_vertical\_factor=(\frac{VOP\_WIN0\_ACT\_INFO[31:16]}{VOP\_WIN0\_DSP\_INFO[31:16]})\times 2^{12}$$

$$y\_rgb\_horizontal\_factor=(\frac{VOP\_WIN0\_ACT\_INFO[15:0]}{VOP\_WIN0\_DSP\_INFO[15:0]})\times 2^{12}$$

$$yuv422\_yuv444\_Cbr\_vertical\_factor=(\frac{VOP\_WIN0\_ACT\_INFO[31:16]}{VOP\_WIN0\_DSP\_INFO[31:16]})\times 2^{12}$$

$$yuv420\_Cbr\_vertical\_factor=(\frac{VOP\_WIN0\_ACT\_INFO[31:16]/2}{VOP\_WIN0\_DSP\_INFO[31:16]})\times 2^{12}$$

$$yuv444\_Cbr\_horizontal\_factor=(\frac{VOP\_WIN0\_ACT\_INFO[15:0]}{VOP\_WIN0\_DSP\_INFO[15:0]})\times 2^{12}$$

$$yuv422\_yuv420\_Cbr\_horizontal\_factor=(\frac{VOP\_WIN0\_ACT\_INFO[15:0]/2}{VOP\_WIN0\_DSP\_INFO[15:0]})\times 2^{12}$$

2. Scaling start point offset

The x and y start point of the generated pixels can be adjusted, the offset value is in the range of 0 to 0.99.

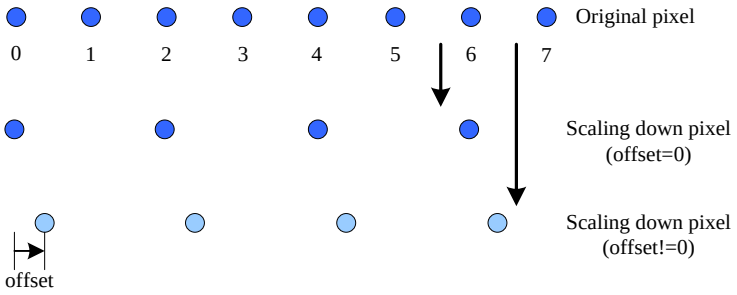


Fig. 2-6 VOP Scaling Down Offset

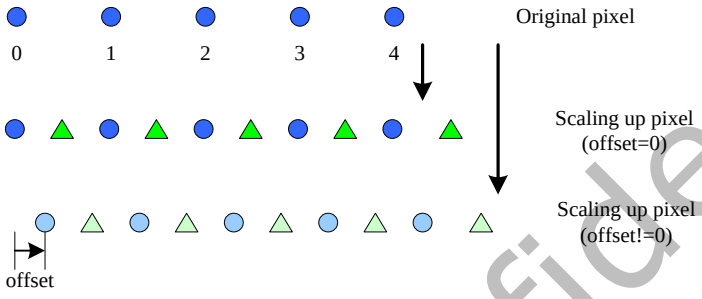


Fig. 2-7 VOP Scaling Up Offset

Table 2-1 VOP Scaling Start Point Offset Registers

scaling down/up start point offset	**Offset variable**	**Register**
Win0 YRGB vertical scaling offset	Win0_YRGB_vscl_offset	Win0_SCL_OFFSET [32:24]
Win0 YRGB horizontal scaling offset	Win0_YRGB_hscl_offset	Win0_SCL_OFFSET [23:16]
Win0 Cbr vertical scaling offset	Win0_CBR_vscl_offset	Win0_SCL_OFFSET [15:8]
Win0 Cbr horizontal scaling offset	Win0_CBR_hscl_offset	Win0_SCL_OFFSET [7:0]

2.3.4 De-flicker

It is necessary to display a non-interlaced video signal on an interlaced display panel (such as TV set). Thus "non-interlaced-to-interlaced conversion" is required.

The easiest approach is to throw away every other active scan line in each non-interlaced frame. Although the cost is minimal, there are problems with this approach. If there is a sharp vertical transition of color or intensity, it will flicker at one-half the refresh rate.

A better solution is to use two lines of non-interlaced data to generate one line of interlace data. Fast vertical transition is smoothed out over several interlace lines.

The vertical filtering of two non-interlaced lines can be done by enabling the vertical scaling offset updated dynamically in different fields, i.e, even field and odd field. The dynamic updated value of scaling offset is half of the scaling factor.

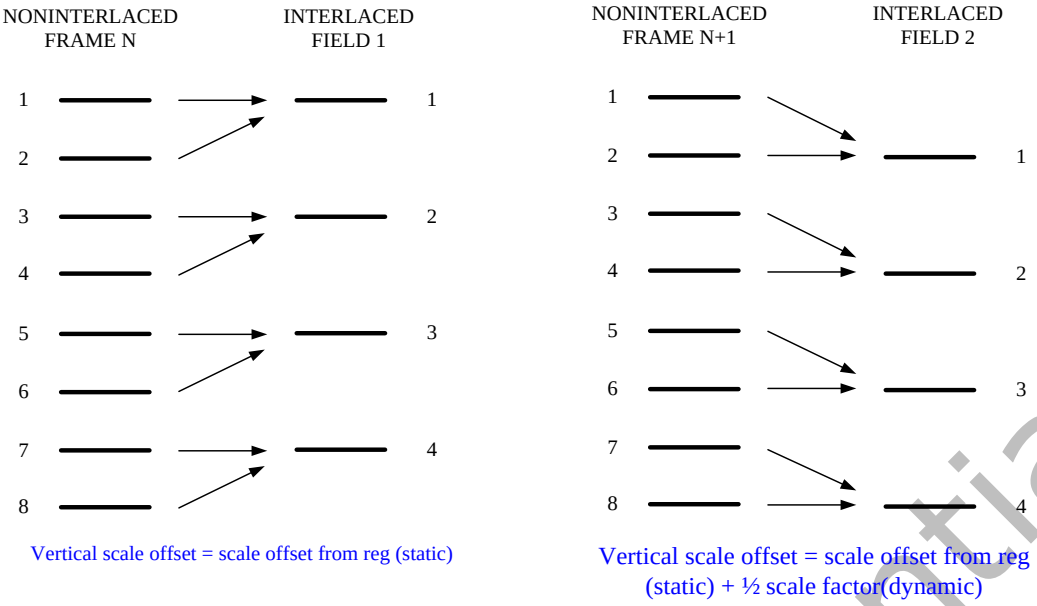


Fig. 2-8 De-flicker

2.3.5 TV ENCODER

The TV ENCODE core feature as follow:

- Single 10-bit output to on-chip VDAC
- PAL/NTSC encoding
- Programable luma filter coefficient
- Programable luma/chroma delay
- Programable brightness/contrast

There is a special registers need to be configured In TV mode.
tve_mode -> dsp_ctrl0[25]
1'b0 : NTSC mode
1'b1 : PAL mode

Other registers reference to resigister description.
There list NTSC and PAL typical register config as follow:

```
ntsc_config[][2] ={
    {0x00 , 0x000a0000} ,
    {0x04 , 0x00C07a81} ,
    {0x08 , 0x169800FC} ,
    {0x0C , 0x96B40000} ,
    {0x10 , 0x21F07BD7} ,
    {0x14 , 0x02ff0000} ,
    {0x18 , 0xF40202fd} ,
    {0x1C , 0xF332d919} ,
    {0x34 , 0x001500D6} ,
    {0x38 , 0x0100888C} ,
    {0x3C , 0x00000000} ,
    {0x50 , 0x00000000} ,
    {0x68 , 0x00000000} ,
    {0x78 , 0x0052543C} ,
    {0x8C , 0x00000002} ,
    {0x90 , 0x00008300}};

pal_config[][2] ={
    {0x00 , 0x010a0000} ,
    {0x04 , 0x00C28381} ,
    {0x08 , 0x2694011D} ,
    {0x0C , 0xB6C00880} ,
```

```
    {0x10 , 0x2A098ACB} ,
    {0x14 , 0x02ff0000} ,
    {0x18 , 0xF40202fd} ,
    {0x1C , 0xF332d919} ,
    {0x34 , 0x001500F6} ,
    {0x38 , 0x4100088A} ,
    {0x3C , 0x00000000} ,
    {0x50 , 0x00000000} ,
    {0x68 , 0x00000000} ,
    {0x78 , 0x002e553C} ,
    {0x8C , 0x00000022} ,
    {0x90 , 0x00008900}};
```

When working in TV mode ,the dclk is 27Mhz,the sw_core_clk_sel should enable.

2.3.6 VDAC

If vop working in pal/ntsc mode ,Tve_dac_dclk_en should be configured to 1'b1, the vdac clk invert can be configured at the same time.
Tve_dac_dclk_en ->vop_base_addr + 0x20[20];
Tve_dac_dclk_inv->vop_base_addr + 0x20[21];
There is a 10 bit on-chip VDAC for the TVE ENCODE.
You should configure the VDAC digital signals. GRF_SOC_CON3 is the VDAC global register, the high 16bit is the write enable signals map to low 16bits.
VDAC GRF signals as follow:

Table 2-2 VDAC Signals

GRF register	function name	function
GRF_SOC_CON3[0]	enextref	Enable control pin to allow internally generated bandgap to be probed in the analog pin 'vbg'. Under normal operation and envbg=1: 1'b1: Internal bandgap is passed to vbg pin; 1'b0: vbg pins is at high impedance.
GRF_SOC_CON3[1]	envbg	Enable control pin to power up internal bandgap. 1'b1: Internal bandgap is ON; 1'b0: Internal bandgap is OFF.
GRF_SOC_CON3[2]	endac	Enable control pin to power up the VDAC
GRF_SOC_CON3[3]	ensc	Sense comparator enable for cable connection detection of DAC
GRF_SOC_CON3[6:4]	enctr[2:0]	Enable control pins for analog biasing Test. In normal mode set enctr[2:0]=3'b000
GRF_SOC_CON3[12:7]	dacgc[5:0]	Gain setting digital input word for VDAC

The detail description of VDAC reference to VDAC chapter.

2.3.7 Virtual display

When in virtual display, the active image is part of the virtual (original) image in frame buffer memory.
The virtual width is indicated by setting VIR_STRIDE for different data format. Note that RGB/BPP has one stride(yrgb_vir_stride)； YUV has two virtual stride(yrgb_vir_stride and cbcr_vir_stride).
For RGB-8bit and YUV-8bit，the stride should be multiples of word (32-bit), with dummy bytes in the end of virtual line if the original width is not 32-bit aligned.

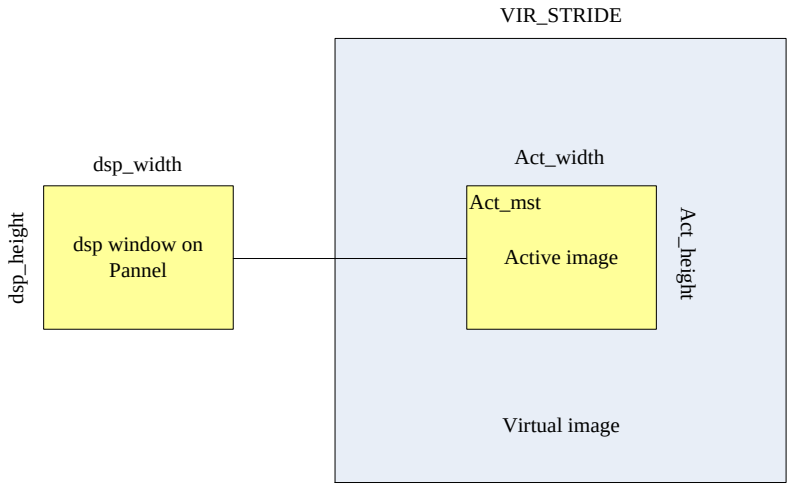


Fig. 2-9 Virtual display

2.3.8 Display process

2.3.8.1 Overlay display

There are totally 4 layers for overlay display: Background, layer0, layer1, and hardware cursor layer(HWC).

Background is a programmable solid color layer, which is always in the bottom of the display screen.

HWC is always on the top of the display screen.

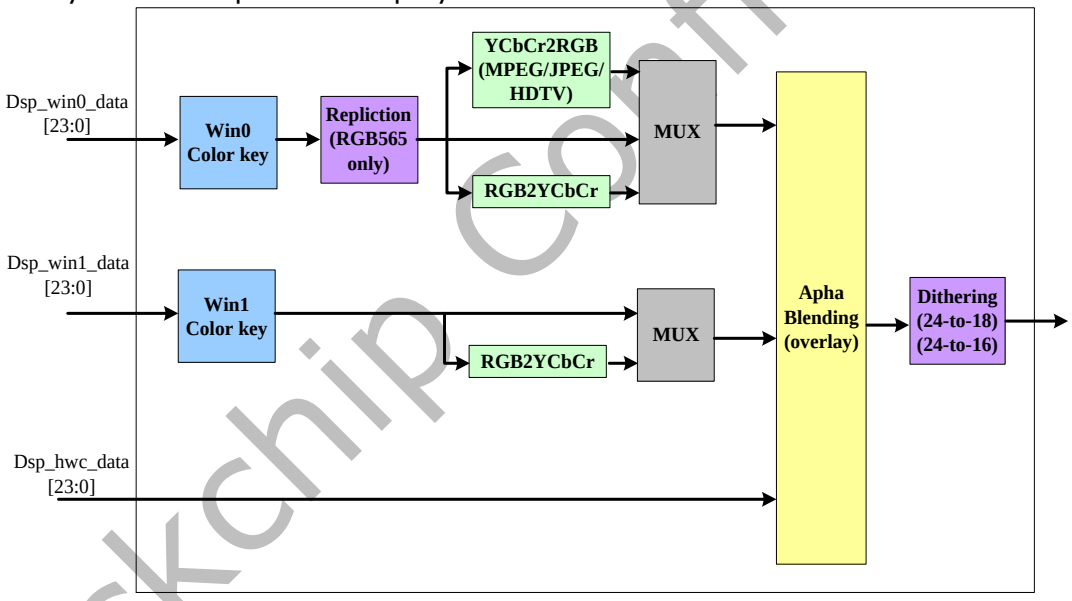


Fig. 2-10 overlay

Following figure is an example of overlay display for win0,win1 and hwc.

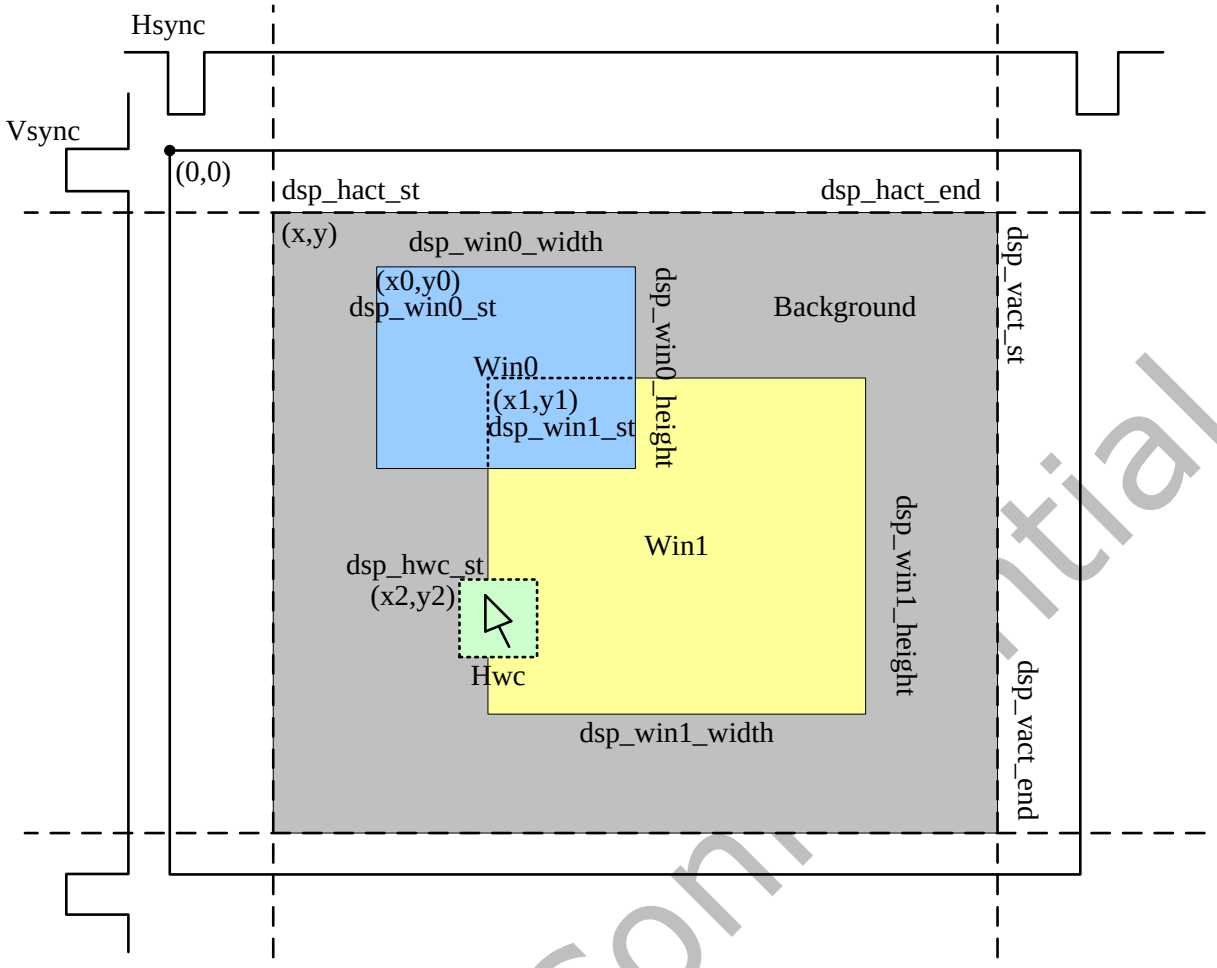


Fig. 2-11 overlay timing

2.3.8.2 Transparency color key

The transparency color key value defines the pixel treated as transparent pixel. The pixel whose value is equal to the color key value could not be visible on the screen, instead of the pixel in the under layer or solid background color.

There are two transparency color key for win0 layer and win1 layer respectively. When color key is enable, the transparency process is done after scaling but before YUV2RGB color space converter.

Moreover, transparency color key is just available for non-scaling mode.

Following figure is an example of transparency color key for win0 and win1.

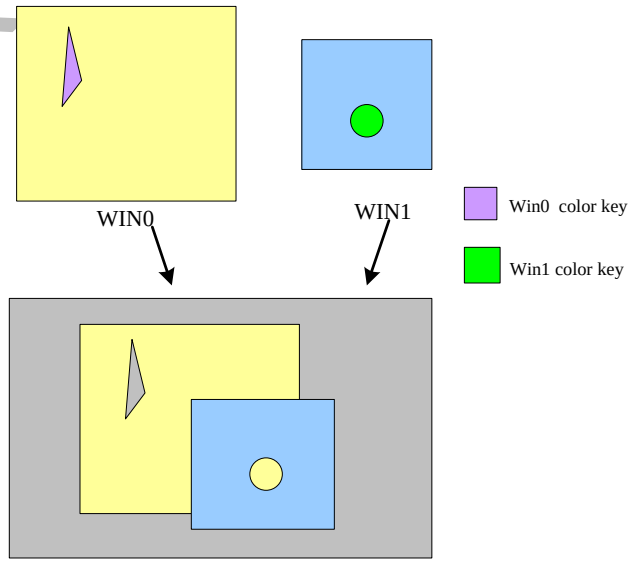


Fig. 2-12 Transparency Color Key

2.3.8.3 Replication(dither up)

If the size of panel data bus is lager than the size of source pixel data,i.e, the source input format is RGB565 and display output format is RGB888, you could do bit replication by replicating MSBs to LSBs if replication is enable or filling with "0" to LSBs if replication is disable .

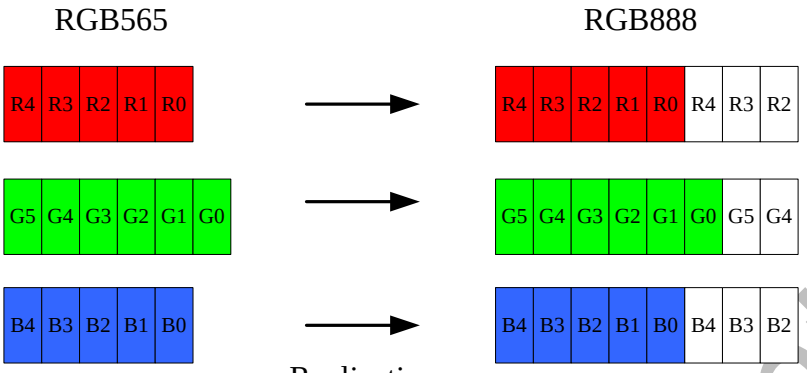


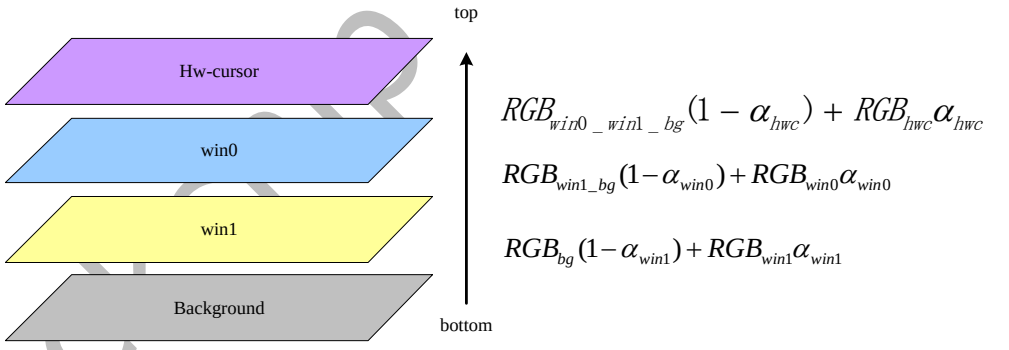
Fig. 2-13 Dither Up

2.3.8.4 Alpha blending

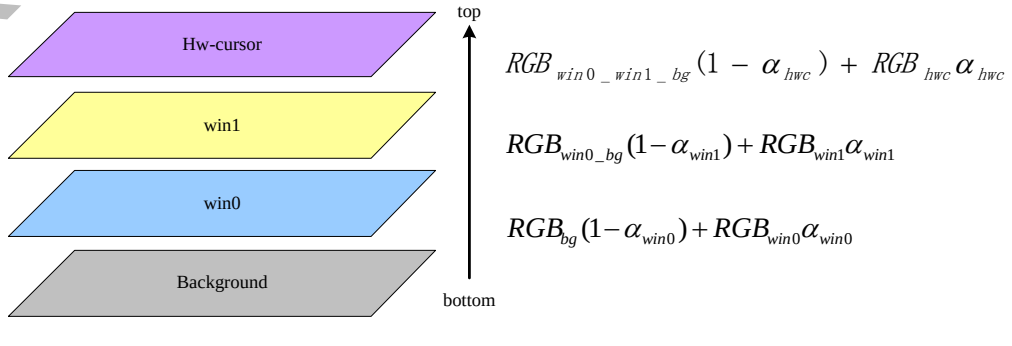
There are three alpha values for blending between four overlay layers: alpha_win0[7:0], alpha_win1[7:0], alpha_hwc[7:0].

Two blending modes are supported. One is per-pixel (ARGB) mode; the other is user-specified mode. In ARGB mode, the alpha value is in the ARGB data (Win0 and Win1 normal mode only). In user-specified mode, the alpha value comes from the register (VOP_ALPHA_CTRL[27: 4]). Pre-multiplied alpha are supported for per-pixel alpha in Win0 and Win 1, for Pre-multiplied alpha, the SRC data has already been multiplied with alpha value.

For win1 layer, it supports alpha scale, and it use "win1_aa_pre_mul" to pre_multiply RGB by alpha in hardware if RGB is not pre_multiplied by software. This is used before scaling alpha channel.



Win0 on top



Win1 on top

Fig. 2-14 VOP Alpha blending

2.3.8.5 BCSH

BCSH is used to adjust "Brightness,Contrast,Saturation,Hue,like IEP BCSH-8bit. For details,please refer to IEP chapter.
The brightness adjust support (-32,31).
The yuv data of color bar are 8bits.

2.3.8.6 Dither Down

Allegro Dither Down

Dithering is an intentional applied form of noise, using to randomize quantization error, and thereby preventing large-scaling patterns such as "banding".
The pixel value is used by dithering process to display the data in a lower color depth on the LCD panel, i.e, the source input format is RGB888 and display output format is RGB565 or RGB666. When dithering is enable, the output data is generated by dithering algorithm based on the pixel position and the value of removed bits. Otherwise, the MSBs of the pixel color components are output as display data.
There are two dither modes: "RGB888 to RGB666" and "RGB888 to RGB565".

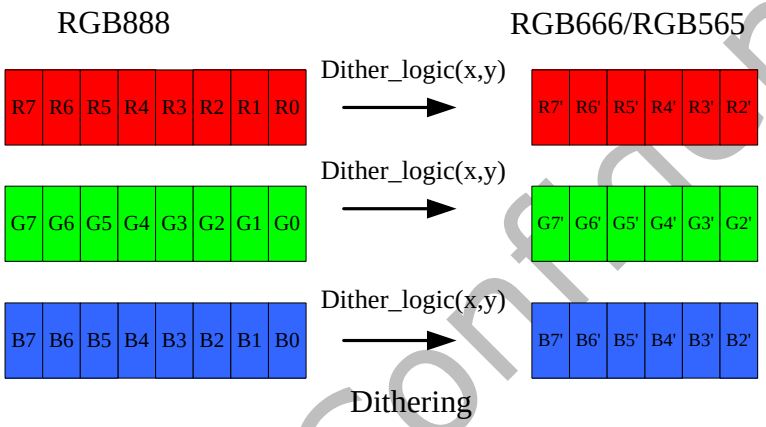


Fig. 2-15 Dither Down

2.3.8.7 Output format

Config dsp_out_mode register to adapt a variety of panel interface. As follow:

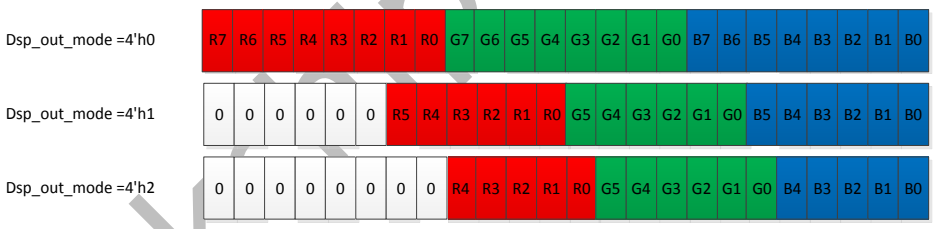


Fig. 2-16 dsp_out_mode description

2.4 Register Description

2.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP_SYS_CTRL	0x0000	W	0x00000000	System control register
VOP_DSP_CTRL0	0x0004	W	0x00000000	Display control register0
VOP_DSP_CTRL1	0x0008	W	0x01000000	Display control register1
VOP_FS_ADDR_MASK	0x000c	W	0x00000000	frame start addr mask

Name	Offset	Size	Reset Value	Description
VOP_INT_STATUS	0x0010	W	0x00000000	Interrupt status register
VOP_ALPHA_CTRL	0x0014	W	0x00000000	Blending control register
VOP_WIN0_COLOR_KEY	0x0018	W	0x00000000	Win0 color key register
VOP_WIN1_COLOR_KEY	0x001c	W	0x00000000	Win1 color key register
VOP_WIN0_YRGB_MST0	0x0020	W	0x00000000	Win0 YRGB memory start address 0
VOP_WIN0_CBR_MST0	0x0024	W	0x00000000	Win0 Cbr memory start address 0
VOP_WIN1_VIR	0x0028	W	0x00000000	Win1 virtual stride
VOP_AXI_BUS_CTRL	0x002c	W	0x00500000	Bus bandwidth ctrol signal
VOP_WIN0_VIR	0x0030	W	0x01400140	Win0 virtual stride
VOP_WIN0_ACT_INFO	0x0034	W	0x00ef013f	Win0 active window width/height
VOP_WIN0_DSP_INFO	0x0038	W	0x00ef013f	Win0 display width/height on panel
VOP_WIN0_DSP_ST	0x003c	W	0x000a000a	Win0 display start point on panel
VOP_WIN0_SCL_FACTOR_YRGB	0x0040	W	0x10001000	Win0 YRGB scaling factor
VOP_WIN0_SCL_FACTOR_CBR	0x0044	W	0x10001000	Win0 CBR scaling factor
VOP_WIN0_SCL_OFFSET	0x0048	W	0x00000000	Win0 scaling start point offset
VOP_HWC_MST	0x0058	W	0x00000000	Hwc memory start address
VOP_HWC_DSP_ST	0x005c	W	0x000a000a	Hwc display start point on panel
VOP_DSP_HTOTAL_HS_END	0x006c	W	0x014a000a	Panel scanning horizontal width and hsync pulse end point
VOP_DSP_HACT_ST_END	0x0070	W	0x000a014a	Panel active horizontal scanning start point and end point
VOP_DSP_VTOTAL_VS_END	0x0074	W	0x00fa000a	Panel scanning vertical height and vsync pulse end point
VOP_DSP_VACT_ST_END	0x0078	W	0x000a00fa	Panel active vertical scanning start point and end point
VOP_DSP_VS_ST_END_F1	0x007c	W	0x00000000	Vertical scanning start point and vsync pulse end point of even filed in interlace mode
VOP_DSP_VACT_ST_END_F1	0x0080	W	0x00000000	Vertical scanning active start point and end point of even filed in interlace mode
VOP_GATHER_TRANSFER	0x0084	W	0x00008220	Gather transfer ctrol signal
VOP_REG_CFG_DONE	0x0090	W	0x00000000	Register config done flag
VOP_VERSION	0x0094	W	0x00000000	version for vop
VOP_WIN1_YRGB_MST0	0x00a0	W	0x00000000	Win1 YRGB memory start address
VOP_WIN1_ACT_INFO	0x00b4	W	0x00ef013f	Win1 active window width/height
VOP_WIN1_DSP_INFO	0x00b8	W	0x00ef013f	Win1 display width/height on panel
VOP_WIN1_DSP_ST	0x00bc	W	0x000a000a	Win1 display start point on panel
VOP_WIN1_SCL_FACTOR_YRGB	0x00c0	W	0x10001000	Win1 YRGB scaling factor
VOP_WIN1_SCL_OFFSET	0x00c8	W	0x00000000	Win1 scaling start point offset

Name	Offset	Size	Reset Value	Description
VOP_BCSH_CTRL	0x00d0	W	0x00000000	Brightness/Contrast enhancement/Saturation/Hue contrl
VOP_BCSH_COL_BAR	0x00d4	W	0x00000000	Colorbar YUV value
VOP_BCSH_BCS	0x00d8	W	0x00000000	Brightness/Contrast enhancement/Saturation
VOP_BCSH_H	0x00dc	W	0x00000000	Hue
VOP_TV_CTRL	0x0200	W	0x00000000	tv mode control register
VOP_TV_SYNC_TIMING	0x0204	W	0x00000000	sync timing ctrl register
VOP_TV_ACT_TIMING	0x0208	W	0x00000000	act timing ctrl register
VOP_TV_ADJ_TIMING	0x020c	W	0x00000000	adjust timing register
VOP_TV_FRQ_SC	0x0210	W	0x00000000	Sub-carrier Frequency
VOP_TV_FILTER0	0x0214	W	0x00000000	Filter 0
VOP_TV_FILTER1	0x0218	W	0x00000000	Filter 1
VOP_TV_FILTER2	0x021c	W	0x00000000	Filter 2
VOP_TV_ACT_ST	0x0234	W	0x00000000	
VOP_TV_ROUTING	0x0238	W	0x00000000	Routing
VOP_TV_SYNC_ADJUST	0x0250	W	0x00000000	Sync Adjust
VOP_TV_STATUS	0x0254	W	0x00000000	TV Status register
VOP_TV_RST	0x0268	W	0x00000000	tv reset Control
VOP_TV_SATURATION	0x0278	W	0x00000000	Colour Burst and Saturation
VOP_TV_BANDWIDTH_CTRL	0x028c	W	0x00000000	Chroma bandwidth
VOP_TV_BRIGHTNESS_CONTRAST	0x0290	W	0x00000000	Brightness and Contrast
VOP_MMU_DTE_ADDR	0x0300	W	0x00000000	MMU current page Table address
VOP_MMU_STATUS	0x0304	W	0x00000000	MMU status register
VOP_MMU_COMMAND	0x0308	W	0x00000000	MMU command register
VOP_MMU_PAGE_FAULT_ADDR	0x030c	W	0x00000000	MMU logical address of last page fault
VOP_MMU_ZAP_ONE_LINE	0x0310	W	0x00000000	MMU Zap cache line register
VOP_MMU_INT_RAWSTAT	0x0314	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_CLEAR	0x0318	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_MASK	0x031c	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_STATUS	0x0320	W	0x00000000	MMU raw interrupt status register
VOP_MMU_AUTO_GATING	0x0324	W	0x00000001	mmu auto gating
VOP_HWC_LUT_ADDR	0x0800	W	0x00000000	Access entry for hwc LUT memory(size is word only)
VOP_DSP_LUT_ADDR	0x0c00	W	0x00000000	Access entry for DSP LUT memory(size is word only)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

2.4.3 Detail Register Description

VOP_SYS_CTRL
Address: Operational Base + offset (0x0000)
System control register

Bit	Attr	Reset Value	Description
31	RW	0x0	auto_gating_en VOP layer axi-clk auto gating enable 1'b0: disable 1'b1: enable
30	RW	0x0	vop_standby_en VOP standby mode Writing "1" to turn VOP into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the VOP go back to work immediately. 1'b0: disable 1'b1: enable * Black display is recommended before setting standby mode enable.
29	RW	0x0	vop_dma_stop VOP DMA stop mode 1'b0: disable 1'b1: enable * If DMA is working, the stop mode would not be active until current bus transfer is finished.
28:27	RO	0x0	reserved
26	RW	0x0	hwc_load_en Hardware cursor data reload enable 1'b0: disable 1'b1: enable *Setting this bit would reload the Hwc data. It would be auto cleared after reload finish.
25:24	RW	0x0	dma_burst_length DMA read Burst length 2'b00: burst16 (burst 15 in rgb888 pack mode) 2'b01: burst8 (burst 12 in rgb888 pack mode) 2'b10: burst4 (burst 6 in rgb888 pack mode)
23	RW	0x0	win1_no_outstanding Win1 AXI master read outstanding 1'b0: enable 1'b1: disable

Bit	Attr	Reset Value	Description
22	RW	0x0	win0_no_outstanding Win0 AXI master read outstanding 1'b0: enable 1'b1: disable
21	RO	0x0	reserved
20	RW	0x0	win1_alpha_swap Win1 RGB alpha swap 1'b0: ARGB 1'b1: RGBA
19	RW	0x0	win1_rb_swap Win1 RGB Red and Blue swap 1'b0: RGB 1'b1: BGR
18	RW	0x0	win0_uv_swap Win0 CbCr swap 1'b0: CrCb 1'b1: CbCr
17	RW	0x0	win0_y8_swap Win0 Y middle 8-bit swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
16	RW	0x0	win0_alpha_swap Win0 RGB alpha swap 1'b0: ARGB 1'b1: RGBA
15	RW	0x0	win0_rb_swap Win0 RGB Red and Blue swap 1'b0: RGB 1'b1: BGR
14	RW	0x0	tve_dac_select 1'b0:dac disable 1'b1:dac enable note:just for FPGA verivication using
13	RW	0x0	tve_mode_slave tve_mode_select 1'b0:master mode 1'b1:slave mode note:for FPGA verivication using
12:11	RO	0x0	reserved
10	RW	0x0	hwc_size Hwc size select 1'b0: 32x32 1'b1: 64x64

Bit	Attr	Reset Value	Description
9	RW	0x0	hwc_lut_en 1'b0: disable 1'b1: enable *This bit should be "0" when CPU updates the LUT, and should be "1" when hwc LUT mode enable.
8:6	RW	0x0	win1_data_fmt Win1 source Format 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 others: reserved
5:3	RW	0x0	win0_data_fmt Win0 source data Format 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100 : YCbCr420 3'b101 : YCbCr422 3'b110 : YCbCr444 others: reserved
2	RW	0x0	hwc_en Hwc enable bit 1'b0: Hwc layer disable 1'b1: Hwc layer enable
1	RW	0x0	win1_en Win1 enable bit 1'b0: Win1 layer disable 1'b1: Win1 layer enable
0	RW	0x0	win0_en Win0 enable bit 1'b0: Win0 layer disable 1'b1: Win0 layer enable

VOP_DSP_CTRL0
Address: Operational Base + offset (0x0004)
Display control register0

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_yrgb_deflick
30	RW	0x0	alpha_mode_sel1 alpha mode select 1 1'b0 : alpha value no change 1'b1 : alpha = alpha + alpha[7]

Bit	Attr	Reset Value	Description
29	RW	0x0	alpha_mode_sel0 alpha mode select 0 1'b0 : Non-premultiplied alpha 1'b1 : Premultiplied alpha
28	RW	0x0	hwc_alpha_mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
27:26	RO	0x0	reserved
25	RW	0x0	tve_mode tve mode select 1'b0 : NTSC mode 1'b1 : PAL mode
24	RO	0x0	reserved
23	RW	0x0	yuv_clip YCrCb clip 1'b0: disable, YCbCr no clip 1'b1: enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CBCR clip: 16~239
22	RO	0x0	reserved
21:20	RW	0x0	win0_csc_mode Win0 YUV2RGB Color space conversion: 2'b00: mpeg 2'b01: jpeg 2'b10: hd 2'b11: reserved
19	RW	0x0	win1_alpha_mode Win1 alpha mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
18	RW	0x0	win0_alpha_mode Win0 alpha mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
17	RW	0x0	win0_cbr_deflick Win0 Cbr deflick mode 1'b0: disable 1'b1: enable
16	RW	0x0	win0_yrgb_deflick Win0 YRGB deflick mode 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
15	RW	0x0	win1_interlace_read Win1 interlace read mode 1'b0: disable 1'b1: enable
14:13	RO	0x0	reserved
12	RW	0x0	dsp_interlace_en Interlace display enable 1'b0: disable 1'b1: enable *This mode is related to the ITU-R656 output, the display timing of odd field must be set correctly. (vop_dsp_vs_st_end_f1/vop_dsp_vact_end_f1)
11:10	RO	0x0	reserved
9	RW	0x0	dither_up dither up RGB565 to RGB888 enable 1'b0: disable 1'b1: enable
8	RW	0x0	dsp_win0_top Win0 and Win1 position swap 1'b0: win1 on the top of win0 1'b1: win0 on the top of win1
7	RW	0x0	dsp_dclk_pol DCLK invert enable 1'b0: normal 1'b1: invert
6	RW	0x0	dsp_den_pol DEN polarity 1'b0: positive 1'b1: negative
5	RW	0x0	dsp_vsync_pol VSYNC polarity 1'b0: negative 1'b1: positive
4	RW	0x0	dsp_hsync_pol HSYNC polarity 1'b0: negative 1'b1: positive
3:0	RW	0x0	dsp_out_mode Display output format 4'b0000: Parallel 24-bit RGB888 output R[7:0],G[7:0],B[7:0] 4'b0001: Parallel 18-bit RGB666 output 6'b0,R[5:0],G[5:0],B[5:0] 4'b0010: Parallel 16-bit RGB565 output 8'b0,R[4:0],G[5:0],B[4:0] Others: Reserved.

VOP_DSP_CTRL1
Address: Operational Base + offset (0x0008)
Display control register1

Bit	Attr	Reset Value	Description
31	RW	0x0	dsp_out_zero DENoutput software ctrl 1'b0：normal output 1'b1：all output '0' means:hsync,vsync,den =000
30	RW	0x0	dsp_dummy_swap Display dummy swap enable 1'b0: B+G+R+dummy 1'b1: dummy+B+G+R
29	RW	0x0	dsp_delta_swap Display delta swap enable 1'b0: disable 1'b1: enable *See detail description in Delta display charpter.
28	RW	0x0	dsp_rg_swap Display output red and green swap enable 1'b0: RGB 1'b1: GRB
27	RW	0x0	dsp_rb_swap Display output red and blue swap enable 1'b0: RGB 1'b1: BGR
26	RW	0x0	dsp_bg_swap Display output blue and green swap enable 1'b0: RGB 1'b1: RBG
25	RW	0x0	dsp_black_en Black display mode When this bit enable, the pixel data output is all black (0x000000)
24	RW	0x1	dsp_blank_en Blank display mode When this bit enable, the hsync/vsync/den output is blank
23:16	RW	0x00	dsp_bg_red Background Red color
15:8	RW	0x00	dsp_bg_green Background Green color
7:0	RW	0x00	dsp_bg_blue Background Blue color

VOP_FS_ADDR_MASK
Address: Operational Base + offset (0x000c)
frame start addr mask

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_INT_STATUS
Address: Operational Base + offset (0x0010)
Interrupt status register

Bit	Attr	Reset Value	Description
31	RO	0x0	line_flag_raw_status Line flag raw Interrupt status
30	RO	0x0	fs_raw_status Frame start raw interrupt status
29	RO	0x0	win1_empty_intr_status win1 data empty interrupt status
28	RO	0x0	win0_empty_intr_status win0 data empty interrupt status
27	W1C	0x0	win1_empty_intr_clr win1 data empty interrupt clear(auto clear)
26	W1C	0x0	win0_empty_intr_clr win0 data empty interrupt clear(auto clear)
25	RW	0x0	win1_empty_intr_en win1 data empty interrupt enable signal 1'b0: disable 1'b1: enable
24	RW	0x0	win0_empty_intr_en win0 data empty interrupt enable signal 1'b0: disable 1'b1: enable
23:12	RW	0x000	dsp_line_frag_num Line number of the Line flag interrupt The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).
11	W1C	0x0	bus_error_intr_clr Bus error Interrupt clear (Auto clear)
10	W1C	0x0	line_frag_intr_clr Line flag Interrupt clear (Auto clear)
9	W1C	0x0	fs_intr_clr Frame start interrupt clear (Auto clear)
8	W1C	0x0	dsp_hold_valid_intr_clr display hold valid interrupt clear (Auto clear)
7	RW	0x0	bus_error_intr_en Bus error interrupt enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
6	RW	0x0	line_frag_intr_en Line flag Interrupt enable 1'b0: disable 1'b1: enable
5	RW	0x0	fs_intr_en Frame start interrupt enable 1'b0: disable 1'b1: enable
4	RW	0x0	dsp_hold_valid_intr_en display hold valid interrupt enable 1'b0: disable 1'b1: enable
3	RO	0x0	bus_error_intr Bus error Interrupt status
2	RO	0x0	line_frag_intr Line flag Interrupt status
1	RO	0x0	fs_intr Frame start interrupt status
0	RO	0x0	dsp_hold_valid_intr display hold valid interrupt status

VOP_ALPHA_CTRL
Address: Operational Base + offset (0x0014)
Blending control register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	hwc_alpha_value HWC alpha blending value
19:12	RW	0x00	win1_alpha_value Win1 alpha blending value
11:4	RW	0x00	win0_alpha_value Win0 alpha blending value
3	RW	0x0	win1_aa_pre_mul win1 pre multiply for alpha scale
2	RW	0x0	hwc_alpha_en HWC alpha blending enable 1'b0: disable 1'b1: enable
1	RW	0x0	win1_alpha_en Win1 alpha blending enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	hwc_alpha_value HWC alpha blending value
19:12	RW	0x00	win1_alpha_value Win1 alpha blending value
11:4	RW	0x00	win0_alpha_value Win0 alpha blending value
3	RW	0x0	win1_aa_pre_mul win1 pre multiply for alpha scale
2	RW	0x0	hwc_alpha_en HWC alpha blending enable 1'b0: disable 1'b1: enable
1	RW	0x0	win1_alpha_en Win1 alpha blending enable 1'b0: disable 1'b1: enable
0	RW	0x0	win0_alpha_en Win0 alpha blending enable 1'b0: disable 1'b1: enable

VOP_WIN0_COLOR_KEY
Address: Operational Base + offset (0x0018)
Win0 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win0_key_en Win0 transparency color key enable 1'b0: disable 1'b1: enable
23:0	RW	0x000000	win0_key_color Win0 key color

VOP_WIN1_COLOR_KEY
Address: Operational Base + offset (0x001c)
Win1 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win1_key_en Win1 transparency color key enable 1'b0: disable 1'b1: enable
23:0	RW	0x000000	win1_key_color Win1 key color

VOP_WIN0_YRGB_MST0
Address: Operational Base + offset (0x0020)
Win0 YRGB memory start address 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb0_mst win0 YRGB frame buffer memory start address 0

VOP_WIN0_CBR_MST0
Address: Operational Base + offset (0x0024)
Win0 Cbr memory start address 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbr0_mst win0 CBR frame buffer memory start address 0

VOP_WIN1_VIR
Address: Operational Base + offset (0x0028)
Win1 virtual stride

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	win1_vir_stride

VOP_AXI_BUS_CTRL
Address: Operational Base + offset (0x002c)
Bus bandwidth ctrol signal

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_io_pad_clk_sel
30	RW	0x0	sw_core_clk_sel
29:24	RO	0x0	reserved
23	RW	0x0	hdmi_dclk_inv hdmi dclk invert select bit 1'b0:hdmi dclk inv disable 1'b1:hdmi dclk inv enable
22	RW	0x1	hdmi_dclk_en hdmi dclk enable bit 1'b0:hdmi dclk disable 1'b1:hdmi dclk enable
21	RW	0x0	tve_dac_dclk_inv Field0000 Abstract 1'b0:tve dac dclk inv disable 1'b1:tve dac dclk inv enable
20	RW	0x1	tve_dac_dclk_en tve dac dclk enable bit 1'b0:tve dac dclk disable 1'b1:tve dac dclk enable

19	RW	0x0	sw_hdmi_clk_i_sel hdmi io clk select bit 1'b0: select dclk to hdmi io 1'b1: select dclk_core to hdmi io
18:17	RO	0x0	reserved
16:12	RW	0x00	sw_axi_max_outstand_num Max number of AXI read outstanding
11	RW	0x0	sw_axi_max_outstand_en AXI read oustanding limited enable bit 1'b0: disable 1'b1: enable
10	RW	0x0	sw_vop_mmu_en Vop MMU enable bit 1'b0: disable 1'b1: enable
9:6	RW	0x0	sw_noc_hurry_threshold Noc hurry threshold 1'b0: disable 1'b1: enable
5:4	RW	0x0	sw_noc_hurry_value Noc hurry level
3	RW	0x0	sw_noc_hurry_en Noc hurry mode enable bit 1'b0: disable 1'b1: enable
2:1	RW	0x0	sw_noc_qos_value Noc QoS level
0	RW	0x0	sw_noc_qos_en Noc QoS mode enable bit 1'b0: disable 1'b1: enable

VOP_WIN0_VIR
Address: Operational Base + offset (0x0030)
Win0 virtual stride

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win0_cbr_vir_stride Number of words of Win0 cbr Virtual width UV420 : ceil(win0_vir_width/4) UV422 : ceil(win0_vir_width/4) UV444 : ceil(win0_vir_width/2)
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win0_cbr_vir_stride Number of words of Win0 cbr Virtual width UV420 : ceil(win0_vir_width/4) UV422 : ceil(win0_vir_width/4) UV444 : ceil(win0_vir_width/2)
15:13	RO	0x0	reserved
12:0	RW	0x0140	win0_yrgb_vir_stride Win0 Virtual stride Number of words of Win0 yrgb Virtual width ARGB888 : win0_vir_width RGB888 : (win0_vir_width*3/4) + (win0_vir_width%3) RGB565 : ceil(win0_vir_width/2) YUV : ceil(win0_vir_width/4)

VOP_WIN0_ACT_INFO
Address: Operational Base + offset (0x0034)
Win0 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win0_act_height Win0 active(original) window height win_act_height = (win0 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win0_act_width Win0 active(original) window width win_act_width = (win0 horizontal size -1)

VOP_WIN0_DSP_INFO
Address: Operational Base + offset (0x0038)
Win0 display width/height on panel

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x0ef	dsp_win0_height Win0 display window height win0_dsp_height = (win0 vertical size -1)
15:11	RO	0x0	reserved
10:0	RW	0x13f	dsp_win0_width Win0 display window width win0_dsp_width = (win0 horizontal size -1)

VOP_WIN0_DSP_ST
Address: Operational Base + offset (0x003c)
Win0 display start point on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_win0_yst Win0 vertical start point(y) of the Panel scanning
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_win0_xst Win0 horizontal start point(x) of the Panel scanning

VOP_WIN0_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0040)
Win0 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_yrgb Win0 YRGB vertical scaling factor factor=((VOP_WIN0_ACT_INFO[31:16])/(VOP_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_yrgb Win0 YRGB horizontal scaling factor factor=((VOP_WIN0_ACT_INFO[15:0])/(VOP_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_FACTOR_CBR
Address: Operational Base + offset (0x0044)
Win0 CBR scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_cbr Win0 CBR vertical scaling factor YCbCr420: factor=((VOP_WIN0_ACT_INFO[31:16]/2)/(VOP_WIN0_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((VOP_WIN0_ACT_INFO[31:16])/(VOP_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_cbr Win0 CBR horizontal scaling factor YCbCr422,YCbCr420: factor=((VOP_WIN0_ACT_INFO[15:0]/2)/(VOP_WIN0_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((VOP_WIN0_ACT_INFO[15:0])/(VOP_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_OFFSET

Address: Operational Base + offset (0x0048)
Win0 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_vs_offset_cbr Cbr Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
23:16	RW	0x00	win0_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win0_hs_offset_cbr Cbr Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win0_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_RESERVED_0X4C
Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_RESERVED_0X50
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_RESERVED_0X54
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_HWC_MST
Address: Operational Base + offset (0x0058)
Hwc memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_mst HWC data memory start address

VOP_HWC_DSP_ST
Address: Operational Base + offset (0x005c)
Hwc display start point on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x00a	dsp_hwc_yst HWC vertical start point(y) of the Panel scanning
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_hwc_xst HWC horizontal start point(x) of the Panel scanning

VOP_HWC_RESERVED0
Address: Operational Base + offset (0x0060)
Hwc LUT color 0

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_HWC_RESERVED1
Address: Operational Base + offset (0x0064)
Hwc LUT color 1

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_HWC_RESERVED2
Address: Operational Base + offset (0x0068)
Hwc LUT color 2

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_DSP_HTOTAL_HS_END
Address: Operational Base + offset (0x006c)
Panel scanning horizontal width and hsync pulse end point

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x14a	dsp_htotal Panel display scanning horizontal period
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_hs_end Panel display scanning hsync pulse width

VOP_DSP_HACT_ST_END
Address: Operational Base + offset (0x0070)
Panel active horizontal scanning start point and end point

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_hact_st Panel display scanning horizontal active start point
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x14a	dsp_hact_end Panel display scanning horizontal active end point

VOP_DSP_VTOTAL_VS_END
Address: Operational Base + offset (0x0074)
Panel scanning vertical height and vsync pulse end point

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0fa	dsp_vtotal Panel display scanning vertical period.
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_vs_end Panel display scanning vsync pulse width

VOP_DSP_VACT_ST_END
Address: Operational Base + offset (0x0078)
Panel active vertical scanning start point and end point

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_vact_st Panel display scanning vertical active start point
15:12	RO	0x0	reserved
11:0	RW	0x0fa	dsp_vact_end Panel display scanning vertical active end point

VOP_DSP_VS_ST_END_F1
Address: Operational Base + offset (0x007c)
Vertical scanning start point and vsync pulse end point of even filed in interlace mode

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode)

VOP_DSP_VACT_ST_END_F1
Address: Operational Base + offset (0x0080)
Vertical scanning active start point and end point of even filed in interlace mode

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

VOP_GATHER_TRANSFER
Address: Operational Base + offset (0x0084)
Gather transfer ctrol signal

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x8	win1_axi_gather_num
11	RO	0x0	reserved
10:8	RW	0x2	win0_cbr_axi_gather_num
7:4	RW	0x2	win0_yrgb_axi_gather_num
3	RO	0x0	reserved
2	RW	0x0	win1_axi_gather_en win1 dma channel AXI read transfer gather 1'b0: disable 1'b1: enable
1	RW	0x0	win0_cbr_axi_gather_en win0 cb/cr dma channel AXI read transfer gather 1'b0: disable 1'b1: enable
0	RW	0x0	win0_yrgb_axi_gather_en win0 yrgb dma channel AXI read transfer gather 1'b0: disable 1'b1: enable

VOP_REG_CFG_DONE
Address: Operational Base + offset (0x0090)
Register config done flag

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	reg_load_en vop register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

VOP_VERSION
Address: Operational Base + offset (0x0094)
version for vop

Bit	Attr	Reset Value	Description
31:24	RO	0x00	major IP major vertion used for IP structure
23:16	RO	0x00	minor minor vertion big feature change under same structure
15:0	RO	0x0000	svnbuild svn number rtl current svn number

VOP_WIN1_YRGB_MST0
Address: Operational Base + offset (0x00a0)
Win1 YRGB memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb0_mst win0 YRGB frame buffer memory start address 0

VOP_RESERVED_0XA4
Address: Operational Base + offset (0x00a4)
Win1 Cbr memory start address

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_RESERVED_0XA8
Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_RESERVED_0XAC
Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_RESERVED_0XB0
Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_WIN1_ACT_INFO
Address: Operational Base + offset (0x00b4)
Win1 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win1_act_height Win1 active(original) window height win_act_height = (win1 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win1_act_width Win1 active(original) window width win_act_width = (win1 horizontial size -1)

VOP_WIN1_DSP_INFO
Address: Operational Base + offset (0x00b8)
Win1 display width/height on panel

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x0ef	dsp_win1_height Win1 display window height win1_dsp_height = (win1 vertical size -1)
15:11	RO	0x0	reserved
10:0	RW	0x13f	dsp_win1_width Win1 display window width win1_dsp_width = (win1 horizontial size -1)

VOP_WIN1_DSP_ST
Address: Operational Base + offset (0x00bc)
Win1 display start point on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_win1_yst Win1 vertical start point(y) of the Panel scanning
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_win1_xst Win1 horizontal start point(x) of the Panel scanning

VOP_WIN1_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x00c0)
Win1 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_yrgb Win1 YRGB vertical scaling factor: factor=((LCDC_WIN1_ACT_INFO[31:16])/(LCDC_WIN1_DSP_INFO[31:16]))*2^12

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_yrgb Win1 YRGB vertical scaling factor: factor=((LCDC_WIN1_ACT_INFO[31:16])/(LCDC_WIN1_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win1_hs_factor_yrgb Win1 YRGB horizontal scaling factor: factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12

VOP_RESERVED_0XC4
Address: Operational Base + offset (0x00c4)
Win1 CBR scaling factor

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_WIN1_SCL_OFFSET
Address: Operational Base + offset (0x00c8)
Win1 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	win1_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RO	0x0	reserved
7:0	RW	0x00	win1_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_BCSH_CTRL
Address: Operational Base + offset (0x00d0)
Brightness/Contrast enhancement/Saturation/Hue contrl

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	bcsh_csc_mode Color space conversion: 2'b00: mpeg 2'b01: jpeg 2'b10: hd 2'b11: Bypass
3:2	RW	0x0	video_mode 2'b00 : black 2'b01 : blue 2'b10 : color bar 2'b11 : normal video
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	bcsh_csc_mode Color space conversion: 2'b00: mpeg 2'b01: jpeg 2'b10: hd 2'b11: Bypass
3:2	RW	0x0	video_mode 2'b00 : black 2'b01 : blue 2'b10 : color bar 2'b11 : normal video
1	RO	0x0	reserved
0	RW	0x0	bcsh_en 1'b0 : bcsh bypass 1'b1 : bcsh enable

VOP_BCSH_COL_BAR
Address: Operational Base + offset (0x00d4)
Colorbar YUV value

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	color_bar_v
15:8	RW	0x00	color_bar_u
7:0	RW	0x00	color_bar_y

VOP_BCSH_BCS
Address: Operational Base + offset (0x00d8)
Brightness/Contrast enhancement/Saturation

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sat_con Saturation*Contrast*256 : 0,1.992*1.992
15:8	RW	0x00	contrast Contrast*256 : 0,1.992
7:6	RO	0x0	reserved
5:0	RW	0x00	brightness Brightness : -128,127

VOP_BCSH_H
Address: Operational Base + offset (0x00dc)
Hue

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

15:8	RW	0x00	cos_hue cos hue value
7:0	RW	0x00	sin_hue sin hue value

VOP_TV_CTRL
Address: Operational Base + offset (0x0200)
tv mode control register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	cvbs_mode 1'b0: Encoding is NTSC 1'b1: Encoding is PAL
23:20	RO	0x0	reserved
19:18	RW	0x0	clk_upstream_en 2'b00: Reserved 2'b01: Upstream enable is 1 * pix_clk (HDTV) 2'b10: Upstream enable is 1/2* pix_clk (SDTV) 2'b11: Reserved
17:16	RW	0x0	timing_en 2'b00: Reserved 2'b01: Timing enable is 1 * pix_clk (HDTV) 2'b10: Timing enable is 1 * pix_clk (SDTV) 2'b11: Reserved
15:11	RO	0x0	reserved
10:9	RW	0x0	filter_gain 2'b00: Luma Filter gain is 1.0 (default value) 2'b01: Luma Filter gain is 0.5 2'b10: Luma Filter gain is 2.0 2'b11: Reserved
8	RW	0x0	filter_upsample 1'b0: Luma Filter output is sampled at 13.5 MHz 1'b1: Luma Filter output is up-sampled to 27 MHz
7:3	RO	0x0	reserved
2:1	RW	0x0	csc_path_sel 2'b00: RGB input to RGB+YUV444 output 2'b01: YUV422 input to YUV444 output 2'b10: Reserved 2'b11: Bypass (YUV444 input to YUV444 output)
0	RO	0x0	reserved

VOP_TV_SYNC_TIMING
Address: Operational Base + offset (0x0204)
sync timing ctrl register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	h_fp Delay to the end of colour burst from H Sync Start , num of 27Mhz clk cycle
15:8	RW	0x00	h_bp Delay to the start of the colour burst from H Sync Start , num of 27Mhz clk cycle
7:0	RW	0x00	h_pw Width of horizontal sync from H Sync Start , num of 27Mhz clk cycle

VOP_TV_ACT_TIMING
Address: Operational Base + offset (0x0208)
act timing ctrl register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	tv_syncs 4'b0000: Sync generator is stopped 4'b0001: 525/60 interlaced 4'b0010: 625/50 interlaced other : reserved
27:16	RW	0x000	h_act_end Delay to the end of active video from H Sync Start , num of 27Mhz clk cycle
15:13	RO	0x0	reserved
12	RW	0x0	sc_rst_en Subcarrier reset enable 1'b0: Subcarrier phase is not reset regularly 1'b1: Subcarrier phase is reset every four fields (NTSC) or eight fields (PAL)
11:0	RW	0x000	h_act_st Delay to the start of the active video from H Sync Start , num of 27Mhz clk cycle

VOP_TV_ADJ_TIMING
Address: Operational Base + offset (0x020c)
adjust timing register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	luma_delay_1 Programmable delay for Luma relative to Chroma
27:16	RW	0x000	h_total Total number of output pixels per line. 525/60 = 1716 625/50 = 1728
15:8	RO	0x0	reserved
7:0	RW	0x00	sc_phase Phase offset applied if subcarrier phase is reset (1.4 degrees per lsb)

VOP_TV_FRQ_SC
Address: Operational Base + offset (0x0210)
Sub-carrier Frequency

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dds_incr colour subcarrier counter . Recommended settings (for 27.00 MHz) are: NTSC: 0x21F07BD7 PAL : 0x2A098ACB

VOP_TV_FILTER0
Address: Operational Base + offset (0x0214)
Filter 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	coeff3 filter coefficients 3
23:16	RW	0x00	coeff2 filter coefficients 2
15:8	RW	0x00	coeff1 filter coefficients 1
7:0	RW	0x00	coeff0 filter coefficients 0

VOP_TV_FILTER1
Address: Operational Base + offset (0x0218)
Filter 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	coeff7 filter coefficients 7
23:16	RW	0x00	coeff6 filter coefficients 6
15:8	RW	0x00	coeff5 filter coefficients 5
7:0	RW	0x00	coeff4 filter coefficients 4

VOP_TV_FILTER2
Address: Operational Base + offset (0x021c)
Filter 2

Bit	Attr	Reset Value	Description
31:24	RW	0x00	coeff11 filter coefficients 11
23:16	RW	0x00	coeff10 filter coefficients 10

Bit	Attr	Reset Value	Description
15:8	RW	0x00	coeff9 filter coefficients 9
7:0	RW	0x00	coeff8 filter coefficients 8

VOP_TV_ACT_ST
Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	v_offset Vertical picture start offset (independent of picture blanking)
15:12	RO	0x0	reserved
11:0	RW	0x000	h_offset Horizontal picture start offset (independent of picture blanking)

VOP_TV_ROUTING
Address: Operational Base + offset (0x0238)
Routing

Bit	Attr	Reset Value	Description
31	RW	0x0	RB_swap 1'b0: No swap 1'b1: Swap Blue/Pb and Red/Pr channels on DACs, relative to the routing shown in 30:28
30:28	RW	0x0	dac_fmt DAC3 DAC2 DAC1 DAC0 3'b000: CVBS Blue Green Red 3'b001: CVBS1 CVBS2 Y C 3'b011: Y CVBS2 CVBS1 C 3'b100: CVBS Pb Y Pr 3'b101: C Pb Y Pr
27:24	RW	0x0	sense_on When ON, outputs a steady mid level on the selected DAC(s) to allow load sensing via DAC or external comparators (application dependent). May be applied singly or together DAC3 DAC2 DAC1 DAC0 4'b0000: OFF OFF OFF OFF 4'b0001: OFF OFF OFF ON 4'b0010: OFF OFF ON OFF 4'b0100: OFF ON OFF OFF 4'b1000: ON OFF OFF OFF 4'b1111: ON ON ON ON
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x0	setup_on When ON, adds 7.5IRE setup to the specified channel Luma Red/Pr Green Blue/Pb 4'b0000: OFF OFF OFF OFF 4'bXXX1: ON 4'bXX1X: ON 4'bX1XX: ON 4'b1XXX: ON
15:12	RW	0x0	AGC_pluse_on When ON, adds AGC and EOF pulses to the specified channel. N.B. This field should not be used for disabling macrovision functionality. Y/C Red/Pr Green Blue/Pb 4'b0000: OFF OFF OFF OFF 4'bXXX1: ON 4'bXX1X: ON 4'bX1XX: ON 4'b1XXX: ON
11:8	RW	0x0	video_on When ON, adds appropriate video format to the specified channel Y/C Red/Pr Green Blue/Pb 4'b0000 : OFF OFF OFF OFF 4'bXXX1: ON 4'bXX1X: ON 4'bX1XX: ON 4'b1XXX: ON
7:4	RW	0x0	sync_on When ON, adds composite sync to the specified channel N.B. Macrovision pseudo-sync pulses (if enabled) will be added to each channel that has sync enabled. Luma Red/Pr Green Blue/Pb 4'b0000: OFF OFF OFF OFF 4'bXXX1: ON 4'bXX1X: ON 4'bX1XX: ON 4'b1XXX: ON
3	RW	0x0	YPP 1'b0: Component output is RGB 1'b1: Component output is YPbPr
2	RW	0x0	chroma_off 1'b0: Chroma is switched ON (normal colour display) 1'b1: Chroma is switched OFF (monochrome display)

Bit	Attr	Reset Value	Description
1	RW	0x0	Picture_Sync_amplitudes1 1'b0 : Composite has picture/sync ratio of 714/286 (NTSC) 1'b1 : Composite has picture/sync ratio of 700/300 (PAL)
0	RO	0x0	reserved

VOP_TV_SYNC_ADJUST
Address: Operational Base + offset (0x0250)
Sync Adjust

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	line_adj Signed number of lines by which to change frame length. Affects every frame whilst a non-zero value.
7:0	RW	0x00	pix_adj Signed number of (27MHz) pixels by which to adjust frame length. Affects every frame whilst a non-zero value.

VOP_TV_STATUS
Address: Operational Base + offset (0x0254)
TV Status register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RO	0x0	pixel_manager_vstt Pixel Manager Vertical Start State 1'b0: Vertical Start not active 1'b1: Vertical Start active
6:4	RO	0x0	pixel_manager_sta Pixel Manager Flow Controller State 3'b000: Idle 3'b001: Seeking 3'b010: Ready 3'b011: First pixel 3'b100: Active 3'b111: Other
3:2	RO	0x0	reserved
1	RO	0x0	sync_gen_VBI Sync Generator Vertical Blanking Interval 1'b0: In VBI 1'b1: Not in VBI
0	RO	0x0	sync_gen_FID Sync Generator Field Identity 1'b0: First Field 1'b1: Second Filed

VOP_TV_RST
Address: Operational Base + offset (0x0268)
tv reset Control

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	disp_rst Software reset for all other TVE functions: 1'b0: Normal operation. 1'b1: Software reset (please do NOT reset the TVE every field or frame).
0	RO	0x0	reserved

VOP_TV_SATURATION
Address: Operational Base + offset (0x0278)
Colour Burst and Saturation

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	burst_size Colour burst amplitude
15:8	RW	0x00	V_weight Conversion factor for Cr to V
7:0	RW	0x00	U_weight Conversion factor for Cb to U

VOP_TV_BANDWIDTH_CTRL
Address: Operational Base + offset (0x028c)
Chroma bandwidth

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	chroma_bandwidth 2'b00: Chroma bandpass filter is bypassed 2'b01: Chroma bandpass filter is centred on 3.58 MHz 2'b10: Chroma bandpass filter is centred on 4.43 MHz
3:0	RW	0x0	cdiff_bandwidth 4'b0000: Colour difference filters OFF (no colour) 4'b0001: Colour difference bandwidth is 0.6 MHz 4'b0010: Colour difference bandwidth is 1.3 MHz 4'b0011: Colour difference bandwidth is 2.0 MHz

VOP_TV_BRIGHTNESS_CONTRAST
Address: Operational Base + offset (0x0290)
Brightness and Contrast

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x00	Contrast This value determines the gain of the luma channel. It does not affect the chroma gain.
7:0	RW	0x00	Brightness This value determines the black level on the luma channel during active video only. The setup (if applicable) is applied in addition to this value.

VOP_MMU_DTE_ADDR
Address: Operational Base + offset (0x0300)
MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR

VOP_MMU_STATUS
Address: Operational Base + offset (0x0304)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x0	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x0	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

VOP_MMU_COMMAND
Address: Operational Base + offset (0x0308)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

VOP_MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x030c)
MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

VOP_MMU_ZAP_ONE_LINE
Address: Operational Base + offset (0x0310)
MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

VOP_MMU_INT_RAWSTAT
Address: Operational Base + offset (0x0314)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_MMU_INT_CLEAR
Address: Operational Base + offset (0x0318)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

VOP_MMU_INT_MASK
Address: Operational Base + offset (0x031c)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_MMU_INT_STATUS
Address: Operational Base + offset (0x0320)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

VOP_MMU_AUTO_GATING
Address: Operational Base + offset (0x0324)
mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating mmu auto gating when it is 1'b1, the mmu will auto gating it self

VOP_WIN1_LUT_ADDR_RESERVED
Address: Operational Base + offset (0x0400)
Access entry for win2 LUT memory(size is word only)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:0	RW	0x0000000	win1_lut_addr Access entry for win2 LUT memory(size is word only)

VOP_HWC_LUT_ADDR
Address: Operational Base + offset (0x0800)
Access entry for hwc LUT memory(size is word only)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:0	RW	0x0000000	win1_lut_addr Access entry for win2 LUT memory(size is word only)

VOP_DSP_LUT_ADDR
Address: Operational Base + offset (0x0c00)
Access entry for DSP LUT memory(size is word only)

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

2.5 Timing Diagram

2.5.1 RGB LCD interface timing

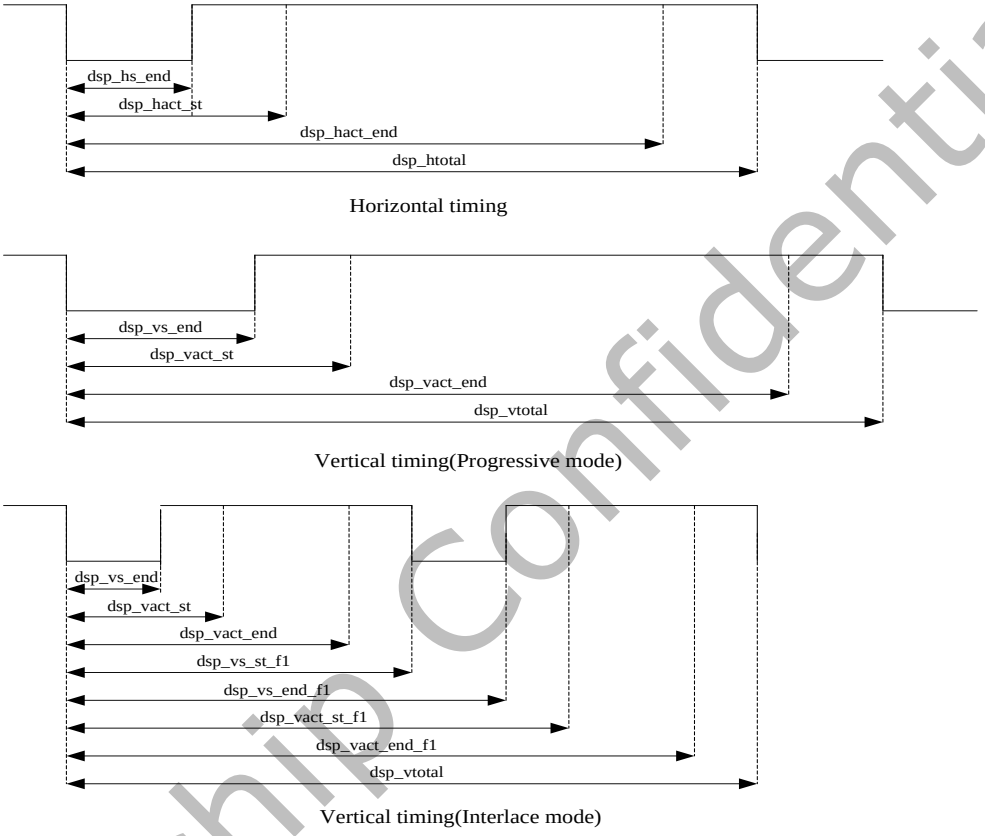


Fig. 2-17 VOP RGB interface timing (SDR)

2.5.2 ITU656 interface timing

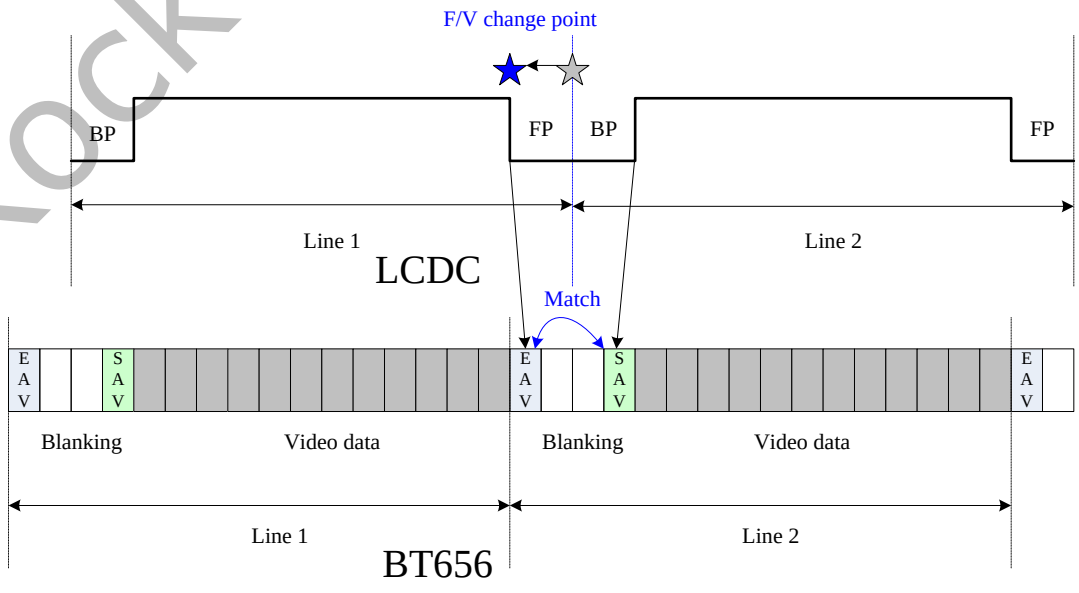


Fig. 2-18 ITU 656 timing

2.6 Interface Description

2.6.1 Display interface description

The VOP is suitable for different display mode by different usage, which is shown as follows.

Table 2-3 RGB IO

Display mode	RGB Parallel 24-bit	RGB Parallel 18-bit	RGB Parallel 16-bit
DCLK	DCLK	DCLK	DCLK
VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC
DEN	DEN	DEN	DEN
DATA	DATA[23:0]	DATA[17:0]	DATA[15:0]

Table 2-4 TV Interface IO

Display mode	ITU656 Mode0	ITU656 Mode1	ITU656 Mode2
DCLK	DCLK	DCLK	DCLK
VSYNC	-	-	-
HSYNC	-	-	-
DEN	-	-	-
DATA	DATA[7:0]	DATA[15:8]	DATA[14:7]

2.7 Application Notes

2.7.1 DMA transfer mode

There are three DMA transfer modes for loading win0 or win1 frame data determined by following parameters(X=0,1,2,3):
dma_burst_length
winX_no_outstanding
winX_gather_en
winX_gather_thres

1. auto outstanding transfer mode(random transfer)

When winX_no_outstanding is 0, multi-bursts transfer command could be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The continuous random burst number is in the range of 1 to 4, mainly depending on the empty level of internal memory, dma_burst_length, data format and active image width.

2. configured outstanding transfer mode(fixed transfer)

When winX_gather_en is 1, fixed-number of bursts transfer command should be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The fixed-number is determined by winX_gather_thres. Since the internal memory size is limited, there is some restriction for the winX_gather_thres as follows.

Table 2-5 Gather configuration for all format

Gather Threshold	dma_burst_length =2'b00(burst16)	dma_burst_length =2'b01(burst8)	dma_burst_length =2'b10(burst4)
YUV420 YUV422 YUV444	0	0,1,2	0,1,2,3
ARGB888 RGB888 RGB565	0,1,2,3	0,1,2,3	0,1,2,3
8BPP	0,1,2,3	0,1,2,3	0,1,2,3

2.7.2 HWC dma load mode

Hardware cursor data is refreshed when hwc_load_en is high, but not needed for every frame. And hwc_load_en will be high until hwc
loading finished.
The HWC data size is 32x32 or 64x64, determined by hwc_size. The data in external memory should be 32-bit aligned or 64-bit aligned, and stored in VOP internal memory in 64-bit aligned as follows.

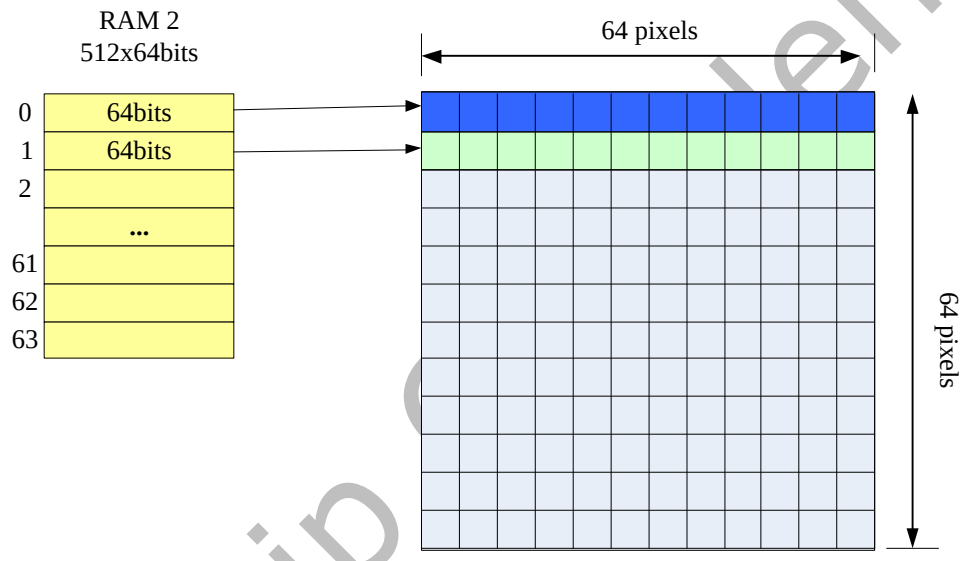


Fig. 2-19 hwc data format

2.7.3 QOS/HURRY

If you want to get higher priority for VOP to access external memory when
the frame data is urgent, a QoS and hurry request can be generated and sent out basing on the configured values:
sw_noc_qos_en: AXI_BUS_CTRL[0]
sw_noc_qos_value: AXI_BUS_CTRL[2:1]
sw_noc_hurry_en: AXI_BUS_CTRL[3]
sw_noc_hurry_value: AXI_BUS_CTRL[5:4]
sw_noc_hurry_threshold: AXI_BUS_CTRL[9:6]
sw_axi_max_outstand_en: AXI_BUS_CTRL[11]
sw_axi_max_outstand_num: AXI_BUS_CTRL[16:12]
QoS request for higher bus priority for hwc
NOC hurry for higher bus prioirity for win0/win1

2.7.4 Interrupt

Every interrupt has independent interrupt enable (VOP_INT_EN,with bit write mask), interrupt clear (VOP_INT_CLR,with bit write mask), interrupt status (VOP_INT_STATUS).
VOP interrupt is comprised of 8 interrupt sources:

- frame start interrupt
- line flag interrupt
- bus error interrupt

win0 empty interrupt
win1 empty interrupt
irq_mmu
irq_tve
dsp hold intrrupt

Every interrupt has independent interrupt enable signal(VOP_INT_EN), interrupt clear signal(VOP_INT_CLR), interrupt status signal (VOP_INT_STATUS).
MMU's and TVE's interrupt enable and clear signal are set in their own group, and are combined with others in top module. The last interrupt to outside is just a combination signal and high active.
There also has 2 raw interruption for debug:
Line flag raw Interrupt status (INT_STATUS[31])
Frame start raw interrupt status(INT_STATUS[30])

2.7.5 RGB display mode

RGB display mode is used for RGB panel display and CCIR656 output. It is a continuous frames display mode.

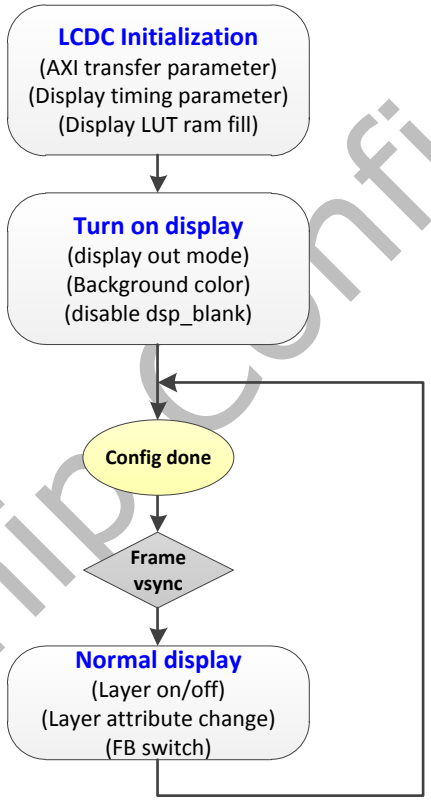


Fig. 2-20 VOP RGB mode Programming flow

1. VOP initialization
VOP initialization should be done before turning display on.
First, AXI bus parameter (VOP_SYS_CTRL) should be set for DMA transfer.
Second, display panel/interface timing should be set for display output. The registers are: VOP_DSP_HTOTAL_HS_END/ VOP_DSP_HACT_ST_END/ VOP_DSP_VTOTAL_HS_END/ VOP_DSP_VACT_ST_END/ VOP_DSP_VS_ST_END_F1/ VOP_DSP_VACT_ST_END_F1
2. Background display
Before normal display, the background display could be turn on.
First, set display output mode according to display device.
Second, disable dsp_blank mode, which would not be enable until frame synchronization.
Finally, writing '1' to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.
3. Normal display

In normal display, all the display layers' attribute could be different according display scenario. So there is a programming loop in this mode.
First, configure all the display layers' attribute registers for the change of image format, location, size, scaling factor, alpha and overlay and so on. Those register would not be enable until frame synchronization.
Finally, write '1' to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.
Immediately control register
There are two type register in VOP , one type is effective immediately, the other is effective by frame sync.
Effective immediately registers list as follows, other registers are all effective by frame sync.

Table 2-6 ffective immediately register table

register address	description
0x000	some ctrl function bit
0x004[31:28] [24:12] [9:0]	some dsp ctrl function bit
0x008	background color register dsp control function bits
0x014	Alpha control register
0x018	win0 color key register
0x01c	win1 color key register
0x06c~0x080	dsp_timing register

Chapter 3 VPU_Combo

3.1 Overview

VPU_Combo is composed by the H.265 (HEVC) decoder and the H.264 decoder to realize the high quality video decoding. VPU_Combo is connected to the AHB bus through an AHB slave and the AXI bus through an AXI master. The register configuration is fed into the VPU_Combo through the AHB slave interface while the stream data is transacted between DDR and VPU_Combo through the AXI master interface.
To reduce the area, H.265 decoder and H.264 decoder not only share several pieces of the internal memories, but also share the bus master and slave interfaces. Therefore VPU_Combo has no any possibility to have the H.265 video decoding and H.264 video decoding to work simultaneously
In order to improve large data transaction performance, VPU embeds MMU (memory management unit) and supports the cacheable bus operation.
VPU_Combo supports the next-generation video coding standard HEVC (High Efficiency Video Coding, aka H.265) full-HD decoding up to 60fps. With HEVC standard, the data compression ratio can be doubled compared to H.264/MEPG-4 at the same video quality or alternatively to provide substantially improved video at the same bit rate.Nand Flash Controller (NandC) is used to control data transmission from host to flash device or from flash device to host. NandC is connected to AHB BUS through an AHB Master and an AHB Slave. The data transmission between host and external memory can be done through AHB Master interface or AHB Slave interface.
VPU_Combo supports the following features:

1. Supports HEVC Main Profile up to Level 4.1: 1920x1080@60 fps
   - MMU embedded
   - Supports frame timeout interrupt , frame finish interrupt and bitstream error interrupt
   - Supports RLC write mode, RLC mode and Normal Mode
2. Supports decoding of the following standards
   - Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage, and YCbCr 4:0:0 is also supported for H.264
   - H.264 up to HP level 4.2 including Baseline Profile, Main Profile : 1920x1088@60fps
   - MPEG-4: Simple Profile up to Level 6; Advanced Profile up to Level 5 (1920x1088@60fps)
   - MPEG-2: Main Profile up to High Level (1920x1088 @60fps)
   - JPEG: Baseline interleaved, and supports ROI (region of image) decode
   - For H.264, Image cropping not supported
   - For H.264, image cropping not supported
   - For MPEG-4, GMC(global motion compensation) not supported
   - For MPEG-4 SP, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit
3. Built-in post processor in H.264 decoder supports:
   - Stand-alone mode: rotation, RGB conversion, scaling, dithering
   - Pipe-ling mode:, RGB conversion, scaling, dithering and alpha blending

3.2 Block Diagram

As shown in the figures above, CPU accesses to HEVC register bank through 32-bit AHB bus. Bitstream and compressed video data are fed into HEVC core though 128-bit AXI read channel, and after several steps of decoding process, decoded pictures are transferred to designated location in the DDR through 64-bit AXI write channel.
CPU accesses to H264 encoder/decoder register bank through 32-bit AHB bus. Video data are fed into H.264 core though 64-bit AXI read channel, and after several steps of decoding process, process results are transferred to designated location in the DDR through 64-bit AXI write channel.

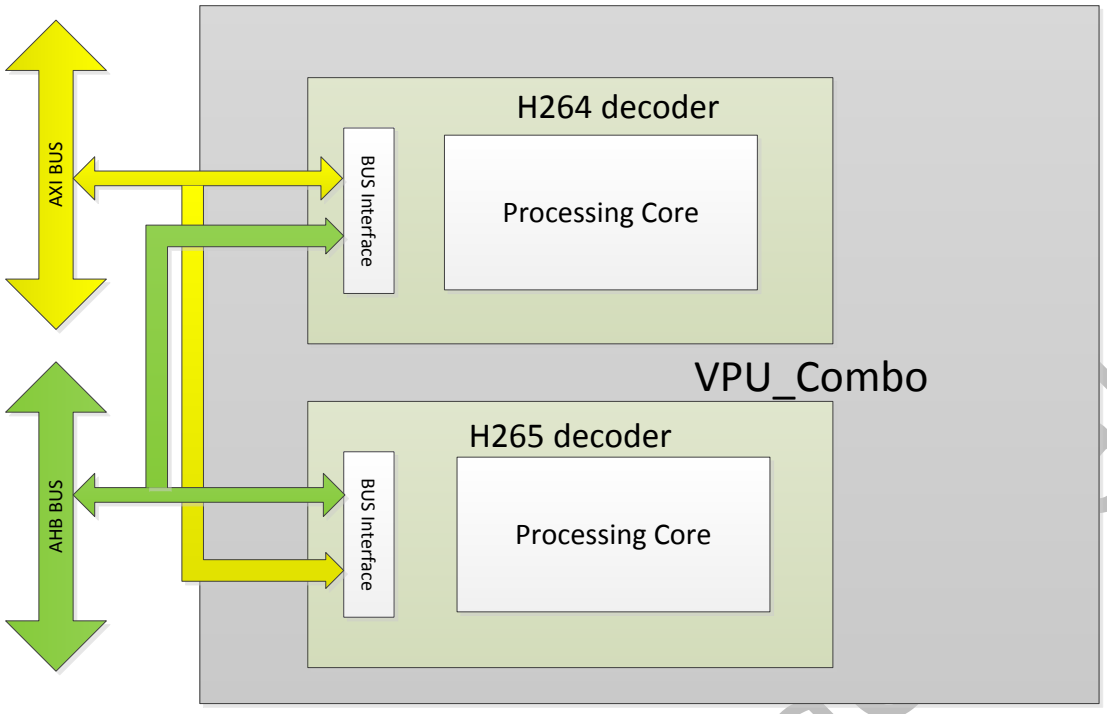


Fig. 3-1 VPU_Combo Block Diagram

3.3 Function Description

3.3.1 HEVC Standard

High Efficiency Video Coding (HEVC) is a video compression standard, a successor to H.264/MPEG-4 AVC (Advanced Video Coding), that was jointly developed by the ISO/IEC Moving Picture Experts Group (MPEG) and ITU-T Video Coding Experts Group (VCEG) as ISO/IEC 23008-2 MPEG-H Part 2 and ITU-T H.265. MPEG and VCEG established a Joint Collaborative Team on Video Coding (JCT-VC) to develop the HEVC standard.
HEVC was designed to substantially improve coding efficiency compared to H.264/MPEG-4 AVC HP, i.e. to reduce bitrate requirements by half with comparable image quality, at the expense of increased computational complexity. HEVC was designed with the goal of allowing video content to have a data compression ratio of up to 1000:1. Depending on the application requirements HEVC encoders can trade off computational complexity, compression rate, robustness to errors, and encoding delay time.Two of the key features where HEVC was improved compared to H.264/MPEG-4 AVC was support for higher resolution video and improved parallel processing methods.

3.3.2 HEVC Coding Tools

1. Coding tree unit
HEVC replaces macroblocks, which were used with previous standards, with Coding Tree Units (CTUs) which can use a larger block structures of up to 64x64 pixels and can better sub-partition the picture into variable sized structures. HEVC initially divides the picture into CTUs which can be 64x64, 32x32, or 16x16 with a larger pixel block size usually increasing the coding efficiency.
2. Parallel processing tools
Tiles allow for the picture to be divided up into a grid of rectangular regions that can independently be decoded/encoded and the main purpose of tiles is to allow for parallel processing.Tiles can be independently decoded and can even allow for random access to specific regions of a picture in a video stream.
Wavefront parallel processing (WPP) is when a slice is divided into rows of CTUs in which the first row is decoded normally but each additional row requires that decisions be made in the previous row. WPP has the entropy encoder use information from the preceding row of CTUs and allows for a method of parallel processing that may allow for better compression than tiles.
Tiles and WPP are allowed but are optional.If tiles are present they must be at least 64 pixels

high and 256 pixels wide with a level specific limit on the number of tiles allowed.
Slices can for the most part be decoded independently from each other with the main purpose of tiles being re-synchronization in case of data loss in the video stream. Slices can be defined as self-contained in that prediction is not made across slice boundaries. When in-loop filtering is done on a picture though information across slice boundaries may be required.[1] Slices are CTUs decoded in the order of the raster scan and different coding types can be used for slices such as I types, P types, or B types.
Dependent slices can allow for data related to tiles or WPP to be accessed more quickly by the system than if the entire slice had to be decoded.[1] The main purpose of dependent slices is to allow for low delay video encoding due to its lower latency.
3. Entropy coding
HEVC uses a context-adaptive binary arithmetic coding (CABAC) algorithm that is fundamentally similar to CABAC in H.264/MPEG-4 AVC. CABAC is the only entropy encoder method that is allowed in HEVC while there are two entropy encoder methods allowed by H.264/MPEG-4 AVC. CABAC and the entropy coding of transform coefficients in HEVC were designed for a higher throughput than H.264/MPEG-4 AVC. For instance, the number of context coded bins have been reduced by 8x and the CABAC bypass-mode has been improved in terms of its design to increase throughput. Another improvement with HEVC is that the dependencies between the coded data has been changed to further increase throughput. Context modeling in HEVC has also been improved so that CABAC can better select a context that increases efficiency when compared to H.264/MPEG-4 AVC.
4. Intra prediction
HEVC specifies 33 directional modes for intra prediction compared to the 8 directional modes for intra prediction specified by H.264/MPEG-4 AVC. HEVC also specifies planar and DC intra prediction modes.[1] The intra prediction modes use data from neighboring prediction blocks that have been previously decoded.
5. Motion compensation
For the interpolation of fractional luma sample positions HEVC uses separable application of one-dimensional half-sample interpolation with an 8-tap filter or quarter-sample interpolation with a 7-tap filter while, in comparison, H.264/MPEG-4 AVC uses a two-stage process that first derives values at half-sample positions using separable one-dimensional 6-tap interpolation followed by integer rounding and then applies linear interpolation between values at nearby half-sample positions to generate values at quarter-sample positions.[1] HEVC has improved precision due to the longer interpolation filter and the elimination of the intermediate rounding error. For 4:2:0 video, the chroma samples are interpolated with separable one-dimensional 4-tap filtering to generate eighth-sample precision, while in comparison H.264/MPEG-4 AVC uses only a 2-tap bilinear filter (also with eighth-sample precision).
As in H.264/MPEG-4 AVC, weighted prediction in HEVC can be used either with uni-prediction (in which a single prediction value is used) or bi-prediction (in which the prediction values from two prediction blocks are combined).
6. Motion vector prediction
HEVC defines a signed 16-bit range for both horizontal and vertical motion vectors (MVs). This was added to HEVC at the July 2012 HEVC meeting with the mvLX variables. HEVC horizontal/vertical MVs have a range of −32768 to 32767 which given the quarter pixel precision used by HEVC allows for a MV range of −8192 to 8191.75 luma samples. This compares to H.264/MPEG-4 AVC which allows for a horizontal MV range of −2048 to 2047.75 luma samples and a vertical MV range of −512 to 511.75 luma samples.
HEVC allows for two MV modes which are Advanced Motion Vector Prediction (AMVP) and merge mode. AMVP uses data from the reference picture and can also use data from adjacent prediction blocks. The merge mode allows for the MVs to be inherited from neighboring prediction blocks. Merge mode in HEVC is similar to "skipped" and "direct" motion inference modes in H.264/MPEG-4 AVC but with two improvements. The first improvement is that HEVC uses index information to select one of several available candidates. The second improvement is that HEVC uses information from the reference picture list and reference picture index.
7. Inverse transforms
HEVC specifies four transform units (TUs) sizes of 4x4, 8x8, 16x16, and 32x32 to code the prediction residual. A CTB may be recursively partitioned into 4 or more TUs.[1] TUs use

integer basis functions that are similar to the discrete cosine transform (DCT). In addition 4x4 luma transform blocks that belong to an intra coded region are transformed using an integer transform that is derived from discrete sine transform (DST). This provides a 1% bit rate reduction but was restricted to 4x4 luma transform blocks due to marginal benefits for the other transform cases. Chroma uses the same TU sizes as luma so there is no 2x2 transform for chroma.

8. Loop filters

HEVC specifies two loop filters that are applied sequentially, with the deblocking filter (DBF) applied first and the sample adaptive offset (SAO) filter applied afterwards. Both loop filters are applied in the inter-picture prediction loop, i.e. the filtered image is stored in the decoded picture buffer (DPB) as a reference for inter-picture prediction.

8.1 Deblocking filter

The DBF is similar to the one used by H.264/MPEG-4 AVC but with a simpler design and better support for parallel processing.[1] In HEVC the DBF only applies to a 8x8 sample grid while with H.264/MPEG-4 AVC the DBF applies to a 4x4 sample grid. DBF uses a 8x8 sample grid since it causes no noticeable degradation and significantly improves parallel processing because the DBF no longer causes cascading interactions with other operations. Another change is that HEVC only allows for three DBF strengths of 0 to 2. HEVC also requires that the DBF first apply horizontal filtering for vertical edges to the picture and only after that does it apply vertical filtering for horizontal edges to the picture. This allows for multiple parallel threads to be used for the DBF.

8.2 Sample adaptive offset

The SAO filter is applied after the DBF and is designed to allow for better reconstruction of the original signal amplitudes by applying offsets stored in a lookup table in the bitstream. Per CTB the SAO filter can be disabled or applied in one of two modes: edge offset mode or band offset mode. The edge offset mode operates by comparing the value of a sample to two of its eight neighbors using one of four directional gradient patterns. Based on a comparison with these two neighbors, the sample is classified into one of five categories: minimum, maximum, an edge with the sample having the lower value, an edge with the sample having the higher value, or monotonic. For each of the first four categories an offset is applied. The band offset mode applies an offset based on the amplitude of a single sample. A sample is categorized by its amplitude into one of 32 bands (histogram bins). Offsets are specified for four consecutive of the 32 bands, because in flat areas which are prone to banding artifacts, sample amplitudes tend to be clustered in a small range.[1][135] The SAO filter was designed to increase picture quality, reduce banding artifacts, and reduce ringing artifacts.

3.3.3 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

4. Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
5. The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:

1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.

2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

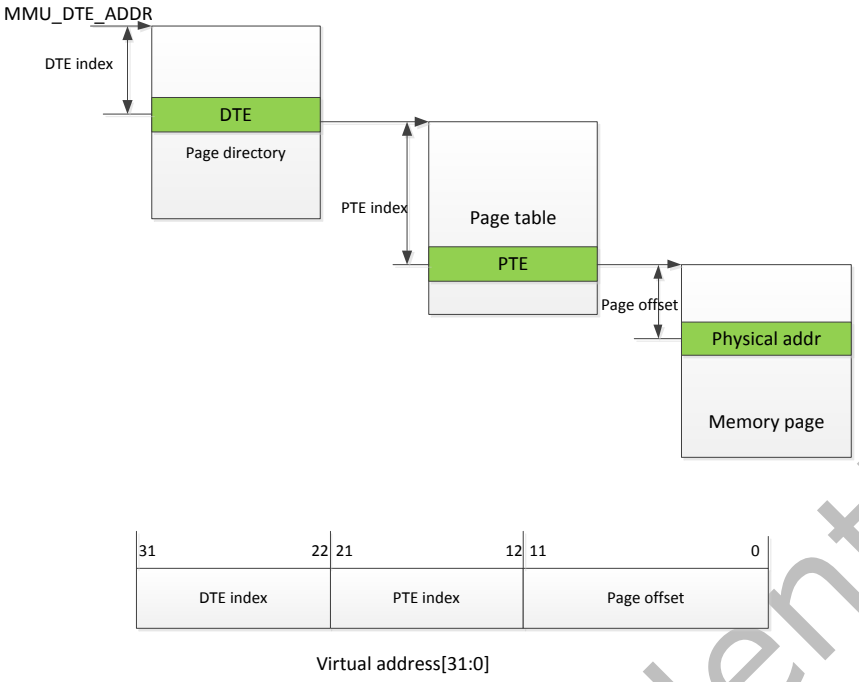


Fig. 3-2 structure of two-level page table

3.3.4 HEVC Working Mode

There are there working modes to be selected for HEVC decoder: RLC Mode, RLC Write Mode, Normal Mode.
The key differences among three working modes are whether CABAC module and Post-CABAC module are involved into the hardware decoding process.
For RLC mode, CABAC are bypassed and the input bitstream to the Post-CABAC module should be already decoded.
For RLC write mode, the decoded results by CABAC are output to the DDR, and the following decoding processes are stopped.
As for the normalmode , all the modules are involved into the decoding process, and complete decoding results are output. Normally, this mode should be selected.

3.3.5 H264 Decoder

The input format in use will be automatically detected. The H.264 video encoding allows the use of multiple reference pictures, which means that the decoding order of the pictures may be different from their display order. The decoder can perform internally the display reordering of the decoded pictures or it can skip this and output all the pictures as soon as they are decoded.
The decoder has two operating modes: in the primary mode the HW performs entropy decoding, and in the secondary mode SW performs entropy decoding. Secondary mode is used in H.264 ASO or Slice Group stream decoding.

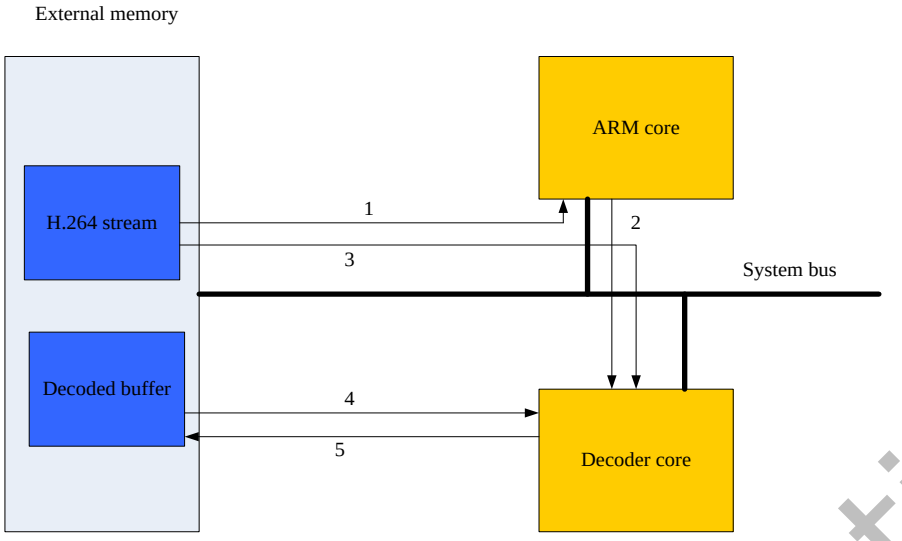


Fig. 3-3 Dataflow of HW performs entropy decoding in video decoder

The dataflow of HW performs entropy decoding is as shown above. The decoder software (SW) starts decoding the first picture by parsing the stream headers (1). Software then setups the hardware control registers (picture size, stream start address etc.) and enables the hardware (2).Hardware decodes the picture by reading stream (3) and the reference pictures (required for inter picture decoding)(4) from the external memory. Hardware writes the decoded output picture to memory one macroblock at a time (5). When the picture has been fully decodedor the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream and address for software to continue and returns to initial state.

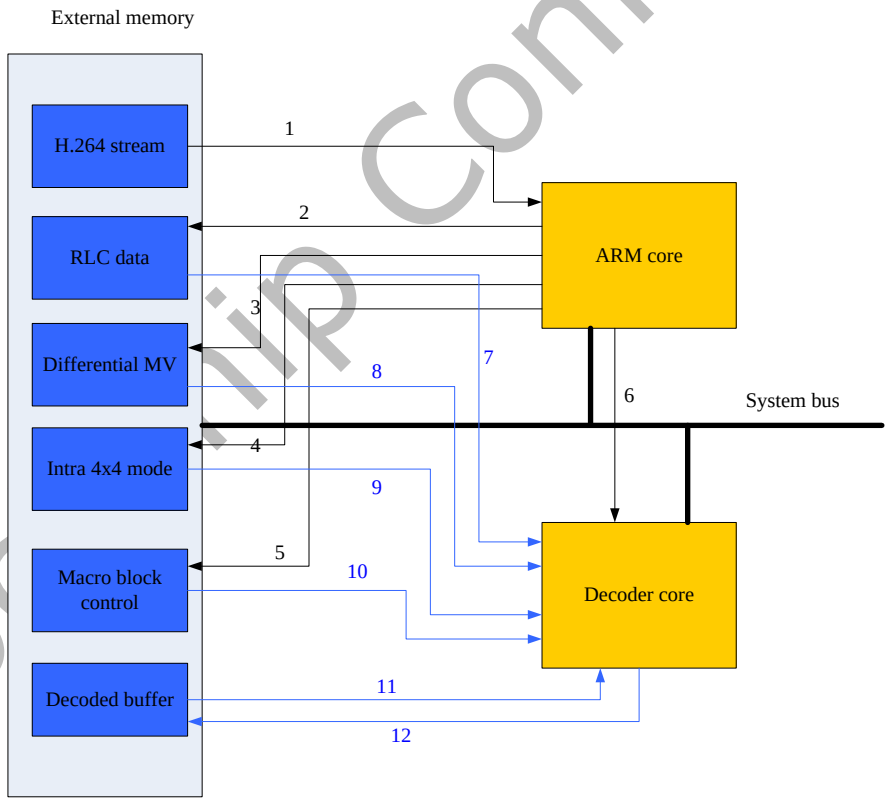


Fig. 3-4 Dataflow of SW performs entropy decoidng in video decoder

3.4 Register Description

3.4.1 Internal Address Mapping

This section describes the control/status registers of the VPU_Combo.
HEVC and H.264 decoder have individual base register address for each other.
If HEVC is chosen to work, HEVC register base address is the base address of the hevc_base.

The HEVC reading MMU master register base address is hevc_base+0x440, the writing MMU register base address is hevc_base + 0x480, and the cache control register base address is hevc_base + 0x400.
If H.264 encoder is chosen to work, and VDPU(decoder) base address is vdpu_base. MMU base address is vdpu +0x400, and VDPU cache control base address is vpu_base + 0x800.

3.4.2 HEVC Registers Summary

Name	Offset	Size	Reset Value	Description
hevc_swreg0_id	0x0000	W	0x68761100	ID register (read only)
hevc_swreg1_int	0x0004	W	0x00200022	interrupt and decoder enable register
hevc_swreg2_sysctrl	0x0008	W	0x00000000	Data input and output endian setting and sys ctrl
hevc_swreg3_picpar	0x000c	W	0x00000000	picture parameters
hevc_swreg4_strm_rlc_base	0x0010	W	0x00000000	the stream or rlc data base address
hevc_swreg5_stream_rlc_len	0x0014	W	0x00000000	amount of stream bytes or rlc data byte in the input buffer or the
hevc_swreg6_cabactbl_base	0x0018	W	0x00000000	the base address of cabac table
hevc_swreg7_decout_base	0x001c	W	0x00000000	base address of decoder output picture base address
hevc_swreg8_y_virstride	0x0020	W	0x00000000	the ouput picture y virtual stride
hevc_swreg9_yuv_virstride	0x0024	W	0x00000000	the ouput picture yuv virtual stride
hevc_swreg10_refer0_base	0x0028	W	0x00000000	base address for reference picture index 0
hevc_swreg11_refer1_base	0x002c	W	0x00000000	base address for reference picture index 1
hevc_swreg12_refer2_base	0x0030	W	0x00000000	base address for reference picture index 2
hevc_swreg13_refer3_base	0x0034	W	0x00000000	base address for reference picture index 3
hevc_swreg14_refer4_base	0x0038	W	0x00000000	base address for reference picture index 4
hevc_swreg15_refer5_base	0x003c	W	0x00000000	base address for reference picture index 5
hevc_swreg16_refer6_base	0x0040	W	0x00000000	base address for reference picture index 6
hevc_swreg17_refer7_base	0x0044	W	0x00000000	base address for reference picture index 7
hevc_swreg18_refer8_base	0x0048	W	0x00000000	base address for reference picture index 8
hevc_swreg19_refer9_base	0x004c	W	0x00000000	base address for reference picture index 9
hevc_swreg20_refer10_base	0x0050	W	0x00000000	base address for reference picture index 10

Name	Offset	Size	Reset Value	Description
hevc_swreg21_refer11_base	0x0054	W	0x00000000	base address for reference picture index 11
hevc_swreg22_refer12_base	0x0058	W	0x00000000	base address for reference picture index 12
hevc_swreg23_refer13_base	0x005c	W	0x00000000	base address for reference picture index 13
hevc_swreg24_refer14_base	0x0060	W	0x00000000	base address for reference picture index 14
hevc_swreg25_refer0_poc	0x0064	W	0x00000000	the poc of reference picture index 0
hevc_swreg26_refer1_poc	0x0068	W	0x00000000	the poc of reference picture index 1
hevc_swreg27_refer2_poc	0x006c	W	0x00000000	the poc of reference picture index 2
hevc_swreg28_refer3_poc	0x0070	W	0x00000000	the poc of reference picture index 3
hevc_swreg29_refer4_poc	0x0074	W	0x00000000	the poc of reference picture index 4
hevc_swreg30_refer5_poc	0x0078	W	0x00000000	the poc of reference picture index 5
hevc_swreg31_refer6_poc	0x007c	W	0x00000000	the poc of reference picture index 6
hevc_swreg32_refer7_poc	0x0080	W	0x00000000	the poc of reference picture index 7
hevc_swreg33_refer8_poc	0x0084	W	0x00000000	the poc of reference picture index 8
hevc_swreg34_refer9_poc	0x0088	W	0x00000000	the poc of reference picture index 9
hevc_swreg35_refer10_poc	0x008c	W	0x00000000	the poc of reference picture index 10
hevc_swreg36_refer11_poc	0x0090	W	0x00000000	the poc of reference picture index 11
hevc_swreg37_refer12_poc	0x0094	W	0x00000000	the poc of reference picture index 12
hevc_swreg38_refer13_poc	0x0098	W	0x00000000	the poc of reference picture index 13
hevc_swreg39_refer14_poc	0x009c	W	0x00000000	the poc of reference picture index 14
hevc_swreg40_cur_poc	0x00a0	W	0x00000000	the poc of cur picture
hevc_swreg41_rlcwrite_base	0x00a4	W	0x00000000	the base address or rlcwrite base addr
hevc_swreg42_pps_base	0x00a8	W	0x00000000	the base address of pps
hevc_swreg43_rps_base	0x00ac	W	0x00000000	the base address of rps
hevc_swreg44_cabac_error_en	0x00b0	W	0x00000000	cabac error enable config
hevc_swreg45_cabac_error_status	0x00b4	W	0x00000000	cabac error status
hevc_swreg46_cabac_error_ctu	0x00b8	W	0x00400000	cabac error ctu
hevc_swreg47_sao_ctu_position	0x00bc	W	0x00000000	sao ctu position
hevc_swreg64_performance_cycle	0x0100	W	0x00000000	hevc performance cycle

Name	Offset	Size	Reset Value	Description
hevc_swreg65_axi_ddr_rdata	0x0104	W	0x00000000	axi ddr read data num
hevc_swreg66_axi_ddr_wdata	0x0108	W	0x00000000	axi ddr write data number

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.4.3 HEVC Detail Register Description

hevc_swreg0_id
Address: Operational Base + offset (0x0000)
ID register (read only)

Bit	Attr	Reset Value	Description
31:16	RO	0x6876	prod_num product number The ascii code of "hv", which is 0x6876
15	RO	0x0	reserved
14	RW	0x0	codec_flag codec flag 0: only dec 1: dec + enc
13	RO	0x0	reserved
12	RW	0x1	profile hevc profile 0: Main 1: Main10
11:9	RO	0x0	reserved
8	RO	0x1	level level 0: FHD 1: UHD
7:0	RO	0x00	minor_ver minor version minor version

hevc_swreg1_int
Address: Operational Base + offset (0x0004)
interrupt and decoder enable register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_softreset_rdy when it is 1'b1, it says that softreset has been done
21	RW	0x1	sw_force_softreset_valid when sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle; when sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle.

Bit	Attr	Reset Value	Description
20	RW	0x0	sw_softrst_en_p softreset enable softreset enable signal write 1 to soft reset, write 0 invalid puls register
19	RO	0x0	reserved
18	RW	0x0	sw_cabu_end_sta cabac decode end status cabac decode end status
17	RW	0x0	sw_colmv_ref_error_sta colmv ref error status colmv ref error status when it is 1'b1, it means that inter module read the invalid dpb frame
16	RO	0x0	reserved
15	RW	0x0	sw_dec_timeout_sta decoder timeout interrupt status When high the decoder has been idling for too long. it will self reset the hardware only when sw_dec_timeout_e is 1'b1, this bit is valid
14	RW	0x0	sw_dec_error_sta status bit of input stream error when high, an error is found in input data stream decoding. It will self reset the hardware
13	RW	0x0	sw_dec_bus_sta bus error status When this bit is high, there is error on the axi bus, it will self reset hardware
12	RW	0x0	sw_dec_rdy_sta decoder ready status when this bit is high, decoder has decoded a picture
11:10	RO	0x0	reserved
9	RW	0x0	sw_dec_irq_raw the raw status of sw_dec_irq the raw status of sw_dec_irq,SW should reset this bit after interrupt is handled
8	RO	0x0	sw_dec_irq decoder IRQ when high, decoder requests an interrrupt. sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)

Bit	Attr	Reset Value	Description
7	RW	0x0	sw_stmerror_waitdecfifo_empty whether the stream error process wait the decfifo empty when it is 1'b0, the stream error process will no wait the ca2decfifo empty when it is 1'b1, the stream error process will wait the ca2decfifo empty
6	RO	0x0	reserved
5	RW	0x1	sw_dec_timeout_e Timeout interrupt enable If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
4	RW	0x0	sw_dec_irq_dis decoder IRQ disable When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status
3:2	RO	0x0	reserved
1	RW	0x1	sw_dec_clkgate_e decoder dynamic clock gating enable 0 = clock is running for all structures 1 = clock is gated for decoder structures that are not used
0	RW	0x0	sw_dec_e decoder enable Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when picture is processed or stream error is detected or bus error or time out interrupt is given

hevc_swreg2_sysctrl

Address: Operational Base + offset (0x0008)

Data input and output endian setting and sys ctrl

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:12	RW	0x00	sw_strm_start_bit exact bit of stream start exact bit of streamd start word where decoding can be started (asosiates with sw_str_rlc_base)
11	RW	0x0	sw_rlc_mode rlc mode enable 0 = HW decodes video from bit stream 1 = HW decodes video from RLC input data
10	RW	0x0	sw_rlc_mode_direct_write cabac decode output direct write cabac decode output direct write enable when this bit is enable , all the module other than cabac and busifd are not work
9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	sw_out_cbcr_swap output cbcr swap 1'b0: cb(u) is in the lower address, cr(v) is in the higher address 1'b1: cb(u) is in the higher address,cr(v) is in the lower address sw_in_cbcr_swap is the same with sw_out_cbcr_swap
7	RW	0x0	sw_out_swap32_e decoder output data and dpb input data 32bit swap may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
6	RW	0x0	sw_out_endian dec output data and colmv , dpb data and colmv input endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
5	RW	0x0	sw_str_swap64_e stream 64bit data swap may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
4	RW	0x0	sw_str_swap32_e stream 32bit data swap may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
3	RW	0x0	sw_str_endian stream data input endian mode 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
2	RW	0x0	sw_in_swap64_e input 64bit data swap for other than stream and dpb data may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
1	RW	0x0	sw_in_swap32_e input 32bit data swap for other than stream and dpb data may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_in_endian decoder input endian mode for other than stream and dpb data 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address

hevc_swreg3_picpar
Address: Operational Base + offset (0x000c)
picture parameters

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	sw_slice_num slice number in a frame slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame) just only used for rps read. 2013.11.27 change the meaning from count from 1, so it will be in 1~200 2013.11.30 sw_slice_num max value is change to 600, so sw_slice_num expand to 10bit
20:12	RW	0x000	sw_uv_hor_virstride Field0000 Abstract picture horizontal virtual stride (the unit is 128bit) the max is (4096x1.5 + 128) /16 = 0x188 suggest this register to config to even for advance ddr performance
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_y_hor_virstride picture horizontal virtual stride picture horizontal virtual stride (the unit is 128bit) the max is (4096x1.5 + 128) /16 = 0x188 suggest this register to config to even for advance ddr performance

hevc_swreg4_strm_rlc_base
Address: Operational Base + offset (0x0010)
the stream or rlc data base address

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_rlc_base the stream or rlc data base address when swreg2.sw_rlc_mode =1, it is base address for rlc data when swreg2.sw_rlc_mode =0, it is base address for stream , after a frame is decoded ready or error (stream error , time out , bus error) , it is the last address of the stream the address should 128bit align
3:0	RO	0x0	reserved

hevc_swreg5_stream_rlc_len
Address: Operational Base + offset (0x0014)
amount of stream bytes or rlc data byte in the input buffer or the

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	sw_stream_len amount of stream (unit is 8bit) in the input buffer amount of stream 8bits in the input buffer the max of sw_stream_len : 4096x2304x1.5x1.5 = 0x1440000 128bits unit: 0x1440000/16 = 0x144000 it is count from 0 2013.10.15 change to 23bit for zty's suggestion 2013.10.28, amount of stream data bytes in input buffer. it is count from 1, change to 27bits

hevc_swreg6_cabactbl_base
Address: Operational Base + offset (0x0018)
the base address of cabac table

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_cabactbl_base the base address of cabac table the base address of cabac table the address should 128bit align
3:0	RO	0x0	reserved

hevc_swreg7_decout_base
Address: Operational Base + offset (0x001c)
base address of decoder output picture base address

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_decout_base base address of decoder output picture addr base address of decoder output picture the address should be 128bit align
3:0	RO	0x0	reserved

hevc_swreg8_y_virstride
Address: Operational Base + offset (0x0020)
the ouput picture y virtual stride

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	sw_y_virstride the output picture y virtual stride the output picture y virtual stride (the unit is 128bit) the max: (4096x1.5 +128) x 2304 = 0xdc8000 we can know the sw_uvout_base = sw_decout_base + (sw_y_virstride <<4)

hevc_swreg9_yuv_virstride
Address: Operational Base + offset (0x0024)
the ouput picture yuv virtual stride

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:0	RW	0x000000	sw_yuv_virstride the ouput picture yuv virtual stride the output picture yuv virtual stride (the unit is 128bit) the max : (4096x1.5 +128) x 2304 x1.5 = 0x14ac000 we can know the sw_mvout_base = sw_decout_base + (sw_yuv_virstride <<4)

hevc_swreg10_refer0_base
Address: Operational Base + offset (0x0028)
base address for reference picture index 0

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer0_base base address for reference picture index0 base address for reference picture index 0 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_0_3 valid flag for picture index 0 ~3 valid flag for picture index 0 ~3

hevc_swreg11_refer1_base
Address: Operational Base + offset (0x002c)
base address for reference picture index 1

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer1_base base address for reference picture index 1 base address for reference picture index 1 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_4_7 valid flag for picture index 4 ~7 valid flag for picture index 4 ~7

hevc_swreg12_refer2_base
Address: Operational Base + offset (0x0030)

base address for reference picture index 2

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer2_base base address for reference picture index 2 base address for reference picture index 2 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_8_11 valid flag for picture index 8~11 valid flag for picture index 8~11

hevc_swreg13_refer3_base
Address: Operational Base + offset (0x0034)
base address for reference picture index 3

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer3_base base address for reference picture index 3 base address for reference picture index 3 (the address should be 128bit align)
3	RO	0x0	reserved
2:0	RW	0x0	sw_ref_valid_12_14 valid flag for picture index 12~14 valid flag for picture index 12~14

hevc_swreg14_refer4_base
Address: Operational Base + offset (0x0038)
base address for reference picture index 4

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer4_base base address for reference picture index 4 base address for reference picture index 4(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg15_refer5_base
Address: Operational Base + offset (0x003c)
base address for reference picture index 5

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer5_base base address for reference picture index 5 base address for reference picture index 5(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg16_refer6_base
Address: Operational Base + offset (0x0040)
base address for reference picture index 6

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer6_base base address for reference picture index 6 base address for reference picture index 6(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg17_refer7_base
Address: Operational Base + offset (0x0044)
base address for reference picture index 7

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer7_base base address for reference picture index 7 base address for reference picture index 7(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg18_refer8_base
Address: Operational Base + offset (0x0048)
base address for reference picture index 8

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer8_base base address for reference picture index 8 base address for reference picture index 8(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg19_refer9_base
Address: Operational Base + offset (0x004c)
base address for reference picture index 9

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer9_base base address for reference picture index 9 base address for reference picture index 9(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg20_refer10_base
Address: Operational Base + offset (0x0050)
base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer10_base base address for reference picture index 10 base address for reference picture index 10(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg21_refer11_base
Address: Operational Base + offset (0x0054)
base address for reference picture index 11

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer11_base base address for reference picture index 11 base address for reference picture index 11(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg22_refer12_base
Address: Operational Base + offset (0x0058)
base address for reference picture index 12

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer12_base base address for reference picture index 12 base address for reference picture index 12(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg23_refer13_base
Address: Operational Base + offset (0x005c)
base address for reference picture index 13

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer13_base base address for reference picture index 13 base address for reference picture index 13(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg24_refer14_base
Address: Operational Base + offset (0x0060)
base address for reference picture index 14

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer14_base base address for reference picture index 14 base address for reference picture index 14(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg25_refer0_poc
Address: Operational Base + offset (0x0064)
the poc of reference picture index 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer0_poc the poc of reference picture index 0 the poc of reference picture index 0

hevc_swreg26_refer1_poc
Address: Operational Base + offset (0x0068)
the poc of reference picture index 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer1_poc the poc of reference picture index 1 the poc of reference picture index 1

hevc_swreg27_refer2_poc
Address: Operational Base + offset (0x006c)
the poc of reference picture index 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer2_poc the poc of reference picture index 2 the poc of reference picture index 2

hevc_swreg28_refer3_poc
Address: Operational Base + offset (0x0070)
the poc of reference picture index 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer3_poc the poc of reference picture index 3 the poc of reference picture index 3

hevc_swreg29_refer4_poc
Address: Operational Base + offset (0x0074)
the poc of reference picture index 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer4_poc the poc of reference picture index 4 the poc of reference picture index 4

hevc_swreg30_refer5_poc
Address: Operational Base + offset (0x0078)
the poc of reference picture index 5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer5_poc the poc of reference picture index 5 the poc of reference picture index 5

hevc_swreg31_refer6_poc
Address: Operational Base + offset (0x007c)
the poc of reference picture index 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer6_poc the poc of reference picture index 6 the poc of reference picture index 6

hevc_swreg32_refer7_poc
Address: Operational Base + offset (0x0080)
the poc of reference picture index 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer7_poc the poc of reference picture index 7 the poc of reference picture index 7

hevc_swreg33_refer8_poc
Address: Operational Base + offset (0x0084)
the poc of reference picture index 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer8_poc the poc of reference picture index 8 the poc of reference picture index 8

hevc_swreg34_refer9_poc
Address: Operational Base + offset (0x0088)
the poc of reference picture index 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer9_poc the poc of reference picture index 9 the poc of reference picture index 9

hevc_swreg35_refer10_poc
Address: Operational Base + offset (0x008c)
the poc of reference picture index 10

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer10_poc the poc of reference picture index 10 the poc of reference picture index 10

hevc_swreg36_refer11_poc
Address: Operational Base + offset (0x0090)
the poc of reference picture index 11

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer11_poc the poc of reference picture index 11 the poc of reference picture index 11

hevc_swreg37_refer12_poc
Address: Operational Base + offset (0x0094)
the poc of reference picture index 12

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer12_poc the poc of reference picture index 12 the poc of reference picture index 12

hevc_swreg38_refer13_poc
Address: Operational Base + offset (0x0098)
the poc of reference picture index 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer13_poc the poc of reference picture index 13 the poc of reference picture index 13

hevc_swreg39_refer14_poc
Address: Operational Base + offset (0x009c)
the poc of reference picture index 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer14_poc the poc of reference picture index 14 the poc of reference picture index 14

hevc_swreg40_cur_poc
Address: Operational Base + offset (0x00a0)
the poc of cur picture

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cur_poc the poc of the cur picture the poc of the cur picture

hevc_swreg41_rlcwrite_base
Address: Operational Base + offset (0x00a4)
the base address or rlcwrite base addr

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_rlcwrite_base the base address of rlcwrite the base address of rlcwrite(the address should 64bit align) cabac output write to this rlcwrite base address when sw_rlc_mode_direct_write in swreg2_sysctrl is valid

Bit	Attr	Reset Value	Description
2:0	RO	0x0	reserved

hevc_swreg42_pps_base
Address: Operational Base + offset (0x00a8)
the base address of pps

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_pps_base the base address of pps the base address of pps (the address should 128bit align) it is for storing sps(sequence parameter set) and pps(picture parameter set)
3:0	RO	0x0	reserved

hevc_swreg43_rps_base
Address: Operational Base + offset (0x00ac)
the base address of rps

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_rps_base rps base address rps(reference picture set) base address (the address should 128bit align)
3:0	RO	0x0	reserved

hevc_swreg44_cabac_error_en
Address: Operational Base + offset (0x00b0)
cabac error enable config

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_cabac_error_e cabac error enable regs cabac error enable regs

hevc_swreg45_cabac_error_status
Address: Operational Base + offset (0x00b4)
cabac error status

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_colmv_error_ref_picidx colmv error ref picidx when sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module
27:0	RW	0x0000000	sw_cabac_error_status cabac error status cabac error status

hevc_swreg46_cabac_error_ctu
Address: Operational Base + offset (0x00b8)
cabac error ctu

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x40	sw_streamfifo_space2full stream fifo space to full It is for debug use, to tell the stream fifo space to full
15:8	RW	0x00	sw_cabac_error_ctu_yoffset cabac error ctu yoffset cabac error ctu yoffset
7:0	RW	0x00	sw_cabac_error_ctu_xoffset cabac error ctu xoffset cabac error ctu xoffset

hevc_swreg47_sao_ctu_position
Address: Operational Base + offset (0x00bc)
sao ctu position

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_saowr_yoffset saowr y offset saowr y offset , its unit is 4 pixels
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_saowr_xoffet saowr x address offset saowr x address offset, its unit is 128bit

hevc_swreg64_performance_cycle
Address: Operational Base + offset (0x0100)
hevc performance cycle

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_performance_cycle hevc running cycle hevc running cycle if just want to analys a frame performance cycle, should set the register 0 before start a frame

hevc_swreg65_axi_ddr_rdata
Address: Operational Base + offset (0x0104)
axi ddr read data num

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_rdata axi ddr rdata num axi ddr rdata num, the unit is byte

hevc_swreg66_axi_ddr_wdata
Address: Operational Base + offset (0x0108)
axi ddr write data number

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_wdata hevc write data byte num hevc write data byte num

3.4.4 VDPU Registers Summary

Name	Offset	Size	Reset Value	Description
VDPU_SWREG0_NEW_VERSION	0x0000	W	0x03680000	ID register(read only)
VDPU_SWREG0	0x0000	W	0x00000000	Register0000 Abstract
VDPU_SWREG1	0x0004	W	0x00000000	interrupt register decoder
VDPU_SWREG2	0x0008	W	0x01000400	device configuration register decoder
VDPU_SWREG3	0x000c	W	0x00000001	Device control register 0(decmode, picture type etc)
VDPU_SWREG4_H264	0x0010	W	0x00000000	decoder control register 1(picture parameters)
VDPU_SWREG4	0x0010	W	0x00000000	decoder control register 1(picture parameters)
VDPU_SWREG5	0x0014	W	0x00000000	decoder control register2 (stream decoding table selects)
VDPU_SWREG5_H264	0x0014	W	0x00000000	decoder control register2 (stream decoding table selects)
VDPU_SWREG6	0x0018	W	0x00000000	decoder control register 3(stream buffer information)
VDPU_SWREG7	0x001c	W	0x00000000	decoder control register 4(H264)
VDPU_SWREG8	0x0020	W	0x00000000	decoder control register 5
VDPU_SWREG9	0x0024	W	0x00000000	decoder control register 6
VDPU_SREG10_H264_RLC	0x0028	W	0x00000000	Base address for differential motion vector base address
VDPU_SREG10_H264	0x0028	W	0x00000000	Base address for differential motion vector base address
VDPU_SWREG11_H264_RLC	0x002c	W	0x00000000	decoder control register 7
VDPU_SWREG11_H264	0x002c	W	0x00000000	decoder control register 7
VDPU_SWREG12	0x0030	W	0x00000000	Base address for RLC data (RLC) / stream start address/decoded
VDPU_SWREG13	0x0034	W	0x00000000	Base address for decoded picture / base address for JPEG deco
VDPU_SWREG14	0x0038	W	0x00000000	Base address for reference picture index 0 / base address for J
VDPU_SWREG15_JPEG_ROI	0x003c	W	0x00000000	JPEG roi control
VDPU_SWREG15	0x003c	W	0x00000000	Base address for reference picture index 1 / JPEG control
VDPU_SWREG16	0x0040	W	0x00000000	base address for reference picture index 2 / List of VLC code len
VDPU_SWREG17	0x0044	W	0x00000000	Base address for reference picture index 3 / List of VLC code le

Name	Offset	Size	Reset Value	Description
VDPU_SWREG18	0x0048	W	0x00000000	Base address for reference picture index 4 /MPE
VDPU_SWREG19	0x004c	W	0x00000000	Base address for reference picture index 5
VDPU_SWREG20	0x0050	W	0x00000000	Base address for reference picture index 6
VDPU_SWREG21	0x0054	W	0x00000000	Base address for reference picture index 7
VDPU_SWREG22	0x0058	W	0x00000000	Base address for reference picture index 8
VDPU_SWREG23	0x005c	W	0x00000000	Base address for reference picture index 9
VDPU_SWREG24	0x0060	W	0x00000000	Base address for reference picture index 10
VDPU_SWREG25	0x0064	W	0x00000000	Base address for reference picture index 11
VDPU_SWREG26	0x0068	W	0x00000000	Base address for reference picture index 12
VDPU_SWREG27	0x006c	W	0x00000000	Base address for reference picture index 13
VDPU_SWREG28	0x0070	W	0x00000000	Base address for reference picture index14
VDPU_SWREG29	0x0074	W	0x00000000	Base address for reference picture index15
VDPU_SWREG30	0x0078	W	0x00000000	Reference picture numbers for index 0 and 1 (H264 VLC
VDPU_SWREG31	0x007c	W	0x00000000	Reference picture numbers for index 2 and 3 (H264 VLC) /
VDPU_SWREG32	0x0080	W	0x00000000	Reference picture numbers for index 4 and 5 (H264 VLC)
VDPU_SWREG33	0x0084	W	0x00000000	Reference picture numbers for index 6 and 7 (H264 VLC)
VDPU_SWREG34	0x0088	W	0x00000000	Reference picture numbers for index 8 and 9 (H264 VLC)
VDPU_SWREG35_JPEG_ROI	0x008c	W	0x00000000	JPEG roi offest/dc base address
VDPU_SWREG35	0x008c	W	0x00000000	Reference picture numbers for index 10 and 11 (H264 VLC)
VDPU_SWREG36	0x0090	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)
VDPU_SWREG36_JPEG_ROI	0x0090	W	0x00000000	JPEG roi offset/dc length
VDPU_SWREG37	0x0094	W	0x00000000	Reference picture numbers for index 14 and 15 (H264 VLC)
VDPU_SWREG38	0x0098	W	0x00000000	Reference picture long term flags (H264 VLC) prediction filt
VDPU_SWREG38_H264	0x0098	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)
VDPU_SWREG39	0x009c	W	0x00000000	Reference picture valid flags (H264 VLC) prediction filter ta
VDPU_SWREG39_H264	0x009c	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)
VDPU_SWREG40	0x00a0	W	0x00000000	Base address for standard dependent tables

Name	Offset	Size	Reset Value	Description
VDPU_SWREG41	0x00a4	W	0x00000000	Base address for direct mode motion vectors
VDPU_SWREG42	0x00a8	W	0x00000000	bi_dir initial ref pic list register (0-2) prediction filter taps
VDPU_SWREG43	0x00ac	W	0x00000000	bi-dir initial ref pic list register (3-5) prediction filter taps
VDPU_SWREG44	0x00b0	W	0x00000000	bi-dir initial ref pic list register (6-8) prediction filter taps
VDPU_SWREG45	0x00b4	W	0x00000000	bi-dir initial ref pic list register (9-11) prediction filter taps
VDPU_SWREG46	0x00b8	W	0x00000000	bi-dir initial ref pic list register (12-14)
VDPU_SWREG47	0x00bc	W	0x00000000	bi-dir and P fwd initial ref pic list register (15 and P 0-3)
VDPU_SWREG48	0x00c0	W	0x00000000	Error concealment register
VDPU_SWREG49	0x00c4	W	0x00000000	Prediction filter tap register for H264, MPEG4
VDPU_SWREG50	0x00c8	W	0xfbb56f80	Synthesis configuration register decoder 0 (read only)
VDPU_SWREG51	0x00cc	W	0x00000000	Reference picture buffer control register
VDPU_SWREG52	0x00d0	W	0x00000000	Reference picture buffer information register 1 (read only)
VDPU_SWREG53	0x00d4	W	0x00000000	Reference picture buffer information register 2 (read only)
VDPU_SWREG54	0x00d8	W	0xe5da0000	Synthesis configuration register decoder 1 (read only)
VDPU_SWREG55	0x00dc	W	0x00000000	Reference picture buffer 2 / Advanced prefetch control register
VDPU_SWREG56	0x00e0	W	0x00000000	Reference buffer information register 3 (read only)
VDPU_SWREG57_INTRA_INTER	0x00e4	W	0x00000000	intra_dll3t,intra_dblspeed,inter_dblspeed,stream_len_hi
VDPU_SWREG57	0x00e4	W	0x00000000	intra_dll3t,intra_dblspeed,inter_dblspeed,stream_len_hi
VDPU_SWREG58	0x00e8	W	0x00000000	Decoder debug register 0 (read only)
VDPU_SWREG59	0x00ec	W	0x00000000	H264 Chrominance 8 pixel interleaved data base
VDPU_SWREG60	0x00f0	W	0x00000000	Interrupt register post-processor
VDPU_SWREG61	0x00f4	W	0x01010100	Device configuration register post-processor
VDPU_SWREG62	0x00f8	W	0x00000000	Deinterlace control register
VDPU_SWREG63	0x00fc	W	0x00000000	base address for reading post-processing input picture uminan
VDPU_SWREG64	0x0100	W	0x00000000	Base address for reading post-processing input picture Cb/Ch
VDPU_SWREG65	0x0104	W	0x00000000	Base address for reading post-processing input picture Cr
VDPU_SWREG66	0x0108	W	0x00000000	Base address for writing post-processed picture luminance/RGB

Name	Offset	Size	Reset Value	Description
VDPU_SWREG67	0x010c	W	0x00000000	Base address for writing post-processed picture Ch
VDPU_SWREG68	0x0110	W	0x00000000	Register for contrast adjusting
VDPU_SWREG69	0x0114	W	0x00000000	Register for colour conversion and contrast adjusting
VDPU_SWREG70	0x0118	W	0x00000000	Register for colour conversion 0
VDPU_SWREG71	0x011c	W	0x00000000	Register for colour conversion 1 + rotation mode
VDPU_SWREG72	0x0120	W	0x00000000	PP input size and -cropping register
VDPU_SWREG73	0x0124	W	0x00000000	PP input picture base address for Y bottom field
VDPU_SWREG74	0x0128	W	0x00000000	PP input picture base for Ch bottom field
VDPU_SWREG79	0x013c	W	0x00000000	Scaling ratio register 1 & padding for B
VDPU_SWREG80	0x0140	W	0x00000000	Scaling register 0 ratio & padding for R and G
VDPU_SWREG81	0x0144	W	0x00000000	Scaling ratio register 2
VDPU_SWREG82	0x0148	W	0x00000000	Rmask register
VDPU_SWREG83	0x014c	W	0x00000000	Gmask register
VDPU_SWREG84	0x0150	W	0x00000000	Bmask register
VDPU_SWREG85	0x0154	W	0x00000000	Post-processor control register
VDPU_SWREG86	0x0158	W	0x00000000	Mask 1 start coordinate register
VDPU_SWREG87	0x015c	W	0x00000000	Mask 2 start coordinate register
VDPU_SWREG88	0x0160	W	0x00000000	Mask 1 size and PP original width register
VDPU_SWREG89	0x0164	W	0x00000000	Mask 2 size register
VDPU_SWREG90	0x0168	W	0x00000000	PiP register 0
VDPU_SWREG91	0x016c	W	0x00000000	PiP register 1 and dithering control
VDPU_SWREG92	0x0170	W	0x00000000	Display width and PP input size extension register
VDPU_SWREG93	0x0174	W	0x00000000	Display width and PP input size extension register
VDPU_SWREG94	0x0178	W	0x00000000	Base address for alpha blend 2 gui component
VDPU_SWREG95	0x017c	W	0x00000000	Base address for alpha blend 2 gui component
VDPU_SWREG98	0x0188	W	0x00000000	PP outupt width/height extension
VDPU_SWREG99	0x018c	W	0xe000f000	PP fuse register (read only)
VDPU_SWREG100	0x0190	W	0xff874780	Synthesis configuration register post-processor (read only)
VDPU_SWREG101	0x0194	W	0x00000000	soft reset signals
VDPU_SWREG102	0x0198	W	0x00000000	vpu performance cycle
VDPU_SWREG103	0x019c	W	0x00000000	AXI DDR READ DATA NUM
VDPU_SWREG104	0x01a0	W	0x00000000	Register0000 Abstract
VDPU_SWREG105	0x01a4	W	0x00000000	
VDPU_SWREG106	0x01a8	W	0x00000000	
VDPU_SWREG107	0x01ac	W	0x00000000	

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address
VCODEC_MMU_STATUS	0x0004	W	0x00000018	MMU status register
VCODEC_MMU_COMMAND	0x0008	W	0x00000000	MMU command register

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
VCODEC_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
VCODEC_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x0000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x0004	W	0x06110206	L2 cache SIZE
pref_cache_STATUS	0x0008	W	0x00000000	Status register
pref_cache_COMMAND	0x0010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x0014	W	0x00000000	clear page register
pref_cache_MAX_READS	0x0018	W	0x0000001c	maximum read register
pref_cache_PERFCNT_SRC0	0x0020	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL0	0x0024	W	0x00000000	performance counter 0 value register
pref_cache_PERFCNT_SRC1	0x0028	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL1	0x002c	W	0x00000000	performance counter 1 value register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.4.5 VDPU Detail Register Description

VDPU_SWREG0_NEW_VERSION

Address: Operational Base + offset (0x0000)

ID register(read only)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RO	0x3	major_version 0:1080p support 1:2160p support
23:16	RO	0x68	minor_version 0: audis 1: audi 2: maybach 3:audib ff:share memory with hevc,so should read verision from hevc register
15:0	RW	0x0000	build the rtl's svn num in ic server

VDPU_SWREG0

Address: Operational Base + offset (0x0000)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pro_num product number
15:12	RW	0x0	major_version major_version major_version
11:4	RW	0x00	minor_version minor_version minor_version
3	RW	0x0	ID_ASCII_EN ASCII type product ID enable ASCII type product ID enable
2:0	RW	0x0	build_version build_version build_version

VDPU_SWREG1
Address: Operational Base + offset (0x0004)
interrupt register decoder

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	sw_dec_pic_inf B slice detected. This signal is driven high during picture ready interrupt if B-type slice is found. This bit does not launch interrupt but is used to inform SW about h264 tools. [note]:the h264 decoder will use these bits.
23:19	RO	0x0	reserved
18	RW	0x0	sw_dec_timeout Interrupt status bit decoder timeout. When high the decoder 0 has been idling for too long. HW will self reset. Possible only if timeout interrupt is enabled [note]:the h264 decoder will use these bits.
17	RW	0x0	sw_dec_slice_int Interrupt status bit dec_slice_decoded. When high SW must set new base addresses for sw_dec_out_base and sw_jpg_ch_out_base before reseting this status bit. Used for JPEG snapshot modes [note]:the JPEG decoder will use these bits.
16	RW	0x0	sw_dec_error_int Interrupt status bit input stream error. When high, an error is found in input data stream decoding. HW will self reset. [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
15	RW	0x0	sw_dec_aso_int Interrupt status bit ASO (Arbitrary Slice Ordering) detected.When high, ASO detected in input data stream decoding. HW will self reset. [note]:the h264 decoder will use these bits.
14	RW	0x0	sw_dec_buffer_int Interrupt status bit input buffer empty. When high, input stream buffer is empty but picture is not ready. HW will not self reset. [note]:the h264 decoder will use these bits.
13	RW	0x0	sw_dec_bus_int Interrupt status bit bus. Error response from bus. HW will self reset [note]:the h264 decoder will use these bits.
12	RW	0x0	sw_dec_rdy_int Interrupt status bit decoder. When this bit is high decoder has decoded a picture. HW will self reset. [note]:the h264 decoder will use these bits.
11:9	RO	0x0	reserved
8	RW	0x0	sw_dec_irq Decoder IRQ. When high, decoder requests an interrupt. SW will reset this after interrupt is handled. [note]:the h264 decoder will use these bits.
7:5	RO	0x0	reserved
4	RW	0x0	sw_dec_irq_dis Decoder IRQ disable. When high, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt statuses. [note]:the h264 decoder will use these bits.
3:1	RO	0x0	reserved
0	RW	0x0	sw_dec_en decoder enable. Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when picture is processed or ASO or stream error is detected or bus error or timeout interrupt is given. [note]:the h264 decoder will use these bits.

VDPU_SWREG2

Address: Operational Base + offset (0x0008)

device configuration register decoder

Bit	Attr	Reset Value	Description
31:24	RW	0x01	sw_dec_axi_rd_id Read ID used for decoder reading services in AXI bus (if connected to AXI) [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
23	RW	0x0	sw_dec_timeout_e Timeout interrupt enable. If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture. [note]:the h264 decoder will use these bits.
22	RW	0x0	sw_dec_strswap32_e Decoder input 32bit data swap for stream data (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) [note]:the h264 decoder will use these bits.
21	RW	0x0	sw_dec_strendian_e Decoder input endian mode for stream data: 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order) [note]:the h264 decoder will use these bits.
20	RW	0x0	sw_dec_inswap32_e Decoder input 32bit data swap for other than stream data (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) [note]:the h264 decoder will use these bits.
19	RW	0x0	sw_dec_outswap32_e Decoder output 32bit data swap (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) [note]:the h264 decoder will use these bits.
18	RW	0x0	sw_dec_data_disc_e Data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally. [note]:the h264 decoder will use these bits.
17	RW	0x0	sw_tiled_mode_msb Tiled mode msb. Concanated to Tiled mode lsb which form 2 bit tiled mode. Definition of tiledmode: 0 = Tiled mode not enabled 1 = Tiled mode enabled for 8x4 tile size 2,3 Reserved [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
16:11	RW	0x00	sw_dec_latency Decoder master interface additional latency. Can be used to slow down decoder HW between services in steps of 8 clock cycles: 0 = no latency 1 = minimum 8 cycles of IDLE between services 2 = minimum 16 cycles of IDLE between services ... 63 = minimum latency of 504 cycles of IDLE between services [note]:the h264 decoder will use these bits.
10	RW	0x1	sw_dec_clk_gate_e Decoder dynamic clock gating enable: 0 = Clock is running for all structures 1 = Clock is gated for decoder structures that are not used Note: Clock gating value can be changed only when decoder is disabled
9	RW	0x0	sw_dec_in_endian Decoder input endian mode for other than stream data: 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order) [note]:the h264 decoder will use these bits.
8	RW	0x0	sw_dec_out_endian Decoder output endian mode: 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order) [note]:the h264 decoder will use these bits.
7	RW	0x0	sw_tiled_mode_lsb Tiled mode lsb. Concanated to Tiled mode msb which form 2 bit tiled mode. Defined in tiled_mode_msb [note]:the h264 decoder will use these bits.
6	RW	0x0	sw_dec_adv_pre_dis Advanced PREFETCH mode disable (advanced reference picture reading mode for video) [note]:the h264 decoder will use these bits.
5	RW	0x0	sw_dec_scmd_dis AXI Single Command Multiple Data 0 disable. (where only the first addresses of the burst are given from address generator). This bit is used to disable the feature (possible SW workaround if something is not working correctly) [note]:the h264 decoder will use these bits.
4:0	RW	0x00	sw_dec_max_burst Maximum burst length for decoder bus transactions. Valid values: AXI: 1-16 [note]:the h264 decoder will use these bits.

VDPU_SWREG3

Address: Operational Base + offset (0x000c)
Device control register 0(decmode, picture type etc)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_dec_mode Decoding mode: 0 = H.264, 1 = MPEG-4, 2 = H.263, 3 = JPEG, 5 = MPEG-2, 6 = MPEG-1, others = reserved [note]:all the decoder mode will use these bits.
27	RW	0x0	sw_rlc_mode_e RLC mode enable: 1 = HW decodes video from RLC input data + side information (Differential MV's, separate DC coeffs, Intra 4x4 modes, MB control). Valid only for H.264 Baseline and MPEG- 4 SP. 0 = HW decodes video from bit stream (VLC mode) + side information [note]:the h264 and MPEG4 decoder will use these bits.
26	RW	0x0	sw_skip_mode
25	RW	0x0	reserved
24	RW	0x0	sw_pjpeg_e Progressive JPEG enable: 0 = baseline JPEG 1 = progressive JPEG
23	RW	0x0	sw_pic_interlace_e Coding mode of the current picture: 0 = progressive 1 = interlaced [note]:the h264 decoder will use these bits.
22	RW	0x0	sw_pic_fieldmode_e Structure of the current picture (residual structure) 0 = frame structure, this means MBAFF structured picture for interlaced sequence 1 = field structure [note]:the h264 decoder will use these bits.
21	RW	0x0	sw_pic_b_e B picture enable for current picture: 0=picture type is I or P depending on sw_pic_inter_e 1=picture type is BI (vc1)/D (mpeg1) or B depending on sw_pic_inter_e (not valid for H264 since its slice based information)

Bit	Attr	Reset Value	Description
20	RW	0x0	sw_pic_inter_e Picture type. 1= Inter type (P) 0= Intra type (I) See also sw_pic_b_e
19	RW	0x0	sw_pic_topfield_e If field structure is enabled this bit informs which one of the fields is being decoded: 0 = bottom field 1 = top field [note]:the h264 decoder will use these bits.
18	RW	0x0	sw_fwd_interlace_e Coding mode of forward reference picture: 0 = progressive 1 = interlaced Note: for backward reference picture the coding mode is always same as for current picture.
17	RW	0x0	reserved
16	RW	0x0	sw_ref_topfield_e Indicates which field should be used as reference if sw_ref_frames = 0 0 = bottom field 1 = top field used only in VC-1 mode
15	RW	0x0	sw_dec_out_dis Disable decoder output picture writing: 0 = Decoder output picture is written to external memory 1 = Decoder output picture is not written to external memory [note]:the h264 decoder will use these bits.
14	RW	0x0	sw_filtering_dis De-block filtering disable 1 = filtering is disabled for current picture 0 = filtering is enabled for current picture [note]:the h264 decoder will use these bits.
13	RW	0x0	sw_pic_fixed_quant sw_pic_fixed_quant (DEC mode is VC-1 and AVS) 0 = Quantization parameter can vary inside picture 1 = Quantization parameter is fixed (pquant) sw_mvc_e(DEC mode is H264) multi view coding enable. Possible for H264 only [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
12	RW	0x0	sw_write_mvs_e Direct mode motion vector write enable for current picture / MPEG2 motion vector write enable for error concealment purposes: 0 = writing disabled for current picture 1 = the direct mode motion vectors are written to extrenal memory. H264 direct mode motion vectors are written to DPB aside with the corresponding reference picture. Other decoding mode dir mode mvs are written to external memory starting from sw_dir_mv_base [note]:the h264 decoder will use these bits.
11	RW	0x0	sw_reftopfirst_e Indicates which FWD reference field has been decoded first. 0 = FWD reference bottom field 1 = FWD reference top field [note]:the h264 decoder will use these bits.
10	RW	0x0	sw_seq_mbaff_e Sequence includes MBAFF coded pictures [note]:the h264 decoder will use these bits.
9	RW	0x0	sw_picord_count_e h264_high config: Picture order count table read enable. If enabled HW will read picture order counts from memory in the beginning of picture [note]:the h264 decoder will use these bits.
8	RW	0x0	sw_dec_timeout_mode dec timeout mode selset when 1'b0,timeout cycle is 181'b1 when 1'b1,timeout cycle is 221'b1 [note]:the h264 decoder will use these bits.
7:0	RW	0x01	sw_dec_axi_wr_id Write ID used for decoder writing services in AXI bus (if connected to AXI) [note]:the h264 decoder will use these bits.

VDPU_SWREG4_H264
Address: Operational Base + offset (0x0010)
decoder control register 1(picture parameters)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_pic_mb_width Picture width in macroblocks = ((width in pixels + 15) /16) [note]:the h264 decoder will use these bits.
22:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:11	RW	0x00	sw_pic_mb_height_p Picture height in macroblocks =((height in pixels+15)/16). Picture height is informed as size of the (progressive) frame also for single field (of interlaced content) is being decoded [note]:the h264 decoder will use these bits.
10:5	RO	0x0	reserved
4:0	RW	0x00	sw_ref_frames 264: num_ref_frames, maximum number of short and long term reference frames in decoded picture buffer.

VDPU_SWREG4
Address: Operational Base + offset (0x0010)
decoder control register 1(picture parameters)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_pic_mb_width Picture width in macroblocks = ((width in pixels + 15) /16)
22:19	RW	0x0	sw_mb_width_off The amount of meaningfull horizontal pixels in last MB (width offset) 0 if exactly 16 pixels multiple picture and all the horizontal pixels in last MB are meaningfull
18:11	RW	0x00	sw_pic_mb_height_p Picture height in macroblocks =((height in pixels+15)/16). Picture height is informed as size of the (progressive) frame also for single field (of interlaced content) is being decoded
10:7	RW	0x0	sw_mb_height_off The amount of menaingfull vertical pixels in last MB (height offset 0 if exactly 16 pixels multiple picture and all the vertical pixels in last MB are meaningfull
6	RW	0x0	sw_alt_scan_e indicates alternative vertical scan method used for interlacedd frames
5:3	RW	0x0	sw_pic_mb_w_ext Picture mb width extension. If sw_pic_mb_width does not fit tod 9 bits then these bits are used to increase the range upto 11 bits (used as 3 msb)
2:0	RW	0x0	sw_pic_mb_h_ext Picture mb height extension. If sw_pic_mb_height_p does not fit to 9 bits then these bits are used to increase the range upto 11 bits (used as 3 msb)

VDPU_SWREG5
Address: Operational Base + offset (0x0014)
decoder control register2 (stream decoding table selects)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_strm_start_bit Exact bit of stream start word where decoding can be started (assosiates with sw_rlc_vlc_base)
25	RW	0x0	sw_sync_marker_e Sync markers enable: '0' = synch markers are not used, '1' = synch markers are used. For progressive JPEG this indicates that there are restart markers in the stream after restart interval steps
24	RW	0x0	sw_type1_quant_e MPEG4: Type 1 quantization enable '0' = type 2 inverse Q method '1' = type 1 inverse Q method (Q-tables used) H264 (h264_high config:): scaling matrix enable: '0' = normal transform '1' = use scaling matrix for transform (read from external
23:19	RW	0x00	sw_ch_qp_offset Chroma Qp filter offset. (For H.264 this offset concerns Cb only)
18:14	RW	0x00	sw_ch_qp_offset2 Chroma Qp filter offset for cr type
13:1	RO	0x0	reserved
0	RW	0x0	sw_fieldpic_flag_e Flag for streamd that field_pic_flag exists in stream

VDPU_SWREG5_H264

Address: Operational Base + offset (0x0014)

decoder control register2 (stream decoding table selects)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_strm_start_bit Exact bit of stream start word where decoding can be started (assosiates with sw_rlc_vlc_base)
25	RO	0x0	reserved
24	RW	0x0	sw_type1_quant_e MPEG4: Type 1 quantization enable '0' = type 2 inverse Q method '1' = type 1 inverse Q method (Q-tables used) H264 (h264_high config:): scaling matrix enable: '0' = normal transform '1' = use scaling matrix for transform (read from external
23:19	RW	0x00	sw_ch_qp_offset Chroma Qp filter offset. (For H.264 this offset concerns Cb only)
18:14	RW	0x00	sw_ch_qp_offset2 Chroma Qp filter offset for cr type
13:1	RO	0x0	reserved
0	RW	0x0	sw_fieldpic_flag_e Flag for streamd that field_pic_flag exists in stream

VDPU_SWREG6
Address: Operational Base + offset (0x0018)
decoder control register 3(stream buffer information)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_start_code_e Bit for indicating stream start code existence: '0' = stream doesn't contain start codes '1' = stream contains start codes [note]:the h264 decoder will use these bits.
30:25	RW	0x00	sw_init_qp Initial value for quantization parameter (picture quantizer). [note]:the h264 decoder will use these bits.
24	RW	0x0	sw_ch_8pix_ileav_e Enable for additional chrominance data format writing where decoder writes chrominance in group of 8 pixels of Cb and then corresponding 8 pixels of Cr. Data is written to sw_dec_ch8pix_base. Cannot be used if tiled mode is enabled [note]:the h264 decoder will use these bits.
23:0	RW	0x000000	sw_stream_len Amount of stream data bytes in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (assosiates with sw_rlc_vlc_base). For VC-1 the buffer must include data for one picture/slice of the picture For H264/MPEG4/H263/MPEG2/MPEG1 the buffer must include at least data for one slice of the picture For JPEG the buffer size must be a multiple of 256 bytes or the amount of data for onepicture. [note]:the h264 decoder will use these bits.

VDPU_SWREG7
Address: Operational Base + offset (0x001c)
decoder control register 4(H264, VC-1 control)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_cabac_e CABAC enable [note]:the h264 decoder will use these bits.
30	RW	0x0	sw_blackwhite_e '0' = 4:2:0 sampling format '1' = 4:0:0 sampling format (H264 monochroma) [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
29	RW	0x0	sw_dir_8x8_infer_e Specifies the method to use to derive luma motion vectors in B_skip, B_Direct_16x16 and B_direct_8x8_inference_flag (see direct_8x8_inference flag) [note]:the h264 decoder will use these bits.
28	RW	0x0	sw_weight_pred_e Weighted prediction enable for P slices [note]:the h264 decoder will use these bits.
27:26	RW	0x0	sw_weight_bipr_idc weighted prediction specification for B slices: "00" = default weighted prediction is aplied to B slices "01" = explicit weighted prediction shall be applied to B slices "10" = implicit weighted prediction shall be applied to B slices [note]:the h264 decoder will use these bits.
25:21	RO	0x0	reserved
20:16	RW	0x00	sw_framenum_len H.264: Bit length of frame_num in data stream [note]:the h264 decoder will use these bits.
15:0	RW	0x0000	sw_framenum current frame_num, used to identify short-term reference frames. Used in reference picture reordering [note]:the h264 decoder will use these bits.

VDPU_SWREG8
Address: Operational Base + offset (0x0020)
decoder control register 5(H264 control)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_const_intra_e constrained_intra_pred_flag equal to 1 specifies that intra prediction uses only neighbouring intra macroblocks in prediction. When equal to 0 also neighbouring inter macroblocks are used in intra prediction process. [note]:the h264 decoder will use these bits.
30	RW	0x0	sw_filt_ctrl_pres deblocking_filter_control_present_flag indicates whether extra variables controlling characteristics of the deblocking filter are present in the slice header. [note]:the h264 decoder will use these bits.
29	RW	0x0	sw_rdpic_cnt_pres redundant_pic_cnt_present_flag specifies whether redundant_pic_cnt syntax elements [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
28	RW	0x0	sw_8x8trans_flag_e 8x8 transform flag enable for stream decoding [note]:the h264 decoder will use these bits.
27:17	RW	0x000	sw_refpic_mk_len Length of decoded reference picture marking bits [note]:the h264 decoder will use these bits.
16	RW	0x0	sw_idr_pic_e IDR (instantaneous decoding refresh) picture flag. [note]:the h264 decoder will use these bits.
15:0	RW	0x0000	sw_idr_pic_id idr_pic_id, identifies IDR (instantaneous decoding refresh) picture [note]:the h264 decoder will use these bits.

VDPU_SWREG9
Address: Operational Base + offset (0x0024)
decoder control register 6

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pps_id pic_parameter_set_id, identifies the picture parameter set that is referred to in the slice header. [note]:the h264 decoder will use these bits.
23:19	RW	0x00	sw_refidx1_active pecifies the maximum reference index that can be used while decoding inter predicted macro blocks. [note]:the h264 decoder will use these bits.
18:14	RW	0x00	sw_refidx0_active Specifies the maximum reference index that can be used while decoding inter predicted macro blocks. This is same as in previous decoders (width increased with q bit) [note]:the h264 decoder will use these bits.
13:8	RO	0x0	reserved
7:0	RW	0x00	sw_poc_length Length of picture order count field in stream [note]:the h264 decoder will use these bits.

VDPU_SREG10_H264_RLC
Address: Operational Base + offset (0x0028)
Base address for differential motion vector base address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_diff_mv_base for H264 and MPEG4, RLC mode: Differential motion vector base address.
1:0	RO	0x0	reserved

VDPU_SREG10_H264
Address: Operational Base + offset (0x0028)
Base address for differential motion vector base address

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_pinit_rlist_f9 initial reference picture list for P forward picid 9
24:20	RW	0x00	sw_pinit_rlist_f8 initial reference picture list for P forward picid 8
19:15	RW	0x00	sw_pinit_rlist_f7 initial reference picture list for P forward picid 7
14:10	RW	0x00	sw_pinit_rlist_f6 initial reference picture list for P forward picid 6
9:5	RW	0x00	sw_pinit_rlist_f5 initial reference picture list for P forward picid 5
4:0	RW	0x00	sw_pinit_rlist_f4 initial reference picture list for P forward picid 4

VDPU_SWREG11_H264_RLC
Address: Operational Base + offset (0x002c)
decoder control register 7

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_i4x4_or_dc_base RLC mode: H.264: Intra prediction 4x4 mode base address. RLC mode: MPEG-4: DC component base address.
1:0	RO	0x0	reserved

VDPU_SWREG11_H264
Address: Operational Base + offset (0x002c)
decoder control register 7

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_pinit_rlist_f15 Initial reference picture list for P forward picid 15
24:20	RW	0x00	sw_pinit_rlist_f14 Initial reference picture list for P forward picid 14
19:15	RW	0x00	sw_pinit_rlist_f13 Initial reference picture list for P forward picid 13
14:10	RW	0x00	sw_pint_rlist_f12 Initial reference picture list for P forward picid 12
9:5	RW	0x00	sw_pint_rlist_f11 Initial reference picture list for P forward picid 11
4:0	RW	0x00	sw_pint_rlist_f10 Initial reference picture list for P forward picid 10

VDPU_SWREG12
Address: Operational Base + offset (0x0030)
Base address for RLC data (RLC) / stream start address/decoded

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_rlc_vlc_base RLC mode: Base address for RLC data (swreg3.sw_rlc_mode_e = 1). VLC mode: Stream start address / end addr+I288ess with byte precision (swreg4.rlc_mode_en = 0), start bit number in swreg5.stream_start_bit. When sw_dec_buffer_int is high or sw_dec_e is low this register contains HW return value of last_byte_address (not valid for jpeg) where stream has been read (and used) in accuracy of byte. For debug purposes the last_byte_address is also written when stream error/ASO is detected even though it may not be accurate. [note]:the h264 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG13
Address: Operational Base + offset (0x0034)
Base address for decoded picture / base address for JPEG deco

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dec_out_base Video: Base address for decoder output picture. Points directly to start of decoder output picture or field. JPEG snapshot: Base address for decoder output luminance picture [note]:the h264 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG14
Address: Operational Base + offset (0x0038)
Base address for reference picture index 0 / base address for J

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer0_base Base address for reference picture index 0. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer0_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer0_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG15_JPEG_ROI
Address: Operational Base + offset (0x003c)
JPEG roi control

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	sw_jpegroi_in_endian jpeg offset input endian sw_jpegroi_in_endian 0 = big endian (0-1-2-3 order) 1 = little endian (3-2-1-0 order)
18	RW	0x0	sw_jpegroi_in_swap32 jpeg offset input 32-bit swap sw_jpegroi_in_swap32 0: no swapping of 32 bit words 1: 32bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1 byte order (also little endian should be enabled)
17:16	RW	0x0	sw_roi_sample_size ROI MB num sample each time ROI MB num sample each time 00:1 01:8 10:16 11:8
15:12	RW	0x0	sw_roi_distance roi distance The distance between the sample MB and ROI start MB
11:10	RW	0x0	sw_roi_out_sel roi output selection ROI output selection 00: output offset/dc 01: output picture 10: output offset/dc and picture 11: output offset/dc
9	RW	0x0	sw_roi_decode roi decode JPEG ROI decode 0: build offset/dc table 1: ROI decode
8	RW	0x0	sw_roi_en roi enable JPEG roi mode enable 0: normal jpeg decode mode 1: JPEG roi mode
7:0	RO	0x0	reserved

VDPU_SWREG15
Address: Operational Base + offset (0x003c)
Base address for reference picture index 1 / JPEG control

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer1_base Base address for reference picture index 1. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer1_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer1_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG16
Address: Operational Base + offset (0x0040)
base address for reference picture index 2 / List of VLC code len

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer2_base Base address for reference picture index 2. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer2_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer2_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG17
Address: Operational Base + offset (0x0044)
Base address for reference picture index 3 / List of VLC code le

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer3_base Base address for reference picture index 3. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_refer3_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer3_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG18
Address: Operational Base + offset (0x0048)
Base address for reference picture index 4 / VC1 control / MPE

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer4_base Base address for reference picture index 4. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer4_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer4_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG19
Address: Operational Base + offset (0x004c)
Base address for reference picture index 5

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer5_base Base address for reference picture index 5. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer5_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_refer5_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG20
Address: Operational Base + offset (0x0050)
Base address for reference picture index 6

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer6_base Base address for reference picture index 6. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer6_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer6_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG21
Address: Operational Base + offset (0x0054)
Base address for reference picture index 7

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer7_base Base address for reference picture index 7. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer7_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer7_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG22

Address: Operational Base + offset (0x0058)
Base address for reference picture index 8

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer8_base Base address for reference picture index 8. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer8_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer8_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG23
Address: Operational Base + offset (0x005c)
Base address for reference picture index 9

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer9_base Base address for reference picture index 9. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer9_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer9_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG24
Address: Operational Base + offset (0x0060)
Base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer10_base Base address for reference picture index 10. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer10_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer10_top_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG25
Address: Operational Base + offset (0x0064)
Base address for reference picture index 11

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	sw_refer11_base Base address for reference picture index 11. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer11_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer11_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG26
Address: Operational Base + offset (0x0068)
Base address for reference picture index 12

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer12_base Base address for reference picture index 12. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer12_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer12_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG27
Address: Operational Base + offset (0x006c)
Base address for reference picture index 13

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer13_base Base address for reference picture index 13. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer13_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_refer13_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG28
Address: Operational Base + offset (0x0070)
Base address for reference picture index14

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer14_base Base address for reference picture index 14. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer14_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer14_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG29
Address: Operational Base + offset (0x0074)
Base address for reference picture index15

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer15_base Base address for reference picture index 15. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer15_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer15_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG30
Address: Operational Base + offset (0x0078)
Reference picture numbers for index 0 and 1 (H264 VLC

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer1_nbr Number for reference picture index 1
15:0	RW	0x0000	sw_refer0_nbr Number for reference picture index 0

VDPU_SWREG31
Address: Operational Base + offset (0x007c)
Reference picture numbers for index 2 and 3 (H264 VLC) /

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer3_nbr Number for reference picture index 3
15:0	RW	0x0000	sw_refer2_nbr Number for reference picture index 2

VDPU_SWREG32
Address: Operational Base + offset (0x0080)
Reference picture numbers for index 4 and 5 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer5_nbr Number for reference picture index 5
15:0	RW	0x0000	sw_refer4_nbr Number for reference picture index 4

VDPU_SWREG33
Address: Operational Base + offset (0x0084)
Reference picture numbers for index 6 and 7 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer7_nbr Number for reference picture index 7
15:0	RW	0x0000	sw_refer6_nbr Number for reference picture index 6

VDPU_SWREG34
Address: Operational Base + offset (0x0088)
Reference picture numbers for index 8 and 9 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer9_nbr Number for reference picture index 9
15:0	RW	0x0000	sw_refer8_nbr Number for reference picture index 8

VDPU_SWREG35_JPEG_ROI
Address: Operational Base + offset (0x008c)
JPEG roi offest/dc base address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_jpegdcoff_base JPEG roi offset/dc base address JPEG roi offest/dc base address
1:0	RO	0x0	reserved

VDPU_SWREG35
Address: Operational Base + offset (0x008c)
Reference picture numbers for index 10 and 11 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer11_nbr Number for reference picture index 11
15:0	RW	0x0000	sw_refer10_nbr Number for reference picture index 10

VDPU_SWREG36
Address: Operational Base + offset (0x0090)
Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer13_nbr Number for reference picture index 13
15:0	RW	0x0000	sw_refer12_nbr Number for reference picture index 12

VDPU_SWREG36_JPEG_ROI
Address: Operational Base + offset (0x0090)
JPEG roi offset/dc length

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	sw_jpegdcoff_len sw_jpegdcoff_len The number of 64bit jpegdcoff, it can be used both when sw_roi_decode is 1'b0 or 1'b1

VDPU_SWREG37
Address: Operational Base + offset (0x0094)
Reference picture numbers for index 14 and 15 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer15_nbr Number for reference picture index 15
15:0	RW	0x0000	sw_refer14_nbr Number for reference picture index 14

VDPU_SWREG38
Address: Operational Base + offset (0x0098)
Reference picture long term flags (H264 VLC) prediction filt

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_3_3 Prediction filter set 3, tap 3
21:12	RW	0x000	sw_pred_bc_tap_4_0 Prediction filter set 4, tap 0

Bit	Attr	Reset Value	Description
11:2	RW	0x000	sw_perd_bc_tap_4_1 Prediction filter set 4, tap 1
1:0	RO	0x0	reserved

VDPU_SWREG38_H264

Address: Operational Base + offset (0x0098)

Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer_lterm_e long term flag for reference picture index [31:0]

VDPU_SWREG39

Address: Operational Base + offset (0x009c)

Reference picture valid flags (H264 VLC) prediction filter ta

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_4_2 Prediction filter set 4, tap 2
21:12	RW	0x000	sw_pred_bc_tap_4_3 Prediction filter set 4, tap 3
11:2	RW	0x000	sw_pred_bc_tap_5_0 Prediction filter set 5, tap 0
1:0	RO	0x0	reserved

VDPU_SWREG39_H264

Address: Operational Base + offset (0x009c)

Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer_valid_e valid flag for reference picture index [31:0]

VDPU_SWREG40

Address: Operational Base + offset (0x00a0)

Base address for standard dependent tables

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_qtable_base Base address for standard dependent tables: JPEG= AC,DC, QP tables MPEG4=QP table base address if type 1 quantization is used MPEG2=QP table base address H.264=base address for various tables [note]:the h264 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG41

Address: Operational Base + offset (0x00a4)
Base address for direct mode motion vectors

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dir_mv_base Direct mode motion vector write/read base address. For H264 this is used only for direct mode motion vector write base. Progressive JPEG: ACDC coefficient read/write base address. If current round is for DC components this base address is pointing to luminance (separate base adderesses for chrominances), for AC component rounds this base is used for current type
1:0	RO	0x0	reserved

VDPU_SWREG42
Address: Operational Base + offset (0x00a8)
bi_dir initial ref pic list register (0-2)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b2 Initial reference picture list for bi- direct backward picid 2
24:20	RW	0x00	sw_binit_rlist_f2 Initial reference picture list for bi- direct forward picid 2
19:15	RW	0x00	sw_binit_rlist_b1 Initial reference picture list for bi- direct backward picid 1
14:10	RW	0x00	sw_binit_rlist_f1 Initial reference picture list for bi- direct forward picid 1
9:5	RW	0x00	sw_binit_rlist_b0 Initial reference picture list for bi- direct backward picid 0
4:0	RW	0x00	sw_binit_rlist_f0 Initial reference picture list for bi- direct forward picid 0

VDPU_SWREG43
Address: Operational Base + offset (0x00ac)
bi-dir initial ref pic list register (3-5)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b5 Initial reference picture list for bi- direct backward picid 5
24:20	RW	0x00	sw_binit_rlist_f5 Initial reference picture list for bi- direct forward picid 5
19:15	RW	0x00	sw_binit_rlist_b4 Initial reference picture list for bi- direct backward picid 4
14:10	RW	0x00	sw_binit_rlist_f4 Initial reference picture list for bi- direct forward picid 4
9:5	RW	0x00	sw_binit_rlist_b3 Initial reference picture list for bi- direct backward picid 3

Bit	Attr	Reset Value	Description
4:0	RW	0x00	sw_binit_rlist_f3 Initial reference picture list for bi- direct forward picid 3

VDPU_SWREG44
Address: Operational Base + offset (0x00b0)
bi-dir initial ref pic list register (6-8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b8 Initial reference picture list for bi- direct backward picid 8
24:20	RW	0x00	sw_binit_rlist_f8 Initial reference picture list for bi- direct forward picid 8
19:15	RW	0x00	sw_binit_rlist_b7 Initial reference picture list for bi- direct backward picid 7
14:10	RW	0x00	sw_binit_rlist_f7 Initial reference picture list for bi- direct forward picid 7
9:5	RW	0x00	sw_binit_rlist_b6 Initial reference picture list for bi- direct backward picid 6
4:0	RW	0x00	sw_binit_rlist_f6 Initial reference picture list for bi- direct forward picid 6

VDPU_SWREG45
Address: Operational Base + offset (0x00b4)
bi-dir initial ref pic list register (9- 11)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b11 Initial reference picture list for bi- direct backward picid 11
24:20	RW	0x00	sw_binit_rlist_f11 Initial reference picture list for bi- direct forward picid 11
19:15	RW	0x00	sw_binit_rlist_b10 Initial reference picture list for bi- direct backward picid 10
14:10	RW	0x00	sw_binit_rlist_f10 Initial reference picture list for bi- direct forward picid 10
9:5	RW	0x00	sw_binit_rlist_b9 Initial reference picture list for bi- direct backward picid 9
4:0	RW	0x00	sw_binit_rlist_f9 Initial reference picture list for bi- direct forward picid 9

VDPU_SWREG46
Address: Operational Base + offset (0x00b8)
bi-dir initial ref pic list register (12- 14)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:25	RW	0x00	sw_binit_rlist_b14 Initial reference picture list for bi- direct backward picid 14
24:20	RW	0x00	sw_binit_rlist_f14 Initial reference picture list for bi- direct forward picid 14
19:15	RW	0x00	sw_binit_rlist_b13 Initial reference picture list for bi- direct backward picid 13
14:10	RW	0x00	sw_binit_rlist_f13 Initial reference picture list for bi- direct forward picid 13
9:5	RW	0x00	sw_binit_rlist_b12 Initial reference picture list for bi- direct backward picid 12
4:0	RW	0x00	sw_binit_rlist_f12 Initial reference picture list for bi- direct forward picid 12

VDPU_SWREG47
Address: Operational Base + offset (0x00bc)
bi-dir and P fwd initial ref pic list register (15 and P 0-3)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_pinit_rlist_f3 Initial reference picture list for P forward picid 3
24:20	RW	0x00	sw_pinit_rlist_f2 Initial reference picture list for P forward picid 2
19:15	RW	0x00	sw_pinit_rlist_f1 Initial reference picture list for P forward picid 1
14:10	RW	0x00	sw_pinit_rlist_f0 Initial reference picture list for P forward picid 0
9:5	RW	0x00	sw_binit_rlist_b15 Initial reference picture list for bi- direct backward picid 15
4:0	RW	0x00	sw_binit_rlist_f15 Initial reference picture list for bi- direct forward picid 15

VDPU_SWREG48
Address: Operational Base + offset (0x00c0)
Error concealment register

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_startmb_x Start MB from SW for X dimension. Used in error concealment case [note]:the h264 decoder will use these bits.
22:15	RW	0x00	sw_startmb_y Start MB from SW for Y dimension. Used in error concealment case [note]:the h264 decoder will use these bits.
14:0	RO	0x0	reserved

VDPU_SWREG49
Address: Operational Base + offset (0x00c4)
Prediction filter tap register for H264, MPEG4, VC1

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_0_0 Prediction filter set 0, tap 0 [note]:the h264 decoder will use these bits.
21:12	RW	0x000	sw_pred_bc_tap_0_1 Prediction filter set 0, tap 1 [note]:the h264 decoder will use these bits.
11:2	RW	0x000	sw_pred_bc_tap_0_2 Prediction filter set 0, tap 2 [note]:the h264 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG50
Address: Operational Base + offset (0x00c8)
Synthesis configuration register decoder 0 (read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	SW_DEC_MPEG2_PROF Decoding format support, MPEG-2 / MPEG-1 '0' = not supported '1' = supported
30:29	RO	0x3	SW_DEC_VC1_PROF Decoding format support, VC-1 0 = not supported 1 = supported up to simple profile 2 = supported up to main profile 3 = supported up to advanced profile
28	RO	0x1	SW_DEC_JPEG_PROF Decoding format support, JPEG 0 = not supported 1 = supported
27:26	RO	0x2	SW_DEC_MPEG4_PROF Decoding format support, MPEG-4 / H.263 0 = not supported 1 = supported up to simple profile 2 = supported up to advanced simple profile
25:24	RO	0x3	SW_DEC_H264_PROF Decoding format support, H.264 0 = not supported 1 = supported up to baseline profile 2 = supported up to high profile labeled stream with restricted high profile tools [note]:the h264 decoder will use these bits.
23	RO	0x1	reserved

Bit	Attr	Reset Value	Description
22	RO	0x0	SW_DEC_PJEPEG_EXIT Progressive JPEG support: '0' = Not supported '1' = supported
21	RO	0x1	SW_DEC_OBUFF_LEVEL Decoder output buffer level: '0' = 1 MB buffering is used '1' = 4 MB buffering is used [note]:the h264 decoder will use these bits.
20	RO	0x1	SW_REF_BUFF_EXIST [note]:the h264 decoder will use these bits.
19:16	RO	0x5	SW_DEC_BUS_STRD [note]:the h264 decoder will use these bits.
15:14	RO	0x1	SW_DEC_SYNTH_LAN [note]:the h264 decoder will use these bits.
13:12	RO	0x2	SW_DEC_BUS_WIDTH 0 = error 1 = 32 bit bus 2 = 64 bit bus 3 = 128 bit bus [note]:the h264 decoder will use these bits.
11	RO	0x1	reserved
10:0	RO	0x780	SW_DEC_MAX_OWIDTH Max configured decoder video resolution that can be decoded. Informed as width of the picture in pixels [note]:the h264 decoder will use these bits.

VDPU_SWREG51
Address: Operational Base + offset (0x00cc)
Reference picture buffer control register

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_refbu_e Refer picture buffer enable: '0' = refer picture buffer disabled '1' = refer picture buffer enabled. Valid if picture size is QVGA or more [note]:the h264 decoder will use these bits.
30:19	RW	0x000	sw_refbu_thr Reference buffer disable threshold value (cache miss amount). Used to buffer shut down (if more misses than allowed) [note]:the h264 decoder will use these bits.
18:14	RW	0x00	sw_refbu_picid The used reference picture ID for reference buffer usage [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
13	RW	0x0	sw_refbu_eval_e Enable for HW internal reference ID calculation. If given threshold level is reached by any picture_id after first MB row, that picture_id is used for reference buffer fill for rest of the picture [note]:the h264 decoder will use these bits.
12	RW	0x0	sw_refbu_fparmod_e Field parity mode enable. Used in refbufferd evaluation mode '0' = use the result field of the evaluation '1' = use the parity mode field [note]:the h264 decoder will use these bits.
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_refbu_y_offset Y offset for refbufferd. This coordinate is used to compensate the global motion of the video for better buffer hit rate [note]:the h264 decoder will use these bits.

VDPU_SWREG52
Address: Operational Base + offset (0x00d0)
Reference picture buffer information register 1 (read only)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refbu_hit_sum The sum of the refbufferd hits of the picture. Determined for each 8x8 luminance partition of the picture. The proceeding of the HW calculation can be read during HW decoding [note]:the h264 decoder will use these bits.
15:0	RW	0x0000	sw_refbu_intra_sum The sum of the luminance 8x8 intra partitons of the picture. The proceeding of the HW calculation can be read during HW decoding [note]:the h264 decoder will use these bits.

VDPU_SWREG53
Address: Operational Base + offset (0x00d4)
Reference picture buffer information register 2 (read only)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RW	0x000000	sw_refbu_y_mv_sum The sum of the decoded motion vector y-components of the picture. The first luminance motion vector of each MB is used in calculation. Other motion vectors of the MB are discarded. Each motion vector is saturated between -256 - 255 before calculation. The proceeding of the HW calculation can be read during HW decoding [note]:the h264 decoder will use these bits.

VDPU_SWREG54
Address: Operational Base + offset (0x00d8)
Synthesis configuration register decoder 1 (read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	SW_DEC_JPEG_EXTENS JPEG sampling support extension for 411 and 444 samplings and support for bigger max resolution than 16 Mpix (up to 67Mpixels): '0' = not supported '1' = supported
30	RO	0x1	SW_DEC_REFBU_ILACE Refbufferd support for interlaced content: '0' = not supported '1' = supported [note]:the h264 decoder will use these bits.
29	RO	0x1	reserved
28	RO	0x0	SW_REF_BUFF2_EXIST Reference picture buffer 2 usage: '0' = not supported '1' = reference buffer 2 is used [note]:the h264 decoder will use these bits.
27:26	RO	0x1	reserved
25	RO	0x0	SW_DEC_RTL_ROM ROM implementation type (If design includes ROMs) '0': ROMs are implemented from actual ROM units '1': ROMs are impelemted from RTL
24	RO	0x1	reserved
23	RO	0x1	reserved
22	RO	0x1	SW_DEC_AVS_PROF Decoding format support, AVS 0 = not supported 1 = supported
21:20	RO	0x1	SW_DEC_MVC_PROF Decoding format support, MVC 0 = not supported 1 = supported
19	RO	0x1	reserved
18:17	RO	0x1	SW_DEC_TILED_L Tiled mode support level 0 = not supported 1 = supported with 8x4 tile size 2,3 = reserved [note]:the h264 decoder will use these bits.
16:0	RO	0x0	reserved

VDPU_SWREG55
Address: Operational Base + offset (0x00dc)
Reference picture buffer 2 / Advanced prefetch control register

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_refbu2_buf_e Refer picture buffer 2 enable: '0' = refer picture buffer disabled '1' = refer picture buffer enabled. Valid if picture size is QVGA or more (can be turned of by HW if threshold value reached) [note]:the h264 decoder will use these bits.
30:19	RW	0x000	sw_refbu2_thr Reference buffer disable threshold value (buffer miss amount). Used to buffer shut down (if more misses than allowed) [note]:the h264 decoder will use these bits.
18:14	RW	0x00	sw_refbu2_picid The used reference picture ID for reference buffer usage [note]:the h264 decoder will use these bits.
13:0	RW	0x0000	sw_apf_threshold Advanced prefetch threshold value. If current MB exceeds the threshold the advanced mode is not used. Value 0 disables threshold usage and advanced prefetch usage is restricted by internal memory limitation only [note]:the h264 decoder will use these bits.

VDPU_SWREG56
Address: Operational Base + offset (0x00e0)
Reference buffer information register 3 (read only)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refbu_top_sum The sum of the top partitions of the picture [note]:the h264 decoder will use these bits.
15:0	RW	0x0000	sw_refbu_bot_sum The sum of the bottom partitions of the picture [note]:the h264 decoder will use these bits.

VDPU_SWREG57_INTRA_INTER
Address: Operational Base + offset (0x00e4)
intra_dll3t,intra_dblspeed,inter_dblspeed,stream_len_hi

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:8	RO	0x00	debug_service debug_service signals service_wr[2:0], service_rd[3:0]

Bit	Attr	Reset Value	Description
7	RW	0x0	sw_cache_en cache enable 1'b1: cache enable 1'b0: cache disable when sw_cache_en is 1'b1, sw_pref_sigchan should also be 1'b1
6	RW	0x0	sw_pref_sigchan prefetch single channel enable 1'b1: prefetch single channel enable
5	RW	0x0	sw_axiwr_sel axi write master select 1'b0: auto sel encoder axi signals and decoder axi signals 1'b1: sel decoder axi signals (it only use to set bu_dec_e to 1'b0 in the middle of a frame)
4	RW	0x0	sw_paral_bus paral_bus enable when it is set to 1'b1, the axi support read and write service parallel; when it is set to 1'b0, the axi only support read and write serial
3	RW	0x0	sw_intra_dbl3t sw_intra_dbl3t In chroma dc intra prediction, when this bit is enable, there will 3 cycle enhance for every block
2	RW	0x0	sw_intra_dblspeed intra double speed enable Intra double speed enable
1	RW	0x0	sw_inter_dblspeed inter double speed enable Inter double speed enable
0	RW	0x0	sw_stream_len_hi stream length high bit The extension bit of sw_stream_len

VDPU_SWREG57

Address: Operational Base + offset (0x00e4)

intra_dll3t,intra_dblspeed,inter_dblspeed,stream_len_hi

Bit	Attr	Reset Value	Description
31	RW	0x0	fuse_dec_h264 1 = H.264 enabled
30	RW	0x0	fuse_dec_mpeg4 1 = MPEG-4/H.263 enabled
29	RW	0x0	fuse_dec_mpeg2 1 = MPEG-2/MPEG-1 enabled N
28	RW	0x0	reserved

Bit	Attr	Reset Value	Description
27	RW	0x0	fuse_dec_jpeg Field0000 Abstract 1 = JPEG enabled
26	RW	0x0	reserved
25	RW	0x0	fuse_dec_vc1 1 = VC1 enabled
24	RW	0x0	fuse_dec_pjpeg 1 = Progressive JPEG enabled (Requires also JPEG to be enabled
23	RW	0x0	reserved
22	RW	0x0	reserved
21	RW	0x0	reserved
20	RW	0x0	reserved
19	RW	0x0	reserved
18	RW	0x0	fuse_dec_mvc enabled (requires also H264 to be enabled)
17:16	RO	0x0	reserved
15	RW	0x0	fuse_dec_maxw_1920 1 = Max video width up to 1920 pixels enabled. Priority coded with priority 1.
14	RW	0x0	fuse_dec_maxw_1280 1 = Max video width up to 1280 pixels enabled. Priority coded with priority 2.
13	RW	0x0	fuse_dec_maxw_720 1 = Max video width up to 720 pixels enabled. Priority coded with priority 3.
12	RW	0x0	fuse_dec_maxw_352 1 = Max video width up to 352 pixels enabled. Priority coded with priority 4
11:8	RO	0x0	reserved
7	RW	0x0	fuse_dec_refbuffer 1 = reference buffer used
6:0	RO	0x0	reserved

VDPU_SWREG58
Address: Operational Base + offset (0x00e8)
Decoder debug register 0 (read only)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	debug_mv_req mvst_mv_req signal value
29	RO	0x0	debug_rlc_req prtr_res_y_req signal value
28	RO	0x0	debug_res_y_req prtr_res_y_req signal value

Bit	Attr	Reset Value	Description
27	RO	0x0	debug_res_c_req prtr_res_c_req signal value
26	RO	0x0	debug_strm_da_e strm_da_e signal value
25	RO	0x0	debug_framerdy dfbu_framerdy signal value
24	RO	0x0	debug_filter_req dfbu_req_e signal value
23	RO	0x0	debug_referreq0 prbu_referreq0 signal value
22	RO	0x0	debug_referreq1 prbu_referreq1 signal value
21	RO	0x0	reserved
20:0	RO	0x000000	debug_dec_mb_count HW internal MB counter value

VDPU_SWREG59
Address: Operational Base + offset (0x00ec)
H264 Chrominance 8 pixel interleaved data base

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dec_ch8pix_base Base address for additional chrominance data format where chrominance is interleaved in group of 8 pixels. The usage is enabled by sw_ch_8pix_ileav_e [note]:the h264 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG60
Address: Operational Base + offset (0x00f0)
Interrupt register post-processor

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	sw_pp_bus_int Interrupt status bit bus. Error response from bus. In pipeline mode this bit is not used
12	RW	0x0	sw_pp_rdy_int Interrupt status bit pp. When this bit is high post processor has processed a picture in external mode. In pipeline mode this bit is not used.
11:9	RO	0x0	reserved
8	RW	0x0	sw_pp_irq Post-processor IRQ. SW will reset this after interrupt is handled. HINTpp is not used for pp if IRQ disable pp is high (sw_pp_irq_n_e = 1). In pipeline mode this bit is not used
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	sw_pp_irq_dis Post-processor IRQ disable. When high, there are no interrupts from HW concerning post processing. Polling must be used to see the interrupt
3:2	RO	0x0	reserved
1	RW	0x0	sw_pp_pipeline_e Decoder –post-processing pipeline enable: 0 = Post-processing is processing different picture than decoder or is disabled 1 = Post-processing is performed in pipeline with decoder
0	RW	0x0	sw_pp_e External mode post-processing enable. This bit will start the post-processing operation. Not to be used if PP is in pipeline with decoder (sw_pp_pipeline_e = 1). HW will reset this when picture is post-processed.

VDPU_SWREG61
Address: Operational Base + offset (0x00f4)
Device configuration register post-processor

Bit	Attr	Reset Value	Description
31:24	RW	0x01	sw_pp_axi_rd_id Read ID used for AXI PP read services (if connected to AXI)
23:16	RW	0x01	sw_pp_axi_wr_id Write ID used for AXI PP write services (if connected to AXI)
15	RO	0x0	reserved
14	RW	0x0	sw_pp_scmd_dis AXI Single Command Multiple Data disable.
13	RW	0x0	sw_pp_in_a2_endsel Endian/swap select for Alpha blend input source 2: '0' = Use PP in endian/swap definitions (sw_pp_in_endian, sw_pp_in_swap) '1' = Use Ablend source 1 endian/swap definitions
12	RW	0x0	sw_pp_in_a1_swap32 Alpha blend source 1 input 32bit data swap (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled))
11	RW	0x0	sw_pp_in_a1_endian Alpha blend source 1 input data byte endian mode. 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order)

Bit	Attr	Reset Value	Description
10	RW	0x0	sw_pp_in_swap32_e PP input 32bit data swap (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled))
9	RW	0x0	sw_pp_data_disc_e PP data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally.
8	RW	0x1	sw_pp_clkgate_e PP dynamic clock gating enable: 1 = Clock is gated from PP structures that are not used 0 = Clock is running for all PP structures Note: Clock gating value can be changed only when PP is not enabled
7	RW	0x0	sw_pp_in_endian PP input picture byte endian mode. Used only if PP is in standalone mode. If PP is running pipelined with the decoder, this bit has no effect. 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order)
6	RW	0x0	sw_pp_out_endian PP output picture endian mode for YCbCr data or for any data if config value SW_PP_OEN_VERSION=1 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order) (NOTE: For SW_PP_OEN_VERSION=0 16 bit RGB data this bit works as pixel swapping bit. For 32 bit RGB this bit has no meaning)
5	RW	0x0	sw_pp_out_swap32_e PP output data word swap (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order (also little endian should be enabled))
4:0	RW	0x00	sw_pp_max_burst Maximum burst length for PP bus transactions. 1-16

VDPU_SWREG62

Address: Operational Base + offset (0x00f8)

Deinterlace control register

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_deint_e De-interlace enable. Input data is in interlaced format and deinterlacing needs to be performed
30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_deint_threshold Threshold value used in deinterlacing
15	RW	0x0	sw_deint_blend_e Blend enable for de-interlacing
14:0	RW	0x0000	sw_deint_edge_det Edge detect value used for deinterlacing

VDPU_SWREG63
Address: Operational Base + offset (0x00fc)
base address for reading post-processing input picture uminan

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_in_lu_base Base address for post-processing input luminance picture. If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only.
1:0	RO	0x0	reserved

VDPU_SWREG64
Address: Operational Base + offset (0x0100)
Base address for reading post-processing input picture Cb/Ch

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_in_cb_base Base address for post-processing input Cb picture or for both chrominance pictures (if chrominances interleaved). If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only
1:0	RO	0x0	reserved

VDPU_SWREG65
Address: Operational Base + offset (0x0104)
Base address for reading post-processing input picture Cr

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_in_cr_base Base address for post-processing input cr picture. Used in external mode only
1:0	RO	0x0	reserved

VDPU_SWREG66
Address: Operational Base + offset (0x0108)
Base address for writing post-processed picture luminance/RGB

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_pp_out_lu_base Base address for post-processing output picture (luminance/YUYV/RGB).

VDPU_SWREG67
Address: Operational Base + offset (0x010c)
Base address for writing post-processed picture Ch

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_pp_out_ch_base Base address for post-processing output chrominance picture (interleaved chrominance).

VDPU_SWREG68
Address: Operational Base + offset (0x0110)
Register for contrast adjusting

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_contrast_thr1 Threshold value 1, used with contrast adjusting
23:20	RO	0x0	reserved
19:10	RW	0x000	sw_contrast_off2 Offset value 2, used with contrast adjusting
9:0	RW	0x000	sw_contrast_off1 Offset value 1, used with contrast adjusting

VDPU_SWREG69
Address: Operational Base + offset (0x0114)
Register for colour conversion and contrast adjusting

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_pp_in_start_ch For YUYV 422 input format. Enable for start_with_chrominance. '0' = the order is Y0CbY0Cr or Y0CrY0Cb '1' = the order is CbY0CrY0 or CrY0CbY0
30	RW	0x0	sw_pp_in_cr_first For YUYV 422 input format and YCbCr 420 semiplanar format. Enable for Cr first (before Cb) '0' = the order is Y0CbY0Cr or CbY0CrY0 (if 420 semiplanar chrominance: CbCrCbCr) '1' = the order is Y0CrY0Cb or CrY0CbY0 (if 420 semiplanar chrominance: CrCbCrCb)
29	RW	0x0	sw_pp_out_start_ch For YUYV 422 output format. Enable for start_with_chrominance. '0' = the order is Y0CbY0Cr or Y0CrY0Cb '1' = the order is CbY0CrY0 or CrY0CbY0
28	RW	0x0	sw_pp_out_cr_first For YUYV 422 output format. Enable for Cr first (beforeCb) '0' = the order is Y0CbY0Cr or CbY0CrY0 '1' = the order is Y0CrY0Cb or CrY0CbY0
27:18	RW	0x000	sw_color_coeffa2 Coefficient a2, used with Y pixel to calculate all color components

Bit	Attr	Reset Value	Description
17:8	RW	0x000	sw_color_coeffa1 Coefficient a1, used with Y pixel to calculate all color components
7:0	RW	0x00	sw_contrast_thr2 Threshold value 2, used with contrast adjusting

VDPU_SWREG70
Address: Operational Base + offset (0x0118)
Register for colour conversion 0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_color_coeffd Coefficient d, used with Cb to calculate green component value
19:10	RW	0x000	sw_color_coeffc Coefficient c, used with Cr to calculate green component value
9:0	RW	0x000	sw_color_coeffb Coefficient b, used with Cr to calculate red component value

VDPU_SWREG71
Address: Operational Base + offset (0x011c)
Register for colour conversion 1 + rotation mode

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:21	RW	0x000	sw_crop_startx Start coordinate x for the cropped area in macroblocks.
20:18	RW	0x0	sw_rotation_mode Rotation mode: 000 = rotation disabled 001 = rotate + 90 010 = rotate –90 011 = horizontal flip (mirror) 100 = vertical flip 101 = rotate 180
17:10	RW	0x00	sw_color_coefff Coefficient f, used with Y to adjust brightness
9:0	RW	0x000	sw_color_coeffe Coefficient e, used with Cb to calculate blue component value

VDPU_SWREG72
Address: Operational Base + offset (0x0120)
PP input size and -cropping register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_crop_starty Start coordinate y for the cropped area in macroblocks.
23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:18	RW	0x00	sw_rangemap_coef_y Range map value for Y component (RANGE_MAPY+9 in VC-1 standard)
17	RO	0x0	reserved
16:9	RW	0x00	sw_pp_in_height PP input picture height in MBs. Can be cropped from a bigger input picture in external mode
8:0	RW	0x000	sw_pp_in_width PP input picture width in MBs. Can be cropped from a bigger input picture in external mode

VDPU_SWREG73
Address: Operational Base + offset (0x0124)
PP input picture base address for Y bottom field

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_bot_yin_base PP input Y base for bottom field
1:0	RO	0x0	reserved

VDPU_SWREG74
Address: Operational Base + offset (0x0128)
PP input picture base for Ch bottom field

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_bot_cin_base PP input C base for bottom field (mixed chrominance)
1:0	RO	0x0	reserved

VDPU_SWREG79
Address: Operational Base + offset (0x013c)
Scaling ratio register 1 & padding for B

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rangemap_y_e Range map enable for Y component (RANGE_MAPY_FLAG in VC-1 standard). For VC1 main profile this bit is used as range expansion enable
30	RW	0x0	sw_rangemap_c_e Range map enable for chrominance component RANGE_MAPUV_FLAG in VC-1 standard)
29	RW	0x0	sw_ycbcr_range Defines the YCbCr range in RGB conversion: 0 = 16 --> 235 for Y,16 --> 240 for Chrominance 1 = 0 --> 255 for all components

Bit	Attr	Reset Value	Description
28	RW	0x0	sw_rgb_pix_in32 RGB pixel amount/ 32 bit word 0 = 1 RGB pixel/32 bit 1 = 2 RGB pixels/32 bit
27:23	RW	0x00	sw_rgb_r_padd Amount of ones that will be padded in front of the R-component
22:18	RW	0x00	sw_rgb_g_padd Amount of ones that will be padded in front of the G-component
17:0	RW	0x00000	sw_scale_wratio Scaling ratio for width (outputw-1/inputw-1)

VDPU_SWREG80
Address: Operational Base + offset (0x0140)
Scaling register 0 ratio & padding for R and G

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_pp_fast_scale_e 0 = fast downscaling is not enabled 1 = fast downscaling is enabled. The quality of the picture is decreased but performance is improved
29:27	RW	0x0	sw_pp_in_struct PP input data picture structure: 0 = Top field / progressive frame structure: Read input data from top field base address /frame base address and read every line 1 = Bottom field structure: Read input data from bottom field base address and read every line. 2 = Interlaced field structure: Read input data from both top and bottom field base address and take every line from each field. 3 = Interlaced frame structure: Read input data from both top and bottom field base address and take every second line from each field. 4 = Ripped top field structure: Read input data from top field base address and read every second line. 5 = Ripped bottom field structure: Read input data from bottom field base address and read every second line
26:25	RW	0x0	sw_hor_scale_mode Horizontal scaling mode: 00 = Off 01 = Upscale 10 = Downscale

Bit	Attr	Reset Value	Description
24:23	RW	0x0	sw_ver_scale_mode Vertical scaling mode: 00 = Off 01 = Upscale 10 = Downscale
22:18	RW	0x00	sw_rgb_b_padd Amount of ones that will be padded in front of the B-component
17:0	RW	0x00000	sw_scale_hratio Scaling ratio for height (outputh-1/inputh-1)

VDPU_SWREG81
Address: Operational Base + offset (0x0144)
Scaling ratio register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_wscale_invra Inverse scaling ratio for width, or ch (inputw-1 / outputw-1)
15:0	RW	0x0000	sw_hscale_invra Inverse scaling ratio for height or cv (inputh-1 / outputh-1)

VDPU_SWREG82
Address: Operational Base + offset (0x0148)
Rmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_r_mask Bit mask for R component (and alpha channel)

VDPU_SWREG83
Address: Operational Base + offset (0x014c)
Gmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_g_mask Bit mask for G component (and alpha channel)

VDPU_SWREG84
Address: Operational Base + offset (0x0150)
Bmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_b_mask Bit mask for B component (and alpha channel)

VDPU_SWREG85
Address: Operational Base + offset (0x0154)
Post-processor control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:29	RW	0x0	sw_pp_in_format PP input picture data format 0 = YUYV 4:2:2 interleaved (supported only in external mode) 1 = YCbCr 4:2:0 Semi-planar in linear raster-scan format 2 = YCbCr 4:2:0 planar (supported only in external mode) 3 = YCbCr 4:0:0 (supported only in pipelined mode) 4 = YCbCr 4:2:2 Semi-planar (supported only in pipelined mode) 5 = YCbCr 4:2:0 Semi-planar in tiled format (supported only in external mode (8170 decoder only) 6 = YCbCr 4:4:0 Semi-planar (supported only in pipelined mode, possible for jpeg only) 7 = Escape pp input data format. Defined in swreg86
28:26	RW	0x0	sw_pp_out_format PP output picture data format: 0 = RGB 1 = YCbCr 4:2:0 planar (Not supported) 2 = YCbCr 4:2:2 planar (Not supported) 3 = YUYV 4:2:2 interleaved 4 = YCbCr 4:4:4 planar (Not supported) 5 = YCh 4:2:0 chrominance interleaved 6 = YCh 4:2:2 (Not supported) 7 = YCh 4:4:4 (Not supported)
25:15	RW	0x000	sw_pp_out_height Scaled picture height in pixels (Must be dividable by 2 or by any if Pixel Accurate PP output configuration is enabled) Max scaled picture height is 1920 pixels or maximum three times the input source height minus 8 pixels
14:4	RW	0x000	sw_pp_out_width Scaled picture width in pixels. Must be dividable by 8 or by any if Pixel Accurate PP output configuration is enabled. Max scaled picture width is 1920 pixels or maximum three times the input source width minus 8 pixels
3	RW	0x0	sw_pp_out_tiled_e Tiled mode enable for PP output. Can be used only for YCbYCr 422 output format. Can be used only if correpongind configuration supports this feature. Tile size is 4x4 pixels.
2	RW	0x0	sw_pp_out_swap16_e PP output swap 16 swaps 16 bit halfs inside of 32 bit word. Can be used for 16 bit RGB to change pixel orders but is valid also for any output format NOTE: requires that configuration of SW_PPD_OEN_VERSION=1

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_pp_crop8_r_e PP input picture width is not 16 pixels multiple. Only 8 pixels of the most right MB of the unrotated input picture is used for PP input.
0	RW	0x0	sw_pp_crop8_d_e PP input picture height is not 16 pixels multiple. Only 8 pixel rows of the most down MB of the unrotated input picture is used for PP input.

VDPU_SWREG86
Address: Operational Base + offset (0x0158)
Mask 1 start coordinate register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	sw_pp_in_format_es Escape PP in format. Used if sw_pp_in_format is defined to 7: 0 0 = YCbCr 4:4:4 1 = YCbCr 4:1:1
28	RO	0x0	reserved
27:23	RW	0x00	sw_rangemap_coef_c Range map value for chrominance component (RANGE_MAPUV+9 in VC-1 standard)
22	RW	0x0	sw_mask1_ablend_e Mask 1 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 1 base address. Alpha blending can be enabled only for RGB/ YUYV 422 data.
21:11	RW	0x000	sw_mask1_starty Vertical start pixel for mask area 1. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions
10:0	RW	0x000	sw_mask1_startix Horizontal start pixel for mask area 1. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions

VDPU_SWREG87
Address: Operational Base + offset (0x015c)
Mask 2 start coordinate register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_mask2_ablend_e Mask 2 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 2 base address. Alpha blending can be enabled only for RGB/YUYV 422 data.

Bit	Attr	Reset Value	Description
21:11	RW	0x000	sw_mask_starty Verical start pixel for mask area 2. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP ouput Y picture. See Table 47 for restrictions
10:0	RW	0x000	sw_mask2_startx Horizontal start pixel for mask area 2. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output Y picture. See Table 47 for restrictions

VDPU_SWREG88
Address: Operational Base + offset (0x0160)
Mask 1 size and PP original width register

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_ext_orig_width PP input picture original width in macro blocks.
22	RW	0x0	sw_mask1_e Mask 1 enable. If mask 1 is used this bit is high
21:11	RW	0x000	sw_mask1_endy Mask 1 end coordinate y in pixels (inside of PPD output picture). Range must be between [Mask1StartCoordinateY, ScaledHeight].
10:0	RW	0x000	sw_mask1_endx Mask 1 end coordinate x in pixels (inside of PPD output picture). Range must be between [Mask1StartCoordinateX, ScaledWidth]

VDPU_SWREG89
Address: Operational Base + offset (0x0164)
Mask 2 size register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_mask2_e Mask 2 enable. If mask 1 is used this bit is high
21:11	RW	0x000	sw_mask2_endy Mask 2 end coordinate y in pixels (inside of PP output picture). Range must be between [Mask2StartCoordinateY, ScaledHeight].
10:0	RW	0x000	sw_mask2_endx Mask 2 end coordinate x in pixels (inside of PP output picture). Range must be between [Mask2StartCoordinateX, ScaledWidth].

VDPU_SWREG90
Address: Operational Base + offset (0x0168)
PiP register 0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_right_cross_e Right side overcross enable. 0 = No right side overcross, 1 = right side overcross
28	RW	0x0	sw_left_cross_e Left side overcross enable. 0 = No left side overcross, 1 = left side overcross
27	RW	0x0	sw_up_cross_e Upward overcross enable. 0 = No upward overcross, 1 = upward overcross
26	RW	0x0	sw_down_cross_e Downward overcross enable. 0 = No downward overcross, 1 = downward overcross
25:15	RW	0x000	sw_up_cross Amount of upward overcross (vertical pixels outside of display from the upper side). Range must be between [0, ScaledHeight].
14:11	RO	0x0	reserved
10:0	RW	0x000	sw_down_cross Amount of downward overcross (vertical pixels outside of displayfrom the down side). Range must be between [0, ScaledHeight].

VDPU_SWREG91
Address: Operational Base + offset (0x016c)
PiP register 1 and dithering control

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_dither_select_r Dithering control for R channel: 00 = dithering disabled 01 = use four-bit dither matrix 10 = use five-bit dither matrix 11 = use six-bit dither matrix
29:28	RW	0x0	sw_dither_select_g Dithering control for G channel: 00 = dithering disabled 01 = use four-bit dither matrix 10 = use five-bit dither matrix 11 = use six-bit dither matrix
27:26	RW	0x0	sw_dither_select_b Dithering control for B channel: 00 = dithering disabled 01 = use four-bit dither matrix 10 = use five-bit dither matrix 11 = use six-bit dither matrix

Bit	Attr	Reset Value	Description
25:24	RO	0x0	reserved
23:22	RW	0x0	sw_pp_tiled_mode Input data is in tiled mode (at the moment valid only for YCbCr 420 data, pipeline or external mode): 0 = Tiled mode not used 1 = Tiled mode enabled for 8x4 sized tiles 2,3 = reserved
21:11	RW	0x000	sw_right_cross Amount of right side overcross (Horizontal pixels outside o display from the right side). Range must be between [0, ScaledWidth].
10:0	RW	0x000	sw_left_cross Amount of left side overcross (Horizontal pixels outside of display from the left side). Range must be between [0, ScaledWidth].

VDPU_SWREG92
Address: Operational Base + offset (0x0170)
Display width and PP input size extension register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	sw_pp_in_h_ext Extended PP input height. Used with JPEG
28:26	RW	0x0	sw_pp_in_w_ext Extended PP input width. Used with JPEG
25:23	RW	0x0	sw_crop_starty_ext Extended PP input crop start coordinate x. Used with JPEG
22:20	RW	0x0	sw_crop_start_ext Extended PP input crop start coordinate y. Used with JPEG
19:12	RO	0x0	reserved
11:0	RW	0x000	sw_display_width Width of the display in pixels. Max HDTV (1920)

VDPU_SWREG93
Address: Operational Base + offset (0x0174)
Display width and PP input size extension register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_abledn1_base Base address for alpha blending input 1 (if mask1 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 1 size or with ablend1_scanline if ablend cropping is supported in configuration.

VDPU_SWREG94
Address: Operational Base + offset (0x0178)
Base address for alpha blend 2 gui component

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ablend2_base Base address for alpha blending input 2 (if mask2 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 2 size or with ablend2_scanline if ablend cropping is supported in configuration.

VDPU_SWREG95
Address: Operational Base + offset (0x017c)
Base address for alpha blend 2 gui component

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:13	RW	0x0000	sw_ablend2_scan Scanline width in pixels for Ablend 2. Usage enabled if corresponding configuration bit is enabled
12:0	RW	0x0000	sw_ablend1_scan Scanline width in pixels for Ablend 1. Usage enabled if corresponding configuration bit is enabled

VDPU_SWREG98
Address: Operational Base + offset (0x0188)
PP outupt width/height extension

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	sw_pp_out_h_ext sw_pp_out_h_ext PP output heightextension
0	RW	0x0	sw_pp_out_w_ext sw_pp_out_w_ext PP output widthextension

VDPU_SWREG99
Address: Operational Base + offset (0x018c)
PP fuse register (read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	fuse_pp_pp 1 = PP enabled
30	RO	0x1	fuse_pp_deint 1 = Deinterlacing enabled
29	RO	0x1	fuse_pp_ablend 1 = Alpha Blending enabled
28:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15	RO	0x1	fuse_pp_maxw_1920 1 = Max PP output width up to 1920 pixels enabled. Priority coded with priority 1
14	RO	0x1	fuse_pp_maxw_1280 1 = Max PP output width up to 1280 pixels enabled. Priority coded with priority 2
13	RO	0x1	fuse_pp_maxw_720 1 = Max PP output width up to 720 pixels enabled. Priority coded with priority 3
12	RO	0x1	fuse_pp_maxw_352 1 = Max PP output width up to 352 pixels enabled. Priority coded with priority 4
11:0	RO	0x0	reserved

VDPU_SWREG100

Address: Operational Base + offset (0x0190)

Synthesis configuration register post-processor (read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	SW_ABLEND_CROP_E Alpha blending support for input cropping: '0' : Not supported. External memory must include the exact image of the area being alpha blended '1' : Supported. External memory can include a picture from blended area can be cropped. Requires usage of swreg95
30	RO	0x1	SW_PPD_PIXAC_E Pixel Accurate PP output mode exists: '0' = PIP, Scaling and masks can be adjusted by steps of 8 pixels (width) or 2 pixels (height) '1' = PIP, Scaling and masks can be adjusted by steps of 1 pixel for RGB and 2 pixels for subsampled chroma formats (by using bus specific write strobe functionality)
29	RO	0x1	SW_PPD_TILED_EXIST PP output YCbYCr 422 tiled support (4x4 pixel tiles) '0' = Not supported '1' = Supported
28	RO	0x1	SW_PPD_DITH_EXIST Dithering exists: '0' = no '1' = yes
27:26	RO	0x3	SW_PPD_SCALE_LEVEL Scaling support: 00 = No scaling 01 = Scaling with lo perfomance architecture 10 = Scaling with high performance architecture 11 = Scaling with high performance architecture + fast

Bit	Attr	Reset Value	Description
25	RO	0x1	SW_PPD_DEINT_EXIST De-interlacing exits: '0' = no '1' = yes
24	RO	0x1	SW_PPD_BLEND_EXIST Alpha blending exists: '0' = no '1' = yes
23	RO	0x1	SW_PPD_IBUFF_LEVEL PP input buffering level: '0' = 1 MB input buffering is used '1' = 4 MB input buffering is used
22:19	RO	0x0	reserved
18	RO	0x1	SW_PPD_OEN_VERSION PP output endian version: '0' = Endian mode supported for other than RGB '1' = Endian mode supported for any output format
17	RO	0x1	SW_PPD_OBUFF_LEVEL PP output buffering level: '0' = 1 unit output buffering is used '1' = 4 unit output buffering is used
16	RO	0x1	SW_PPD_PP_EXIST PPD exists: '0' = no '1' = yes
15:14	RO	0x1	SW_PPD_IN_TILED_L PPD input tiled mode support level 0 = not supported 1 = 8x4 tile size supported
13:11	RO	0x0	reserved
10:0	RO	0x780	SW_PPD_MAX_OWIDTH Max supported PP output width in pixels

VDPU_SWREG101
Address: Operational Base + offset (0x0194)
soft reset signals

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_soft_reset softreset pulse signal softreset pulse signal write to 1'b1, valid; write to 1'b0, invalid;

VDPU_SWREG102

Address: Operational Base + offset (0x0198)
vpu performance cycle

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vpu_work_cycle vpu working cycle number write initial/reset value in the begin of frame start,then will auto count base this value.

VDPU_SWREG103
Address: Operational Base + offset (0x019c)
AXI DDR READ DATA NUM

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_rdata axi ddr rdata num axi ddr rdata num, the unit is byte

VDPU_SWREG104
Address: Operational Base + offset (0x01a0)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_axi_ddr_wdata vdpu write data byte num vdpu write data byte num

VDPU_SWREG105
Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	mon_sig_sel1 monitor signal sellected for cnt1 select the counter be used for which to calculate cycle num 4'b0000: don't work 4'b0001:mv buffer hold back stream decode working cycles 4'b0010:the output fifo of cabac keep full cycles 4'b0011:the Code stream parsing block working cycles 4'b0100:scd block can't write data to scd buffer cycles 4'b0101:The speed of reconsitution and interpolation fast than reference frames feach cycles 4'b0110:The speed of reconsitution and interpolation slow than reference frames feach cycles 4'b0111:the cycles filter block hold back pred block 4'b1000:the cycles of pred block waiting for Residual data 4'b1001:the cycles of bus Related modules working
15:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	mon_sig_sel0 monitor signal sellected for cnt0 select the counter be used for which to calculate cycle num 4'b0000: don't work 4'b0001:mv buffer hold back stream decode working cycles 4'b0010:the output fifo of cabac keep full cycles 4'b0011:the Code stream parsing block working cycles 4'b0100:scd block can't write data to scd buffer cycles 4'b0101:The speed of reconsitution and interpolation fast than reference frames feach cycles 4'b0110:The speed of reconsitution and interpolation slow than reference frames feach cycles 4'b0111:the cycles filter block hold back pred block 4'b1000:the cycles of pred block waiting for Residual data 4'b1001:the cycles of bus Related modules working

VDPU_SWREG106
Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	performance_mon_cnt0 the counter for the secected signal valid cycles whic describe in swreg105[3:0] write initial/reset value

VDPU_SWREG107
Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	performance_mon_cnt1 Field0000 Abstract the counter for the secected signal valid cycles whic describe in swreg105[19:16] write initial/reset value

VCODEC_MMU_DTE_ADDR
Address: Operational Base + offset (0x0000)
MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU_DTE_ADDR MMU current page Table address

VCODEC_MMU_STATUS
Address: Operational Base + offset (0x0004)
MMU status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID page fault bus id Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE page fault acess The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY replay buffer empty status 1'b1:The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE mmu idle status The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE stall active status MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE page fault active status MMU page fault mode currently enabled . The mode is enabled by command. 1'b1: page fault is active
0	RO	0x0	PAGING_ENABLED Paging enabled status 1'b0: paging is disabled 1'b1: Paging is enabled

VCODEC_MMU_COMMAND
Address: Operational Base + offset (0x0008)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	WO	0x0	MMU_CMD mmu cmd MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

VCODEC_MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x000c)
MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR page fault addr address of last page fault

VCODEC_MMU_ZAP_ONE_LINE
Address: Operational Base + offset (0x0010)
MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE zap one line address to be invalidated from the page table cache

VCODEC_MMU_INT_RAWSTAT
Address: Operational Base + offset (0x0014)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error read bus error status
0	RW	0x0	PAGE_FAULT page fault page fault status

VCODEC_MMU_INT_CLEAR
Address: Operational Base + offset (0x0018)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	WO	0x0	READ_BUS_ERROR read bus error write 1 to clear read bus error
0	WO	0x0	PAGE_FAULT page fault clear write 1 to page fault clear

VCODEC_MMU_INT_MASK
Address: Operational Base + offset (0x001c)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error enable the read bus interrupt souce when this bit is set to 1'b1
0	RW	0x0	PAGE_FAULT page fault mask enable the page fault interrupt souce when this bit is set to 1'b1

VCODEC_MMU_INT_STATUS
Address: Operational Base + offset (0x0020)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error status 1'b1:read bus error status
0	RO	0x0	PAGE_FAULT page fault status 1'b1:page fault

VCODEC_MMU_AUTO_GATING
Address: Operational Base + offset (0x0024)
mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_clkgating mmu_auto_clkgating when it is 1'b1, the mmu will auto gating it self

pref_cache_VERSION
Address: Operational Base + offset (0x0000)
VERSION register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID Field0000 Abstract Field0000 Description
15:8	RO	0x01	VERSION_MAJOR Field0000 Abstract Field0000 Description
7:0	RO	0x01	VERSION_MINOR Field0000 Abstract Field0000 Description

pref_cache_SIZE
Address: Operational Base + offset (0x0004)
L2 cache SIZE

Bit	Attr	Reset Value	Description
31:24	RO	0x06	External_bus_width Field0000 Abstract Log2 external bus width in bits
23:16	RO	0x11	CACHE_SIZE Field0000 Abstract Log2 cache size in bytes
15:8	RO	0x02	ASSOCIATIVITY Field0000 Abstract Log2 associativity
7:0	RO	0x06	LINE_SIZE Field0000 Abstract Log2 line size in bytes

pref_cache_STATUS
Address: Operational Base + offset (0x0008)
Status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	DATA_BUSY Field0000 Abstract set when the cache is busy handling data
0	RO	0x0	CMD_BUSY Field0000 Abstract set when the cache is busy handling commands

pref_cache_COMMAND
Address: Operational Base + offset (0x0010)
Command setting register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	sw_addrb_sel Field0000 Abstract 2'b00:to sel b[14:6] 2'b01:to sel b[15:9], b[7:6] 2'b10:to sel b[16:10], b[7:6] 2'b11:to sel b[17:11], b[7:6]
3	RO	0x0	reserved
2:0	WO	0x0	COMMAND Field0000 Abstract The possible command is 1 = Clear entire cache

pref_cache_CLEAR_PAGE
Address: Operational Base + offset (0x0014)
clear page register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE Field0000 Abstract writing an address, invlidates all lines in that page from the cache

pref_cache_MAX_READS
Address: Operational Base + offset (0x0018)
maximum read register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x1c	MAX_READS Field0000 Abstract Limit the number of outstanding read transactions to this amount

pref_cache_PERFCNT_SRC0
Address: Operational Base + offset (0x0020)
performance counter 0 source register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	PERFCNT_SRC0 Field0000 Abstract This register holds all the possible source values for Performance Counter 0 0: total clock cycles 1: active clock cycles 2: read transactions, master 3: word reads, master 4: read transactions, slave 5: word reads, slave 6: read hit, slave 7: read misses, slave 8: read invalidates, slave 9: cacheable read transactions, slave 10: bad hit nmber, slave

pref_cache_PERFCNT_VAL0
Address: Operational Base + offset (0x0024)
performance counter 0 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Field0000 Abstract Performance counter 0 value

pref_cache_PERFCNT_SRC1
Address: Operational Base + offset (0x0028)
performance counter 0 source register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	PERFCNT_SRC1 Field0000 Abstract This register holds all the possible source values for Performance Counter 1 0: total clock cycles 1: active clock cycles 2: read transactions, master 3: word reads, master 4: read transactions, slave 5: word reads, slave 6: read hit, slave 7: read misses, slave 8: read invalidates, slave 9: cacheable read transactions, slave 10: bad hit nmber, slave

pref_cache_PERFCNT_VAL1
Address: Operational Base + offset (0x002c)
performance counter 1 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Field0000 Abstract Performance counter 1 value

3.4.6 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
mmu_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address
mmu_STATUS	0x0004	W	0x00000018	MMU status register
mmu_COMMAND	0x0008	W	0x00000000	MMU command register
mmu_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
mmu_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
mmu_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
mmu_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
mmu_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
mmu_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
mmu_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.4.7 MMU Detail Register Description

mmu_DTE_ADDR
Address: Operational Base + offset (0x0000)
MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR mmu dte base addr mmu dte base addr , the address must be 4kb aligned

mmu_STATUS
Address: Operational Base + offset (0x0004)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID page fault bus id Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE page fault acess The direction of access for last page fault: 0 = Read 1 = Write

Bit	Attr	Reset Value	Description
4	RO	0x1	REPLAY_BUFFER_EMPTY replay buffer empty status 1'b1:The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE mmu idle status The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE stall active status MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE page fault active status MMU page fault mode currently enabled . The mode is enabled by command. 1'b1: page fault is active
0	RO	0x0	PAGING_ENABLED Paging enabled status 1'b0: paging is disabled 1'b1: Paging is enabled

mmu_COMMAND
Address: Operational Base + offset (0x0008)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD Field0000 Abstract MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

mmu_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x000c)
MMU logical address of last page fault

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Field0000 Abstract address of last page fault

mmu_ZAP_ONE_LINE
Address: Operational Base + offset (0x0010)
MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Field0000 Abstract address to be invalidated from the page table cache

mmu_INT_RAWSTAT
Address: Operational Base + offset (0x0014)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RW	0x0	PAGE_FAULT Field0000 Abstract page fault

mmu_INT_CLEAR
Address: Operational Base + offset (0x0018)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	WO	0x0	PAGE_FAULT Field0000 Abstract page fault

mmu_INT_MASK
Address: Operational Base + offset (0x001c)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT Field0000 Abstract page fault enable an interrupt source if the corresponding mask bit is set to 1

mmu_INT_STATUS
Address: Operational Base + offset (0x0020)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RO	0x0	PAGE_FAULT Field0000 Abstract page fault

mmu_AUTO_GATING
Address: Operational Base + offset (0x0024)
mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating mmu auto gating when it is 1'b1, the mmu will auto gating it self

3.4.8 PREF CACHE Registers Summary

Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x0000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x0004	W	0x07110206	L2 cache SIZE
pref_cache_STATUS	0x0008	W	0x00000000	Status register
pref_cache_COMMAND	0x0010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x0014	W	0x00000000	clear page register
pref_cache_MAX_READS	0x0018	W	0x0000001c	maximum read register
pref_cache_ENABLE	0x001c	W	0x00000003	enables cacheable accesses and cache read allocation
pref_cache_PERFCNT_SRC0	0x0020	W	0x00000000	performance counter 0 source register

Name	Offset	Size	Reset Value	Description
pref_cache_PERFCNT_VAL0	0x0024	W	0x00000000	performance counter 0 value register
pref_cache_PERFCNT_SRC1	0x0028	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL1	0x002c	W	0x00000000	performance counter 1 value register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.4.9 PREF CACHE Detail Register Description

pref_cache_VERSION
Address: Operational Base + offset (0x0000)
VERSION register

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID
15:8	RO	0x01	VERSION_MAJOR
7:0	RO	0x01	VERSION_MINOR

pref_cache_SIZE
Address: Operational Base + offset (0x0004)
L2 cache SIZE

Bit	Attr	Reset Value	Description
31:24	RO	0x07	External_bus_width Log2 external bus width in bits
23:16	RO	0x11	CACHE_SIZE Log2 cache size in bytes
15:8	RO	0x02	ASSOCIATIVITY Log2 associativity
7:0	RO	0x06	LINE_SIZE Log2 line size in bytes

pref_cache_STATUS
Address: Operational Base + offset (0x0008)
Status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	DATA_BUSY set when the cache is busy handling data
0	RW	0x0	CMD_BUSY set when the cache is busy handling commands

pref_cache_COMMAND
Address: Operational Base + offset (0x0010)
Command setting register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	COMMAND The possible command is 1 = Clear entire cache

pref_cache_CLEAR_PAGE
Address: Operational Base + offset (0x0014)
clear page register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE writing an address, invlidates all lines in that page from the cache

pref_cache_MAX_READS
Address: Operational Base + offset (0x0018)
maximum read register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x1c	MAX_READS Limit the number of outstanding read transactions to this amount

pref_cache_ENABLE
Address: Operational Base + offset (0x001c)
enables cacheable accesses and cache read allocation

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	sw_cache_clk_disgate cache clk disgate cache clk disgate when it is 1'b0, enable cache clk auto clkgating when it is 1'b1, disable cache clk auto clkgating
2	RW	0x0	sw_readbuffer_counter_reject_en counter reject enable default is 1'b0, for enhance cacheable read performnace in readbuffer. 1'b1: normal origin counter reject
1	RW	0x1	permit_cache_read_allocate cache read allocate 1'b1: permit cache read allocate
0	RW	0x1	permit_cacheable_access cacheable access 1'b1: permit cacheable access

pref_cache_PERFCNT_SRC0
Address: Operational Base + offset (0x0020)
performance counter 0 source register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	PERFCNT_SRC0 This register holds all the possible source values for Performance Counter 0 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

pref_cache_PERFCNT_VAL0
Address: Operational Base + offset (0x0024)
performance counter 0 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Performance counter 0 value

pref_cache_PERFCNT_SRC1
Address: Operational Base + offset (0x0028)
performance counter 0 source register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	PERFCNT_SRC1 This register holds all the possible source values for Performance Counter 1 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

pref_cache_PERFCNT_VAL1
Address: Operational Base + offset (0x002c)
performance counter 1 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Performance counter 1 value

3.5 Application Notes

3.5.1 HEVC Configuration Flow

1. Prepare the data in the DDR.
2. Set the HEVC general system configuration in HEVC.swreg2, such as working mode, in/out endian.
3. Set the picture parameters with HEVC.swreg3.
4. Set the input and output data base address and HEVC reference configuration with HEVC.swreg4~HEVC.swreg43.
5. If CABAC error detection is desired, set the HEVC.swreg44 to enable the corresponding error detection.
6. Set the interrupt configuration and start the HEVC with HEVC.swreg1.
7. Wait for the frame interrupt, and then get the processed results in the target DDR
8. Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

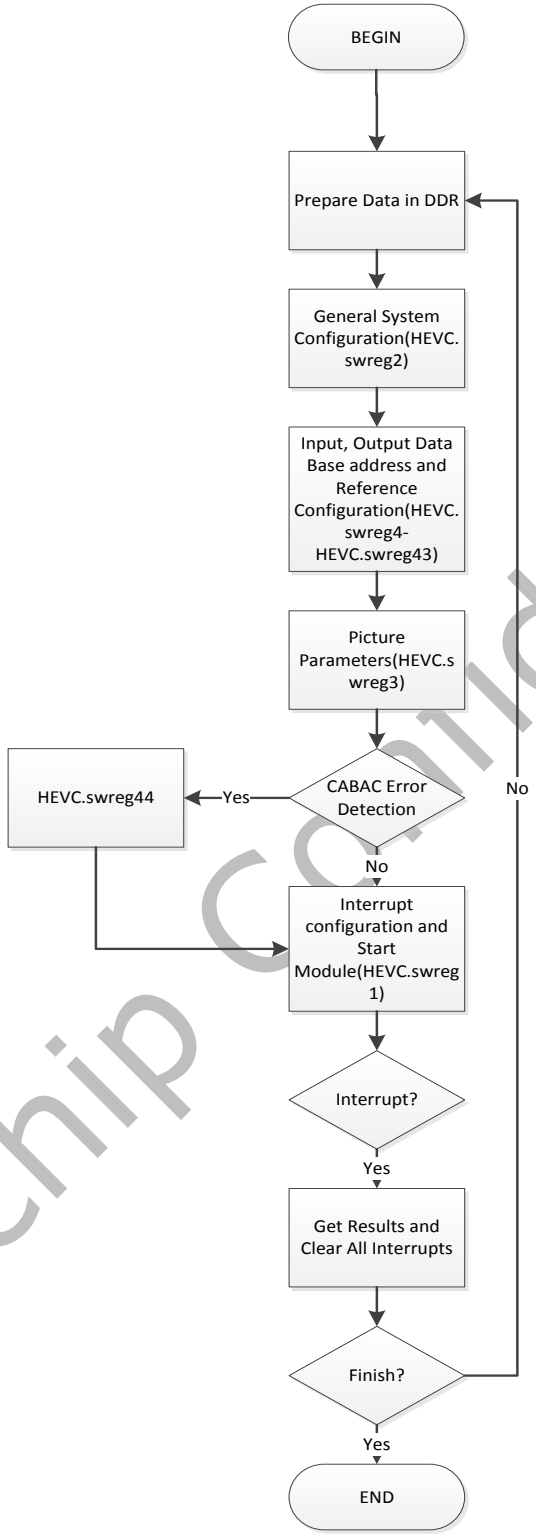


Fig. 3-5 HEVC Common Configuration Flow

3.5.2 H264 Configuration Flow

1. Prepare the decoder data in the DDR memory, And in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used. and please notice that which be list as follows:
The decoder can support ref buffer mode or cacheable mode, but they can't be both enabled. We can config the swreg57[6],swreg57[7] to enable cache and config the swreg51 to control

the ref buffer.
3. You should config VDPU_SWREG1[0] as 1’b1 to enable video decoder. And config VDPU_SWREG60[0] as 1’b1 to enable pp. If pp performed in pipeline with decoder, you should config VDPU_SWREG60[1] as 1’b1 and then config VDPU_SWREG1[0] as 1’b1 to enable decoder and pp.
4. Wait for the frame interrupt,and then check if the frame decoder ready interrupt is right or not, after that,you can get the processed results in the target DDR
5. Clear all the interrupts,repeat step 2~5 to start a new frame decoder .