

LAB 1: STUDYING LOGIC GATES AND VERIFYING THEIR TRUTH TABLES

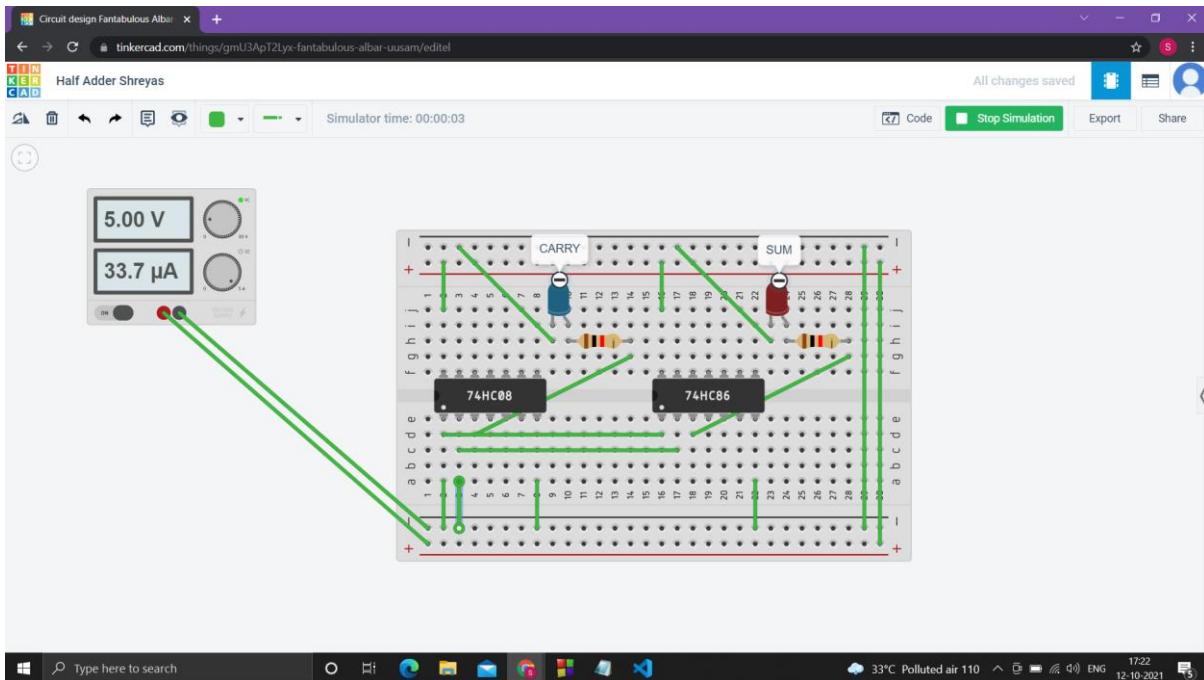
Name: Shreyas Sawant

Div: D7A

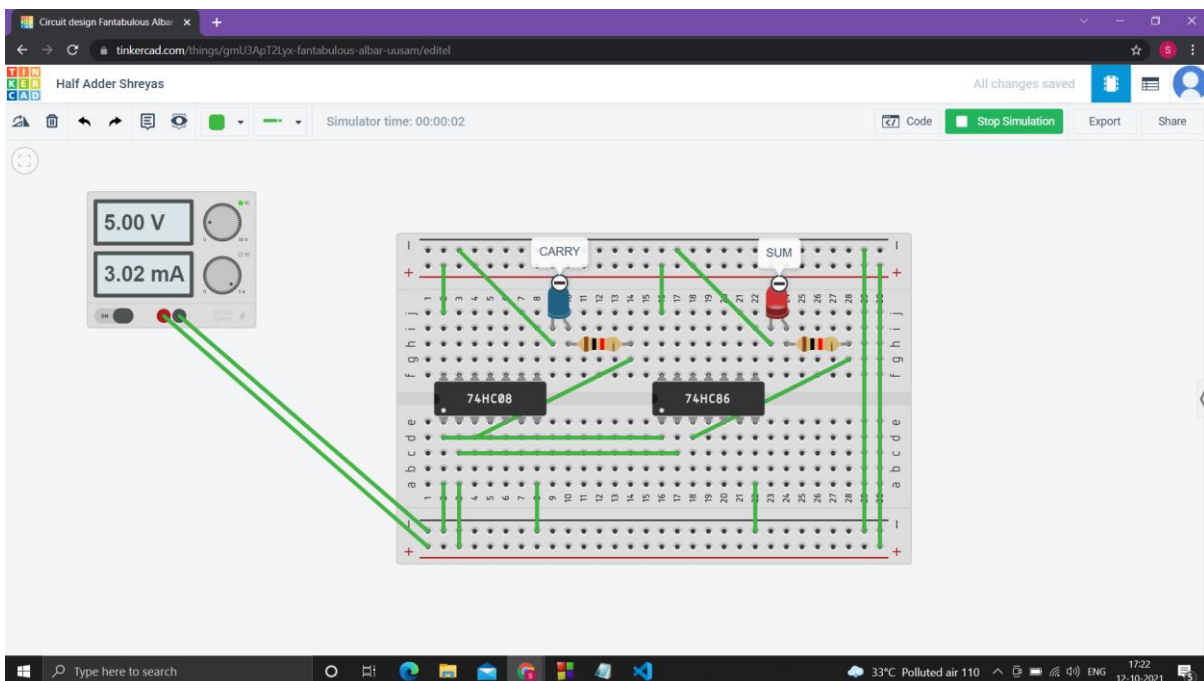
Roll No.: 55

1) Half Adder

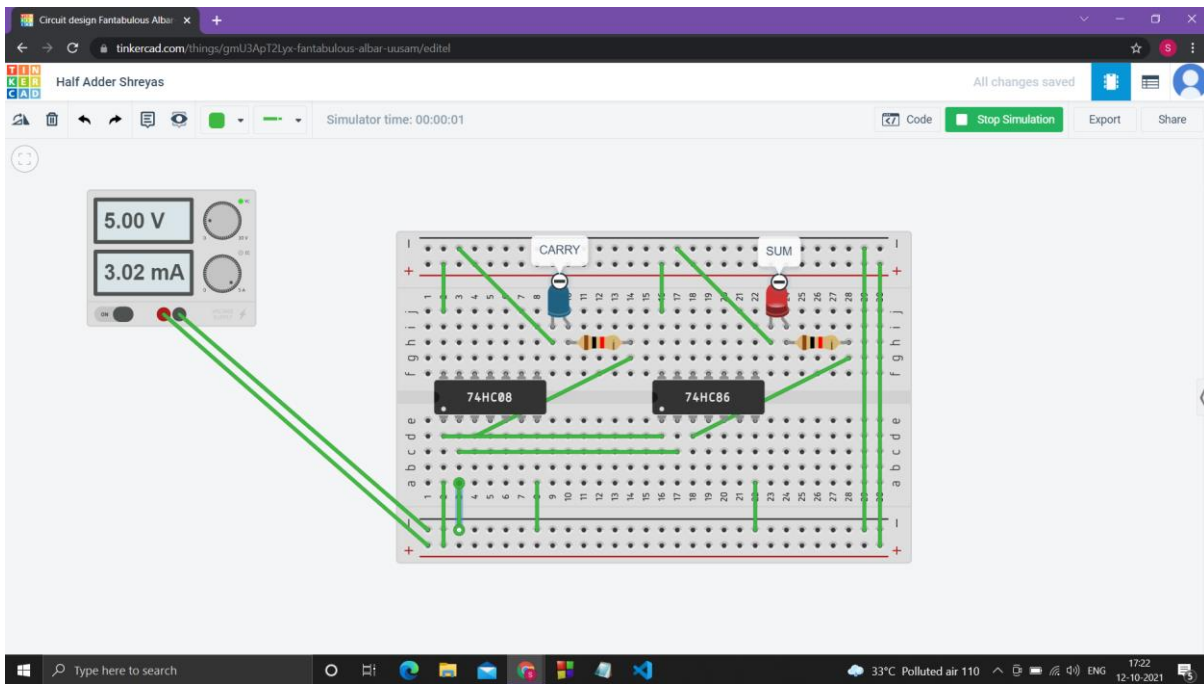
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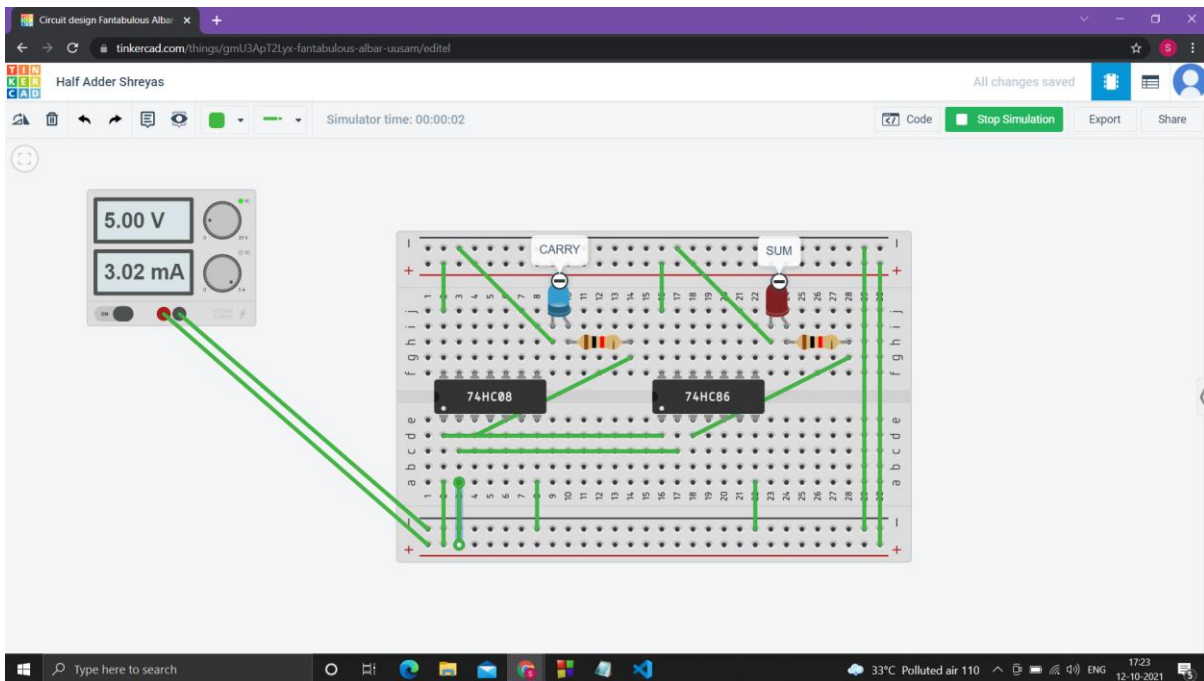
A=0 B=1



A=0 B=1

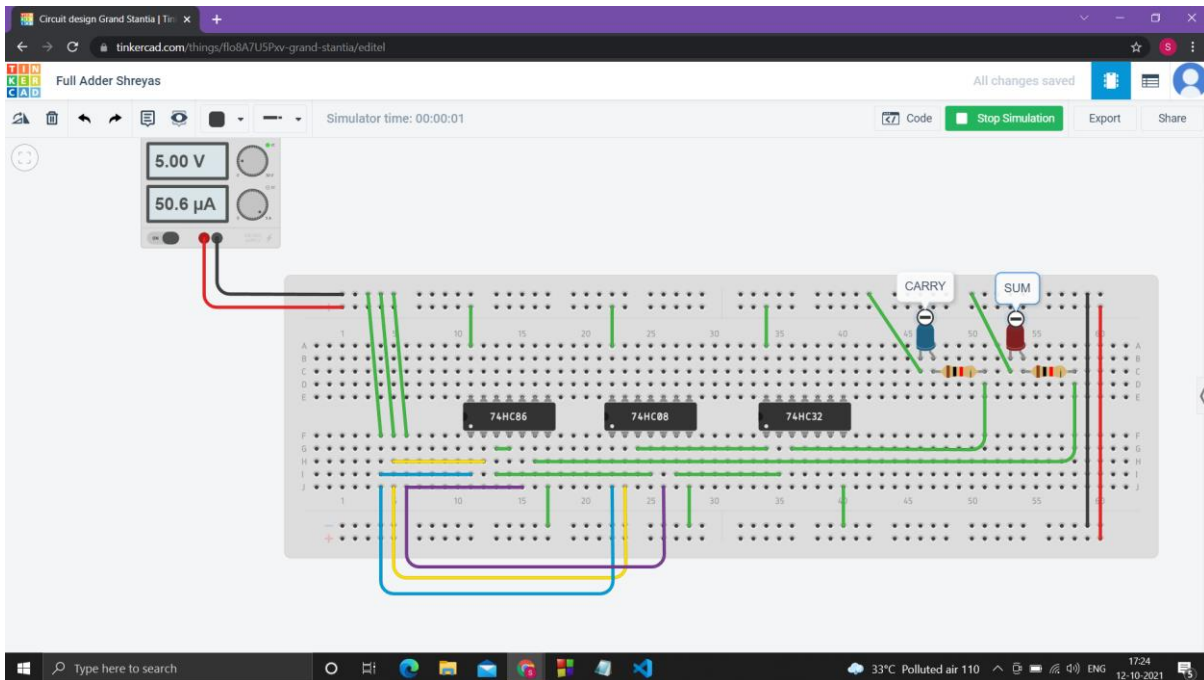


A=1 B=1

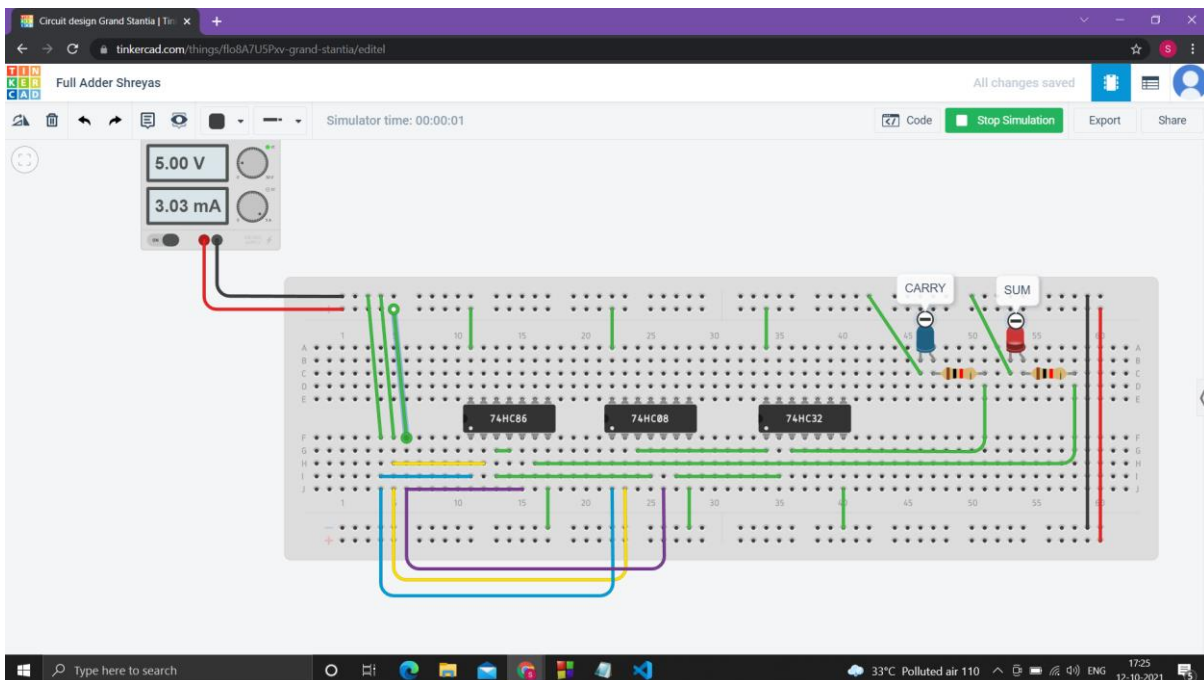


2) Full Adder

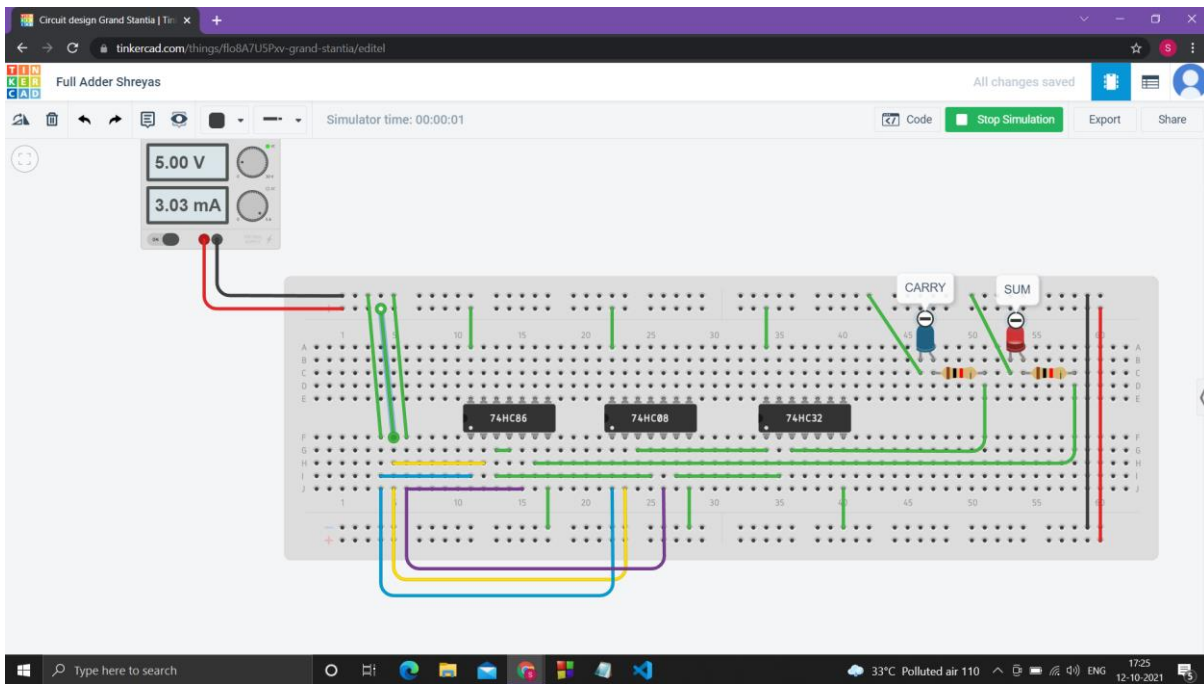
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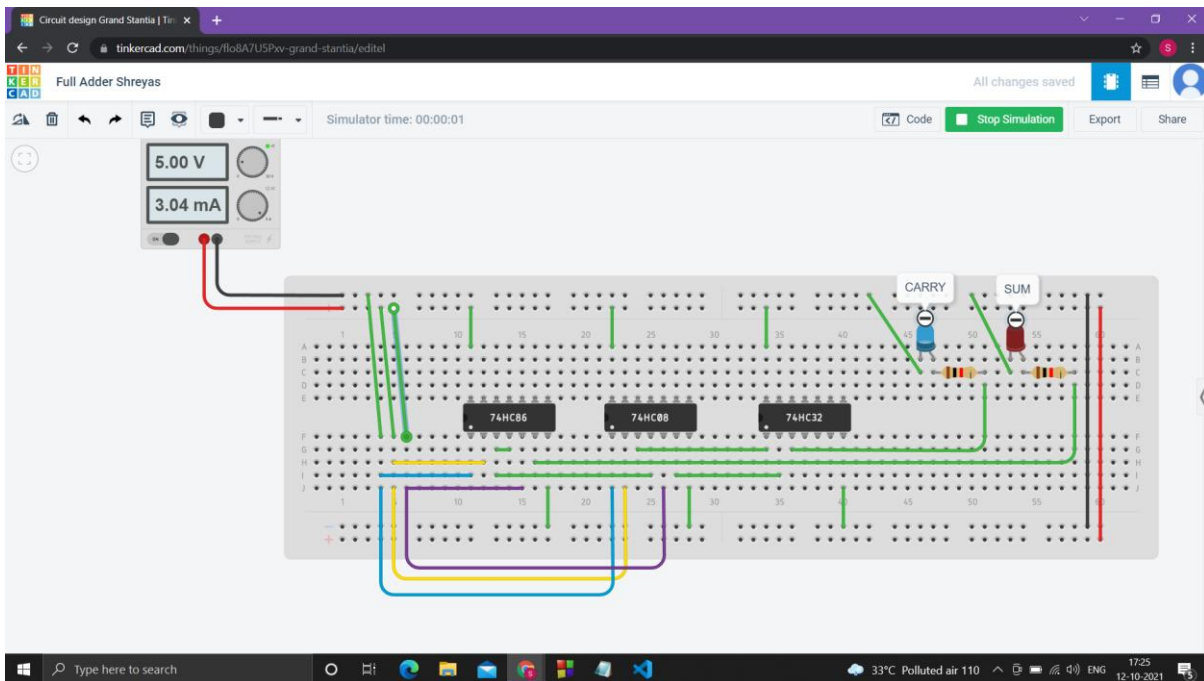
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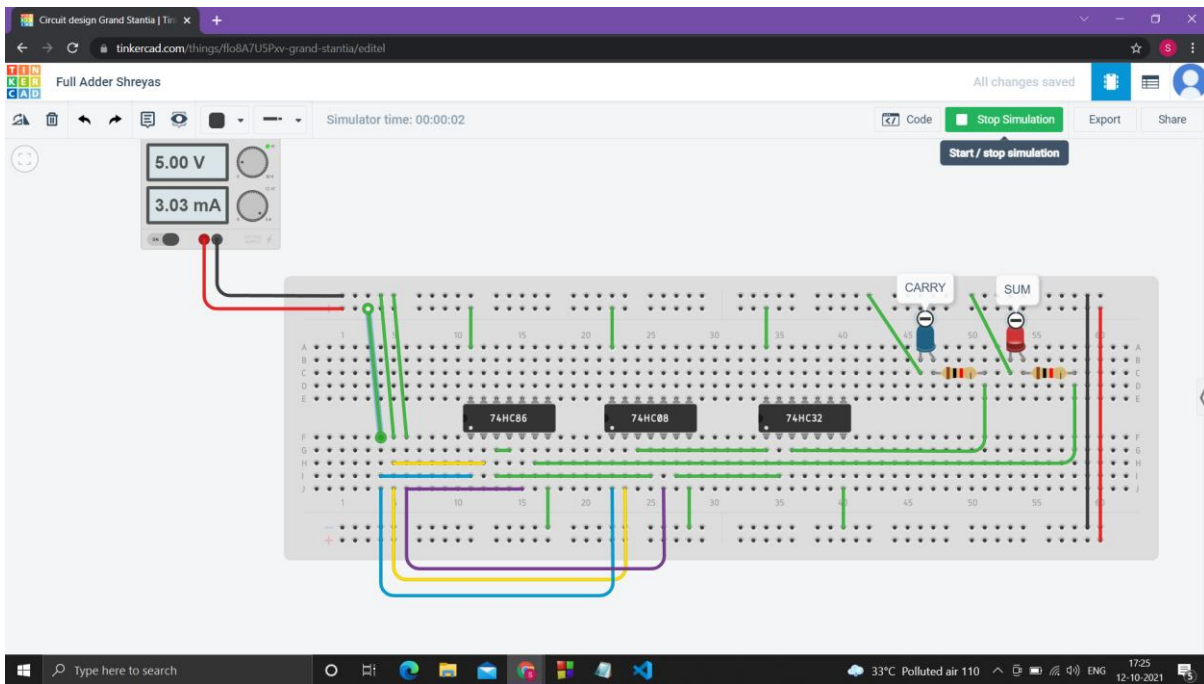
A=0 B=1 C=0



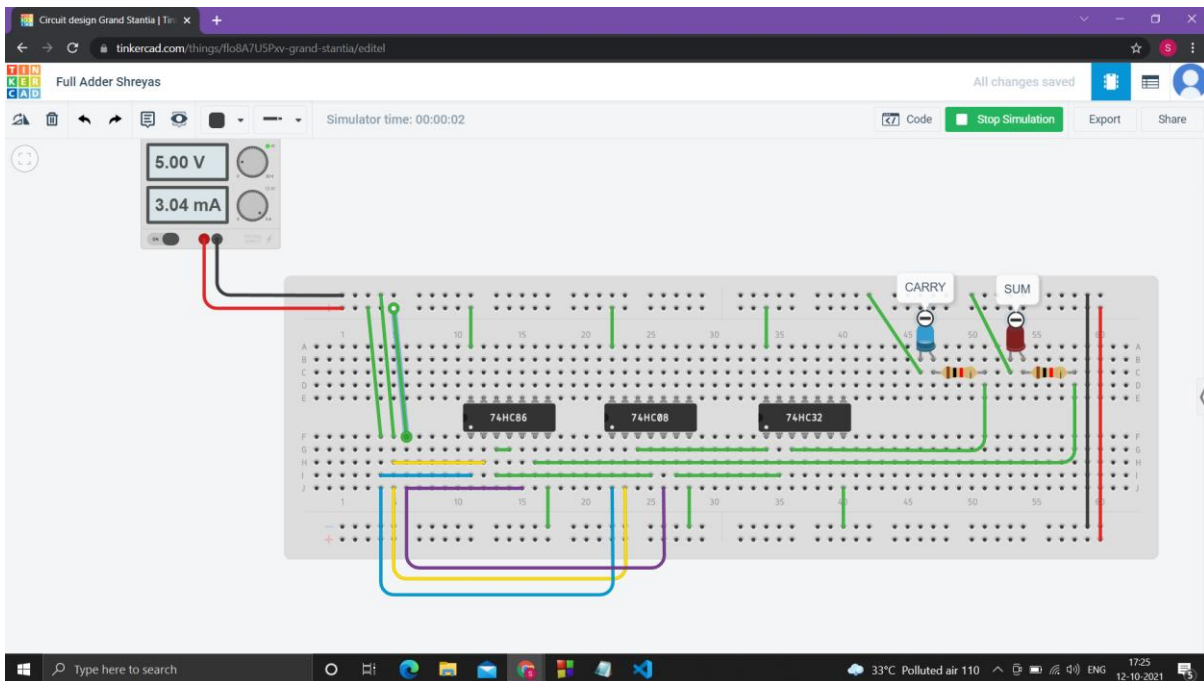
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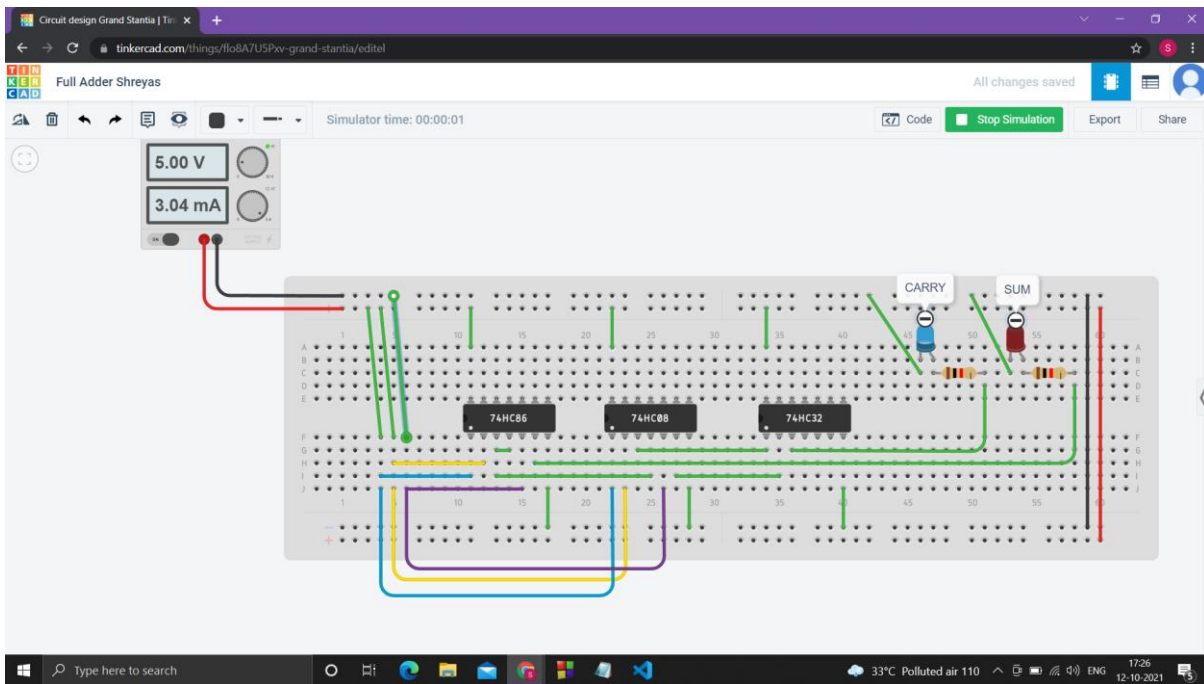
A=1 B=0 C=0



A=1 B=0 C=1



A=1 B=1 C=0



A=1 B=1 C=1

