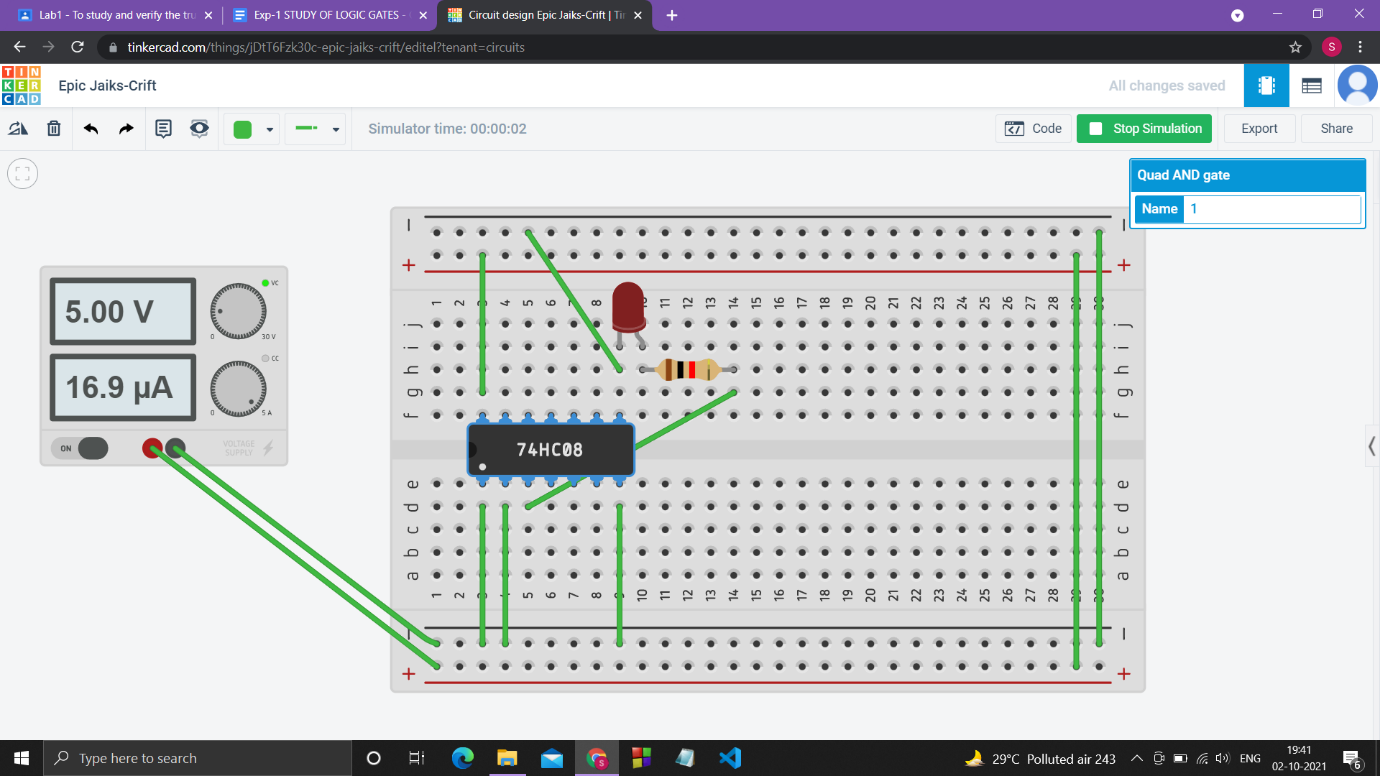
LAB 1: STUDYING LOGIC GATES AND VERIFYING THEIR TRUTH TABLES

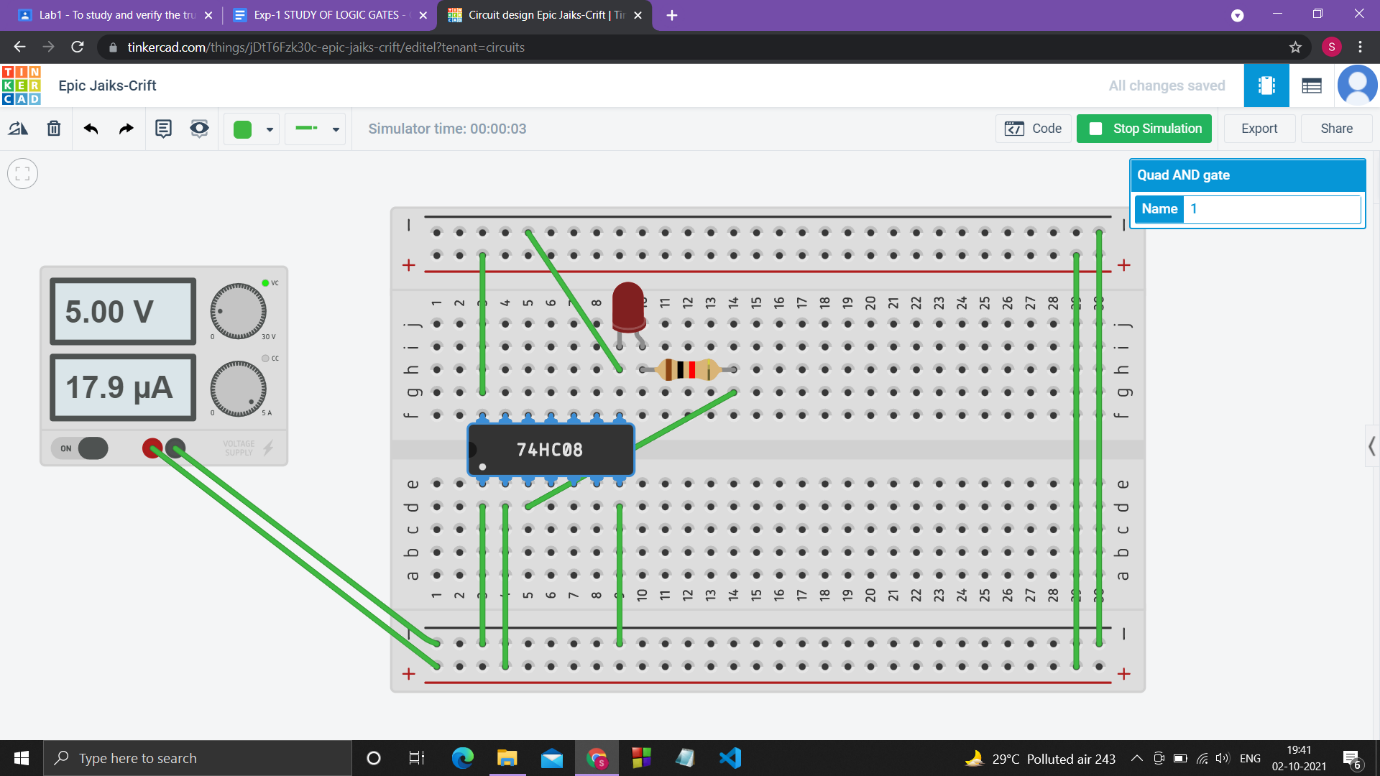
Name: Shreyas Sawant Div: D7A Roll No.: 55

1) AND Gate

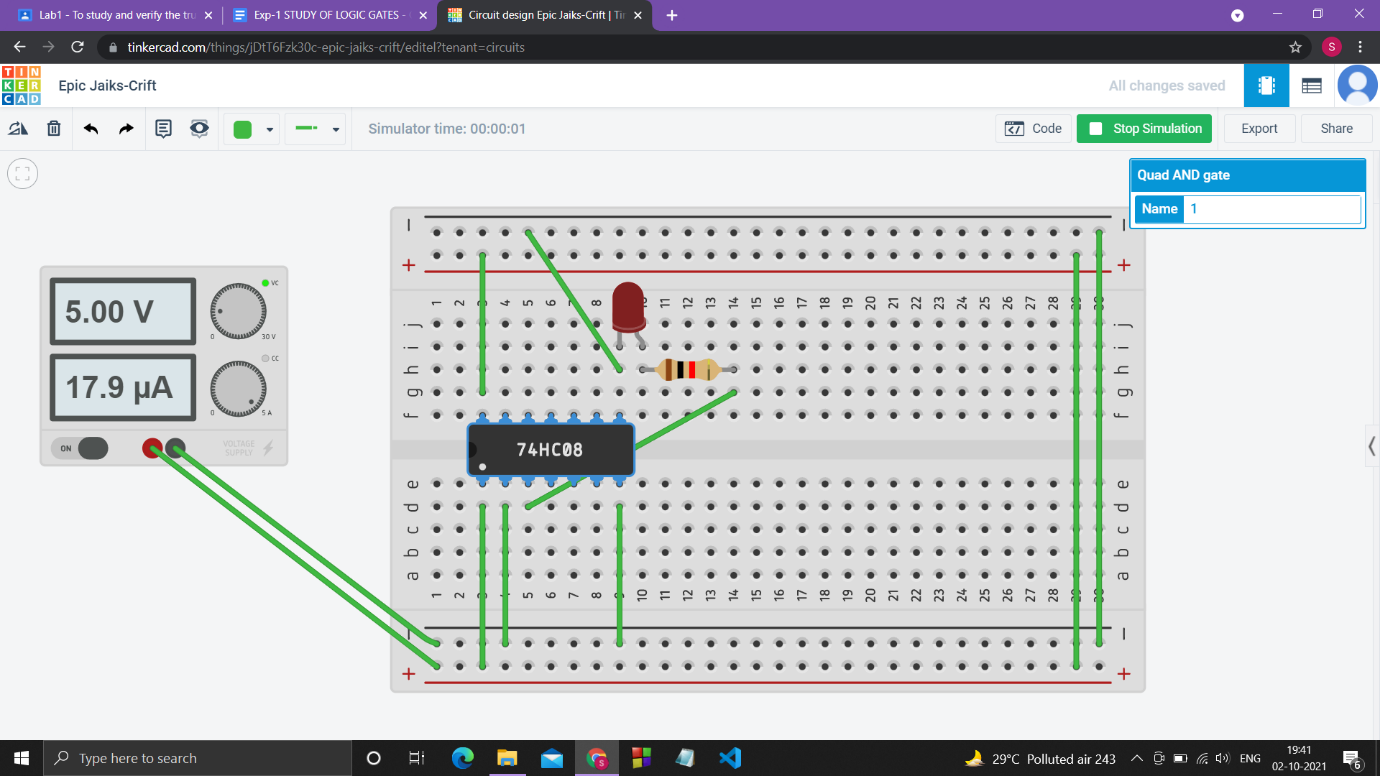
A=0 B=0



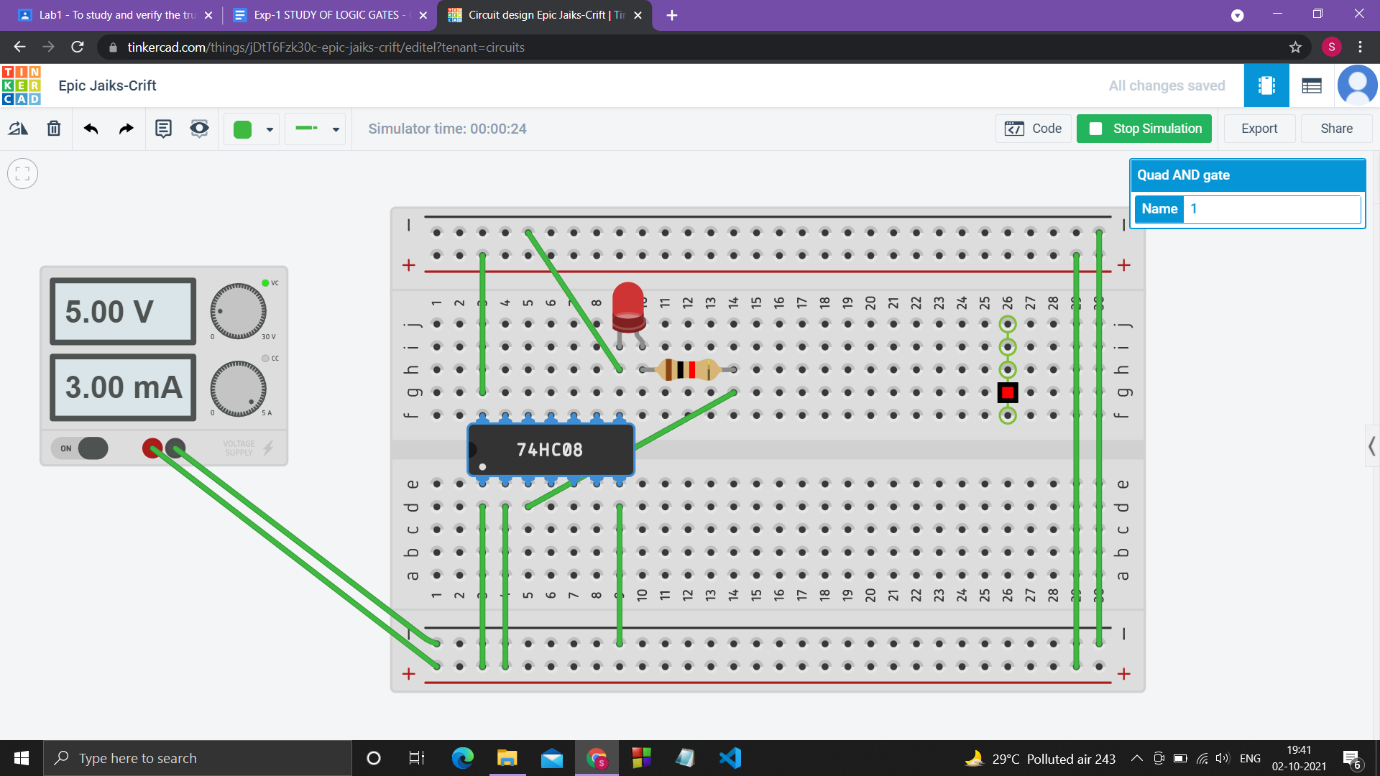
A=0 B=1



A=1 B=0

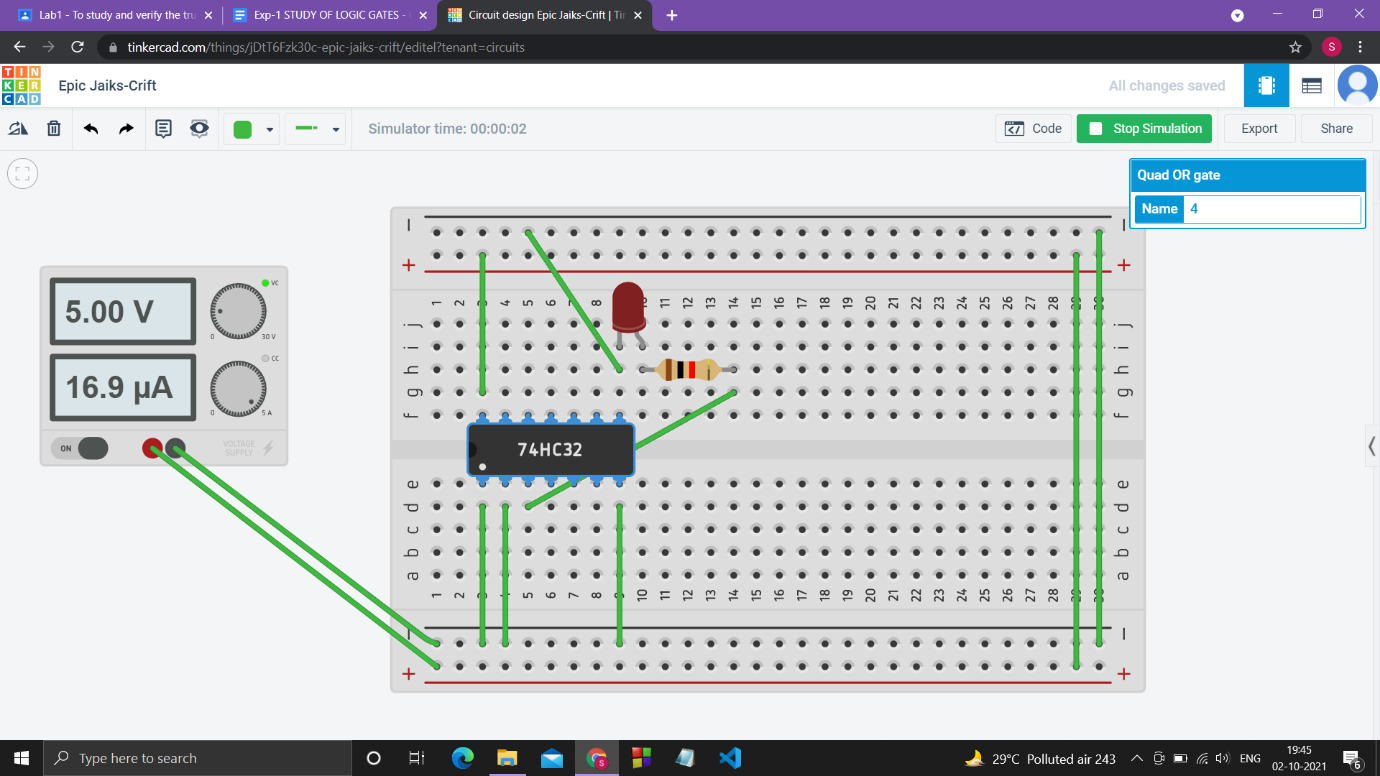


A=1 B=1

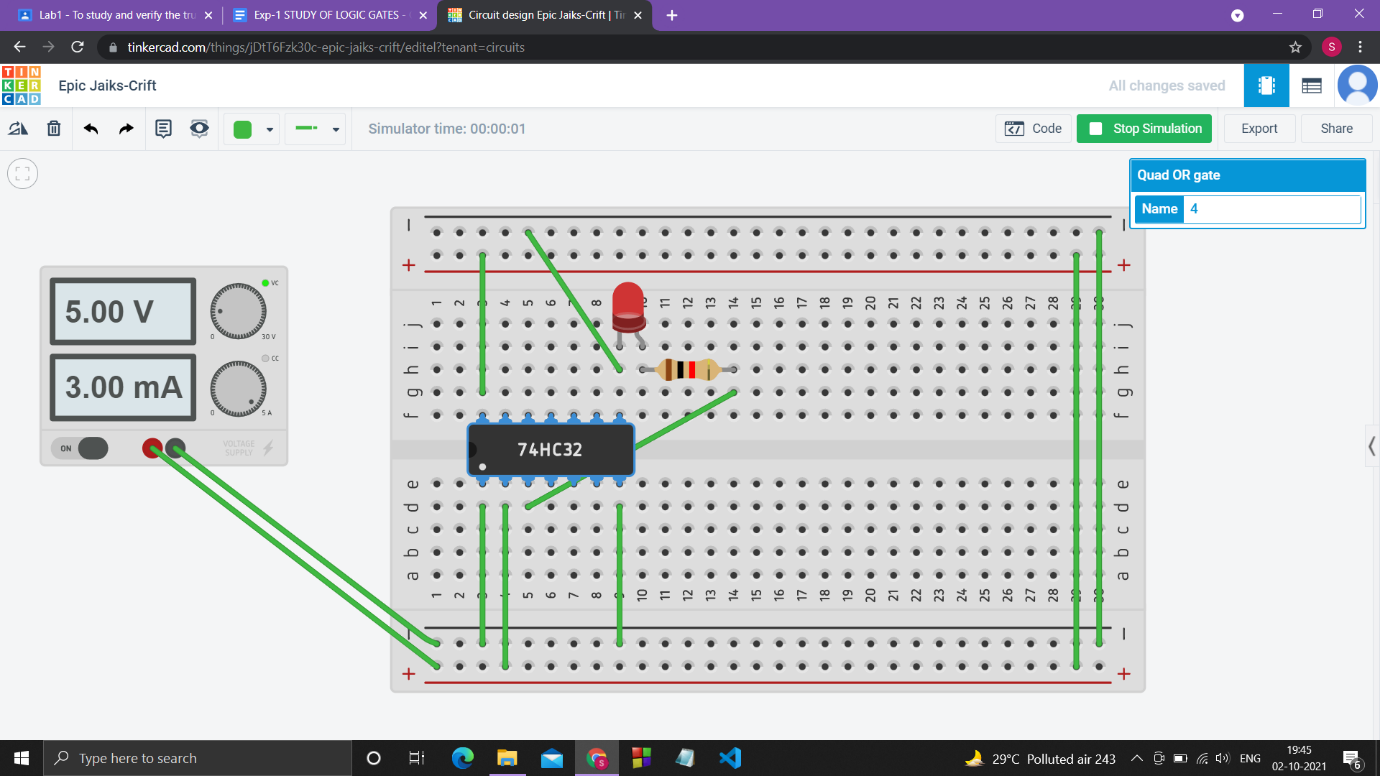


2) OR Gate

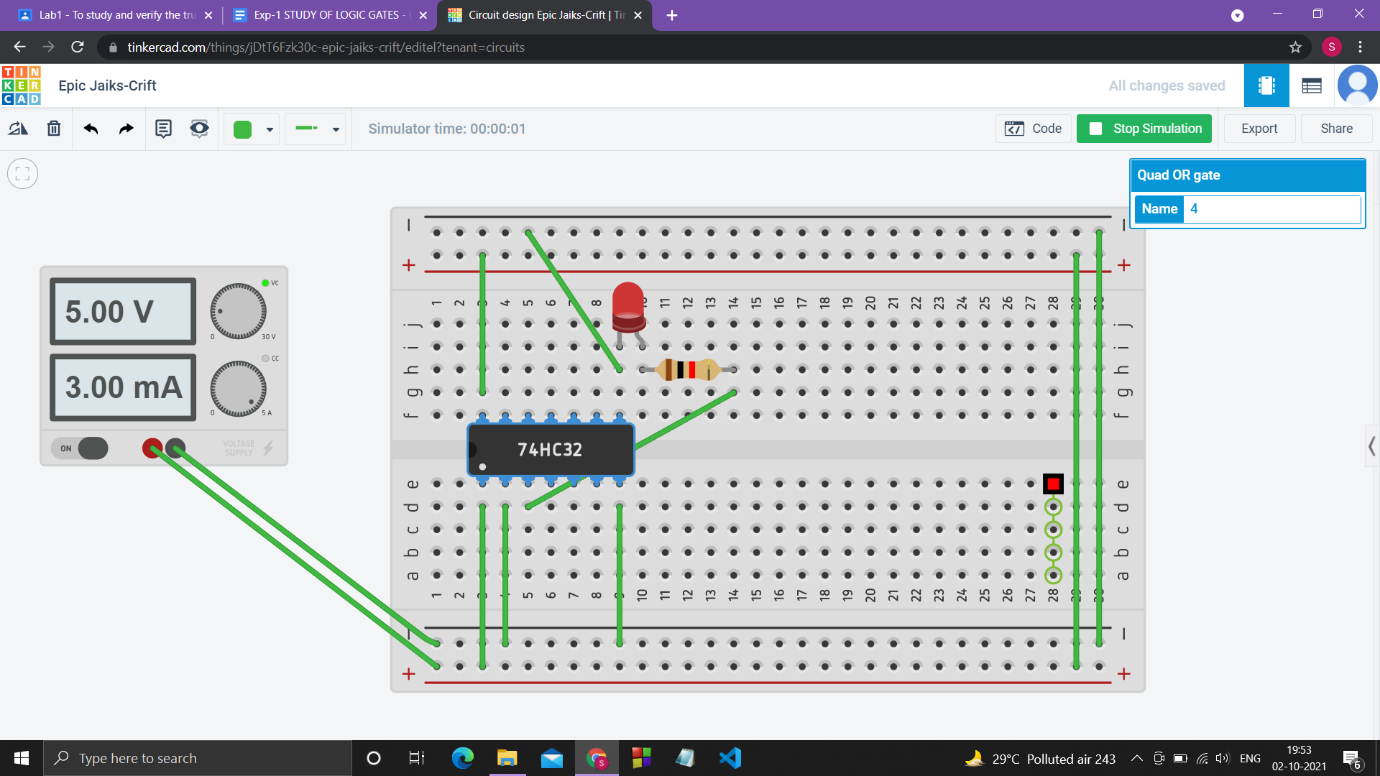
A=0 B=0



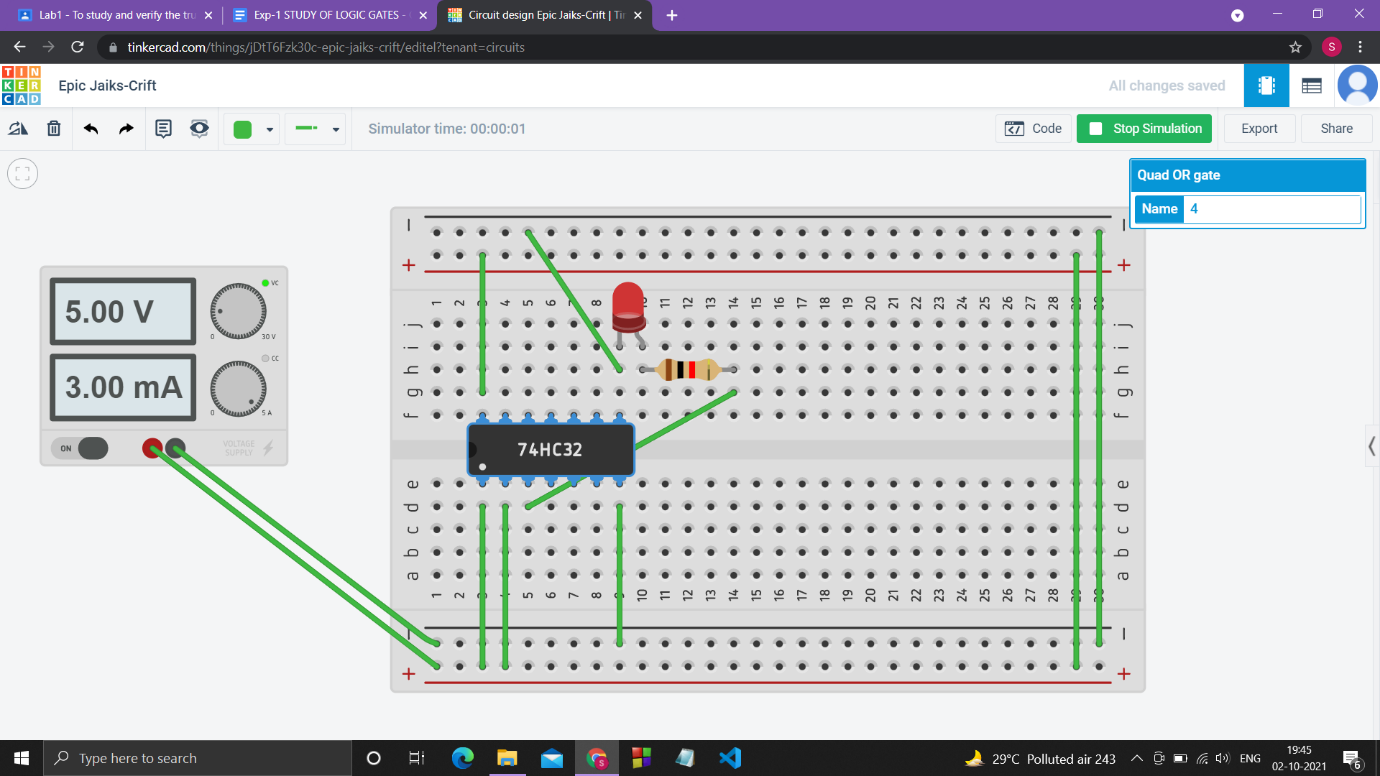
A=0 B=1



A=1 B=0

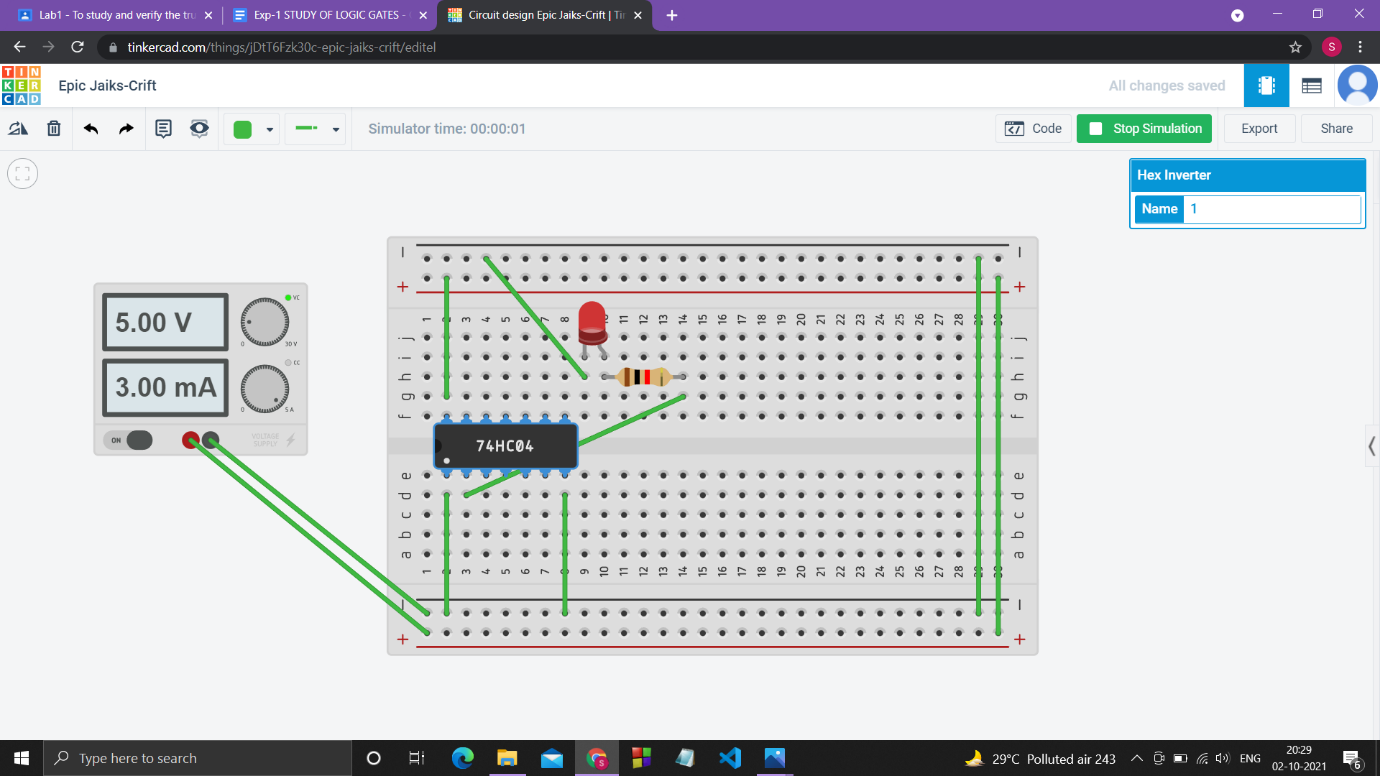


A=1 B=1

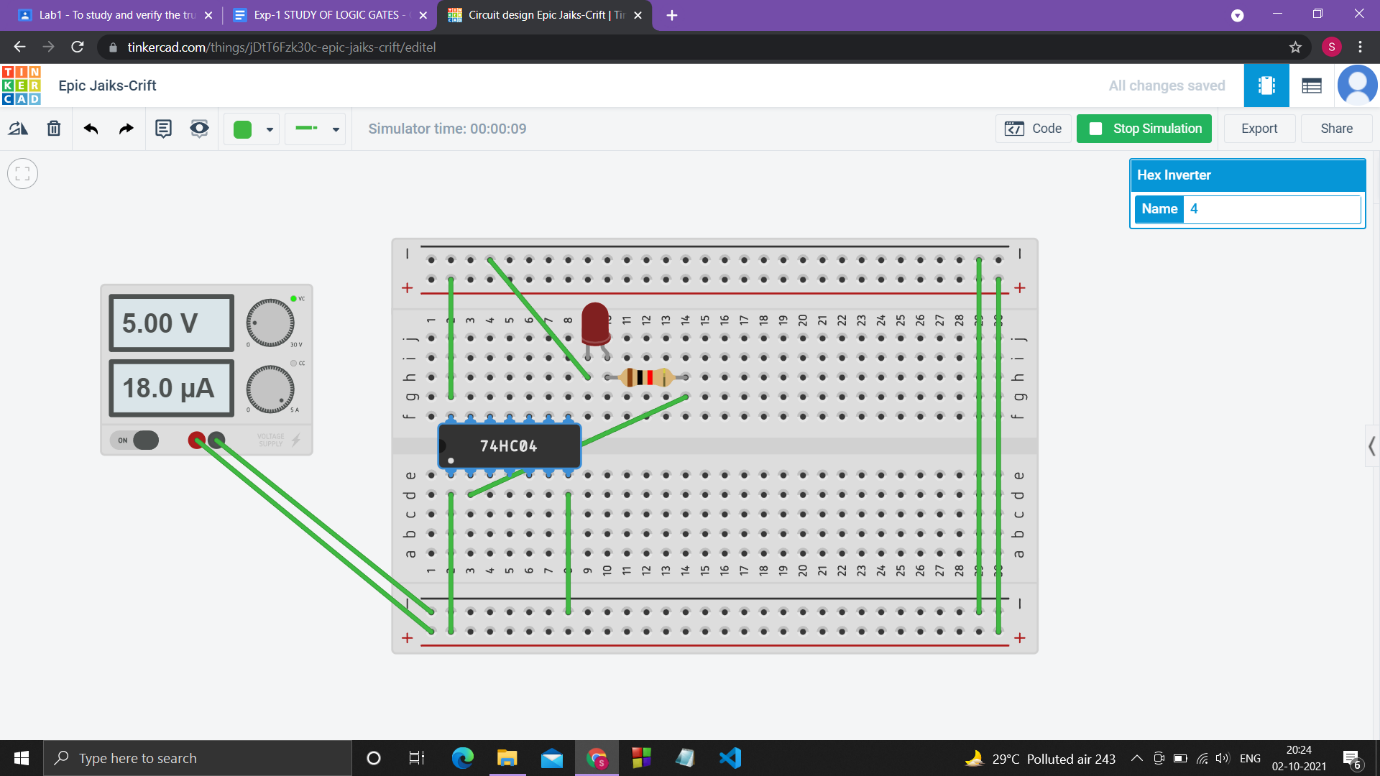


3) NOT Gate

A=0

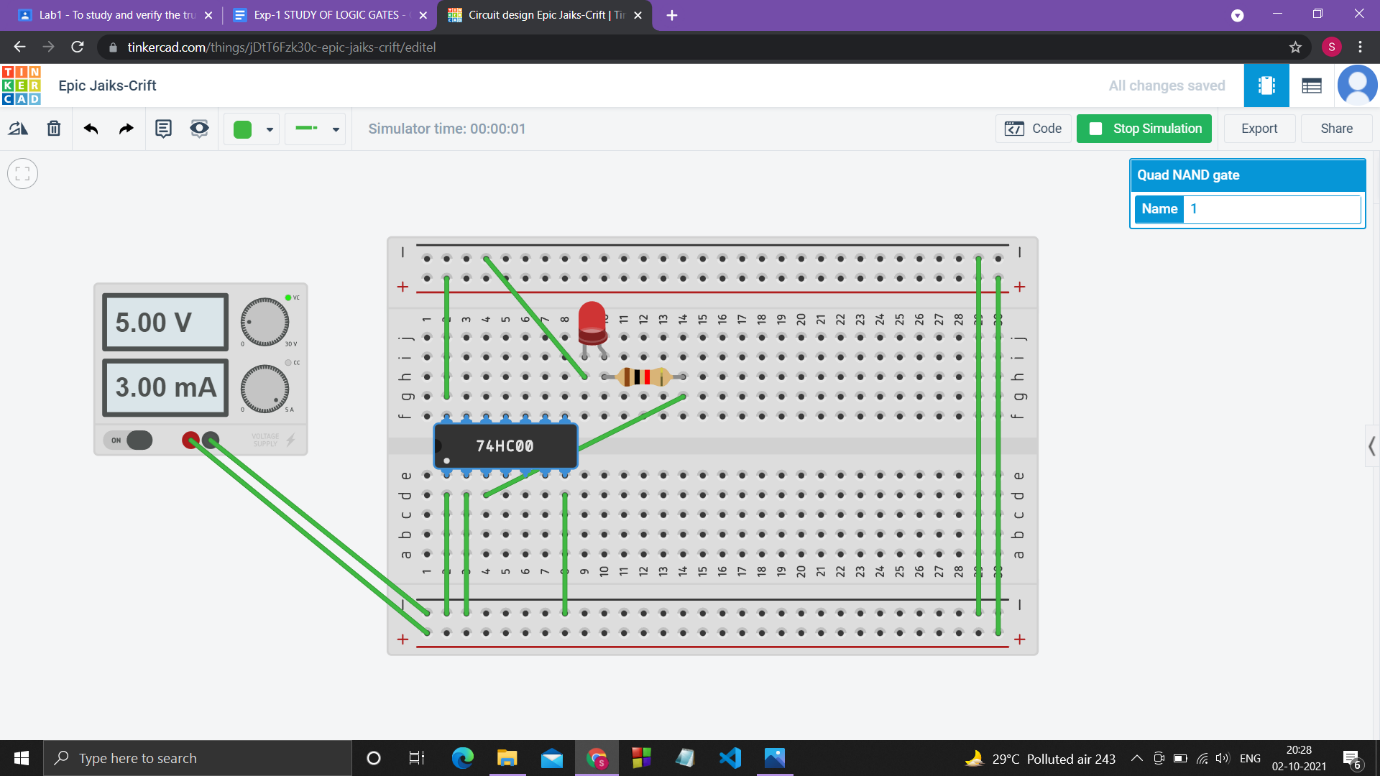


A=1

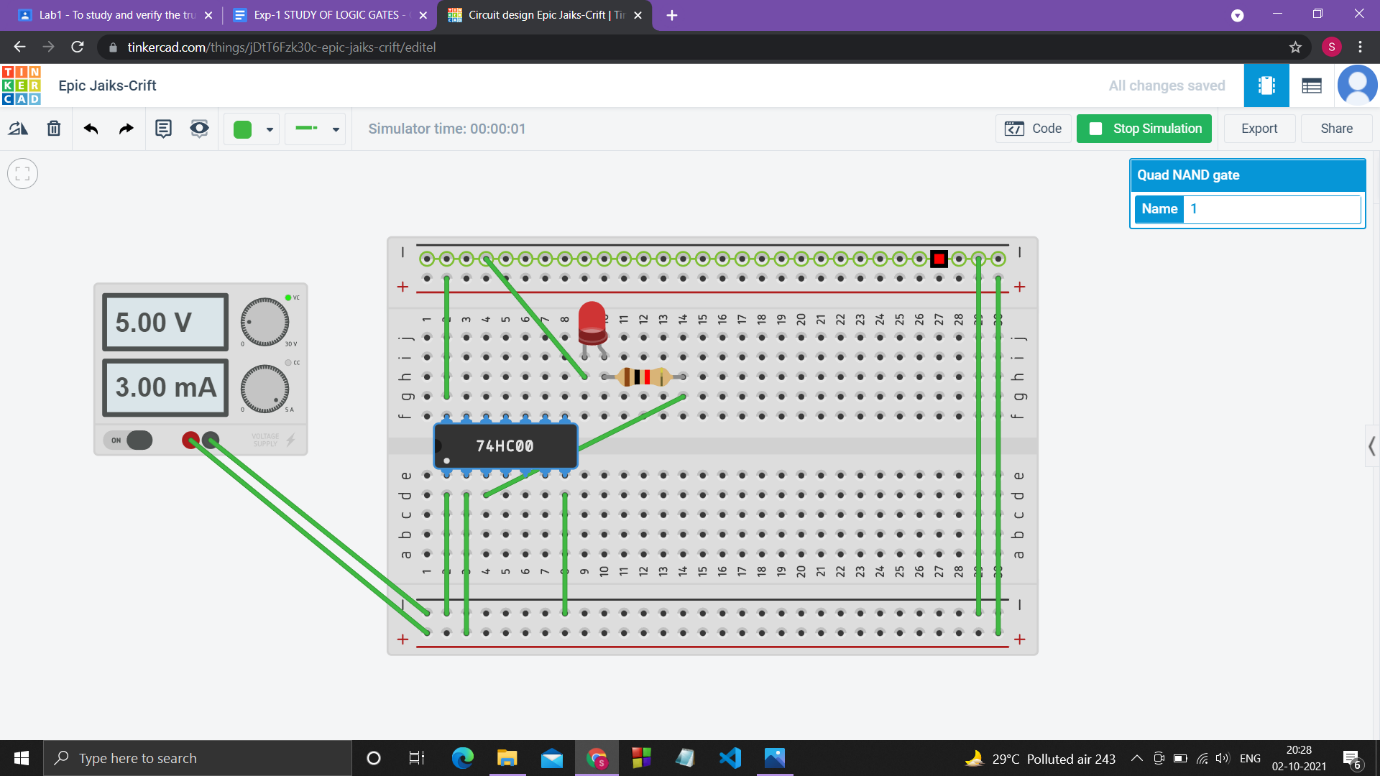


4) NAND Gate

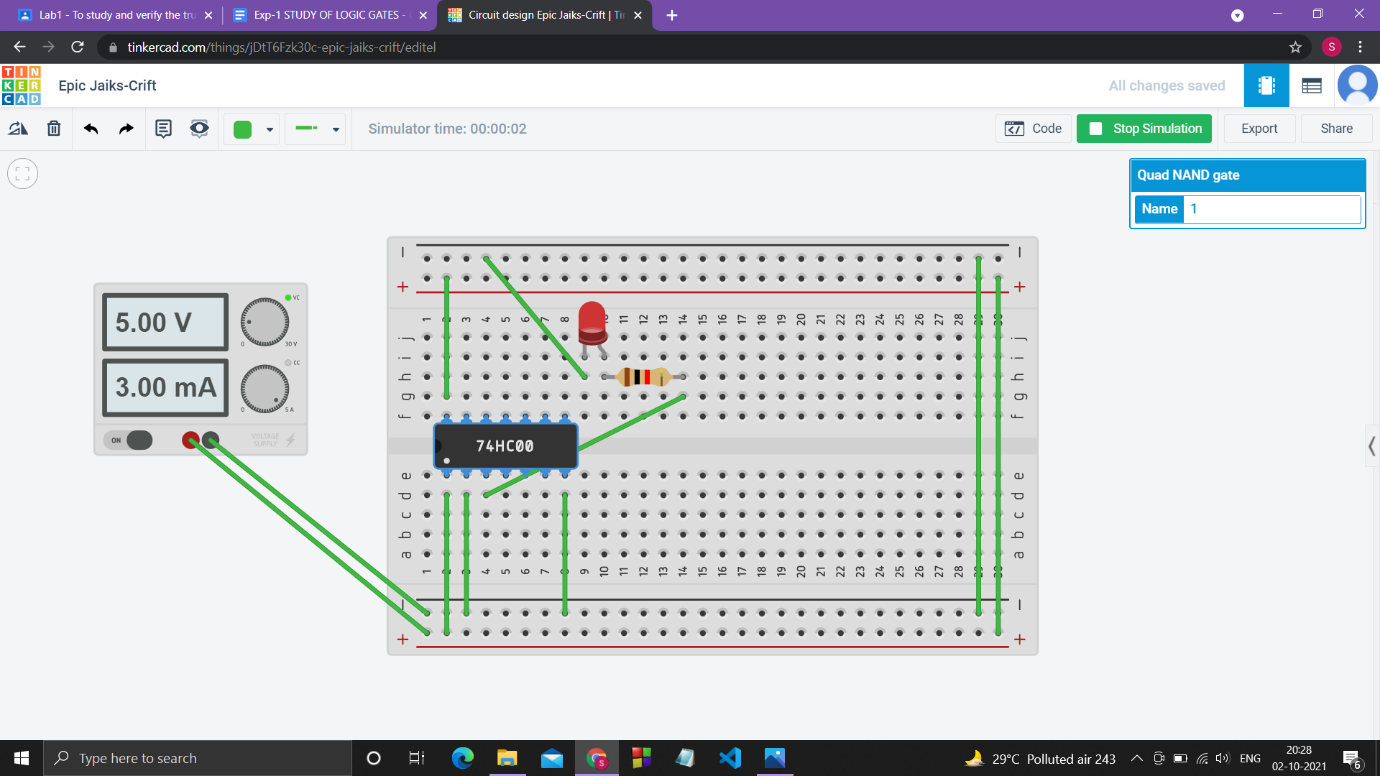
A=0 B=0



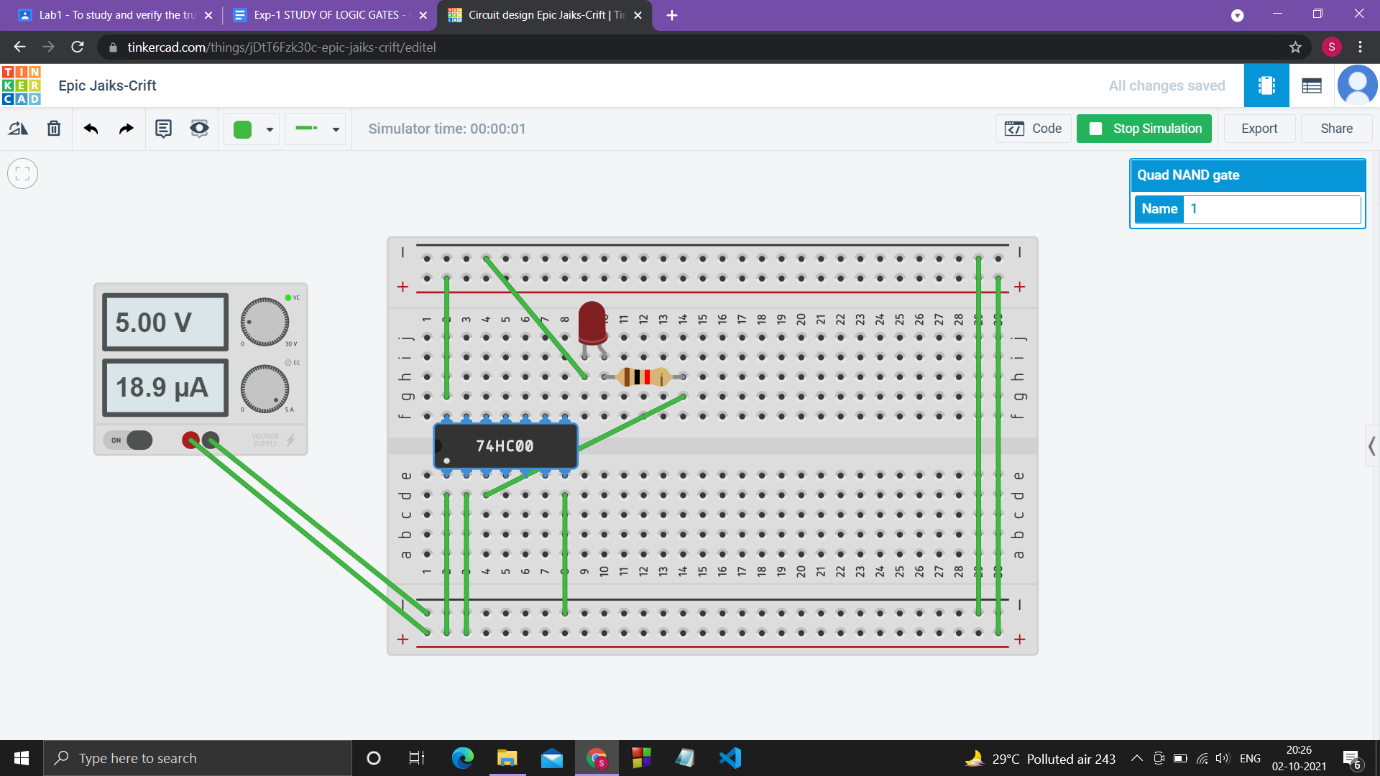
A=0 B=1



A=1 B=0

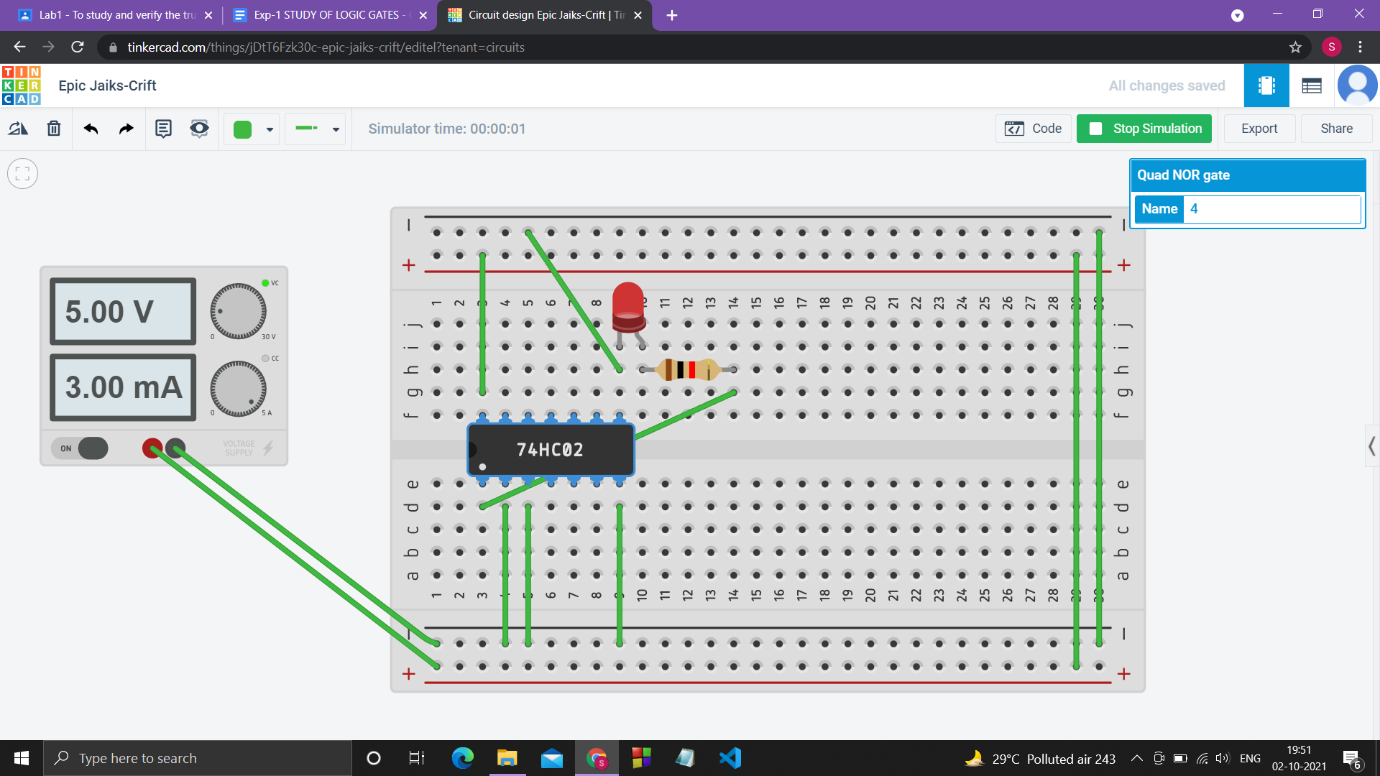


A=1 B=1

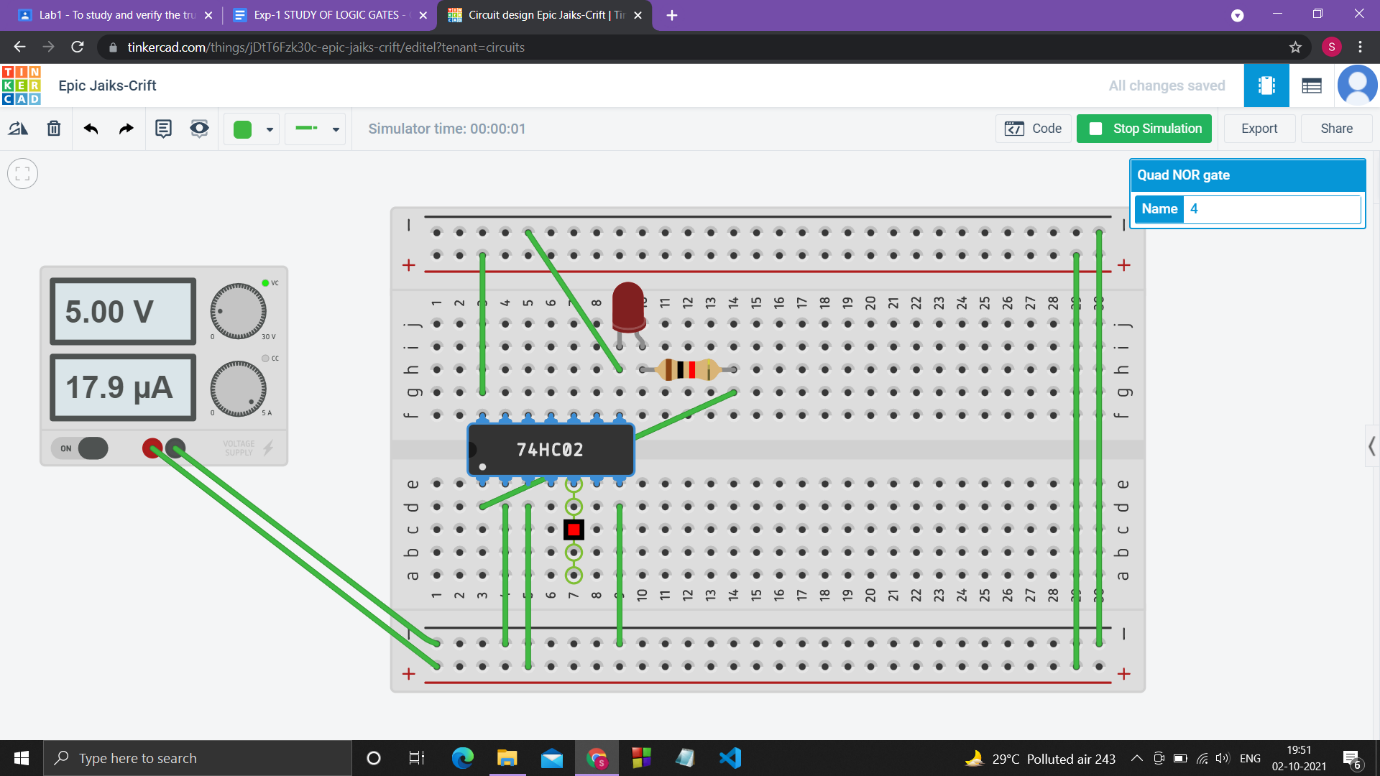


5) NOR Gate

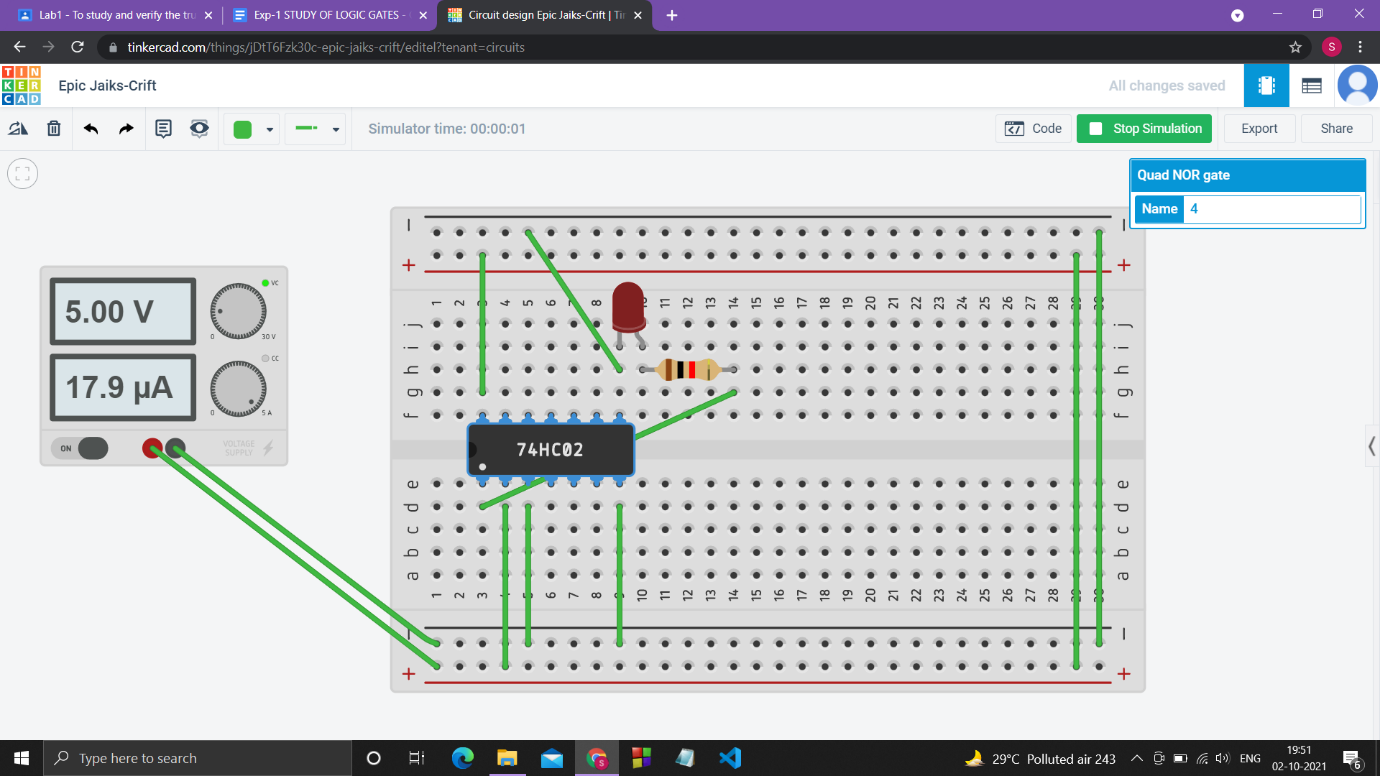
A=0 B=0



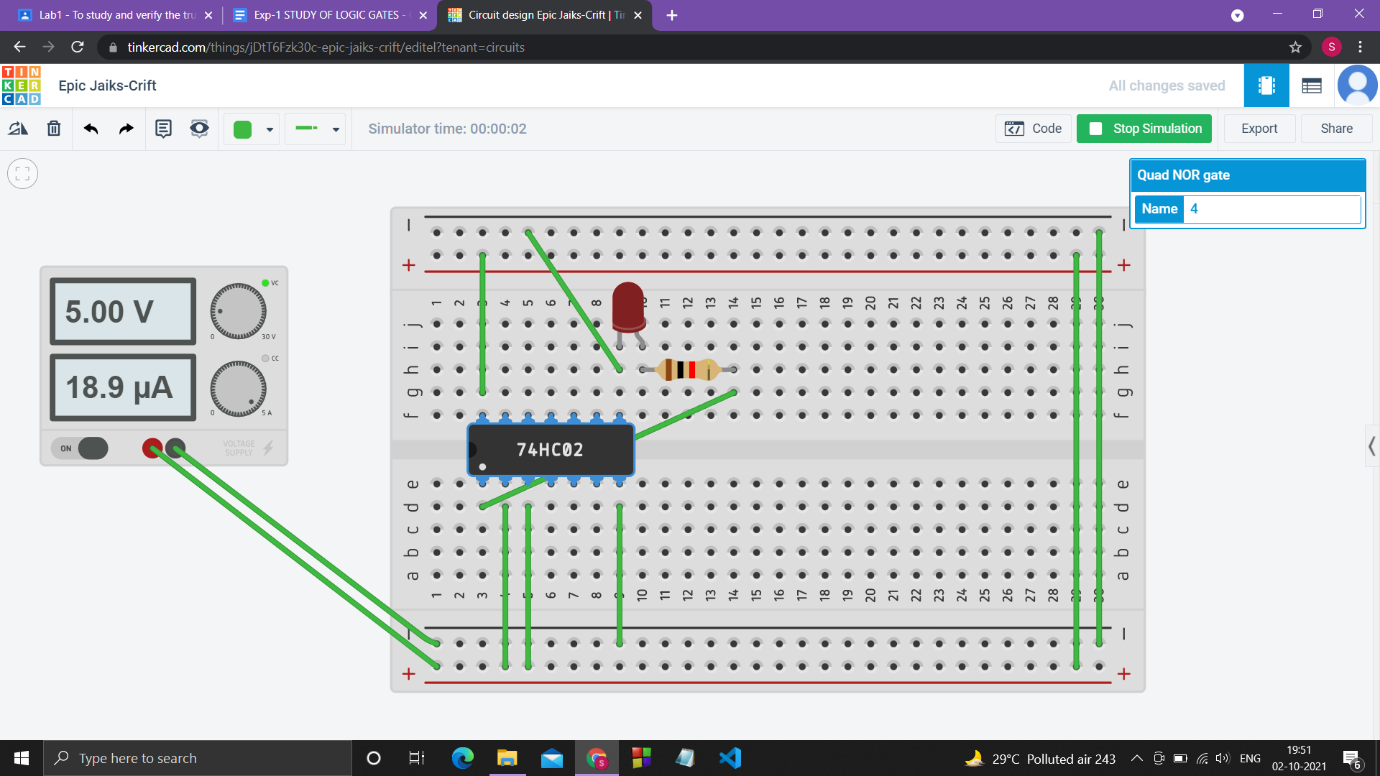
A=0 B=1



A=1 B=0

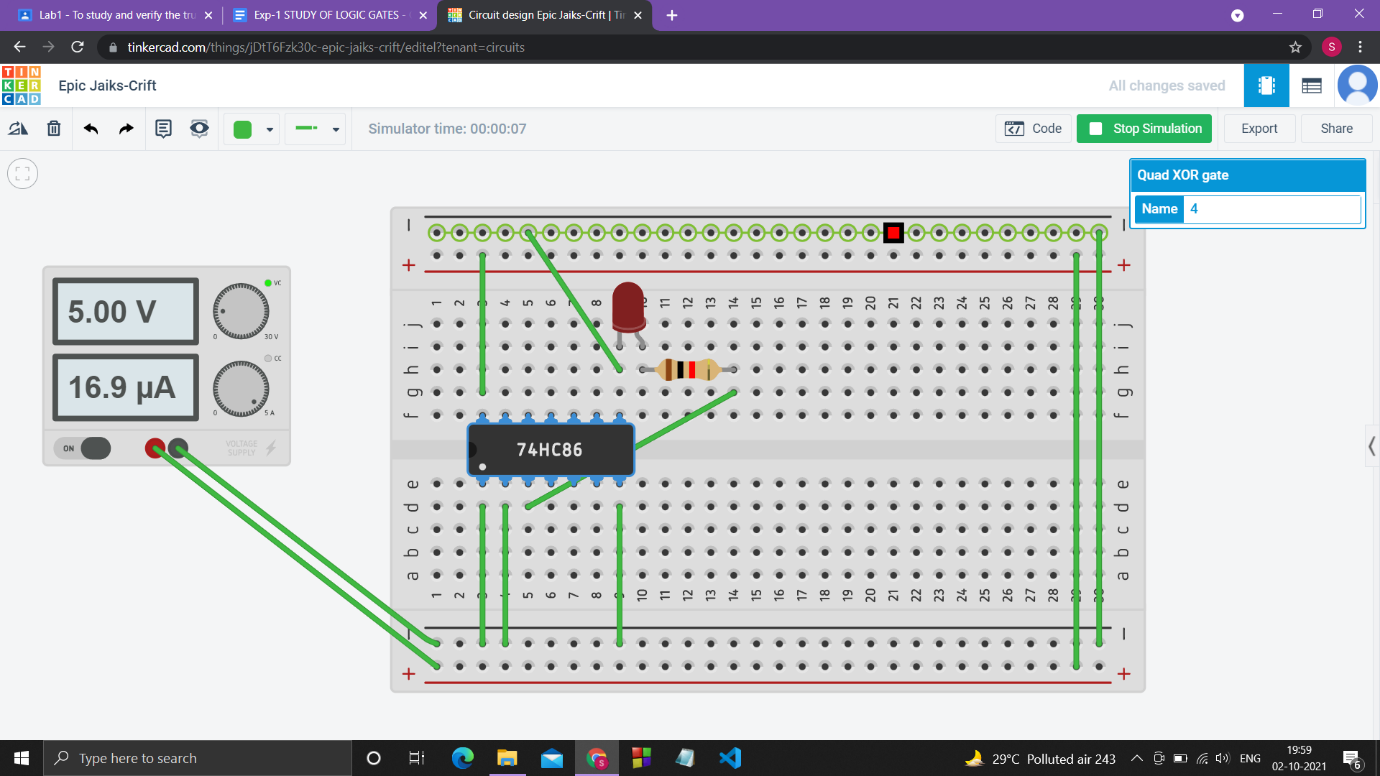


A=1 B=1

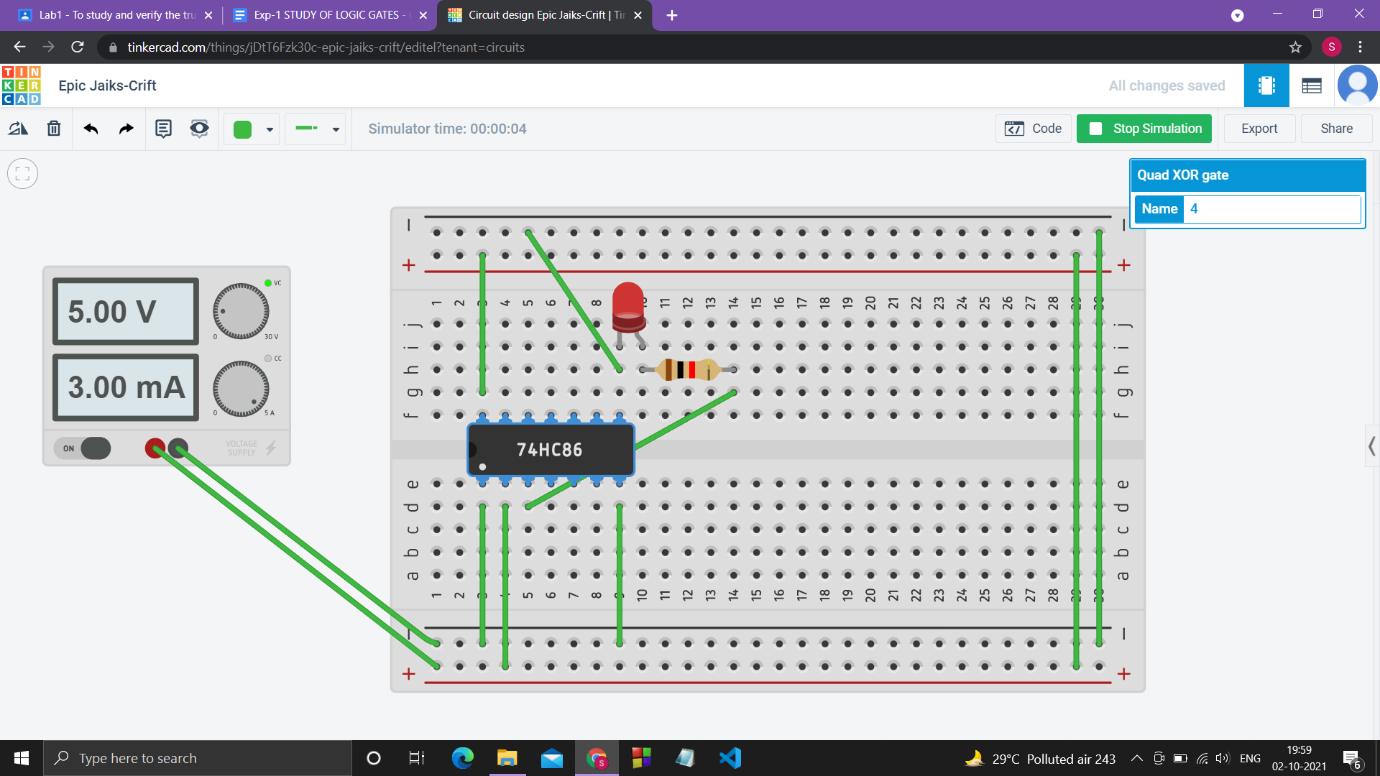


6) XOR Gate

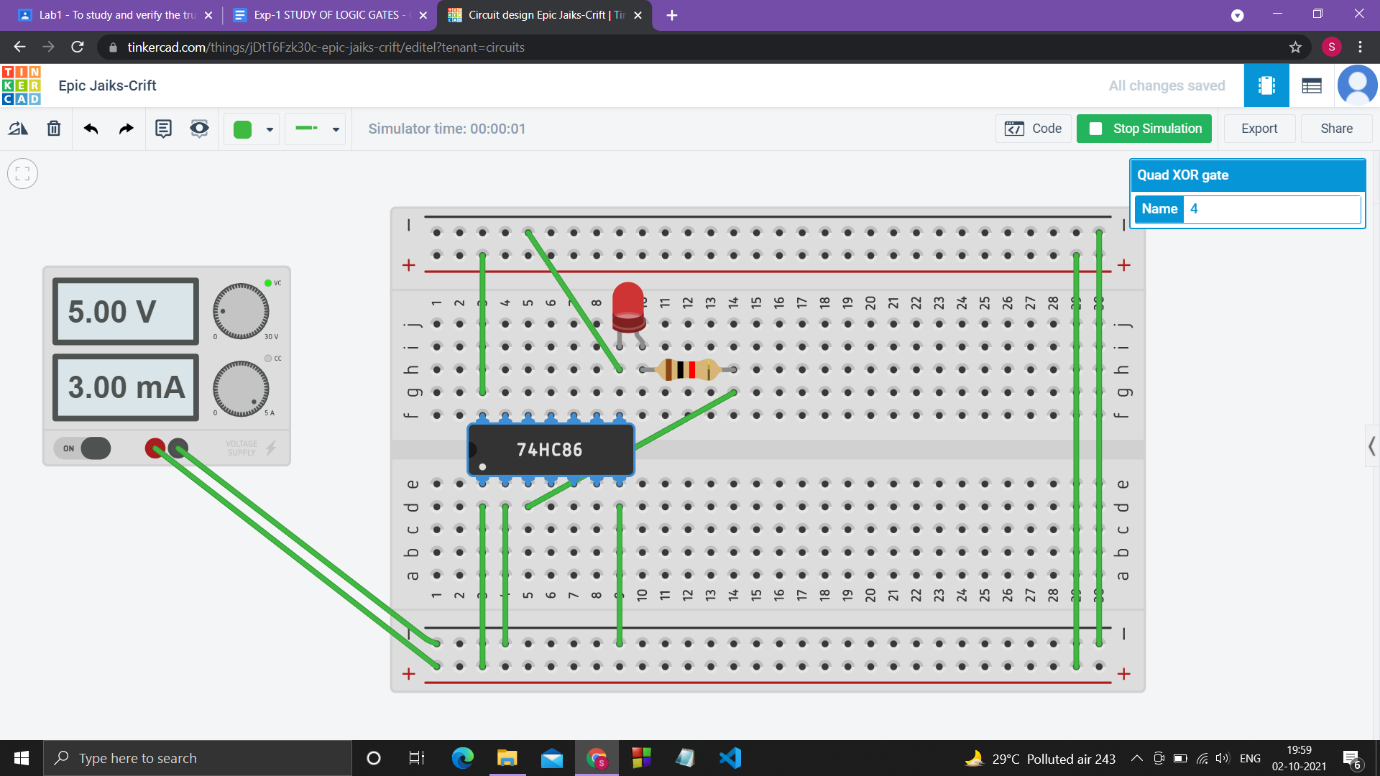
A=0 B=0



A=0 B=1



A=1 B=0



A=1 B=1

