Jirong Yang yjrcs@umich.edu | 734-882-8266 | Ann Arbor, MI

Education

University of Michigan, Ann Arbor Ann Arbor, MI
B.S. in Computer Science and B.S. in Statistics, GPA 3.83/4 2023/08 - 2025/12
Harbin Institute of Technology Harbin, China
B.S. in Computer Science, GPA 93.63/100 2021/08 - 2023/06
Coursework: Computer Architecture, Microarchitecture, Parallel Computer Architecture, Operating System, Scalable System, Compiler, Parallel Computing, Machine Learning, Computer Vision

Award

- **S&S Fund for International Students Scholarship (10000$)**
- **Summer Undergraduate Research in Engineering (SURE) program (6000$)**

Experience

Research Assistant | Advisor: Prof. Krisztian Flautner Ann Arbor, MI
– **Stack**: *E-Graph, Compiler, ISA Design, Design Space Exploartion.* ***Present***
- Developed an ISA-level E-Graph rewriting framework for RISC-V that enables superoptimization to guide ISA extension design while also accelerating saturation to make real-time compiler integration feasible.

Research Assistant | Synergy Lab - Advisor: Prof. Tushar Krishna Atlanta, GA
– **Stack**: *Symbolic AI, ASIC Design, Dataflow Optimization.* ***Present***
- Analyzed neuro-symbolic AI workflows to identify core symbolic operators, and designed an ASIC accelerator system that optimizes heterogeneous dataflow for such hybrid paradigms.

Research Assistant | Advisor: Prof. Nathan Bleier Ann Arbor, MI
– **Stack**: *Deep Learning, ASIC Design, Dataflow Optimization, Design Space Exploration, Chiplet.* *2025/01–2025/08*
- Proposed a heterogeneous ASIC chiplet ecosystem leveraging hierarchical design-space exploration to integrate chiplet heterogeneity, tensor fusion, and tensor/pipeline parallelism to improve energy efficiency and reduce cost.

Research Assistant | LIMOS Lab - Advisor: Prof. Yafeng Yin Ann Arbor, MI
– **Stack**: *LLM Agent, Transportation System.* 2024/05 – 2024/12
- Developed an LLM-based agent framework to simulate travel demand models, designing prompts to optimize trip planning and decision-making.

Publication

T. Liu, **J. Yang**, Y. Yin. Toward LLM-agent-based modeling of transportation systems: A conceptual framework. Artificial Intelligence for Transportation, 2025.
H. Jin, **J. Yang**, Y. Liu, B. Lyu, K. Zhang, N. Bleier. Mozart: An Ecosystem-Accelerator Codesign Framework for Composable Heterogeneous Chiplet Based Neural Network Accelerators. ASPLOS'26, **under review**.

Projects

N-way Superscalar Out-of-Order R10K Processor | **Advisor: Prof. Krisztian Flautner** 2024/09 - 2024/12
- Developed a high-performance RISC-V CPU from scratch in SystemVerilog, based on the MIPS R10K architecture. Achieved a 7.7ns clock period and an average CPI of 1.7 across C programs.
- **Branch Prediction**: Implemented PAg, Gshare, and Tournament branch predictors, achieving over 90% accuracy. Integrated early branch resolution to reduce misprediction penalties and improve pipeline efficiency.
- **Memory System**: Designed both a speculative and a conservative Load-Store Queue with internal forwarding. Developed an instruction cache with prefetching and a victim cache, and a non-blocking data cache.
- Synthesized and extensively tested the design, using a top-down **cycle-level simulator** to identify processor bottlenecks. Developed automation and visualization tools to streamline debugging and performance evaluation. The entire project comprised approximately 40,000 lines of code.

WriteBoost Read-Copy Update (RCU) Library 2024/10 - 2024/12
- Developed a simplified interface for a Read-Copy Update (RCU) library that handles read, write, and reclaim synchronization responsibilities, improving usability and reducing programming complexity.
- Optimized update-side performance through batch processing and memory pooling, achieving competitive write performance while maintaining exceptional read-side scalability.

Skills

Language: C/C++, Verilog/System Verilog, Python, CUDA, Chisel