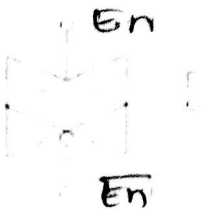
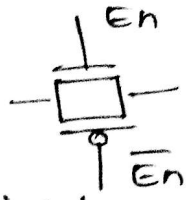


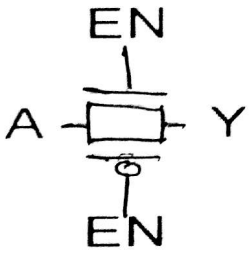
En	A	B
1	0	0
1	1	1
0	0	Z
0	1	Z



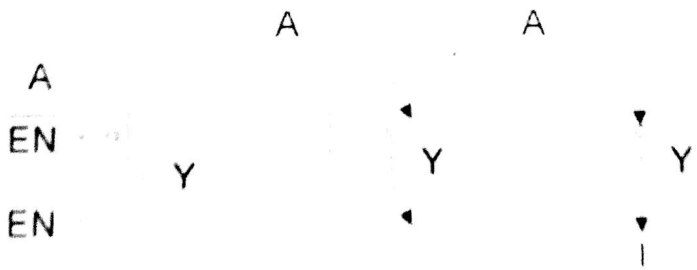
High impedance

High impedance.

- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y



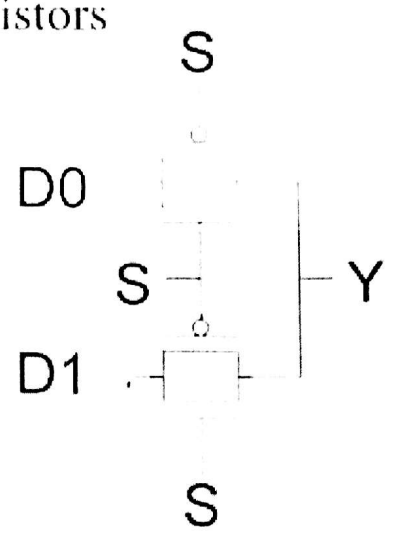
- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output



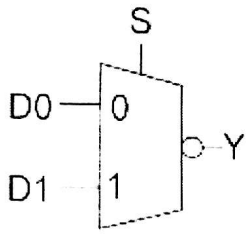
EN = 0
Y = 'Z'

EN = 1
Y = A

- Nonrestoring mux uses two transmission gates
  - Only 4 transistors

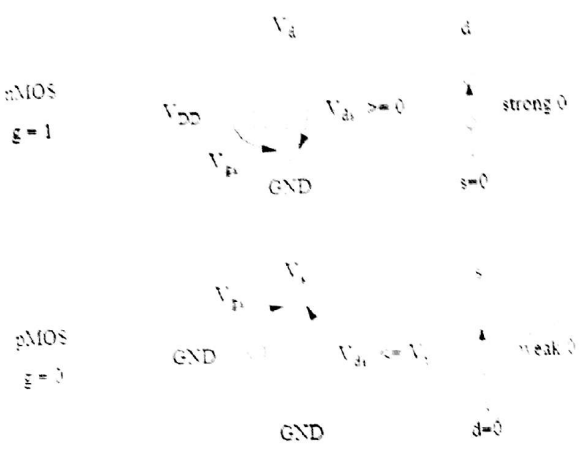


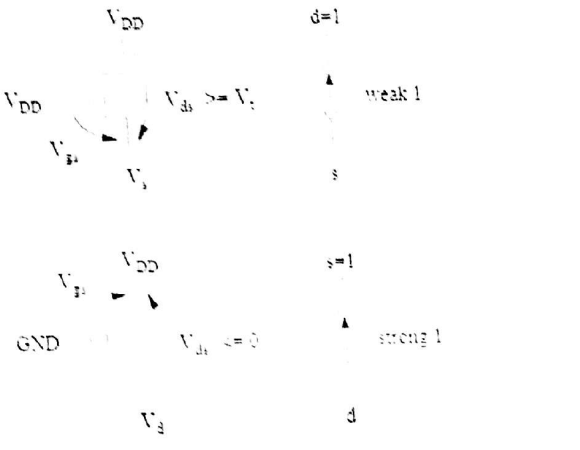
Restoring gates mux



Transmission Gate Notes

Transmission Gate





nMOS

$V_d = 0$

g = 1

s = 0 → d = strong 0

$V_d = V_{DD} - V_t$

g = 1

s = 1 → d = weak 1

pMOS

$V_s = V_t$

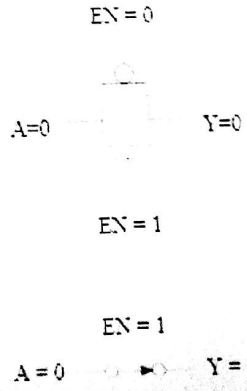
g = 0

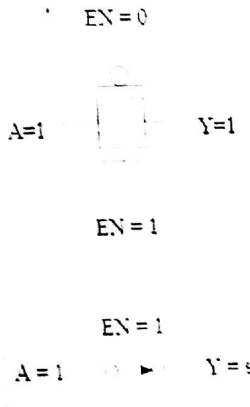
d = 0 → s = weak 0

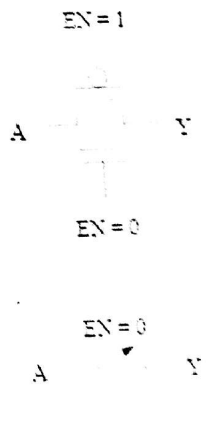
$V_s = V_{DD}$

g = 0

d = 1 → s = strong 1







Transmission gate Notes

Transmission Gate

pMOS

g = 0

GND

$V_{ds} <= V_t$

weak 0

GND

d=0

nMOS

$V_d = 0$

$V_d = V_{DD} - V_t$

g = 1

s = 0 — d = strong 0

g = 1

s = 1 — d = weak 1

pMOS

$V_s = V_t$

$V_s = V_{DD}$

g = 0

d = 0 — s = weak 0

g = 0

d = 1 — s = strong 1

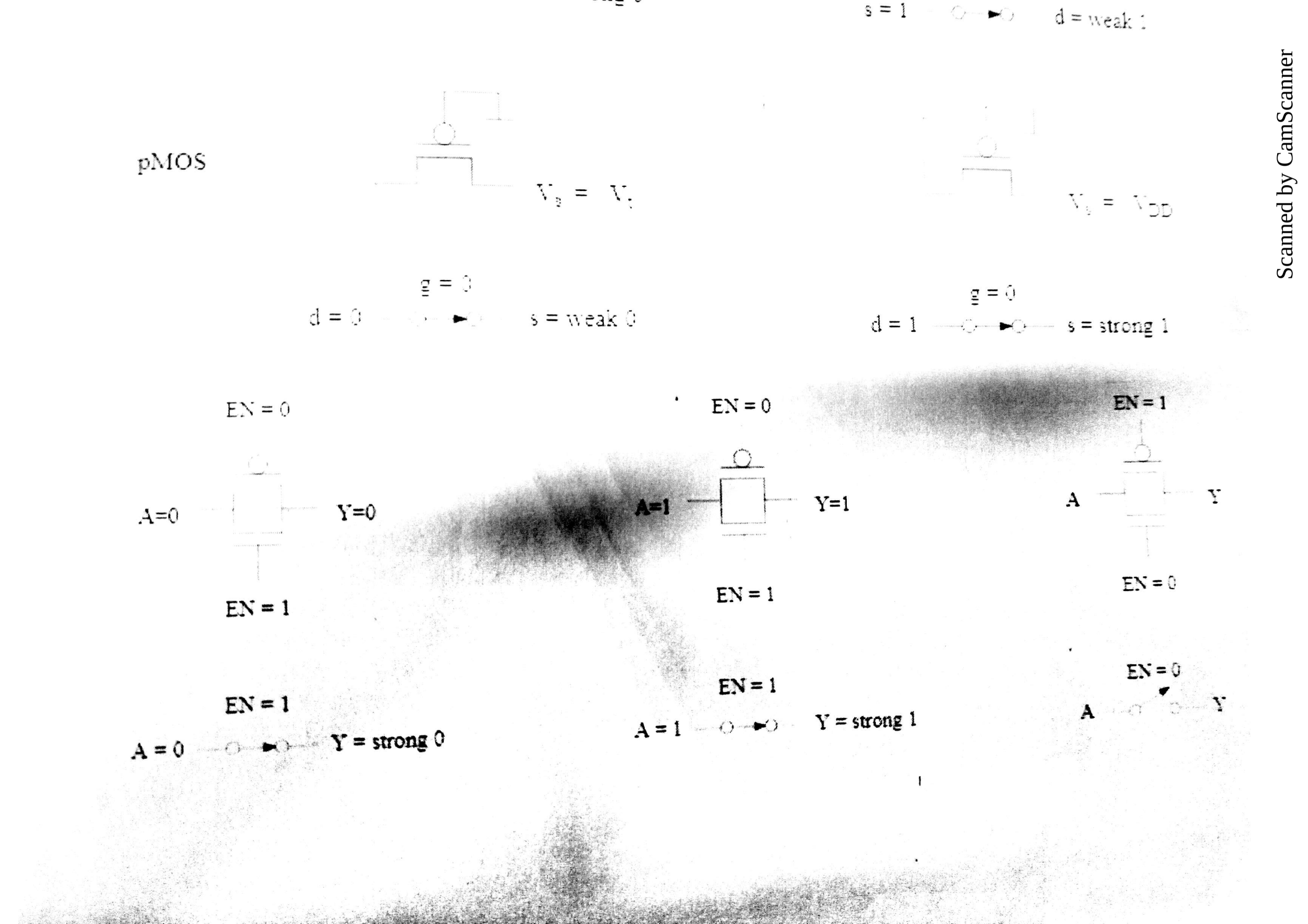
EN = 0

EN = 0

EN = 1

A

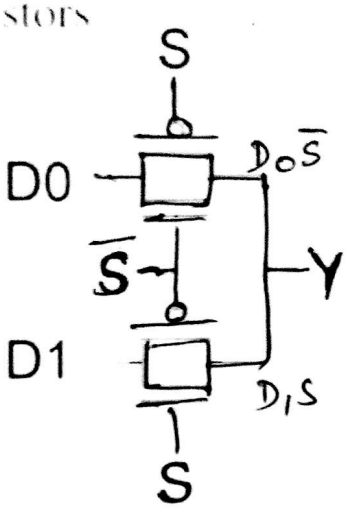
Y



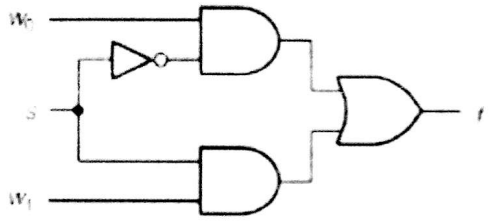
2:1 mux

- Nonrestoring mux uses two transmission gates
  - Only 4 transistors

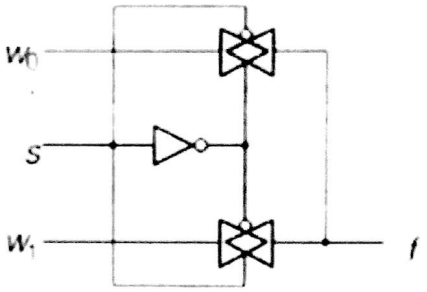
(I)



$D_0\bar{S} + D_1S$

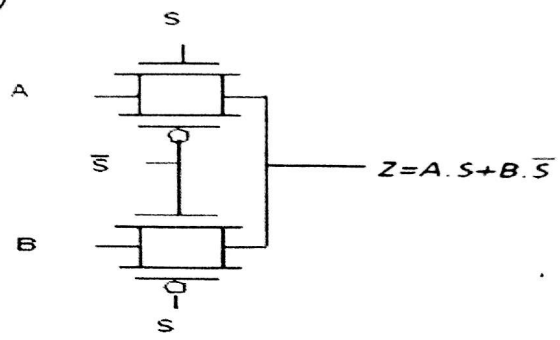


(a) Sum-of-products circuit



(c) Circuit with transmission gates

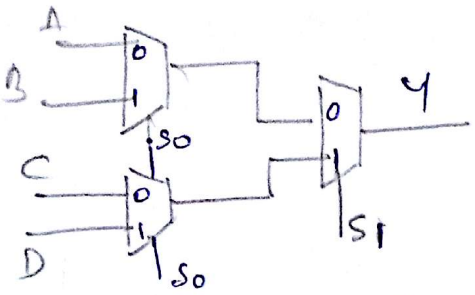
(II) (or)



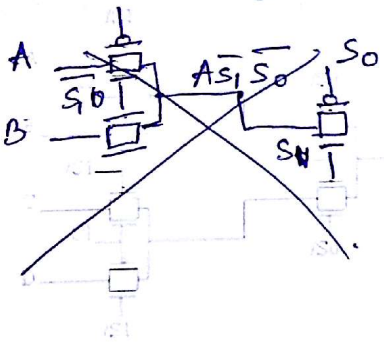
When S=0, $\bar{S}$ = 1, then, PMOS and NMOS of B will be ON and Z= A.0 + B.1=B

When S=1, $\bar{S}$ = 0, then, PMOS and NMOS of A will be ON and Z= A.1 + B.0=A

4:1 Mux



S_1	S_0	Y
0	0	A
0	1	B
1	0	C
1	1	D



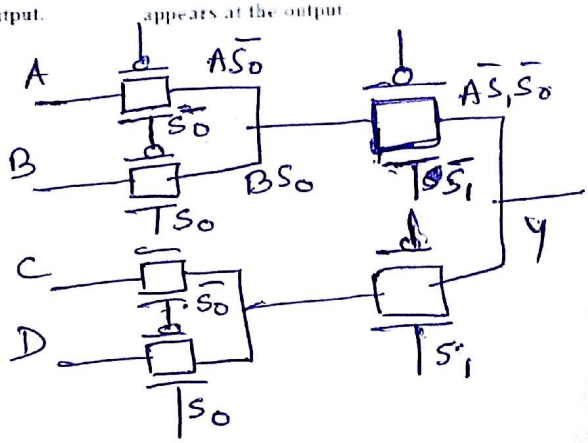
When S1=0, S1=1,
B and D turns ON, and,
When S0=0, S0=1,
D is selected and
appears at the output

When S1=1, S1=0,
A and C turns ON, and,
When S0=0, S0=1,
C is selected and
appears at the output

When S1=0, S1=1,
B and D turns ON, and,
When S0=1, S0=0,
B is selected and
appears at the output.

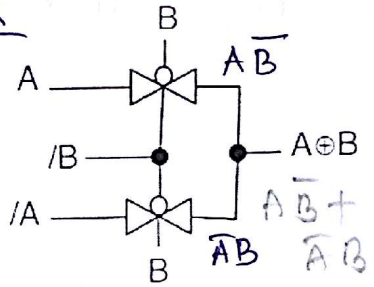
When S1=1, S1=0,
A and C turns ON, and,
When S0=1, S0=0,
A is selected and
appears at the output

$$\bar{S}_1 S_0 + C S_1 \bar{S}_0 + B \bar{S}_1 S_0 + A S_1 \bar{S}_0$$



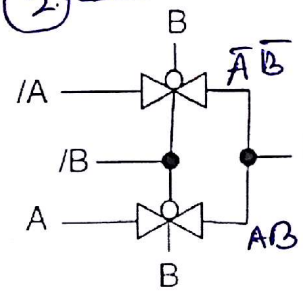
Transmission as a logic gates

① XOR



$A\bar{B} + \bar{A}B$

② XNOR

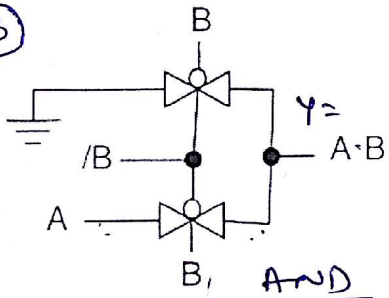


$AB + \bar{A}\bar{B}$

Not(A⊕B) =XNOR

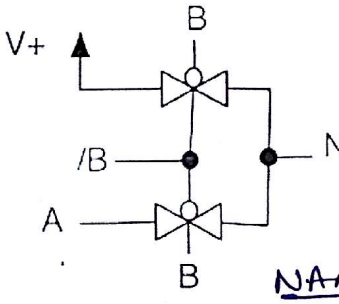
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

③



AND

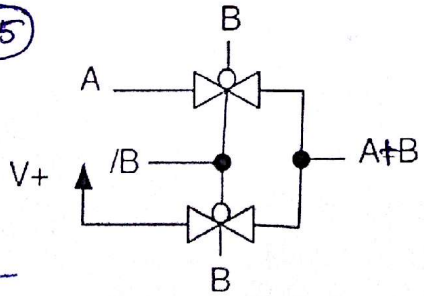
④



NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

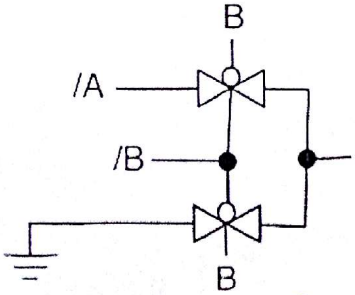
⑤



OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

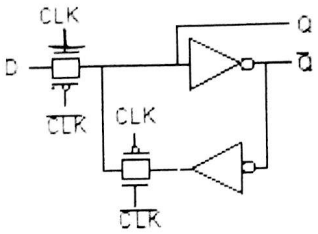
⑥

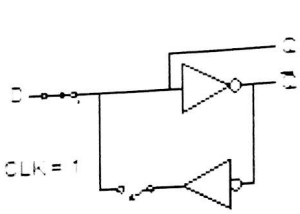


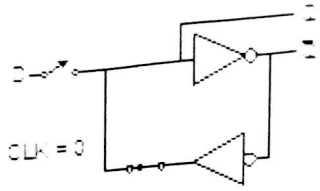
NOR

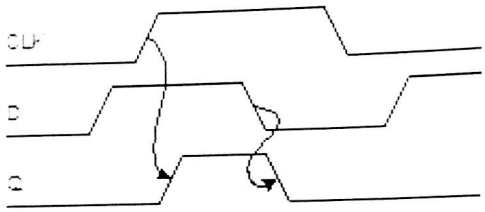
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

D Latch

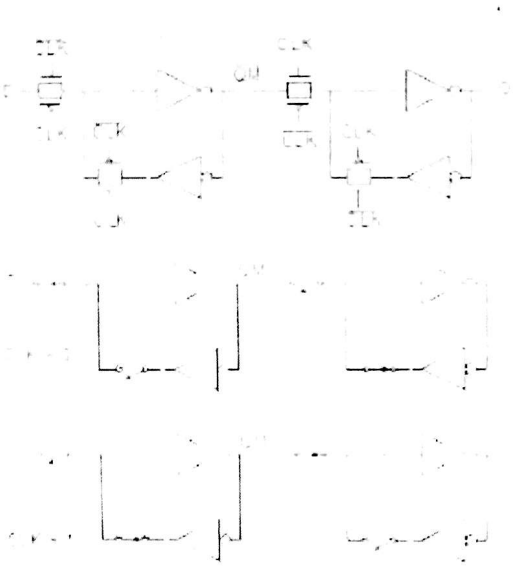




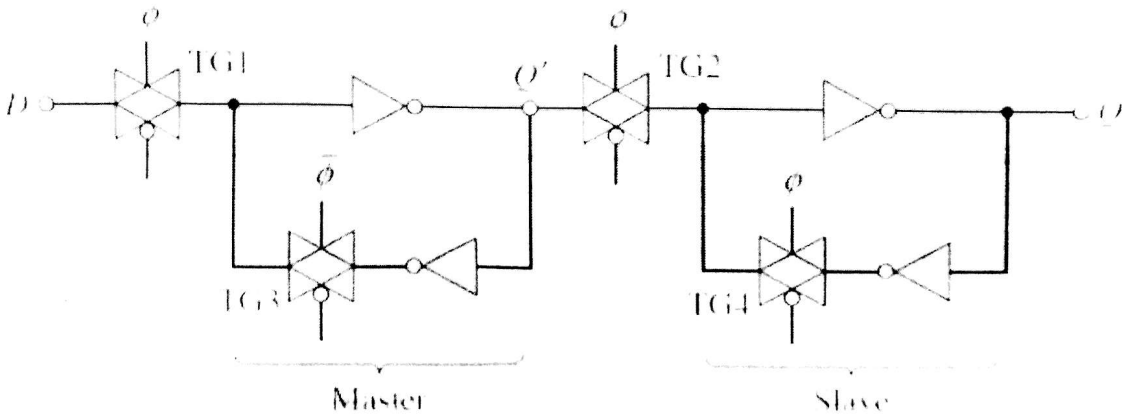




D-Flipflop



CLK	D	Q	$\overline{Q}$
1	1	↑	
1	0	0	
0	×	previous value	



D-Flipflop