DRC (Design Rule check)

objectives :—

* Design rule check is to achieve a high overall yield and reliable for the design.

* A Completed layout consists not only of the geometric representation of the design, but also data that provides support for the manufacture of the design.

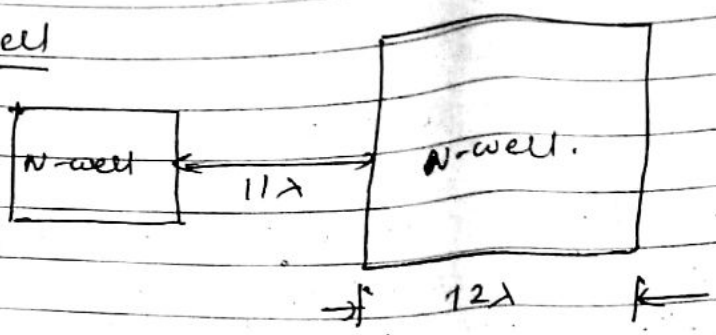
* DRC do not Validate that the design will operate correctly, they are constructed to verify that the structure meets the process constraints for a given design type and process technology.

* DRC software usually takes as input a layout in the GDSII Standard format and a list of rules specific to the semiconductor process chosen for fabrication. and it produces a report of design rule violation that the designer may or may not choose to correct.

* DRCs in Ic design include:

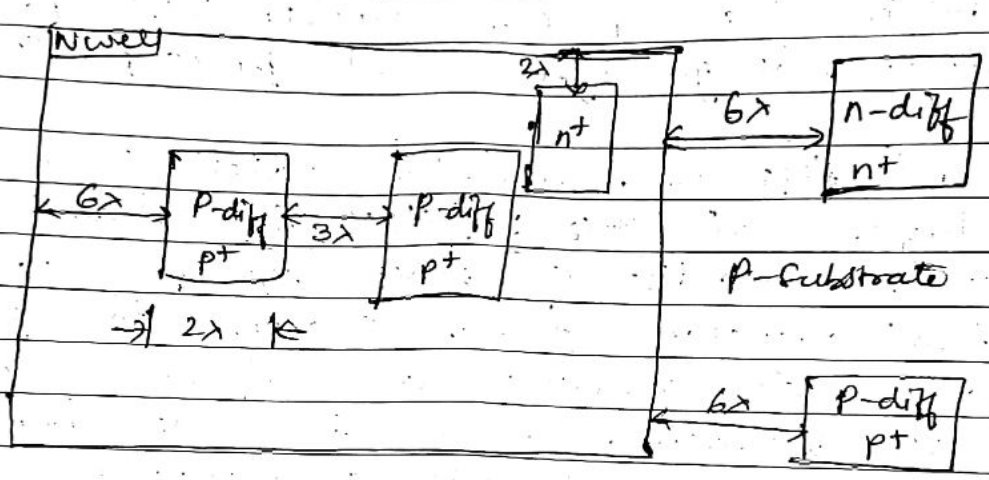
  1. Active to active spacing
  2. well to well spacing
  3. Minimum channel length of the Transistor
  4. Metal to metal spacing
  5. Minimum metal width.
  6. Metal fill density
  7. ESD & IO rules.
  8. Lambda based design rules.

(1) Nwell



minimum surface area of the well is $144\lambda^2$

(2) Design rules for n-diff and p-diff

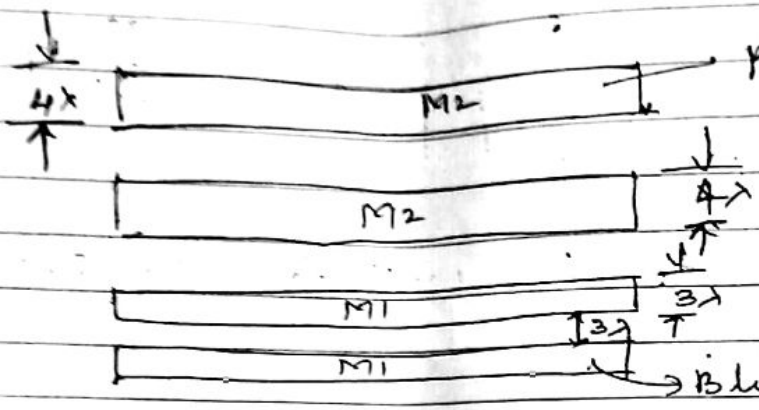


- minimum n^+-diff and p^+-diff width is 2λ.
- minimum spacing between two n^+-diff and p^+-diff is 3λ
- Extension of n-well after p^+-diff is 6λ
- minimum spacing between n^+-diff and n-well is 6λ
- Border of well after n^+ bias in n^+ well is 2λ
- Distance between n-well and p^+ bias is 6λ

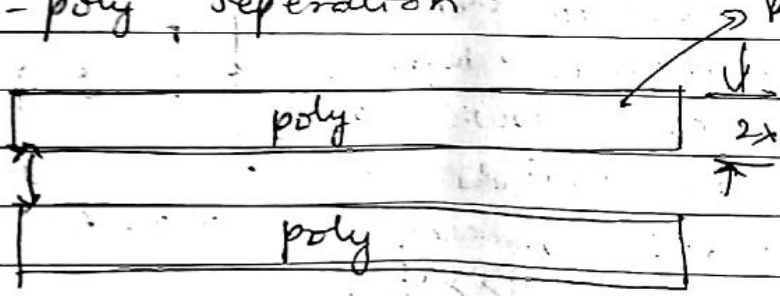
DRC for wires (conduction path)

Design rule specify the minimum distances and width of the wires to be followed in fabrication

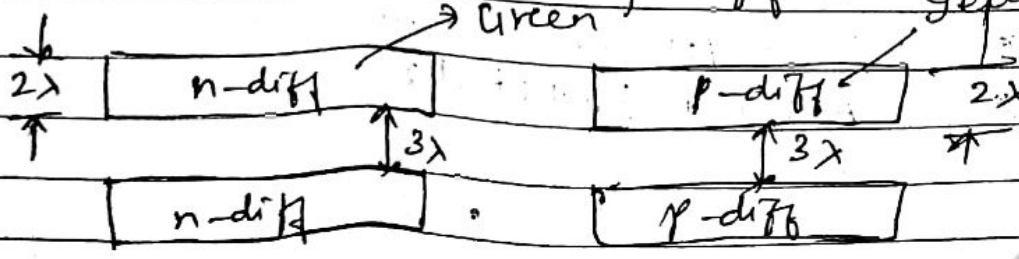
- For metal 1, min width should be 3λ and min seperation from another metal 1 wire is 3λ.
- For metal 2, min width should be 4λ and min seperation from another metal 2 wire is 4λ.



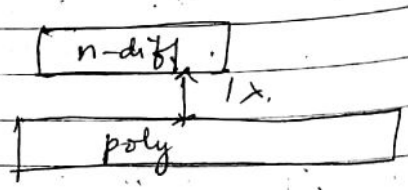
- For polysilicon wire the min width is 2λ and minimum seperation from another poly wire is 2λ. and it is called as poly-poly seperation.



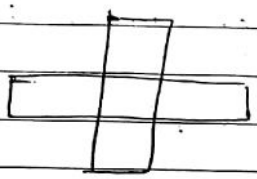
- If the wires are P & n-diff wires, min width of each wire is 2λ and min. seperation n-diff & anoth n-diff is 3λ. and same valid for p-diff.



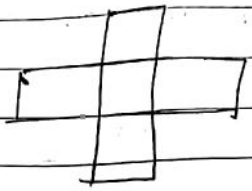
* minimum seperation between n-diff/p-diff wires and polysilicon wire is 1λ



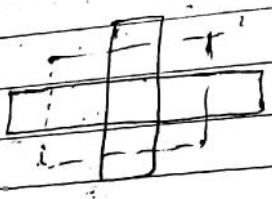
n-MOSFET



pMOSFET



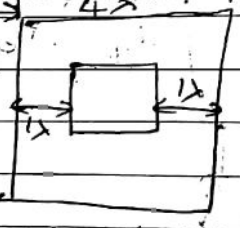
Depletion nMOSFET



Construction rules for transistors

Design Rules for Contact Cuts

* Contact cuts are also known as Via cuts. cuts are 2λ and 2λ dimension.
* They are used to connect two wires on different layers.
* The material on both layers to be connected extends 1λ in all directions making total contact size $4\lambda \times 4\lambda$



Contact cut types are

* n/p diffusion to polysilicon
* polysilicon to metal 1
* n/p diffusion to metal 1
* metal 1 to metal 2.

Stick Diagrams :-

Stick diagrams provide a top view of the patterns. It is simplified version of layout. Stick diagrams are useful for planning the layout and routing of integrated circuits.

In stick diagram, every line of a conducting material / layer is represented by a line of distinct colour. The colours allow us to trace signal flow paths through the conducting layers in a complex integrated circuit. physical design ~~org~~ planning, stick diagram before going to CAD tool save lot of time and energy.

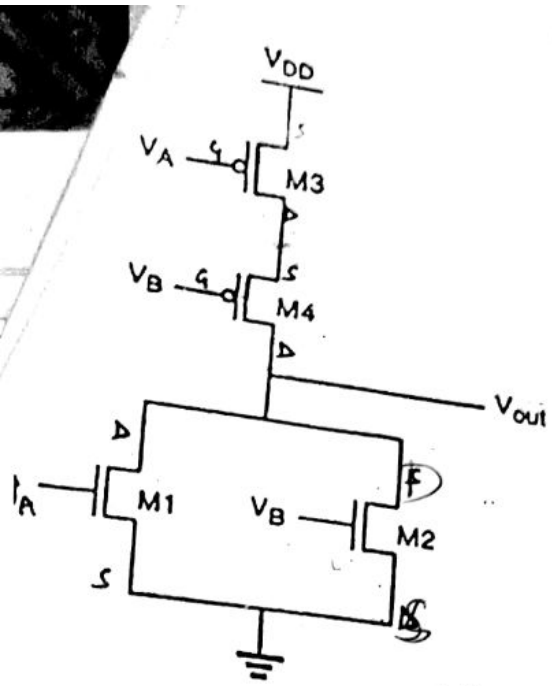
Stick diagram include:

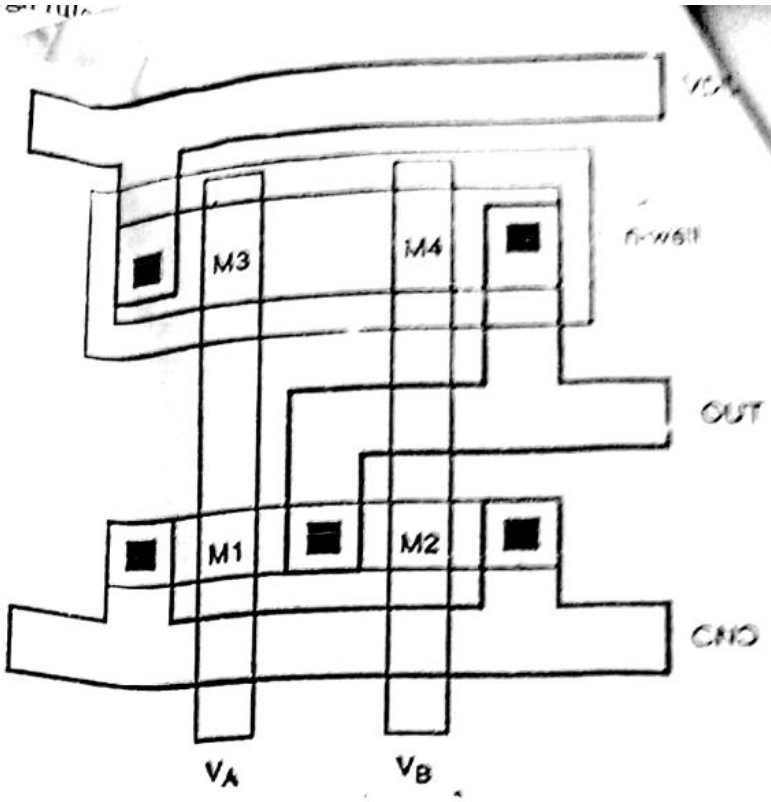
- It act as an interface between symbolic circuit and the actual layout.
- It does show all components / Vias.
- It shows relative placement of components.
- It goes one step closer to layout.
- and it helps to plan the layout & routing.

Stick diagram does not show

- Exact placement of components
- Transistor sizes.
- Wire lengths, wire widths, tub boundaries
- Any other low level details such as parasitic, etc

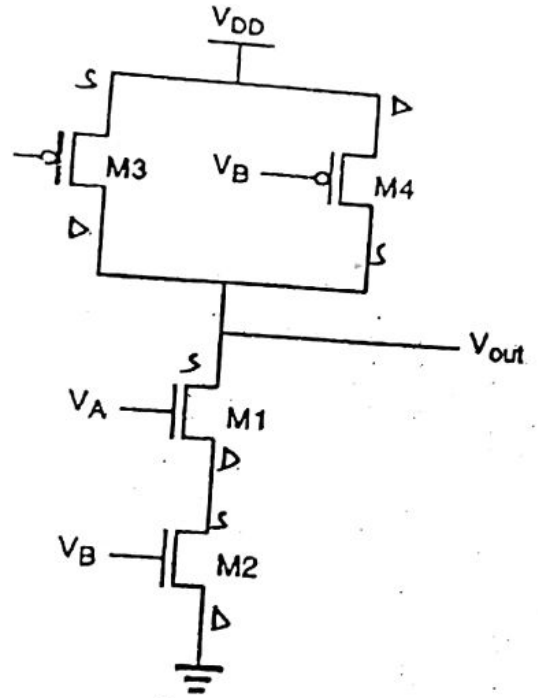
- It is a cartoon of a layout and it is used to solve routing problems.

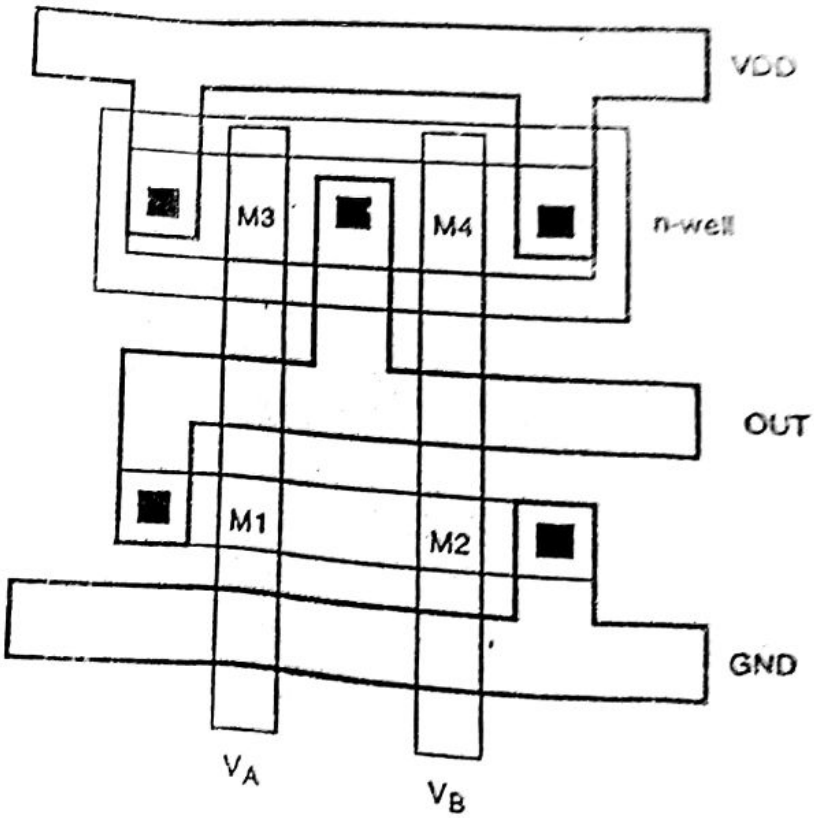




cmos Design

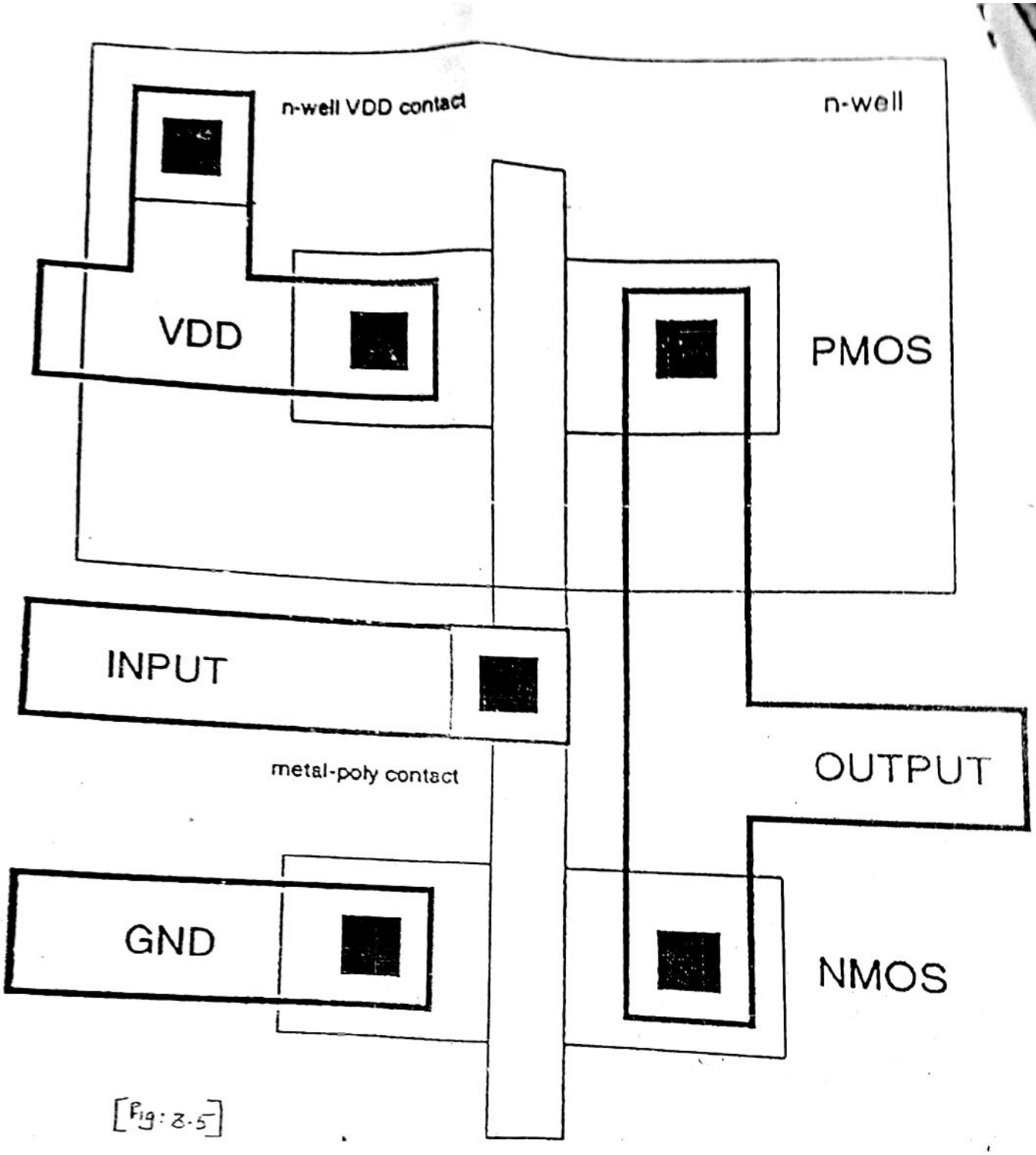
NOR





NAND

fig 3.7: Sample layout of NOR2 & NAND2 gate



[Fig: 3.5]

CMOS inverter

fig: 3.5! Complete Mask layout of CMOS Inverter