Basic CMOS Technology

The four CMOS Technologies are:

- n-well Process , p-well Process, twin tub process, silicon on insulator

1) n-well Process (refer to diagram)

A common approach is to start with a lightly doped p-type substrate (wafer), create the n-type well for p-channel device and build a n-channel transistor in the native p-substrate (fig-a).

The first mask defines n-well; p-ch transistor will be fabricated in this well. Ion implantation or deposition and diffusion are used to produce the n-well.

Next mask is "active" mask , it defines where areas of thin oxide are needed to implement transistor gates & allow implantation to form p- or n- type diffusion for transistor S/D regions (fig-b)

Channel stop is then completed. This uses p-well mask. It dopes the p substrate in areas where there are no n-transistors p+ using a photo resist mask. (fig-c) This prevents the conduction between unrelated transistors S/D.

Photo resist mask is striped leaving the previously masked SiO_2/SiN sandwich defining the active regions. The thick field Oxide is then grown in areas where the SiN layer is absent. (fig-d) This oxide construction is called LOCOS- Local Oxidation of silicon.

Defining poly gate involves covering the surface with poly and etching the required pattern. (fig-e)

An n+ Mask is then used to define the areas to be implanted with n+. Hence a thin oxide area exposed by the n-plus mask will become an n+ diffusion area (fig-f).

Instead of using one single diffusion or implantation step & mask to produce S/D regions, complicated structures are used such as LDD [lightly doped drain structure] as shown in [fig-g]

This consist of a shallow n-LDD implant that covers the S/D regions where there is no poly (normal S/D region)

A spacer oxide is then grown over polysilicon gate.

Next step used the complement of the P-plus mask although an extra mask is normally not needed. The absence of an n+ regions over a thin oxide area indicate that the area will be a p^+ diffusion or p-active P-active in n-well defines possible p-transistors & wires as shown in fig-h.

Contact cuts are then defined. This involves etching any SiO_2 down to surface to be contacted. (fig-i) This allows metal (next step) to contact diffusion regions or polysilicon regions.

> Metallization is then applied to the surface & selectively etched (fig-j) to produce circuit interconnections.

> As a final step, the wafer is passivated and openings to the bond pads are etched to allow for wire bonding. Passivation protects the silicon surface against the ingress of contaminants that can modify circuit behaviour in deleterious ways.

> The finished N-well process is shown in fig 3.8 (c)

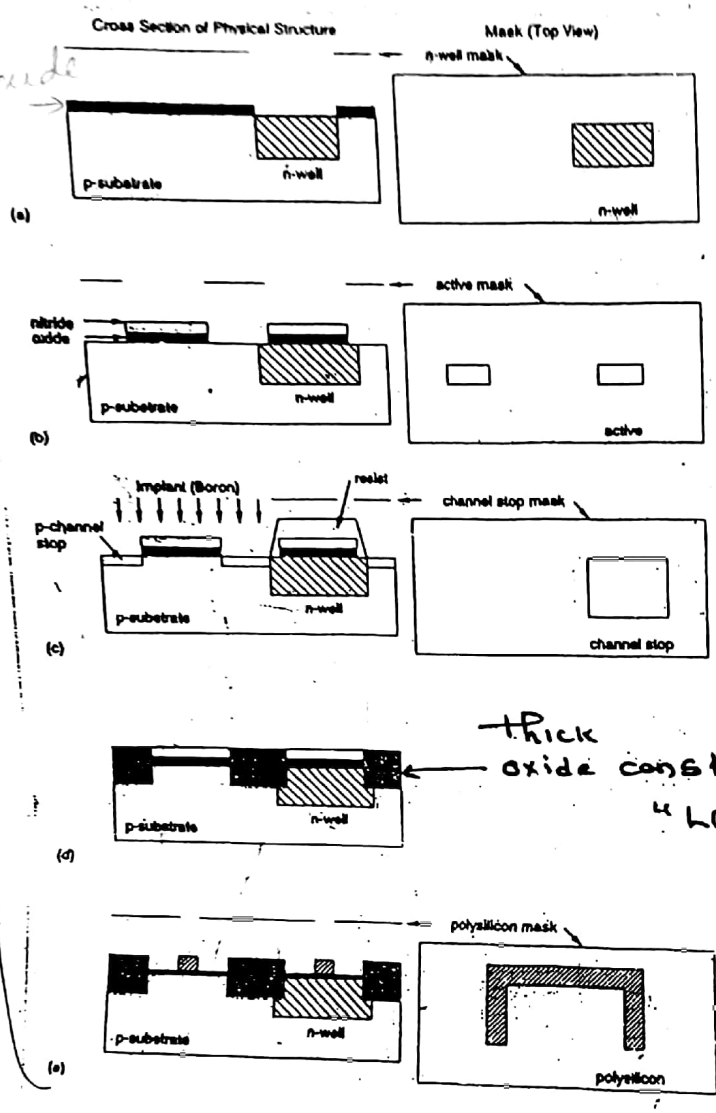
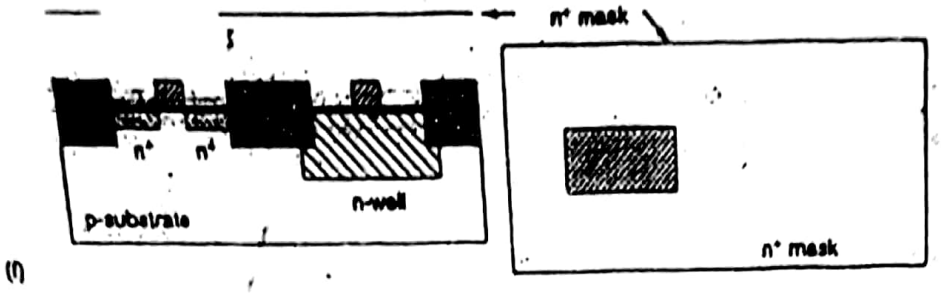


FIGURE 3.7 A typical n-well CMOS process

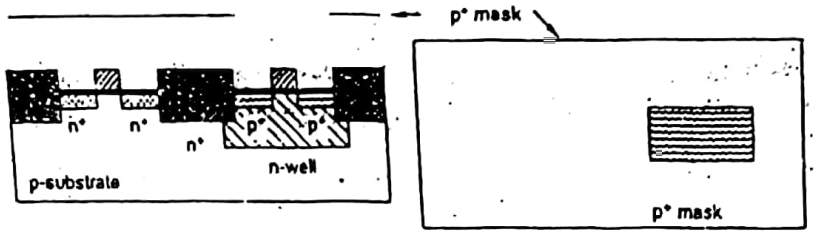
- The channel-stop implant is usually then completed. This uses the p-well mask (the complement of the n-well mask). It dopes the p-substrate in areas where there are no n-transistors p^+ using a photoresist mask (Fig. 3.7c). This, in conjunction with the thick field oxide that will cover these areas, aids in preventing conduction between unrelated transistor source/drains.



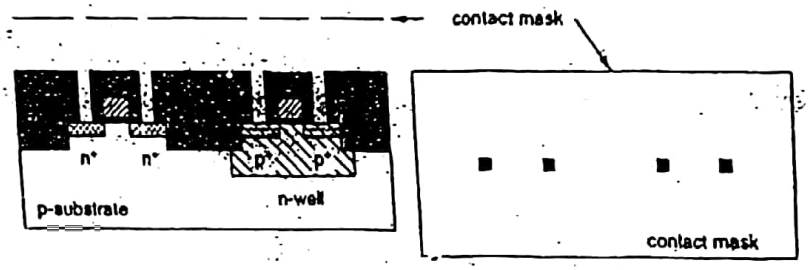
(f)

(g)

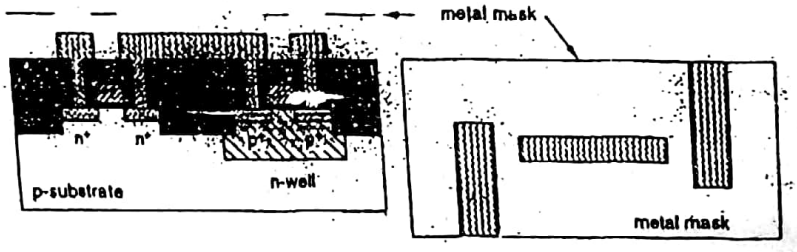
Lightly Doped dra



(h)



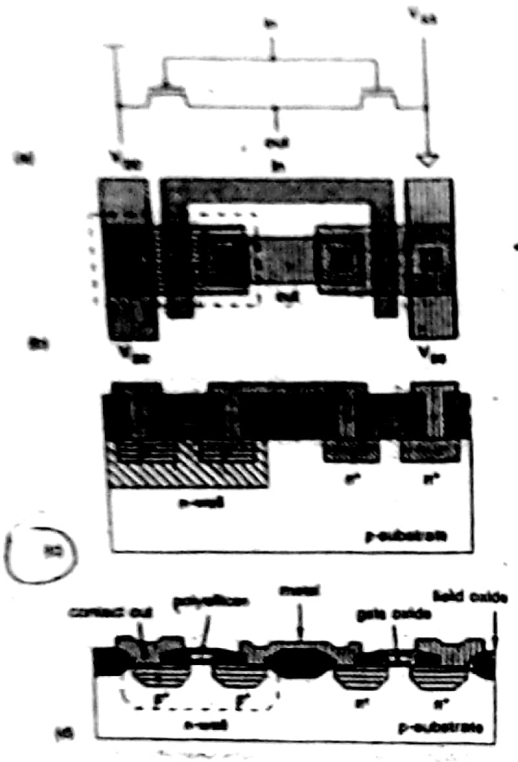
(i)



(continued)

(j)

- Following the channel-stop implant, the photoresist mask is stripped, leaving the previously masked SiO_2/SiN sandwich defining the active regions. The thick field oxide is then grown. This grows in areas where the SiN layer is absent. The oxide grows in both directions ver-



← layout

N-well process

P-type sub → -ve Vss

nWell → +ve supply

through Vdd Substra contact

>Topside connection preferred → as it r parasitic capacitance

FIGURE 3.8 Cross sectio of a CMOS inverter in an n-well process

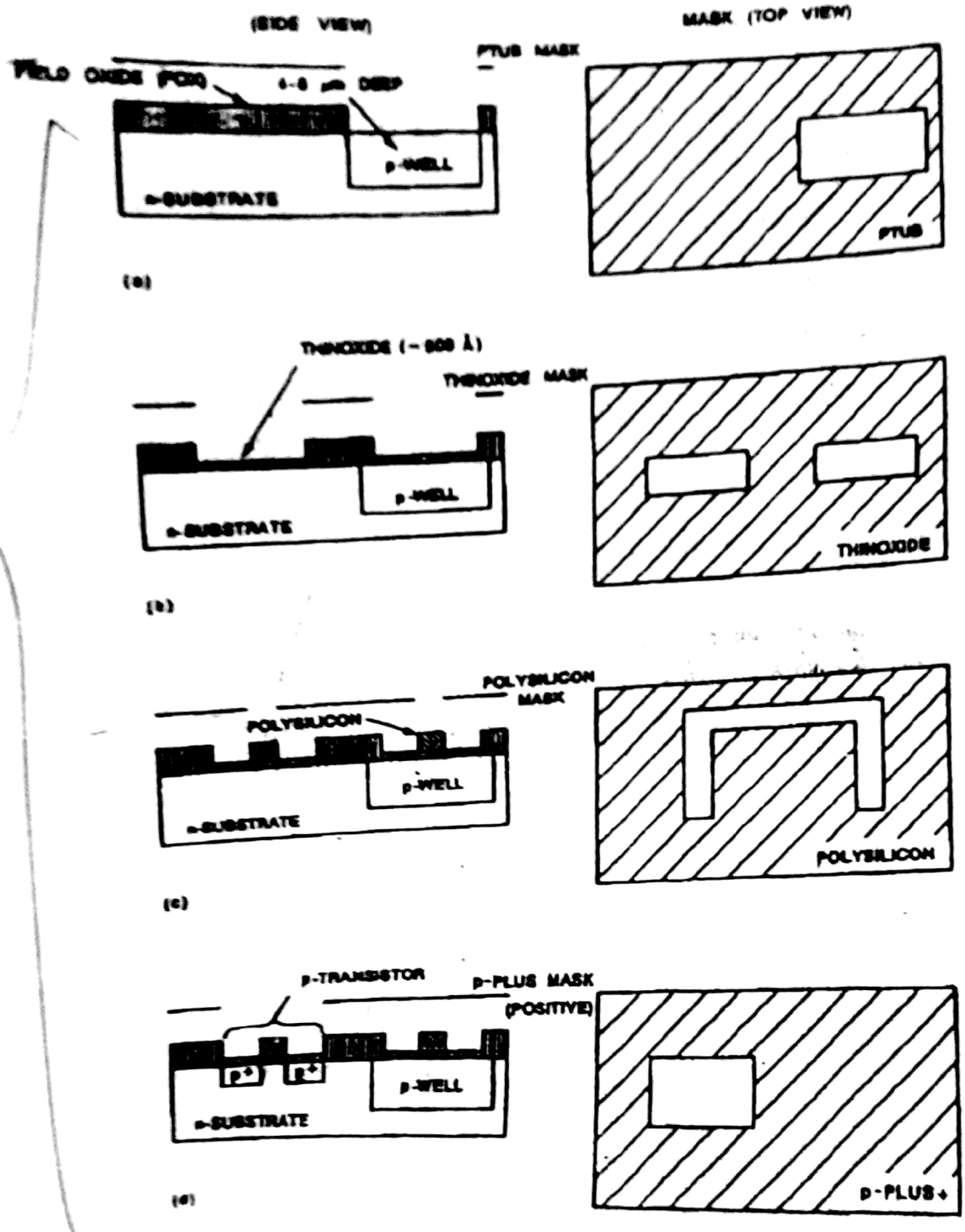
The P-well process

The P-well fabrication steps are similar to an n-well process, except that a p-well is implanted rather than an n-well.

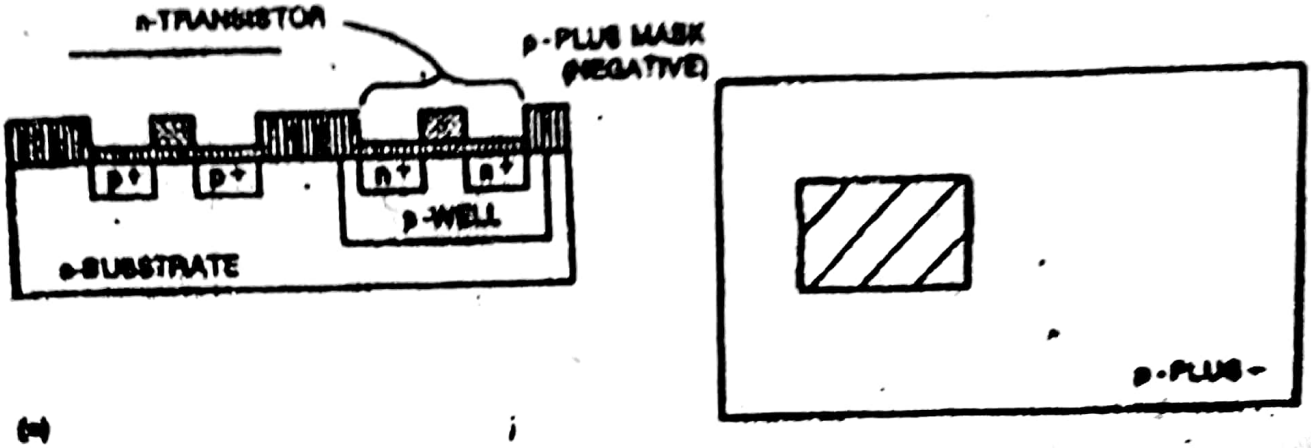
- first masking steps defines P-well regions.
- This is followed by low-dose boron implant driven in by a high temperature step for the formation of P-well.
- The well depth is optimized to ensure against n-substrate to n^+ diffusion breakdown, without compromising P-well to p^+ lateral
- Next step to define devices & other diffusions;
  - to grow field oxide
  - contact cuts
  - Metalization
- A p-well mask is used to define p-well regions, as opposed to an n-well mask in an n-well process.
- A p^+ mask is used to define the P-channel transistor & V_{SS} contacts.

P-Well CMOS PROCESS

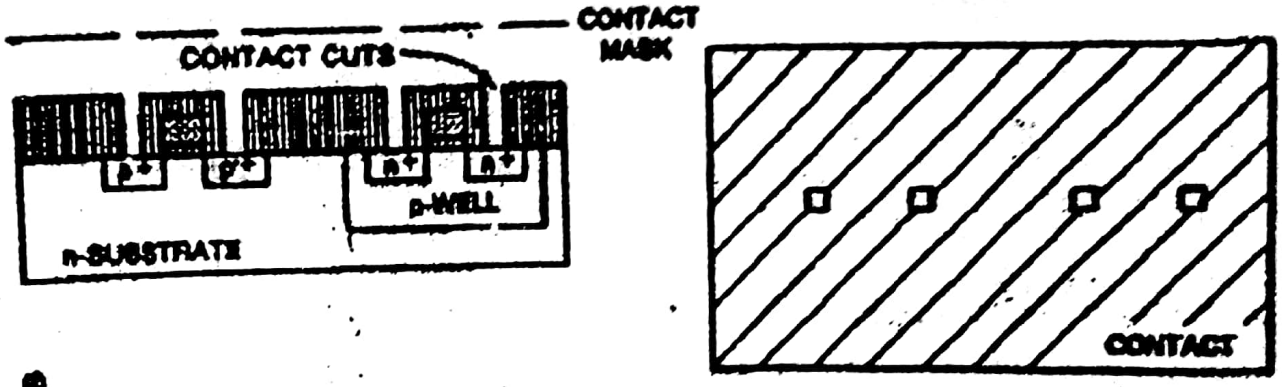
CROSS SECTION OF PHYSICAL STRUCTURE



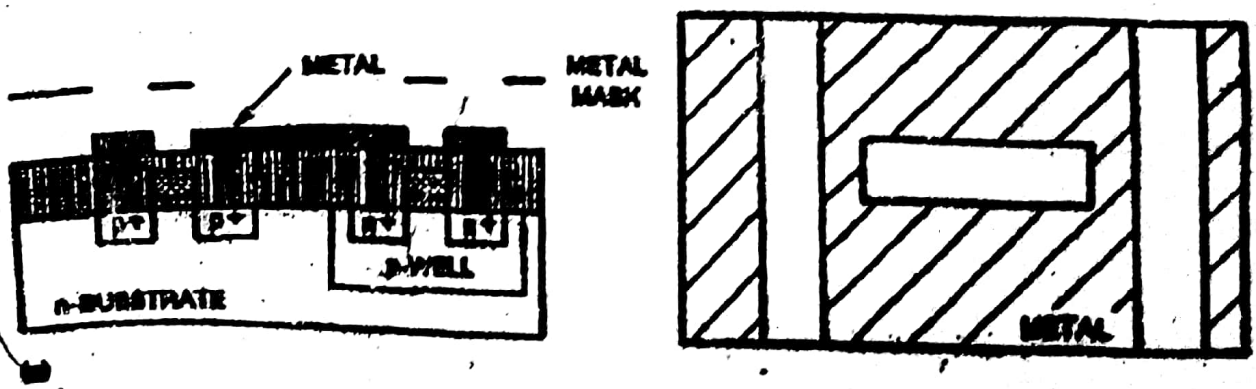
Typical p-well CMOS process steps with corresponding masks required



(a)



(b)



(c)

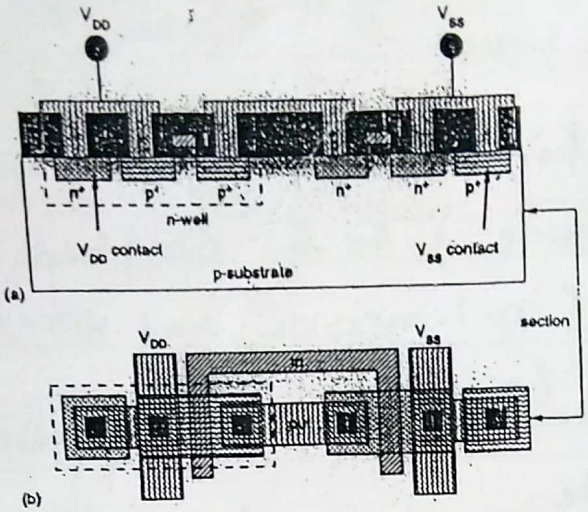


FIGURE 3.9 Substrate and well contacts in an n-well process

Typical processing steps. [P-well CMOS Process]

1) PTUB Mask : Defines the areas in which the deep P-well diffusion are to take place.

2) Thinoxide Mask : Defines thinox regions, namely those areas where the thick oxide is to be stripped and thin oxide grown to accomodate P- & n-transistor and wires.

3) Polysilicon Mask : Used to pattern the polysilicon which is deposited after the thin oxide.

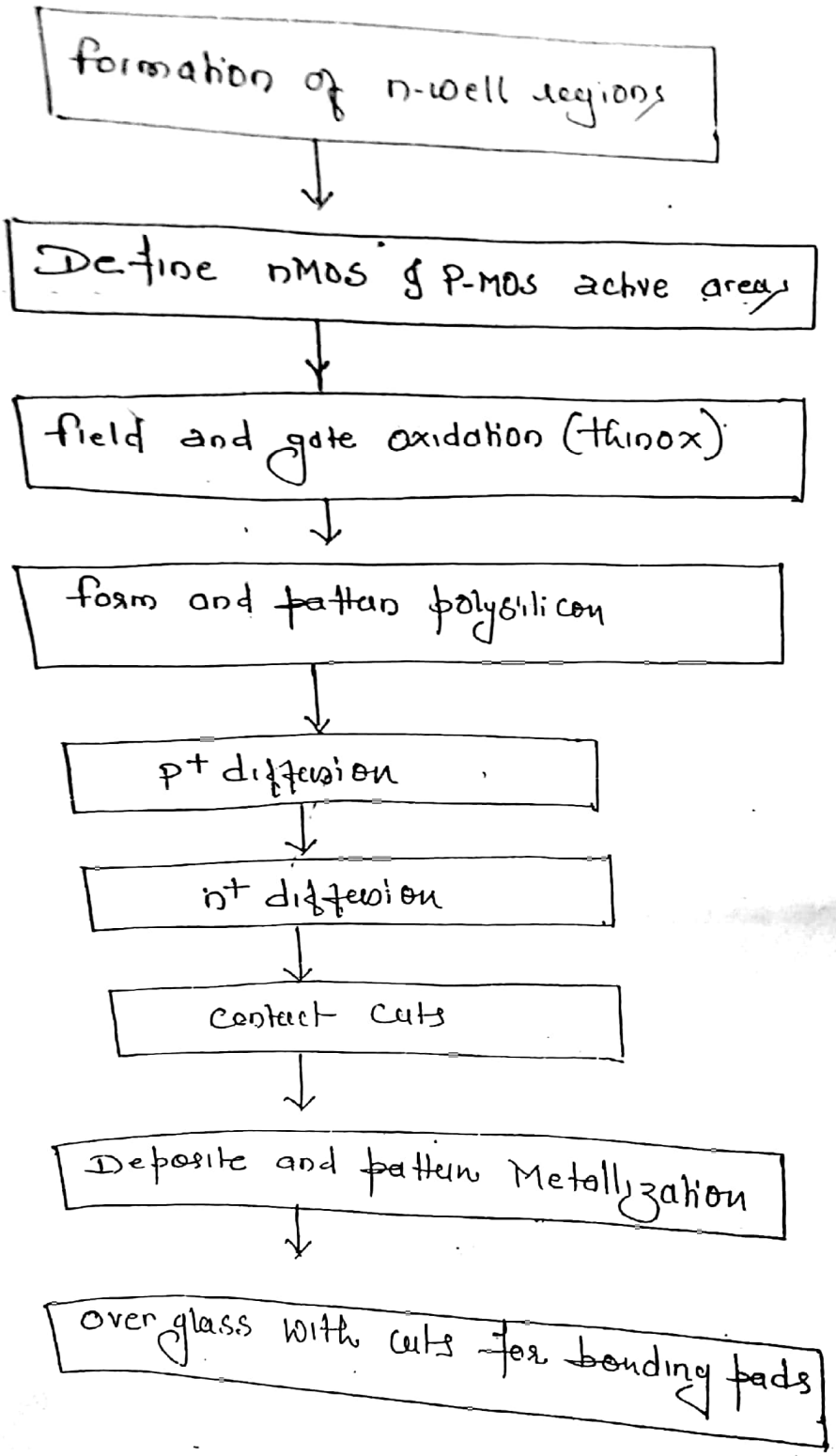
4) P-plus Mask : A p-plus mask is used to define all areas where p-diffusion is to take place.

5) P-plus Mask (negative) :- This is usually performed using the negative form of the p-plus mask and defines those areas where n-type diffusion is to take place.

6) Contact Mask :- Used to define contact cuts.

7) Metal Mask : The metal layer pattern is defined by this mask.

Main Steps Involved in typical n-well process



Twin-Tub Process

> Twin tub CMOS technology provides basis for separate optimization of the P-type and n-type transistors, thus making it possible for threshold voltage, body effect & the gain associated with n- and p-devices to be independently optimized.

> Generally, starting material is either an n^+ or p^+ substrate with a lightly doped epitaxial or epilayer which is used protection against latchup.

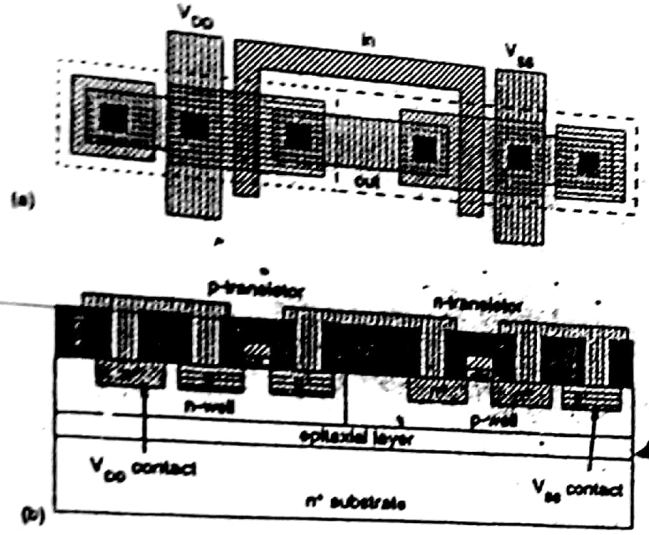


FIGURE 3.10 Twin-well CMOS process cross section

ness with accurately determined dopant concentrations distributed homogeneously throughout the layer. The electrical properties of this layer are determined by the dopant and its concentration in the silicon. The process sequence, which is similar to the n-well process apart from the tub formation where both p-well and n-well are utilized, entails the following steps:

- Tub formation.
- Thin-oxide construction.
- Source and drain implantations.
- Contact cut definition.
- Metallization.

Since this process provides separately optimized wells, balanced performance n-transistors and p-transistors may be constructed. Note that the use of threshold adjust steps is included in this process. These masks are derived from the active and n-plus masks. The cross-section of a typical twin-tub structure is shown in Fig. 3.10. The substrate contacts (both of which are required) are also included.