

Unit 4

(20)

Syllabus:

**Testing:** Test procedure, Design for Testability (DFT) Scan - Based test, Boundary-scan design, Built-in self-test (BIST), Automatic Test-Pattern generation (ATPG), fault models, fault simulation.

**Course Outcome:**

ETC/ECE 5.5.6	Ability to understand the fabrication of MOS and compute the test pattern which will detect Faults in a given integrated circuits
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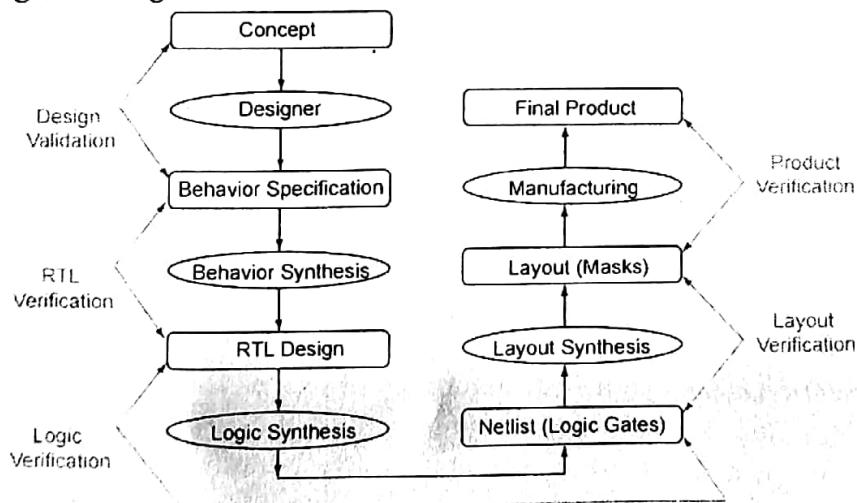
**What is testing and Explain it.**

Testability verifies correctness of manufactured hardware, it is a manufacturing test. The chip must be exercised to demonstrate that no manufacturing defects render the chip useless.

Three factors conspire to create considerable difficulties for the test engineer and for design testing for his/her own prototypes:

- Complexity of VLSI system
- The fact that entire surface of the chip, other than over the pads, is sealed by layer and thus circuit probe for monitoring or excitation
- There is no way to modify circuit when under test to make it work as required.

Thus chip design/fabrication can very costly, both in terms of money and time; lack thought at design stage may mean it cannot be properly tested at all. Design for testability (DFT) is an essential part of good design.



After the chip is fabricated it is tested for manufacturing defects. The chip designer must verify or validate the design to ensure the circuit performance. Verification or validation is a different process than testing.

Verification is related to formal proof of correctness and validation is a technique that increases confidence in correctness.

Testability verifies correctness of manufactured hardware, it is a manufacturing test. The chip must be exercised to demonstrate that no manufacturing defects render the chip useless.

### **Explain in detail Classification of manufactured testing .**

Manufacturing test fall under number of categories depending upon intended goal:

#### 1. Diagnostic test

- » used in chip/board debugging
- » defect localization

#### 2 “go/no go” or production test or functional test

- » Used in chip production
- » Manufactured component is functional or not

#### 3. Parametric test

- »  $x \in [v,i]$  versus  $x \in [0,1]$
- » check parameters such as NM,  $V_t$ ,  $t_p$ , T

- **Diagnostic test:** It is used in chip debugging or board debugging and tries to detect failing part, identify and locate the offending faults.
- **Functional Test:** This is also called as go/no go test or production test. It determines whether the component is functional or not. As this test must be executed on every manufactured die and has a direct impact on the cost, it must be simple and shift as possible.
- **Parametric test:** it checks on a number of parameters of the design under variety of working conditions, this requires different setup from the others where the signals of ‘0’ or ‘1’ have to be considered. They are divided as static (DC) and dynamic (AC) tests.

### **Explain Manufactured Testing Procedure:**

**Typical Manufactured testing procedure takes places as follows:**

- The predefined test patterns are loaded into the tester that provides excitation to device under test (DUT) and collects the corresponding responses.
- The test pattern are defined in a test program (e.g. test bench in VHDL) that describe the waveforms to be applied, voltage levels, clock frequency and expected response.
- A new part is fed automatically into the tester. The tester executes the test program, applies the sequence of the input pattern to the DUT and compares the obtained response with expected one.
- If difference in output is observed, the part is marked as faulty and the probes are automatically moved to next die on the wafer. During the scribing process that divides wafer into dies spotted parts will automatically discarded.

- In the last step the DUT is removed from the testing board and placed into the good or faulty bin depending upon the outcome of the output. The entire process is completed in few seconds and thus making it possible for the tester to handle thousands of parts in an hour.

## What is Design for Testability (DFT) and need of

*Design for testability* (DFT) refers to those design techniques that make test generation and test application cost-effective.

It is used to indicate that we need to build fault models to test the chip, which comes off the manufacturing line called as the manufacturing test.

### Need of Testability:

- Defects can be catastrophic (contamination that destroys every transistor on the wafer).
- Debugging cost increases around chip to board level then to system level.
- Need of testing within short time for timely delivery to consumers.

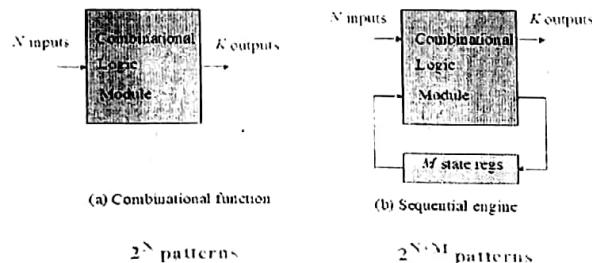
To overcome such difficult issues, DFT has become even more critical.

### What are the issues in Design for Testability?

#### Describe Exhaustively Testing

Issues in design for Testability:((Combinational and sequential circuits under test):

##### 1) Combinational devices under test (CDUT):



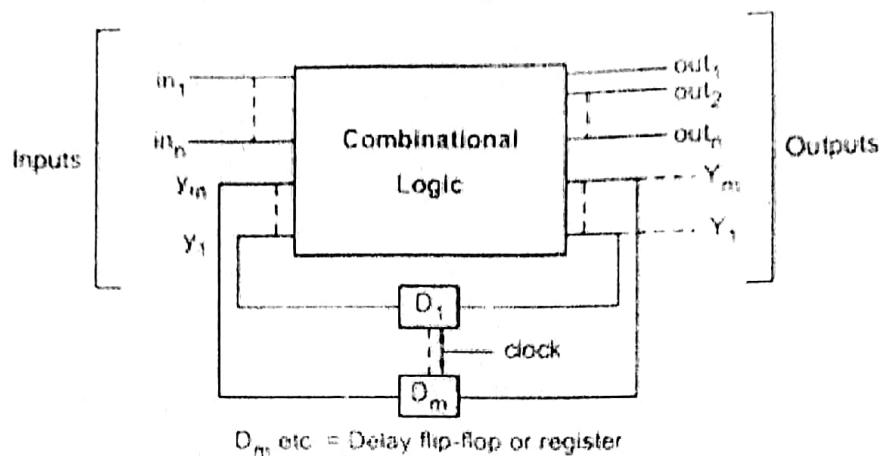
The correctness of the combinational logic modules can be validated by exhaustively applying all possible input patterns and observing the responses. A circuit having N inputs has  $2^N$  input combination which can be generated by N-bit counter to satisfy controllability and then observe the outputs and check for observability. But this is possible only when N is comparatively small. If the application and observation takes 1μsec, the total tests of the module 1 sec if combinations are 1 million.

Number of inputs (N)	Input combination	Total Test time
20 inputs	$2^{20}$	$2^{20} \times 10^{-7} \geq 7 \text{ minutes}$
40 inputs	$2^{40}$	$2^{40} \times 10^{-7} \geq 30 \text{ hours}$
64 inputs	$2^{64}$	$2^{64} \times 10^{-7} \geq 57400 \text{ years}$

Therefore test times are highly impractical and hence other techniques are used for testing cause as the number of inputs increase the time requirement is more.

## 2) Sequential Device Under test (SDUT):

The outputs of the circuit depend not only upon the inputs applied and also upon the values of the previous state. To test this finite machine state (FSM) requires the application of  $2^{M+N}$  input patterns; where M is no of state registers and N is the number of inputs.



There are m feedback variables that make the state vector and decide the maximum number of the finite states that the circuit can assume. Usually, the next state the machine would assume and its output are both functions of current state and independent inputs. Generally, the delay elements are associated with the feedback path. In case of clocked or synchronous the delay elements are flip-flops while in synchronous they may be due to circuit propagation delays. The generation of the test signals/ test patterns is not very easy because they not only have to be logically correct, but also occur at correct time with respect to other signals.

An alternative approach is required as the above two are not possible if the number of inputs increase, a more feasible testing approach is based on:

- An exhaustive enumeration of all possible input patterns contain a substantial amount of redundancy i.e. single fault in the circuit covered by a no. of input patterns.
- A substantial reduction in the number of patterns can be obtained by relaxing the condition that all faults must be detected so test procedures only attempt 95%-99% fault coverage.
- **Design test approach for combinational logic?**

(or)

**Define Design for Testability (DFT)? Write short notes on Controllability and Observability?**

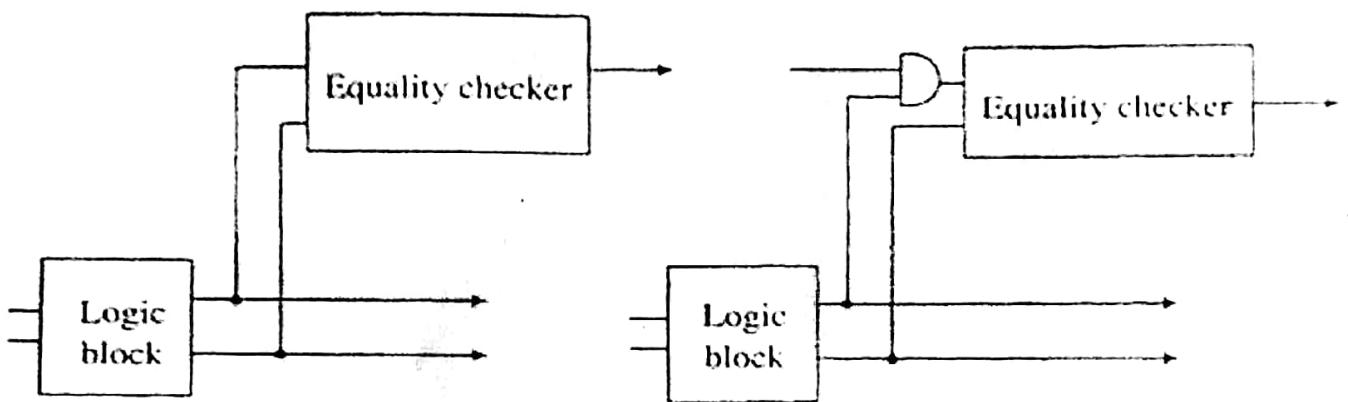
- Design for Testability (DFT) is basically meant for providing a method for testing each and every node in the design for structural and other faults.
- Higher the number of nodes which can be tested through the targeted number of patterns, greater is the test coverage of the design.

- For this to be possible, every node in the design has to be controllable and observable.

### Controllability:

- It measures the ease of bringing a circuit node to a given input pin and a node can easily be controllable, if it can be brought to any condition with only a single input vector.
- A single node (or circuit) with low controllability needs a long sequence of vectors to be brought to a desired state.
- A high degree of controllability is desirable to test design. Controllability refers to the ability to apply test patterns to the inputs of sub-circuit via primary inputs; it is present at the input side.

### Example:

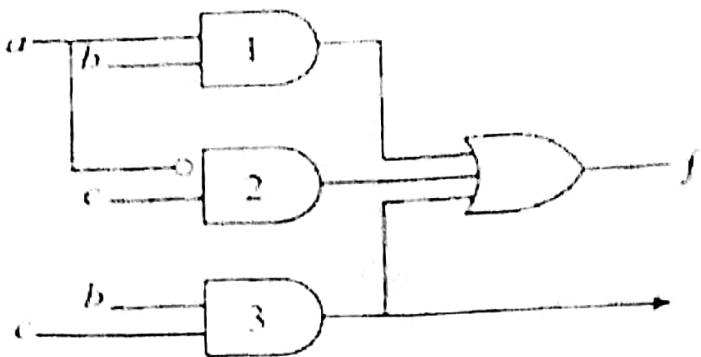


We can consider these as the two basic principles of DFT which are to be followed in order to have the maximum test coverage possible through minimum number of patterns.

There are two key concepts in designing for testability: *controllability* and *observability*. Controllability refers to the ability to apply test patterns to the inputs of a subcircuit via the primary inputs of the circuit. For example, in Fig. 5.1(a) if the output of the equality checker circuit is always in the state of *equal*, it is not possible to test whether the equality checker is operating correctly or not. If a control gate is added to the circuit (Fig. 5.1(b)), the input of the equality checker

### Observability:

- It measures the ease of observing the value of a node at output pins. A node with high observability can be monitored directly on the output pins.
- A node with low observability needs a number of cycles before its state appears on the outputs.
- A complex circuit with limited number of output pins, a testable circuit should have high observability.
- Observability refers to the ability to observe the output response of a sub circuit via primary outputs



Observability refers to the ability to observe the response of a subcircuit via the primary outputs of the circuit or at some other output points. For example, in Fig. 5.2 the outputs of all three AND gates are connected to the inputs of the OR gate. A stuck-at-0 fault at the output of the AND gate 3 is not detectable because the effect of the fault is masked and cannot be observed at the primary output. To enhance the observability, we must observe the output of the gate separately as shown.

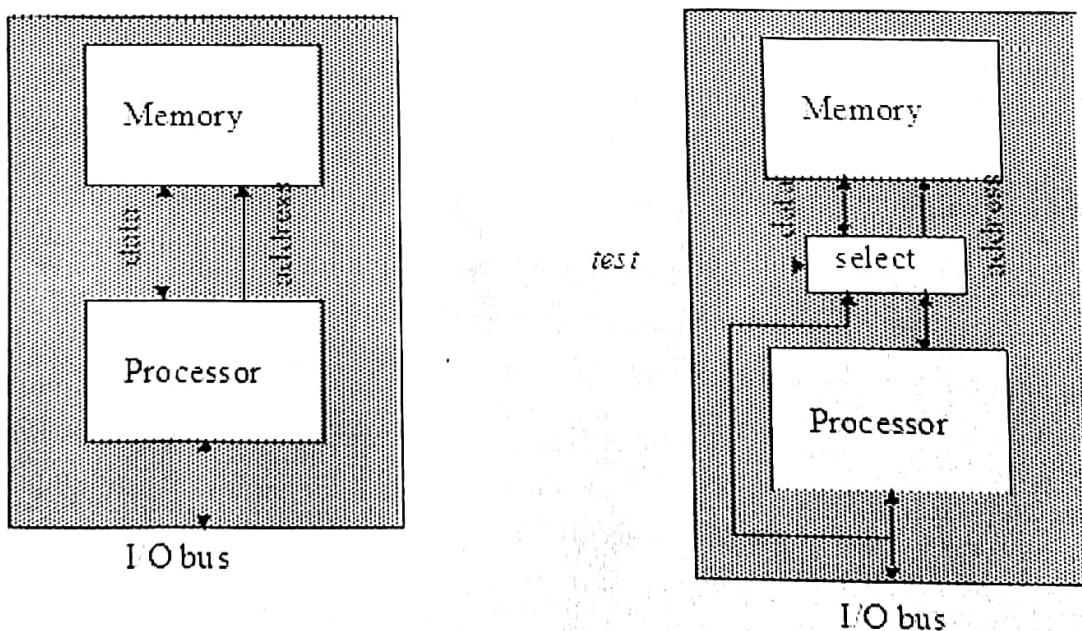
In general, the controllability/observability of a circuit can be enhanced by incorporating some control gates and input lines (controllability), and by adding some output lines (observability).

## Test Approaches for the sequential modules

- 1) Ad-hoc testing
- 2) Scan-based Test
- 3) Self-Test

### 1) Ad-hoc testing

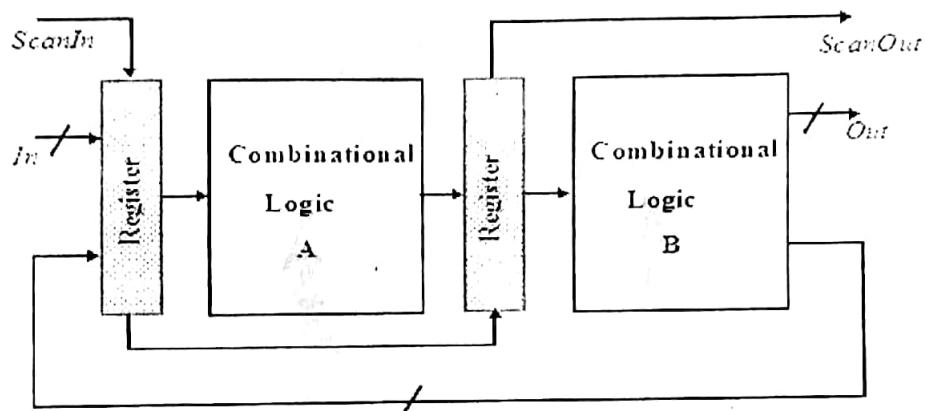
- Ad Hoc testing:



- It combines a collection of tricks and techniques that can be used to increase the observability and controllability of a design that are applied in a dependent fashion.

- Design for low testability. It is a simple processor with its data memory is only accessible through the processor. Writing and reading of data value in and out of a single memory position requires a number of clock cycles
- The controllability and observability of memory can be dramatically improved by adding (select lines) multiplexers on the data and address bus as shown in the above figures.
- During normal operation mode, these selectors direct the memory ports to the processor. During Test Mode the data and address ports are connected directly to I/O pins and testing the memory can proceed more efficiently.
- Ad Hoc testing approach also includes the portioning of the machines, addition of extra test points, provision of reset states and introduction of test buses and most of the approaches depend upon application and architecture.

## 2) Scan Based Test (Serial Scan List):



### **Objective:**

- Simple Read/Write access all or subsequent storage elements in a design
- Direct control of storage elements to an arbitrary value (0 or 1)
- Direct observation of storage elements and hence internal state of circuit.
- The registers are modified to support two operation modes:
  - In normal mode they act as a N-bit wide clocked registers
  - In test mode the registers are chained together as single shift register

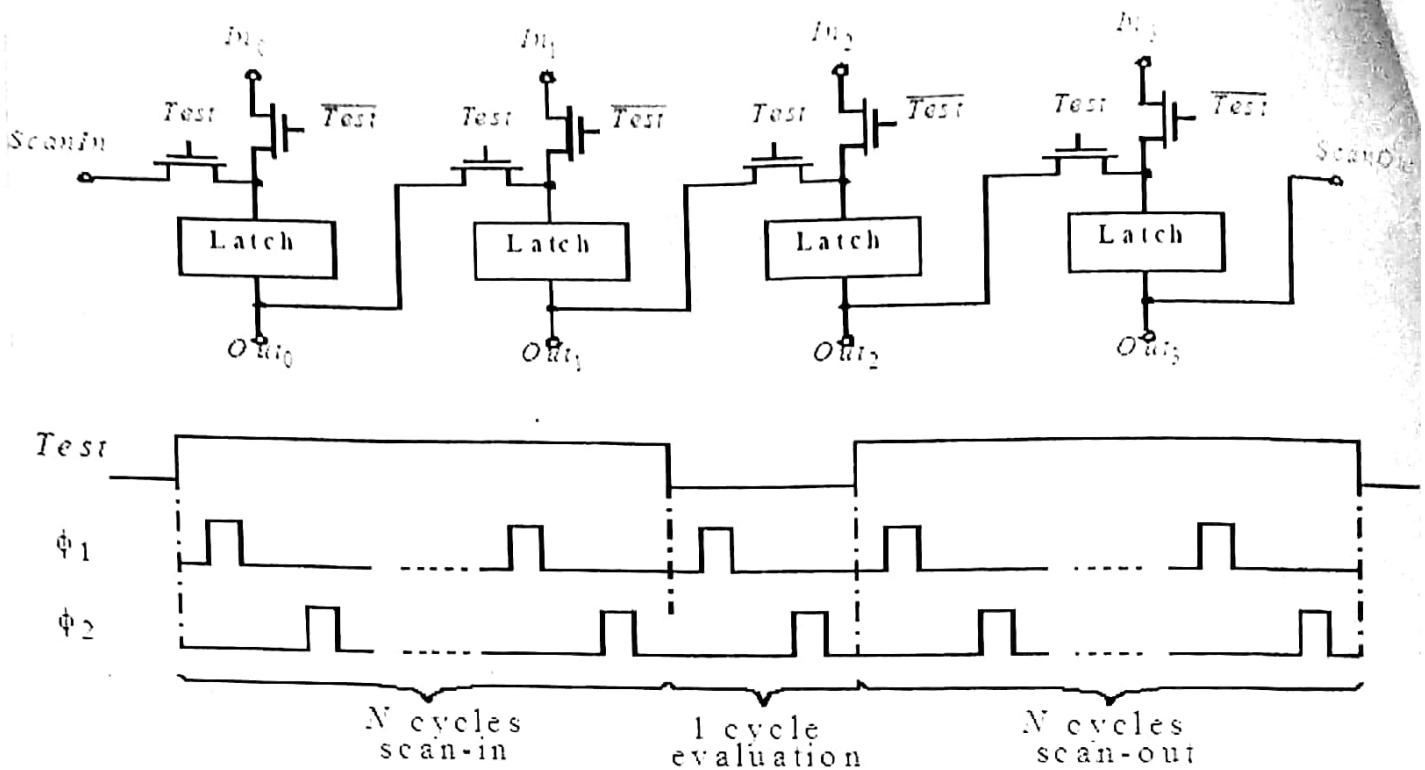
The method of testing a circuit with the scan path is as follows:

1. Set test mode signal, flip-flops accept data from input scan-in
2. Verify the scan path by shifting in and out test data
3. Set the shift register to an initial state
4. Apply a test pattern to the primary inputs of the circuit
5. Set normal mode, the circuit settles and can monitor the primary outputs of the circuit
6. Activate the circuit clock for one cycle
7. Return to test mode
8. Scan out the contents of the registers, simultaneously scan in the next pattern

### **Advantages:**

- This approach gives a minimal overhead
- The serial nature of the scan chain reduces the routing overhead
- Enhanced controllability and observability

### a) Registers extended with serial Scan-based Test — Operation



### b) Level Sensitive Scan Design (LSSD):

Level sensitive means that the sequential network is designed so that when input change occurs the response or output is independent of the component and wiring delays with network.

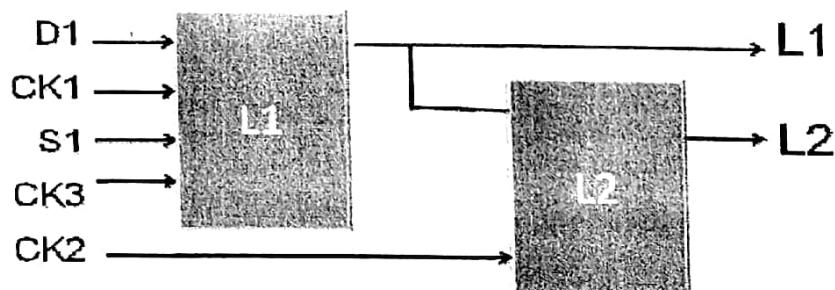


Figure 8.14: Level sensitivity scan design

Here clock 1 and 2 (CK1 and CK2) control normal operation and CK3 and CK2 control scan path movements through SRL (shift register latches) L<sub>1</sub> and L<sub>2</sub> and D1 is the normal data input pin. S1 is the scan data pin.

The level sensitive aspect means that the sequential network is design so that when an input changes occurs, the response independent of the component and wiring delays within the network. It consists of two latches L<sub>1</sub> and L<sub>2</sub>.

In normal operation mode signal D1,L1, CK1 serves as latch input, output and clock respectively. CK2 and CK3 are low in this mode

In scan mode S1, SO serves as scan in and scan output respectively. CK1 is low during this interval and CK2 and CK3 are non-overlapping two phase test clocks.

## Advantages:

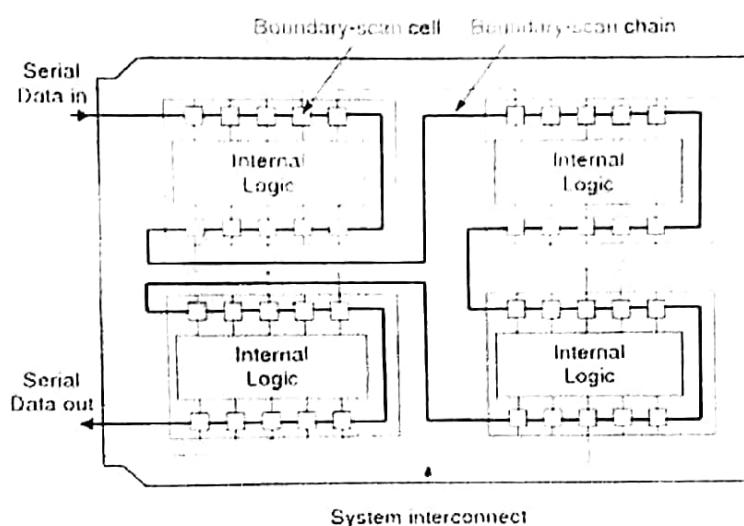
- The circuit operation is independent of the dynamic characteristics of the logic elements- rise and fall time and propagation delays
- ATP generation is simplified since the tests need only be generated for a combinational circuit
- LSSD methods, when adopted in design, eliminate hazards and races so, greatly simplifies test generation and fault simulation

## Advantages

- Circuit operation is independent of dynamic characteristics of the logic elements
- ATP generation is simplified
- Eliminate hazards and races
- Simplifies test generation and fault simulation

## C)Boundary Scan Test (BST) Industry Standards:

It is design under test (DUT) technique for PCB design and Board Testing.



This is a technique involving scan path and self-testing to resolve the problems associated with the testing boards carrying VLSI circuits and/or surface mounted devices (SMDs). Printed circuit boards (PCBs) are becoming very dense and complex, so most test equipment cannot guarantee good fault coverage.

Boundary scan is standardised to ensure compatibility between different vendors (e.g. IEEE 1149). It connects the input-output pins of the components on a board into serial data chain. During normal operation the boundary scan pads acts as normal input output devices. In test mode, vectors can be scanned in and out of the pads providing controllability and observability at the boundary of the components. Various control modes allow for testing the individual components as well as board components.

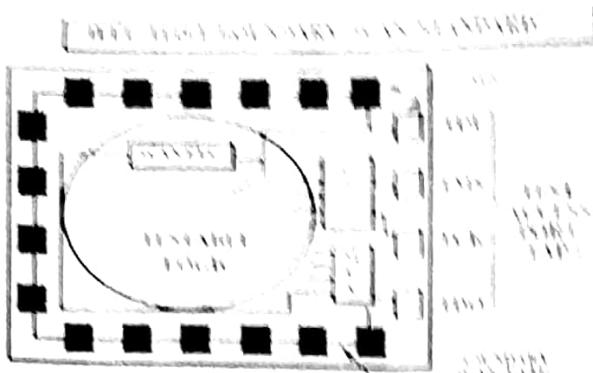


Figure 8.15. Boundary Scan Test (BIST)

**Boundary scan is accessed through five pins:**

TCK:	test clock
TMS:	test mode select
TDI:	test data in
TDO:	test data out
TRST*:	test reset (optional)

### Merits of Boundary Scan Check:

- Increased fault coverage system
- The boundary scan check is much more time efficient i.e. time required is less as compared to other systems
- The process of boundary scan is very simple
- In built scan path and self test makes it more accurate and efficient

### **Random Scan Method:**

- The scan function is implemented like a random access memory (RAM)
- All flip-flops form a RAM in scan mode
- A subset of flip-flops can be included in the RAM if partial scan is desired
- In scan mode, any flip-flop can be read or written

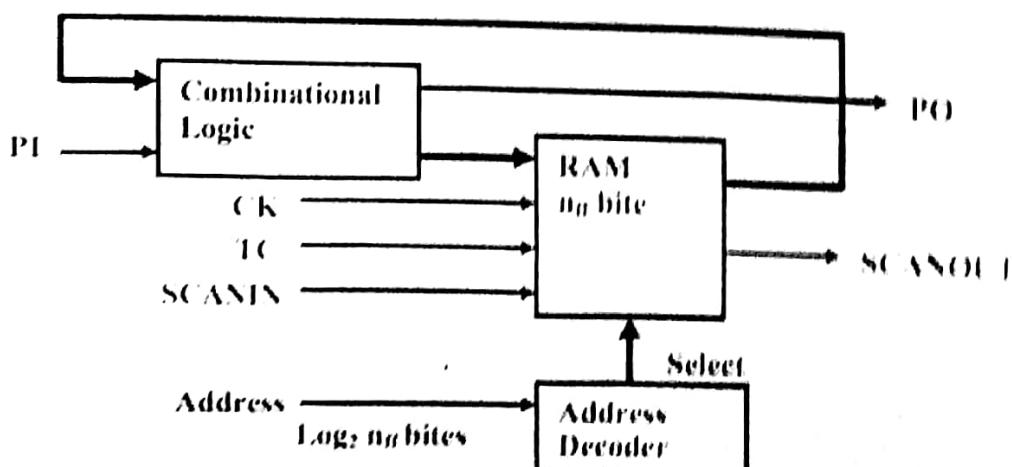


Fig. 39.6 The Random Access structure

## Partial Scan design

A subset of flip-flops is scanned.

### **Objectives:**

- Minimize area overhead and scan sequence length, yet achieve required fault coverage
- Exclude selected flip-flops from scan:
  - Improve performance
  - Allow limited scan design rule violations
- Allow automation:
  - In scan flip-flop selection
  - In test generation
- Shorter scan sequences – reduce application time

- In this approach only a subset of flip-flops is scanned. The main objectives of this approach are to minimize the area overhead and scan sequence length. It would be possible to achieve required fault coverage
- In this approach sequential ATPG is used to generate test patterns. Sequential ATPG has number of difficulties such as poor initializability, poor controllability and observability of the state variables etc. Number of gates, number of FFs and sequential depth give little idea regarding testability and presence of cycles makes testing difficult. Therefore sequential circuit must be simplified in such a way so that test generation becomes easier
- Removal of selected flip-flops from scan improves performance and allows limited scan design rule violations.
- It also allows automation in scan flip-flop selection and test generation

## **3) Built in Self Test (BIST)**

**Logic built-in self-test** (BIST) is a *design for testability* (DFT) technique in which a portion of a circuit on a chip, board, or system is used to test the digital logic circuit itself. Logic BIST is crucial for many applications, in particular for life-

In this approach testability is having the circuit itself generate the test pattern instead of requiring an application of external patterns.

The objectives of BIST are:

- To reduce test pattern generation cost
- To reduce the volume of test data
- To reduce test time

### **Advantage:**

- Lower system test effort
- Improved system maintained and repair
- Better diagnosis at component level.

BIST techniques aim to effectively integrate an automatic test system into the chip design.

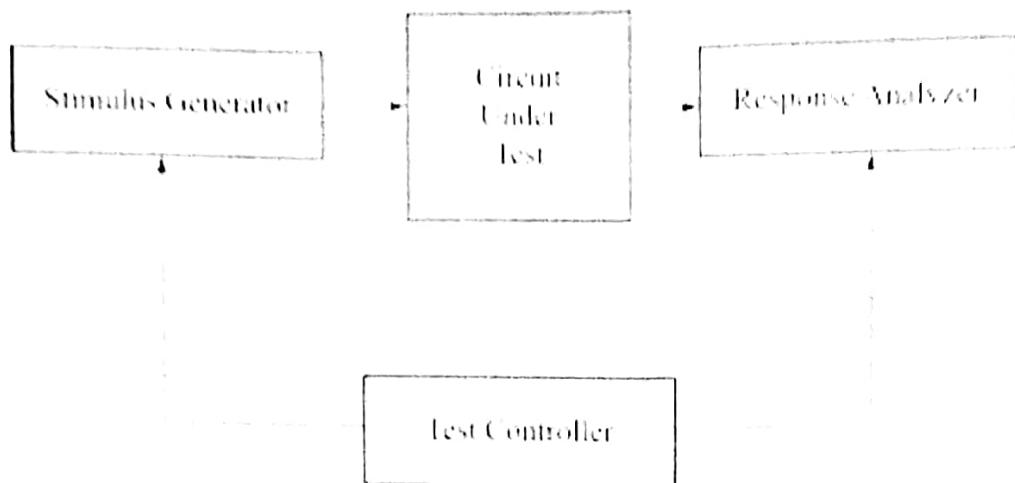


Fig. 9.11 General format of BIST

BIST is a set of structured test techniques for combinational and sequential logic, memories and multiplexers and other embedded logic blocks. It contains a means for supplying test patterns to the DUT (device under test)/ sub-circuit under test and a means of comparing the device's response to a known correct sequence.

**Explain different ways to generate stimulus in BIST?**

**There are many ways to generate Stimulus pattern:**

**a) Exhaustive approach:**

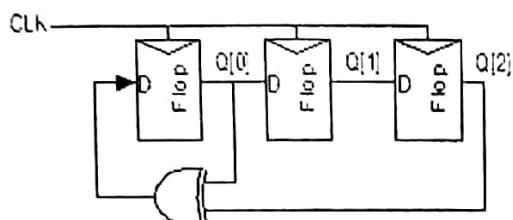
The test length is  $2^N$ ; N is the no. of inputs to the circuit. In exhaustive nature of the test means that all detectable faults will be detected given the space of the available input signal.  
Ex: N-bit counter

**b) Random Approach:**

It implies the application of a randomly chosen sub set of  $2^N$  possible input patterns. But the subset has to be chosen such that reasonable fault coverage is obtained. Ex: Pseudo random pattern generator.

### 3) Linear Feedback Shift Register (LFSR) or Pseudo-Random Sequence Generator(PRSG)

- Shift register with input taken from XOR of state



Step	Q
0	111
1	110
2	101
3	010
4	100
5	001
6	011
7	111 (repeats)

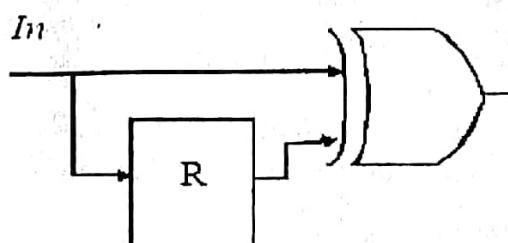
- Some of the outputs are XOR and fed back into the circuit. An N-bit LFSR cycles through  $2^{N-1}$  states before repeating the sequence, which produces a random pattern.
- LFSR model is that of finite state machine comprising storage elements and modulo two adders (XOR Gates) connected in feedback loop.
- LFSR techniques can be applied in a no. of ways. LFSR can either be series or parallel the differences being in the operating speed and in the area of silicon occupied parallel LFSR being faster.

### Observer(

Explain different methods in Response Analyzer?

#### a)Signature Analysis(Compact test)

- Signature analysis performs polynomial division .ie to say division of data out of the device under test(DUT).
- Signature  $R(x)=p(x)/c(x)$ .Polynomial  $p(x)$  ,characteristic  $c(x)$ .
- The signature from the DUT is compared with the expected signature to determine if DUT is fault free.
- The difference between the faulty signature and a good signature is used to indicate the nature of the fault.
- Signature analysis has been proved to be a reliable and attractive to full uncompactected testing



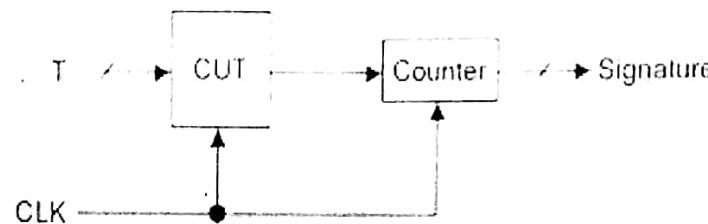
Counts transitions on single bit stream = compression in time

## b) Transition count Testing

The theory behind transition count testing is similar to that for ones count testing except that the signature is defined as the number of 0-to-1 and 1-to-0 transitions.

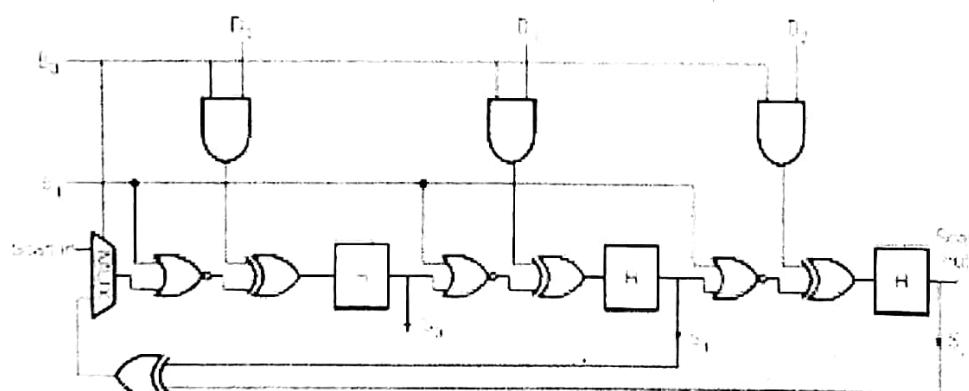
The transition count test technique [Hayes 1976] simply requires using a D flip-flop and an XOR gate connected to a ones counter (see Figure 5.28), to count the

number of transitions in the output data stream. Consider the example given above. Because  $R_0 = \{0101100\}$ , the signature or transition count of  $R_0$ ,  $TC(R_0)$ , will be 4. Assume that the initial state of the D flip-flop,  $r_{-1}$ , is 0. Fault  $f_1$  causing an erroneous response  $R_1 = \{1100110\}$  will not be detected because  $TC(R_1) = TC(R_0) = 4$ , but fault  $f_2$  causing  $R_2 = \{0101010\}$  will be detected because  $TC(R_2) = 6$ .



## BILBO (Built in logic Block Observer)

Explain BILBO along with block diagram and different operation mode and give its application.



$B_0$	$B_1$	Operation mode
1	1	Normal
0	0	Scan
1	0	Pattern generation or Signature analysis
0	1	Reset

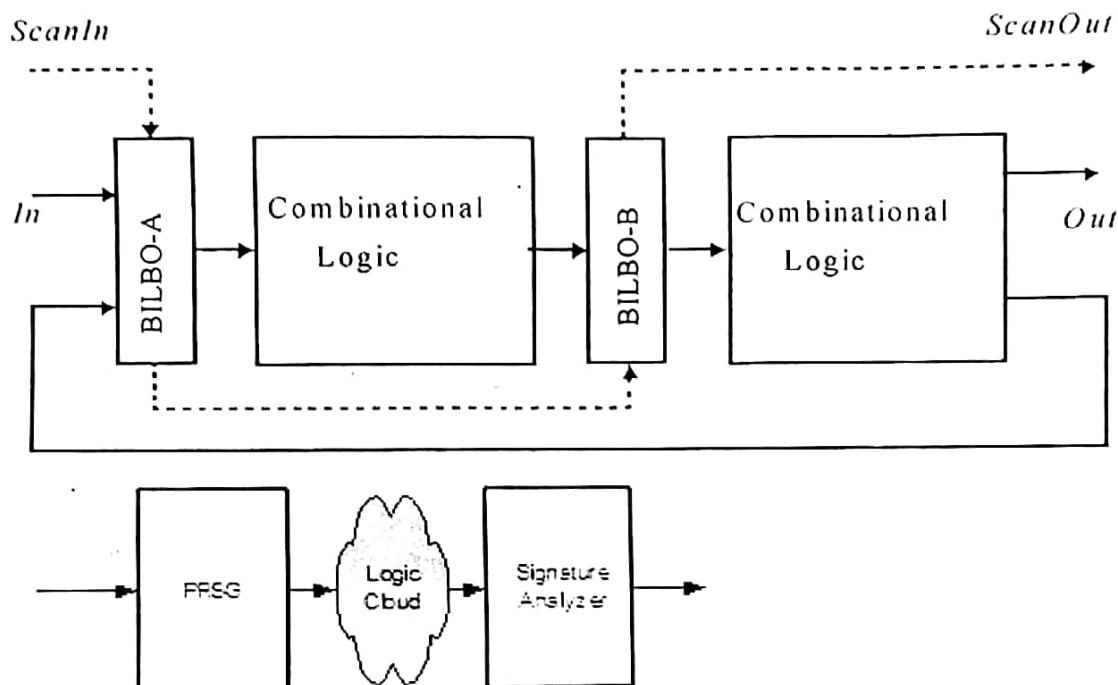
Fig: Different operation mode

In this method, signature analysis along with scan path is used.

- It is aimed at integrated modular and bus-oriented systems, such as microprocessor and similar circuits

- In the normal mode,  $B_0 = B_1 = 1$  and the storage elements are used independently by the circuit.
- In the Test1 mode(Scan)  $B_0 = B_1 = 0$  and the storage elements are configured as a scan path, all storage elements being connected as a serial shift register. Test vectors are then applied to the scan-in input and responses shifted out at the scan path output. The analysis of data is then similar to that for a simple scan path test.
- In the Test2 mode  $B_0 = 1, B_1 = 0$  and the circuit is then configured in a LFSR mode and can be used either as a polynomial divider to compact data or as a random test pattern generator.
- In the final mode(Reset),  $B_0 = 0, B_1 = 1$  which resets the BILBO.

## BILBO Application



Write Short notes on Automatic test Pattern generation

## Automatic test Pattern generation

- It is an electronic design automation method/technology used to find an input (or test) sequence that, when applied to a digital circuit, enables automatic test equipment to distinguish between the correct circuit behaviour and the faulty circuit behaviour caused by defects.
- The generated patterns are used to test semiconductor devices after manufacture, and in some cases to assist with determining the cause of failure analysis.<sup>1</sup>
- The effectiveness of ATPG is measured by the amount of modelled defects, or fault models, that are detected and the number of generated patterns.
- These metrics generally indicate test quality (higher with more fault detections) and test application time (higher with more patterns).
- ATPG is influenced by the fault model under consideration, the type of circuit under test (full scan, synchronous sequential, or asynchronous sequential), the level of abstraction used to represent the circuit under test (gate, register-transfer, switch), and the required test quality.

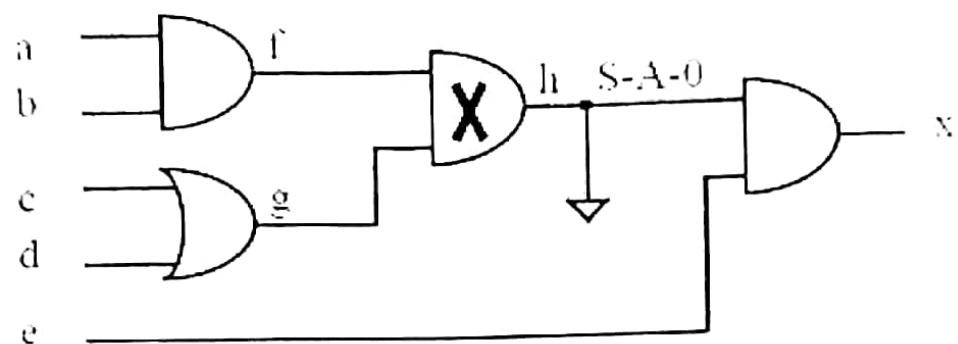
- for given fault, determine excitation vector (called test vector) that will propagate error to primary (observable) output

Illustrate along with example different Fault models in Fault simulation

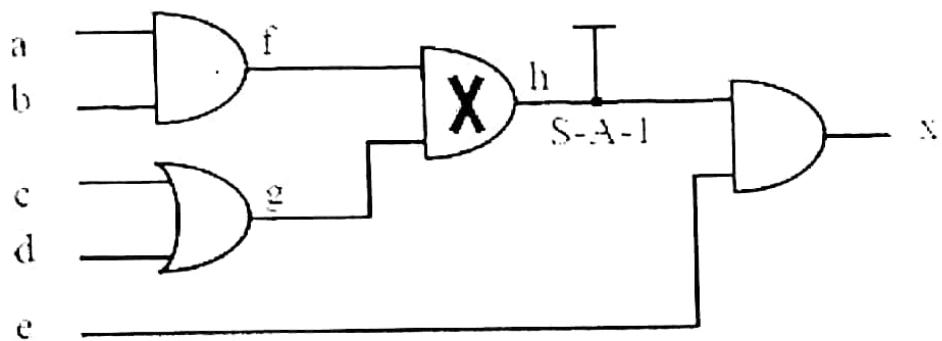
### Different types of Fault Models

- Stuck at fault model

**Stuck-at-0**

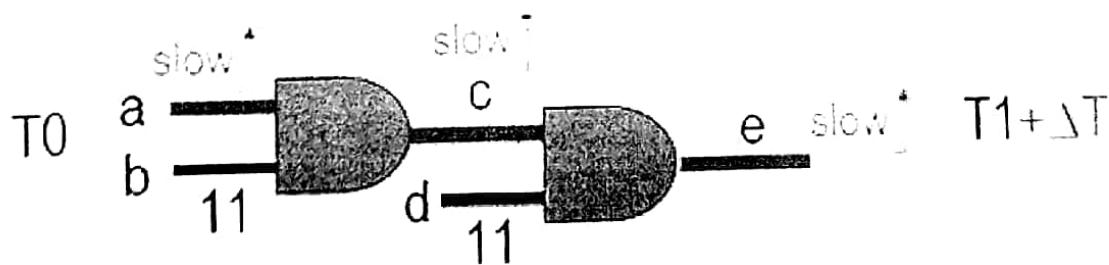


**Stuck-at-1**



- Path delay fault

A defect can affect the speed of a path in the circuit

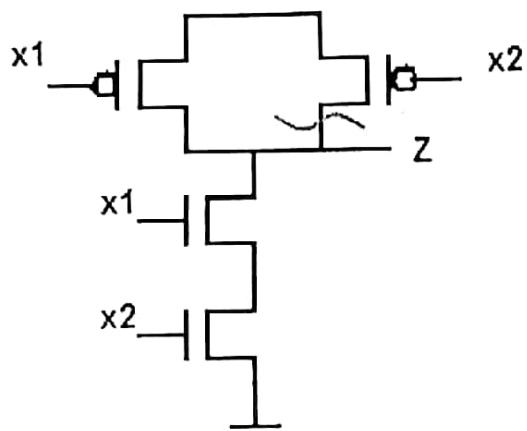


### c) Transistor faults

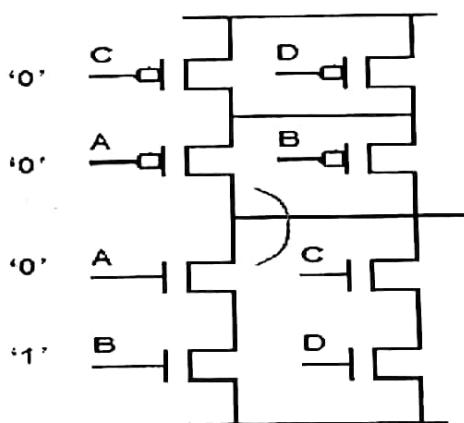
This model is used to describe faults for CMOS logic gates.

At transistor level, a transistor maybe stuck-short or stuck-open.

In stuck-short, a transistor behaves as it is always conducts (or stuck-on), and stuck-open is when a transistor never conducts current (or stuck-off). Stuck-short will produce a short between VDD and VSS



### d) Bridging faults

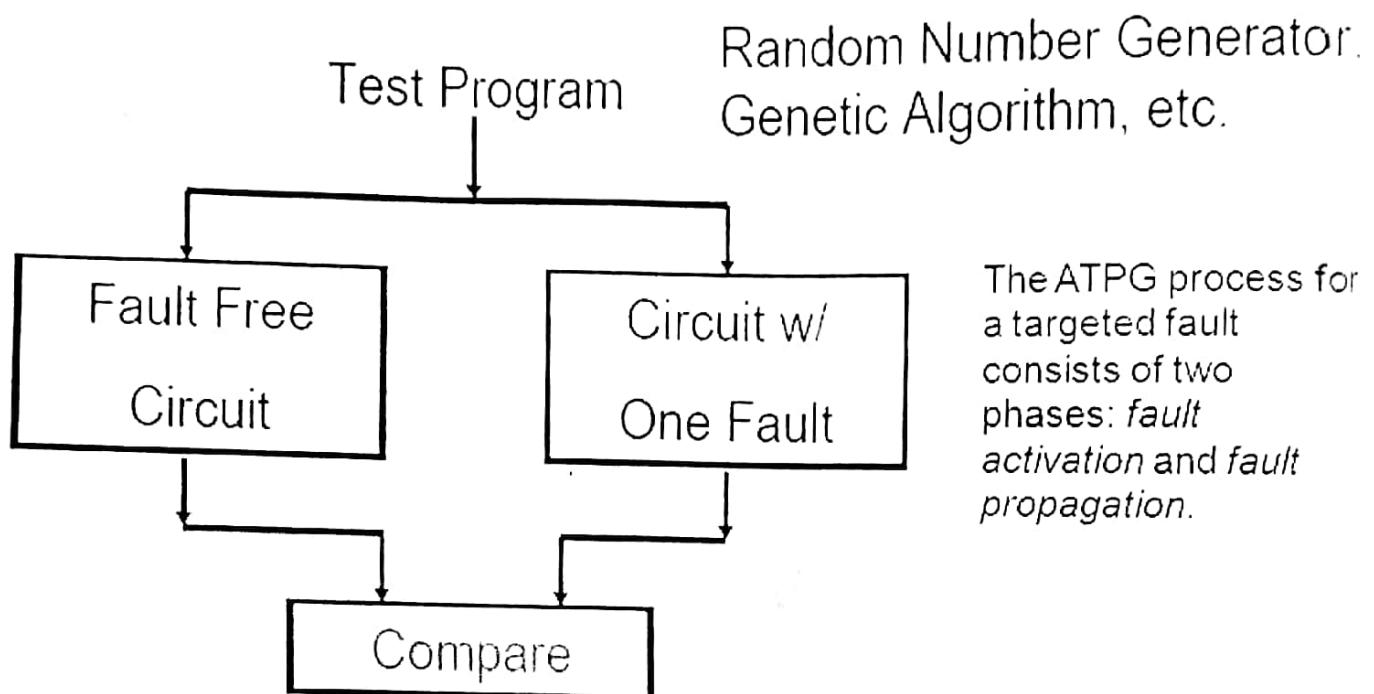


A short circuit between two signal lines is called bridging faults. Bridging to VDD or Vss is equivalent to stuck at fault model. Traditionally both signals after bridging were modeled with logic AND or OR of both signals. If one driver dominates the other driver in a bridging situation, the dominant driver forces the logic to the other one, in such case a dominant bridging fault is used. To better reflect the reality of CMOS VLSI devices, a Dominant AND or Dominant OR bridging fault model is used.

What is Fault Simulation along with diagram

### Fault Simulation

- determines test coverage of proposed test-vector set
- simulates correct network in parallel with faulty networks



Testing very-large-scale integrated circuits with high fault coverage is a difficult task because of complexity. Therefore many different ATPG methods have been developed to address combinational and sequential circuits.

Ex: Path sensitization method, Boolean difference, D-alg, PODEM

Solve problems based on Path sensitization and Boolean difference method

**Don Bosco College of Engineering, Fatorda, Goa**  
**Department of Electronics and Telecommunication Engineering**

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To evolve into a Holistic Learning Hub that moulds technologically proficient engineers in the field of Electronics and Telecommunication; contributing to the global industry and society with Integrity, Ethics and Professionalism as envisaged by Don Bosco

## **MISSION**

- To impart education abreast with the fundamentals and advances in technology and transform students into globally accepted professionals.
- To foster networking with all stakeholders for promoting technical innovation, research and entrepreneurship.
- To encourage various skill enhancing activities and extra-curricular activities to instill high levels of work ethics and responsibility for a better society.

## **Course Outcomes**

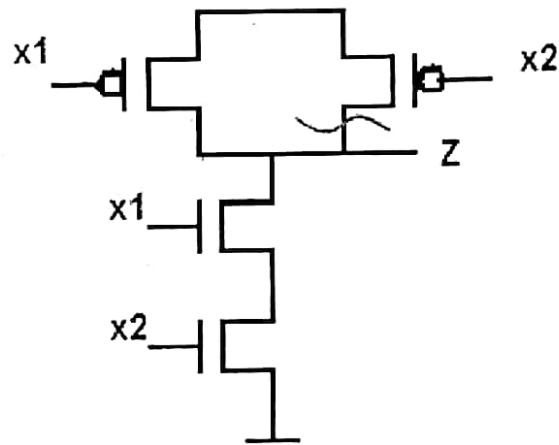
<b>ETC/ECE 5.5.1</b>	Be able use mathematical methods to calculate the threshold voltage for a given MOSFET and obtain the value of Drain current for any given biasing condition and analyze the effects of narrow and short channel on device characteristics and implement in spice programs.
<b>ETC/ECE 5.5.2</b>	Be able to create models of voltage parameters and noise margin of a CMOS inverter and also explain its switching characteristics and the capability to develop SPICE programs for various circuits.
<b>ETC/ECE 5.5.3</b>	Ability to implement designing integrated circuits using Spice for modelling CMOS circuits
<b>ETC/ECE 5.5.4</b>	Be able to design combinational circuits in transmission gates ,CMOS logic and design combinational, sequential circuits using VHDL
<b>ETC/ECE 5.5.5</b>	Ability to analyze the concepts CMOS design and draw Euler's diagram. Implement layouts for the design.
<b>ETC/ECE 5.5.6</b>	Ability to understand the fabrication of MOS and compute the test pattern which will detect Faults in a given integrated circuits

### c) Transistor faults

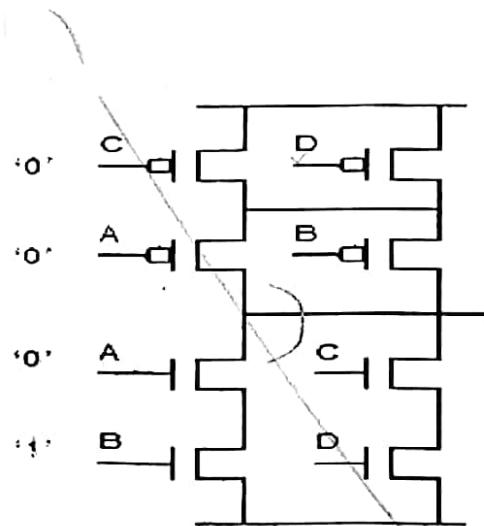
This model is used to describe faults for CMOS logic gates.

At transistor level, a transistor maybe stuck-short or stuck-open.

In stuck-short, a transistor behaves as it is always conducts (or stuck-on), and stuck-open is when a transistor never conducts current (or stuck-off). Stuck-short will produce a short between VDD and VSS



### d) Bridging faults



A short circuit between two signal lines is called bridging faults. Bridging to VDD or Vss is equivalent to stuck at fault model. Traditionally both signals after bridging were modeled with logic AND or OR of both signals. If one driver dominates the other driver in a bridging situation, the dominant driver forces the logic to the other one, in such case a dominant bridging fault is used. To better reflect the reality of CMOS VLSI devices, a Dominant AND or Dominant OR bridging fault model is used.