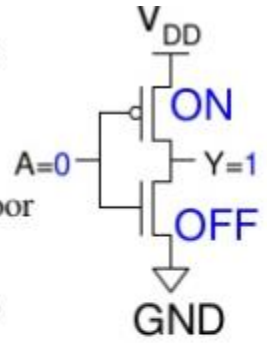
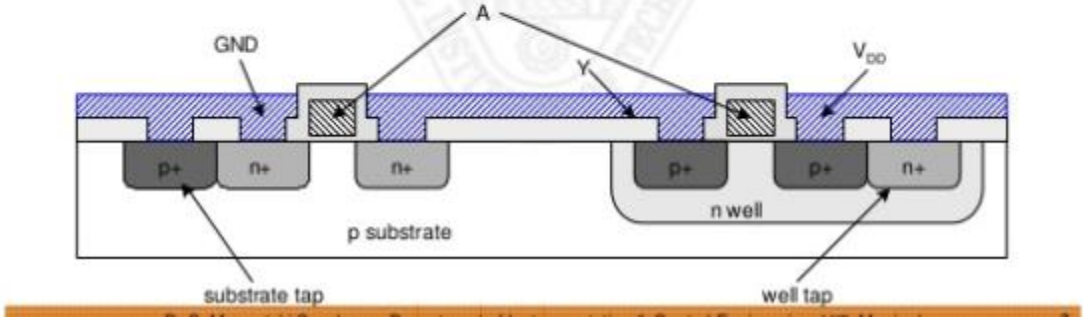
CMOS Fabrication

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors
- Substrate must be tied to GND and n-well to VDD
- Metal to lightly-doped semiconductor forms poor connection
- Use heavily doped well and substrate contacts / taps



1)



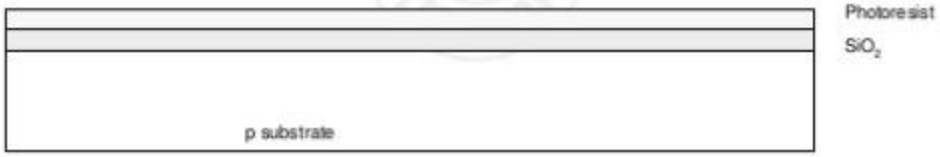
- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

2)

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace

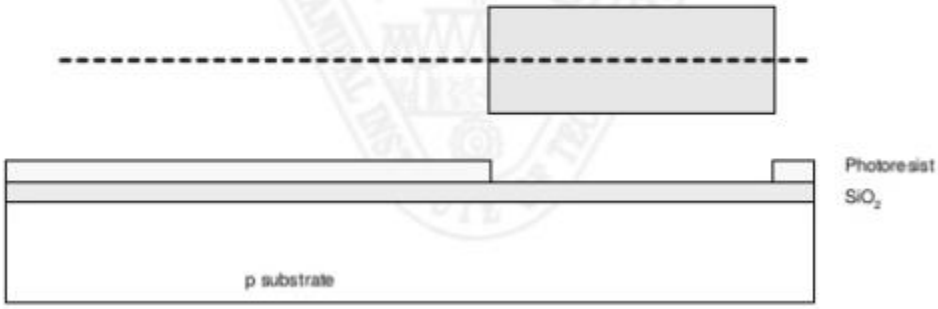
3)

- Used for lithography.
- Lithography is a process used to transfer a pattern to layer on the chip. Similar to printing process.
- Spin on photoresist (about 1 mm thickness)
  - Photoresist is a light-sensitive organic polymer
  - Positive Photoresist: Softens where exposed to light
  - Negative Photoresist: Harden where exposed to light, Not used in practice generally.



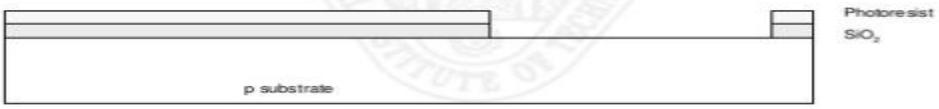
4)

- Expose photoresist through n-well mask
- Strip off exposed photoresist



5)

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed

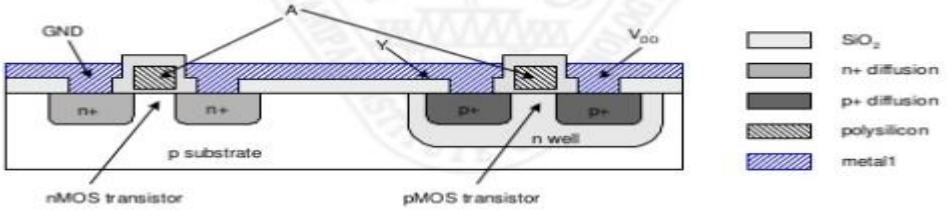


6)

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step

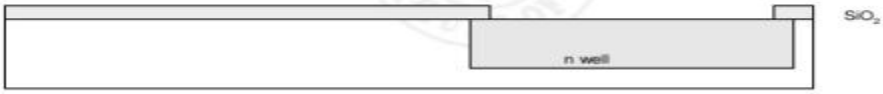
- Typically use p-type substrate for nMOS transistors

- Requires n-well for body of pMOS transistors



7)

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



8)

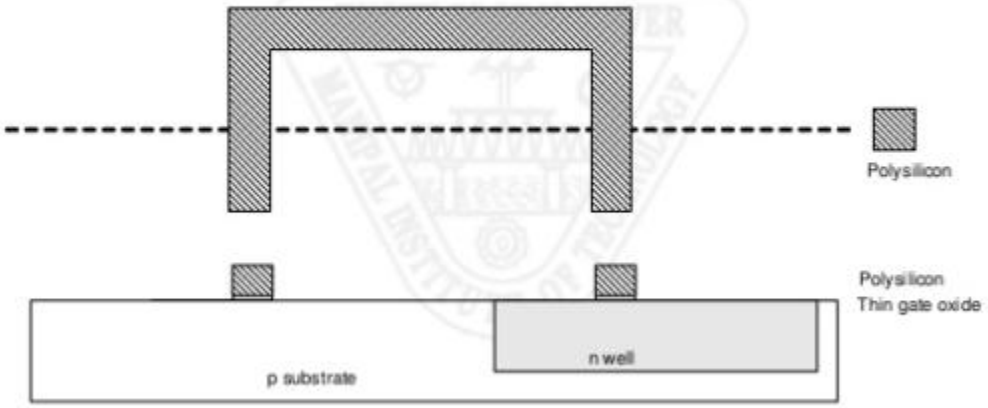
- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor

9)

10)

- Use same lithography process to pattern polysilicon

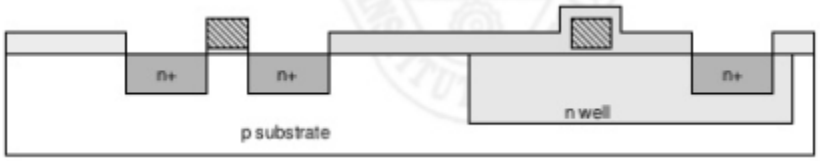


- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact

11)

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion

12)

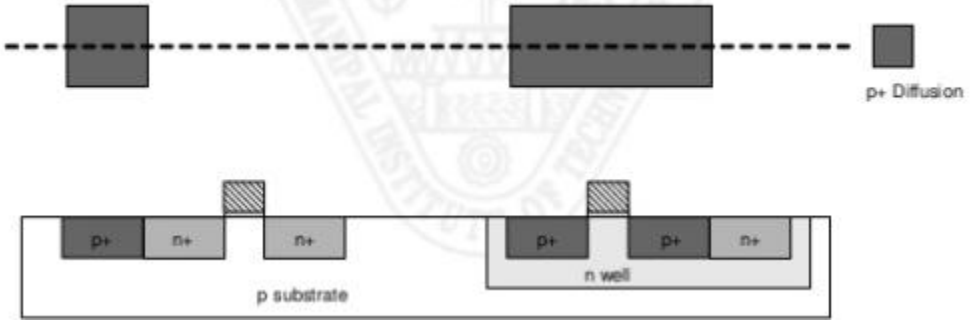


13_)

- Strip off oxide to complete patterning step

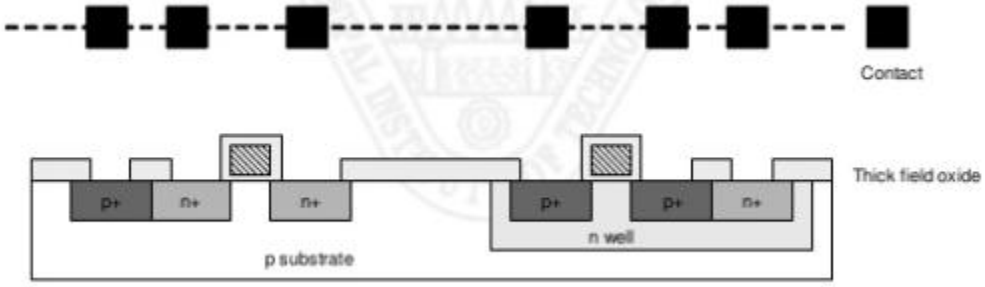
14)

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact

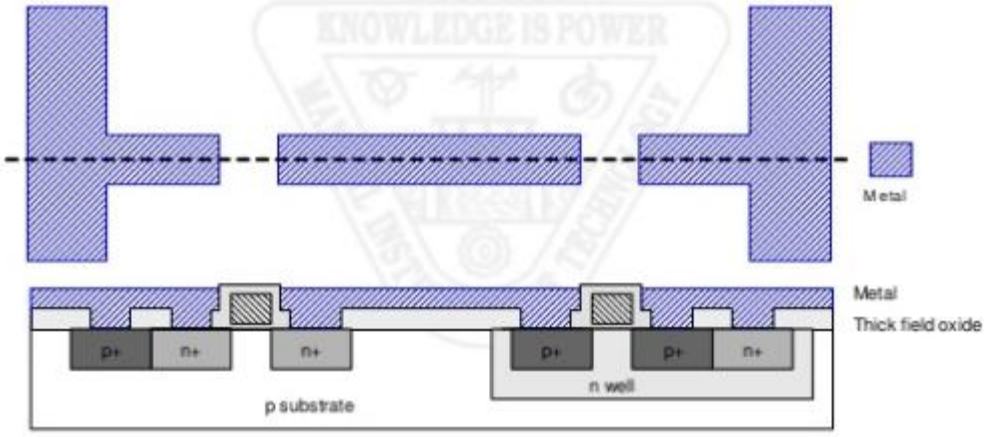


- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

15)



- Sputter on aluminium over whole wafer
- Pattern to remove excess metal, leaving wires



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