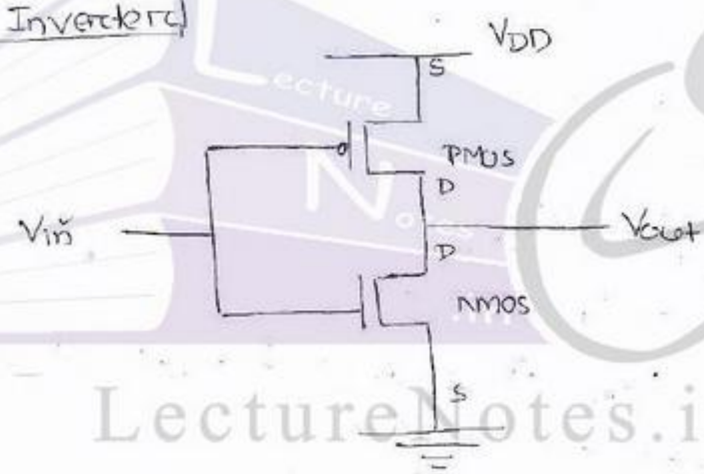
CMOS Inverter



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Operating modes

for PMOS transistor,

$$V_{GS,P} = V_G - V_S = V_{in} - V_{DD}$$

$$V_{DS,P} = V_{out} - V_{DD}$$

for nMOS transistor

$$V_{GS,n} = V_G - V_S = V_{in} - 0 = V_{in}$$

$$V_{DS,n} = V_{out}$$

The n-MOS transistor operates in linear region if

$$V_{DS,n} \leq V_{GS,n} - V_{TO,n}$$

$$\boxed{V_{out} \leq V_{in} - V_{TO,n}}$$

saturation region

$$V_{DS,n} \geq V_{GS,n} - V_{TO,n}$$

$$\boxed{V_{out} \geq V_{in} - V_{TO,n}}$$

cutoff

$$V_{GS} < V_{TO,n}$$

$$\boxed{V_{in} < V_{TO,n}}$$

The PMOS transistor operates in linear region if

$$V_{DS,P} \geq V_{GS,P} - V_{TO,P}$$

$$V_{out} - \cancel{V_{DD}} \geq V_{in} - \cancel{V_{DD}} - V_{TO,P}$$

$$\boxed{V_{out} \le V_{in} - V_{T0,p}}$$

PMOS is in cut-off region if

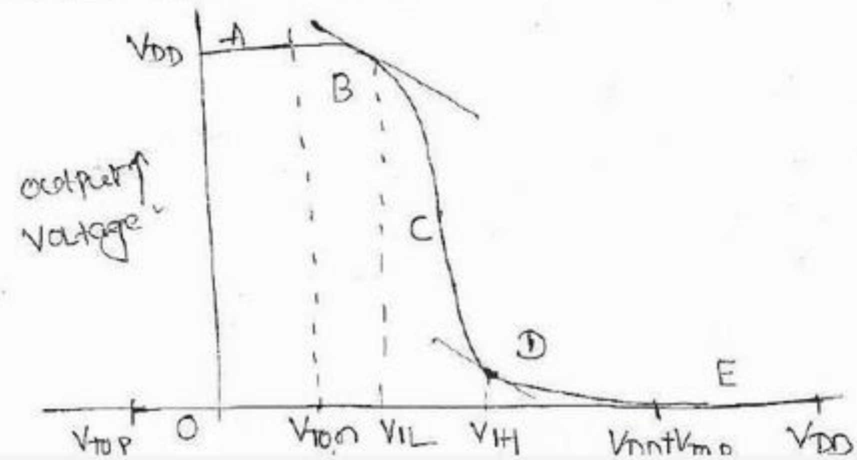
$$V_{GSP} > V_{T0,P}$$

$$V_{in} - V_{DD} > V_{T0,P}$$

$$\boxed{V_{in} > V_{DD} + V_{T0,P}}$$

VTC of CMOS inverter.

VTC of CMOS inverter.



Region	V_{IN}	V_{out}	nMOS	PMOS
A	$< V_{T0,n}$	V_{OH}	cutoff	linear
B	V_{IL}	High $\approx V_{OH}$	Saturation	Linear
C	V_{th}	V_{th}	Saturation	Saturation
D	V_{IH}	$\simeq V_{OL}$	Linear	Saturation
E	$> V_{DD} + V_{T0,P}$	V_{OL}	linear	cutoff

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In Region A, where $V_{in} < V_{T0,n}$ the nMOS transistor is cutoff and the output voltage is equal to $V_{OH} = V_{DD}$. As the input voltage is increased beyond $V_{T0,n}$ ie Region B, the nMOS transistor starts conducting in saturation mode and the output voltage begins to decrease. The critical voltage V_{IL} corresponds to $dV_{out}/dV_{in} = -1$ located within Region B. As the output voltage further decreases, the pMOS transistor enters saturation at Region C. The inverter threshold voltage, where $V_{in} = V_{out}$, is located in region C. When the output voltage falls below $V_{in} - V_{T0,n}$ the nMOS transistor starts to operate in linear mode. This corresponds to Region D where critical voltage point V_{IH} with $dV_{out}/dV_{in} = -1$ is located. Finally in Region E, with the input voltage $V_{in} > V_{DD} + V_{T0,p}$ the pMOS transistor is cutoff and the output voltage is $V_{OL} = 0$

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Calculation of V_{IL}

$V_{in} = V_{IL}$

Slope of the VTC is equal to (-1) ie. $\frac{dV_{out}}{dV_{in}} = -1$

nmos transistor operates in saturation and pmos trasistor is in linear region.

$$I_{D,n} = I_{D,p}$$

$$\frac{k_n}{2}\left(V_{GS,n} - V_{T0,n}\right)^2 = \frac{k_p}{2}\left[2\left(V_{GS,p} - V_{T0,p}\right)V_{DS,p} - V_{DS,p}^2\right]$$

$$\frac{k_n}{2}\left(V_{in} - V_{T0,n}\right)^2 = \frac{k_p}{2}\left[2\left(V_{in} - V_{DD} - V_{T0,p}\right)\left(V_{out} - V_{DD}\right) - \left(V_{out} - V_{DD}\right)^2\right]$$

Differentiating w.r.t. V_{in}

$$\frac{k_n}{\cancel{2}}\left[\cancel{2}\left(V_{in} - V_{T0,n}\right)\right] = \frac{k_p}{\cancel{2}}\left[\cancel{2}\left(V_{in} - V_{DD} - V_{T0,p}\right)\frac{dV_{out}}{dV_{in}} + \left(V_{out} - V_{DD}\right)\cancel{2} - \cancel{2}\left(V_{out} - V_{DD}\right)\frac{dV_{out}}{dV_{in}}\right]$$

put $dV_{out}/dV_{in} = -1$

$$k_n\left[V_{in} - V_{T0,n}\right] = k_p\left[\left(V_{in} - V_{DD} - V_{T0,p}\right)(-1) + \left(V_{out} - V_{DD}\right) - \left(V_{out} - V_{DD}\right)(-1)\right]$$

$$V_{in} = V_{IL}$$

$$k_n\left[\left(V_{IL} - V_{T0,n}\right)\right] = k_p\left[\left(\cancel{V_{DD}} + V_{T0,p} - V_{IL} + 2V_{out} - \cancel{V_{DD}} + V_{DD}\right)\right]$$

$$k_n V_{IL} - k_n V_{T0,n} = k_p\left[V_{T0,p} - V_{IL} + 2V_{out} - V_{DD}\right]$$

$$\frac{k_n}{k_p}V_{IL} - \frac{k_n}{k_p}V_{T0,n} = V_{T0,p} + 2V_{out} - V_{DD} - V_{IL}$$

$$V_{IL} + \frac{k_n}{k_p}V_{IL} = V_{T0,p} + 2V_{out} - V_{DD} + \frac{k_n}{k_p}V_{T0,n}$$

$$V_{IL}\left[1 + k_R\right] = 2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}$$

$$k_R = \frac{k_n}{k_p}$$

$$\boxed{V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R}}$$

2. Calculation of V_{IH}

$V_{in} = V_{IL}$

nmos $\rightarrow$ linear

pmos $\rightarrow$ saturation

$$I_{D,p} = I_{D,n}$$

$$\frac{k_p}{2}\left[V_{GS,p} - V_{TO,p}\right]^2 = \frac{k_n}{2}\left[2\left(V_{GS,n} - V_{TO,n}\right)V_{DS,n} - V_{DS,n}^2\right]$$

$$\frac{k_p}{2}\left[V_{in} - V_{DD} - V_{TO,p}\right]^2 = \frac{k_n}{2}\left[2\left(V_{in} - V_{TO,n}\right)V_{out} - V_{out}^2\right]$$

differentiating w.r.t. V_{in}

$$\frac{k_p}{\cancel{2}}\left[\cancel{2}\left(V_{in} - V_{DD} - V_{TO,p}\right)\right] = \frac{k_n}{\cancel{2}}\left[\cancel{2}\left(V_{in} - V_{TO,n}\right)\frac{dV_{out}}{dV_{in}} + \cancel{2}V_{out} - \cancel{2}V_{out}\frac{dV_{out}}{dV_{in}}\right]$$

put $V_{in} = V_{IH}$, $\frac{dV_{out}}{dV_{in}} = -1$

$$k_p\left(V_{IH} - V_{DD} - V_{TO,p}\right) = k_n\left[\left(V_{IH} - V_{TO,n}\right)(-1) + V_{out} - V_{out}(-1)\right]$$

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$$= k_n\left[V_{TO,n} - V_{IH} + 2V_{out}\right]$$

$$k_pV_{IH} - k_pV_{DD} - k_pV_{TO,p} = k_nV_{TO,n} - k_nV_{IH} + 2k_nV_{out}$$

$$(k_p + k_n)V_{IH} = k_p\left(V_{DD} + V_{TO,p}\right) + k_n\left(2V_{out} + V_{TO,n}\right)$$

$$V_{IH} = \frac{k_p\left(V_{DD} + V_{TO,p}\right) + \left(2V_{out} + V_{TO,n}\right)k_n}{k_p + k_n}$$

Dividing by k_n

$$V_{IH} = \frac{\frac{k_p}{k_n}(V_{DD} + V_{T0,p}) + 2V_{out} + V_{T0,n}}{1 + \frac{k_p}{k_n}}$$

$$= \frac{\frac{1}{k_R}(V_{DD} + V_{T0,p}) + 2V_{out} + V_{T0,n}}{1 + \frac{1}{k_R}}$$

$$\boxed{V_{IH} = \frac{(V_{DD} + V_{T0,p}) + k_R(2V_{out} + V_{T0,n})}{1 + k_R}}$$

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3. Calculation of V_{TH}

$V_{in} = V_{TH}$

pmos, nmos } saturation

$$I_{D,p} = I_{D,n}$$

$$\frac{k_p}{2}(V_{GS,p} - V_{T0,p})^2 = \frac{k_n}{2}(V_{GS,n} - V_{T0,n})^2$$

$$\Rightarrow k_p(V_{in} - V_{DD} - V_{T0,p})^2 = k_n(V_{in} - V_{T0,n})^2$$

$$\Rightarrow k_p(V_{TH} - V_{DD} - V_{T0,p})^2 = k_n(V_{TH} - V_{T0,n})^2$$

$$(V_{DD} - V_{TH} + V_{T0,p})^2 = \frac{k_n}{k_p}(V_{TH} - V_{T0,n})^2$$

$$V_{DD} - V_{TH} + V_{T0,p} = \sqrt{\frac{k_n}{k_p}}(V_{TH} - V_{T0,n})$$

$$V_{DD} + V_{T0,p} - V_{TH} = \sqrt{k_R}(V_{TH} - V_{T0,n})$$

$$V_{DD} + V_{T0,p} + \sqrt{k_R}\, V_{T0,n} = \sqrt{k_R}\, V_{TH} + V_{TH}$$

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$$= (\sqrt{k_R} + 1) V_{TH}$$

$$V_{TH} = \frac{V_{DD} + V_{T0,p} + V_{T0,n}\sqrt{k_R}}{1 + \sqrt{k_R}}$$

$$\boxed{V_{Th} = \frac{V_{TO,n} + \frac{1}{\sqrt{K_R}}\left(V_{DD} + V_{TO,p}\right)}{1 + \frac{1}{\sqrt{K_R}}}}$$

Design of CMOS Inverters

the inverter threshold voltage is one of the most important parameters of the CMOS inverter circuit.

$$V_{TH} + \frac{1}{\sqrt{K_R}} V_{TH} = V_{TO,n} + \frac{1}{\sqrt{K_R}}\left(V_{DD} + V_{TO,p}\right)$$

$$V_{TH} - V_{TO,n} = \frac{1}{\sqrt{K_R}}\left(V_{DD} + V_{TO,p} - V_{TH}\right)$$

$$\sqrt{\frac{1}{K_R}} = \frac{V_{TH} - V_{TO,n}}{V_{DD} + V_{TO,p} - V_{TH}}$$

for an ideal CMOS inverter $V_{TH} = \frac{V_{DD}}{2}$

$$\left(\frac{k_n}{k_p}\right)_{ideal} = \left[\frac{V_{DD} + V_{TO,p} - \frac{V_{DD}}{2}}{\frac{V_{TH}}{2} - V_{TO,n}}\right]^2$$

$$= \left[\frac{0.5\,V_{DD} - V_{TO,p}}{0.5\,V_{DD} - V_{TO,n}}\right]^2$$

For symmetric inverter

$$\boxed{V_{TO,n} = V_{TO,p}}$$

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$$\left(\frac{k_n}{k_p}\right)_{\substack{\text{symmetric}\\ \text{inverter}}} = 1$$

The ratio k_R is defined as

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p}$$

$$k_R = \frac{\mu_n\left(\frac{W}{L}\right)_n}{\mu_p\left(\frac{W}{L}\right)_p}$$

assuming that the gate oxide thickness t_{ox} and hence, the gate oxide capacitance C_{ox} have the same value for both nMOS and pMOS transistors

$$\frac{\left(\frac{W}{L}\right)_n \mu_n}{\left(\frac{W}{L}\right)_p \mu_p} = 1 \Big|_{\substack{\text{symmetric}\\ \text{inverter}}}$$

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230\ cm^2/V\text{-}s}{580\ cm^2/V\text{-}s}$$

$$\boxed{\left(\frac{W}{L}\right)_p \simeq 2.5\left(\frac{W}{L}\right)_n}$$

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- Symmetric CMOS inverter

$$V_{TO,n} = |V_{TO,p}|$$

$$k_R = 1$$

$$V_{IL} = \frac{2V_{out} + V_{TO,p} - V_{DD} + k_R V_{TO,n}}{1 + k_R}$$

$$= \frac{2V_{out} + 2V_{T0,n} - V_{DD}}{2}$$

pmos → linear
nmos → saturation

$$\boxed{V_{IL} = \frac{1}{8}\left(3V_{DD} + 2V_{T0,n}\right)}$$

$$\boxed{V_{IH} = \frac{1}{8}\left(5V_{DD} - 2V_{T0,n}\right)}$$

In a symmetric inverter the sum of V_{IL} & V_{IH} is always equal to V_{DD}

$$\boxed{V_{IL} + V_{IH} = V_{DD}}$$

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Symmetric inverter

$$\boxed{\begin{array}{l} V_{OH} = V_{DD} \\ V_{OL} = 0 \end{array}}$$

Noise margin $NM_L = V_{IL} - V_{OL} = V_{IL}$

$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$

Q Consider a CMOS inverter circuit with the following parameters:

$V_{DD} = 3.3V$

$V_{T0,n} = 0.6V$

$V_{T0,p} = -0.7V$

$K_n = 200\,\mu A/V^2$

$K_p = 80\,\mu A/V^2$

Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $K_R = 2.5$ and $V_{T0,n} \neq |V_{T0,p}|$ hence it is not a symmetric inverter.

$\underline{\underline{V_{IL}}}$ $V_{IL} = \dfrac{2V_{out} + V_{T0,p} - V_{DD} + K_R V_{T0,n}}{1+K_R}$

$$= \frac{2V_{out} - 0.7 - 3.3 + 2.5 \times 0.6}{1 + 2.5}$$

$$\boxed{V_{IL} = 0.57 V_{out} - 0.71}$$

pMOS → linear
nMOS → saturation

$$\frac{K_n}{2}(V_{in} - V_{T0,n})^2 = \frac{K_p}{2}\left[2(V_{in} - V_{DD} - V_{T0,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

$$2.5(0.57V_{out} - 0.71 - 0.6)^2 = 2(0.57V_{out} - 0.71 - 3.3 + 0.7)$$

$$(V_{out} - 3.3) - (V_{out} - 3.3)^2$$

$$0.66V_{out}^2 + 0.05V_{out} - 6.65 = 0$$

$$\boxed{V_{out} = 3.14V} \quad \because V_{out} > 0$$

$$V_{IL} = 0.57V_{out} - 0.71$$

$$= 0.57 \times 3.14 - 0.71$$

$$\boxed{V_{IL} = 1.08V}$$

$\underline{\underline{V_{IH}}}$ $V_{IH} = \dfrac{V_{DD} + V_{T0,p} + K_R(2V_{out} + V_{T0,n})}{1 + K_R}$

$$= \frac{3.3 - 0.7 + 2.5(2V_{out} + 0.6)}{1 + 2.5}$$

$$V_{IH} = 1.43V_{out} + 1.17$$

pmos → saturation
nmos → linear

nmos → linear

$$\frac{k_n}{2}\left[2(V_{in}-V_{T0,n})\cdot V_{out}-V_{out}^2\right]=\frac{k_p}{2}(V_{in}-V_{DD}-V_{T0,p})^2$$

$$2.5\left[2(1.43V_{out}+1.17-0.6)V_{out}-V_{out}^2\right]$$
$$=(1.43V_{out}+1.17-3.3+0.7)^2$$

$$2.61V_{out}^2+6.94V_{out}-2.04=0$$

$$\boxed{V_{out}=0.27V}$$

$$V_{IH}=1.43V_{out}+1.17$$
$$=1.43\times0.27+1.17$$
$$\boxed{V_{IH}=1.55V}$$

Noise margin

$$NM_L=V_{IL}-V_{OL}=1.08V \quad \because V_{OL}=0$$
$$NM_H=V_{OH}-V_{IH}=3.3-1.55 \quad \because V_{OH}=V_{DD}$$
$$=1.75V$$

Advantages of CMOS inverter

i) Static power dissipation is zero.

ii) Noise margin is high

iii) Provides full output voltage swing between 0V & VDD

Disadvantages of CMOS inverter

i) It occupies more area

ii) circuit complexity is more