Layout Design Rules ... manufacture ... or rules, which ...

(a)

(1)

M - II

(1)

Switching circuit characteristics :-

→ The switching speed of a cmos gate is limited by the time taken to charge and discharge the load capacitance C_L.

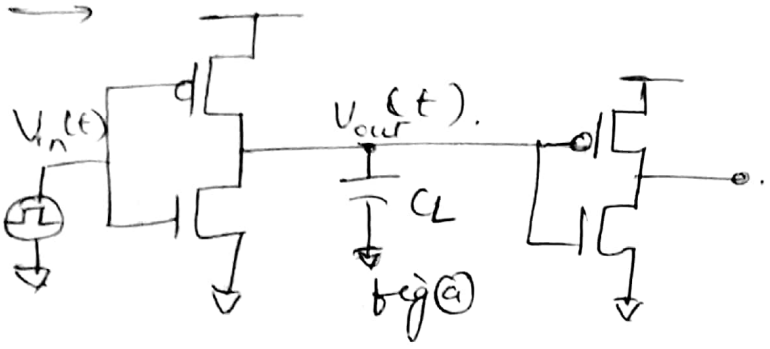


fig (a)

Rise time t_r = time for a wave form to rise from 10% to 90% of its steady state value.

Fall time t_f = time for a wave form to rise from 10% to 90% of its steady state value.

Delay time t_d = time difference b/w input transition (50%) and the 50% output level.
(This is the time taken for a logic transition to pass from input to output).

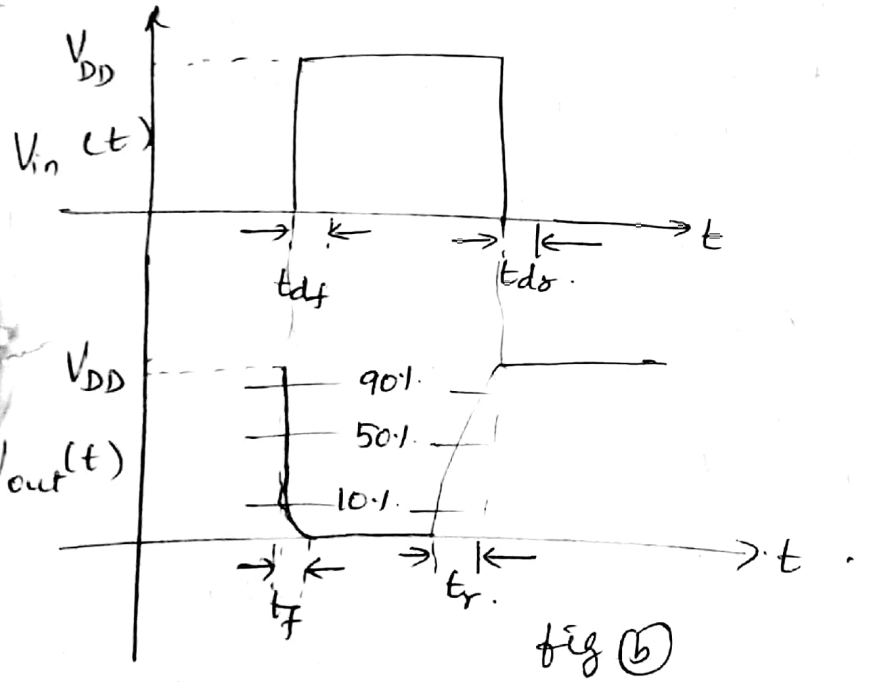


fig (b)

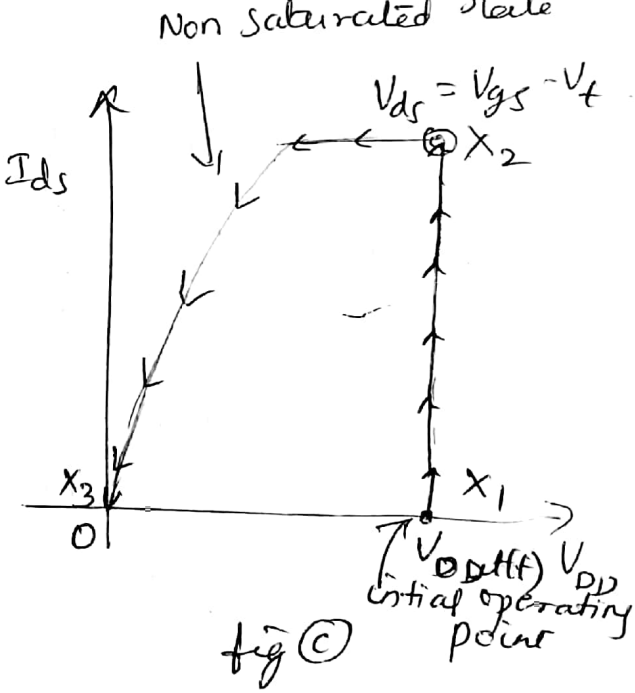


fig (c)

Switching char for cmos inverter

Analytical Delay Models :-

Fall Time

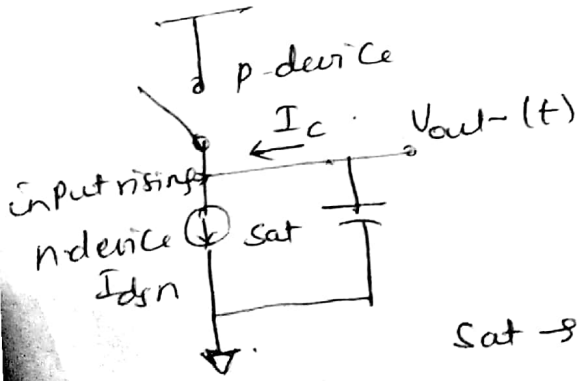
→ From fig @, the capacitance load C_L that represents the load capacitance fig (b) shows, $V_{out}(t)$ is driven by a step waveform of $V_{in}(t)$. The trajectory of the n-transistor operating point as the input voltage, $V_{in}(t)$ charges from zero volts to V_{DD}.

→ when the n-device is cut off and the load capacitor C_L is charged to V_{DD} and it is represented by X_1 on the characteristic curve and at the input of inverter charges the operating point to X_2. and then trajectory moves on the $V_{gs} = V_{DD}$ characteristic curve toward point X_3 at the origin.

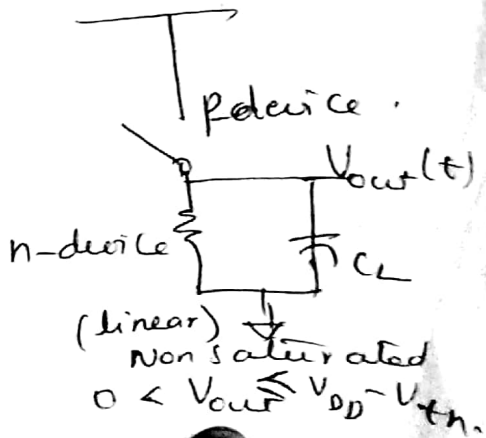
t_f → fall time consists of two intervals :-

1. t_{f1} = period during which the capacitor voltage V_{out} drops from $0.9\,V_{DD}$ to $(V_{DD} - V_{tn})$.
2. t_{f2} = period during which the capacitor voltage V_{out}, drops from $(V_{DD} - V_{tn})$ to $0.1\,V_{DD}$.

The equivalent circuits for the fall and rise-time determination



sat → $V_{out} \geq V_{DD} - V_{tn}$



process must ... generally ...

The ② while in Saturation, (2)

$$C_L \frac{dV_{out}}{dt} + \frac{\beta_n}{2}(V_{DD} - V_{tn})^2 = 0$$

Integrating from $t = t_1$, corresponding to $V_{out} = 0.9V_{DD}$ to $t = t_2$ corresponding to $V_{out} = (V_{DD} - V_{tn})$ results in

$$t_{f1} = 2\frac{C_L}{\beta_n (V_{DD} - V_{tn})^2} \int_{V_{DD}-V_{tn}}^{0.9V_{DD}} dV_{out} = \frac{2C_L (V_{tn} - 0.1V_{DD})}{\beta_n (V_{DD} - V_{tn})^2}$$

When the ② device begins to operate in linear region, the discharge current is no longer constant. The time t_{f2} taken to discharge the capacitor voltage from $(V_{DD} - V_{tn})$ to $0.1V_{DD}$

$$t_{f2} = \frac{C_L}{\beta_n (V_{DD} - V_{tn})} \int_{0.1V_{DD}}^{V_{DD}-V_{tn}} \frac{dV_{out}}{\frac{V_{out}^2}{2(V_{DD}-V_{tn})} - V_{out}}$$

$$= \frac{C_L}{\beta_n (V_{DD} - V_{tn})} \ln\left(\frac{19V_{DD} - 20V_{tn}}{V_{DD}}\right)$$

$$t_{f2} = \frac{C_L}{\beta_n V_{DD}(1-n)} \ln(19 - 20n)$$

where $n = V_{tn}/V_{DD}$.

The complete term for the falltime t_f is

$$t_f = 2\frac{C_L}{\beta_n V_{DD}(1-n)} \left[\frac{(n-0.1)}{(1-n)} + \frac{1}{2}\ln(19 - 20n)\right]$$

$$\boxed{t_f = k \times \frac{C_L}{\beta_n V_{DD}}}$$

The delay is $\propto$ le to load capacitance

$\boxed{t_f \propto kC_L}$

~~known as Metal Silicon~~

~~Secondly, it is inversely proportional to supply voltage.~~

$$t_f = \frac{k C_L}{\beta_n V_{DD}}$$

k = 3 to 4 values

V_{tn} = 0.5 to 01 volt.

V_{DD} = 3 to 5 volts

→ These 3 points form the major basis by which cmos designer optimize speed of cmos

(*) The delay is directly proportional to load capacitance. To achieve high Speed circuit one has to minimize the load capacitance seen by gate.

Secondly, the delay is inversely proportional to supply voltage.

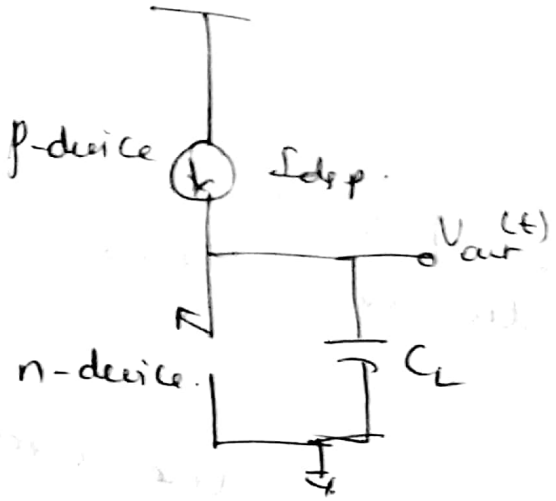
(*) As the supply voltage is raised the delay time is reduced. Thus lowering the supply voltage on a circuit will reduce the speed of the gates in that circuit.

(*) Finaly, the delay is inversely proportional to the β of the driving transistor.

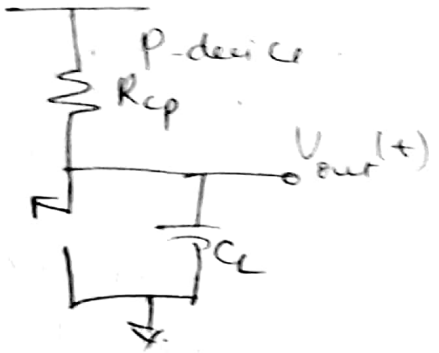
(*) As the width of a transistor is increased or length is decreased, the delay for that transistor decreases.

If t_f ...

Fall time (input)



Sat : $V_{out} \leq |V_{tp}|$



Non saturated $|V_{tp}| < V_{out} < V_{DD}$

Due to the symmetry of the CMOS ckt, we can obtain for t_r (rise time).

$$t_r = 2 \frac{C_L}{\beta_p V_{DD} (1-P)} \left[\frac{(P-0.1)}{(1-P)} + \frac{1}{2} \ln (19-20P) \right]$$

with $P = \frac{|V_{tp}|}{V_{DD}}$

$$t_r = 3 \longrightarrow 4 \frac{C_L}{\beta_p V_{DD}}$$

For equally sized n & p transistors $\beta_n = 2\beta_p$

$$\boxed{t_f = \frac{t_r}{2}}$$

The fall time is faster than rise time, due difference carrier mobilities associated with p & n devices ($\mu_n = 2\mu_p$)

If a metal line ...

we have to approximately the same open ... in an inverter rise & fall time for an

$$\frac{\beta_n}{\beta_p} = 1$$

Thus the channel width for p device must be increased to appr two or 3 times that of the n-device

$$W_p = 2\text{-}3\, W_n$$

To accurately specify the width ratio required to achieve equal rise & fall times, an accurate ratios of β_n & β_p must be known.

Delay time :-

In cmos circuits, the delay of a single gate is dominated by the output rise and fall time.

$$t_{dr} = \frac{t_r}{2} \quad \& \quad t_{df} = \frac{t_f}{2}$$

An alternative formulation is given by.

$$t_{df} = A_N \frac{C_L}{\beta_n}$$

Where, A_N is a process constant for a specific supply voltage.

$$A_N = \frac{1}{V_{DD}(1-n)} \left[\frac{2n}{1-n} + \ln \left(\frac{2(1-n) - V_O}{V_O} \right) \right]$$

Where $n = \frac{V_{tn}}{V_{DD}}$, $V_O = \frac{V_{out}}{V_{DD}}$.

for $V_{tn}=0.7V$, $V_{DD}=5V$, $V_{out}=2.5$ volts, A_N is 0.36

$$t_{d_r} = A_p \frac{C_L}{\beta_p}$$

$A_p \rightarrow$ process constant for a specific supply voltage.

$$A_p = \frac{1}{V_{DD}(1+P)}\left[\frac{-2P}{1+P} + \ln\left(\frac{2(1+P)-V_0}{V_0}\right)\right]$$

where $P = \frac{V_{tp}}{V_{DD}}$

For $V_{tp}=-0.7$, $V_{DD}=5$, $V_{out}=2.5$, $A_p \rightarrow 0.283$.

The Average gate delay for rising and falling transition is

$$t_{av} = \frac{t_{df}+t_{dr}}{2}$$

Empirical Delay Model:-

In empirical delay model, a circuit simulator is used to model the inverter or gate in question. and measured values are back substituted into appropriate delay equations.

$$t_{df} = A_N \frac{C_L}{\beta_n} \quad \text{--- (1)} \qquad t_{dr} = A_p \frac{C_L}{\beta_p} \quad \text{--- (2)}.$$

and for simulation $\boxed{\omega_p = 2\omega_n}$ Given $t_{df\,spice}=0.$

$$A_p = t_{dr\text{-}spice}\frac{\beta_p}{C_L} = .52\times10^{-9} \times \frac{3.49\times10^{-4}}{0.5\times10^{-12}} = 0.36. \qquad t_{df\text{-}spice}=0.45n$$

$$A_N = t_{df\text{-}spice}\frac{\beta_n}{C_L} = 0.45\times10^{-9} \times \frac{4.04\times10^{-4}}{0.5\times10^{-12}} = 0.36.$$

$$t_{dr} = 0.36 \frac{C_L}{\beta_p}$$

$$t_{df} = 0.36 \frac{C_L}{\beta_n}$$

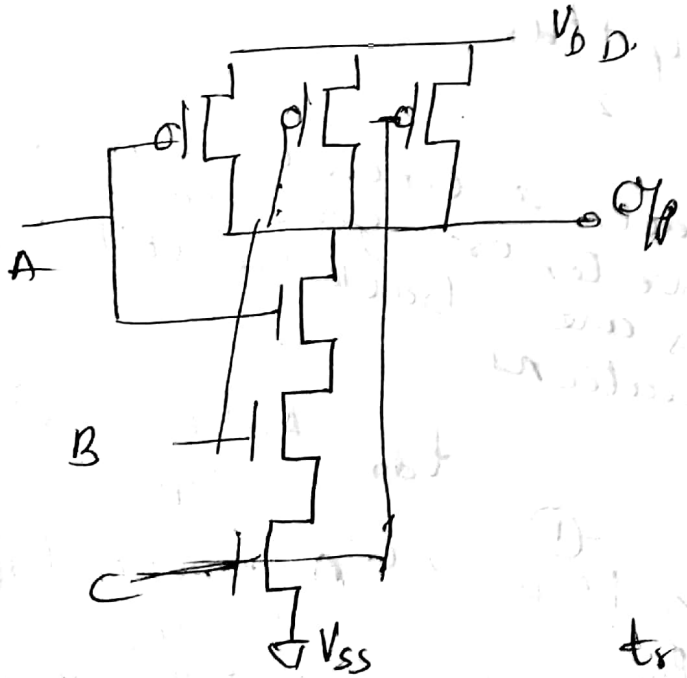
Gate Delays

(*) The delay of simple gates may be approximated by constructing an equivalent inverter.

Ex:- 3-input NAND gate.

~~$Y = A + B +$~~ $Y = \overline{ABC}$

$Y = \bar{A} + \bar{B} + \bar{C}$



$$\beta_{neff} = \frac{1}{\frac{1}{\beta_{n1}} + \frac{1}{\beta_{n2}} + \frac{1}{\beta_{n3}}}$$

for $\beta_{n1} = \beta_{n2} = \beta_{n3}$

$$\beta_{neff} = \frac{\beta_n}{3}$$

$$\boxed{\beta_{eff} = \beta_p}$$

for $\beta_p = 0.3\beta_n$.

$$t_r = k\frac{C_L}{0.3\beta_n V_{DD}}, \quad t_f = k\frac{C_L}{\frac{\beta_n}{3} V_{DD}}$$

$$\frac{t_r}{t_f} = \frac{kC_L}{0.3\beta_n V_{DD}} \times \frac{\frac{\beta_n}{3} V_{DD}}{kC_L}$$

$$= 1$$

· Series transistor Connection

ex:- 3 n-Tr in series

* Three Transistors of same width & length is series brought closer together.

* The resulting transistor has a length 3L

$$\beta_{series} = \frac{\beta_n}{3}$$

and hence $\tau_{series} = k \frac{C_L}{\frac{\beta_n}{3} V_{DD}}$.

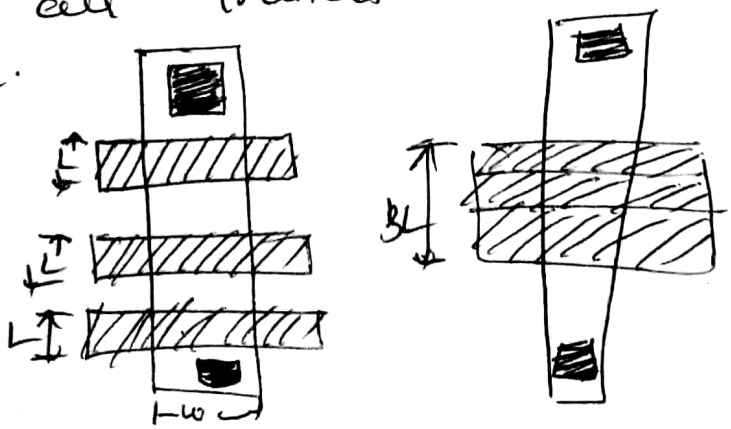
which is 3 times the delay time for one transistor.

In general, the fall time t_f is mt_f for m n-transistors in series.

Why, the rise time t_r for k p-transistors in series is kt_r.

In Comparison, the fall time 't_f' for a parallel Connection of transistors is t_f/m for m-transistors is parallel, if all the transistors are turned on simultaneously.

* For k p-transistors in parallel ~~the transistors are turned on simultaneously~~. the rise time is t_r/k for k devices in parallel if all transistors are turned on simultaneously.

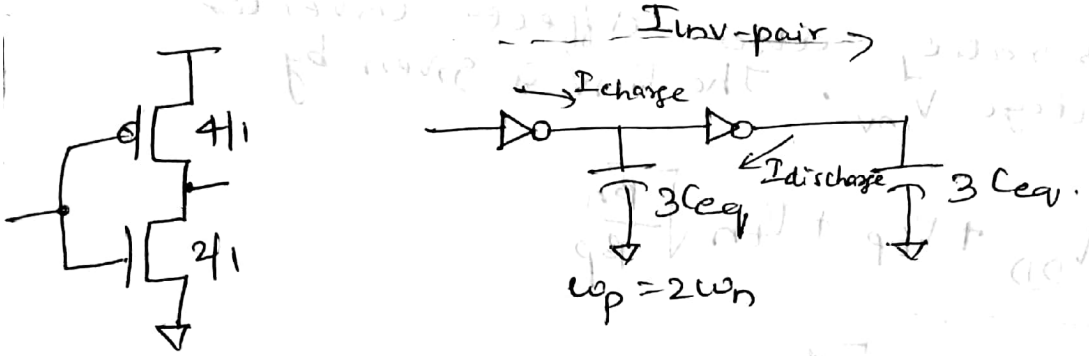


10S - Gate Transistor sizing

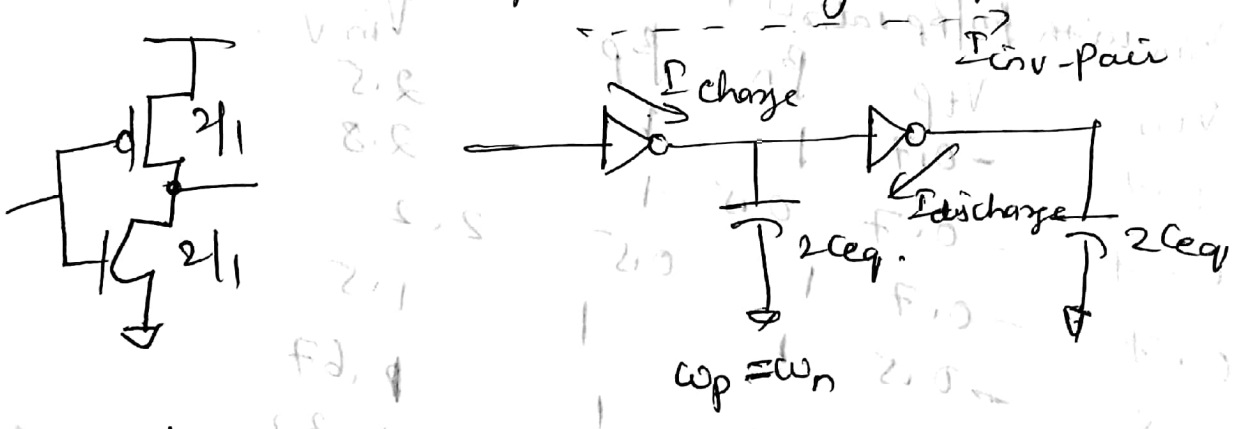
Cascaded complementary inverters

To approximate the same rise and fall times for an inverter, for current cmos process, we must make $w_p \approx (2 \to 3) \times w_n$.

$w_p \to$ channel width of p-device
$w_n \to$ —"— n-device



cmos inverter pair timing response.



The delay response for an inv pair with $w_p = 2w_n$ is given by

$$t_{inv\ pair} \propto t_{fall} + t_{rise}$$
$$\propto R\,3C_{eq} + \frac{2R}{2}\,3C_{eq}.$$
$$\propto 3RC_{eq} + 3RC_{eq}.$$
$$\propto 6RC_{eq}.$$

R → effective "on" resistance of a unit n-transistor & $C_{eq} = C_g + C_d$ is the capacitance of a unit-sized gate and drain region.

The inverter pair delay, with $w_p = w_n$ is

$$t_{inv\text{-}pair} \propto t_{fall} + t_{rise}$$
$$\propto R2C_{eq} + 2R2C_{eq}$$
$$\propto 6RC_{eq}$$

Changes in β ratio also affect inverter threshold voltage V_{inv}. The V_{inv} is given by

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}$$

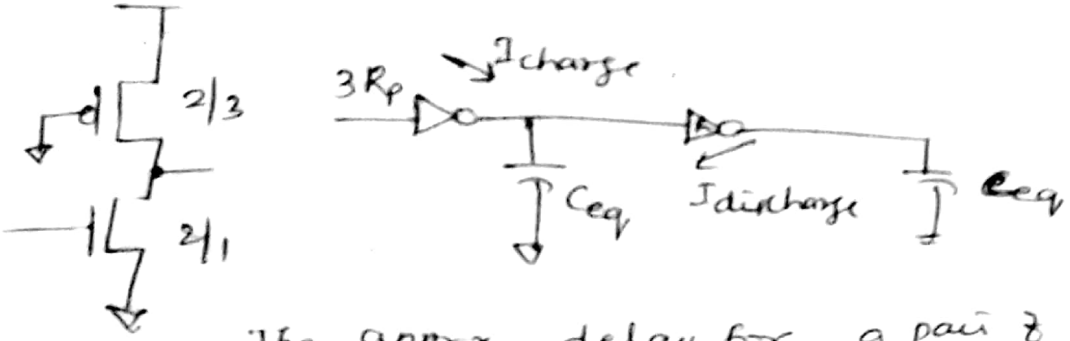
Variation V_{inv} with β_n/β_p ratio.

V_{DD}	V_{tn}	V_{tp}	β_n	β_p	V_{inv}
5	0.7	-0.7	1	1	2.5
5	0.7	-0.7	0.5	1	2.8
5	0.7	-0.7	1	0.5	2.2
5	0.7	-0.7	1	1	1.5
3	0.5	-0.5	1	1	1.67
3	0.5	-0.5	0.5	0.5	1.32
3	0.5	-0.5	1	0.5	for these β ratios.

∠ 15% variation in V_{inv}

This optimization does not apply when the circuits have to drive any significant routing load, and n & p transistors should be sized to yield equal rise & fall times

Cascaded pseudo - nmos inverters :-



The approx delay for a pair of inverters is

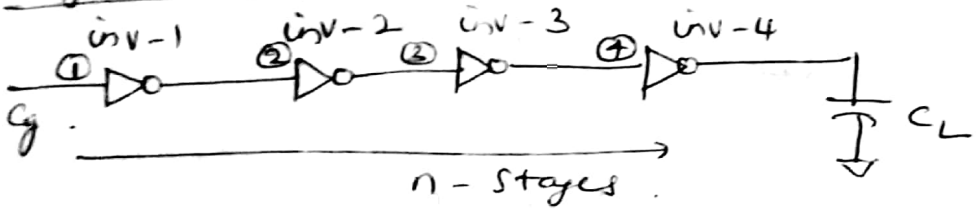
$t_{inv-pair} \propto 6R(C_g + 2C_d) + R(C_g + 2C_d)$

$\propto TRC_{eq}$

$C_{eq} = C_g + 2C_d$

speed may be improve by sacrificing noise margins (making the pullup stronger).

Stage Ratio :-



→ It is desired to drive large load capacitances such as long buses, I/O buffers, or pads and off-chip capacitive loads. and it is achieved by using a chain of inverters, where each successive inverters is made larger than previous one until the last inverter in the chain can drive the large load in the time reqd.

constant

ln(R) depends on the ratio of internal to external load and is constant for a given load and process

$$a_{opt} = e^{\frac{k + a_{ops}}{a_{ops}}}$$

k = intrinsic output load capacitance and input gate capacitance of an inverter.

Power Dissipation :-

Two components that establish the amount of power dissipated in a CMOS circuit.

(a) Static dissipation
→ Due to leakage current or other current drawn continuously from the power supply.

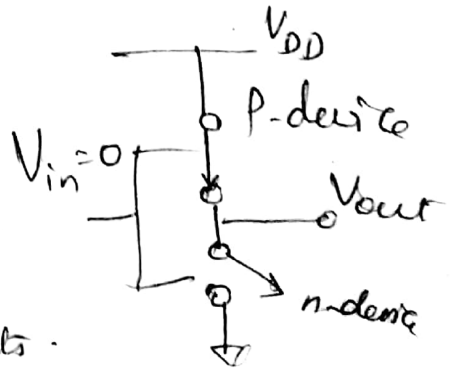
(a) Dynamic Dissipation
→ switching transient current
→ charging and discharging of load capacitances

Static Dissipation :-

→ If input = '0', the n-device is 'off' & p-device is 'ON' and output voltage is V_{DD} or logic '1'.

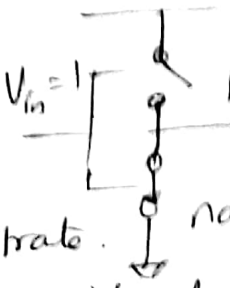
When input = '1', the associated n-channel device is biased 'ON' & P-ch device is 'off' the output voltage is '0' volts.

→ one of the transistors is always 'off' when the gate is either of their logic states.



CMOS inverter model for static Power dissipation.

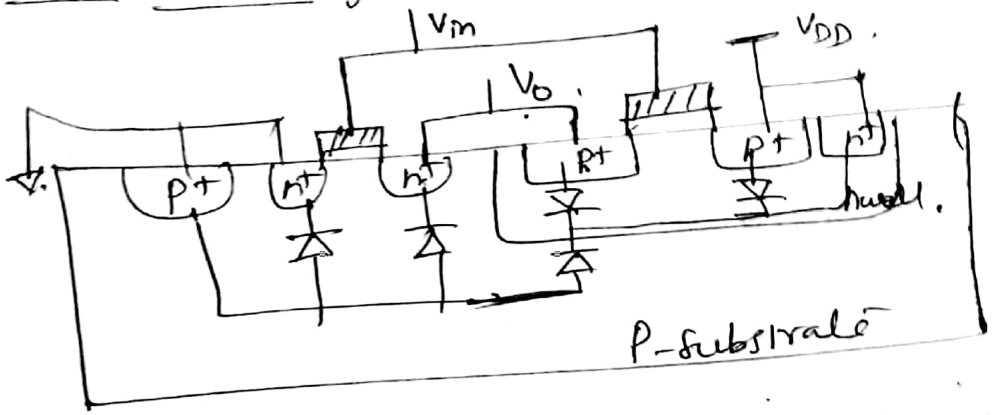
→ No current flows into the gate terminal and there is no DC current path from V_{DD} to V_{SS} and resultant quiescent (Steady-~~Barrent~~ state) current & hence (static) power P_S is zero.



→ small static dissipation due to reverse bias leakage b/w ~~refi~~ diffusion regions & the substrate.

→ Sub threshold conduction can contribute to the static dissipation.

Model describing Parasitic diodes present in CMOS inverter



④ The source-drain diffusions and the n-well diffusion form parasitic diodes.

⑤ In the model, a parasitic diode is shown b/w n-well and substrate.

Since ~~diss~~ parasitic diodes are reverse biased, only their leakage current contributes to static power dissipation.

⑥ The leakage current is described by the diode eqn

$$i_D = i_S (e^{qV/KT} - 1)$$

i_S = reverse saturation current.

V = diode current.

q = electronic charge ($1.6 \times 10^{-19} C$)

K = Boltzmann's constant (1.38×10^{-23} J/K)

T = Temperature.

The static power dissipation is the product of the device leakage current and the supply voltage.

$i_s \rightarrow$ 0.1nA to 0.5nA / device at room temp.

The total static power dissipation, P_S is obtained from:

$$P_S = \sum^{n} \text{leakage current} \times \text{Supply voltage.}$$

n = no of devices.

ex:- static power dissipation due to leakage for an inverter operating at 5V is 4nw 1⁄2 nw.

ex:- A device $k_p = 30\mu A/V^2$ & $k_n = 55\mu A/V^2$ $V_{tn} = |V_{tp}| = 0.7V, V_{DD} = 5V$) calculate static power dissipation of a 32×32 Rom which contains a 1:32 pseudo-nmos row decoder & pmos pull ups on the 32-bit lines.

The aspect ratio of all pmos pull ups (W/L) is 1

Ans: pmos load can source $\frac{(k(V_{gs} - V_t)^2)}{2}$ of current

$$I_{load} = \frac{(30(5-0.7)^2)}{2} = 277\mu A$$

$$P_{load} = (277\mu A \times 5) = 1.4mw$$

$$P_{total} = 17 \times 1.4mw = 23.6mw.$$

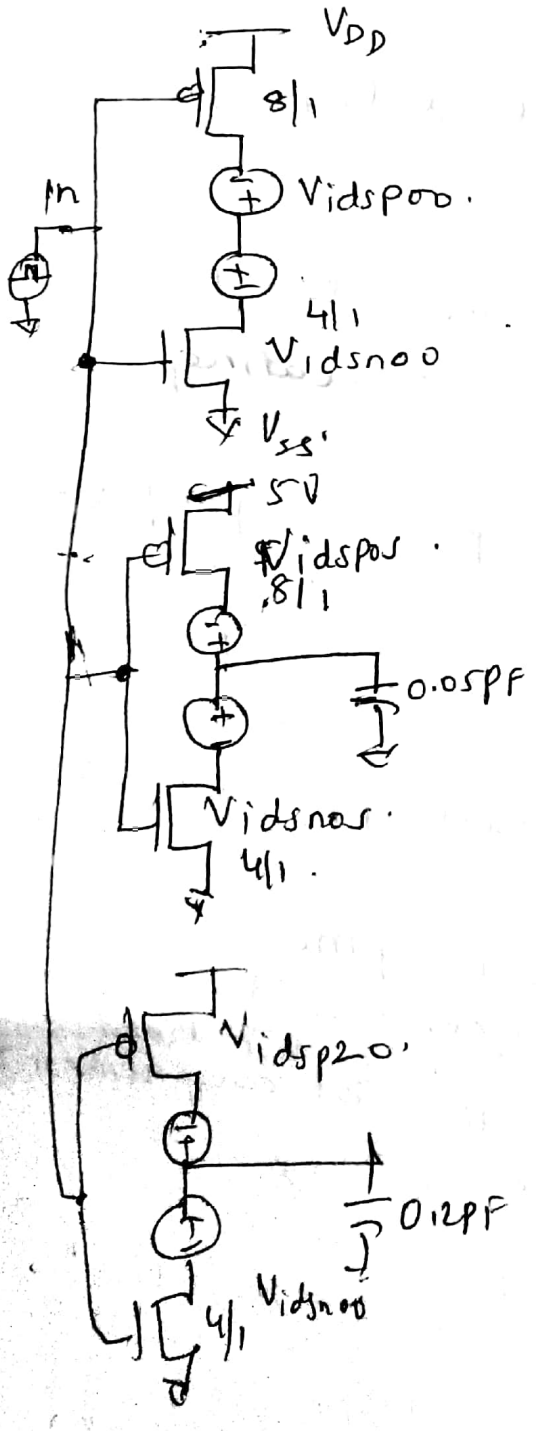
one row decoder is on (50% of bit lines are on at any time) $\frac{32}{2} = 16$ $\frac{32}{2}$

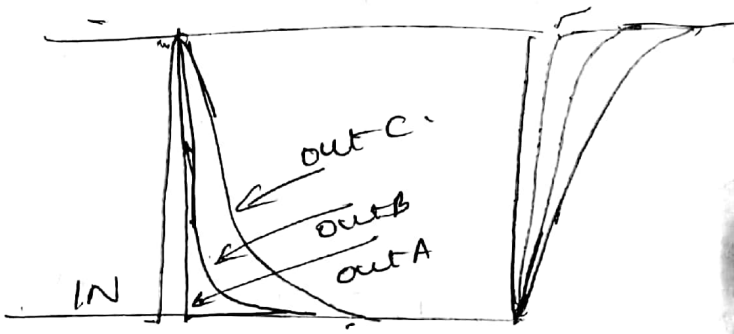
(16+1)

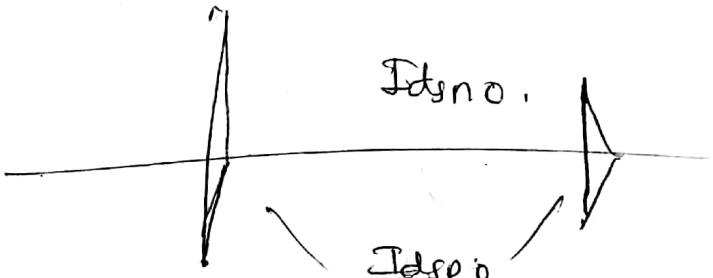
Dynamic Dissipation :-

(*) During transition from either '0' to '1' or alternatively from '1' to '0' both n & P transistors are on for a short period of time. and this results in a short current pulse from V_{DD} to V_{SS}.

(*) The current pulse from V_{DD} to V_{SS} results in a "short circuit dissipation that is dependent on the input rise/fall time, the load Capacitance & gate design.







Short circuit current

Capacitor current.