Tony Nowatzki

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Research Interests

Computer Architecture

- Designing programmable accelerators which balance generality and efficiency
- Compilers and run-time systems for transparent and dynamic optimization
- Design and compiler-development automation for programmable hardware

Mathematical Modeling and Optimization

- Using mathematical optimization to explore design trade-offs and comprehend complex systems
- Generalized instruction scheduling techniques using mathematical optimization

Education

University of Wisconsin , Madison (4.00) • Ph.D. in Computer Sciences (Fall 2016)

University of Wisconsin , Madison (4.00) • MS in Computer Sciences (Spring 2011)

University of Minnesota , Twin Cities (3.95) • B.S. in Comp. Sciences & Comp. Engineering, (Spring 2009)

Awards and Honors

- IEEE Micro Top Picks, 2017
- IEEE Micro Top Picks, 2016
- Best of CAL, 2015
- Publication Nominated to SIGARCH for a CACM Research Highlights, 2015
- Google PhD Fellowship in Computer Architecture, 2014
- Distinguished Paper Award, PLDI 2013
- Publication Nominated by SIGPLAN for a CACM Research Highlights, 2013
- University of Wisconsin Alumni Scholar, 2009
- Roger M. Norby Engineering Scholarship, 2007
- John Tate Scholarship, 2006

Academic Experience

University of California Los Angeles, PolyArch Research Group (January 2017–Present)
Assistant Professor

- Forming the PolyArch research group to study design of heterogeneous programmable processors and their compilers.

University of Wisconsin,Vertical Research Group (June 2010–December 2016)
Research Assistant

- Design and evaluation of modular general purpose processor architecture, including several in-core dataflow architectures.
- Modeling techniques for fundamentally understanding and designing programmable accelerators.
- Mathematical optimization-based compiler for general spatial scheduling using Integer Linear Programming.

University of Wisconsin, Department of Computer Sciences (Fall 2009–Spring 2011)
Teaching Assistant

- Worked with professors to develop curriculum for two courses in computer architecture.
- Gained leadership experience teaching in a classroom and in one-on-one environments.

University of Minnesota, Digital Technology Center (2005–2009)
Research Assistant

- Worked with a team to organize and run large scale physics simulations on clusters and super computers.

- Lead developer on C# application for visualizing 3D volumetric data, which leveraged a cluster of rendering nodes for real-time data exploration and cinematic capture/playback.

Industry Experience

Qualcomm, Qualcomm Research Silicon Valley (Summer 2011 & 2012)
Internship

- Implementing and evaluating next-generation dynamic compilers.

Conference Publications

- T. Nowatzki, V. Gangadhar, K. Sankaralingam. Stream-Dataflow Acceleration *ISCA*, 2017.
- T. Nowatzki, V. Gangadhar, K. Sankaralingam, G. Wright. Pushing the Limits of Accelerator Efficiency While Retaining General-Purpose Programmability. *HPCA*, 2016. **Selected for IEEE Micro Top Picks 2017**
- T. Nowatzki, K. Sankaralingam. A Framework and Analysis of Behavior Specialized Accelerators. *ASPLOS* 2016.
- M. Watkins, T. Nowatzki, A. Carno. Software Transparent Dynamic Binary Translation for Coarse-Grain Reconfigurable Architectures. *HPCA*, 2016.
- T. Nowatzki, V. Gangadhar, K. Sankaralingam. Exploring the Potential of Heterogeneous Von Neumann/Dataflow Execution Models. *ISCA*, 2015. **Selected for IEEE Micro Top Picks 2016**
- C. Ho, V. Govindaraju, T. Nowatzki, R. Nagaraju, Z. Marzec, P. Agarwal, C. Frericks, R. Cofell, K. Sankaralingam. Performance evaluation of a DySER FPGA prototype system spanning the compiler, microarchitecture, and hardware implementation. *ISPASS* 2015.
- T. Nowatzki, M. Sartin-Tarm, L. De Carli, K. Sankaralingam, C. Estan, B. Robatmili. A General Constraint-centric Scheduling Framework for Spatial Architectures. *PLDI*, 2013. ***Distinguished Paper Award***
- V. Govindaraju, T. Nowatzki, K. Sankaralingam. Breaking SIMD Shackles with an Exposed Flexible Microarchitecture and the Access Execute PDG. *PACT*, 2013.
- J. Benson, R. Cofell, C. Frericks, C. Ho, V. Govindaraju, T. Nowatzki, K. Sankaralingam. Design Integration and Implementation of the DySER Hardware Accelerator into OpenSPARC. *HPCA*, 2012.

Journal and Magazine Publications

- T. Nowatzki, V. Gangadhar, K. Sankaralingam, G. Wright. Domain Specialization is Generally Unnecessary for Accelerators. *IEEE Micro Top Picks in Computer Architecture*, 2017.
- G. Gupta, T. Nowatzki, V. Gangadhar, and K. Sankaralingam. Kickstarting Semiconductor Innovation with Open Source Hardware. *IEEE Computer*, 2017
- T. Nowatzki, J. Menon, C. Ho, K. Sankaralingam. Architectural Simulators Considered Harmful. *IEEE Micro, 2015.*
- A. Yazdanbakhsh, R. Balasubramanian, T. Nowatzki, K. Sankaralingam. Comprehensive Circuit Failure Prediction and Detection for Logic and SRAM using Virtual Aging, Sampled Redundancy, and Asymmetric Checkers. IEEE Micro, 2015.
- T. Nowatzki, V. Govindaraju, K. Sankaralingam, A Graph-Based Program Representation for Analyzing Hardware Specialization Approaches. *CAL*, 2015. ***Best of CAL – presented at HPCA 2016***
- T. Nowatzki, M. Sartin-Tarm, L. De Carli, K. Sankaralingam, C. Estan, B. Robatmili. A Scheduling Framework for Spatial Architectures Across Multiple Constraint-solving Theories. *TOPLAS*, 2014.
- M. Sartin-Tarm, T. Nowatzki, L. De Carli, K. Sankaralingam, C. Estan. Constraint centric scheduling guide. *SIGARCH Comput. Archit. News*, 2013.
- V. Govindaraju, C. Ho, T. Nowatzki, J. Chhugani, N. Satish, K. Sankaralingam, C. Kim. DySER: Unifying Functionality and Parallelism Specialization for Energy Efficient Computing. *IEEE Micro*, 2012.
- P. Woodward, J. Jayaraj, P. Lin, P. Yew, M. Knox, J. Greensky, T. Nowatzki, K. Stoffels. Boosting the performance of computational fluid dynamics codes for interactive supercomputing. *Int. Conf. on Membrane Computing*, 2010.

- P. Woodward, F. Herwig, D. Porter, T. Fuchs, T. Nowatzki. Nuclear burning and mixing in the first stars: Entrainment at a convective boundary using the PPB advection scheme. *AIP*, 2008.

Books

- T. Nowatzki, M. Ferris, K. Sankaralingam, C. Estan, N. Vaish, D. Wood. Optimization and Mathematical Modeling in Computer Architecture. *Synthesis Lectures on Computer Architecture*, September 2013.

Workshop Publications

- T. Nowatzki J. Menon, C. Ho, K. Sankaralingam. gem5, GPGPUSim, McPAT, GPUWattch, "Your favorite simulator here" Considered Harmful. *WDDD*, 2014.

Patents/Disclosures

- A. Yazdanbakhsh, R. Balasubramanian, T. Nowatzki, K. Sankaralingam. Computer System Predicting Memory Failure, US P150070US01, Issued March 2016
- T. Nowatzki, V. Gangadhar, K Sankaralingam. Computer with Hybrid Von-Neumann/Dataflow Execution Architecture, US P150319US01, Filed August 2015

Additional Experience

- Invited Keynote: "General Purpose Acceleration and the Challenges for Irregular Workloads", International Workshop on Architecture for Graph Processing, Toronto, June. 2017
- Invited Talk: Transparently Specialized Cores. Intel, Santa Clara, Dec. 2015
- Invited Talk: Automatic Data-Parallel Acceleration using CGRAs. Qualcomm MMR&D, San Diego, Sept. 2012
- Poster: "Prototyping the DySER Specialization Architecture with OpenSPARC", Hot Chips 24, Aug. 2012

Skills

- Programming Languages: C, C++, C#, Java, Python, Ruby (+Rails), Javascript, Fortran
- Modeling Languages: GAMS, Julia-Jump (w/ CPLEX & Gurobi)
- Kernel Experience: Linux, Android
- Compilers: LLVM Compiler Infrastructure
- Architecture Sims/Tools: Gem5, GEMS, Simplescalar, PIN, McPAT