**Circuit and Software Design**

**Fixed Challenge 2019**

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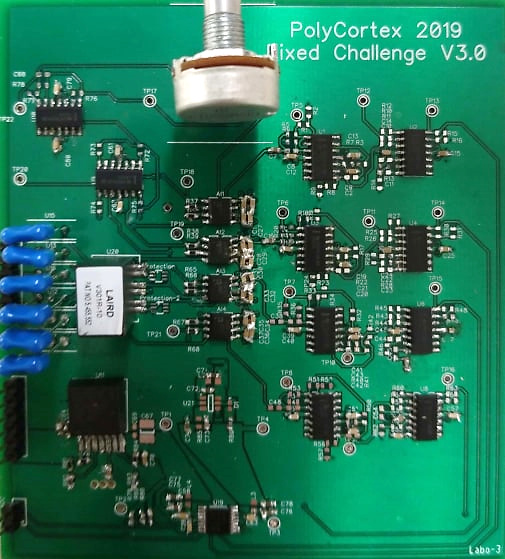
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# Circuit design – Prototype PCB, version 3.0 – Fixed Challenge 2019

## Overview of the Circuit

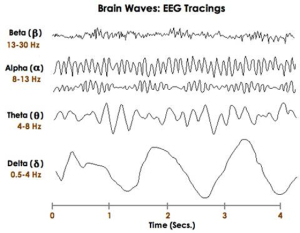
PolyCortex is a neurotechnology student organization participating in the NeuroTechX Fixed and Open Challenge competitions. The electronics team tasked with designing the circuit and PCB for the acquisition of EEG signal (Fixed Challenge) works alongside the software team in charge of programming an interface to visualize the signal.

The circuits PolyCortex has designed for this year’s fixed challenge are detailed in this document. This section covers the more ambitious prototype PCB. It is composed of 4 separate channels that can be wired to electrodes. Each channel includes filtering components (common mode chokes, RF filters), instrumentation amplifiers, various filters (high pass, low pass and notch) and a final amplification stage. Once the signal is treated and amplified, it is directed to the ADC which converts the signal from analog to digital in order to be forwarded to the interface for visualization. The circuit is powered by 9V batteries. However, the ADC is powered by ±2.5V provided by DC-to-DC converters included in the circuit. To insure the grounding standard of the board, a right leg driver (RLD) circuit configuration has been added to the board. Lastly, the subject wearing the electrodes is protected by a transient voltage suppressor (TVS).

The conception of the circuit was simulated with LTspice and implemented in the DipTrace software, which allows the creation of a schematic and layout of the PCB. It was printed by Labo Circuits Inc. and the components ordered from Digi-Key Electronics were welded by PolyCortex’s electronics team.

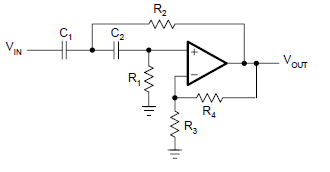
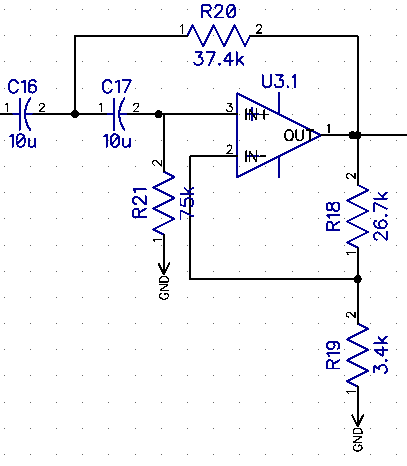
## Filtering

Due to their weak amplitudes, EEG signals are very susceptible to electromagnetic and common mode contamination. Additionally, EEG signals collected with electrodes may contain EMG information from the subject’s muscular activity and ECG signals from the polarizing cycles of heart cells. Is it thus important to filter the signal in order to isolate the frequency bands of interests for EEG analysis. The electroencephalogram is composed of 4 distinct waves ranging between 0.5 and 30Hz; the beta waves (13-30Hz), the alpha waves (8-13Hz), the theta waves (4-8Hz) and the delta waves (0.5-4Hz). PolyCortex therefore decided to filter outside of a bandwidth ranging from 0.3 to 35Hz to preserve all relevant EEG information.



*Figure 1 : Frequencies of EEG waves*

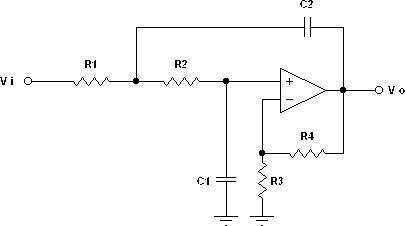
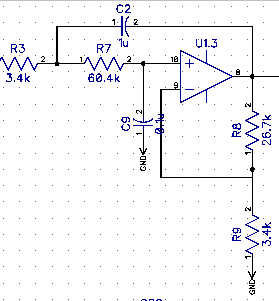
### High pass

The first filtering stage is a high pass second order Butterworth filter. The cutoff frequency *f* for such a filter is determined by the value of R2 and the value of C1 following the equation with R1=2 \* R2 and C1 = C2. PolyCortex has chosen R1 = 75kΩ, R2 =37.4kΩ and C1 = C2 = 10µF, thus providing a cutoff frequency of 0.3Hz. The remaining resistors provide a gain to the filter, as explained in the Circuit Amplification section.

*Figure 2 : High pass filter configuration (left : DipTrace schematic, right: theorical configuration)*

### Low pass

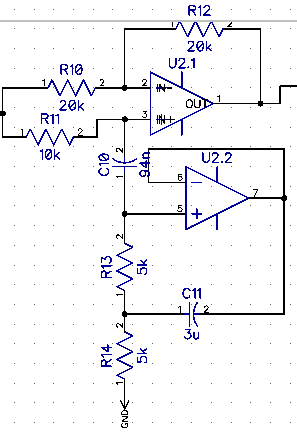
To insure the cutting off of EMG signals and other noise, the Butterworth low pass filter has a cutoff frequency of 35Hz. The cutoff frequency of this filter is given by the following equation : , referring to the right-side image of figure 3. In PolyCortex’s schematics (left-side of figure 3), these values have been set to R1 = 3.4Ωk, R2=60.4Ωk, C1= 0.1µF and C2= 1µF. Therefore, the cutoff frequency is 35Hz.



*Figure 3 : Low pass filter configuration (left : DipTrace schematic, right: theorical configuration)*

### Notch

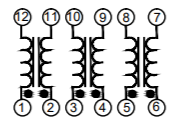
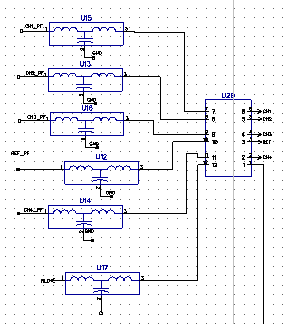
When functioning near electrical power-lines, the electronic circuits will be contaminated by the mains hum, or electric hum, which is a noise associated with the alternating current of the power-line. In PolyCortex’s case, the fundamental frequency of the mains hum is 60Hz coming from Hydro-Quebec, the local power supplier, and has an approximated intensity of 30dB. It was considered wise to add a notch filter to the circuit to target this particular noise. For the chosen notch configuration, the cutoff frequency is given by the equation : , with and (referring to the right-side of figure 4). To obtain a cutoff frequency centered around 60Hz with a gain of at least -30dB to eliminate the mains hum, PolyCortex chose values of R1 = R2 = 5Ωk, R3 = 10Ωk, R4 = R5 = 20Ωk, C1 = 94nF and C2 = 3 µF. These values produce a gain of about -36dB when simulated in LTspice (see Simulation section).



*Figure 4 : DipTrace schematic for the notch filter (cut-off frequency of 60Hz)*

### Common mode chokes

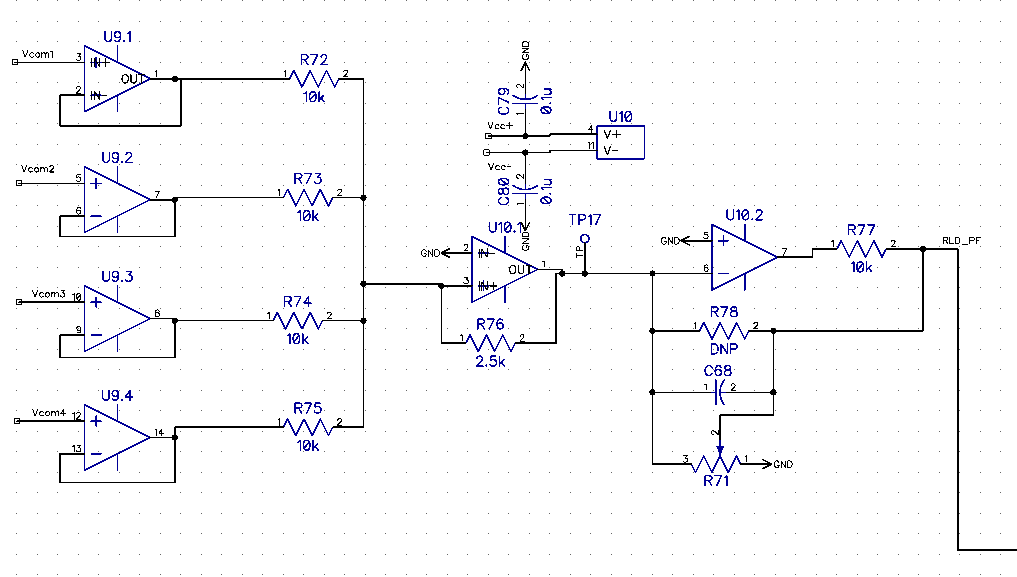
The circuit includes common mode chokes to eliminate a maximum of electromagnetic and radio frequency interferences from the power supply lines and other electronic devices. The common-mode current creates a magnetic field when passing through the coil that opposes any increase of its intensity. The magnetic field is thus blocking the common-mode current and passing differential current. PolyCortex chose CM4732V301R-10 by LAIRD, which works at a maximum rated current of 8,000mA and 30V.



*Figure 5 : DipTrace schematic of common mode chokes (left) and equivalent circuit (right)*

### Right leg driver

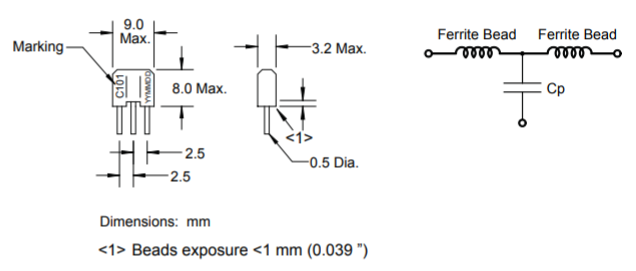
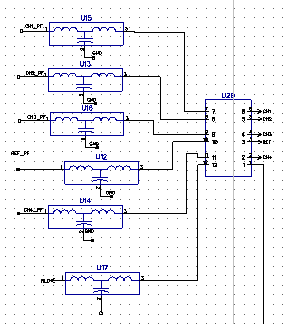
According to Texas Instruments, the common-mode rejection (CMR) is one of the most important parameters in ECG and EEG systems. Therefore, a right leg driver (RLD) circuit was added to further decrease the common-mode interference. The RLD circuit sets the user’s common-mode voltage in order to increase the effective CMR ratio of the circuit. To do so, it low-passes the common-mode voltage measured by the differential amplification stage. This method provides a grounding standard by preventing the loss of voltage due to the difference in impedance between the reference electrode on the subject and the circuit ground.



*Figure 6 : Schematic for right leg driver*

### RF filters

Radio frequency (RF) filters were added to the circuit to remove high frequency (MHz-GHz) signals originating from broadcast and wireless communication. The filtering of these frequencies is important considering they could affect the envelop of the output signal. PolyCortex uses Bourns Inc.’s EMI103T-RC filter for their good noise filtering properties, which also attenuate the mains hum with a factor of about -50dB.



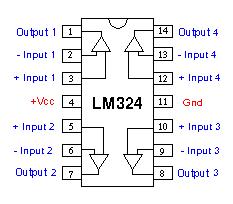
*Figure 7 : Configuration of RF filter (left : DipTrace schematic, right : functional diagram)*

## Amplification

Electrical signals coming from the human body have weak amplitudes typically ranging from 1mV to 100mV. Specifically, with regards to the electroencephalogram (EEG), the voltage that can be measured at the surface of the brain is about 1-2mV whereas it decreases to microvolts (μV) when measured on the scalp with electrodes. Thus, acquiring and visualizing EEG signals requires amplification of approximatively 50,000. Such a gain allows the manipulation of the signals without saturating properly powered operational amplifiers present in the circuit.

### Operational amplifier

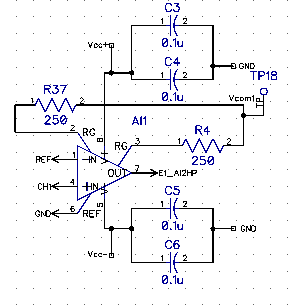
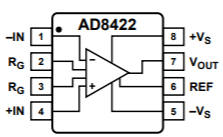
The op-amps used in the circuits are Texas Instruments’ trusted LM324. They were chosen for their built-in 4 operational amplifiers, their supply range of 3V to 32V and their typical common-mode rejection of -120dB.



*Figure 8 : Functional diagram of LM324 amp-op*

### Instrumentation Amplifier

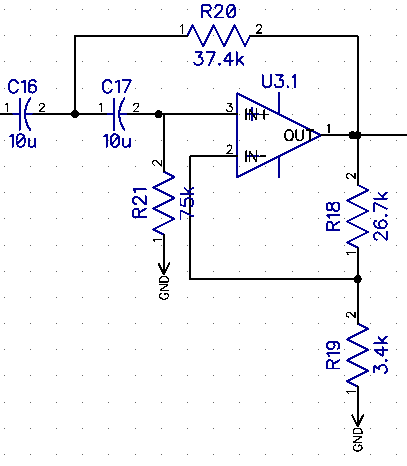
The circuit to acquire EEG signals contains operational amplifiers placed after the electrodes to provide the signal with an initial gain before being filtered. The instrumentation-amps used are Analog Devices’ AD8422, which are high performance, low power, rail-to-rail precision amplifiers. The gain is determined by placing a single resistor RG across pin 2 and 3 (figure 9). PolyCortex decided the value of this resistor would be two times 250Ω, therefore inducing a gain of 40.6 (Gain = 1 + 19.8kΩ/RG). Furthermore, the datasheet suggests placing bypass capacitors (C3, C4, C5 and C6) as close as possible to each supply pin to regulate the supply tension.

*Figure 9 : DipTrace Schematic and connection diagram of the in-op* *AD8422*

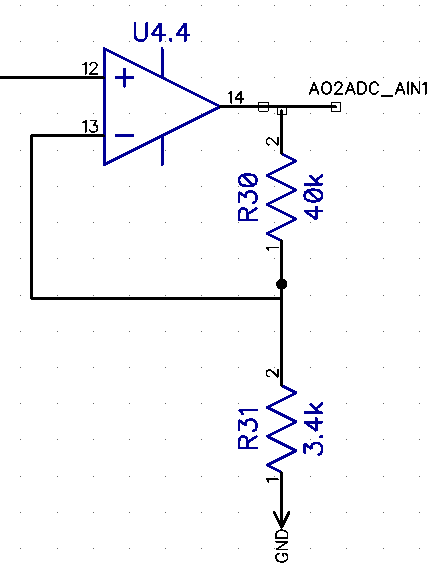
### Circuit Amplification

To obtain the expected gain of ≈50,000, the different filtering layers can also be used to introduce a gain. The filters employed in this EEG circuit are second order Butterworth active filters where two resistors, Rf and Ri (R18 and R19 on figure 10), can be connected to the output signal without affecting the cutoff frequency. Consequently, the gain of the high pass and low pass filter is proportional to the ratio of these two resistors (Gain = 1 + Rf/Ri). During the design process, PolyCortex chose to introduce a gain of 8.9 in both filtering levels.



*Figure 10 : High pass filter with a gain (G = 1 + R18/R19) of 8.9*

After the signal has made its way through the amp-op and the filtering levels, it is amplified a final time with a non-inverting operational amplifier. For this configuration, the gain is once more proportional to the ratio of the chosen resistors (Gain = 1 + Rf/Ri) R30 and R31 on figure 11.



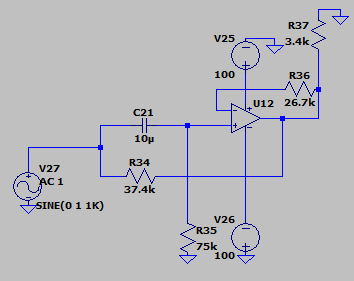
*Figure 11 : Final amplification level with a gain of 12.8 (G = 1 + R30/R31)*

The total gain produced by the cascading of the amp-op, the high pass and low pass filter and the non-inverter is thereby the multiplication of each individual gain, producing a final gain of ≈41100.

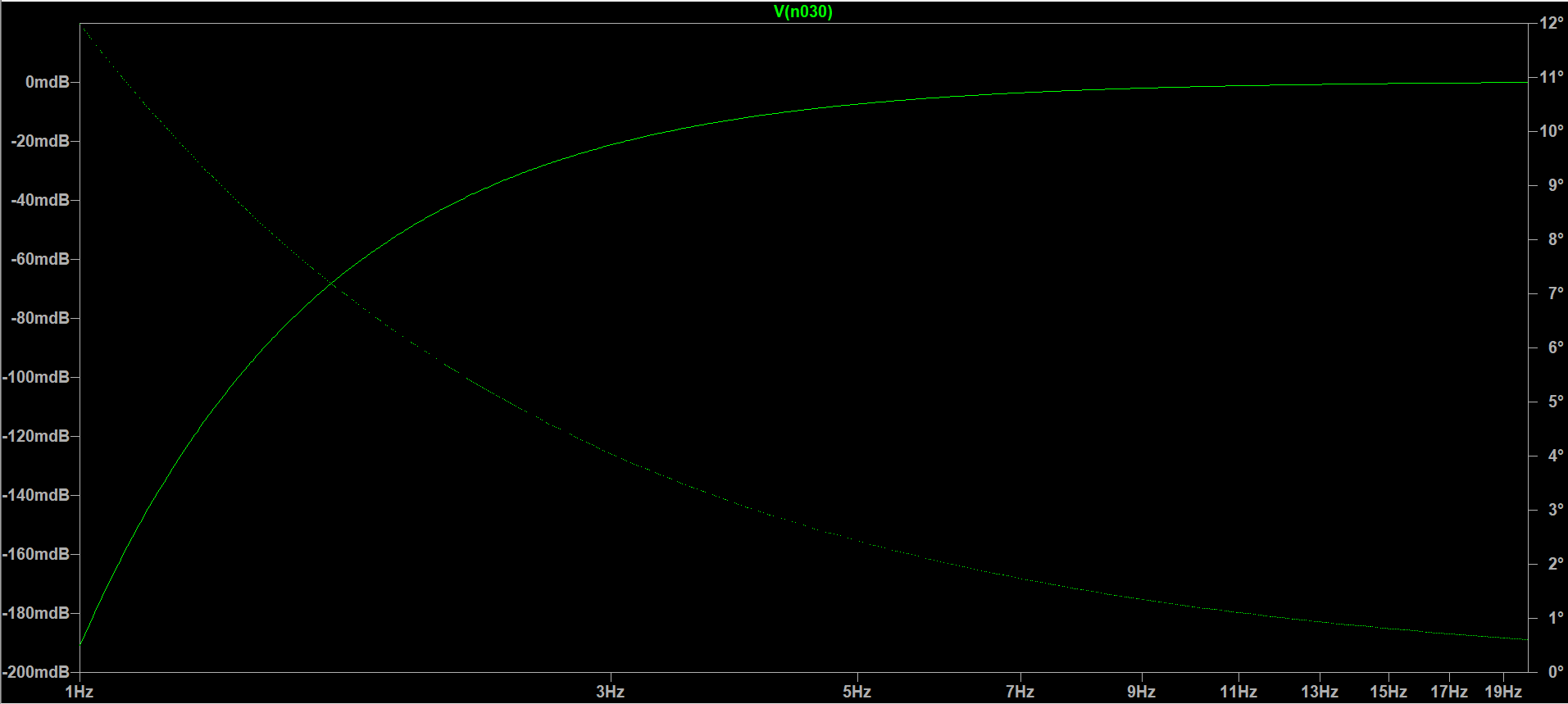
## Simulation

To insure the circuit behaves as it should, PolyCortex simulated every filtering stages with LTspice and tested the final amplification as well as the filtering capacities. In order to test the filters, a AC Analysis with 100 steps per decade, a start frequency of 0.1Hz and a stop frequency of 200Hz. This kind of analysis allows the visualizing of the circuit’s frequency response between the start and stop frequency and displays the Bode plot.

### High pass filter



*Figure 12 : LTspice schematic of the high pass filter*

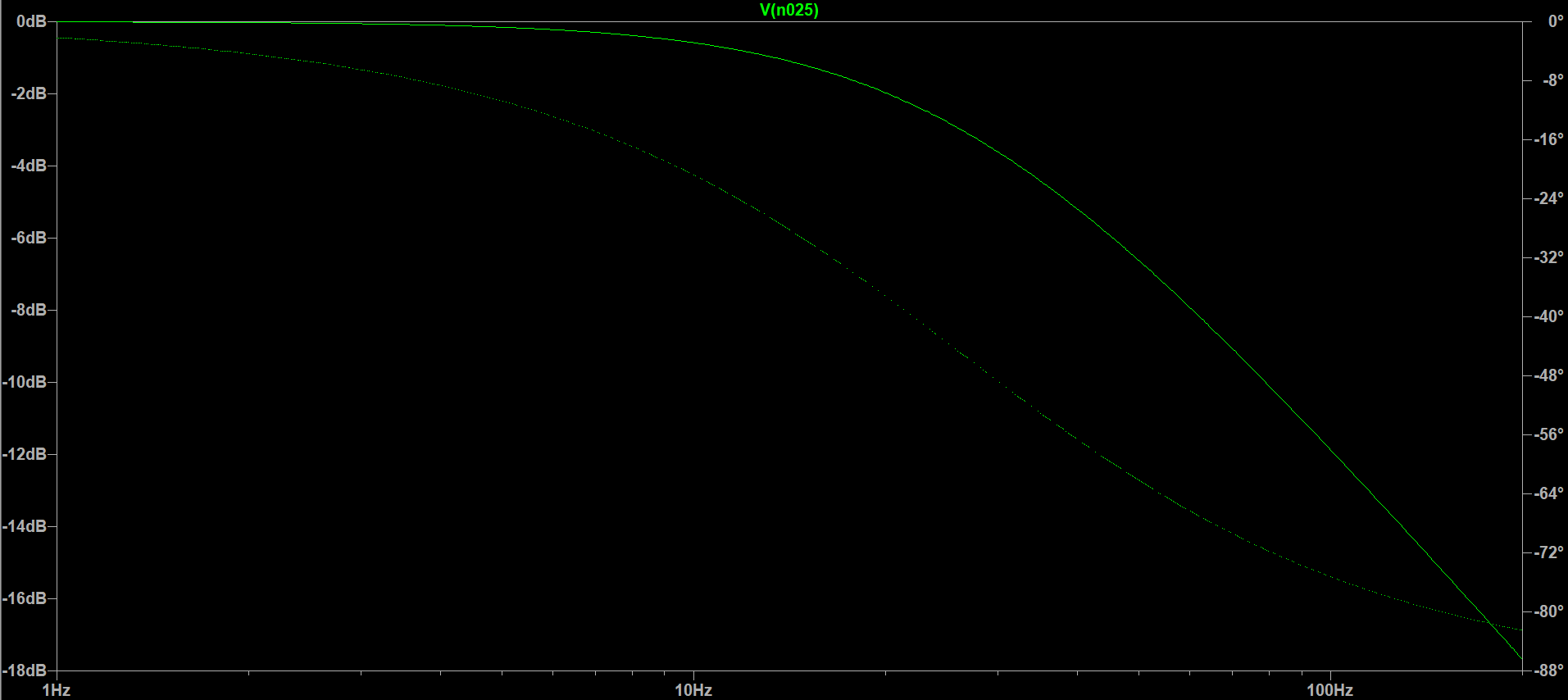


*Figure 13 : Bode plot of high pass filter with a cutoff frequency of 0.3Hz*

### Low pass filter

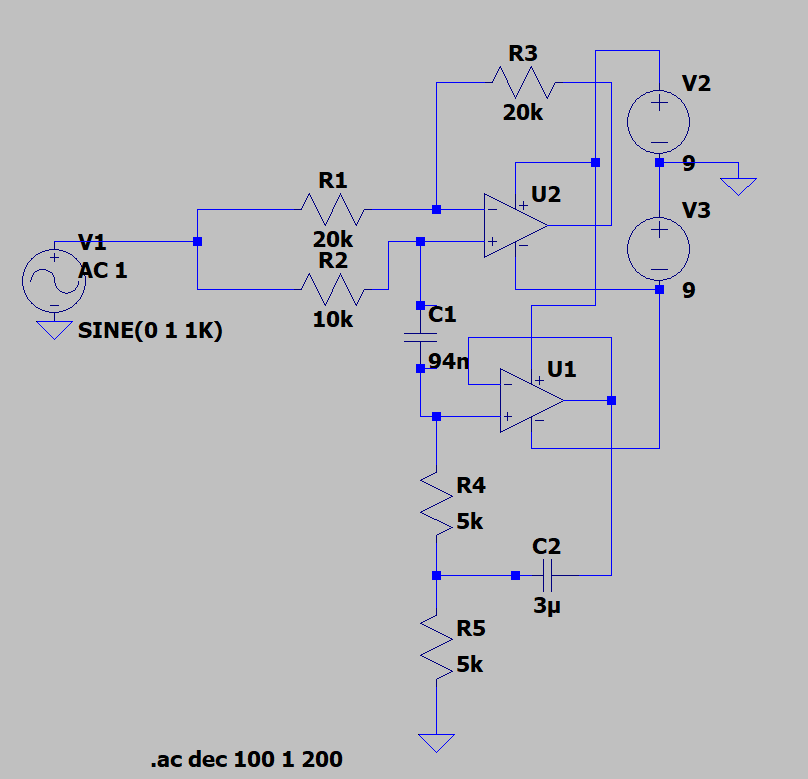


*Figure 14 : LTSpice schematic of low pass filter*

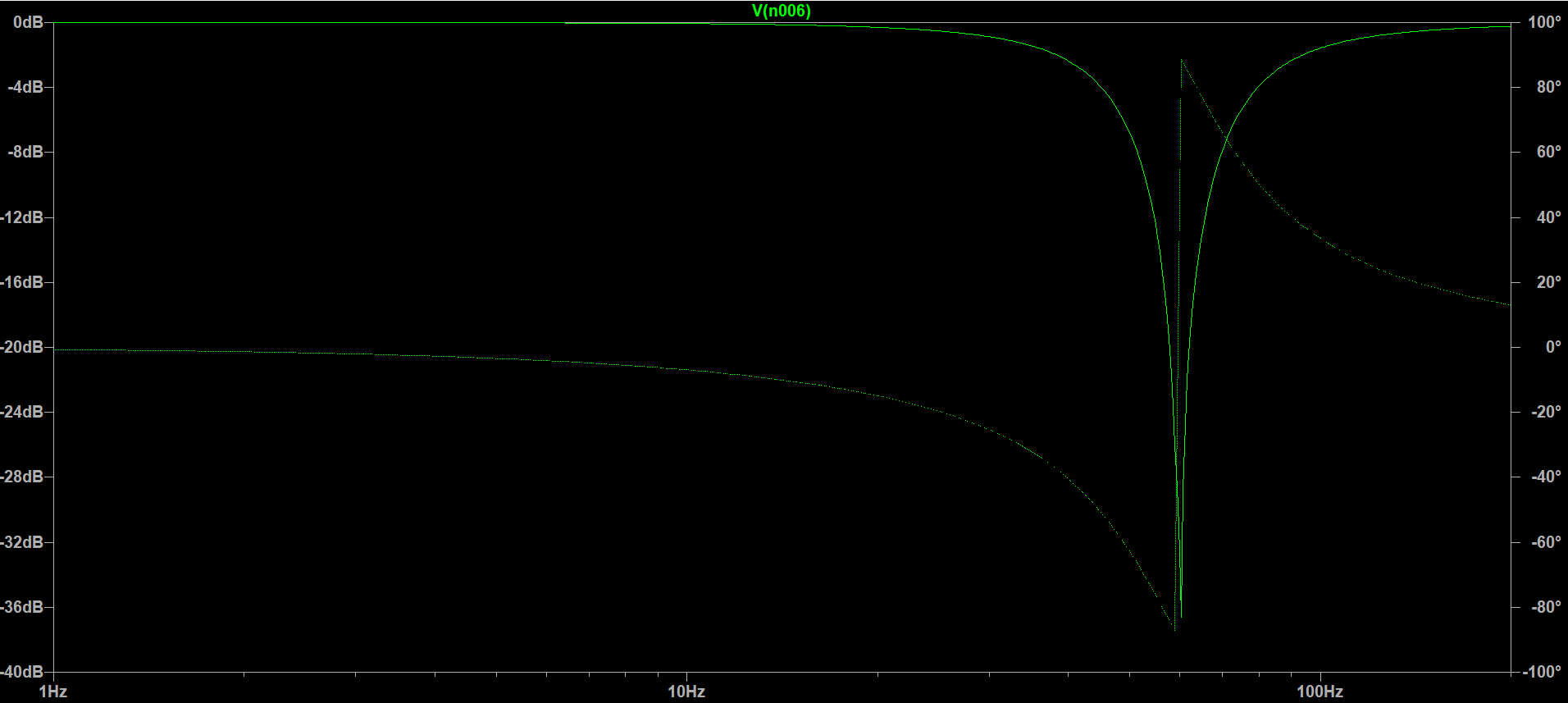


*Figure 15 : Bode plot of low pass filter with a cut off frequency of 35Hz*

### Notch



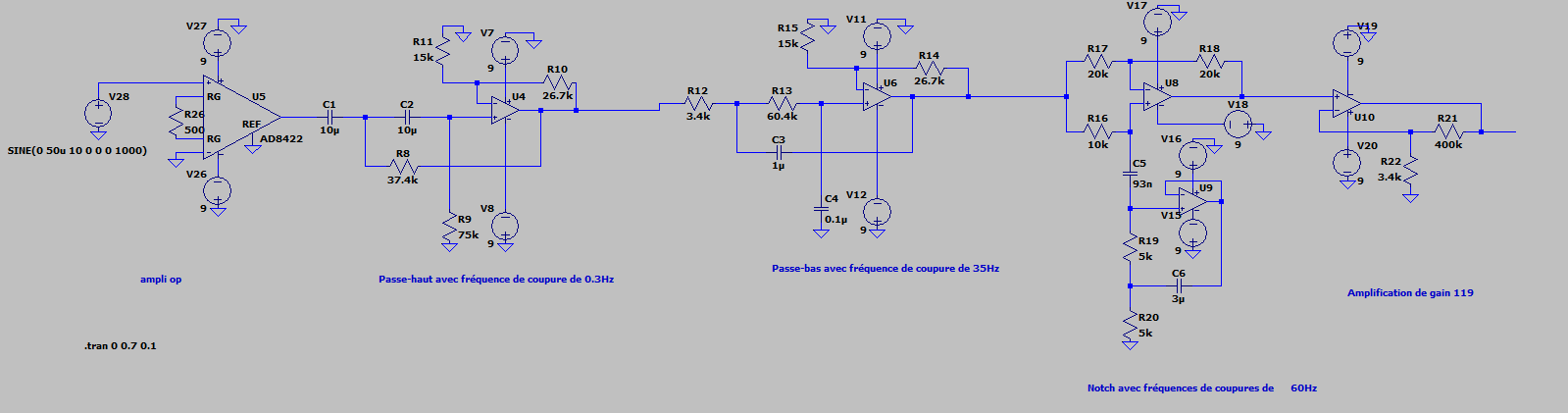
*Figure 16 : LTspice schematic of notch filter*



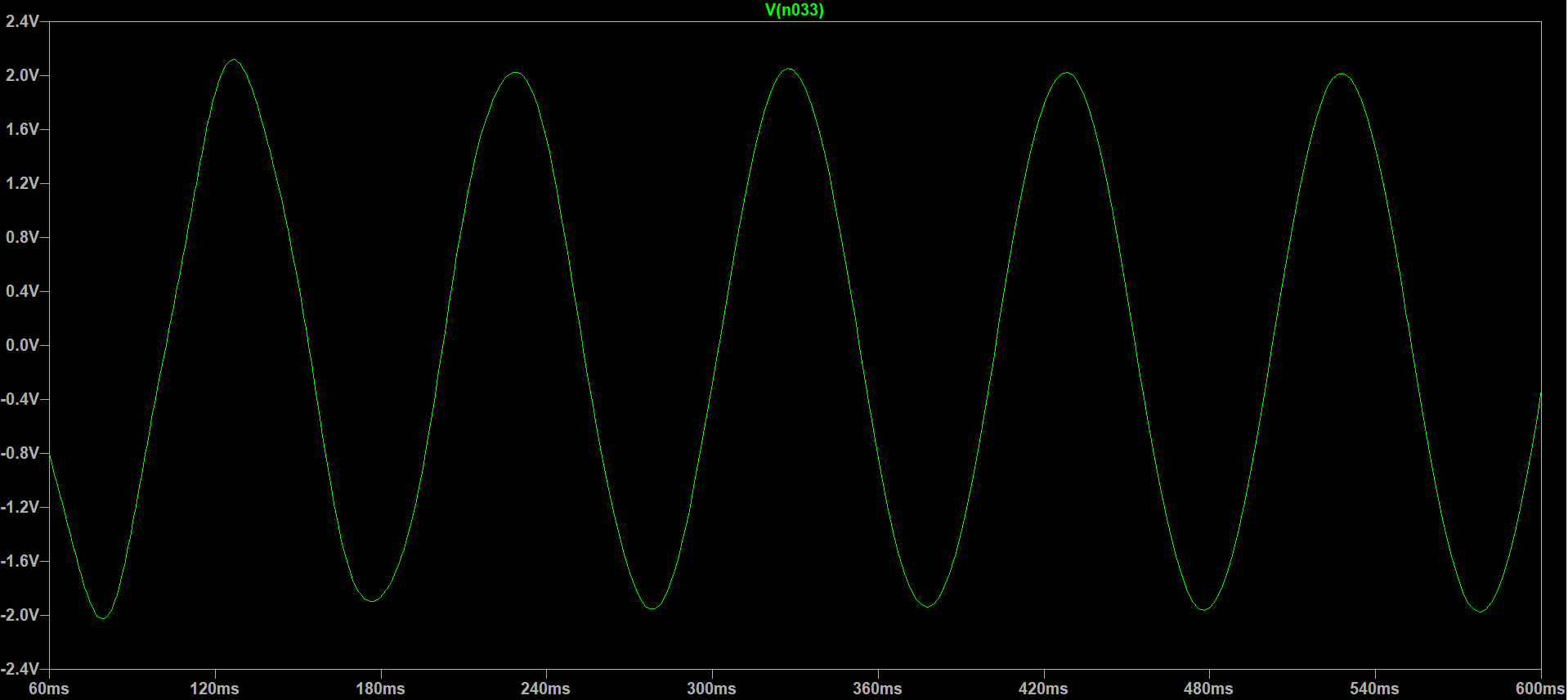
*Figure 17 : Bode plot of notch filter with a center frequency of 60Hz*

### Complete circuit for 1 channel

To test the complete circuit over one channel, Transient analysis was used with a stop time of 0.7 seconds. Such an analysis allows the visualisation of the non linear transition response of the circuit in the temporal domain, much like an oscilloscope would. The input signal is a sin wave with an amplitude of 50µV and a frequency of 10Hz. As seen in figure 19, the output signal has an amplitude of ≈2.05V, indicating a gain of ≈41000. It is important to note the slight offset, as the output sine wave is not centered around 0V. While testing the notch on a smaller specific PCB, PolyCortex observed the same offset in the output signal. The notch is therefore the likeliest cause of this offset.



*Figure 18 : LTspice schematic of complete circuit for one channel*



*Figure 19 : Output signal of complete circuit for one channel*

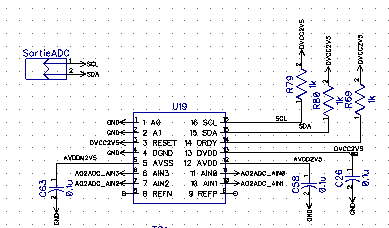
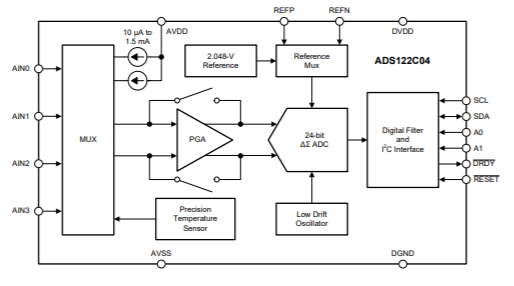
## Other Components

### Power supply

In previous version of the EEG acquisition circuit, the amp-ops were supplied with 5V and saturation was observed while gathering EEG data. Instead of decreasing the overall gain of the circuit, PolyCortex decided to increase the power supplying the circuit. The Vcc+ net of the circuit was thus set to 9V and the Vcc- to -9V since the board is powered with 9V batteries.

### ADC

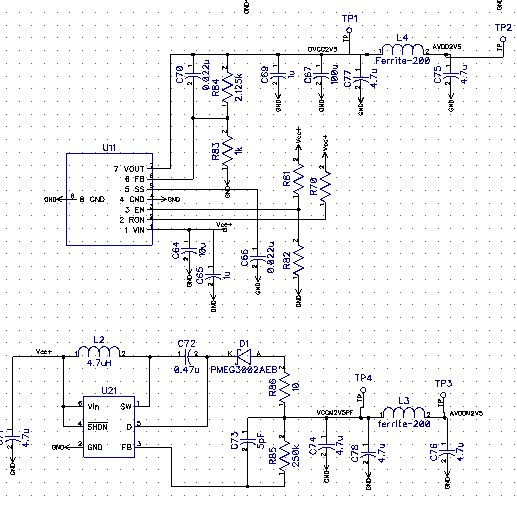
The PCB created to acquire the EEG waves is made to be wired to an interface to visualize the signals. To insure the communication between the circuit and the interface’s program, the voltage of the four channels must be converted from analog to digital. Texas Instruments’ 24-bit ADS122C04 was selected for its 4-channel input and its high sampling rate of 2kSPS. Furthermore, this ADC uses the Delta-sigma analog-to-digital converting method, which pushes the noise to higher frequencies in order to increase its resolution. This ADC also helps eliminate common-mode noise by providing a typical CMRR of 110dB for a frequency of 60Hz (with DR=2kSPS).

*Figure 20 : DipTrace schematic of the ADS122C04 ADC and functional diagram*

### DC-to-DC converters

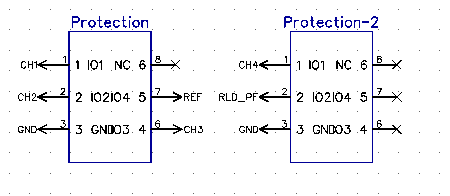
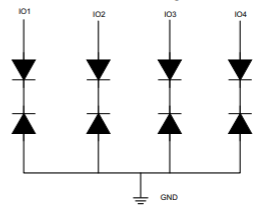
The ADC requires ±2.5V analog and digital supply to function. Therefore, a LT3483IS6 and a LMZ12002TZ DC-to-DC converter were added to the circuit in order to transform the 9V from the battery to ±2.5V while also regulating the voltage input of the ADC. The LT3483 is commonly used to produce analog negative voltage outputs, while the LMZ12002TZ is used to carry out analog and digital output. Both were chosen for their input range (2.5V to 16V for LT3483IS6 and 4.5V to 20V for LMZ12002TZ), which largely accommodate the 9V of the battery, and their voltage output (-2.5V to -38V for LT3483IS6 and 0.8V to 6V for LMZ12002TZ) suitable to power the ADC.



*Figure 21 : DipTrace schematic of DC-to-DC converter (top : LMZ12002TZ, bottom : LT3483IS6)*

### Protections

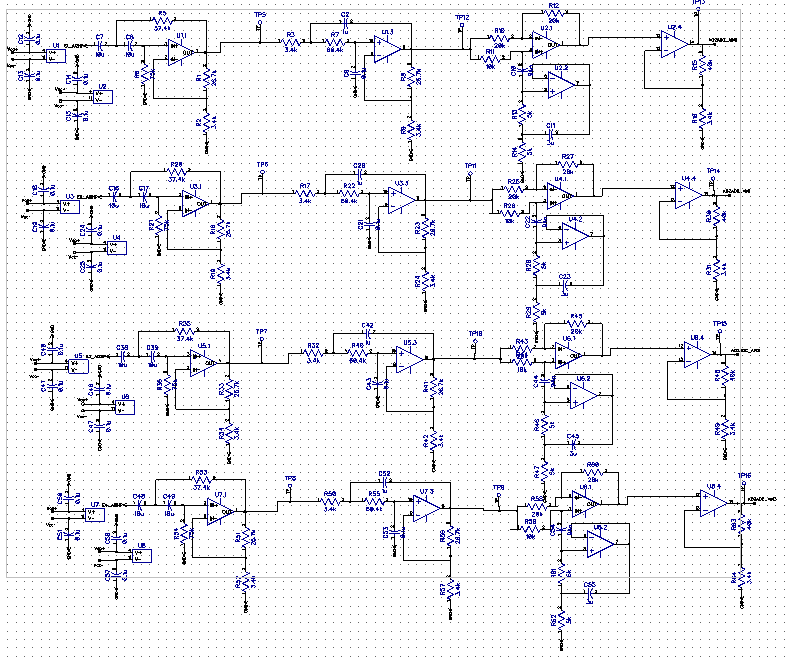
Since PolyCortex will be testing the board on a human subject to acquire their EEG signals, it was considered wise to add a circuit protection component between the electrodes and the beginning of the circuit. Texas Instruments’ TPD4E1B06DCKR 4-channel bi-directional Transient Voltage Suppressor (TVS) diode array was chosen for its low leakage current (0.5nA) which insure the precision of analog measurements. It offers protection for currents exceeding 3.0A (8/20µS).

*Figure 22 : DipTrace schematic of protection circuit TPD4E1B06DCKR and functional diagram*

## Schematic, layout and routing

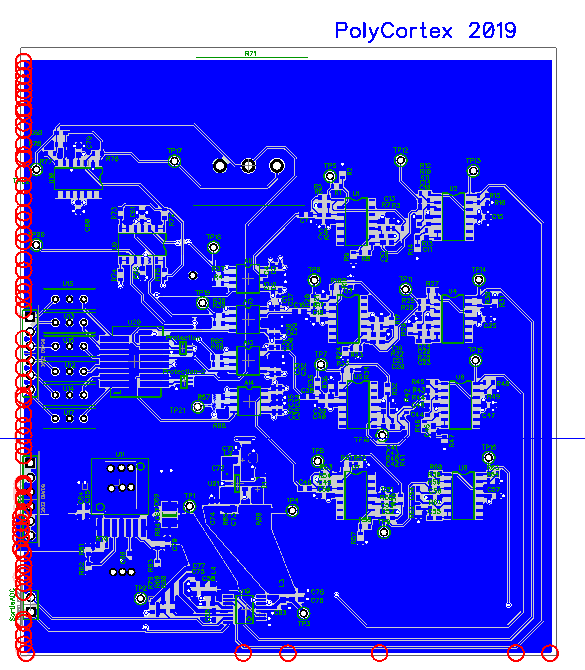
Before the PCB can be printed out, the circuit must be translated to a schematic. Then, the schematic is converted to a PCB layout, where the components must be placed and routed to one another. These steps were executed with the DipTrace software, which offers a schematic capture editor, a PCB layout editor, a component editor and a pattern editor module. The component and pattern editor tools are used to incorporate custom components that might not be included in DipTrace libraries.



*Figure 23 : DipTrace schematic for the 4-channel circuit*

The PCB PolyCortex created has 4 layers : the top one contains the pads on which the components are wielded and wires, the middle layers consists of the ground and power supply, and the bottom layer contains additional wiring. A copper plating was placed on top to surround the components and wires to further isolated them and reduce parasitic interference between the channels.

When doing the layout, PolyCortex took into consideration the size of the board, which could not exceed a self placed limit of 20cm by 20cm, and the proximity of the components. The components were placed as close to each other as possible to minimize signal quality degradation. Furthermore, the analog and digital components were separated to avoid interference. While routing the circuit, the 90° angles were carefully avoided to prevent current concentration. Long parallel wire line were also avoided to stop parasitic impedance from contaminating the signals.



*Figure 24 : DipTrace layout of the finished PCB*

The completed PCB was exported in *gerber* files and sent to Labo Circuits Inc. for printing.

## Testing

PolyCortex has not completed the testing phase of the prototype PCB. Due to the circuit’s complexity and the highly optimized layout, soldering the components onto the board was much longer and much harder then anticipated. Key components, such as the DC-to-DC converters and common mode chokes, required more advanced soldering techniques not previously explored by PolyCortex. Thus, the PCB will be completed over the summer of 2019, using hot air soldering and reflow ovens. Testing this prototype PCB is important to further the team’s comprehension of designing more complex circuits and understanding of the limitations of electronics. The prototype PCB includes many testing points (TP1 through TP22) which will help PolyCortex identify and rectify any discovered design issue. Proper testing of the PCB should allow our members to leverage its technology in a future NeuroTechX competition.

The filtering stages that were tested seemed to cause unwanted saturation of the amp-ops visible from the different testing points of the board. PolyCortex believes this observation is due to gains added to the filtering levels.

## Board cost

A list of the 207 components of the circuit is annexed to this document. The total cost of the components, which were ordered on Digi-Key Electronics, is 157,06 CAN$. The PCB was printed by Labo Circuits Inc. for a fixed cost of 225 CAN$ and 57,16$ per copy. The board cost can therefore be evaluated at 282,16 CAN$. The combined total cost of the board and the components is 439,21 CAN$ (329,67 US$).

## Encountered difficulties and limitations of the design

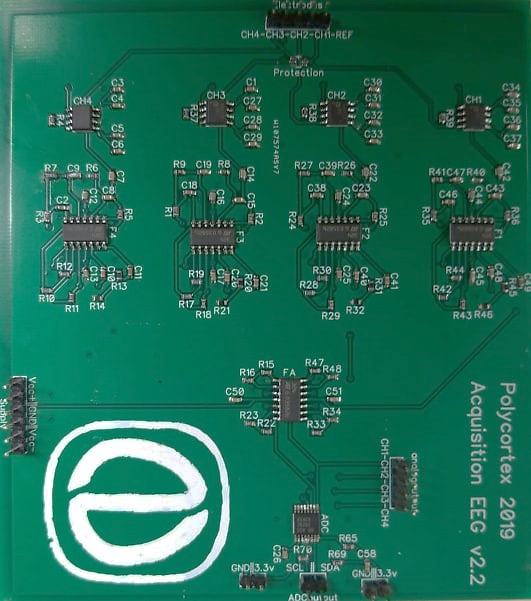
The most obvious limitation of the prototype PCB is that it has not yet been fully tested and isn’t ready to acquire EEG waves from a subject. Furthermore, the size of its components 0603 (metric) and the proximity of the pads on the layout make the board considerably hard to solder by hand. PolyCortex has encountered problems soldering components on pads too close to each other, as the melted tin would sometimes touch other pads and create shorts.

## Lessons learnt and future

The prototype PCB has a much greater complexity than any board previously attempted by PolyCortex. Although it is not yet fully functional, this ambitious PCB has a lot of potential and lessons to teach. First of all, the difficulties soldering the PCB brought PolyCortex to reconsider using 0603 components for future boards. A bigger size of 1206 (metric) will most definitely be used in future designs, since there are no particular restrictions on the overall size and weight of the PCB. Using components easier to solder would also simplify the reproducibility of the board and minimize soldering errors. Since PolyCortex is a team that values inclusion and teaching of new skills, easier soldering would allow more members to participate in assembling the PCB. Additionally, a special attention will be paid to the distance between the pads when laying out the components. Further conclusions will arise from testing the board. PolyCortex is looking to determine the effect of components like RF filters and common mode chokes on the quality of the signal and the artefact removal. Moreover, the 24-bit ADC used on this PCB is more powerful and better suitable for EEG application than the ADC used on previous cards and will likely help PolyCortex acquire more precise data in future versions of the PCB.

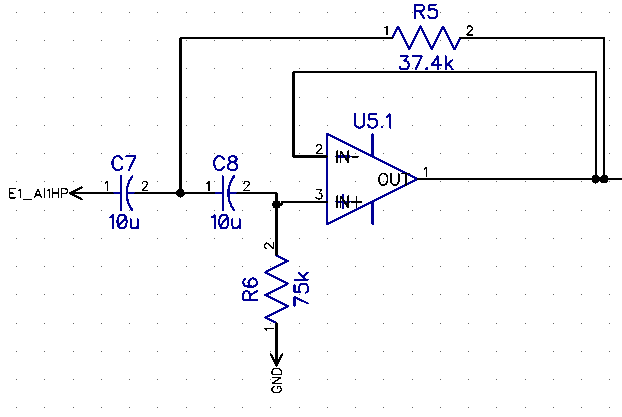
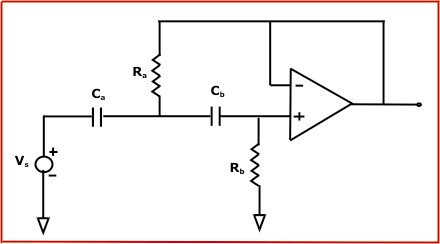
# Circuit design – Secondary PCB, version 2.2 – Fixed Challenge 2019

## Circuit Overview

The circuit presented previously is considerably more complex than the minimum required to acquire EEG waves. Therefore, PolyCortex chose to develop a secondary PCB to account for the potential mistakes in the prototype PCB and ensure the delivery of a functional board. This secondary PCB contains the strict minimum to filter, amplify and convert the signals from analog to digital, while still insuring the safety of the subject to which the electrodes are connected. The circuit separates the analog and the digital portion, which are respectively powered by 9V batteries and by an Arduino microcontroller (3.3V). The analog portion includes 4 channels composed of an instrumentation amplifier, three stages of filtering and a final amplification stage. The digital portion includes the ADC component to insure the transfer of the data onto the interface. Furthermore, the board has two separate outputs for digital and analog data.

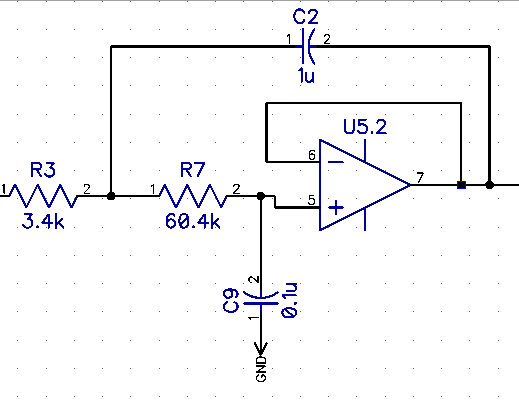
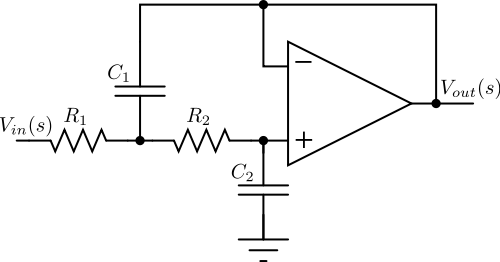
## Filtering

### High pass filter

During preliminary testing of the prototype card, the PolyCortex team noticed unexpected saturation behavior between the different filtering stage. It was thus decided to remove the resistors responsible for the gain of the filters (see figure 10 and 11), as they can modify the frequency response and can degrade the signal if the gain is too high. The high pass filter used for this circuit is the same Butterworth 2nd order configuration, but it doesn’t provide any amplification gain to the signal. The cutoff frequency *f* of such a filter is determined by the value of Ra and the value of Ca following the equation : , with Ra= 2 \* Rb and Ca= Cb. PolyCortex has chosen Ra = 75kΩ, Rb =37.4kΩ and Ca = Cb = 10µF, thus providing a cutoff frequency of 0.3Hz.

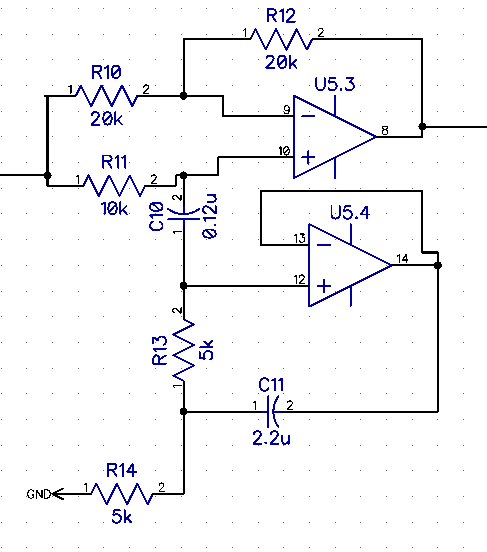
*Figure 25 :* Secondary *PCB high pass filter configuration (left : DipTrace schematic, right: theorical configuration)*

### Low pass filter

 Similarly as with the high pass filter, the resistors responsible for the gain of the lowpass filter were removed from the configuration. The cutoff frequency of this filter is given by the following equation: , referring to the right-side image of figure 26. In PolyCortex’s schematics (left-side of figure 3), these values have been set to R1 = 3.4Ωk, R2=60.4Ωk, C1= 0.1µF and C2= 1µF. Therefore, the cutoff frequency is 35Hz.

*Figure 26 : Secondary PCB low pass filter configuration (left : DipTrace schematic, right: theorical configuration)*

### Notch

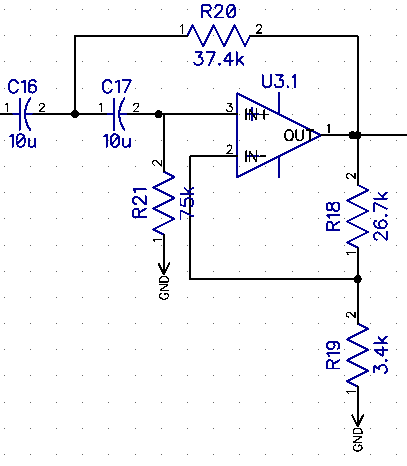
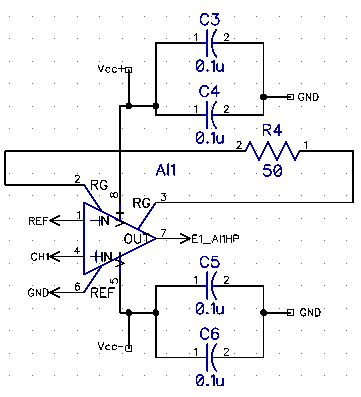
The notch used for this circuit is the same as the one designed for the prototype PCB (see figure 4), and therefore also has a narrow bandwidth cutting the 60Hz frequency. For this specific configuration, the cutoff frequency is given by the equation : , with and (referring to the right-side of figure 4). To obtain a cutoff frequency centered around 60Hz with a gain of at least -30dB to eliminate the mains hum, PolyCortex chose values of R1 = R2 = 5Ωk, R3 = 10Ωk, R4 = R5 = 20Ωk, C1 = 0.12µF and C2 = 2.2µF.

*Figure 27 : Secondary PCB notch filter configuration (left : DipTrace schematic, right: theorical configuration)*

## Amplification

Since the resistors providing a gain on each filtering stages were removed, the amplification provided by the instrumentation amplifier and the last amplification stage needed to be increased. Like the prototype PCB, the operational amplifiers used are Texas Instruments’ LM324 (see Operational amplifier section of prototype PCB and figure 8). Furthermore, the instrumentation amplifiers used for this circuit are also the AD8422 (see figure 9).

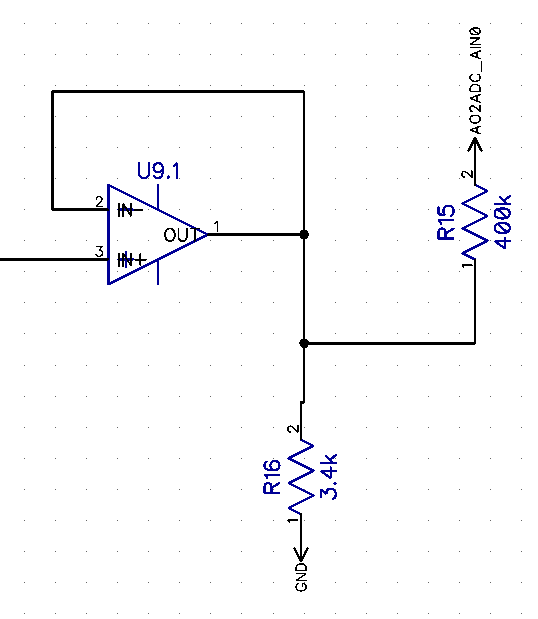
### Instrumentation amplifier

The instrumentation amplifier configuration used in the secondary card differs from the prototype circuit regarding the resistor used and the gain produced. The gain, which is given by Gain = 1 + 19.8kΩ/RG, was increased by using a single 50Ω RG resistor instead of two 250Ω resistors. Thus, the instrumentation amplifier is responsible for a gain of about 398. The bypass capacitors used in the prototype PCB were kept to regulate the supply voltage of the instrumentation amplifier.

*Figure 28 : DipTrace Schematic for secondary card and connection diagram of the instrumentation amplifier AD8422*

### Circuit amplification

Similarly to the prototype PCB, this circuit contains a final amplification stage located after the filters. It provides a gain because of its non-inverter op-amp configuration. For this configuration, the gain is once more proportional to the ratio of the chosen resistors (Gain = 1 + Rf/Ri) R15 and R16 on figure 29. To increase the gain compared to the prototype PCB, PolyCortex chose to use R15=400kΩ and R16=3.4kΩ, therefore providing a gain of ≈119.



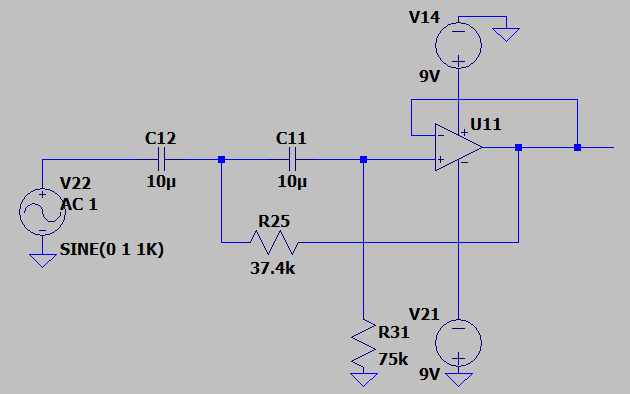
*Figure 29 : Diptrace schematic of non-inverter final amplification stage of secondary PCB*

The total gain of the circuit is therefore ≈47 362 (398 \* 119).

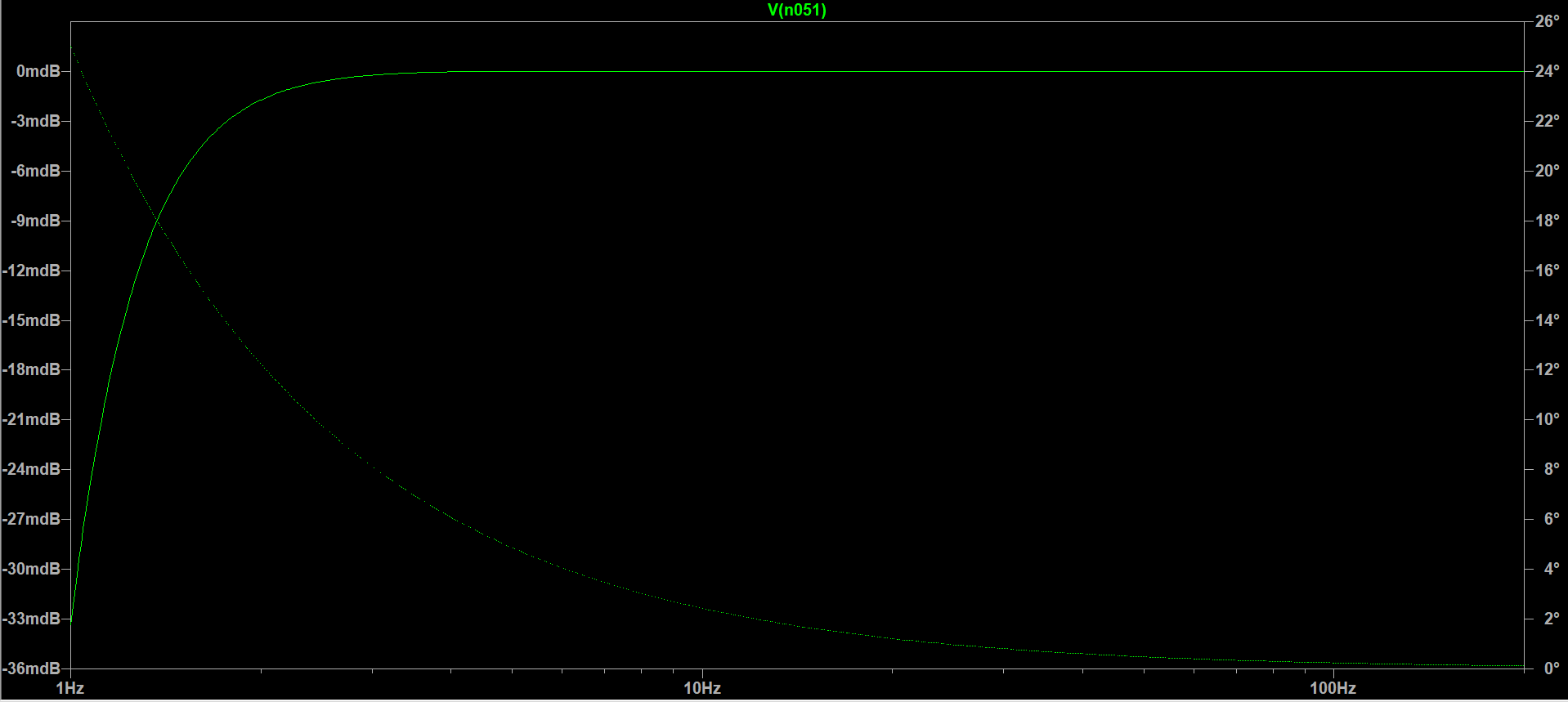
## Simulation

Using the LTspice software, the filters were individually simulated using the same method as the prototype PCB and a Bode plot was produced to verify the cutoff frequencies.

### High Pass Filter

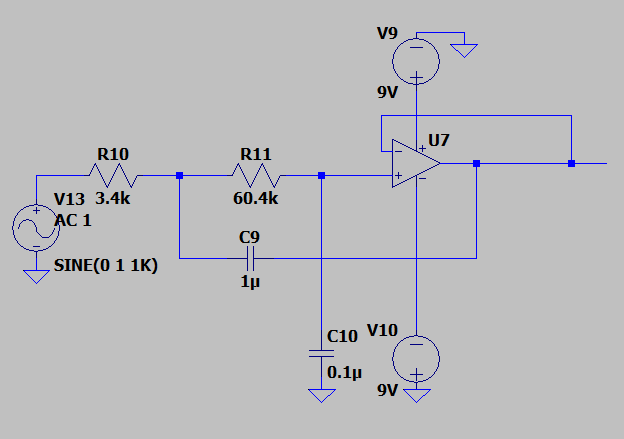


*Figure 31 : LTspice schematic of high pass filter for the secondary PCB*

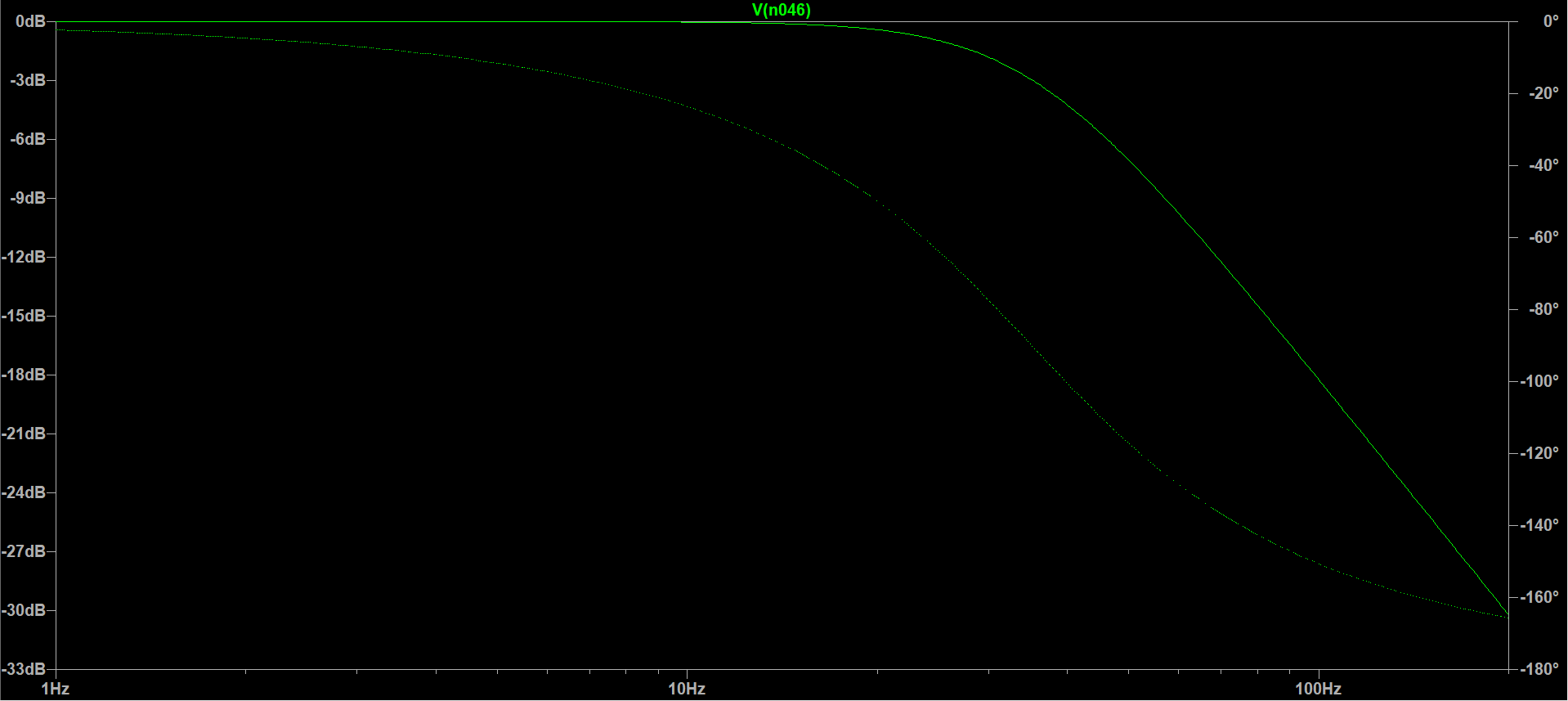


*Figure 32 : Bode plot of high pass filter with cutoff frequency of 0.3Hz for the secondary PCB*

### Low Pass Filter

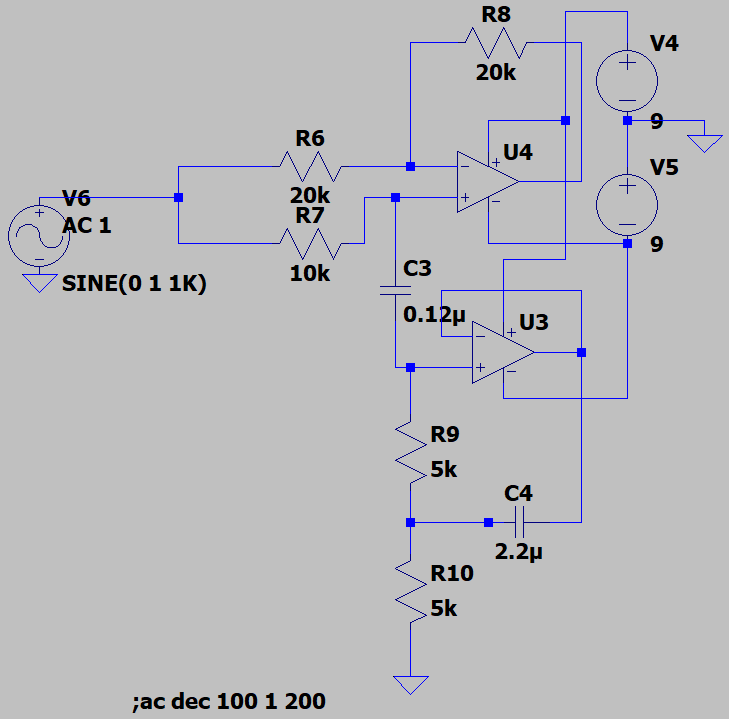


*Figure 33 : LTspice schematic of low pass filter for the secondary PCB*

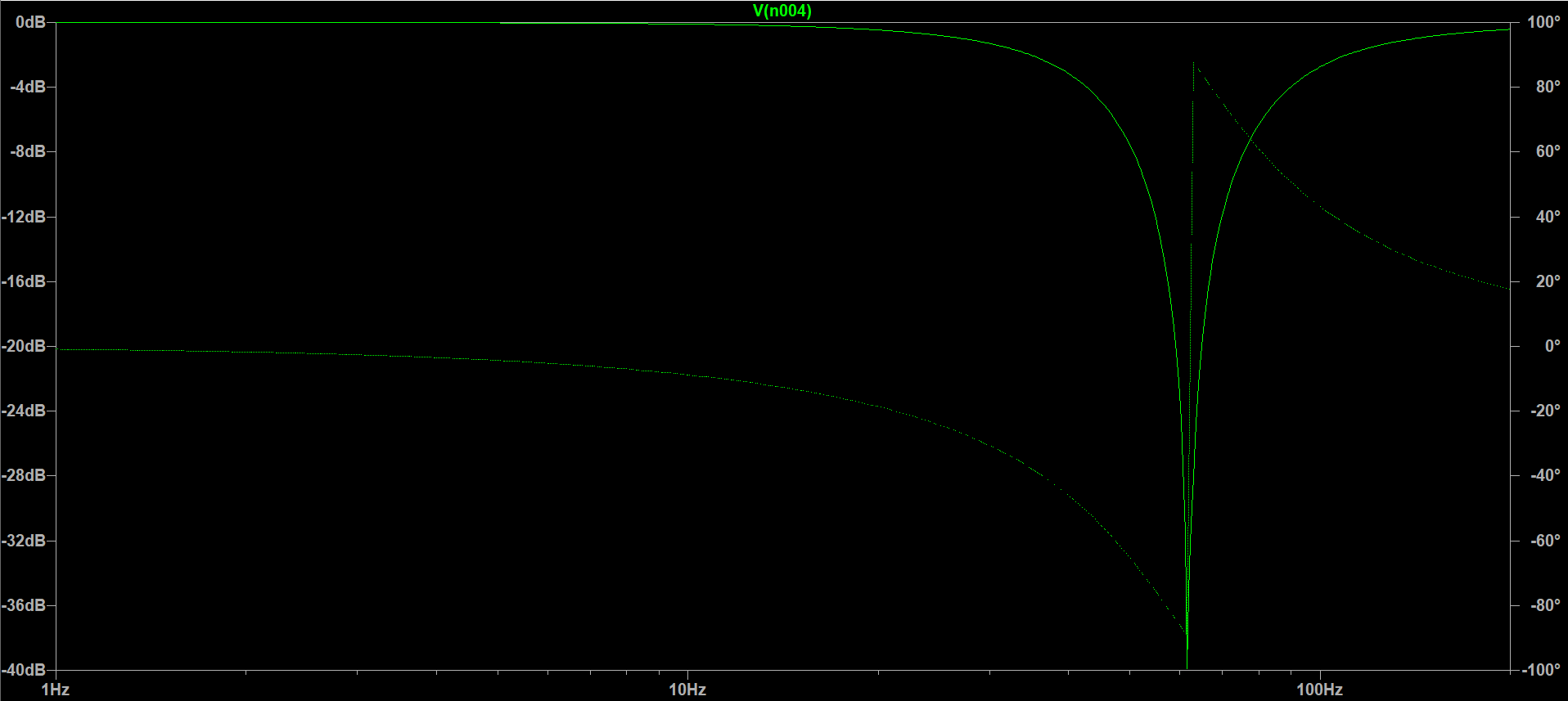


*Figure 34 : Bode plot of low pass filter with cutoff frequency of 35Hz for the secondary PCB*

### Notch



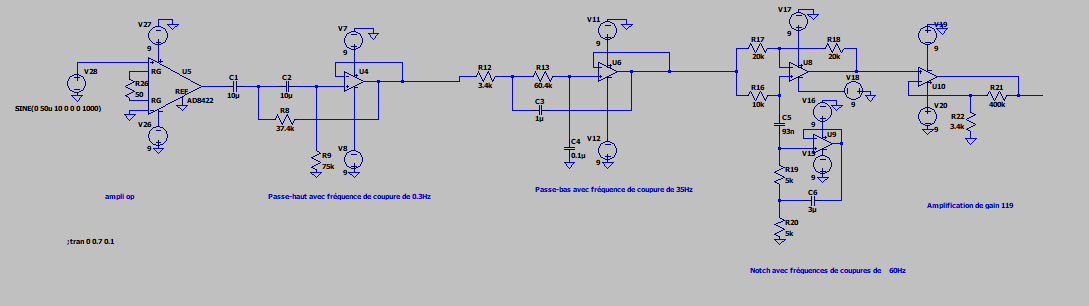
*Figure 35 : LTspice schematic of notch filter for the secondary PCB*



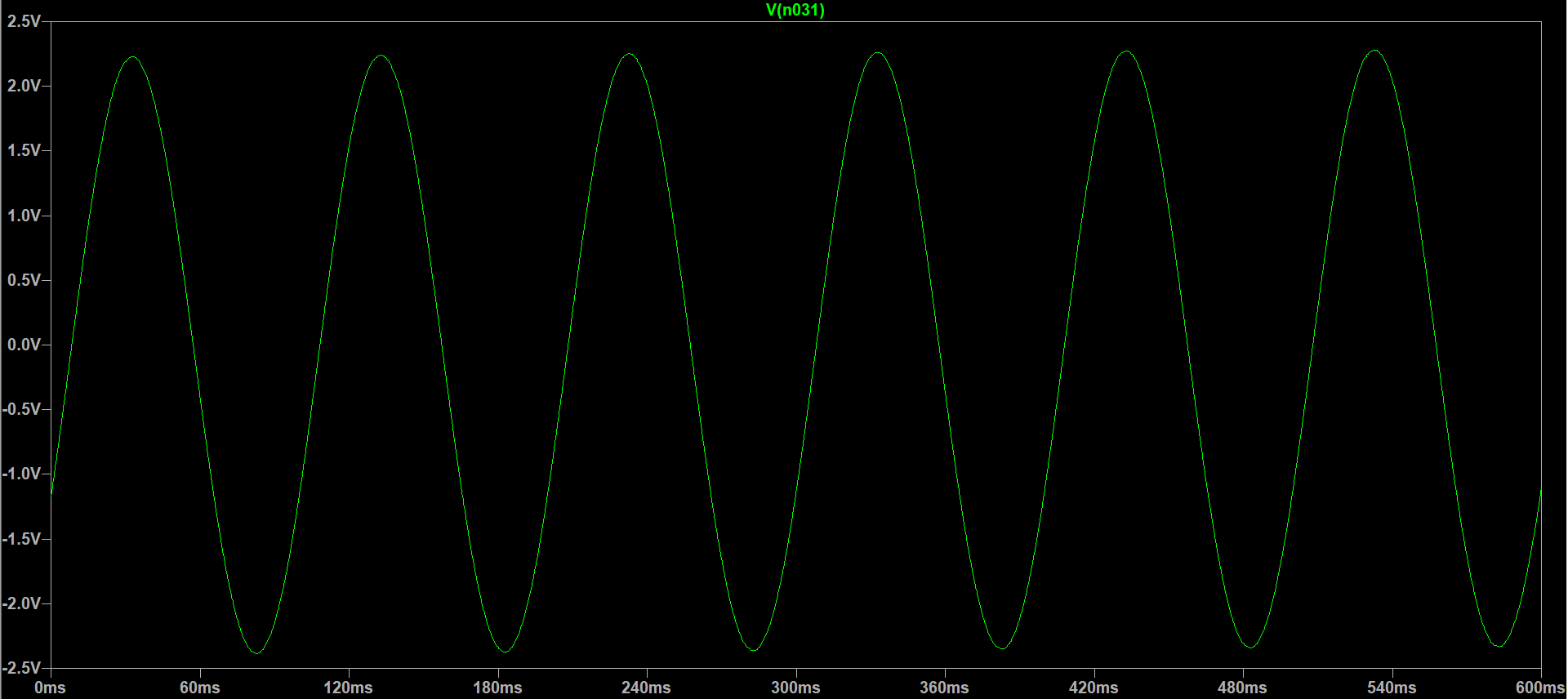
*Figure 36 : Bode plot of notch filter for the secondary PCB*

### Complete channel

The circuit for a complete EEG acquisition channel was simulated with an input sinusoidal source with an amplitude of 100µV peak-to-peak. The output signal is roughly 4.6V peak-to-peak, indicating a over gain of ≈46 000, which is coherent with the theorical gain of 47 362. The different between the theory and the simulation lies in the tolerance of the resistors. A slight offset is visible on the output signal, as it is not completely centered around 0V like it was originally, which is most likely due to the notch filter used.



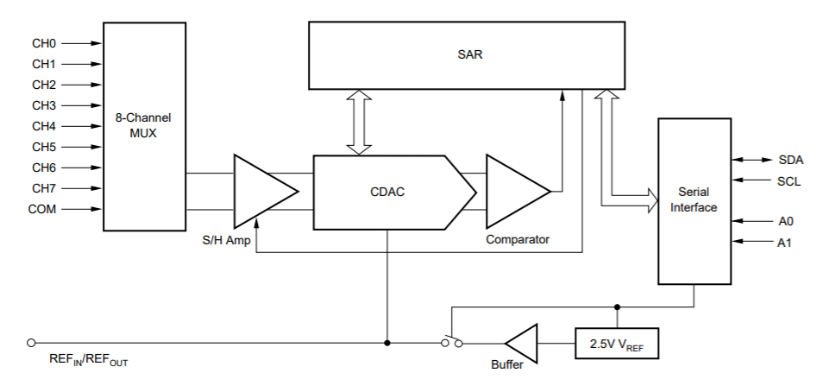
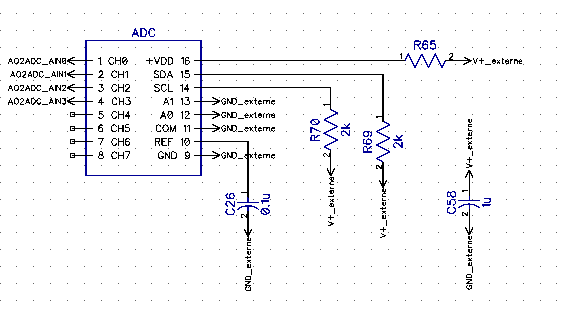
*Figure 37 : LTspice schematic of complete channel circuit for secondary PCB*



*Figure 38 : Output signal of complete circuit of 1 channel for secondary PCB*

## Other components

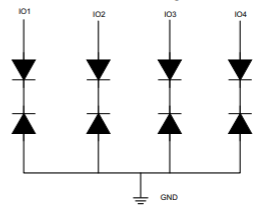
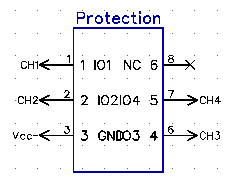
### ADC

PolyCortex chose to resort to an ADC model that had been tested by the team with the printing of a PCB containing only the ADC and its corresponding circuit. Thus, instead of using the Delta-Sigma ADS112C04 of the prototype PCB, the secondary PCB uses Texas Instruments’ ADS7828. This ADC is slightly less performant, as it uses a sampling method over 12-bit instead of the Delta-Sigma converting process over 24-bit of the ADS112C04. The ADS7828 has a built in asynchronous clock, an 8-channel multiplexer (MUX) and a sample-and-hold amplifier. It supports the I2C interface and can be set to standard, fast and high-speed modes. In order to communicate with the interface PolyCortex has created to visualise the EEG signal, the ADC’s output is connected to an Arduino microcontroller. The Arduino also supplies the ADC with 3.3V, as the ADS7828 has an input range of 2.3V to 5V.

*Figure 39 : DipTrace schematic of the ADS122C04 ADC and functional diagram*

### Protection

To prevent the subject from being electrocuted by leakage electricity, the secondary card also uses Texas Instruments’ TPD4E1B06DCKR 4-channel bi-directional Transient Voltage Suppressor (TVS) diode array. It has a low leakage current (0.5nA), which insure the precision of analog measurements and it offers protection for currents exceeding 3.0A (8/20µS).



*Figure 40 : DipTrace schematic of protection circuit TPD4E1B06DCKR and functional diagram*

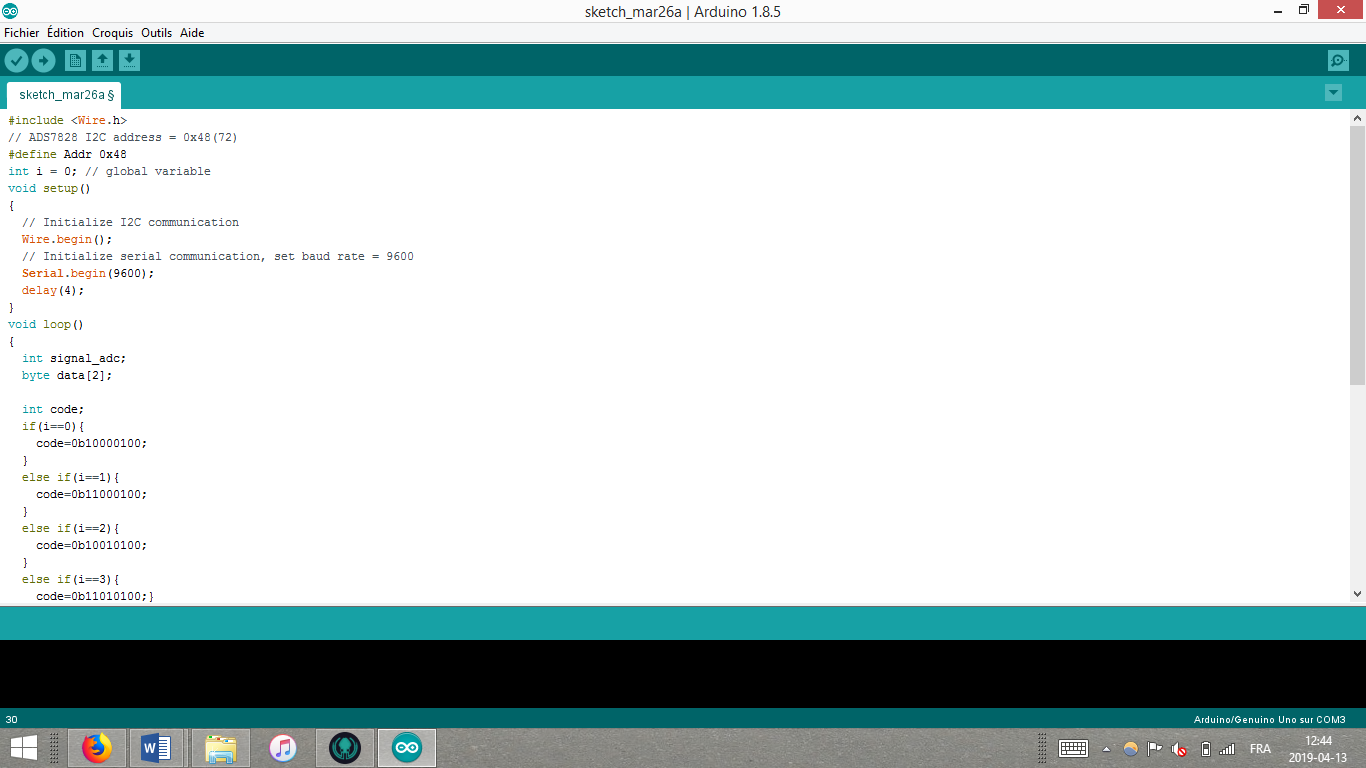
#### ADC – Arduino I2C communication

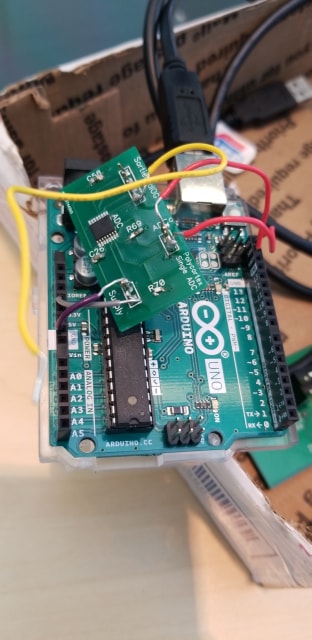
An Arduino Uno board is used by PolyCortex’s team to control the MUX of the ADC. The user-friendly I2C protocol was privileged and could provide sufficient communication speeds for a 2 kHz sampling rate (enough for EEG acquisition). Hence, a looped sequence was programmed on the Arduino to switch the MUX and read the incoming 8-bit data, that was transformed in a 12-bit integer. It was then sent directly through the serial port to the software team’s Python interface for real-time display. Simplicity was the primary aim in this part of the pipeline, in order to ensure that data would get from the acquisition board to the computer as efficiently as possible.

A copy of the C++ code which we uploaded onto the Arduino board for data transfer is based on an open-source code from the *ControlEverythingCommunity*, accessible via their GitHub repository:

<https://github.com/ControlEverythingCommunity/ADS7828>

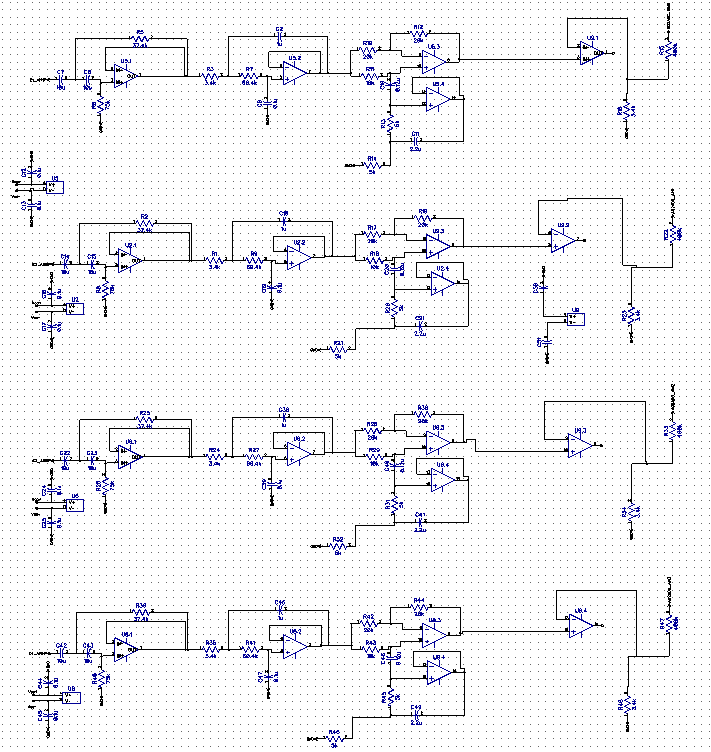
(Continued)



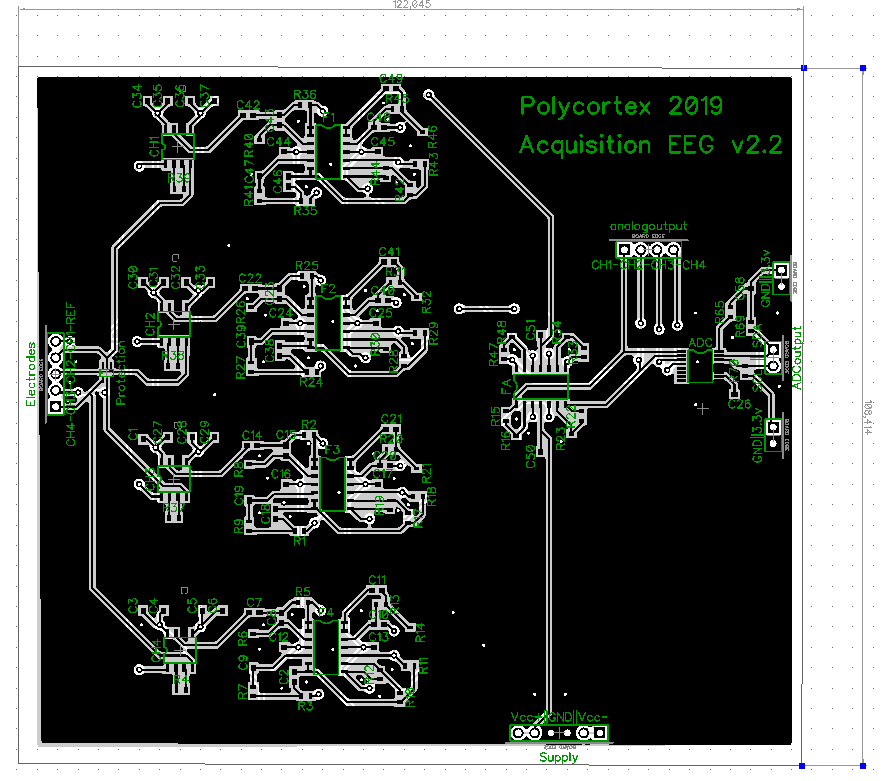


## Schematic, Layout and Routing

As with the prototype PCB, the PCB for the secondary circuit was routed in Diptrace. However, PolyCortex noticed the components on the prototype PCB were very close to each other, making the board hard to weld. Thus, the components on the secondary board were placed further apart while still respecting the maximum dimensions of 20cm by 20cm. The PCB itself, due to its simpler nature, was laid out and printed on only two layers (the prototype PCB has four). The components lie on the top layer, which is linked to the bottom layer through static vias. Both top and bottom layers are covered by an extra coating of copper to provide the circuit’s ground, isolate the components and reduce interference between the channels. The input and output pin locations were placed on the edges of the board as much as possible to facilitate access while still reducing route lengths.



*Figure 41 : Diptrace schematic of complete 4 channels*



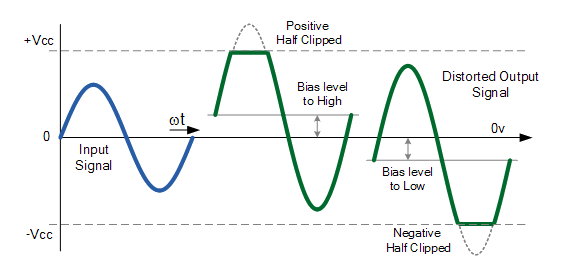
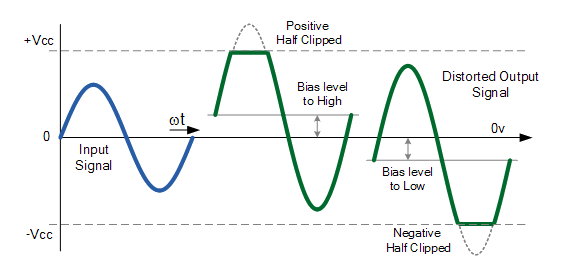
*Figure 42 : Diptrace layout and routing for secondary PCB*

The PCB was printed with PCBway, reducing the cost, and to an extent, the quality when compared to printing with Labo Circuit. PolyCortex also ordered the stencil used to weld the components onto the PCB with a soldering reflow oven.

## Testing

The board was tested over one channel at a time with a sinusoidal signal from a waveform generator at minimal tension (50mV) wired to a tension divider to produce a signal of 20µV. While testing the card, the leakage currents were closely monitored by the team and never exceeded 0.10A. The output signal was observed with an oscilloscope wired to the ‘analog output’ pin corresponding to the channel being tested. It was quickly observed that the labels CH-1 to CH-4 were not written in the correct order and should have been mirrored, as the channel on the far left of the PCB is CH-4 and the one on the far right is CH-1 (see figure 42). Despite the labelling mistake, the output signals were indeed reaching the analog output pins and were visible on the oscilloscope.

The signals were not exactly sinusoidal when displayed on the oscilloscope, but rather a portion of the lower end of the sinus was clipped (see figure 43). This kind of behavior usually indicates saturation. However, the amplitude of the signal received on the oscilloscope was about 2.25V peak-to-peak, which should not have saturated the am-op powered by 9V batteries. To further investigate, an AC voltage offset was applied to the signal to verify if the negative portion of the sinus would appear. This maneuver was effective for a short period of time, after which the signal would return to its cropped shape. Since the ADC is powered with 0 to 3.3V, the idea of this component saturating was brought up, but quickly ruled out because the signal was being observed from the analog output pins. PolyCortex then concluded that the likeliest cause of this behavior is an incorrect biasing (Q-point) level preventing the amp-ops from amplifying the signals over a whole cycle.



*Figure 43 : Amplifier distortion due to incorrect bias*

The filters were tested by increasing the frequency from the waveform generator and observing the analog output. As expected, the frequency of the output rose according to the input and the amplitude of the output started to decrease after 35Hz. Although greatly attenuated by the notch, the main hum noise of 60Hz was still present. This was expected as the used notch filter’s cutting bandwidth is very sensible to the tolerance of the resistors composing it.

The digital output and the ADC were then tested with the Arduino connected to a computer as previously described in the ‘ADC – Arduino I2C Communication’ section. The output signal observed were similar to the ones from the analog output displayed on the oscilloscope, thus validating the ADC’s proper functioning.

After these testing procedures, a subject was connected to the board via electrodes. Five electrodes were used to occupy the four channels and the reference pin. The signals were sent from the Arduino to the visualization interface designed by the software team. A numeric filter was placed on the 60Hz to attenuate the remaining noise. EEG signals from the four channels were observed on the interface with very little interference between the channels. PolyCortex’s team therefore deemed the PCB a success. Data was recorded for cycles of 2 minutes during which the subject had their eyes open and then closed in order to analyse the 3D spectrograms.

## Encountered difficulties and limitations of the design

Following the difficulties encountered welding the prototype PCB, PolyCortex decided to use a reflow oven to complete this board. This decision saved a lot of time and prevented soldering mistakes that could have affected the PCB if it was assembled by hand. The first limitation of the v2.2 board is the lower clipping of the signal, which is responsible for the loss of EEG information. Furthermore, while moving the electrodes onto the subject’s arms and chest, the interface displayed clear ECG signal at a frequency of about 0.015Hz. This might indicate that the lowpass filter isn’t powerful enough to attenuate all ECG signals. Interference between the four channels is still slightly present, though at a much lesser degree than with PCBs designed in the past. Notch filtering as proved itself hard to perfectly implement, as it does not fully attenuate the main hum and additional numerical filtering was required.

## Lessons learnt and future

Version 2.2 of the EEG acquisition circuit taught PolyCortex that soldering with a reflow oven provides much cleaner and faster results than soldering the components by hand. The society may consider purchasing its own oven for future PCB assemblies. PolyCortex still intends to continue developing the soldering skills of its members. It would be informative to compare the performances of two identical PCBs that have been soldered with a reflow oven and by hand. Another lesson learned regarding the board concerns filtering. The main hum noise is challenging to eliminate and can re-enter the signal at any point in the filtering stages due to devices like computers and the Arduino microcontroller. Numerical filters are therefore essential to complete artefact removal. It is likely that the board itself could also filter the main hum more effectively with the use of RF filters and common mode chokes. These options are currently being explored in the v.3 prototype PCB. The notch filter could be improved by using a larger bandwidth with a stronger attenuation power to ensure the 60Hz is successfully eliminated despite the errors due to component tolerance. Lastly, in future PolyCortex will strive to prevent signal clipping and all amplifier distortions.

## Board Cost

A list of the 138 components of the circuit is annexed to this document. The total cost of the components ordered on Digi-Key Electronics is 102,87 CAN$. Five copies of the PCB were printed by PCBways for a fix cost of 141 CAN$. The board cost can therefore be evaluated to 282,16 CAN$. The total cost of the board with the component is 243,87 CAN$ (183,10 US$). The secondary board is much cheaper than the prototype due to the simplicity of its circuit and the lesser quality of the printed PCB.

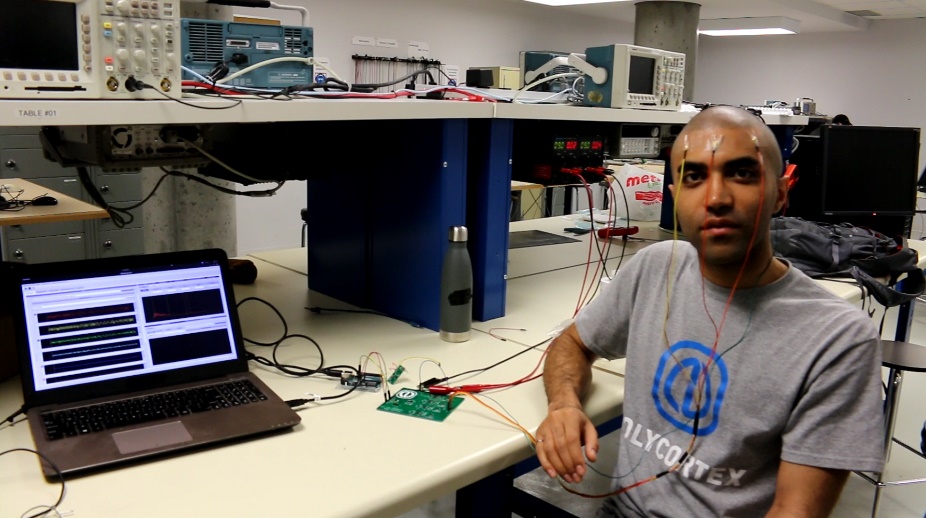
# Software design – Fixed Challenge 2019

## Overview of the Software

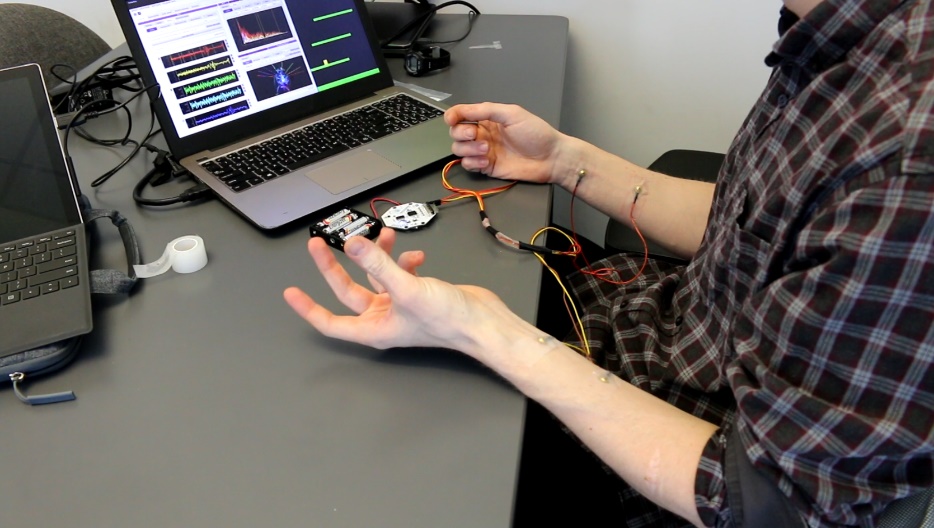
The real-time EEG visualization software was completely redesigned as part of our Fixed Challenge submission. The software is python-based, object-oriented, fully open-source and was originally implemented in Linux and developed using EEG signals input from an OpenBCI cyton acquisition board ([Cyton Biosensing Board](https://shop.openbci.com/products/cyton-biosensing-board-8-channel?variant=38958638542)). Having been developed with input from the cyton board, the software is currently designed to accommodate up to 8 channels.

## Data Transmission

With our own PCB, data is received from the connection to an Arduino Uno R3 microcontroller. With the cyton board, data is received directly from board. With the addition of an OpenBCI WiFiShield to the cyton board, data can be transmitted to the software wirelessly. Using the competition PCB, the sampling frequency is limited by the capabilities of the ADC which has a specified 6250 Hz sampling rate. Using OpenBCI hardware, sampling is limited by the WiFiShield and should have the ability to reach over 2000 Hz with a high speed network switch, with a theoretical limit of 16000 Hz according to OpenBCI.



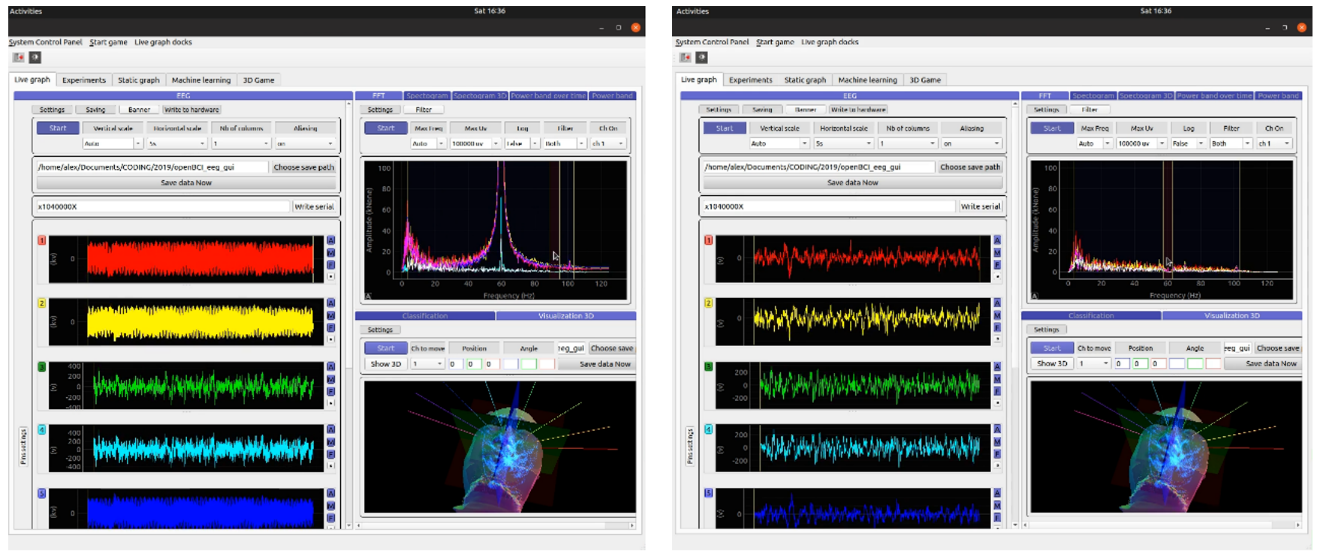
*Figure 44 : Software with EEG data transmission from the secondary PCB*



*Figure 45 : Software with EMG data transmission from the OpenBCI cyton biosensing board*

## Digital Signal Processing

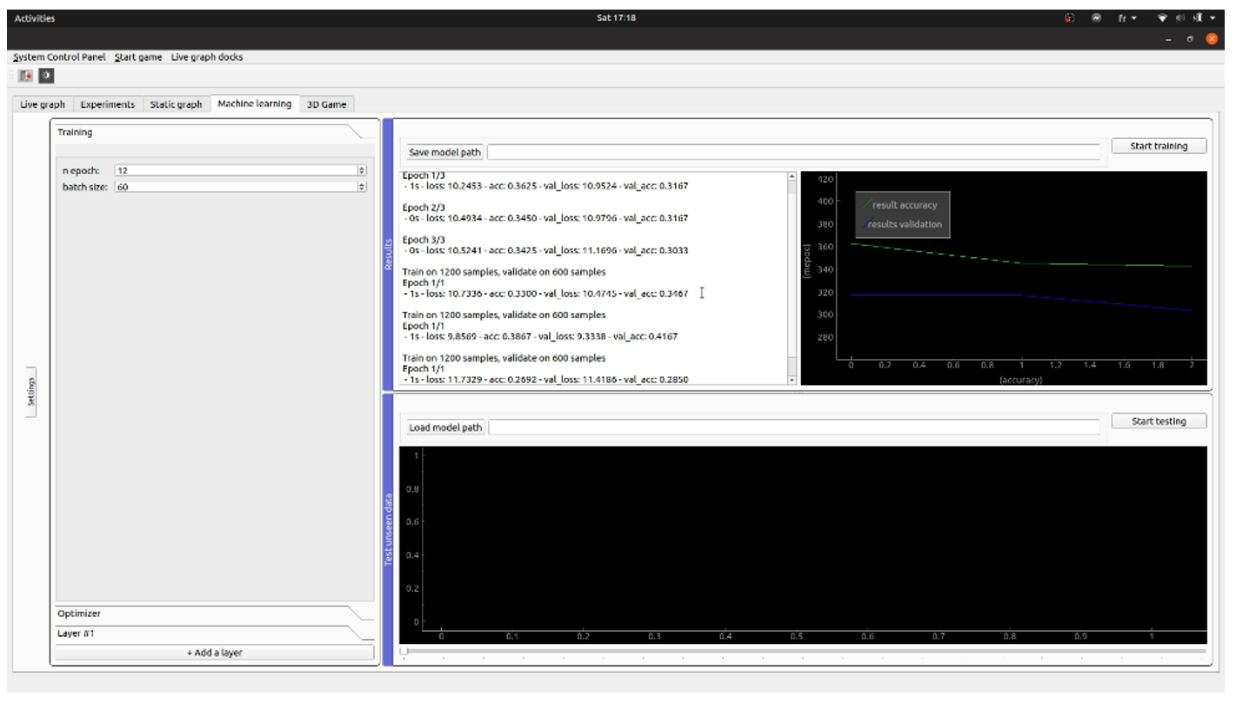
The software provides signal processing redundancy in the form of dynamic adjustable bandpass and bandstop filtering. High pass filtering from the bandpass filter stabilizes the signal so that there would not be large, slow voltage shifts over time. The bandstop filtering effectively helps eliminate any main power line interference that has evaded analog processing.



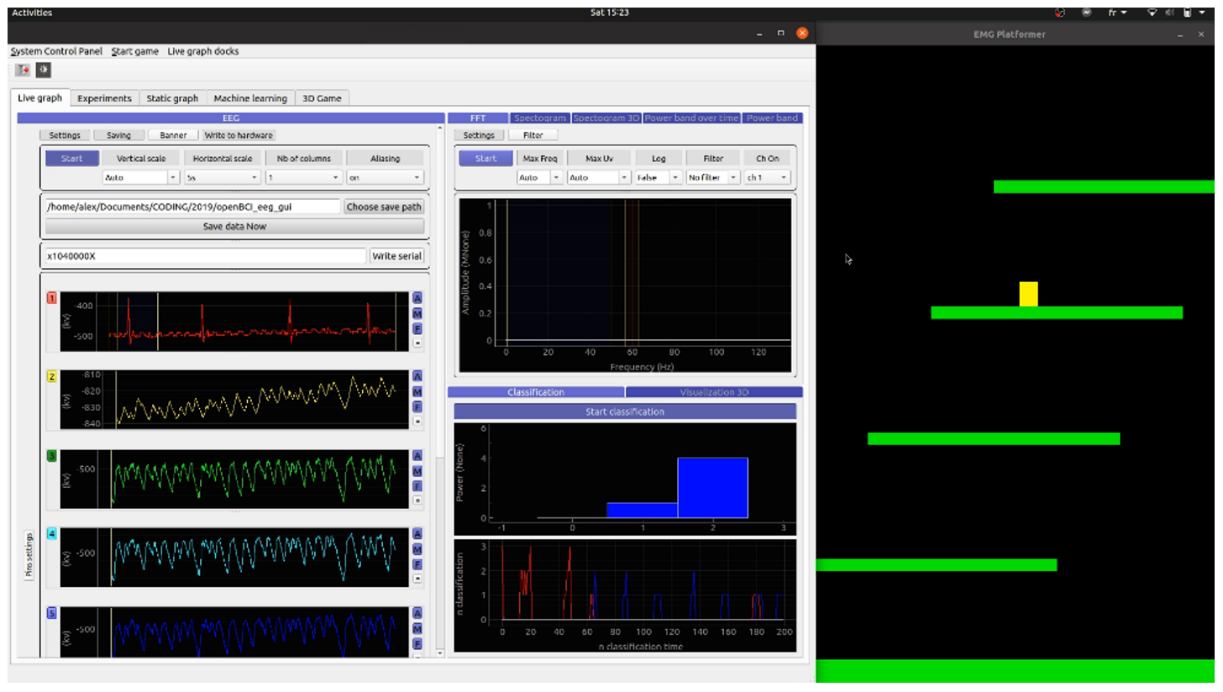
*Figure 46 : Dynamic adjustable bandstop filter, before (left) and after (right) application to mains hum*

## Artificial Intelligence

Owing to recent development in the field of machine learning and the many signal processing opportunities that are derived from it, the software is equipped with a convolutional neural network training module. The module was tested with EMG recorded using the cyton board, and EMG detection capability can be demonstrated through a featured signal classification-based game.



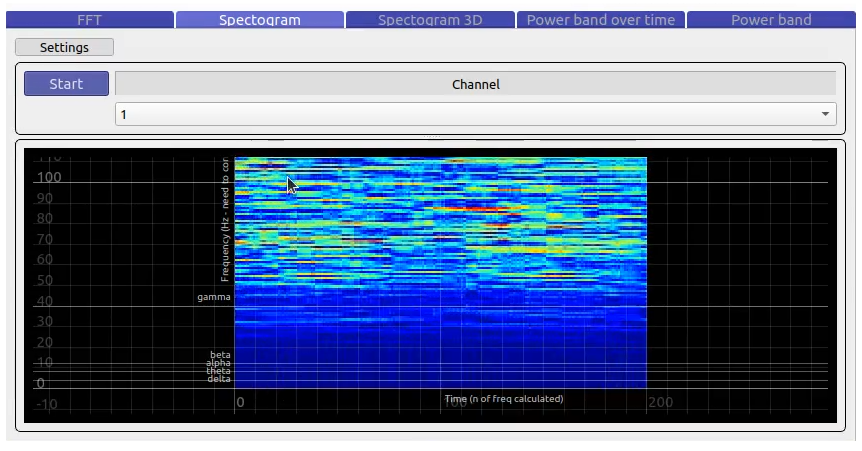
*Figure 47 : Acquisition software machine learning trainer interface*

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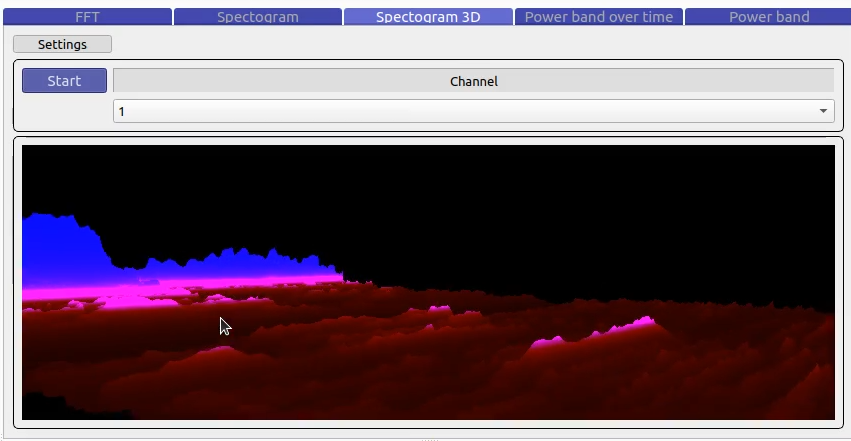
*Figure 48 : Featured machine learning EMG* *signal classification-based game*

## Real-time visualization

The software offers a variety of informative and pleasing visualisation options. Of course, time and frequency domains for each channel are on display. Also included are a graph of the evolution of individual averaged frequency bands over time. The software also features a 3D scalp time domain EEG visualizer, and 2D and 3D spectrograms facilitating characterization of the eye closure paradigm. While the frequency domain displays, alpha band changes over time and spectrograms allow characterization of the eye closure paradigm, the software also theoretically has the capability to be trained to recognize it.



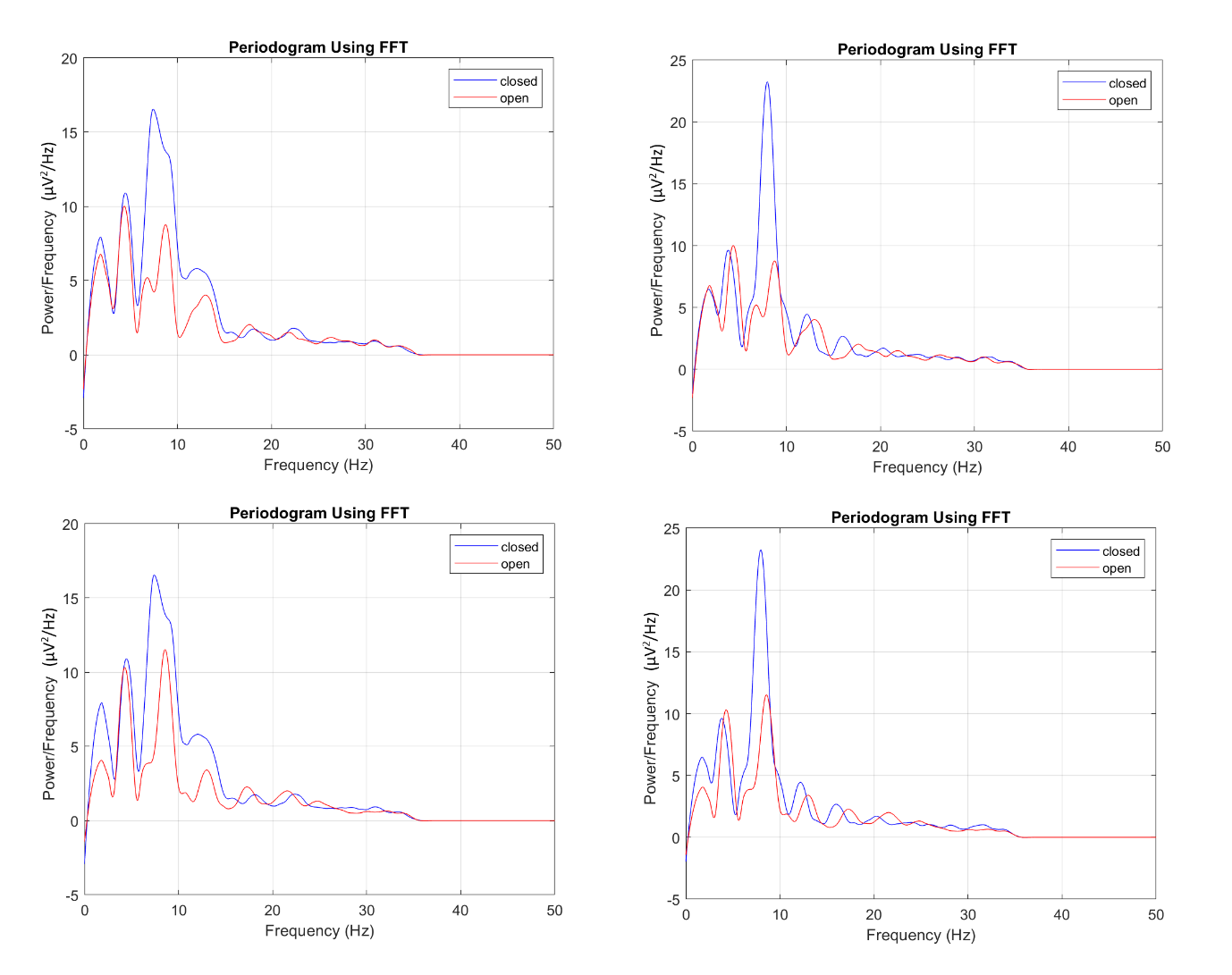
*Figure 49 : Acquisition software interface live spectrogram*



*Figure 50 : Acquisition software interface live 3D spectrogram*

## Data storage format

The timeseries data can be exported as a .csv file for subsequent static analysis. A conversion factor which depends on the hardware used is applied to the signal data to recover initial pre-processed signal voltage values. For use with the cyton board, the following equation can be used:

******

*Figure 51 : Eye closure test results with the cyton board*

# Annexes

## Table 1 : List of components of the prototype PCB

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Component** | **Value** | **Pattern** | **Quantity** | **$/u** | **Total $** |
| ADC | - | ADS122C04 | 1 | 9,93 | 9,93 |
| Capacitor | 0.1u | CAP\_0603 | 43 | 0,0558 | 2,3994 |
| Capacitor | 1u | CAP\_0603 | 6 | 0,15 | 0,9 |
| Capacitor | 10u | CAP\_0603 | 9 | 0,21 | 1,89 |
| Capacitor | 0.12u | CAP\_0603 | 4 | 0,33 | 1,32 |
| Capacitor | 2.2u | CAP\_0603 | 4 | 0,154 | 0,616 |
| Capacitor | 0.022u | CAP\_0603 | 2 | 0,073 | 0,146 |
| Capacitor | 100u | CAP\_1210 | 1 | 0,949 | 0,949 |
| Capacitor | 4.7u | CAP\_0603 | 6 | 0,15 | 0,9 |
| Capacitor | 0.47u | CAP\_0603 | 1 | 0,12 | 0,12 |
| Capacitor | 5pF | CAP\_0603 | 1 | 0,061 | 0,061 |
| Common mode choke | - | CM4732V301R-10 | 1 | 4,43 | 4,43 |
| CON | - | CON6M | 14 | 0,068 | 0,94 |
| DCDC Converter | - | LMZ12002 | 1 | 7,69 | 7,69 |
| DCDC Converter | - | LT3483IS6 | 1 | 6,81 | 6,81 |
| Diode | - | PMEG3002AEB | 1 | 0,49 | 0,49 |
| Inductance | 4.7uH | LQH2MCN100K02L | 1 | 0,38 | 0,38 |
| Inductance | - | Ferrite-200 | 2 | 0,079 | 0,158 |
| Instrumentation amp | - | AD8422 | 4 | 8,81 | 35,24 |
| Operational amp | - | LM324 | 10 | 0,295 | 2,95 |
| Potentiometer | 500-1M | 201XR | 1 | 0,79 | 0,79 |
| Protection | - | TPD4E1B0 | 2 | 0,736 | 1,472 |
| Resistor | 26.7k | RES\_0603 | 8 | 0,53 | 4,24 |
| Resistor | 3.4k | RES\_0603 | 16 | 0,53 | 8,48 |
| Resistor | 250 | RES\_0603 | 8 | 2,15 | 17,2 |
| Resistor | 37.4k | RES\_0603 | 4 | 0,15 | 0,6 |
| Resistor | 75k | RES\_0603 | 4 | 1 | 4 |
| Resistor | 60.4k | RES\_0603 | 4 | 0,53 | 2,12 |
| Resistor | 20k | RES\_0603 | 8 | 0,1172 | 0,9376 |
| Resistor | 10k | RES\_0603 | 9 | 0,15 | 1,35 |
| Resistor | 5k | RES\_0603 | 8 | 3,07 | 24,56 |
| Resistor | 40k | RES\_0603 | 4 | 0,839 | 3,356 |
| Resistor | 1k | RES\_0603 | 4 | 0,15 | 0,6 |
| Resistor | 32.4k | RES\_0603 | 2 | 0,1172 | 0,2344 |
| Resistor | 2.5k | RES\_0603 | 1 | 1,217 | 1,217 |
| Resistor | 11.8k | RES\_0603 | 1 | 0,3 | 0,3 |
| Resistor | 2.1k | RES\_0603 | 1 | 0,39 | 0,39 |
| Resistor | 250k | RES\_0603 | 1 | 0,8761 | 0,8761 |
| Resistor | 10 | RES\_0603 | 1 | 0,54 | 0,54 |
| RF Filter | - | EMI T filter | 6 | 0,483 | 2,898 |
| Supply battery | 9V | - | 1 | 2,572 | 2,572 |
| **TOTAL** | **-** | **-** | **207** | **-** | **157,06** |

## Table 2 : List of components for secondary PCB

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Componant** | **Value or Model** | **Pattern** | **Quantity** | **Price $/u** | **Total** |
| ADC | ADS7828 | ADS7828 | 1 | 11,66 | 11,66 |
| Capacitor | 0.12u | CAP\_0603 | 4 | 0,33 | 1,32 |
| Capacitor | 0.1u | CAP\_0603 | 31 | 0,0558 | 1,7298 |
| Capacitor | 10u | CAP\_0603 | 8 | 0,21 | 1,68 |
| Capacitor | 1u | CAP\_0603 | 5 | 0,15 | 0,75 |
| Capacitor | 2.2u | CAP\_0603 | 4 | 0,154 | 0,616 |
| CON | Male | - | 22 | 0,0671429 | 1,4771438 |
| Instrumentation amp | AD8422 | AD8422 | 4 | 8,81 | 35,24 |
| Operational amp | LM324 | LM324 | 5 | 0,295 | 1,475 |
| Protection | TPD4E1B06DCKR | TPD4E1B0 | 1 | 0,739 | 0,739 |
| Resistor | 10k | RES\_0603 | 4 | 0,15 | 0,6 |
| Resistor | 20k | RES\_0603 | 8 | 0,1172 | 0,9376 |
| Resistor | 2k | RES\_0603 | 2 | 0,53 | 1,06 |
| Resistor | 3.4k | RES\_0603 | 8 | 0,53 | 4,24 |
| Resistor | 37.4k | RES\_0603 | 4 | 0,15 | 0,6 |
| Resistor | 400k | RES\_0603 | 4 | 0,511 | 2,044 |
| Resistor | 5 | RES\_0603 | 1 | 0,24 | 0,24 |
| Resistor | 50 | RES\_0603 | 4 | 0,16 | 0,64 |
| Resistor | 5k | RES\_0603 | 8 | 3,07 | 24,56 |
| Resistor | 60.4k | RES\_0603 | 4 | 0,53 | 2,12 |
| Resistor | 75k | RES\_0603 | 4 | 1 | 4 |
| Supply | 9V | - | 2 | 2,572 | 5,144 |
| **TOTAL** | **-** | **-** | **138** | **-** | **102,87** |

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