19-1943; Rev 0; 1/01

MAXIM

Dual, 256-Tap, Low-Drift, Digital Potentiometers in 14-Pin TSSOP

General Description

The MAX5413/MAX5414/MAX5415 is a family of dual linear taper digital potentiometers. Each device has two 3-terminal potentiometers. The MAX5413/MAX5414/MAX5415 operate from +2.7V to +5.5V single-supply voltages and use an ultra-low 0.1µA supply current. These devices also provide glitchless switching between resistor taps, as well as a convenient power-on reset (POR) that sets the wiper to the midscale position at power-up. Each potentiometer consists of a fixed resistor with a wiper contact that is digitally controlled through a 3-wire serial interface and has 256 tap points. It performs the same function as a discrete potentiometer or variable resistor.

These parts are ideal for applications requiring digitally controlled resistors. Three resistance values are available: 10kΩ (MAX5413), 50kΩ (MAX5414), and 100kΩ (MAX5415). A nominal resistor temperature coefficient of 35ppm/°C end-to-end and 5ppm/°C ratiometric make the MAX5413/MAX5414/MAX5415 ideal for applications requiring low temperature-coefficient variable resistors, such as adjustable-gain circuit configurations.

The MAX5413/MAX5414/MAX5415 are available in a 14-pin TSSOP package. Each device is guaranteed over the extended industrial temperature range (-40°C to +85°C).

Applications

Mechanical Potentiometer Replacement

Low-Drift Programmable Gain Amplifier (PGA)

Volume Control

LCD Screen Adjustment

Adjustable Voltage Reference

Programmable Filters, Delays, Time Constant

Impedance Matching

SPI is a trademark of Motorola, Inc.

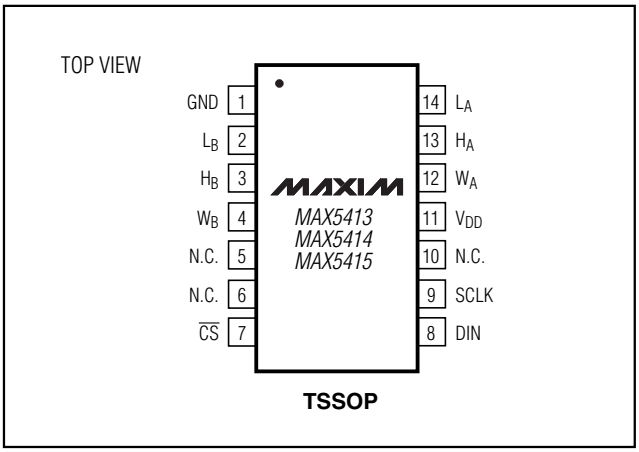
Features

- **14-Pin TSSOP Small-Footprint Package**
- **256 Tap Positions**
- **Ultra-Low 0.1µA Supply Current**
- **+2.7V to +5.5V Single-Supply Operation**
- **Two Independent Potentiometers in a Package**
- **Low End-to-End Temperature Coefficient 35ppm/°C**
- **Low Ratiometric Temperature Coefficient 5ppm/°C**
- **Power-On Reset: Wiper Goes to Midscale (Position 128)**
- **Glitchless Switching Between Resistor Taps**
- **3-Wire SPI™-Interface Compatible**
- **10kΩ/50kΩ/100kΩ Resistor Values**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	R (kΩ)
MAX5413EUD	-40°C to +85°C	14 TSSOP	10
MAX5414EUD	-40°C to +85°C	14 TSSOP	50
MAX5415EUD	-40°C to +85°C	14 TSSOP	100

Pin Configuration



TSSOP

Dual, 256-Tap, Low-Drift, Digital Potentiometers in 14-Pin TSSOP

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
DIN, SCLK, $\overline{CS}$ .....-0.3V to +6V
H_X, L_X, W_X to GND .....-0.3V to (V_{DD} +0.3)
Maximum Continuous Current into H_X, L_X, and W_X.....±1mA
Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, unless otherwise noted. V_H = V_{DD}, V_L = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE (Voltage-Divider Mode)							
Resolution	N			8			Bits
Integral Nonlinearity (Notes 1, 2)	INL					±1/2	LSB
Differential Nonlinearity (Notes 1, 2)	DNL					±1/2	LSB
End-to-End Resistor Tempco	TC_R				35		ppm/°C
Ratiometric Resistor Tempco					5		ppm/°C
Full-Scale Error		MAX5413			-8		LSB
		MAX5414			-1.6		
		MAX5415			0.8		
Zero-Scale Error		MAX5413			+8		LSB
		MAX5414			+1.6		
		MAX5415			+0.8		
DC PERFORMANCE (Variable-Resistor Mode)							
Resolution	N			8			Bits
Integral Nonlinearity (Notes 1, 3)	INL	V_{DD} = +5V				±1	LSB
		V_{DD} = +3V	MAX5413			±3	LSB
			MAX5414			±1.5	
			MAX5415			±1.5	
Differential Nonlinearity (Notes 1, 3)	DNL	V_{DD} = +5V				±1/2	LSB
		V_{DD} = +3V					
DC PERFORMANCE (Resistor Characteristics)							
Wiper Resistance (Note 4)	R_W	V_{DD} = +5V			275		Ω
		V_{DD} = +3V				550	
Wiper Capacitance	C_W	MAX5413			50		pF
		MAX5414/MAX5415			30		
End-to-End Resistance	R_{HL}	MAX5413		7.5	10	12.5	kΩ
		MAX5414		37.5	50	62.5	
		MAX5415		75	100	125	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, unless otherwise noted. V_H = V_{DD}, V_L = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input High Voltage	V_{IH}			0.7 x V_{DD}			V
Input Low Voltage	V_{IL}					0.3 x V_{DD}	V
Input Leakage Current						±1.0	µA
Input Capacitance					5		pF
TIMING CHARACTERISTICS (ANALOG)							
Wiper-Settling Time	t_S	MAX5413			100		ns
		MAX5414			325		
		MAX5415			650		
TIMING CHARACTERISTICS (DIGITAL) (Note 5)							
Maximum SCLK Frequency				10			MHz
SCLK Clock Period	t_{CP}			100			ns
SCLK Pulse Width High	t_{CH}			40			ns
SCLK Pulse Width Low	t_{CL}			40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}			40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}			0			ns
DIN Setup Time	t_{DS}			40			ns
DIN Hold Time	t_{DH}			0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}			10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}			40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}			100			ns
POWER SUPPLIES							
Supply Voltage	V_{DD}			2.7		5.5	V
Supply Current	I_{DD}	$\overline{CS}$ = SCLK = DIN = V_{DD}	V_{DD} = +5V		0.8	5	µA
			V_{DD} = +2.7V		0.1		µA

Note 1: Linearity is defined in terms of the H_X to L_X code-dependent resistance.

Note 2: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H_X = V_{DD} and L_X = 0. The wiper terminal is unloaded and measured with an ideal voltmeter.

Note 3: The DNL and INL are measured with the potentiometer configured as a variable resistor. H_X is unconnected and L_X = 0. At V_{DD} = +5V, the wiper terminal is driven with a source current of 400µA for the 10kΩ configuration, 80µA for the 50kΩ configuration, and 40µA for the 100kΩ configuration. At V_{DD} = +3V, 200µA/40µA/20µA for 10kΩ/50kΩ/100kΩ configurations, respectively.

Note 4: The wiper resistance is the worst value measured by injecting into W_X, a current I_W = V_{DD} / R_{HL}.

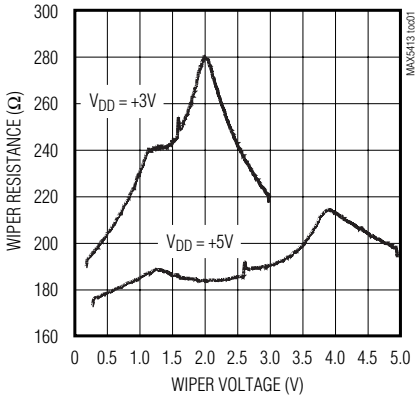
Note 5: Digital timing is guaranteed by design.

Dual, 256-Tap, Low-Drift, Digital Potentiometers in 14-Pin TSSOP

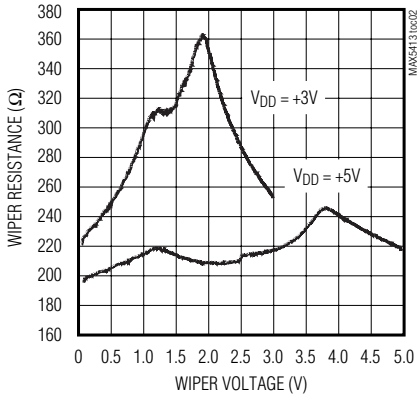
Typical Operating Characteristics

(V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.)

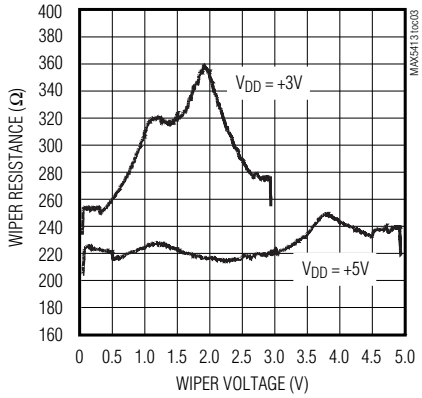
WIPER RESISTANCE vs. WIPER VOLTAGE (10kΩ)



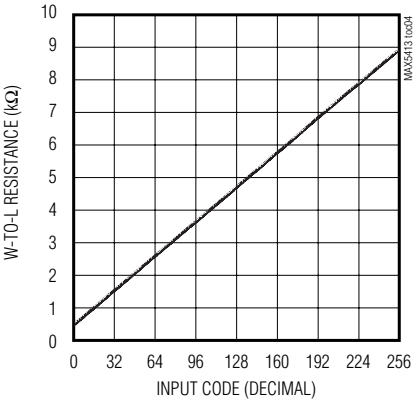
WIPER RESISTANCE vs. WIPER VOLTAGE (50kΩ)



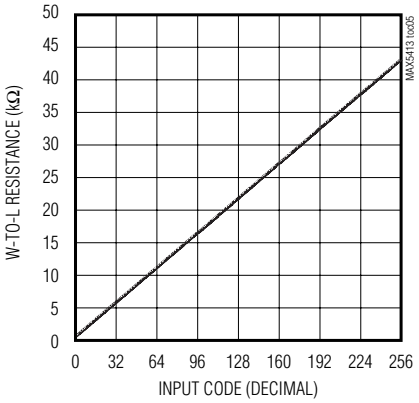
WIPER RESISTANCE vs. WIPER VOLTAGE (100kΩ)



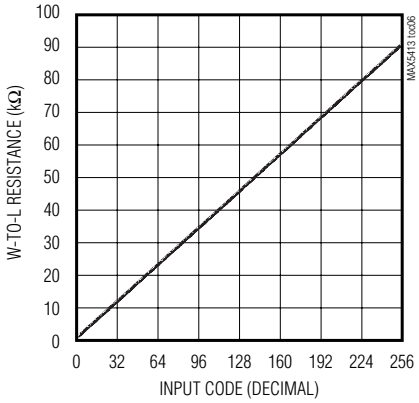
WIPER RESISTANCE vs. INPUT CODE (10kΩ)



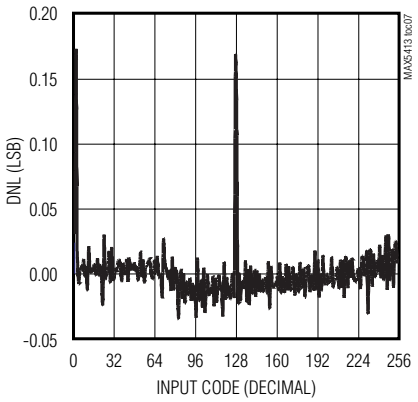
WIPER RESISTANCE vs. INPUT CODE (50kΩ)



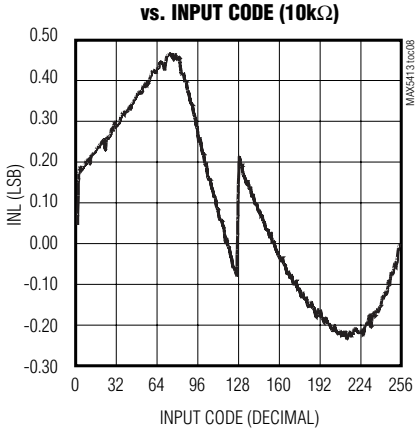
WIPER RESISTANCE vs. INPUT CODE (100kΩ)



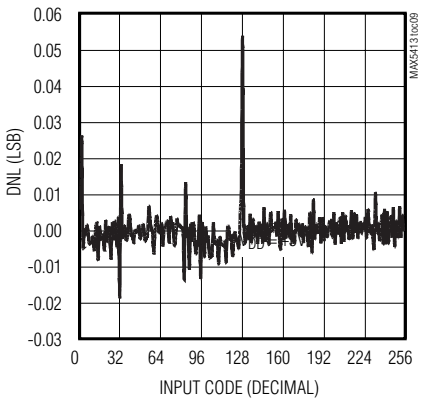
VARIABLE RESISTOR DNL vs. INPUT CODE (10kΩ)



VARIABLE RESISTOR INL vs. INPUT CODE (10kΩ)



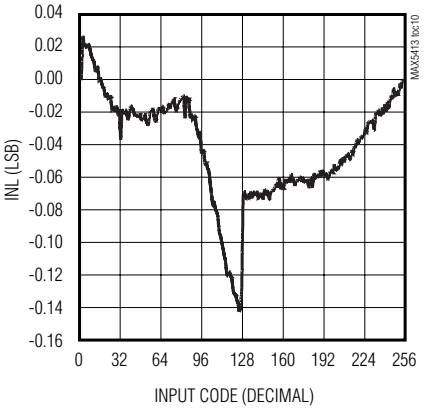
VARIABLE RESISTOR DNL vs. INPUT CODE (50kΩ)



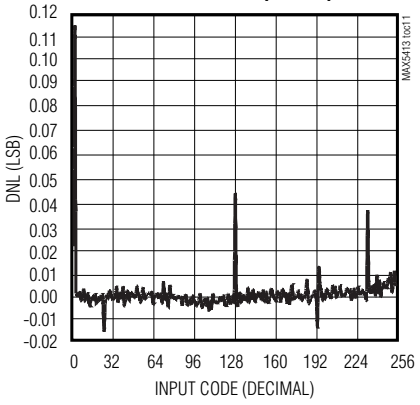
Typical Operating Characteristics (continued)

(V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.)

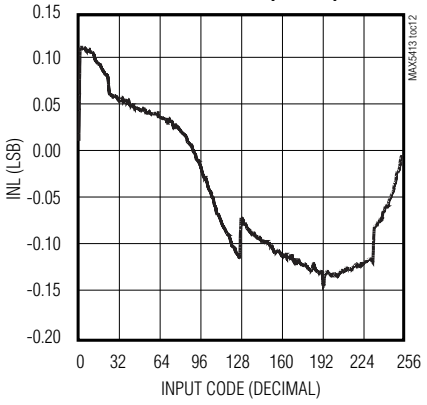
VARIABLE RESISTOR INL vs. INPUT CODE (50kΩ)



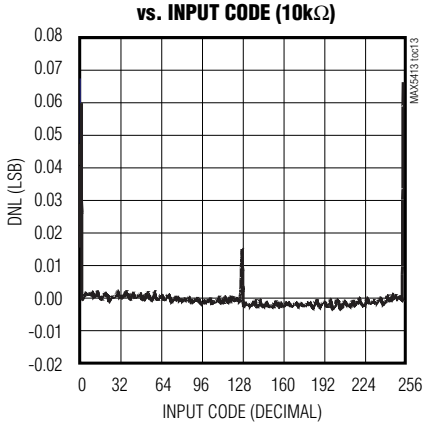
VARIABLE RESISTOR DNL vs. INPUT CODE (100kΩ)



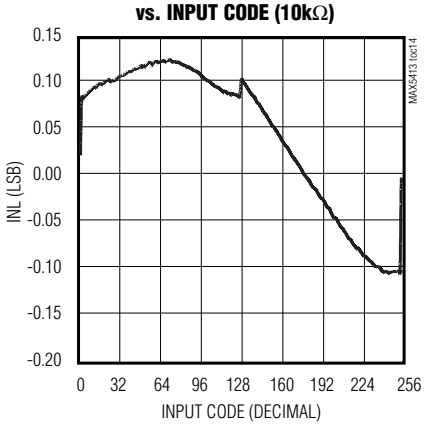
VARIABLE RESISTOR INL vs. INPUT CODE (100kΩ)



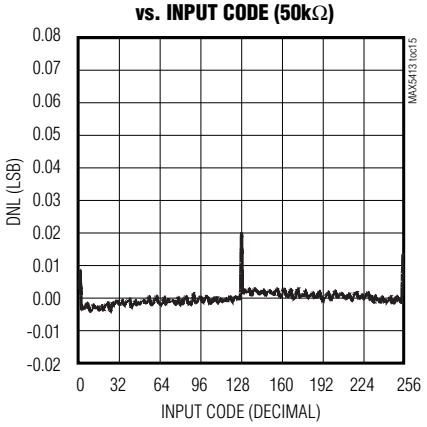
VOLTAGE-DIVIDER DNL vs. INPUT CODE (10kΩ)



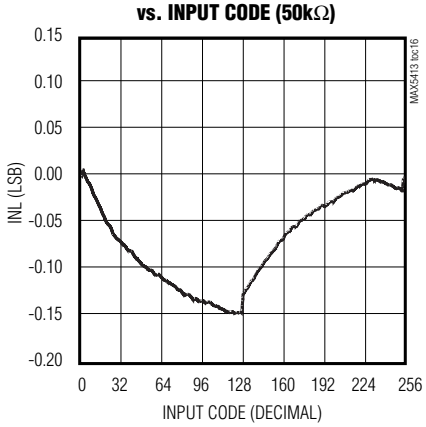
VOLTAGE-DIVIDER INL vs. INPUT CODE (10kΩ)



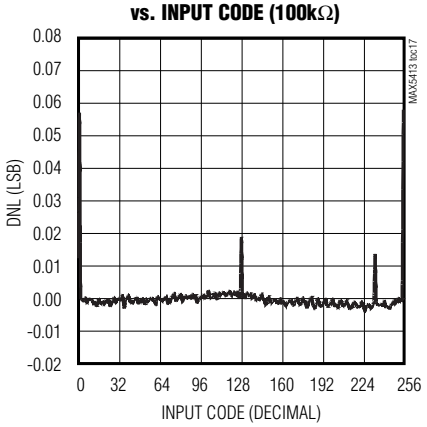
VOLTAGE-DIVIDER DNL vs. INPUT CODE (50kΩ)



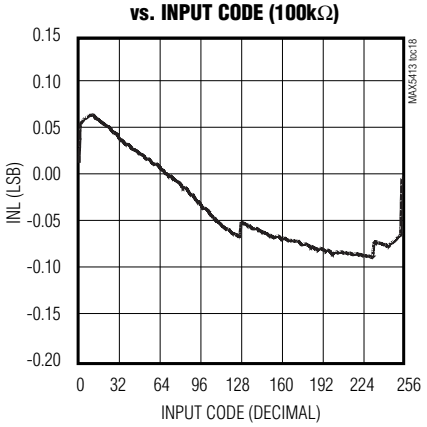
VOLTAGE-DIVIDER INL vs. INPUT CODE (50kΩ)



VOLTAGE-DIVIDER DNL vs. INPUT CODE (100kΩ)



VOLTAGE-DIVIDER INL vs. INPUT CODE (100kΩ)

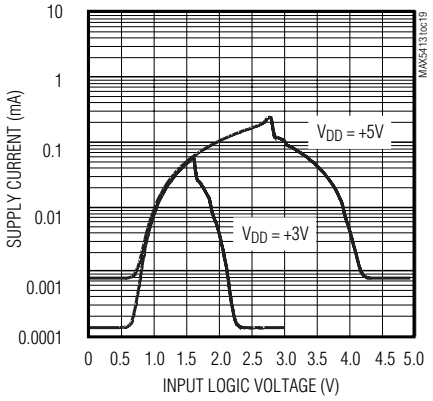


Dual, 256-Tap, Low-Drift, Digital Potentiometers in 14-Pin TSSOP

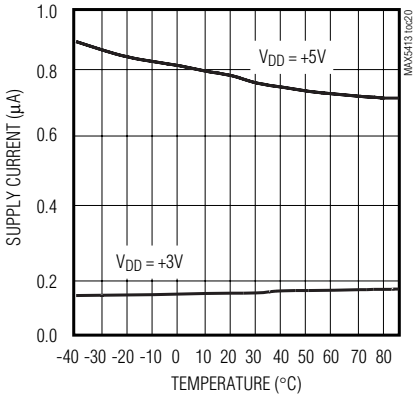
Typical Operating Characteristics (continued)

(V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.)

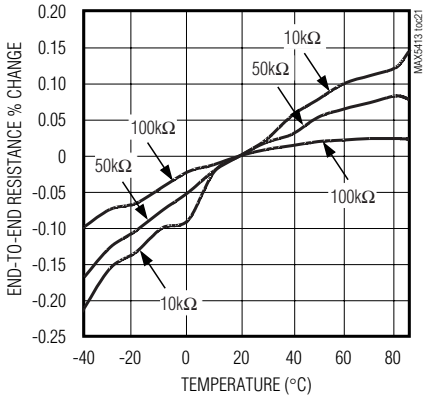
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



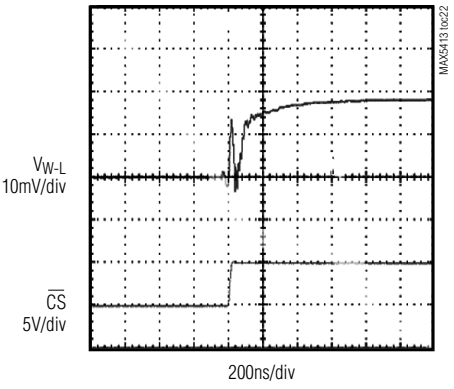
SUPPLY CURRENT vs. TEMPERATURE



END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128)



Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	L_B	Low Terminal of Resistor B
3	H_B	High Terminal of Resistor B
4	W_B	Wiper Terminal of Resistor B
5, 6, 10	N.C.	No Connection to this Terminal
7	$\overline{CS}$	SPI Chip Select
8	DIN	SPI Serial Data Input
9	SCLK	SPI Clock Input
11	V_{DD}	Power Supply, +2.7V to +5.5V. Connect a 0.1µF capacitor to GND.
12	W_A	Wiper Terminal of Resistor A
13	H_A	High Terminal of Resistor A
14	L_A	Low Terminal of Resistor A

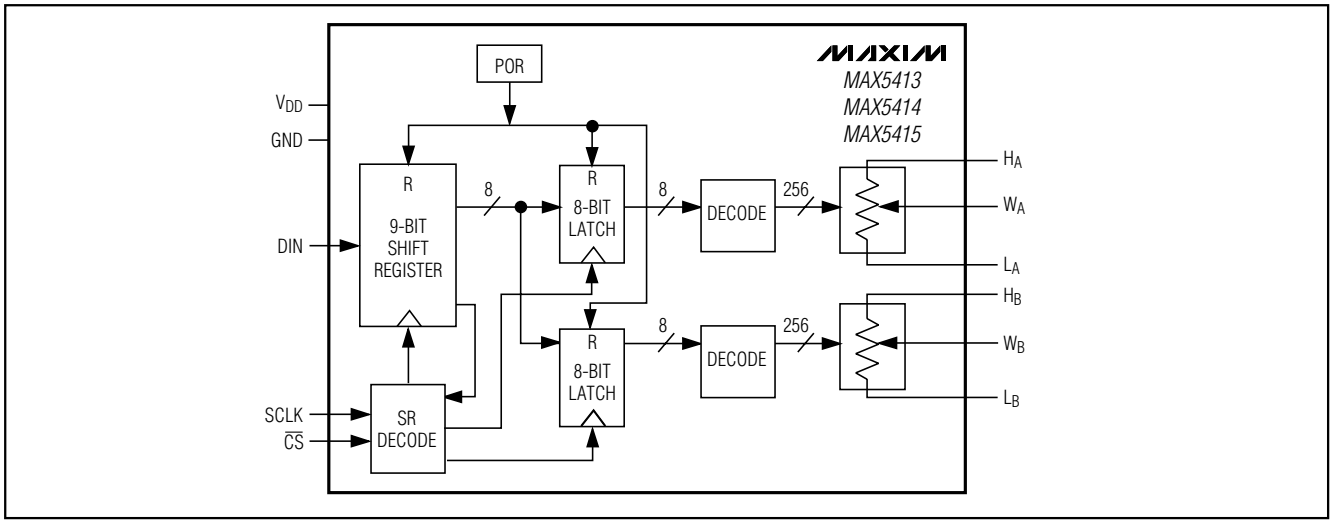


Figure 1. MAX5413/MAX5414/MAX5415 Functional Diagram: Dual 3-Terminal Potentiometers in 14-Pin TSSOP Configuration

Detailed Description

Each potentiometer consists of 255 fixed resistors in series between pins H_X and L_X (Figure 1). The potentiometer wiper (pin W_X) can be programmed to access any one of the 256 different tap points on the resistor string. The MAX5413/MAX5414/MAX5415 require nine bits to program the wiper position. The first bit is an address code, allowing one or the other potentiometer to be selected for programming. The potentiometers are programmed independently of each other.

The MAX5413/MAX5414/MAX5415 use a 3-wire serial data interface to control the wiper tap position. This write-only interface contains three inputs: Chip Select ($\overline{CS}$), Data In (DIN), and Data Clock (SCLK). When $\overline{CS}$ is taken low, data from the DIN pin is synchronously loaded into the serial shift register on each rising edge of each SCLK pulse (Figure 2). After all the data bits

Dual, 256-Tap, Low-Drift, Digital Potentiometers in 14-Pin TSSOP

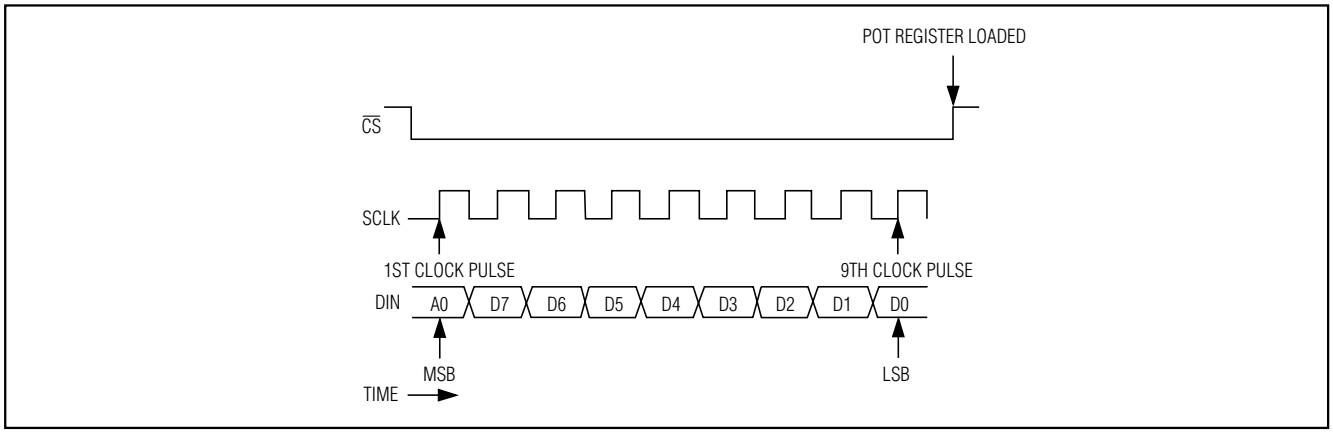


Figure 2. Potentiometer Serial Data Timing Circuit

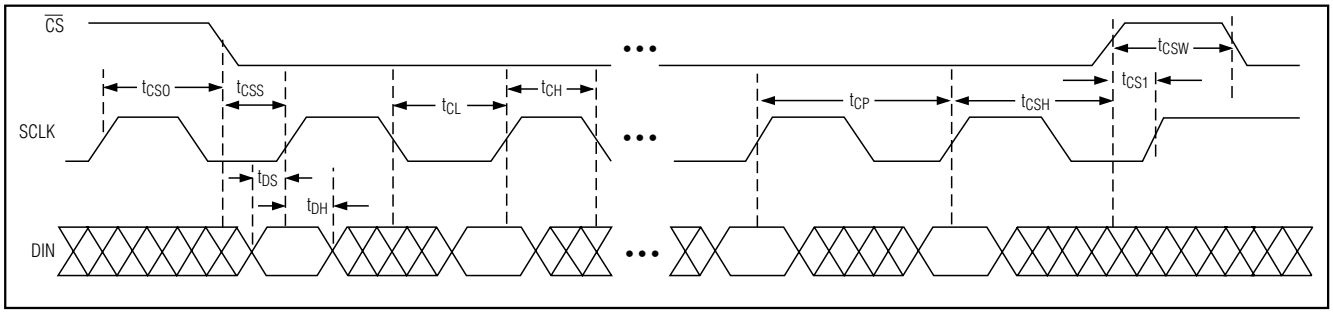


Figure 3. Detailed Serial Interface Timing Diagram

have been shifted in, they are latched into the appropriate potentiometer control register when $\overline{CS}$ transitions from low to high. Note that if $\overline{CS}$ is not kept low during the entire data stream, the data will be corrupted and the device will need to be reloaded.

The first bit A0 (address bit) is used to address one or the other of the potentiometers for programming. Potentiometer control register A is selected for writing when A0 is 'zero,' and potentiometer control register B is selected when A0 is 'one.'

The MAX5413/MAX5414/MAX5415 feature POR circuitry that sets the wiper to the midscale position at power-up.

Applications Information

The MAX5413/MAX5414/MAX5415 are intended for a variety of circuits where accurate, fine-tuning adjustable resistance is required, such as in adjustable voltage or adjustable gain circuit configurations. It is primarily used in either a potentiometer divider or a variable-resistor configuration.

Adjustable Current-to-Voltage Converter

Figure 5 shows the MAX5413/MAX5414/MAX5415 being used with a MAX4250 low-noise op amp to fine tune a current-to-voltage converter. Pins H_X and W_X of the MAX5413/MAX5414/MAX5415 are connected to the node between R3 and R2, and pin L_X is connected to ground. Circuit space is minimized due to both devices' packaging.

Adjustable Gain Amplifier

Figure 6 shows how to use the MAX5413/MAX5414/MAX5415 to digitally adjust the gain of a noninverting op amp configuration. In Figure 6a, connect the MAX5413/MAX5414/MAX5415 as a variable resistor in series with a resistor to ground to form the adjustable gain control of a noninverting amplifier.

Similarly, Figure 6b shows how to use the MAX5413/MAX5414/MAX5415 as a 3-terminal potentiometer. In this application, the MAX5413/MAX5414/MAX5415 low 5ppm/°C ratiometric tempco allows for a very stable adjustable gain configuration over temperature.

ADDRESS	DATA WORD							
B0 (A0)	**B1** (D7)	**B2** (D6)	**B3** (D5)	**B4** (D4)	**B5** (D3)	**B6** (D2)	**B7** (D1)	**B8** (D0)
(MSB)								(LSB)
First Bit In								Last Bit In

Figure 4. Serial Data Format

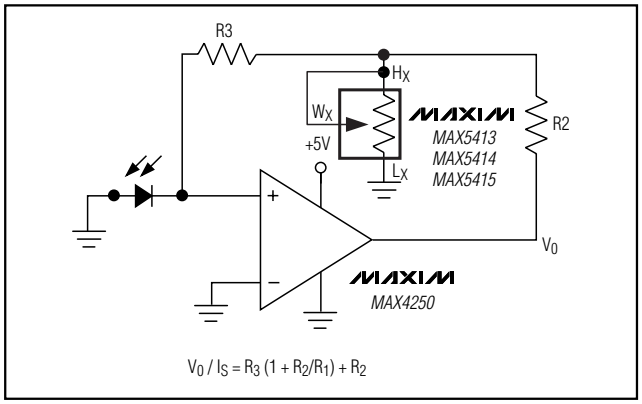


Figure 5. I to V Converter

Adjustable Voltage Reference

In Figure 7, the MAX5413/MAX5414/MAX5415 are shown with the MAX6160 to make an adjustable voltage reference. In this circuit, the H_X pin of the MAX5413/MAX5414/MAX5415 is connected to the OUT pin of the MAX6160, the L_X pin of the MAX5413/MAX5414/MAX5415 is connected to GND, and the W_X pin of the MAX5413/MAX5414/MAX5415 is connected to the ADJ pin of the MAX6160. The MAX5413/MAX5414/MAX5415 allow precise setting of the voltage reference output. A low 5ppm/°C ratiometric tempco allows a very stable adjustable voltage overtemperature.

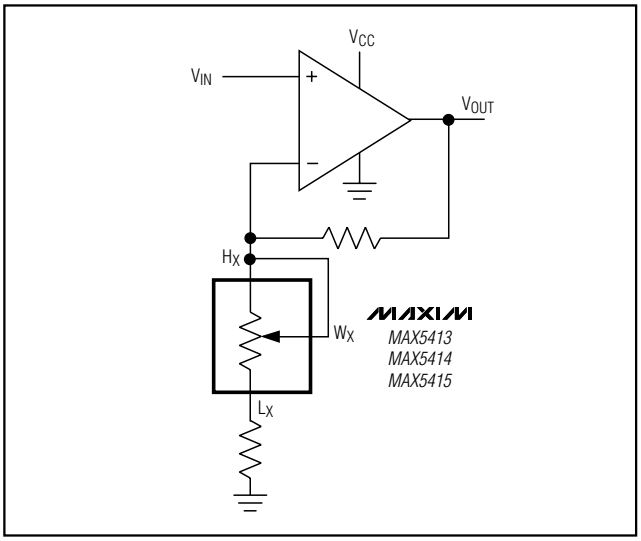


Figure 6a. Adjustable Gain Circuit

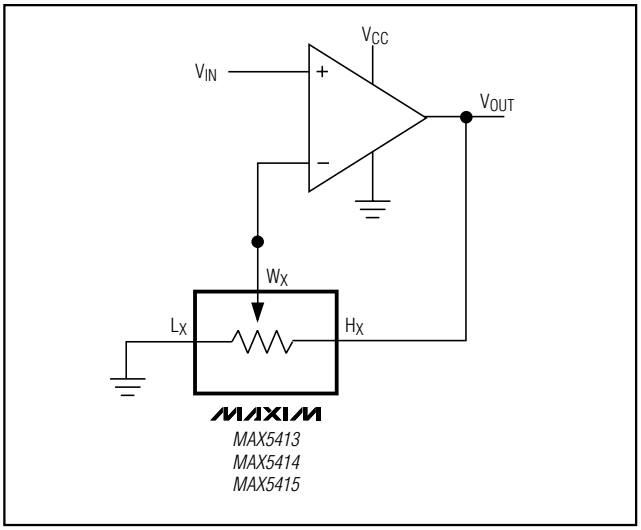


Figure 6b. Adjustable Gain Circuit Using 3-Terminal Potentiometer

Dual, 256-Tap, Low-Drift, Digital Potentiometers in 14-Pin TSSOP

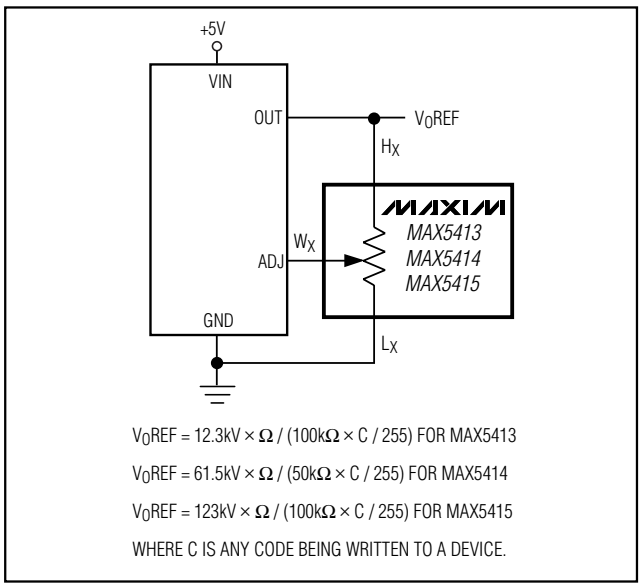


Figure 7. Adjustable Voltage Reference

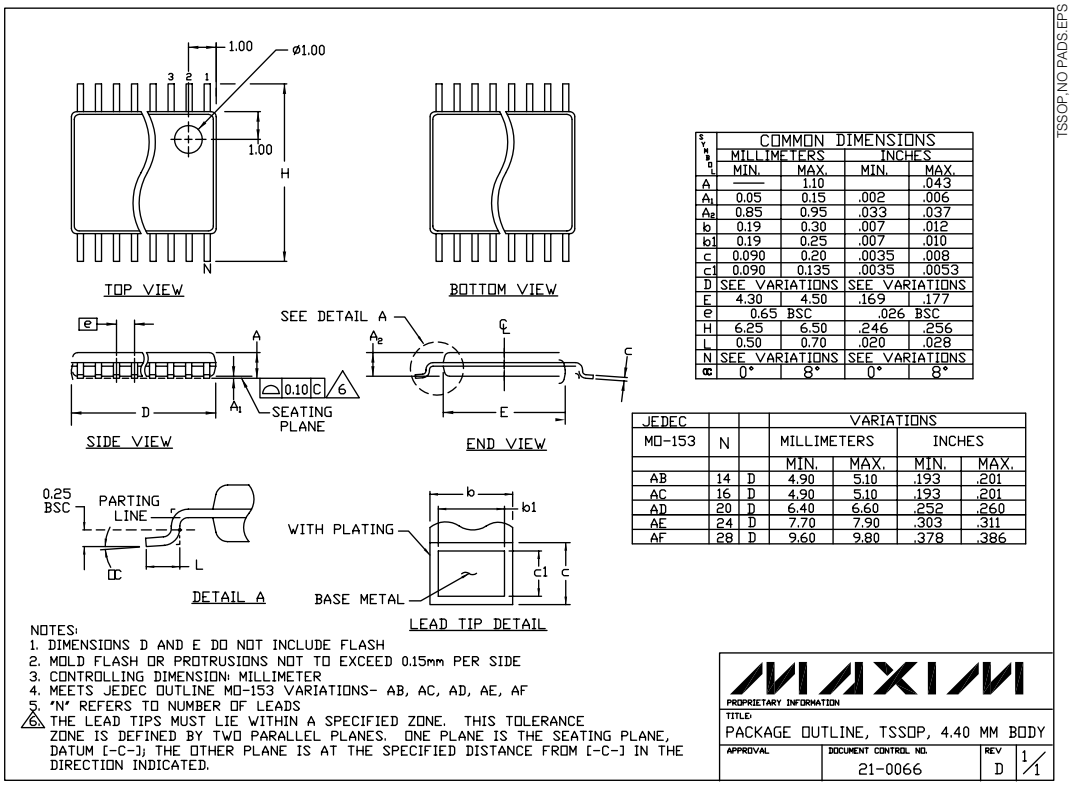
Chip Information

TRANSISTOR COUNT: 8689

PROCESS: BiCMOS

Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AD	20	D	6.40	6.60	.252	.260
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS- AB, AC, AD, AE, AF
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	D	1/1