Analog Discovery 2™ Reference Manual

Revised September 14, 2015
This manual applies to the Analog Discovery 2 rev. C

Table of Contents

Overview

The Digilent Analog Discovery developed in conjunction with Analog Devices is a multi

A D

A D BNC A BNC
D F A
D

The Analog Discovery 2.

- channel oscilloscope V differential
  M MH
  A D BNC A B
- M MH A
  D BNC A B
- A G
- CMO
  M
- I O
  LED
  iv
- CMO
  M
- CMO
- Two programmable power supplies V
  A D
- B
- A
- AC DC
- N B N N
  H MH
- A
  FD N HD
- D B A PI I C A P

A D I
B

M

A D

hardware s features and limitations It is not intended to provide enough information to enable complete
A D

A D A D

- A
  B A D A D
- N
- I
- B

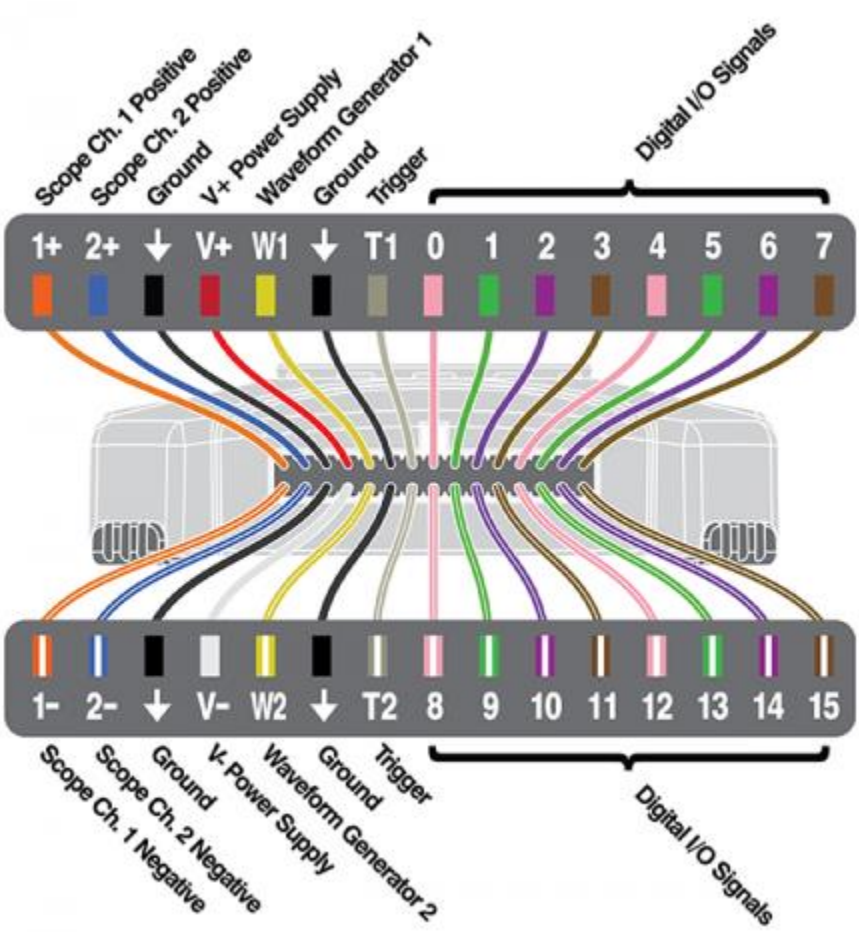

Figure 1. Analog Discovery 2 pinout diagram.

1 Architectural Overview and Block Diagram

A D F A D
FPGA C L L F
programs the Discovery s FPGA at start
O FPGA D PC
F B F FPGA
A D

Analog Input **Scope** use S indexes to indicate they are related to the scope
Analog Output **AWG** use AWG indexes and signals in the **Digital**
D D F

rtain naming conventions Analog voltages are prefixed with a V for
IN M

B F ADC C A G
P N F

Analog Inputs/Scope

Input Divider and Gain Control H
FPGA

Buffer

Driver ADC O

Scope Reference and Offset

ADC

Arbitrary Outputs/AWG

DAC A G

I/V

Out

Audio

A **Oscillator** **Clock Generator** AD DA

Digital I/O FPGA D P G
L A

Power Supplies and Control

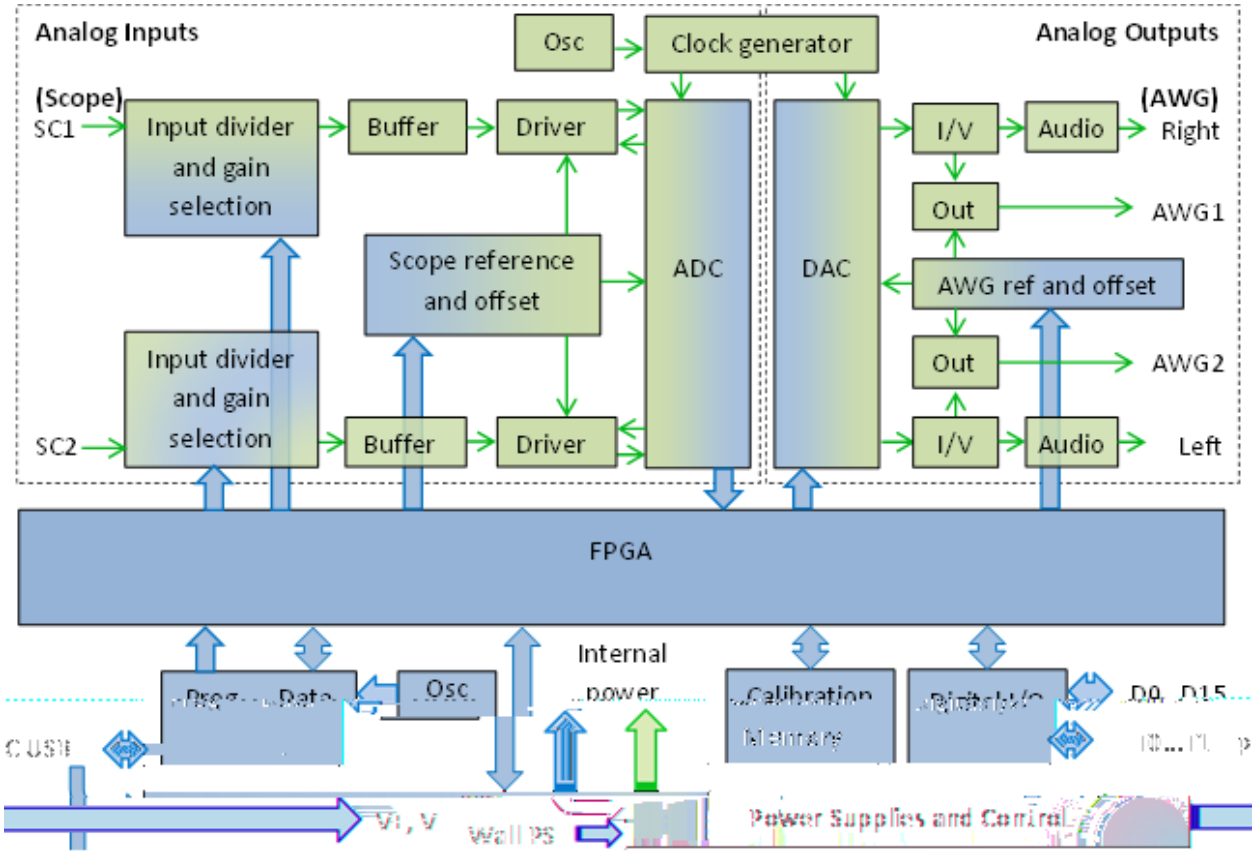

Figure 2. Analog Discovery 2 block diagram.

B B MH
F C CD ON OFF

L G

$$\frac{V_{mux}}{V_{in}} = \frac{R_6}{R_1 + R_4 + R_6} = 0.019 \quad (3)$$

L G

$$|V_{in\,diff}| = |V_{in\,P} - V_{in\,N}| < 50V \quad (4)$$

H G

$$\frac{V_{mux}}{V_{in}} = \frac{R_4 + R_6}{R_1 + R_4 + R_6} = 0.212 \quad (5)$$

H G

$$|V_{in\,diff}| = |V_{in\,P} - V_{in\,N}| < 7V \quad (6)$$

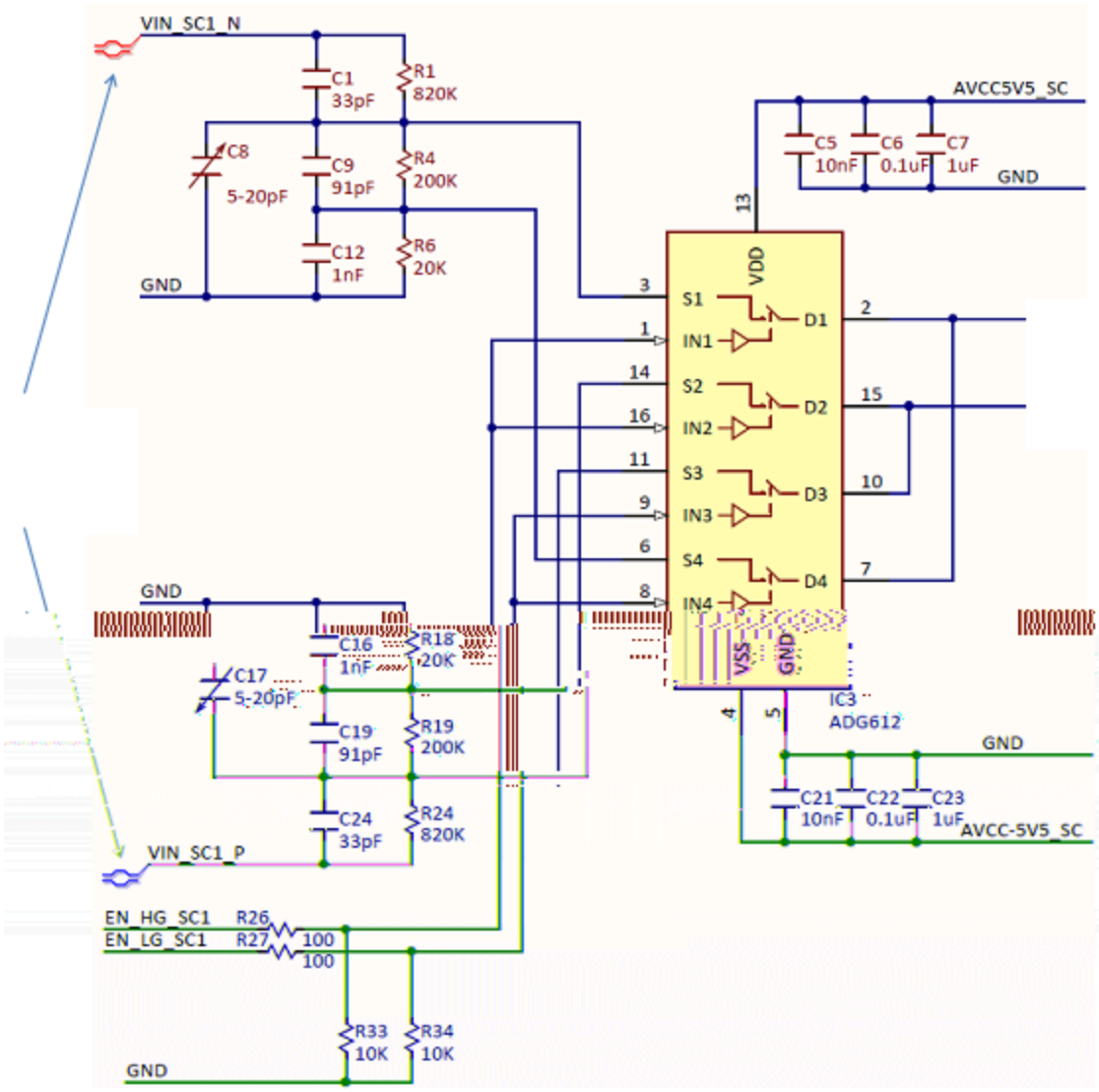

Figure 3. Input divider and gain selection.

2.2 Scope Buffer

A O A F

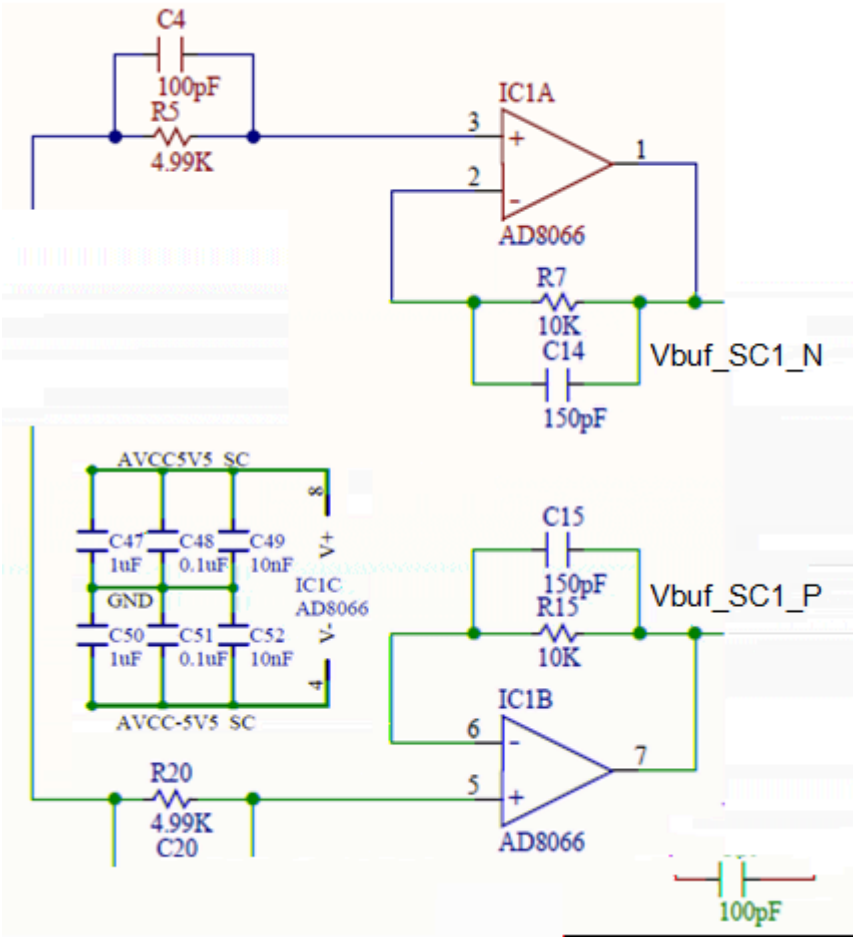

Figure 4. Scope buffer.

AD

FE
A
L
H H d bandwidth G
V s slew rate G
Low noise nV H f kH fA H f kH

L
E
SFDR d c MH
L A
M OP

AD

$$-5.5V < V_{mux\,P}, V_{mux\,N} < 2.2V \quad (7)$$

$$-5.38V < V_{buf\,P}, V_{buf\,N} < 5.4V \quad (8)$$

G

$$\frac{V_{buf}}{V_{mux}} = 1 \quad (9)$$

2.3 Scope Reference and Offset

F A

B

A

DAC B

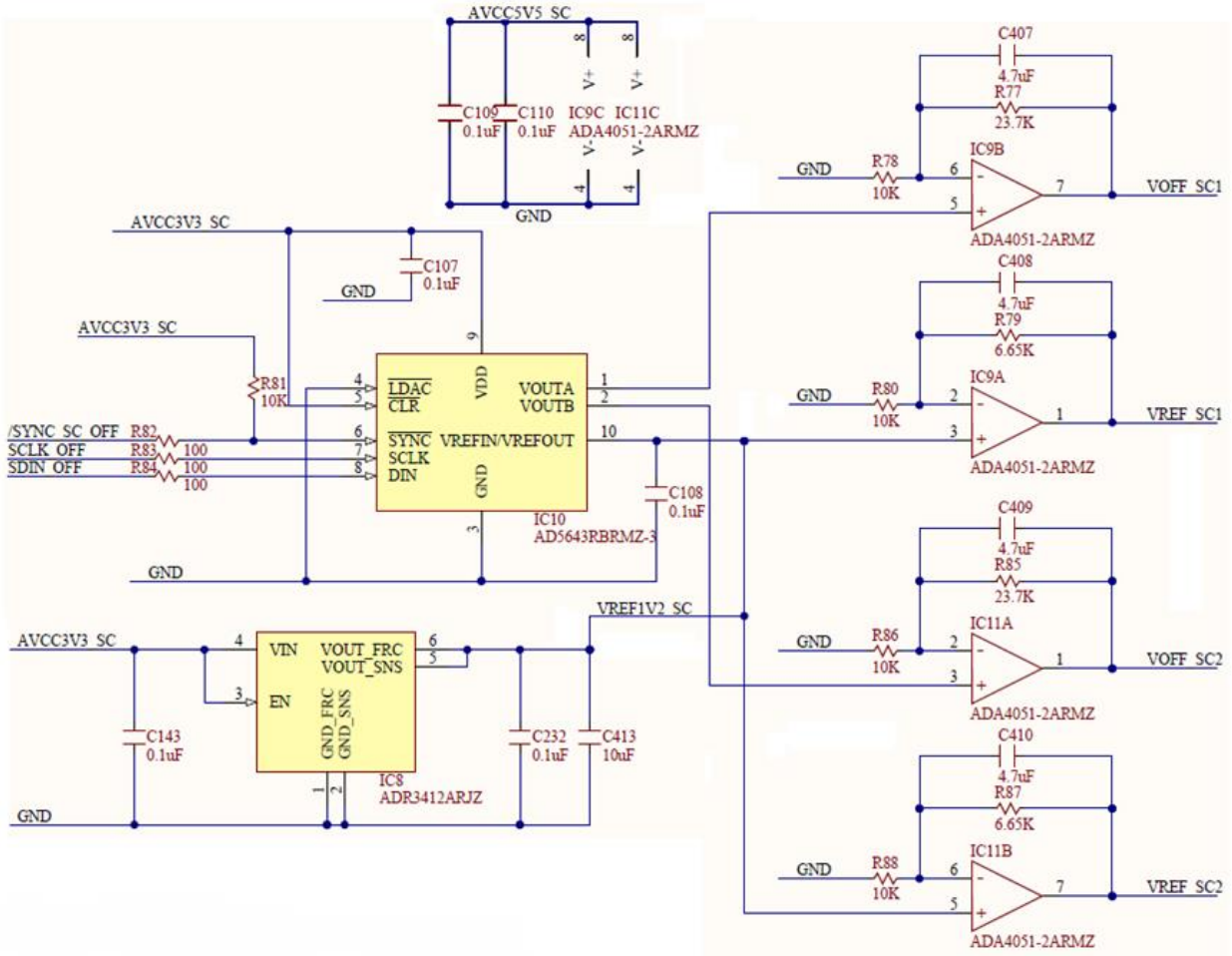

Figure 5. Scope reference and offset.

AD A J M

I
L C
Low quiescent current A maximum
Output noise H to H V p

AD D B DAC

L DAC

MH

ADA M O A

Very low supply current A typical
L V maximum
O C
H P B

$$V_{ref\ SC} = V_{ref\ 1V2} \cdot \left(1 + \frac{R_{79}}{R_{80}}\right) = 2V \quad (10)$$

$$0 \leq V_{off\ SC} = V_{out\ AD5643} \cdot \left(1 + \frac{R_{77}}{R_{78}}\right) < 4.044V \quad (11)$$

2.4 Scope Driver

ADA ADC

MH
E B HD H B HD MH
Low input voltage noise nV H

A
F LFC P
A

IC **Error! Reference source not found.**

D ADC
P ADC
A EF C OFF C

$$V_{Out+IC2A} = V_{CM} + \frac{AVCC1V8}{2} \cdot \frac{R_{23}}{R_{25}} = 0.9V + \frac{1.8V}{2} \cdot \frac{4.99K}{6.34K} = 1.6V \quad (17)$$

D D ADC

$$-0.1V < V_{+ADA4940} = V_{-ADA4940} < 1.9V \quad (18)$$

2.5 Clock Generator

A IC MH F

ADF C G PLL I CO MH
ADC MH DAC

A D ADI PLL F PLL
L B H P M
P H H

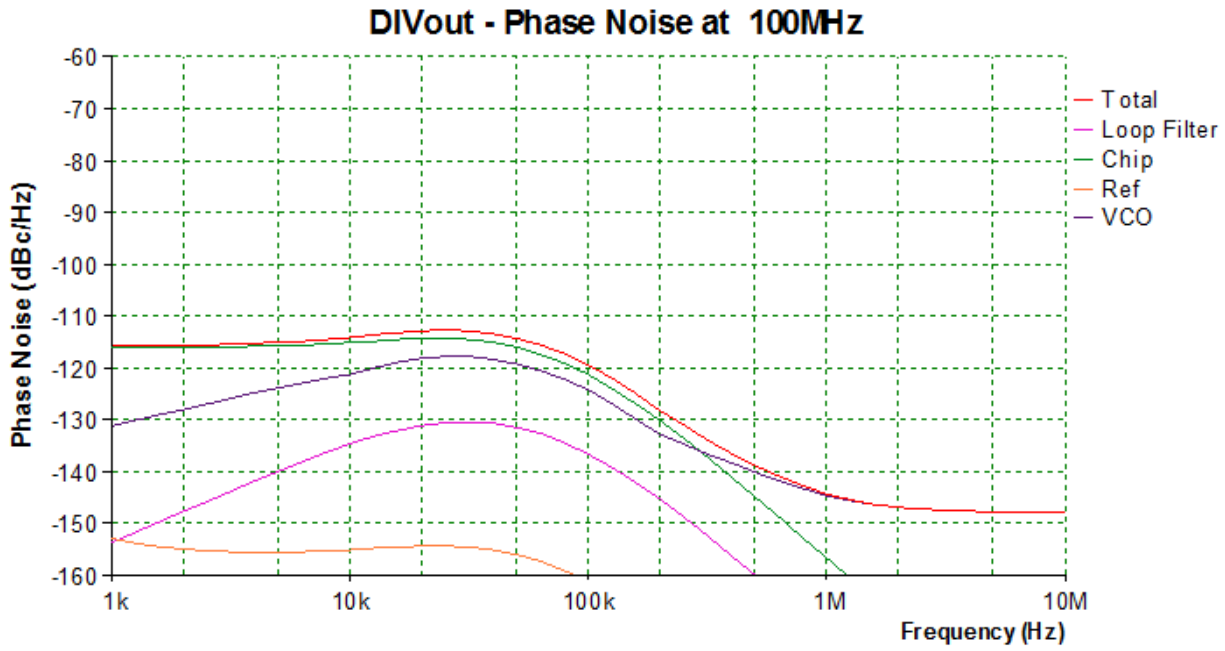

Figure 7. Phase noise figure for the clock generator.

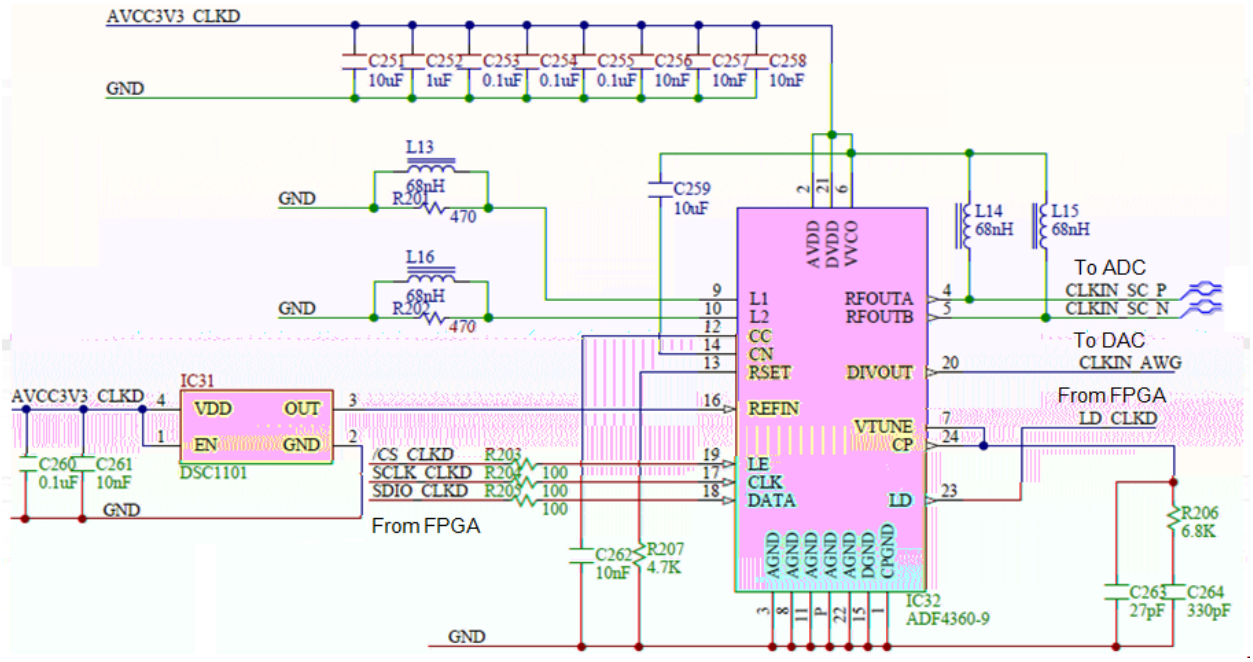

Figure 8. Clock generator.

2.6 Scope ADC

2.6.1 Analog Section

A D M P ADC A
AD F

D

C

AC

MH A IC

ADC CM C

$$-1V < V_{ADC\ diff} < 1V \quad \textbf{(19)}$$

2.6.2 Digital Section

ADC FPGA

FPGA

CLKO C FPGA F

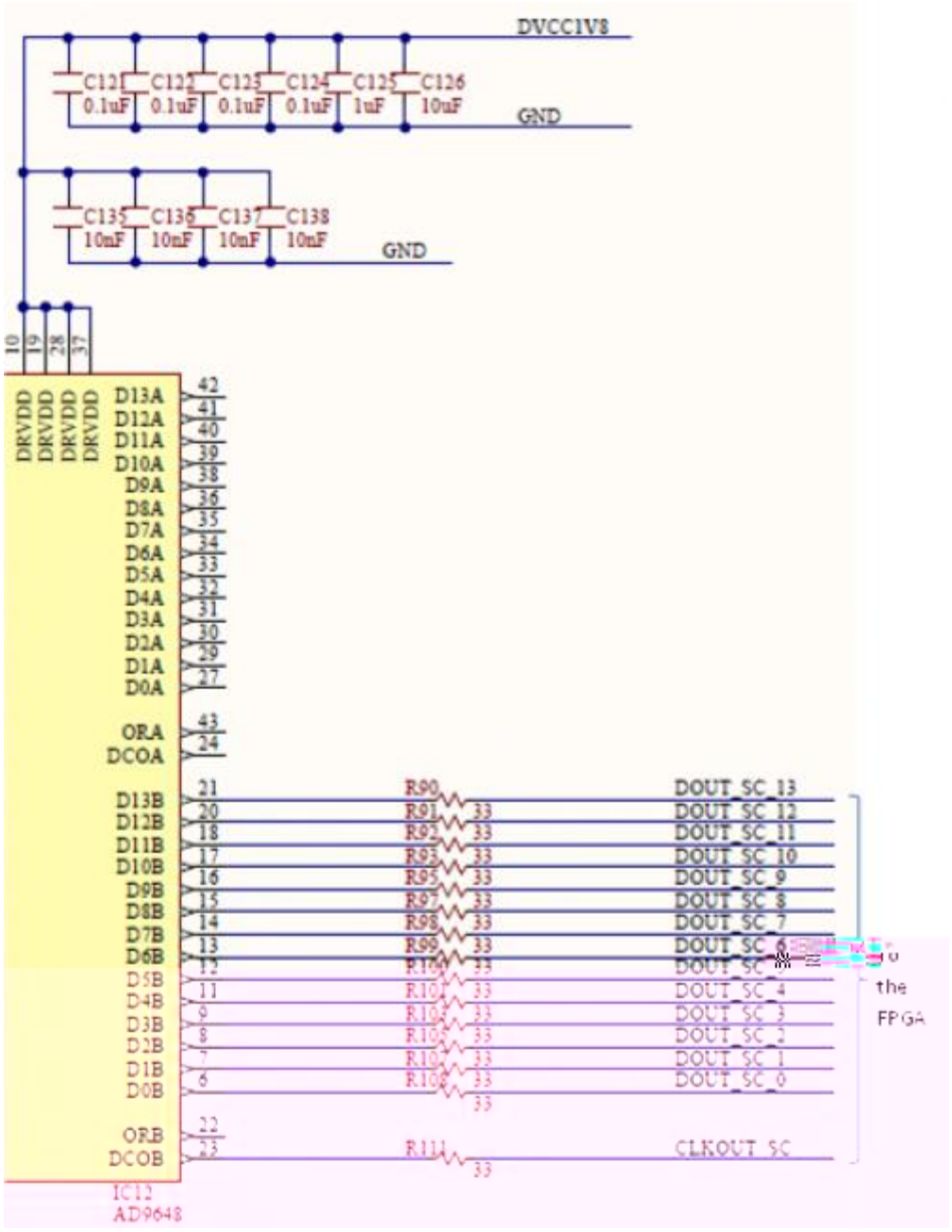

Figure 10. ADC - digital section.

2.7 Scope Signal Scaling

C G **(3) (5) (9) (13) (14) (15)**

$$\boldsymbol{Low\ Gain = \frac{V_{ADC\ diff}}{V_{in\ diff}} = 0.034}$$

$$\boldsymbol{High\ Gain = \frac{V_{ADC\ diff}}{V_{in\ diff}} = 0.375} \quad \textbf{(20)}$$

C ADC **(19)** V_{offsc} **(11)**

$$\textbf{at Low Gain}: -\mathbf{30V} < \boldsymbol{V_{in\,diff}} < 28.\mathbf{6V}$$
$$\textbf{at High Gain}: -\mathbf{2.7V} < \boldsymbol{V_{in\,diff}} < 2.6\mathbf{V} \quad \textbf{(21)}$$

$$\textbf{at Low Gain}: -\mathbf{25V} < \boldsymbol{V_{in\,diff}} < 25\mathbf{V}$$
$$\textbf{at High Gain}: -\mathbf{2.5V} < \boldsymbol{V_{in\,diff}} < 2.5\mathbf{V} \quad \textbf{(22)}$$

(10) (11) (14)

$$-\mathbf{2V} < V_{offSC} - \boldsymbol{V_{refSC}} < 2.\mathbf{044V} \quad \textbf{(23)}$$

$V_{off\ eq\ in}$

$$\textbf{at Low Gain}: -\mathbf{59.3V} < V_{\boldsymbol{off\ eq\ in}} < 59.\mathbf{3V}$$
$$\textbf{at High Gain}: -\mathbf{5.39V} < V_{\boldsymbol{off\ eq\ in}} < 5.3\mathbf{9V} \quad \textbf{(24)}$$

$V_{off\ eq\ in}$ $V_{in\,diff}$ **(21)** **(22)**
$V_{off\ eq\ in}$ **(24)**

E **( ) (7) (8) (12)** **(19)** IC
C F
F E E
L G H G *Vin diff* *Vin CM*
VinP *VinN*

linear range

O
A D A
I

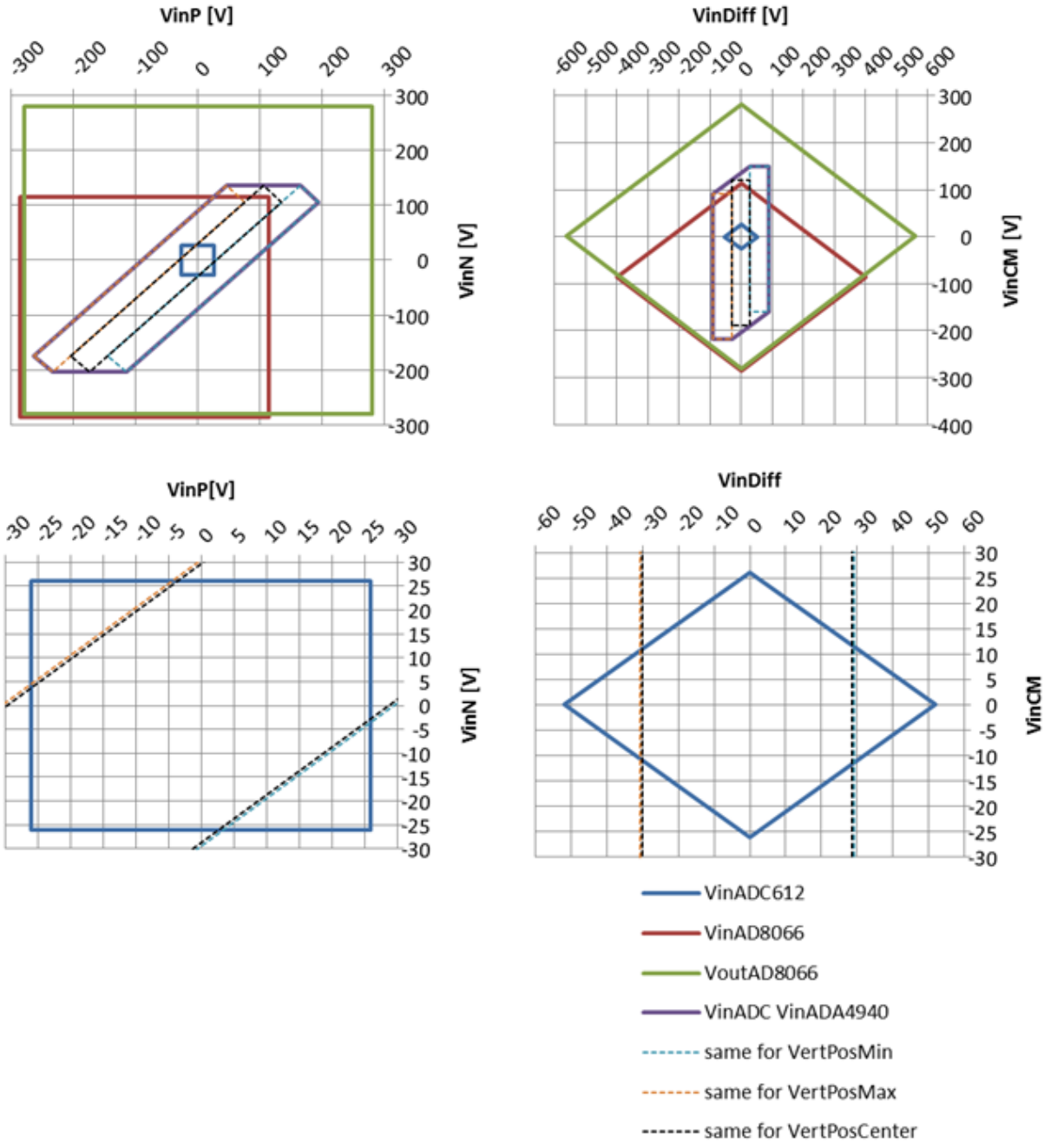

Figure 11. Scope input signal range.

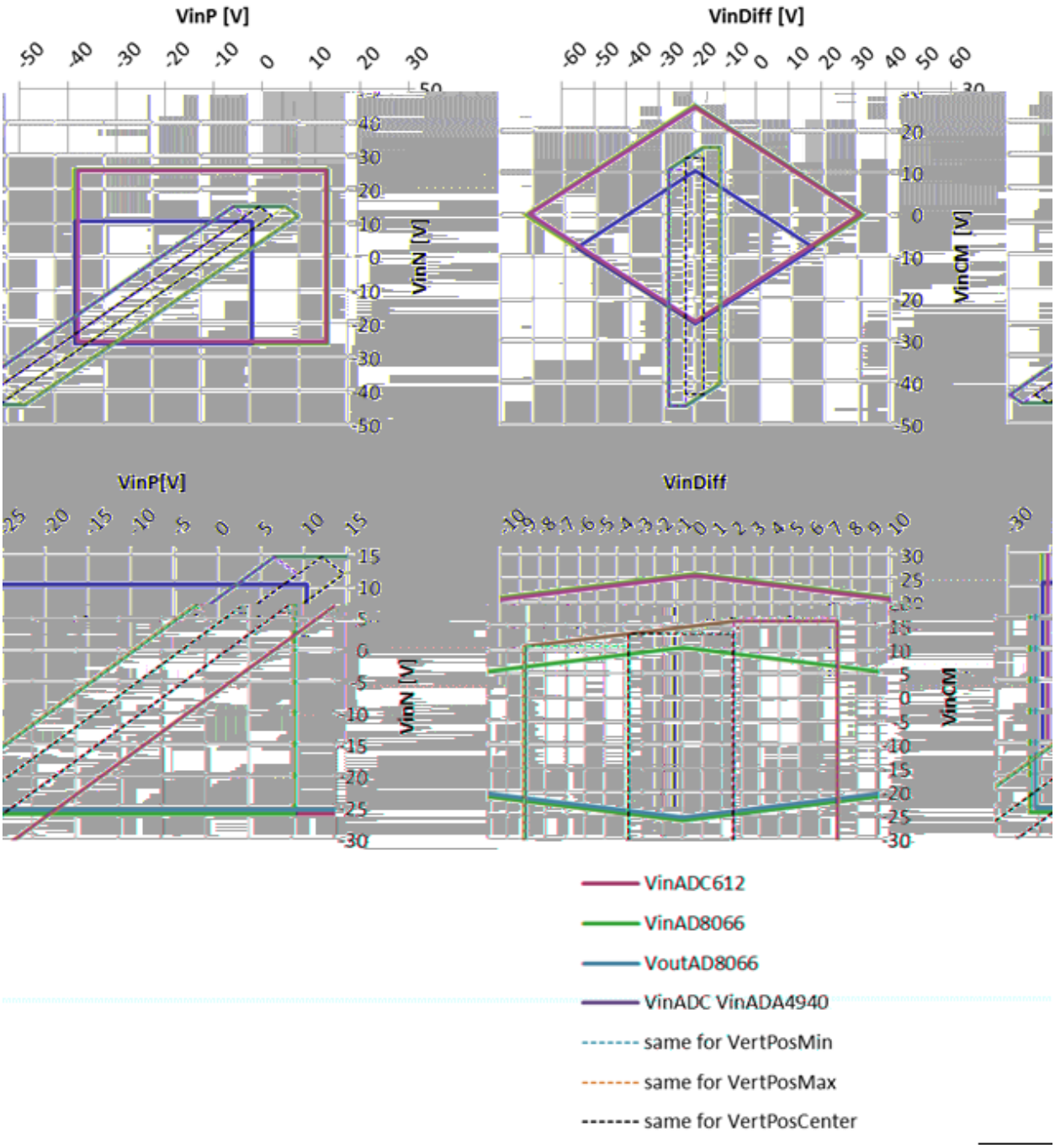

Figure 12. Scope input signal range.

VoffSc = 2.022V **(11)**

VoffSc = 4.044V

VoffSc = 0V A

A

ADC

F

A

ADC
representation It is the user s responsibility to understand and avoid such situations

F L G F
V_{inP}, V_{inN} ( )

F H G F (7) ( )

$$-26V < V_{inP}, V_{inN} < 10V \quad (25)$$

A

$$-7.5V < V_{inDiff} < 7.5V \quad (26)$$

N

F

DC

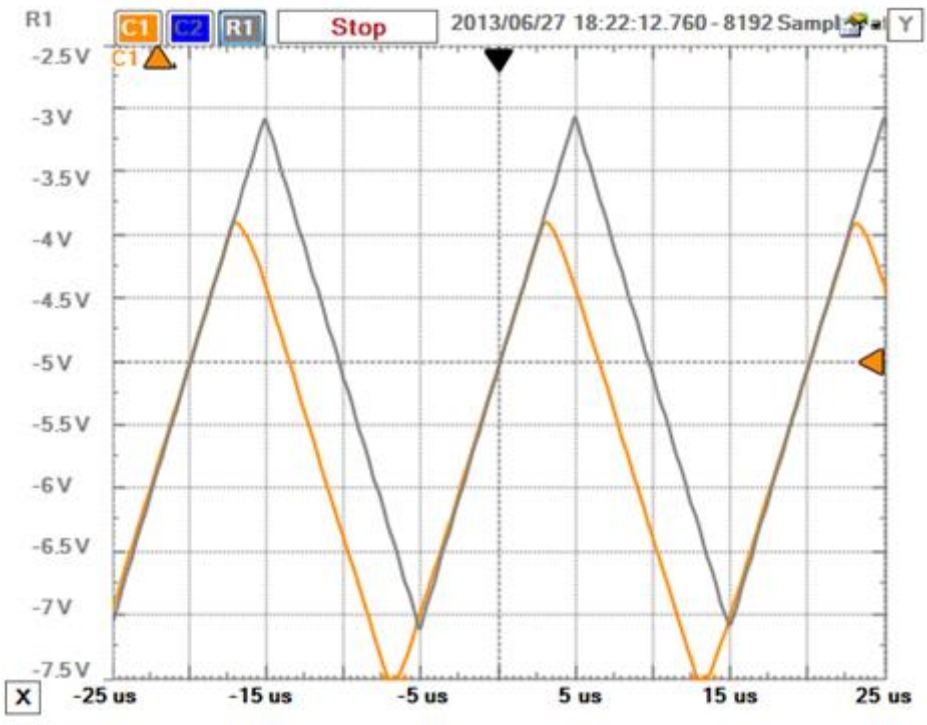

Figure 13. Common mode input voltage limitation.

2.8 Scope Spectral Characteristics

F A A A MH F A
G M H MH A
D D BNC D

N A G E G
F B MH B
MH B MH

B A

A

D MH B MH
MH B MH

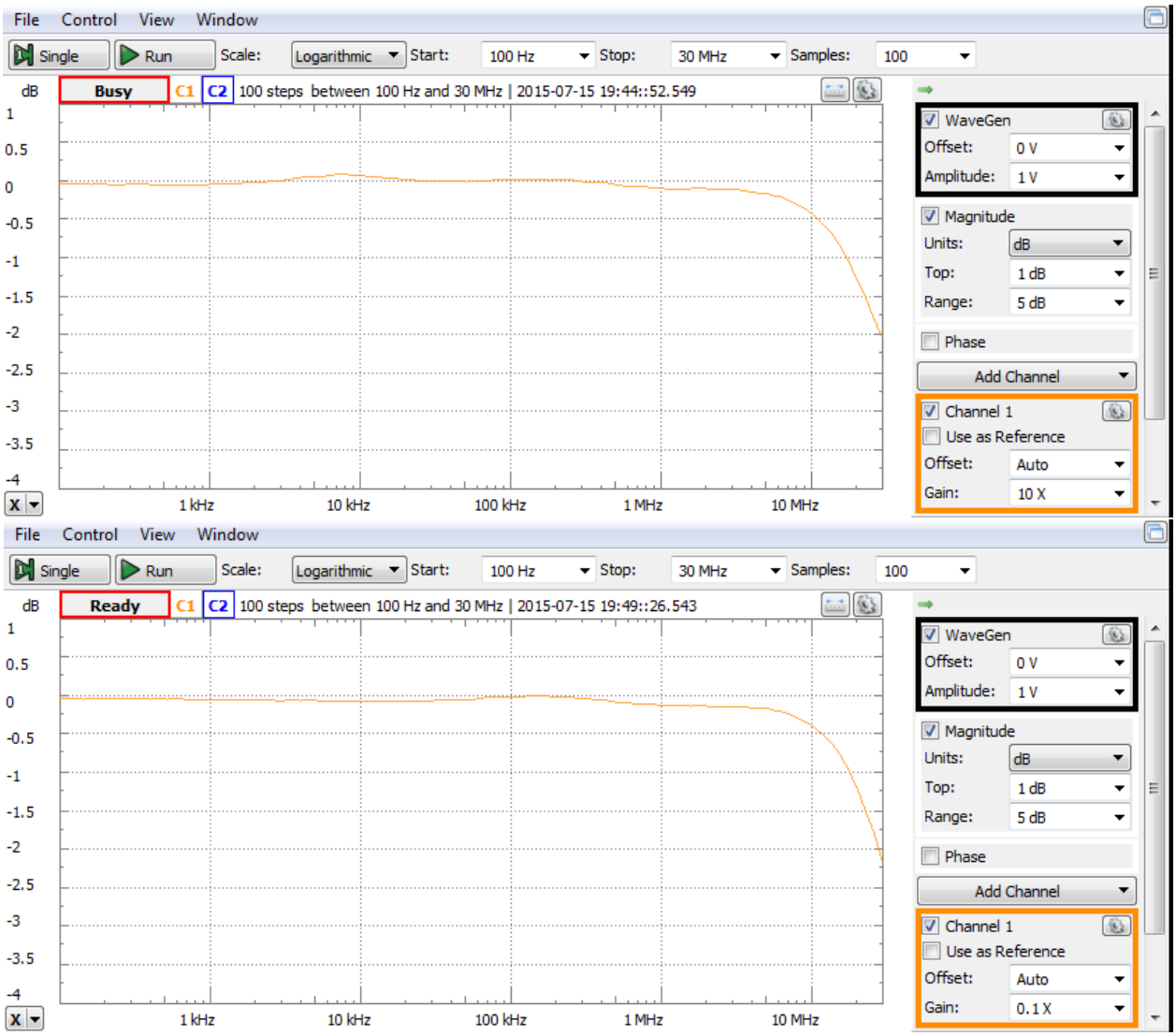

Figure 14. Scope spectral characteristic diagram

- Low Gain (up)
- High Gain (down)

A F D D BNC
A D
A D H

3 Arbitrary Waveform Generator

3.1 AWG DAC

A D AD DAC
F

P A M P

FD N B MH B MH
AD N D MH output SPS mA d c H
D A A
CMO
O

LFC P H

PI FPGA MH
E A G
I A G P N I F F ADJ
F The ADG OS Low Power Dual UX DE UX is used to connect R set of either k or
k from FSADJx pin to GND

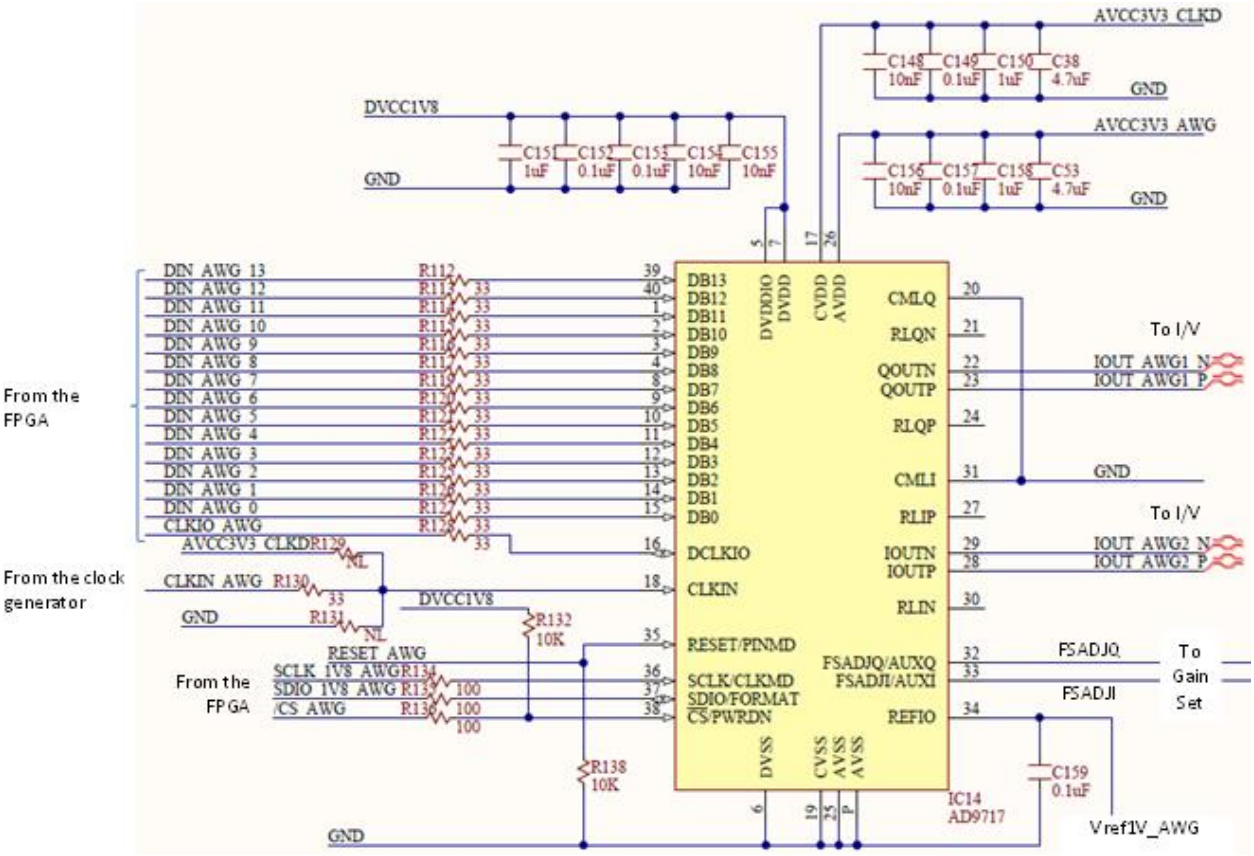

Figure 15. DAC.

ADG

B MH

Low on resistance tγpica

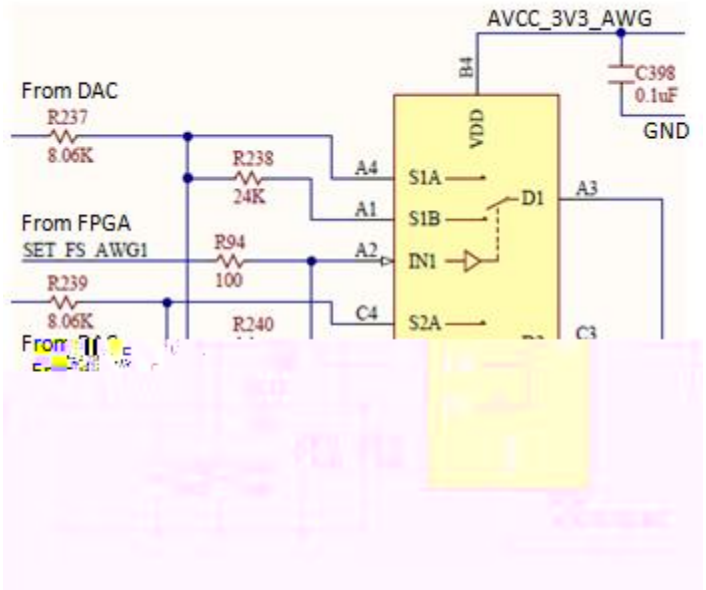

Figure 16. DAC - gain set.

3.2 AWG Reference and Offset

A F A G IC AD A J A DAC

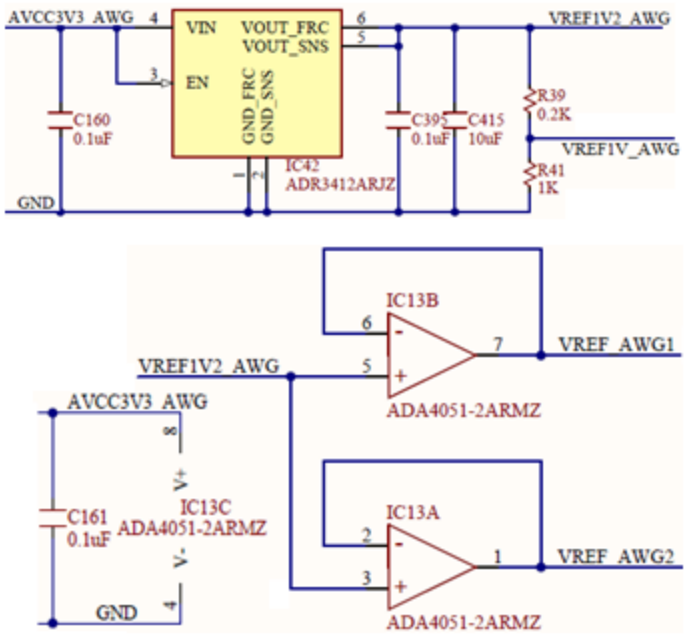

Figure 17. DAC - Reference voltages.

$$V_{ref1V\_AWG} = V_{ref1V2\_AWG} \cdot \frac{R_{41}}{R_{39} + R_{41}} = 1V \quad (27)$$

B I A G F DAC

$$I_{outAWGFS} = 32 \cdot \frac{V_{ref1V\_AWG}}{R_{set}} \quad (28)$$

F H G

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{8k\Omega} = 4mA \quad (29)$$

F L G

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{32k\Omega} = 1mA \quad (30)$$

A AD Q DAC DC A G
F E E

- L DAC
-
- M
- P A G DC

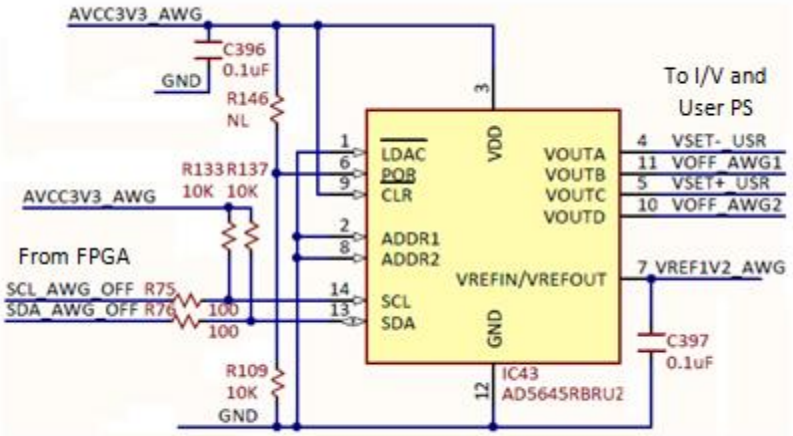

Figure 18. DAC - Offset voltages.

F IC

$$V_{offAWGFS} = V_{SET\_USRFS} = V_{ref1V2AWG} = 1.2V \quad (31)$$

4.3 AWG I/V

IC 15 in

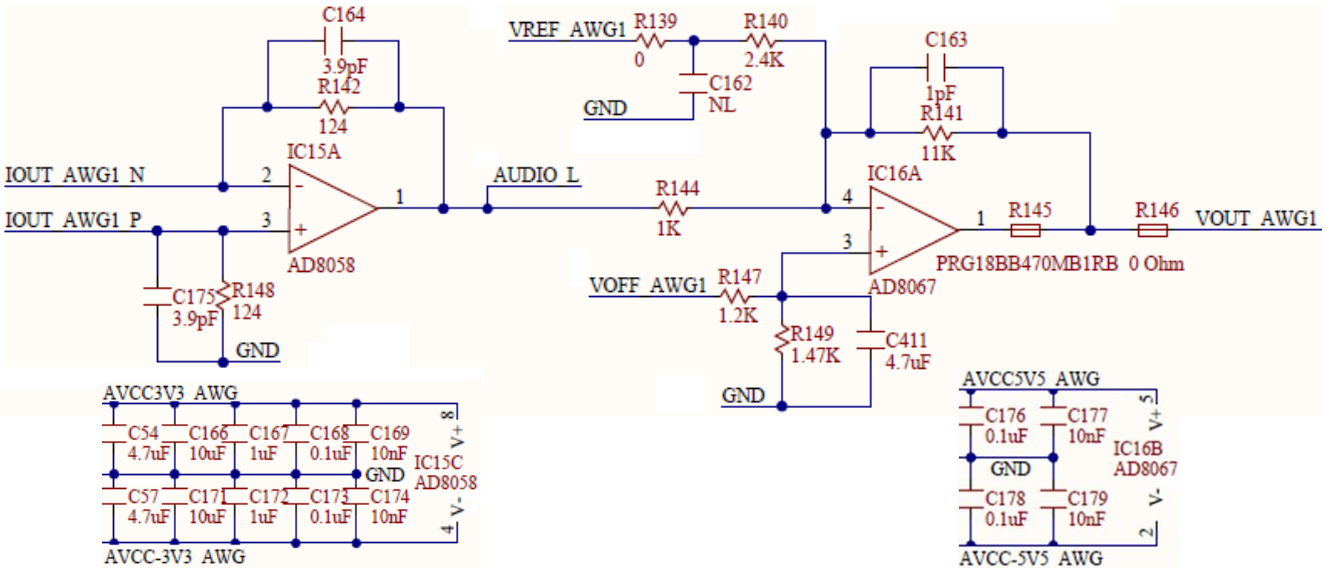

Figure 19. AWG I/V and out.

I AD

- L
- H d bandwidth G
- V s slew rate
- G B MH
- Low noise nV H
- L A
- Low distortion d c H RL k
-
-

$$\begin{gathered}\boldsymbol{V_{Audio} = I_{outAWGP} \cdot R_{148} - I_{outAWGN} \cdot R_{142} =} \\ \boldsymbol{= (1 - 2 \cdot \{A_U\}) \cdot I_{outAWGFS} \cdot R_{142} = \{A_B\} \cdot I_{outAWGFS} \cdot R_{142}}\end{gathered} \quad \textbf{(32)}$$

$$\begin{gathered}\boldsymbol{\{A_U\} = \frac{D}{2^N} \in [0 \dots 1);\ -\ normalized\ unipolar\ DAC\ input\ number} \\ \boldsymbol{\{A_B\} = (1 - 2 \cdot \{A_U\}) \in [-1 \dots 1);\ -\ normalized\ bipolar\ DAC\ input\ number\ (binary\ offset)} \\ \boldsymbol{D \in [0 \dots 2^{14}) = [0 \dots 2^{14} - 1];\ -\ integer\ unipolar\ DAC\ input\ number}\end{gathered} \quad \textbf{(33)}$$

$$\boldsymbol{-V_{AudioFS} \leq V_{Audio} < -V_{AudioFS}} \quad \textbf{(34)}$$

H G L G

$$\begin{gathered}\boldsymbol{V_{AudioFS\_HG} = I_{outAWGFS\_HG} \cdot R_{142} = 496\text{mV}} \\ \boldsymbol{V_{AudioFS\_LG} = I_{outAWGFS\_LG} \cdot R_{142} = 124\text{mV}}\end{gathered} \quad \textbf{(35)}$$

3.4 AWG Out

IC16 in

F A G AD

- FE A
- Stable for gains for High C L
- H H d G
-
- Low noise nV H fA H
- L
-
- L FD B MH
- L A

- L O

M IC

$$\frac{\mathbf{1}}{\mathbf{R_{140}}}+\frac{\mathbf{1}}{\mathbf{R_{141}}}+\frac{\mathbf{1}}{\mathbf{R_{144}}}=\frac{\mathbf{1}}{\mathbf{R_{147}}}+\frac{\mathbf{1}}{\mathbf{R_{149}}} \quad \textbf{(36)}$$

$$\boldsymbol{V_{outAWG}} = -\boldsymbol{V_{Audio}} \cdot \frac{\mathbf{R_{141}}}{\mathbf{R_{144}}} + \left(\mathbf{2} \cdot \boldsymbol{V_{offAWG}} - \boldsymbol{V_{ref1V2AWG}}\right) \cdot \frac{\mathbf{R_{141}}}{\mathbf{R_{140}}} \quad \textbf{(37)}$$

(37)

$$-5.45V < -\mathbf{5V} < V_{ACoutAWG\_HG} < \mathbf{5V} < 5.45V$$
$$-1.36V < \mathbf{1.25V} < V_{ACoutAWG\_LG} < \mathbf{1.25V} < 1.36V \quad \textbf{(38)}$$

L A
L G H G

(37) DC A G L G
H G

$$-5.5V < \mathbf{5V} < V_{DCoutAWG} < \mathbf{5V} < 5.5V \quad \textbf{(39)}$$

AD $\pm 5.5V$ AC DC **(37)**

$$-5.5V < \mathbf{5V} < V_{outAWG} < \mathbf{5V} < 5.5V \quad \textbf{(40)}$$

O **bolded** **(38) (39)** **(40)**

P C

3.5 Audio

A A G F AD

-
- H A
- L A
- Low supply current A Amp
-

A

$$\boldsymbol{V_{outIC18}} = -\mathbf{2} \cdot \boldsymbol{V_{Audio}} + \mathbf{1.5V} \quad \textbf{(41)}$$

(41) DC

AC

$$V_{AudioJack} = -2 \cdot V_{Audio}$$

$$-992mV < V_{AudioJack} < 992mV \ (High\ Gain)$$

$$-248mV < V_{AudioJack} < 248mV \ (Low\ Gain)$$ (42)

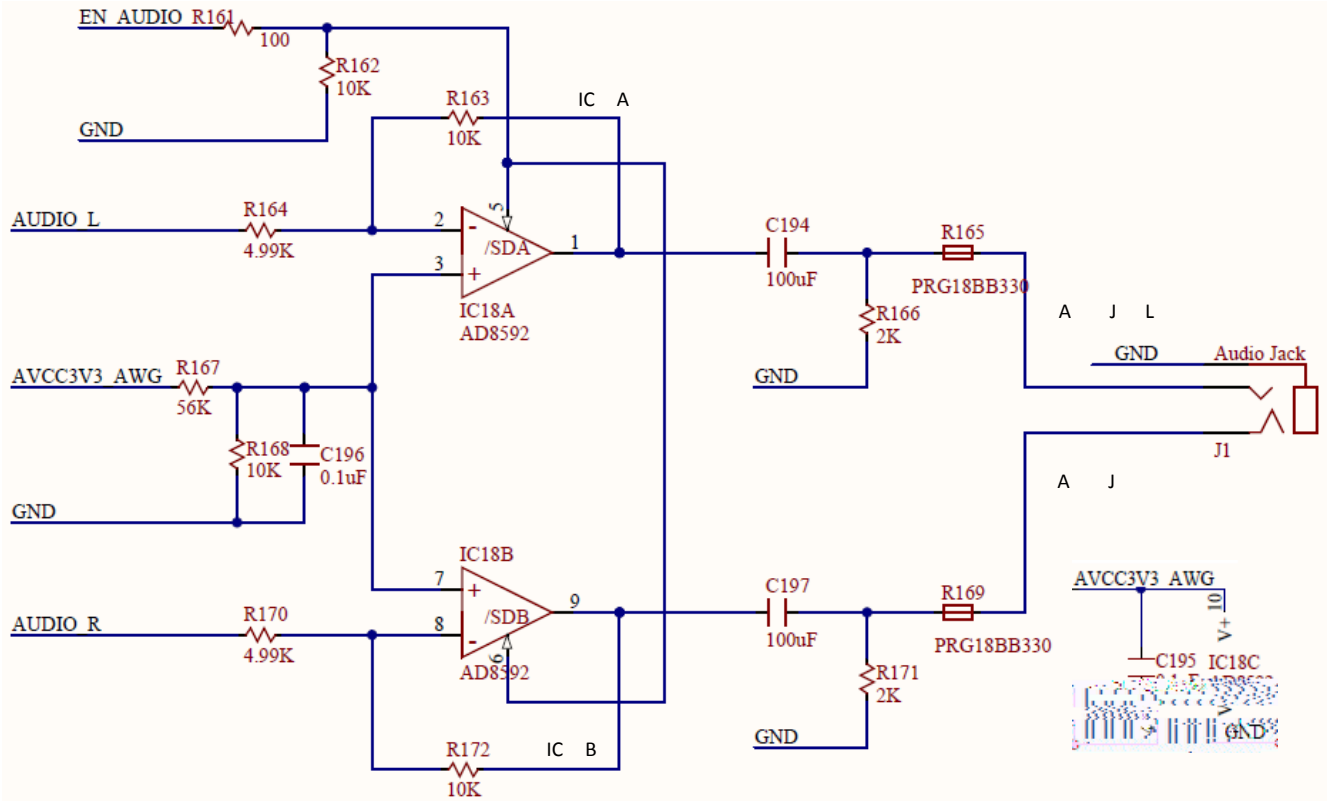

Figure 20. Audio.

3.6 AWG Spectral Characteristics

F A G I

D D BNC A G F

A G A D

A D

A G

N A F

I A G

H MH B

MH MH

A G MH

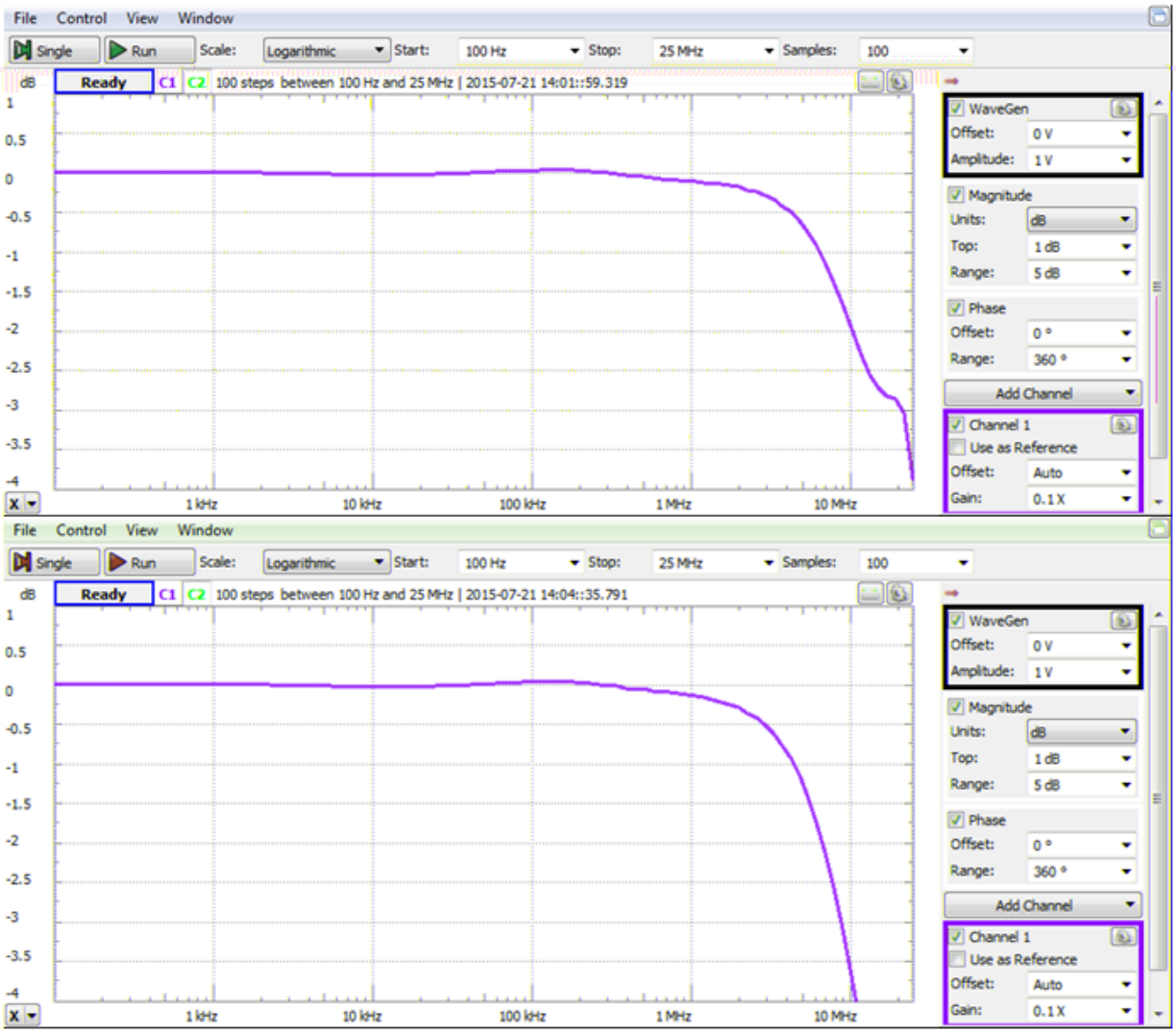

Figure 21. AWG spectral characteristic.

4 Calibration Memory

C DC AC

CMM A D

-
- C I D G

- N
-
-

A A G
A
DC G O C C
C M A D F C F
C D
F C

F A D

5 Digital I/O

F D I O J A D

G FPGA I O A D D I O FPGA LO
A

P C D FPGA E D
N P C
and parasitical capacitance of the Schottky diodes pF and FPGA pins pF limit the bandwidth of the
F P C

I L CMO I O

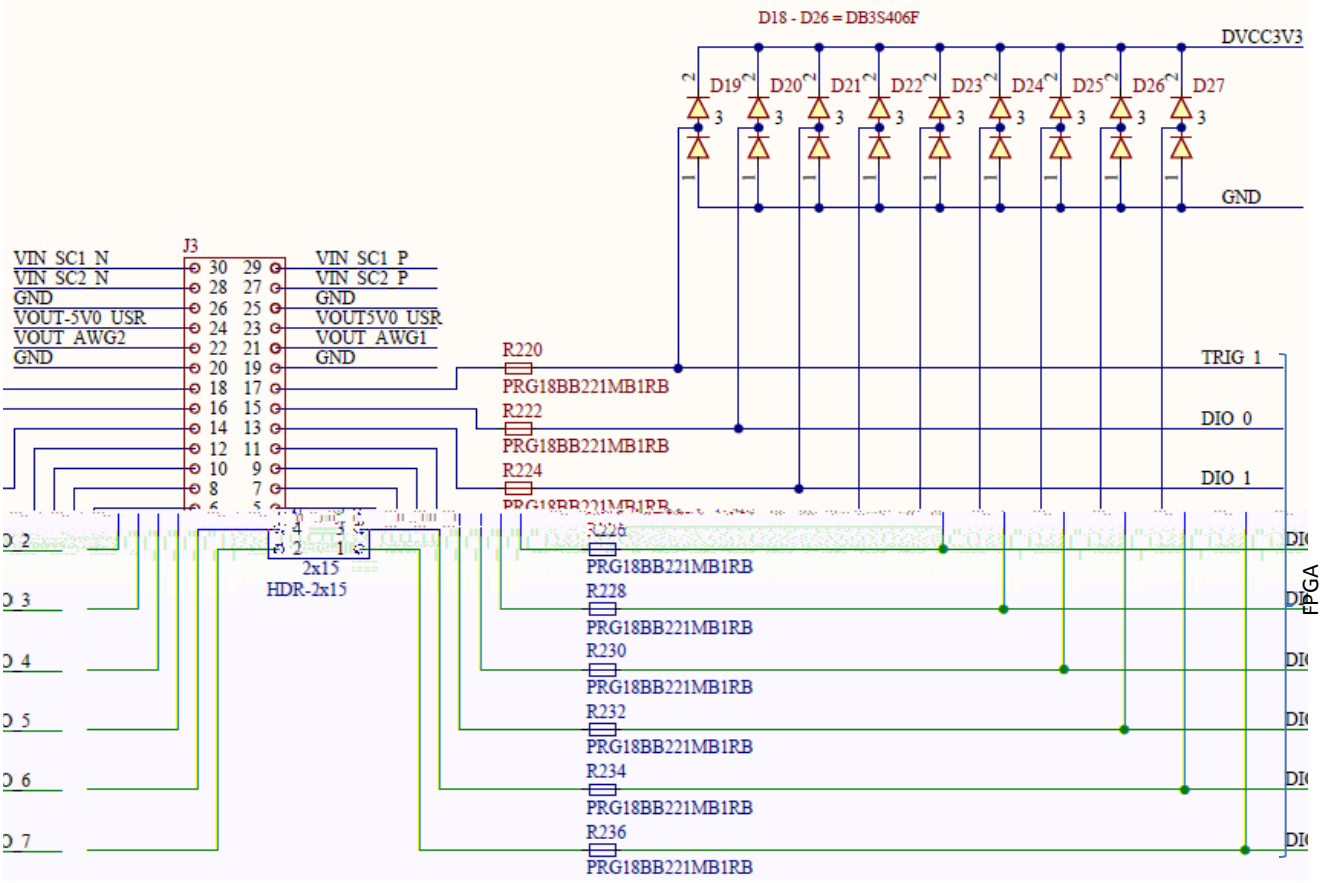

Figure 22. Digital I/O.

6 Power Supplies and Control

6.1 USB Power Control

A F A D B B

J

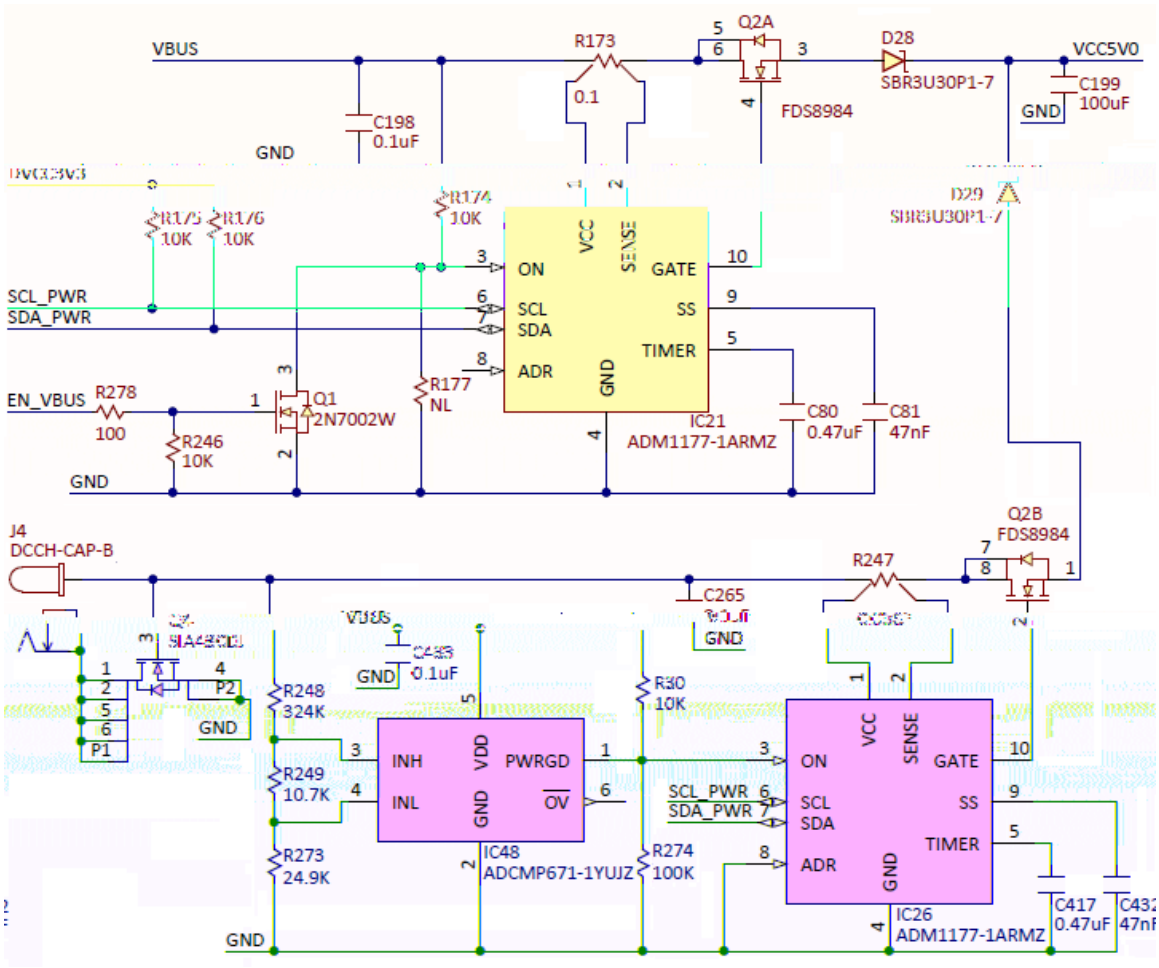

Figure 23. USB power control.

Q OFF

J H

- A D B PC GND EA H
- E J
  EA H

I EA H Q

ADCMP

- I O
- I N N I O
- DD C
-
- Low quiescent current A maximum
- I
- I
- L A
- O
- P
- D

- L O

IC P GD HIGH IC ON

$$\mathbf{4.11V = 400mV \cdot \frac{R_{248} + R_{249} + R_{273}}{R_{249} + R_{273}}} < V_{ext} < 400\mathbf{mV \cdot \frac{R_{248} + R_{249} + R_{273}}{R_{273}} = 5.76V} \quad \textbf{(43)}$$

A D **USB** **External** **Racing OFF** **USB OFF** **Racing**

- **Racing OFF** FPGA P GD HIGH
- **USB OFF** FPGA P GD LO
- **USB** IC ON IC OFF
- **Racing** P GD HIGH F B P C D B P C IC E P IC ON D D FPGA F D **Racing**
- **External** DC IC **(43)** P GD HIGH F B P C IC A B B B IC

A P ON FPGA EN B H Q OFF IC ON A D **USB OFF** P GD LO **Racing OFF** P GD HIGH F FPGA **USB** **Racing** FPGA DC **Racing** P GD HIGH F EN B HIGH B P C IC OFF **External**

I P F **USB** **Racing** **External**

H **External** O B B FPGA EN B H **USB OFF** F FPGA A **USB**

A ADM H C D P M P B **USB** **Racing** IC F

ADM

-

-
- P
- ADC
- A
-
- F
- A
- P IME
-
- I C H

USB Racing IC B

$$I_{limit} = \frac{100mV}{R_{173}} = \frac{100mV}{0.1\Omega} = 1A \quad (44)$$

F

$$t_{fault} = 21.7[ms/\mu F] \cdot C_{80} = 21.7[ms/\mu F] \cdot 0.47\mu F = 10.2ms \quad (45)$$

I I_{limit} t_{fault} IC Q A A

$$t_{cool} = 550[ms/\mu F] \cdot C_{80} = 550\left[\frac{ms}{\mu F}\right] \cdot 0.47\mu F = 258.5ms \quad (46)$$

$$\frac{dI_{limit}}{dt} = \frac{10\mu A}{C_{81}} \cdot \frac{1}{10 \cdot R_{173}} = 212\frac{mA}{ms} \quad (47)$$

I I_{limit} t_{fault}

IC **Racing External**

$$I_{limit} = \frac{100mV}{R_{247}} = \frac{100mV}{0.036\Omega} = 2.78A \quad (48)$$

t_{fault} t_{cool} IC

$$\frac{dI_{limit}}{dt} = \frac{10\mu A}{C_{432}} \cdot \frac{1}{10 \cdot R_{247}} = 591\frac{mA}{ms} \quad (49)$$

A D O E D

C

I

E B B
D F PC B

6.2 Analog Supply Control

D **USB** FPGA IC O
M D A A OC O
C I A O
M D O F IC ADP F
IC F

ADP

- Low RDSon of m
- L
-
- O
-
LC P

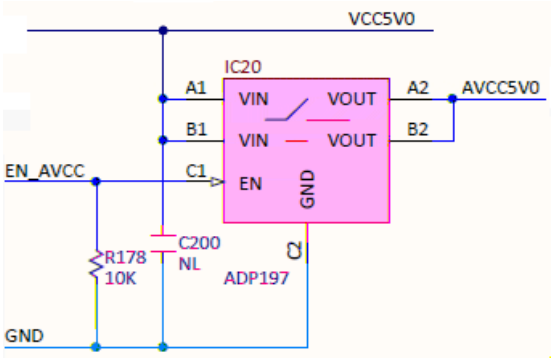

Figure 1. Analog supply control.

6.3 User Supply Control

IC F ADM

- C
- G
- G P FE
- I
- A
- F
- A
- P OA
- P
- A O
- LFC P
- Q OP

IC F
FPGA

D **USB** **Racing** E ILIM LO FPGA I E IC

$$V_{Iset} = \frac{\frac{V_{cap}}{R_{253}}}{\frac{1}{R_{253}} + \frac{1}{R_{254}} + \frac{1}{R_{255}}} = \frac{\frac{3.6V}{10k\Omega}}{\frac{1}{10k\Omega} + \frac{1}{1.74k\Omega} + \frac{1}{22.6k\Omega}} = 0.5V \quad (50)$$

$$I_{limit} = \frac{V_{Iset}}{40 \cdot R_{21}} = \frac{0.5V}{40 \cdot 0.043\Omega} = 290mA \quad (51)$$

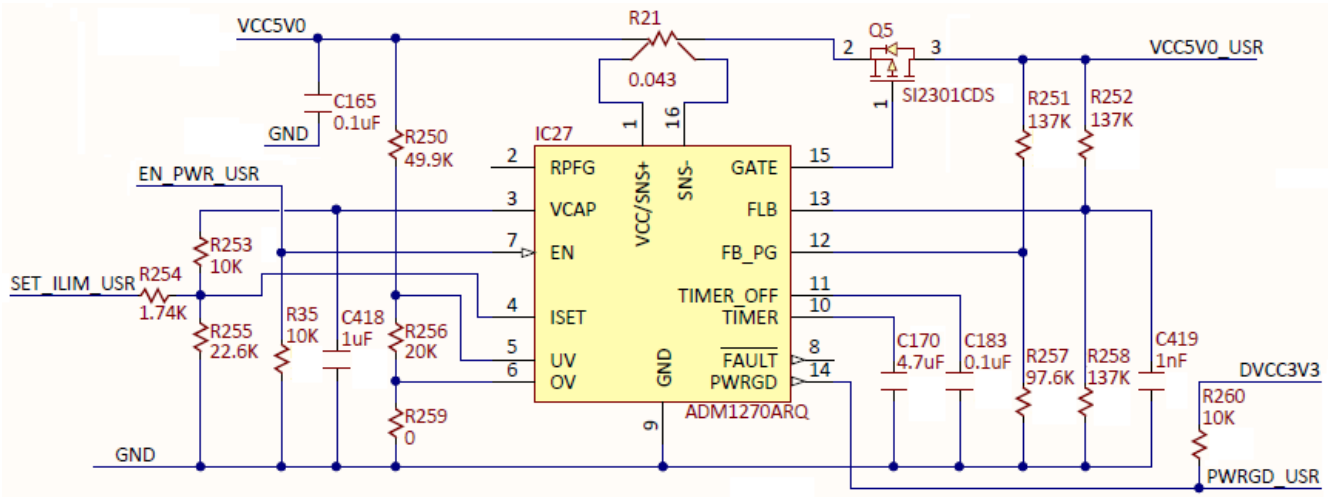

Figure 25. User supplies control.

D **External** **OFF** E ILIM H FPGA I E IC

$$V_{Iset} = \frac{V_{cap} \cdot R_{255}}{R_{253} + R_{255}} = \frac{3.6V \cdot 22.6k\Omega}{10k\Omega + 22.6k\Omega} = 2.5V \quad (52)$$

$$I_{limit} = \frac{V_{Iset}}{40 \cdot R_{21}} = \frac{2.5V}{40 \cdot 0.043\Omega} = 1.45A \quad (53)$$

I I_{limit}

$$t_{fault} = 21.7[ms/\mu F] \cdot C_{170} = 21.7[ms/\mu F] \cdot 4.7\mu F = 102ms \quad (54)$$

I I_{limit} t_{fault} IC Q A

$$t_{cool} = 550[ms/\mu F] \cdot C_{80} = 550[ms/\mu F] \cdot 4.7\mu F = 2.585s \quad (55)$$

C N L

I I_{limit} t_{fault}

(51) **(53)** A

A

USB Only I **External**

6.4 User Voltage Supplies

F ADP C B B DC DC M

- A
- M
- P H MH P M
- A
- A
-

IC A B E E
A IC B

$$V_{+IC46A} = \frac{\frac{V_{OUT+\_USR}}{R_{188}} + \frac{V_{SET+\_USR}}{R_{193}}}{\frac{1}{R_{188}} + \frac{1}{R_{193}}} = V_{-IC46A} = \frac{\frac{V_{FB}}{R_{266}}}{\frac{1}{R_{265}} + \frac{1}{R_{266}}} \quad (56)$$

$$V_{+IC46B} = \frac{\frac{V_{OUT-\_USR}}{R_{187}} + \frac{V_{FB}}{R_{270}}}{\frac{1}{R_{187}} + \frac{1}{R_{270}}} = V_{-IC46B} = \frac{\frac{V_{SET-\_USR}}{R_{190}}}{\frac{1}{R_{72}} + \frac{1}{R_{190}}} \quad (57)$$

$$\frac{1}{R_{188}} + \frac{1}{R_{193}} = \frac{1}{R_{265}} + \frac{1}{R_{266}} \quad (58)$$

$$\frac{1}{R_{187}} + \frac{1}{R_{270}} = \frac{1}{R_{72}} + \frac{1}{R_{190}} \quad (59)$$

$$V_{OUT+\_USR} = V_{FB} \cdot \frac{R_{188}}{R_{266}} - V_{SET+_{USR}} \cdot \frac{R_{188}}{R_{193}} = 5.33V - 4.87 \cdot V_{SET+\_USR} \quad (60)$$

$$V_{OUT-\_USR} = -V_{FB} \cdot \frac{R_{187}}{R_{270}} + V_{SET-\_USR} \cdot \frac{R_{187}}{R_{190}} = -5.33V + 4.87 \cdot V_{SET-\_USR} \quad (61)$$

$$V_{FB} = 1.235V\ typical \quad (62)$$

IC F

$$0 < V_{SET+\_USR}, V_{SET-\_USR} < 1.2V \quad (63)$$

$$-0.51V \leq V_{OUT+USR} < 5.33V \quad (64)$$
$$0.51V \geq V_{OUT+USR} > -5.33V \quad (65)$$

mponents tolerances After calibration the WaveForms SW only allows

E

E FPGA

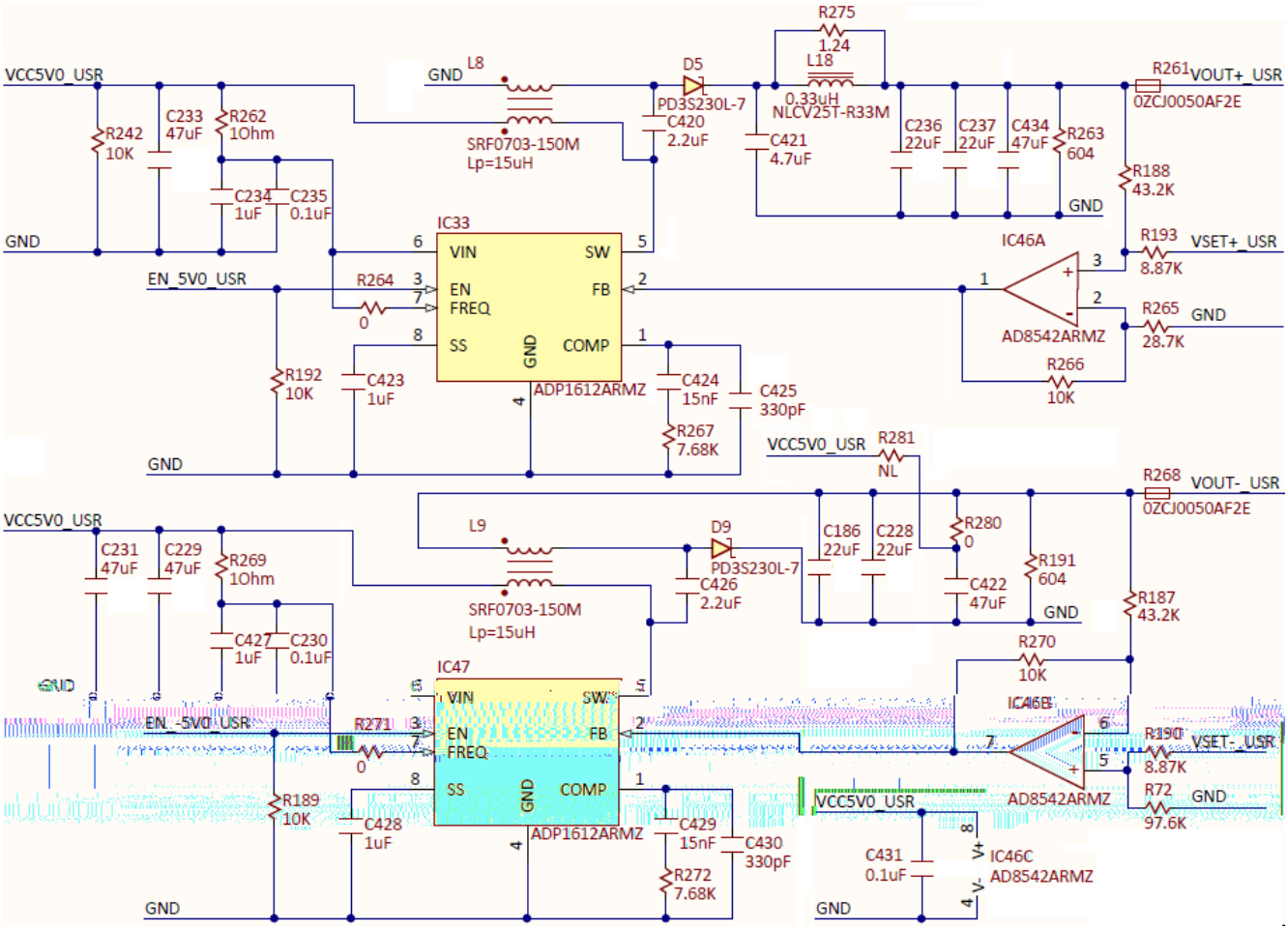

Figure 26. User power supplies.

6.5 Internal Power Supplies

6.5.1 Analog Supplies

A F

F F ADP F

O A MH D DC DC LC

P M

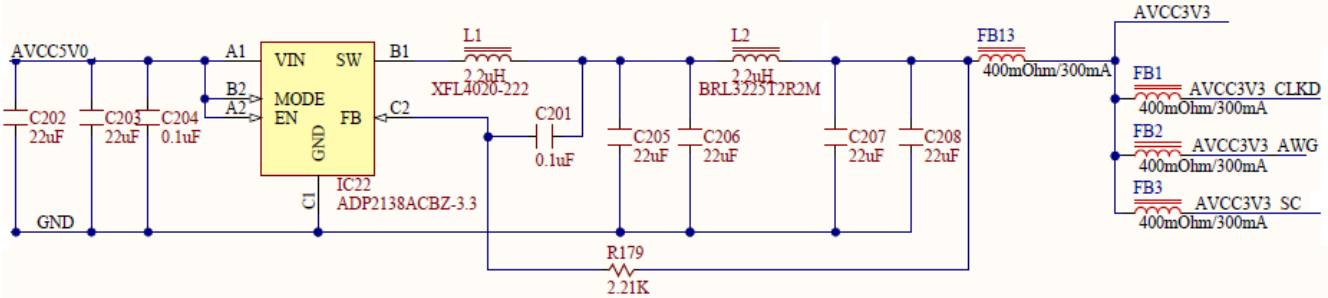

Figure 27. 3.3V internal analog power supply.

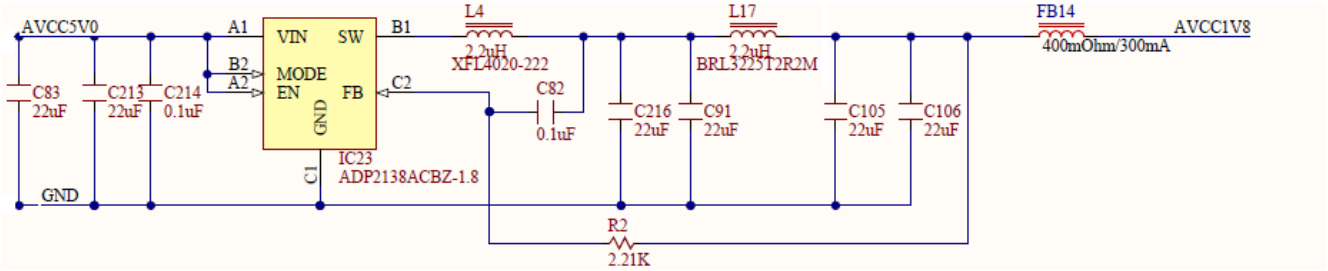

Figure 28. 1.8V internal analog power supply.

- I
- P
- MH
- LC P
- F
-
- I
- C
- F P M P M P M

F ADP D
B B N AN D I B B ADP
ADP ADP

- A
-
- MH
- H
- C
- O IN
- A PFM P M
- I MO FE
- I
- LO O OCP D
- A O

O FB

$$\frac{R_{180}}{R_{181}} = \frac{-V_{out} - V_{ref}}{V_{ref}} \quad (66)$$

C $R_{181} = 10.2k\Omega$

$$R_{180} = \frac{3.3V - 0.8V}{0.8V} \cdot 10.2k\Omega = 31.87k\Omega \quad (67)$$

C $R_{180} = 31.6k\Omega$

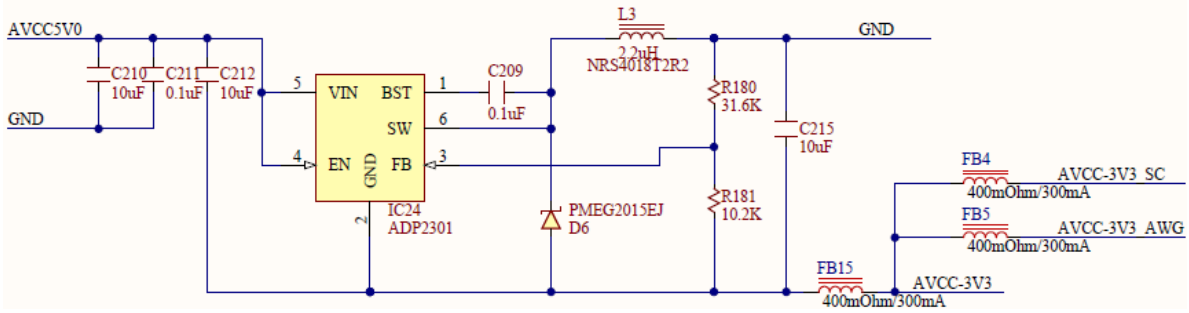

Figure 29. 3.3V internal analog power supply.

F C ADP

DC DC B C

O

F AN A I C

I

O

$$\frac{R_{184}}{R_{185}} = \frac{V_{out} - V_{ref}}{V_{ref}} \quad (68)$$

C $R_{185} = 13.7k\Omega$

$$R_{184} = \frac{5.5V - 1.235V}{1.235V} \cdot 13.7k\Omega = 47.31k\Omega \quad (69)$$

C $R_{184} = 47.5k\Omega$

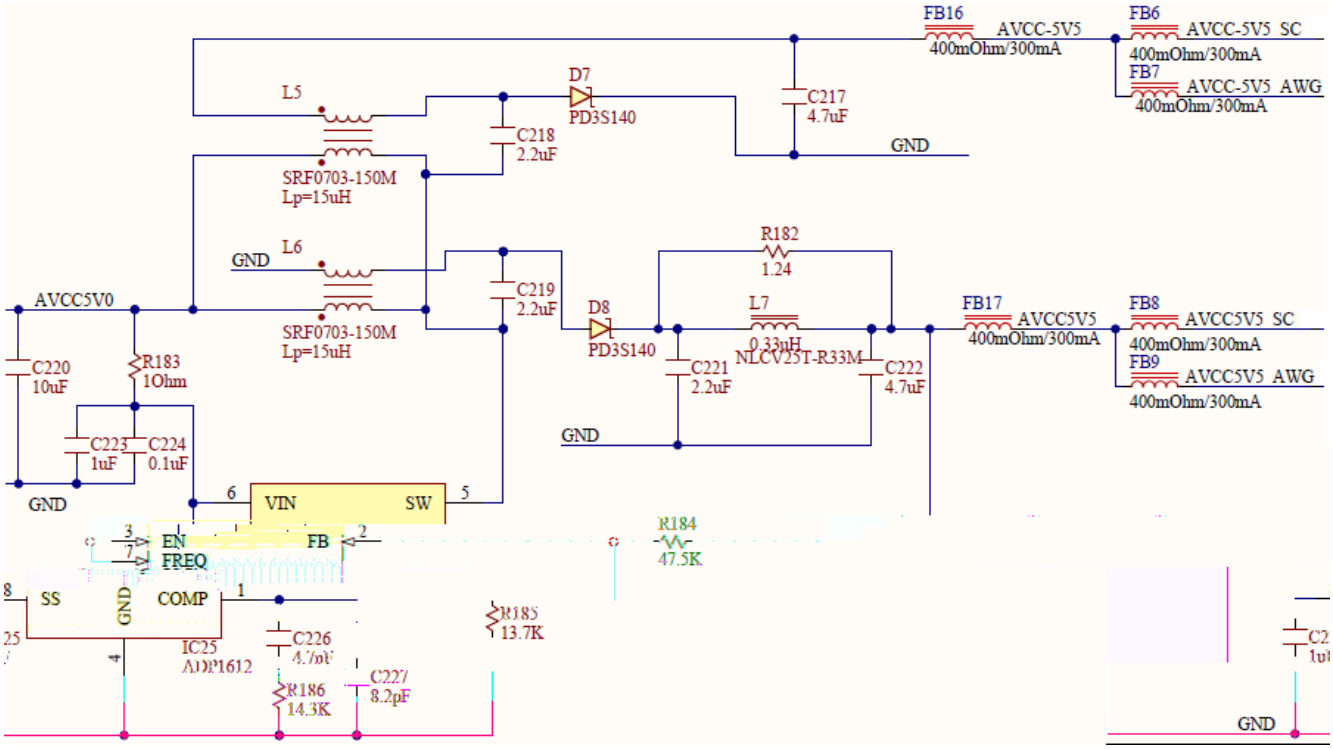

Figure 31. ±5.5V internal analog supplies.

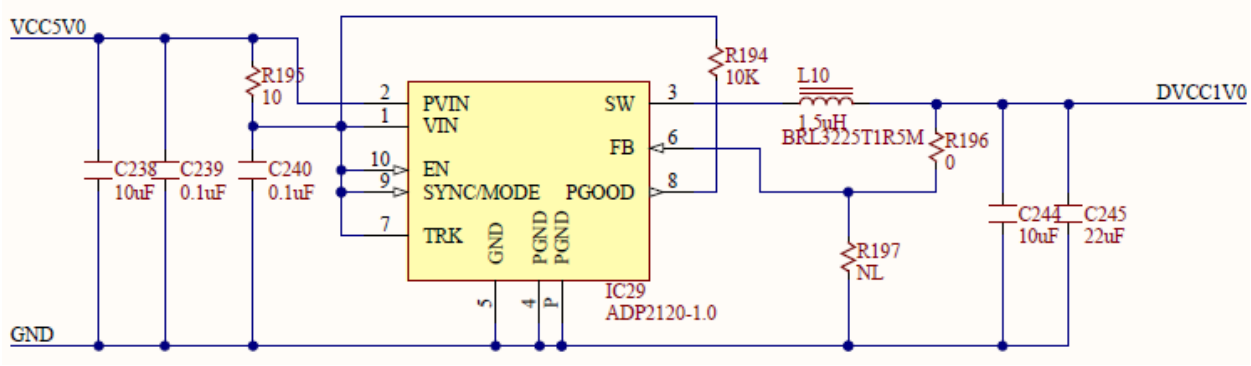

Figure 32. 1V internal digital supply.

6.5.2 Digital Supplies

F ADP I
FPGA I

- A
- m and m integrated OSFETs
- I IN
- MH P M PFM
- C
- I I
- LO O P OCP
- LFC P D

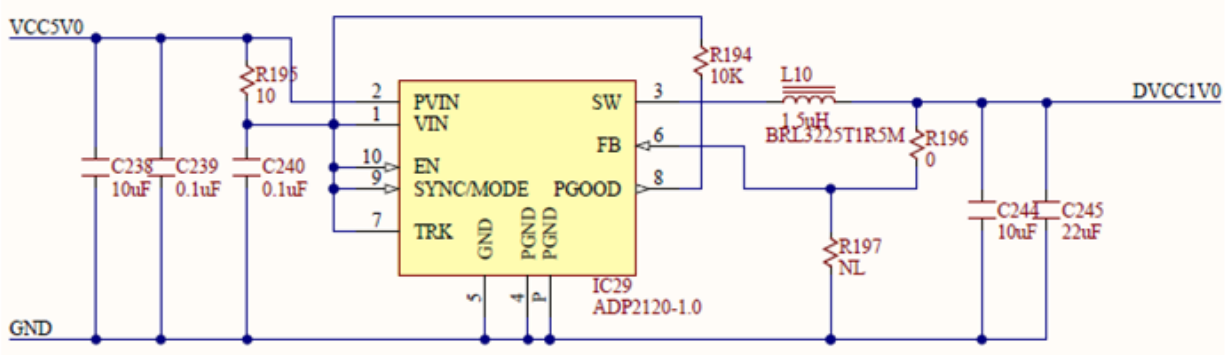

Figure 31. 1V internal digital supply.

F ADP A MH B B DC DC C

-
- A typical quiescent current
- H operation enables H inductor
- I
- F
- F
- I
-
- E
- O
-
-
-
-
- C PCB

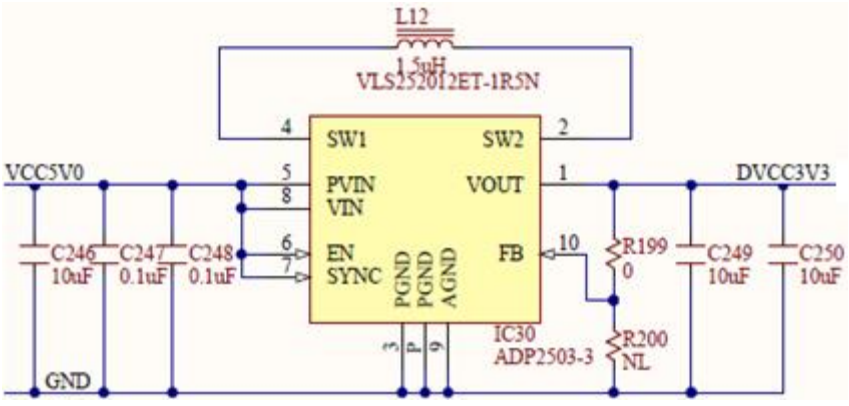

Figure 32. 3.3V internal digital supply.

I

F ADP F O A MH
D DC DC MH
LC P

ADP

- I
- P
- Typical quiescent current A
- F
-
- I
- C
- Ultralow shutdown current A typical
- F P M P M P M

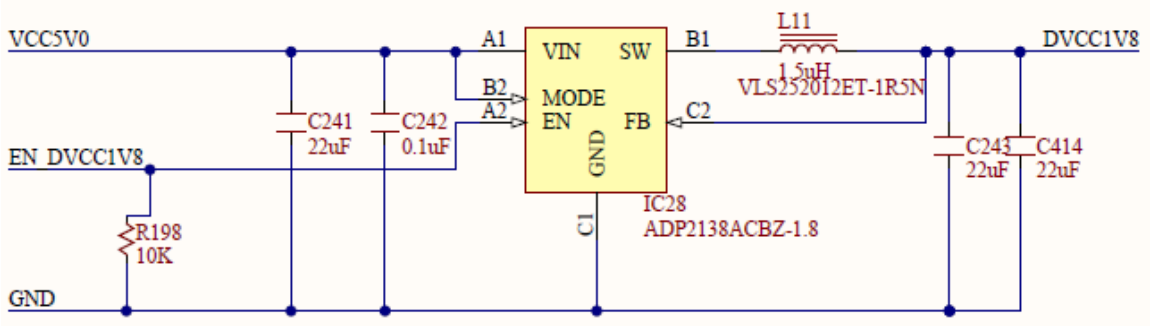

Figure 33. 1.8V internal digital supply.

6.6 Temperature Measurement

A D AD D O
F AD

- Temperature range to
- C C
- MB I C
- Temperature conversion time s typical
- O
- P A

Figure 2. Temperature measurement.

7 USB Controller

B

- **Programming the FPGA** FPGA A D
  F
  D B J AG A
- **Data exchange** A
  D B MB B
  PC

8 FPGA

A D FPGA C L L

- C MH MH B MH
- A D L A
- A AM FM A G
- D
-
- P
- P
- C
- C PC

B D AM FPGA M
F AM

A F E
E

- MH
- E
- E AM FM
- F
  E
- C A L A P G

9.3 Logic Analyzer

- I O
- M P K
- L CMO
- M
- C A L A P G
- I PI I C A P
- C

9.4 Digital Pattern Generator

- I O
- M P
- A
- C K
- D
- C

9.5 Digital I/O

- I O
- L CMO
- PC I O
- C

9.6 Power Supplies

- B
- A A A

9.7 Network Analyzer[xliv]

- MH
- I H MH
-
- A
- B N N

9.8 Voltmeters[xlviii]

- A
- A DC AC M M
-
-
- A

9.9 Spectrum Analyzer[li]

- P FF C
- F
- L
- P
- M B B
- C
- C FD N HD
- D

9.10 Other Features

- B
- H B
- G
-
- C
- H
- N MA LAB MA LAB
- I

L A P G D I O
D I O P G
CMO
L A P G D I O
D I O P G
CMO
L A P G D I O
D I O P G
CMO
CMO

N

H gain is used in the analog signal input path for rough scaling Digital Zooming is used for multiple sc

A D
A D BNC B
MH F
A F ADC H
P
D F D M F M
D M FPGA
D I O A G

F PC
F PC
A I O L A I O
F P G I O
P G I O I O
I O H
D L A F D M F M
D M FPGA
A G L A
D D N FPGA
A D
A D
D D N FPGA
A D
A D
D D N FPGA
A D
A D
F PC FPGA A
FPGA PC

F PC
A I O L A I O
F P G I O
P G I O I O
I O H
FPGA
D P G F D M F M
D M FPGA
A G P G
F PC
F PC
A I O L A I O F
P G I O
P G I O I O I O
H
F PC
F PC
N A F A O A G A I
H A G
A B N
A B
F PC
F PC
F PC
F A I H F
N A A
B B
F PC
F PC
A F A I H
F N A
B A B
F PC
F PC
F PC
F PC

F PC
F PC
F PC
F PC
D D N FPGA
A D
A D
D D N FPGA
A D
A D
F PC
F PC