AN4938
Application note

Getting started with STM32H7x3 hardware development

Introduction

This application note is intended for system designers who develop applications based on STM32H7x3 microcontroller line (STM32H743xx or STM32H753xx) and need an implementation overview of the following hardware features:

- Power supply
- Package selection
- Clock management
- Reset control
- Boot mode settings
- Debug management.

This document describes the minimum hardware resources required to develop an application based on an STM32H743xx or STM32H753xx microcontroller.

Reference documents

The following documents are available on *www.st.com*:

- *STM32H743xx data brief*
- *STM32H753xx data brief*
- *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers* application note (AN2867)
- *STM32 microcontroller system memory boot mode* application note (AN2606).

Contents

List of tables

List of figures

1 General information

This document applies to STM32H7x3 line Arm-based devices.

arm

2 Power supplies

2.1 Introduction

STM32H743/753xx devices require a 1.71 to 3.6 V operating voltage supply (V_{DD}), which can be reduced down to 1.62 V by using an external power supervisor and connecting PDR_ON pin to V_{SS} (refer to the datasheets for details).

The digital power can be supplied either by a internal linear voltage regulator or directly by an external supply voltage. This digital power voltage can be set dynamically at different values ranging from 0.7 to 1.2 V, the highest value allowing to achieve the maximum performance.

The real-time clock (RTC), the RTC backup registers, and the backup SRAM (BKP SRAM) can be powered from the V_{BAT} voltage (1.2 to 3.6 V) when the main V_{DD} supply is powered OFF.

2.1.1 Independent analog supply and reference voltage

To improve analog peripheral performance, the analog peripherals feature an independent power supply which can be separately filtered and shielded from noise on the PCB:

- The analog supply voltage input is available on a separate VDDA pin.
- An isolated supply ground connection is provided on the pin V_{SSA}.

To ensure a better accuracy of low-voltage inputs, the user can connect a separate external reference voltage on V_{REF+}. The voltage applied to V_{REF+} ranges from 1.8 V to V_{DDA}.

When available (depending on the package), V_{REF-} pin must be externally tied to V_{SSA}.

V_{DDA} minimum value (V_{DDA_MIN}) depends on the analog peripheral and on whether a reference voltage is provided or not:

- If no analog peripheral is used, V_{DDAmin} equals 0 V.
- When an ADC or a comparator is used, V_{DDA_MIN} equals 1.62 V.
- When a DAC is used, V_{DDA_MIN} equals 1.8V.
- When an OPAMP is used, V_{DDA_MIN} equals 2.0 V.
- When a reference voltage (VREFBUF_OUT) is provided by the device on V_{REF+} pin, V_{DDA_MIN} depends on the required level for this voltage.

2.1.2 USB transceiver independent power supply

There are different ways to supply the USB transceivers, depending on $V_{DD33USB}$ and $V_{DD50USB}$ availability:

- When the VDD50USB pin is available, this pin can be used to supply an internal regulator dedicated to USB transceivers. In this case, VDD50USB pin should receive a voltage ranging from 4.0 to 5.5 V, typically supplied from the VBUS line of the USB connector. The regulated power (3.0 to 3.6 V) is available on VDD33USB.

  In this configuration $V_{DD50USB}$ voltage can rise indifferently after or before V_{DD} power supply (see *Figure 3*).

  An external capacitor must be connected to VDD33USB.

- When the VDD33USB pin is available, this pin can be used to supply the internal transceiver. In this case, VDD33USB pin should receive a voltage ranging from 3.0 to 3.6 V. If VDD50USB is also available, it must be connected to VDD33USB. As an example, when the device is powered at 1.8 V, an independent 3.3 V power supply can be applied to VDD33USB.

  When VDD33USB is connected to a separate power supply, it is independent from V_{DD} and V_{DDA}. It must be the last supply applied and the first supply switched OFF. The following conditions must be respected (see *Figure 2*):

  – During the power-on and power-down phases (V_{DD} < V_{DD} minimum value), $V_{DD33USB}$ should always be lower than V_{DD}.

  – $V_{DD33USB}$ rising and falling time specifications must be respected (refer to table *power-up/power-down operating conditions (regulator ON)* and table *power-up/power-down operating conditions (regulator OFF)* provided in the device datasheets).

  – In operating mode, $V_{DD33USB}$ can be either lower or higher than V_{DD}:

    If a USB interface is used (USB OTG_HS/OTG_FS), the associated GPIOs powered by $V_{DD33USB}$ operate between $V_{DD33USB\_MIN}$ and $V_{DD33USB\_MAX}$(see *Figure 2*).

    $V_{DD33USB}$ supplies both USB OTG_HS and USB OTG_FS transceivers. If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by $V_{DD33USB}$.

    If no USB interface is used (USB OTG_HS/OTG_FS), the associated GPIOs powered by $V_{DD33USB}$ operate in V_{DD} range (between V_{DD_MIN} and V_{DD_MAX}).

    In the above two configurations, an external capacitor must be connected to VDD33USB.

- When neither VDD33USB nor VDD50USB is available, VDD pins are use to supply USB transceivers and must be in the range of 3.0 to 3.6 V for the transceiver to operate correctly.

Figure 1. VDD33USB connected to V_{DD} power supply

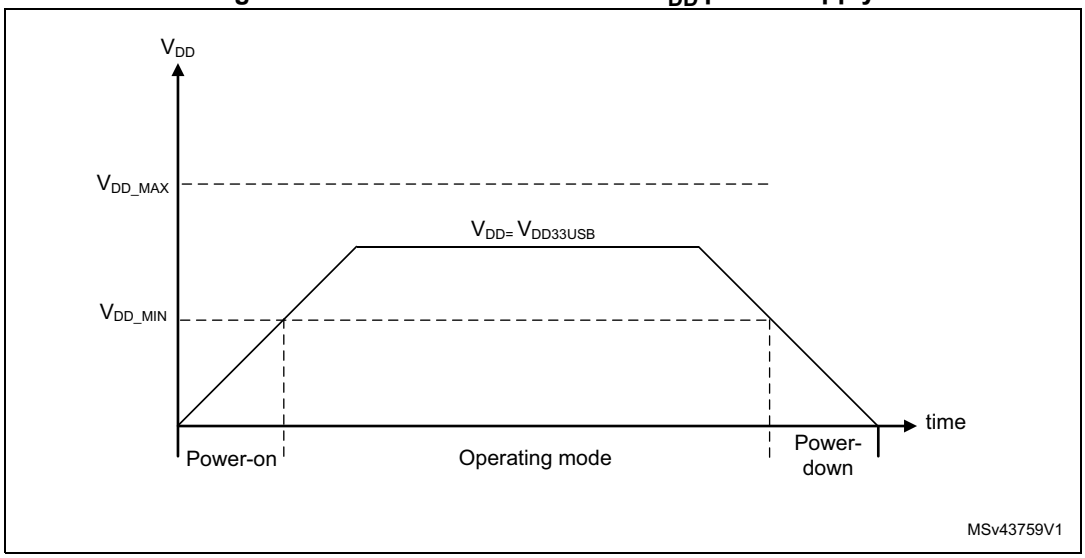


Figure 2. VDD33USB connected to external power supply

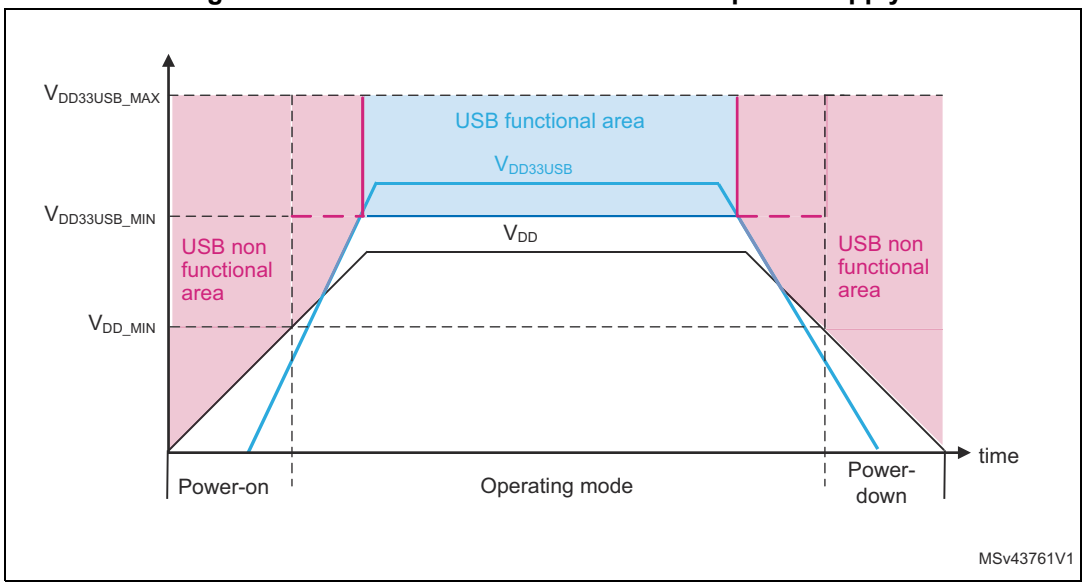
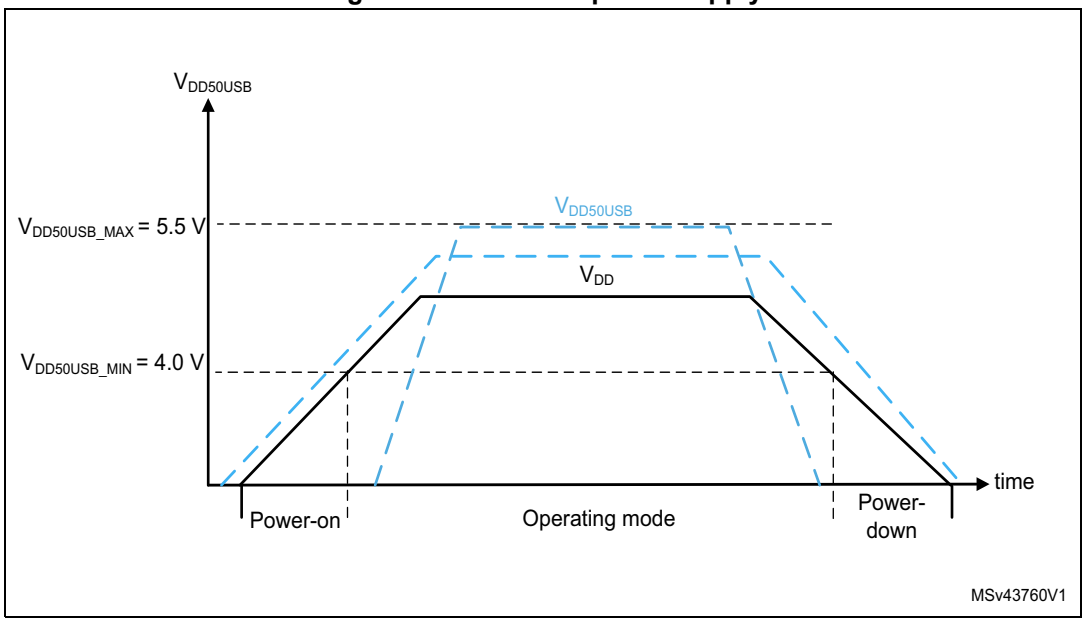


Figure 3. VDD50USB power supply



2.1.3 Battery backup domain

Backup domain description

To retain the content of the RTC backup registers, backup SRAM, and supply the RTC when V_{DD} is turned off, V_{BAT} pin can be connected to an optional 1.2-3.6 V standby voltage supplied by a battery. Otherwise, V_{BAT} must be connected to another source, such as V_{DD}.

When the backup domain is supplied by V_{BAT} (analog switch connected to V_{BAT} since V_{DD} is not present), the following functions are available:

- PC14 and PC15 can be used as LSE pins only.
- PC13 can be used as tamper pin (TAMP1).
- PI8 can be used as tamper pin (TAMP2).
- PC1 can be used as tamper pin (TAMP3).

During $t_{RSTTEMPO}$ (temporization at V_{DD} startup) or after a power-down reset (PDR) is detected, the power switch between V_{BAT} and V_{DD} remains connected to V_{BAT}.

During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ and it is higher than V_{BAT} + 0.6 V, a current may be injected into V_{BAT} pin through an internal diode connected between V_{DD} and the power switch (V_{BAT}). If the power supply/battery connected to the V_{BAT} pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the V_{BAT} pin.

Refer to the device datasheets for the actual value of $t_{RSTTEMPO}$.

Battery charging

When V_{DD} is present, the external battery connected to V_{BAT} can be charged through an internal resistance. This operation can be performed either through an internal 5 kΩ or 1.5 kΩ resistor. The resistor value can be configured by software.

Battery charging is automatically disabled in V_{BAT} mode.

2.1.4 LDO voltage regulator

The LDO voltage regulator is always enabled after reset with a default output level set to 1.0 V (VOS3). The LDO can operate in three different modes depending on the application operating modes:

- In Run mode, the regulator supplies full power to the core and the digital domain.
- In Stop mode, the regulator supplies low power to the core and to the digital domain, thus preserving the contents of the registers and SRAM.
- In Standby mode, the regulator is powered down. The contents of the registers and SRAM are lost except for those related to the standby circuitry and the backup domain.

In Run and Stop mode, the LDO voltage regulator can be dynamical scaled by software to different voltage levels: VOS1, VOS2, and VOS3, SVOS3, SVOS4 or SVOS5.

The LDO regulator requires a capacitor on VCAP pins.

2.2 Power supply scheme

Power supplies

- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, Flash memory and system analog blocks such as reset and PLL

  This power supply is provided externally through VDD pins. VDD pins must be connected to V_{DD} with external decoupling capacitors: one single tantalum or ceramic capacitor (of 4.7 µF minimum capacitance) for the package and a 100 nF ceramic capacitor for each VDD pin.

  When V_{DD} is lower than 1.71 V, an external reset controller is required.

Note: V_{DD} minimum value of 1.62 V is obtained when the internal reset controller is OFF (refer to Section 2.3.6: Internal reset OFF).

- V_{SSA}, V_{DDA} = 1.62 to 3.6 V: external analog power supplies for ADCs, DACs and OPAMPs.

  VDDA pin must be connected to two external decoupling capacitors (100 nF ceramic capacitors and a 1 µF tantalum or ceramic capacitor).

- $V_{DD33USB}$ and $V_{DD50USB}$: external power supplies for USB transceiver

  When VDD50USB is used to provide power, this pin must be connected to the USB connector VBUS line and to a 4.7 µF decoupling capacitor (C_{IN}). In addition, VDD33USB must be connected to a 1 µF capacitor and its maximum ESR should be 600 mΩ.

  When VDD33USB is used to power the USB transceiver (3.0 to 3.6 V), if the VDD50USB pin is available, it must connected to VDD33USB, which must be connected to two external decoupling capacitors (a 100 nF ceramic capacitor and a 1 µF tantalum or ceramic capacitor).

- V_{BAT} = 1.2 to 3.6 V: power supply for the RTC, the external 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

  The V_{BAT} pin can be connected to the external battery (1.2 V < V_{BAT} < 3.6 V). If no external battery is used, it is mandatory to connect this pin to an external power supply: as an example, V_{BAT} pin can be connected to V_{DD} through a 100 nF external ceramic decoupling capacitor.

- V_{REF+} external reference voltage for analog peripherals

  V_{REF+} pin can be connected to V_{DDA} external power supply. If a separate external reference voltage is applied to V_{REF+}, a 100 nF and a 1 µF capacitors must be connected on this pin. In all cases, V_{REF+} must be kept below V_{DDA}. V_{REF+} lower limit is 2 V when V_{DDA} is above 2 V and the ADC is used, otherwise it is 1.62 V.

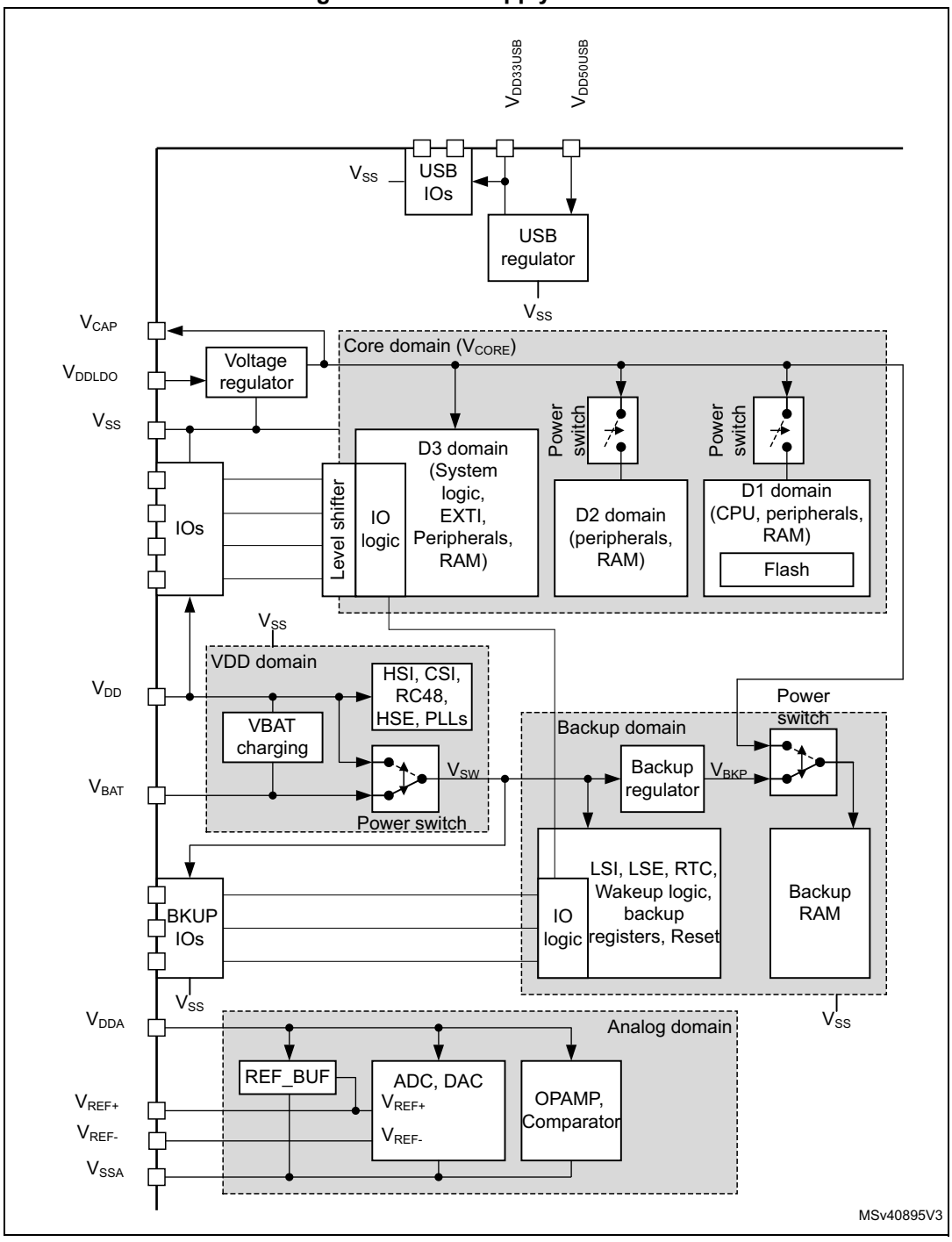
- V_{DDLDO} = 1.62 to 3.6 V: external power supply for voltage regulator

  When the LDO voltage regulator is enabled, VCAP1 and VCAP2 pins must be connected to two 2.2 µF ceramic capacitors with a low ESR (< 100 mΩ). If VCAP3 is available, it must be connected to the other VCAP pins but not additional capacitor is required. In addition, the VDDLDOx pins must be connected together and to a 4.7 µF tantalum or ceramic capacitor.

Additional precautions can be taken to filter analog noise:

- VDDA can be connected to V_{DD} through a ferrite bead.
- The VREF+ pin can be connected to V_{DDA} through a resistor (typically 47 Ω).

Figure 4. Power supply overview



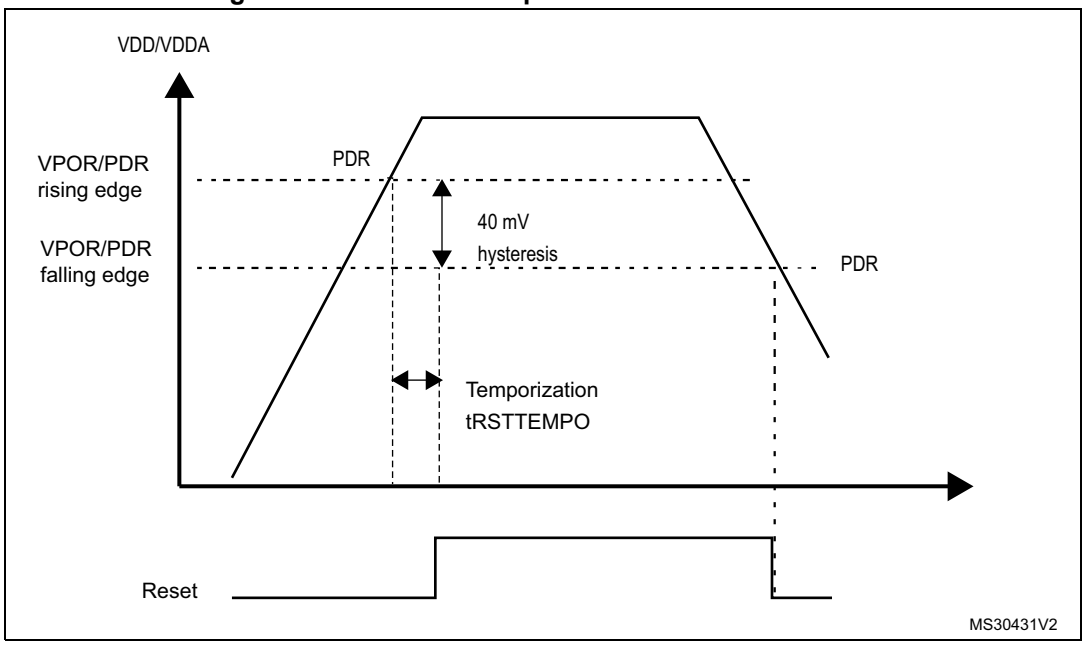
2.3 Reset and power supply supervisor

2.3.1 Power-on reset (POR)/power-down reset (PDR)

The devices have an integrated POR/PDR circuitry that allows a proper operation starting from 1.71 V.

The devices remain in reset mode when V_{DD} is below a specified threshold, VPOR/PDR, without the need for an external reset circuit. For more details concerning the power on/power-down reset threshold, refer to the electrical characteristics of the datasheet.

Figure 5. Power on reset/power down reset waveform



1. $t_{RSTTEMPO}$ is approximately 2.6 ms. VPOR/PDR rising edge is 1.66 V (typical) and VPOR/PDR falling edge is 1.62 V (typical). Refer to the device datasheets for the actual values.

On the packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

2.3.2 Programmable voltage detector (PVD)

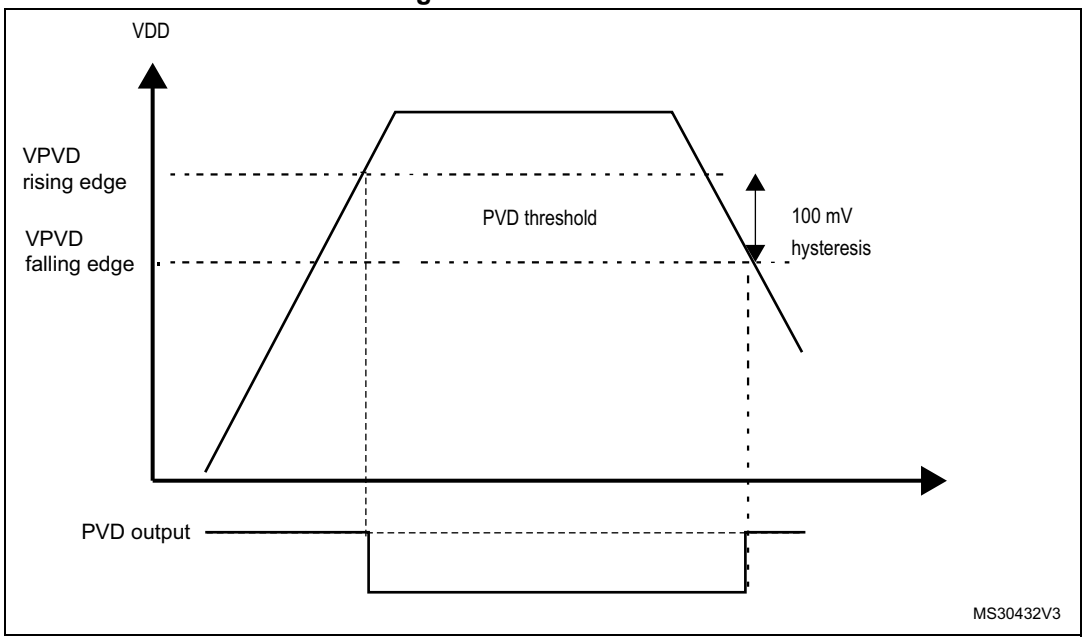
The PVD can be used to monitor the V_{DD} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the PWR power control register (PWR_CR1).

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the PWR power control/status register (PWR_CSR1), to indicate if V_{DD} is higher or lower than the PVD threshold. This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers.

The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example the service routine could perform emergency shutdown tasks.

Figure 6. PVD threshold



2.3.3 Analog voltage detector (AVD)

The AVD can be used to monitor V_{DDA} power supply by comparing it to a threshold selected through the ALS[1:0] bits of the PWR power control register (PWR_CR1). The threshold value can be configured to 1.7, 2.1, 2.5 or 2.8 V (refer to the devices datasheets for the actual values).

The AVD is enabled by setting the AVDEN bit in PWR_CR1 register. An interrupt can be raised when V_{DDA} goes above or below the configured threshold.

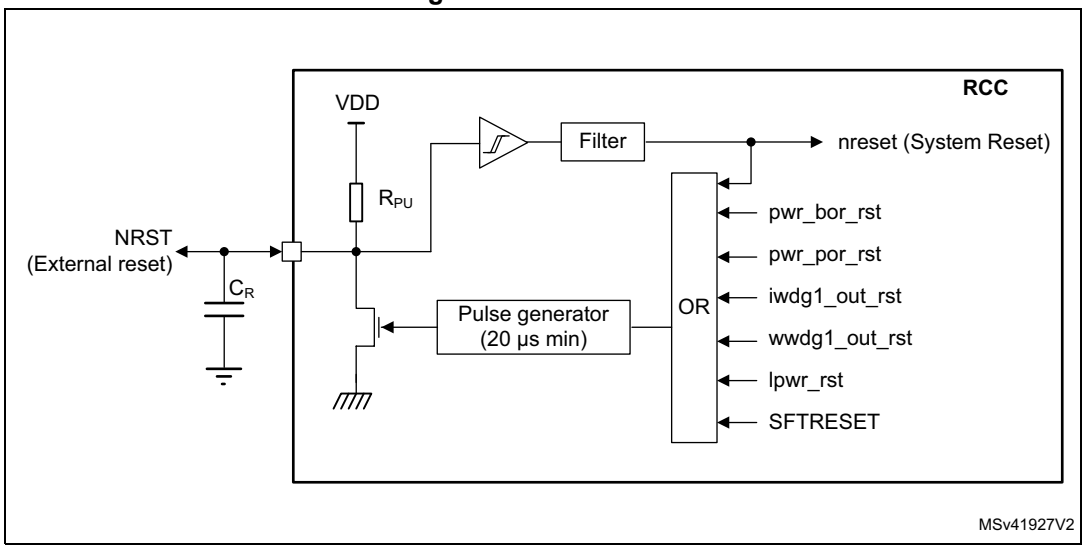
2.3.4 System reset

A system reset sets all the registers to their default values except the reset flags in the clock controller RCC_RSR register and the registers in the backup domain (see *Figure 7*).

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset).
2. Window watchdog end of count condition (WWDG reset).
3. Independent watchdog end of count condition (IWDG reset).
4. A software reset (Software reset).
5. A low-power management reset.

Figure 7. Reset circuit



2.3.5 Internal reset ON

On the packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

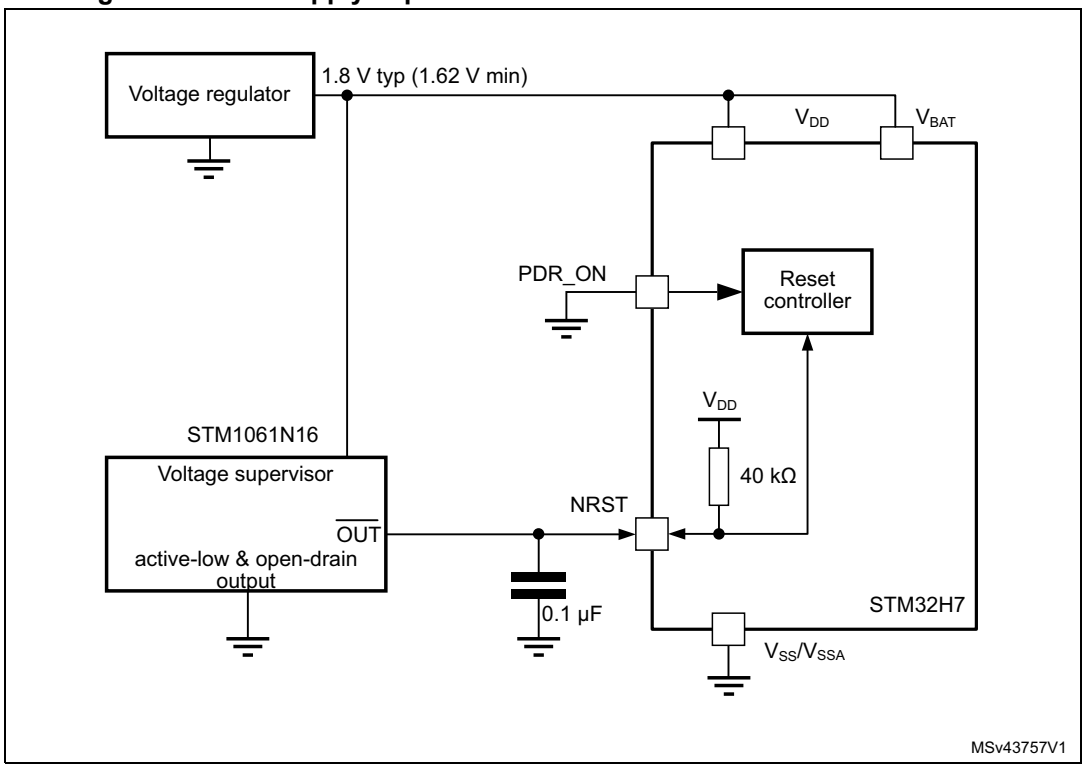
For more details about the internal reset ON, refer to the datasheets.

2.3.6 Internal reset OFF

This feature is available only on the packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to V_{SS}. Refer to *Figure 8: Power supply supervisor interconnection with internal reset OFF*.

Figure 8. Power supply supervisor interconnection with internal reset OFF



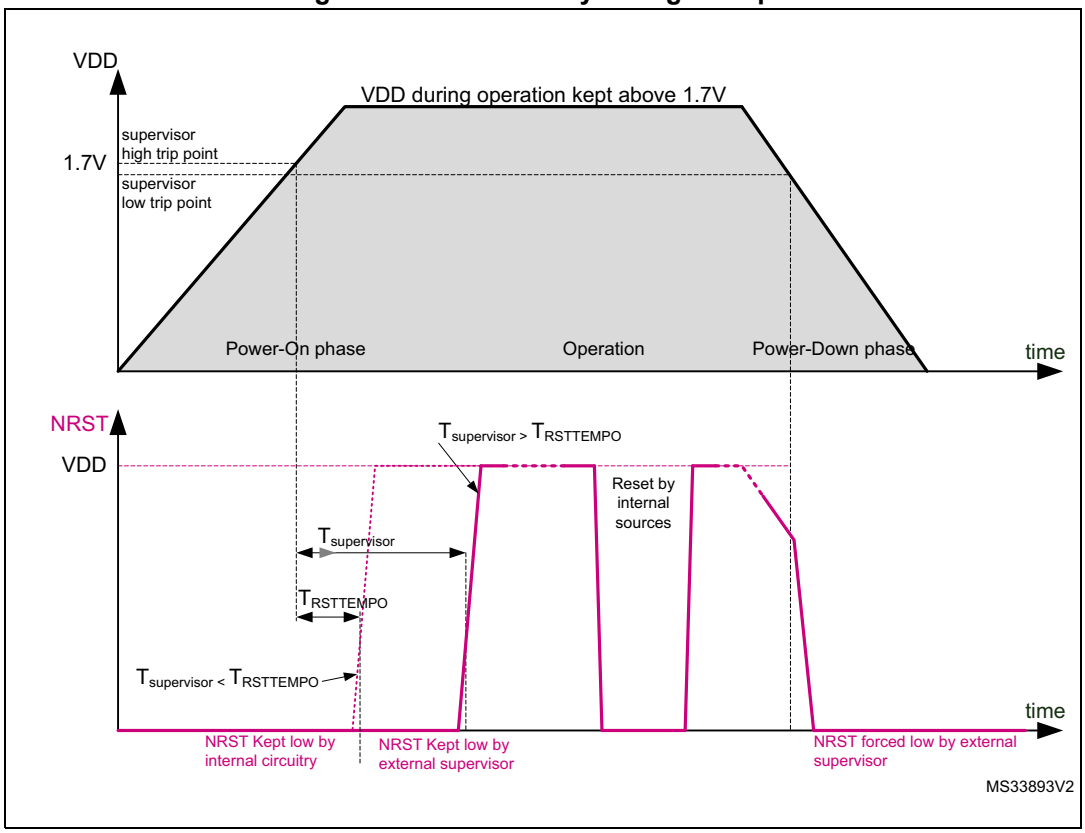
The supply ranges which never go below 1.71 V minimum should be better managed by the internal circuitry (no additional component needed, thanks to the fully embedded reset controller).

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All the packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal when connected to V_{SS}.

Figure 9. NRST circuitry timing example



2.3.7 Bypass mode

The power management unit can be bypassed. This feature can be configured by software. When bypassed, the core power supply should be provided through VCAPx pins connected together.

In Bypass mode, the internal voltage scaling is not managed internally, and the external voltage value (1.0 to 1.2 V) must be consistent with the targeted maximum frequency (see datasheet for the actual VOS level).

It can be lowered to 0.7 to 1.0 V in Stop mode (see datasheet for the actual SVOS level).

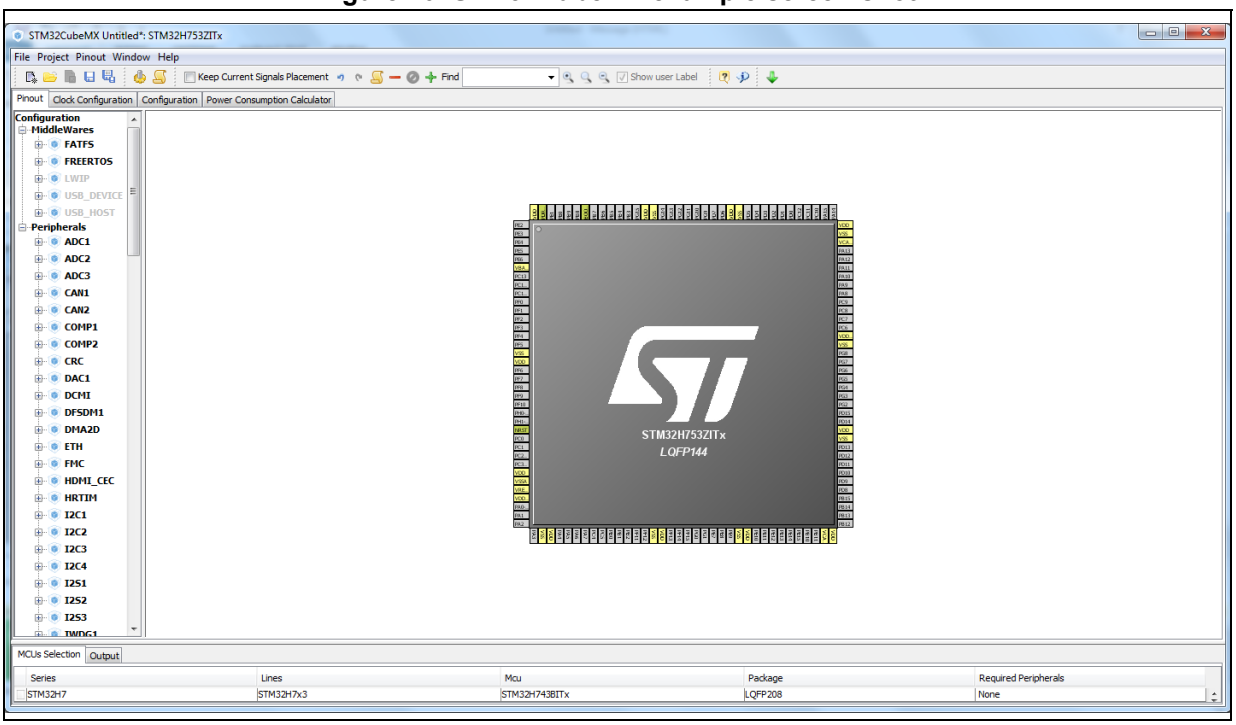
In Standby mode the external source will be switched off and the V_{CORE} domains powered down. The external source will be switched on when exiting Standby mode.

In Bypass mode, the external voltage must be present before or at the same time as V_{DD}. To avoid conflict with the LDO, the external voltage must be kept above 1.15 V until the LDO is disabled by software.

3 Alternate function mapping to pins

In order to easily explore the peripheral alternate functions mapping to the pins it is recommended to use the STM32CubeMX tool available on *http://www.st.com*.

Figure 10. STM32CubeMX example screen-shot



4 Clocks

Four different clock sources can be used to drive the system clock (SYSCLK):

- HSI oscillator clock
- CSI oscillator clock.
- HSE oscillator clock
- Main PLL (PLL) clock

The devices have the two following secondary clock sources:

- 32 kHz low-speed internal RC (LSI RC) which drives the independent watchdog and, optionally, the RTC used for Auto-wakeup from the Stop/Standby mode.
- 32.768 kHz low-speed external crystal (LSE crystal) which optionally drives the RTC clock (RTCCLK).

Each clock source can be switched ON or OFF independently when it is not used, to optimize power consumption.

Refer to device reference manual for a detailed description of the clock tree. In particular, a complete view of clock usage by peripheral is provided in the Kernel clock distribution overview.

4.1 HSE oscillator clock

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external user clock (see *Figure 11*).
- HSE external crystal/ceramic resonator (see *Figure 12*).

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize the output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected resonator.

Figure 11. HSE external clock

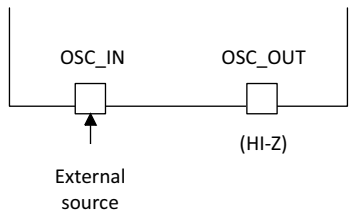
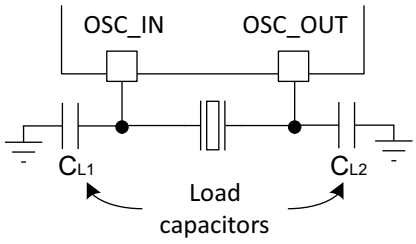


Figure 12. HSE crystal/ceramic resonators



4.1.1 External user clock (HSE bypass)

In this mode, an external clock source must be provided. The user selects this mode by setting the HSEBYP and HSEON bits in the RCC clock control register (RCC_CR). The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC_IN pin while the OSC_OUT pin should be left HI-Z.

4.1.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from 4 to 48 MHz. The external oscillator has the advantage of producing a very accurate main clock. The associated hardware configuration is shown in *Figure 12*. Using a 25 MHz oscillator frequency is a good choice to get accurate Ethernet, USB OTG high-speed peripheral, I2S and SAI.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize the output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. CL1 and CL2, are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of CL1 and CL2. The PCB and MCU pin capacitances must be included when sizing CL1 and CL2 (10 pF can be used as a rough estimate of the combined pin and board capacitance).

The HSERDY flag in the RCC clock control register (RCC_CR) indicates if the high-speed external oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIR).

If it is not used as clock source, the HSE crystal can be switched ON and OFF using the HSEON bit in the RCC clock control register (RCC_CR).

4.2 LSE oscillator clock

The low-speed external clock signal (LSE) can be generated from two possible clock sources:

- LSE user external clock (see *Figure 13*).
- LSE external crystal/ceramic resonator (see *Figure 14*).

Figure 13. LSE external clock

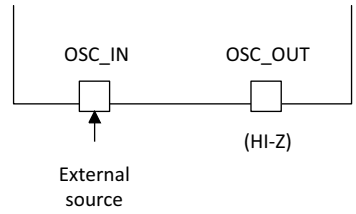
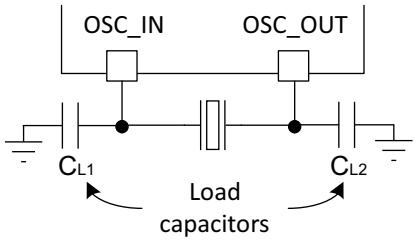


Figure 14. LSE crystal/ceramic resonators



1. *Figure 14: LSE crystal/ceramic resonators*:
To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤ 7 pF.
2. *Figure 13: LSE external clock* and *Figure 14: LSE crystal/ceramic resonators*:
OSC32_IN and OSC32_OUT pins can be used also as GPIO, but it is recommended not to use them as both RTC and GPIO pins in the same application.

The LSE oscillator is switched ON and OFF using the LSEON bit in RCC backup domain control register (RCC_BDCR).

The LSE oscillator includes new modes and has a configurable drive using the LSEDRV [1:0] in RCC_BDCR register:

- 00: Low drive.
- 10: Medium low drive.
- 01: Medium high drive.
- 11: High drive.

The LSERDY flag in the RCC backup domain control register (RCC_BDCR) indicates if the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIR).

4.2.1 External clock (LSE bypass)

The LSE bypass mode is available in all system power modes except for Standby and V_{BAT}. An external clock source must be provided in LSE bypass mode. It must have a frequency up to 1 MHz. The user selects this mode by setting the LSEBYP and LSEON bits in the RCC backup domain control register (RCC_BDCR). The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin should be left HI-Z. See *Figure 13*.

4.2.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize the output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

4.3 Clock security system (CSS)

The device provides two clock security systems (CSS), one for HSE oscillator and one for LSE oscillator. They can be independently enabled by software.

When the clock security system on HSE is enabled, the clock detector is activated after the HSE oscillator startup delay, and disabled when this oscillator is stopped:

- If the HSE oscillator is used directly or indirectly as the system clock (indirectly meaning that it is directly used as PLL input clock, and that PLL clock is the system clock) and a failure is detected, then the system clock switches to the HSI oscillator and the HSE oscillator is disabled.
- If a failure is detected on the HSE clock, this oscillator is automatically disabled, a clock failure event is sent to the break inputs of advanced-control timers TIM1, TIM8, TIM15, TIM16, and TIM17, and a non-maskable interrupt is generated to inform the software about the failure (clock security system interrupt rcc_hsecss_it), allowing the MCU to perform rescue operations. The rcc_hsecss_it is linked to the Cortex®-M7 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator clock was used as PLL clock source, the PLL is also disabled when the HSE fails.

The clock security system on LSE must be enabled only when the LSE is enabled and ready, and after the RTC clock has been selected through the RTCSRC[1:0] bits of RCC_BDCR register.

When an LSE failure is detected, the CSS on LSE wakes up the device from all low-power modes except V_{BAT}. If the failure occurred in V_{BAT} mode, the software can check the failure detection bit when the device is powered on again. In all cases the software can select the best behavior (including disabling the CSS on LSE which is not automatic).

5 Boot configuration

5.1 Boot mode selection

In STM32H743/753xx microcontrollers, two different boot spaces can be selected through the BOOT pin and the boot base address programmed in the BOOT_ADD0 or BOOT_ADD1 option bytes as shown in the *Table 1*.

Table 1. Boot modes

Boot mode selection		Boot space
BOOT pin	**Boot address option bytes**	
0	BOOT_ADD0 [15:0]	Boot address defined by BOOT_ADD0[15:0] user option byte Default factory programmed value: User Flash memory starting at 0x0800 0000
1	BOOT_ADD1 [15:0]	Boot address defined by BOOT_ADD1[15:0] user option byte Default factory programmed value: System Flash memory starting at 0x1FF0 0000

The BOOT_ADD0 and BOOT_ADD1 address option bytes allow to program any boot memory address from 0x0000 0000 to 0x3FFF 0000 which include:

- All the Flash memory address space mapped on AXIM interface.
- All the RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface.
- The system memory bootloader.

The BOOT_ADD0/BOOT_ADD1 option bytes can be modified after the reset in order to boot from any other boot address after the next reset.

If the programmed boot memory address is out of the memory mapped area or a reserved area, the default boot fetch address is programmed as follows:

- Boot address 0: Flash memory at 0x0800 0000
- Boot address 1: ITCM-RAM at 0x0000 0000

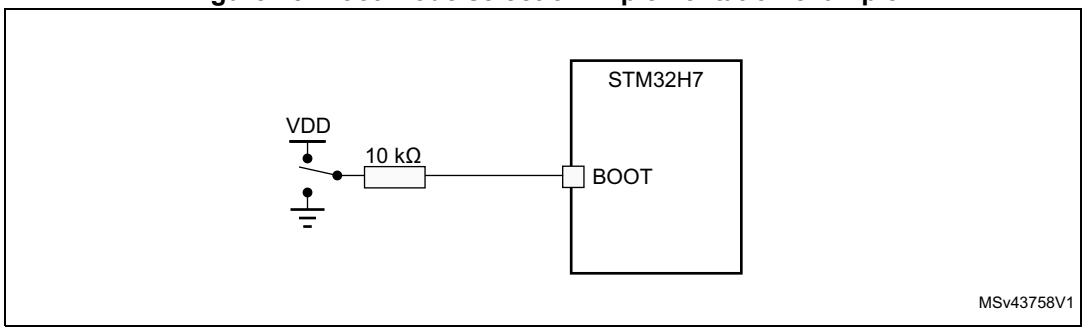
When the Flash level 2 protection is enabled, only boot from Flash memory is available. If the boot address already programmed in the BOOT_ADD0 / BOOT_ADD1 option bytes is out of the memory range or belongs to the RAM address range, the default fetch will be forced from Flash memory at address 0x0800 0000.

Note: When the Secure access mode is enabled through option bytes, the boot behavior differs from the above description (refer to section Root secure services of the product reference manual).

5.2 Boot pin connection

Figure 15 shows the external connection required to select the boot memory of STM32H743/753xx microcontrollers.

Figure 15. Boot mode selection implementation example



1. Resistor values are given only as a typical example.

5.3 System bootloader mode

The embedded bootloader code is located in the system memory. It is programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 2 shows the supported communication peripherals by the system bootloader.

Table 2. STM32H743/753xx bootloader communication peripherals

Bootloader peripherals	Bootloader pins
DFU	USB OTG FS (PA11/PA12) in device mode
USART1	PA9/PA10
USART2	PA2/PA3
USART3	PB10/PB11
CAN2	PB5/PB13
I2C1	PB6/PB9
I2C2	PF0/PF1
I2C3	PA8/PC9
I2C4	PD12/PD13
SPI1	PA4/PA5/PA6/PA7
SPI2	PI0/PI1/PI2/PI3

Table 2. STM32H743/753xx bootloader communication peripherals (continued)

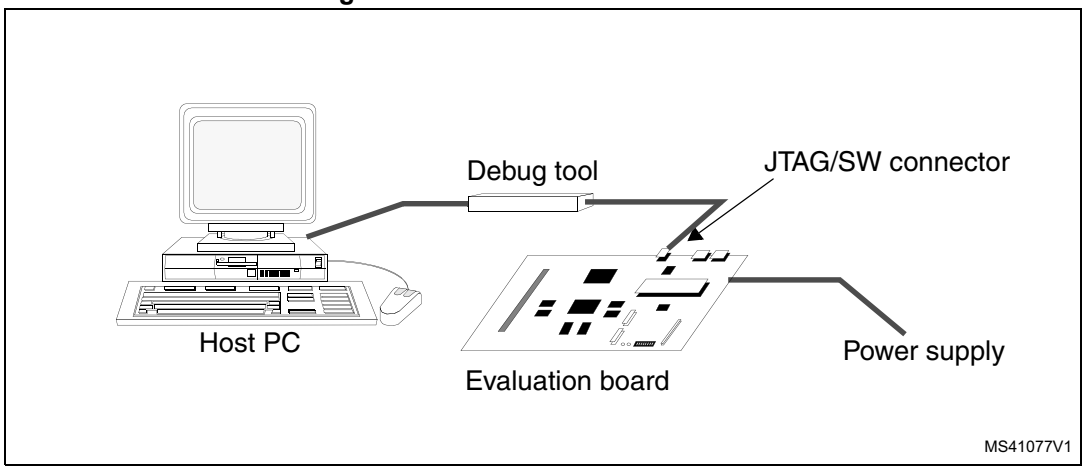
Bootloader peripherals	Bootloader pins
SPI3	PC12/PC11/PC10/PA15
SPI4	PE11 / PE12 / PE13 / PE14
USB OTG_FS in Device mode (DFU)	PA11/PA12

6 Debug management

6.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SW connector and a cable connecting the host to the debug tool. *Figure 16* shows the connection of the host to the evaluation board.

Figure 16. Host to board connection



6.2 SWJ debug port (serial wire and JTAG)

The core of STM32H743/753xx devices integrates the Serial Wire / JTAG Debug Port (SWJ-DP). It is an ARM® standard CoreSight debug port that combines a 5-pin JTAG-DP interface and a 2-pin SW-DP interface.

- The JTAG Debug Port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The Serial Wire Debug Port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

For more details on the SWJ debug port refer to RM0433 SWJ debug port section (serial wire and JTAG).

6.2.1 TPIU trace port

The TPIU trace port comprises four data outputs plus one clock output. The number of data outputs can be configured by software and unused signals can be reused as GPIOs. If the trace port is not required, all the signals can be used as GPIOs. By default, the trace port is disabled.

The trace data and clock can operate at up to 133 MHz. As a result, care must be taken with the layout of these signals: the trace connector should be located as close as possible to the

STM32H743/753xx, while still allowing enough space to attach the trace port analyzer probe.

Refer to *Table 3* for a summary of trace pins and GPIO assignment.

Table 3. TPIU trace pins

Trace pin name	Type	Description	Pin assignment
TRACED0	Output	Trace synchronous data out 0	PC1 or PE3 or PG13
TRACED1	Output	Trace synchronous data out 1	PC8 or PE4 or PG14
TRACED2	Output	Trace synchronous data out 2	PD2 or PE5
TRACED3	Output	Trace synchronous data out 3	PC12 or PE6
TRACECLK	Output	Trace clock	PE2

6.2.2 External debug trigger

The TRGIN and TRGOUT pins are available on some packages. On smaller packages, they are replaced by a bidirectional TRGIO signal, which is configured as TRGIN or TRGOUT by software.

Refer to *Table 4* for a summary of trigger pins and GPIO assignment.

Table 4. External debug trigger pins

Trigger pin name	Type	Description	Pin assignment
TRGIN	Input	External trigger input	PJ7
TRGOUT	Output	External trigger output	PJ12
TRGIO	Input/output	External trigger bi-directional	PC7

6.3 Pinout and debug port pins

STM32H743/753xx devices are available in various packages with different numbers of available pins. As a result, some functionality related to the pin availability (TPIU parallel output interface) may differ between the packages.

6.3.1 SWJ debug port pins

Five pins are used as outputs from the STM32H743/753xx devices for the SWJ-DP as alternate functions of general-purpose I/Os. These pins are available on all packages.

Table 5. SWJ debug port pins

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode Selection	IO	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if asynchronous trace is enabled	PB3
NJTRST	I	JTAG test nReset	-	-	PB4

6.3.2 Flexible SWJ-DP pin assignment

After RESET (SYSRESETn or PORESETn), all the five pins used for the SWJ-DP are assigned as dedicated pins immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32H743/753xx devices offer the possibility of disabling some or all of the SWJ-DP ports and so, of releasing the associated pins for general-purpose IO (GPIO) usage.

Table 6 shows the different possibilities to release some pins.

Table 6. Flexible SWJ-DP assignment

Available debug ports	SWJ IO pin assigned				
	PA13/ JTMS/ SWDIO	PA14/JTCK /SWCLK	PA15/JTDI	PB3/JTDO	PB4/NJTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without NJTRST	X	X	X	X	-
JTAG-DP disabled and SW-DP enabled	X	X	-		
JTAG-DP disabled and SW-DP disabled	Released				

For more details on how to disable SWJ-DP port pins, please refer to the reference manual I/O pin alternate function multiplexer and mapping section.

6.3.3 Internal pull-up and pull-down on JTAG pins

The devices embed internal pull-ups and pull-downs to guarantee a correct JTAG behavior. The following pins are consequently not left floating during reset and they are configured as follows until the user software takes control of them:

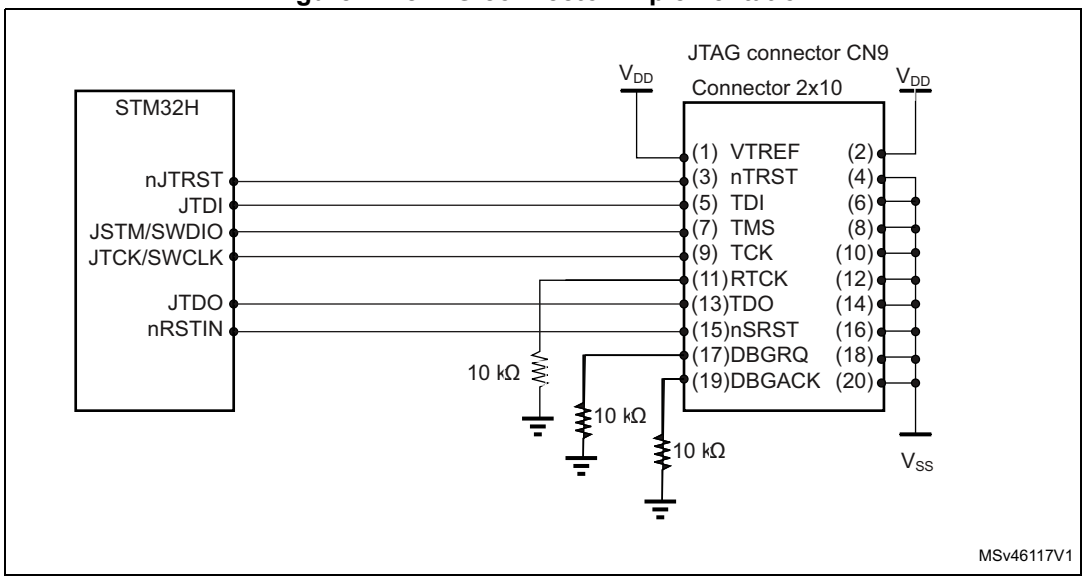
- NJTRST: internal pull-up.
- JTDI: internal pull-up.
- JTMS/SWDIO: internal pull-up.
- TCK/SWCLK: internal pull-down.

If these I/Os are externally connected to a different voltage, leakage current will flow during and after reset, until they are reconfigured by software. Special care must be taken with the TCK/SWCLK pin, which is directly connected to the clock of some of these flip-flops, since it should not toggle before JTAG I/O is released by the user software."

6.3.4 SWJ debug port connection with standard JTAG connector

Figure 17 shows the connection between STM32H743/753xx devices and a standard JTAG connector.

Figure 17. JTAG connector implementation



7 Recommendations

7.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to the ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides a good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for the ground and for the power supply.

7.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce the cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

7.3 Ground and power supply (V_{SS},V_{DD})

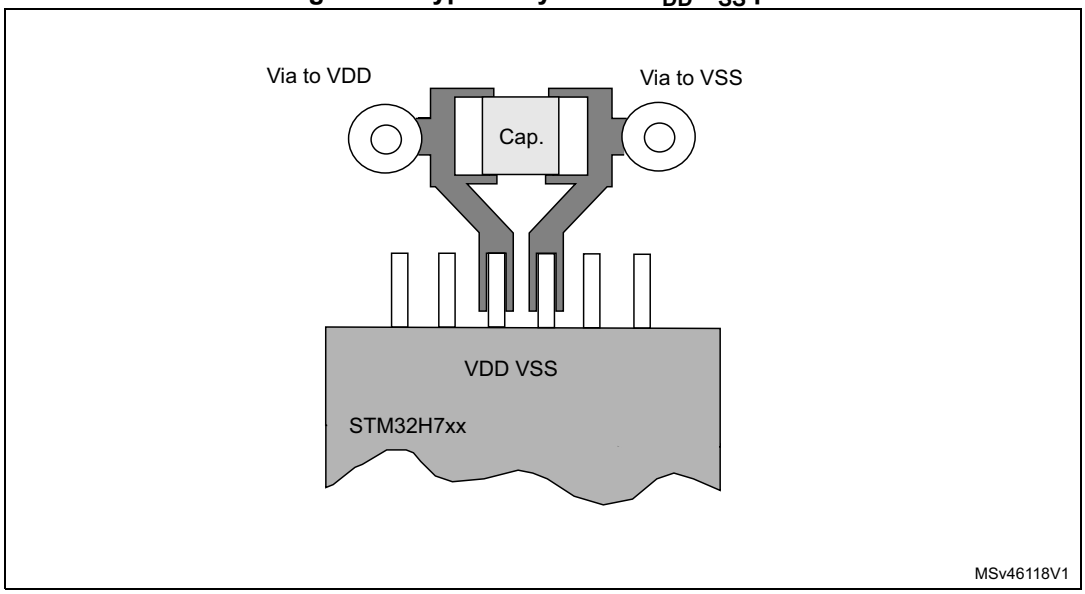
Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the area of the supply loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

7.4 Decoupling

All the power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and one single tantalum or ceramic capacitor (min. 4.7 µF) connected in parallel. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but the exact values depend on the application needs. *Figure 18* shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 18. Typical layout for V_{DD}/V_{SS} pair



7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands). For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve the EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (clock, etc.).
- Sensitive signals (high impedance, etc.).

7.6 Unused I/Os and features

All the microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources. To increase the EMC performance, unused clocks, counters or I/Os, should not be left free, e.g. I/Os should be set to “0” or “1” (pull-up or pull-down to the unused I/O pins.) and unused features should be “frozen” or disabled.

8 Reference design

8.1 Description

The reference design shown in *Figure 19*, is based on the STM32H753XI, a highly integrated microcontroller that combines the ARM® Cortex®-M7 32-bit RISC core running at up to 400 MHz with up to 2 Mbyte dual-bank Flash memory and 1 Mbytes of RAM (including 192 Kbytes of TCM RAM, 864 Kbytes of user RAM and 4 Kbytes of backup SRAM).

8.1.1 Clocks

Two clock sources are used for the microcontroller:

- LSE: X2– 32.768 kHz crystal for the embedded RTC.
- HSE: X1– 25 MHz crystal.

Refer to *Section 4: Clocks on page 20*.

8.1.2 Reset

The reset signal of STM32H753XI device is low active and the reset sources include:

- Reset button B1
- Debugging Tools from JTAG/SWD connector CN15 and ETM trace connector CN12

Refer to *Section 2.3: Reset and power supply supervisor on page 14*.

8.1.3 Boot mode

Refer to *Section 5: Boot configuration on page 24*.

8.1.4 SWJ interface

Refer to *Section 6: Debug management on page 27*.

8.1.5 Power supply

Refer to *Section 2: Power supplies on page 7*.

8.2 Component references

Table 7. Mandatory components

Id	Component name	Reference	Quantity	Comments
1	Microcontroller	STM32H753XI	1	TFBGA240 package
2	Capacitor	100 nF	20	Ceramic capacitors (decoupling capacitors)
3	Capacitor	4.7 µF	1	Ceramic capacitor (decoupling capacitor)
	Capacitor	2.2 µF	2	Ceramic capacitor (regulator capacitor)

Table 8. Optional components

Id	Components name	Reference	Quantity	Comments
1	Resistor	10 kΩ	5	Pull-up and pull-down for JTAG, BOOT pin, PDR
2	Resistor	0 Ω	1	Used as star connection point between V_{DDA} and V_{REF+}
3	Capacitor	100 nF	3	Ceramic capacitor
4	Capacitor	1.5 pF	2	Used for LSE: the value depends on the crystal characteristics
5	Capacitor	1 µF	3	Used for V_{DDA}, V_{REF} and V_{DDUSB}
6	Capacitor	3.9 pF	2	Used for HSE: the value depends on the crystal characteristics
7	Quartz	25 MHz	1	Used for HSE
8	Quartz	32.768 kHz	1	Used for LSE
9	JTAG connector	HE10-20	1	–
10	Battery	3 V	1	If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.
11	Switch	SPDT	1	Used to select the right boot mode.
12	Push-button	B1	1	Reset button
13	Jumper	3 pins	2	Used to select V_{BAT} source
14	Ferrite bead	FCM1608KF-601T03	1	Additional decoupling for V_{DDA}

Figure 19. STM32H753XI reference schematic

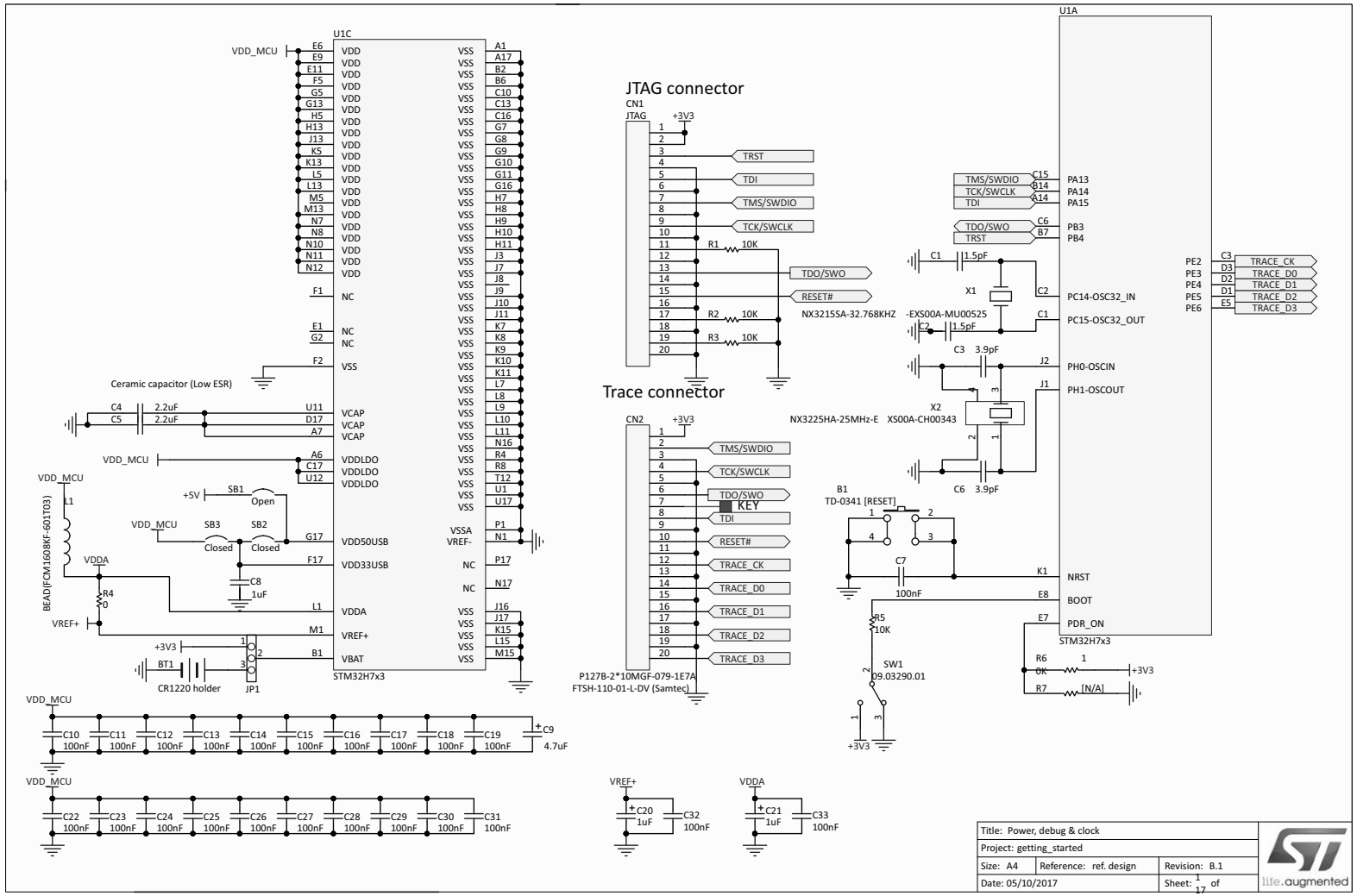


Table 9. Reference connection for all packages

Pin name (function after reset)	Pin/ball name					
	LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25
VSS	-	-	-	-	-	A1
VDD	-	-	-	-	-	E6
VBAT	6	6	C1	6	6	B1
VSS	-	-	-	-	-	A1
VSS	-	-	-	-	-	A1
PC14-OSC32_IN (PC14)(1)(2)	8	8	E1	9	9	C2
PC15-OSC32_ OUT (PC15)(1)(2)	9	9	F1	10	10	C1
VSS	-	-	F2	14	14	A1
VDD	-	-	F3	15	15	E6
VSS	10	16	G2	22	25	B2
VDD	11	17	G3	23	26	E11
PH0-OSC_IN (PH0)(2)	12	23	G1	29	32	J2
PH1-OSC_OUT (PH1)(2)	13	24	H1	30	33	J1
NRST	14	25	J1	31	34	K1
VDD	-	30	G3	36	39	F5
VSS	-	-	-	-	-	B6
VSSA	19	31	M1	37	40	P1
VREF-	-	-	N1	-	-	N1
VREF+	20	32	P1	38	41	M1
VDDA	21	33	R1	39	42	L1
PA0-WKUP (PA0)	22	34	N3	40	43	N5
VDD	-	-	-	-	-	F5
VSS	-	-	-	-	-	C10
VSS	26	38	L4	48	51	C13
VDD	27	39	K4	49	52	G5
VDD	-	-	-	-	59	G13
VSS	-	-	-	-	60	C16

Table 9. Reference connection for all packages (continued)

Pin name (function after reset)	Pin/ball name					
	LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25
VSS	-	51	M8	61	72	F2
VDD	-	52	N8	62	73	H5
VSS	-	-	-	-	-	G7
VDD	-	-	-	-	-	H13
VSS	-	61	M9	71	82	G8
VDD	-	62	N9	72	83	J13
VSS	-	-	-	-	-	G9
VDD	-	-	-	-	-	K5
VCAP1	48	71	M10	81	92	U11
VSS	49	-	-	-	93	G10
VDDLDO1	-	-	-	-	-	U12
VDD	-	72	N10	82	94	K13
VDD33 USB	50	-	-	-	-	-
VSS	-	-	-	-	-	G11
VDD	-	-	-	-	-	L5
VSS	-	-	H12	90	-	H7
VDD	-	-	J12	91	103	L13
VDD	-	-	-	-	-	M5
VSS	-	-	-	-	-	H8
VSS	-	83	-	102	114	H9
VDD	-	84	J13	103	115	M13
VDD	-	-	-	-	-	N7
VSS	-	-	-	-	-	H10
VDD	-	-	-	-	124	N8
VDD	-	-	-	-	-	N10
VSS	-	-	-	-	125	H11
VDD	-	-	-	-	-	N11
VSS	-	-	-	-	-	J7
VDD	-	-	-	-	-	N12
VSS	-	-	-	-	-	J8

Table 9. Reference connection for all packages (continued)

Pin name (function after reset)	Pin/ball name					
	LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25
VSS	-	-	-	-	-	J9
VDD	-	-	-	-	-	P17
VSS	-	94	G12	113	136	J10
VDD50 USB	-	-	-	-	-	G17
VDD33 USB	-	95	H13	114	137	F17
VDD	-	-	-	-	-	E9
VSS	-	-	-	-	-	J11
VDD	-	-	-	-	-	E11
PA13 (JTMS/SWDIO)	72	105	A15	124	147	C15
VCAP2	73	106	F13	125	148	D17
VSS	74	107	F12	126	149	K7
VDDLDO2	-	-	-	-	-	C17
VDD	75	108	G13	127	150	F5
VSS	-	-	-	-	-	K8
VDD	-	-	-	-	-	F5
VSS	-	-	D9	135	-	K9
VDD	-	-	C9	136	158	G5
PA14 (JTCK/SWCLK)	76	109	A14	137	159	B14
PA15(JTDI)	77	110	A13	138	160	A14
VSS	-	-	-	-	-	K10
VDD	-	-	-	-	-	G13
VSS	-	120	D8	148	170	K11
VDD	-	121	C8	149	171	H5
VSS	-	-	-	-	-	L7
VDD	-	-	-	-	-	H13
VSS	-	130	D7	158	184	L8
VDD	-	131	C7	159	185	J13
VSS	-	-	-	-	-	L9
VDD	-	-	-	-	-	K5

Table 9. Reference connection for all packages (continued)

Pin name (function after reset)	Pin/ball name					
	LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25
PB3 (JTDO/TRACESWO)	89	133	A10	161	192	C6
PB4 (NJTRST)	90	134	A9	162	193	B7
VSS	-	-	-	-	-	L10
VDD	-	-	-	-	-	K13
BOOT0	94	138	D6	166	197	E8
VCAP3	-	-	-	-	-	A7
VSS	99	-	D5	-	202	L11
PDR_ON	-	143	C6	171	203	E7
VDDLDO3	-	-	-	-	-	A6
VDD	100	144	C5	172	204	L5
VSS	-	-	-	-	-	J16
VDD	-	-	-	-	-	L13

1. PC1, PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
2. 5 V tolerant except when in analog mode or oscillator mode for PC14, PC15, PH0 and PH1.

9 Recommended PCB routing guidelines for STM32H743/753xx devices

9.1 PCB stack-up

In order to reduce the reflections on high speed signals, it is necessary to match the impedance between the source, sink and transmission lines. The impedance of a signal trace depends on its geometry and its position with respect to any reference planes.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized.

The minimum configuration that can be used is 4 or 6 layers stack-up. An 8 layers boards may be required for a very dense PCBs that have multiple SDRAM/SRAM/NOR/LCD components.

The following stack-ups are intended as examples which can be used as a starting point for helping in a stack-up evaluation and selection. These stack-up configurations are using a GND plane adjacent to the power plane to increase the capacitance and reduce the gap between GND and power plane. So high speed signals on top layer will have a solid GND reference plane which helps to reduce the EMC emissions, as going up in number of layers and having a GND reference for each PCB signal layer will improve further the radiated EMC performance.

Figure 20. Four layer PCB stack-up example

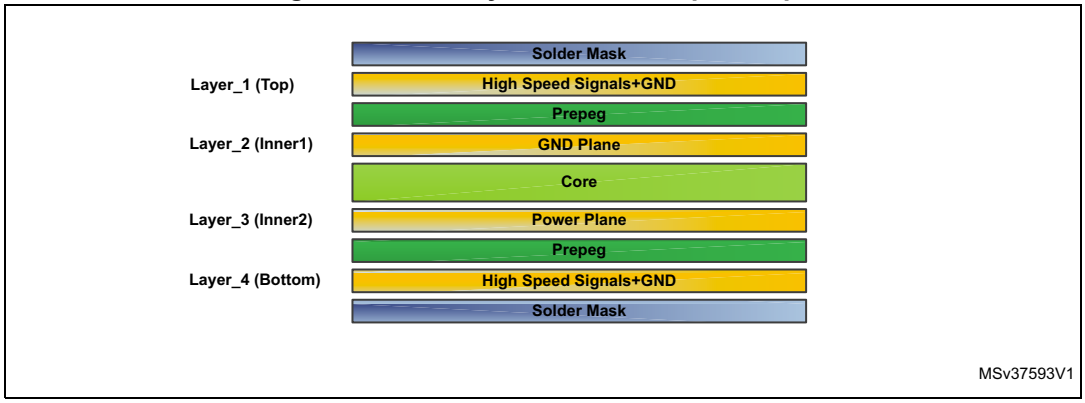
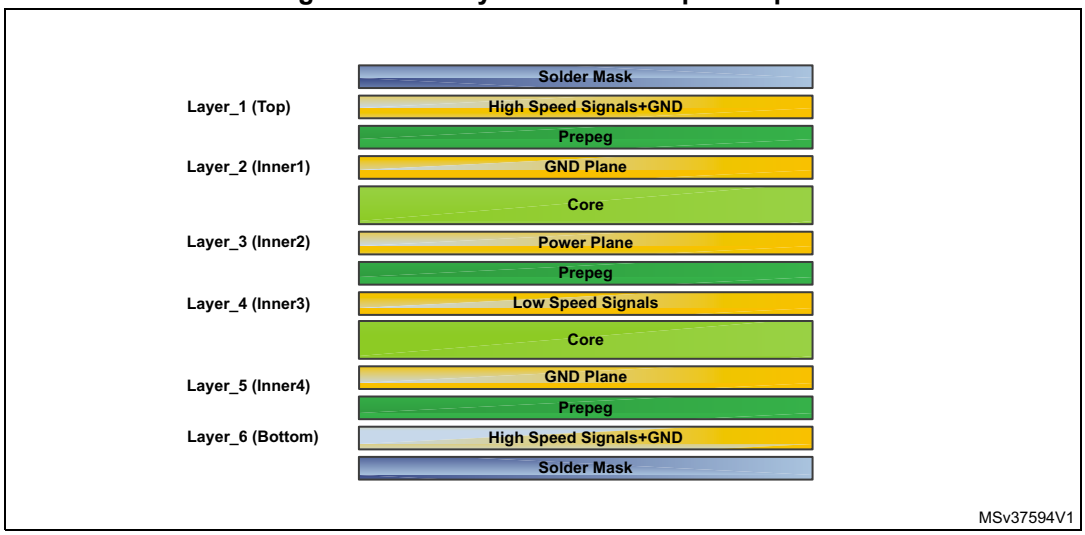


Figure 21. Six layer PCB stack-up example



9.2 Crystal oscillator

Use the application note: *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers* (AN2867), for further guidance on how to layout and route crystal oscillator circuits.

9.3 Power supply decoupling

An adequate power decoupling for STM32H743/753xx devices is necessary to prevent an excessive power noise and ground bounce noise. Please refer to *Section 2.2: Power supply scheme*.

The following recommendations shall be followed:

- Place the decoupling capacitors as close as possible to the power and ground pins of the MCU. For BGA packages, it is recommended to place the decoupling capacitors on the other side of the PCB (see *Figure 22*).
- Add the recommended decoupling capacitors for as many V_{DD}/GND pairs as possible.
- Connect the decoupling capacitor pad to the power and ground plane with a wider, short trace/via. This allows reducing the series inductance, maximizing the current flow and minimizing the transient voltage drops from the power plane which also reduces the possibility of ground bounce.

Figure 23 shows an example of decoupling capacitor placement underneath STM32H743/753xx devices, closer to the pins and with less vias.

Figure 22. Decoupling capacitor placement depending on package type

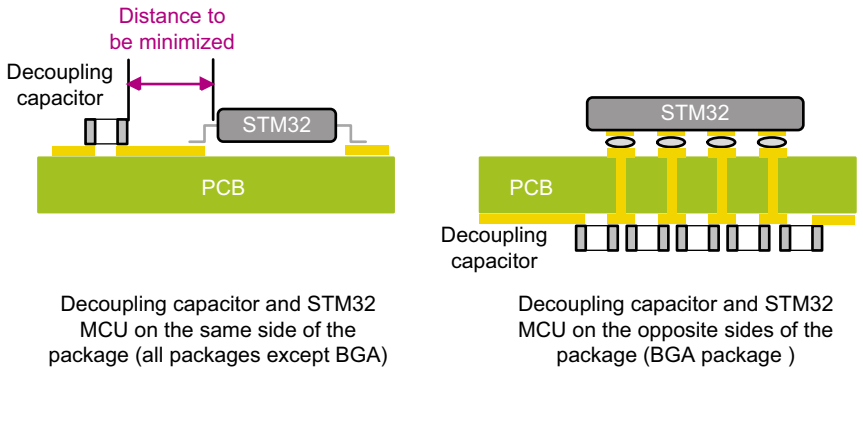
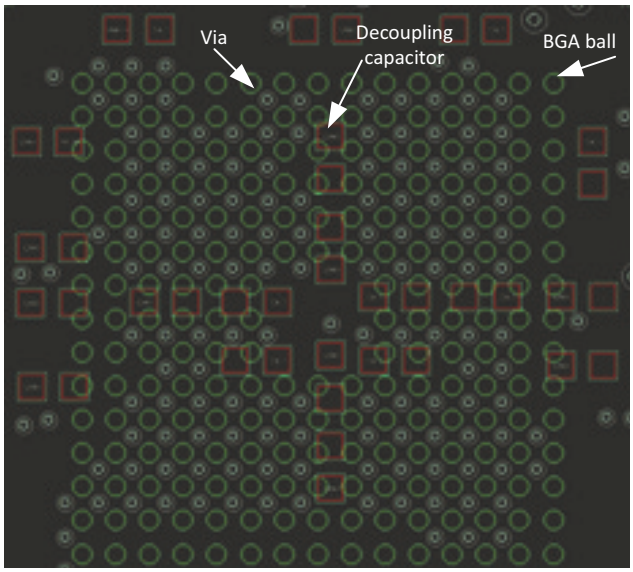


Figure 23. Example of decoupling capacitor placed underneath the STM32H743/753xx



9.4 High speed signal layout

9.4.1 SDMMC bus interface

Interface connectivity

The SD/SDIO MMC card host interface (SDMMC) provides an interface between the AHB peripheral bus and Multi Media Cards (MMCs), SD memory cards and SDIO cards. The SDMMC interface is a serial data bus interface, that consists of a clock (CK), command signal (CMD) and 8 data lines (D[0:7]).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf switching cap between PWR and GND)
- Trace the impedance: 50 Ω ± 10%
- The skew being introduced into the clock system by unequal trace lengths and loads, minimize the board skew, keep the trace lengths equal between the data and clock.
- The maximum skew between data and clock should be below 250 ps @ 10mm
- The maximum trace length should be below 120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- The trace capacitance should not exceed 20 pF at 3.3 V and 15 pF at 1.8 V
- The maximum signal trace inductance should be less than 16 nH
- Use the recommended pull-up resistance for CMD and data signals to prevent bus floating.
- The mismatch within data bus, data and CK or CK and CMD should be below 10mm.
- Keep the same number of vias between the data signals

Note: The total capacitance of the SD memory card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line. The total bus capacitance is $C_L = C_{Host} + C_{Bus} + N*C_{Card}$ where the host is an STM32H743/753xx device, bus is all the signals and Card is SD card.

9.4.2 Flexible memory controller (FMC) interface

Interface connectivity

The FMC controller and in particular SDRAM memory controller which has many signals, most of them have a similar functionality and work together. The controller I/O signals could be split in four groups as follow:

- An address group which consists of row/column address and bank address
- A command group which includes the row address strobe (NRAS), the column address strobe (NCAS), and the write enable (SDWE)
- A control group which includes a chip select bank1 and bank2 (SDNE0/1), a clock enable bank1 and bank2 (SDCKE0/1), and an output byte mask for the write access (DQM).
- A data group/lane which contains 8 signals [(a)]: the eight D (D7–D0) and the data mask (DQM).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50 Ω ± 10%
- The maximum trace length should be below 120mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Reduce the crosstalk, place data tracks on the different layers from the address and control lanes, if possible. However, when the data and address/control tracks coexist on the same layer they must be isolated from each other by at least 5 mm.
- Match the trace lengths for the data group within ± 10 mm of each other to diminish the skew. Serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be used to match the lengths.
- Placing the clock (SDCLK) signal on an internal layer, minimizes the noise (EMI). Route the clock signal at least 3x of the trace away from others signals. Use as less vias as possible to avoid impedance change and reflection. Avoid using serpentine routing.
- Match the clock traces to the data/address group traces within ±10mm.
- Match the clock traces to each signal trace in the address and command groups to within ±10mm (with maximum of <= 20 mm).
- Trace the capacitances:
  - At 3.3 V keep the trace within 20 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 30 pF.
  - At 1.8 V keep the trace within 15 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 20 pF.

9.4.3 Quadrature serial parallel interface (QUADSPI)

Interface connectivity

The QUADSPI is a specialized communication interface targeting single, dual or QUADSPI FLASH memories. The QUADSPI interface is a serial data bus interface, that consists of a clock (SCLK), a chip select signal (nCS) and 4 data lines (IO[0:3]).

a.It depends of the used memory: SDRAM with x8 bus widths have only one data group, while x16 and x32 bus-width SDRAM have two and four lanes, respectively.

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50 W ± 10%
- The maximum trace length should be below 120mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least 3x of the trace away from other signals. Use as less vias as possible to avoid the impedance change and reflection. Avoid using a serpentine routing.
- Match the trace lengths for the data group within ± 10 mm of each other to diminish skew. Serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be used to match the lengths.

- Avoid using a serpentine routing for the clock signal and as less via(s) as possible for the whole path. a via alters the impedance and adds a reflection to the signal.

9.4.4 Embedded trace macrocell (ETM)

Interface connectivity

The ETM enables the reconstruction of the program execution. The data are traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the data bus of 4 lines D[0:3] and the clock signal CLK.

Interface signals layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50 Ω ± 10%
- All the data trace should be as short as possible (<=25 mm),
- Trace the lines which should run on the same layer with a solid ground plane underneath it without a via.
- Trace the clock which should have only point-to-point connection. Any stubs should be avoided.
- It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they should be as short as possible. If longer are required, there should be a possibility to optionally disconnect them (e.g. by jumpers).

10 Conclusion

This application note should be used as a reference when starting a new design with an STM32H743xx or STM32H753xx microcontroller.

11 Revision history

Table 10. Document revision history

Date	Revision	Changes
13-Jun-2017	1	Initial release.
26-Jan-2017	2	Added *Section 1: General information*. Updated *Figure 19: STM32H753XI reference schematic*.