17. Simplify the following functional expressions using Boolean algebra and its identities. List the identity used at each step.

a) 
$$x(y + z)(x' + z') = x(yx' + yz' + zx' + zz')$$
;  $zz' = 0$   
=  $x(yx' + yz' + zx')$   
=  $xyx' + xyz' + xzx'$ ;  $xx' = 0$   
=  $xyz'$ 

b) 
$$xy + xyz + xy'z + x'y'z$$
 =  $y(x + xz) + y'(xz + x'z)$   
=  $y(x(1 + z)) + y'(z(x + x'))$ ;  $1 + z = 1, x + x' = 1$   
=  $yx + y'z$ 

c) 
$$xy'z + x(y + z')' + xy'z' = xy'z + xy'z + xy'z'$$
  
 $= xy'(z + z + z')$   
 $= xy'(z + z')$   
 $= xy'(z + z'); z+z'=1$   
 $= xy'$ 

20. Using the basic identities of Boolean algebra, show that x + x'y = x + y

$$x + x'y = x + y$$
  
 $x + x'y = (x + y)(x+x')$   
 $x + x'y = x + xy + xx' + x'y ; xx' = 0$   
 $x + x'y = x + x'y + xy$   
 $x + x'y = x(1+y) + x'y ; 1+y = 1$   
 $x + x'y = x + x'y$ 

23. The truth table for a Boolean expression is shown below. Write the Boolean expression in sum-of-products form.

х	у	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	11	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

SOP = 
$$x'y'z' + x'y'z + x'yz' + xy'z' + xy'z$$
  
POS =  $(x + y' + z')(x' + y' + z)(x' + y' + z')$ 

30. Draw a half-adder using only NAND gates.

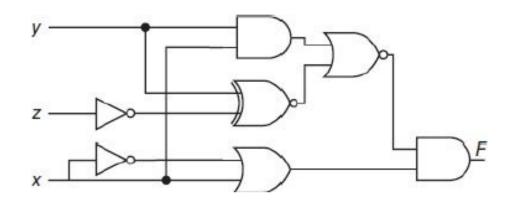
31. Draw a full-adder using only NAND gates.

32. Design a circuit with three inputs x, y, and z representing the bits in a binary number, and three outputs (a, b, and c) also representing bits in a binary number. When the input is 0, 1, 6, or 7, the binary output will be the complement of the input. When the binary input is 2, 3, 4, or 5, the output is the input shifted left with rotate. (For example, 3 = 0112 outputs 110; 4 = 1002 outputs 001.) Show your truth table, all computations for simplification, and the final circuit.

X	Υ	Z	А	В	С
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	0
0	1	1	1	1	0
,1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	0	0	0

Patipol Saechan 60130500219 33. Draw the combinational circuit that directly implements the Boolean expression: F(x,y,z) = xyz + (y'+z)

## 37. Find the truth table that describes the following circuit:



$$F=(yx+(y\bigoplus z')')'(x+x')$$

Х	У	Z	x'	z'	ху	(y ⊕ z')'	x+x'	$(yx + (y \bigoplus z')')'$	$(yx + (y \bigoplus z')')'(x+x')$
0	0	0	1	1	0	0	1	1	1
0	0	1	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1	0	0
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	0	0	1	1	1
1	0	1	0	0	0	1	1	0	0
1	1	0	0	1	1	1	1	0	0
1	1	1	0	0	1	0	1	0	0

## 39. How many inputs does a decoder have if it has 64 outputs?

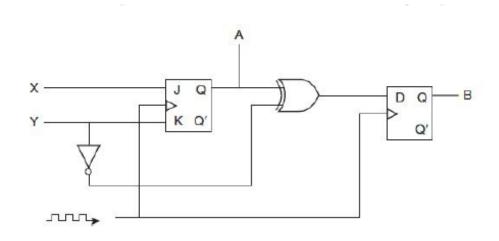
000000 → 111111

It need to contain output 0 to 63 that mean Decoder need to have 6 bit to represent output 0 to 63

44. Design a truth table for a combinational circuit that detects an error in the representation of a decimal digit encoded in BCD. (This circuit should output a 1 when the input is one of the six unused combinations for BCD code.)

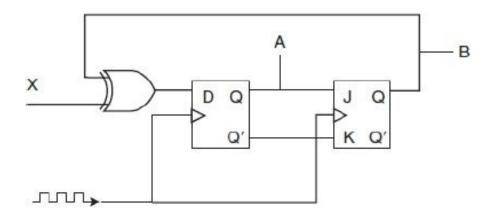
W	Χ	Υ	Z	F
0	0	0	0	0
0	0	0	1	0
0 0 0 0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1 1 1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

## 50. Complete the truth table for the following sequential circuit:



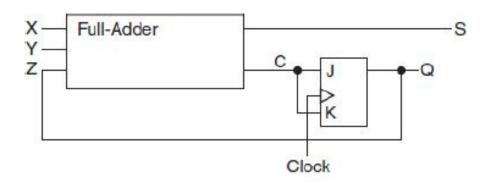
X	Υ	А	Next State		
			Α	В	
0	0	0	0	1	
0	0	1	1	0	
0	1	0	0	0	
0	1	1	0	1	
1	0	0	1	1	
1	0	1	1	0	
1	1	0	1	0	
1	1	1	0	1	

## 51. Complete the truth table for the following sequential circuit:



А	В	Х	Next State		
			А	В	
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	0	
0	1	1	0	0	
1	0	0	0	1	
1	0	1	1	1	
1	1	0	1	1	
1	1	1	0	1	

55. A sequential circuit has one flip-flop; two inputs, X and Y; and one output, S. It consists of a full-adder circuit connected to a JK flip-flop, as shown. Fill in the truth table for this sequential circuit by completing the Next State and Output columns.



Present State	Input		Next State	Output
Q(t)	X	Υ	Q(t+1)	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1