

Logic Synthesis and Verification HW2

Programming ABC

Add file

- src/testC/module.make
- src/testC/testcmd.c
- src/testC/testC.c
- src/testC/testC.h

Change Code

- Makefile
- src/base/main/mainInit.c

Target

- Implement technology mapping with abc and create addition command on it.
- Input files: pa2.lib(cell lib), filename.blif(network)
- Output file: filename.blif.mbench(optimize netlist)

Steps of hw2

1. Read ../PA2/pa2.lib (cell lib)
2. Read network with abc (filename.blif)
3. Strash network to AIG format with abc
4. Create network graph with our code (and, inv, and buf)
5. Compute initial delay and its original power for every gate
6. Check is valid or not (slack ≥ 0 -> valid)
7. Optimize power with decrease greatest slack gate power if its power can be optimize
8. Continue step 8 until slack cannot be optimize
9. Check is valid or not (slack ≥ 0 -> valid)
10. Save initial delay, original power, optimize power, and netlist to filename.blif.mbench

Environment

- Ubuntu
- gcc (Ubuntu 7.5.0-3ubuntu1~18.04) 7.5.0
- g++ (Ubuntu 7.5.0-3ubuntu1~18.04) 7.5.0

Folder Architecture

- Need to put PA2 and abc in same folder.
- If you want to change input cell lib(like pa2.lib), you need to modify the code in abc/src/base/testC/testc.h (#define LIB_NAME "../PA2/pa2.lib")

```
abc/  
  Makefile  
  run_all.sh  
  src/  
    base/  
      main/  
        mainInit.c  
      testC/  
        module.make  
        testC.c  
        testC.h  
        testcmd.c  
    results/  
      c432.blif.mbench  
      c499.blif.mbench  
      c880.blif.mbench  
      c1355.blif.mbench  
      c1908.blif.mbench  
      c2670.blif.mbench  
      c3540.blif.mbench  
      c5315.blif.mbench  
      c6288.blif.mbench  
      c7552.blif.mbench  
  PA2/  
    pa2.lib  
    ISCAS85/  
      c432.blif  
      c499.blif  
      c880.blif  
      c1355.blif  
      c1908.blif  
      c2670.blif  
      c3540.blif  
      c5315.blif  
      c6288.blif  
      c7552.blif
```

Compile Project

```
cd abc  
make
```

Run Code

1. Use abc command with one input network: (output file with save at abc/filename.blif.mbench)

```
cd abc
./abc
read filename.blif
strash
hw2
quit
```

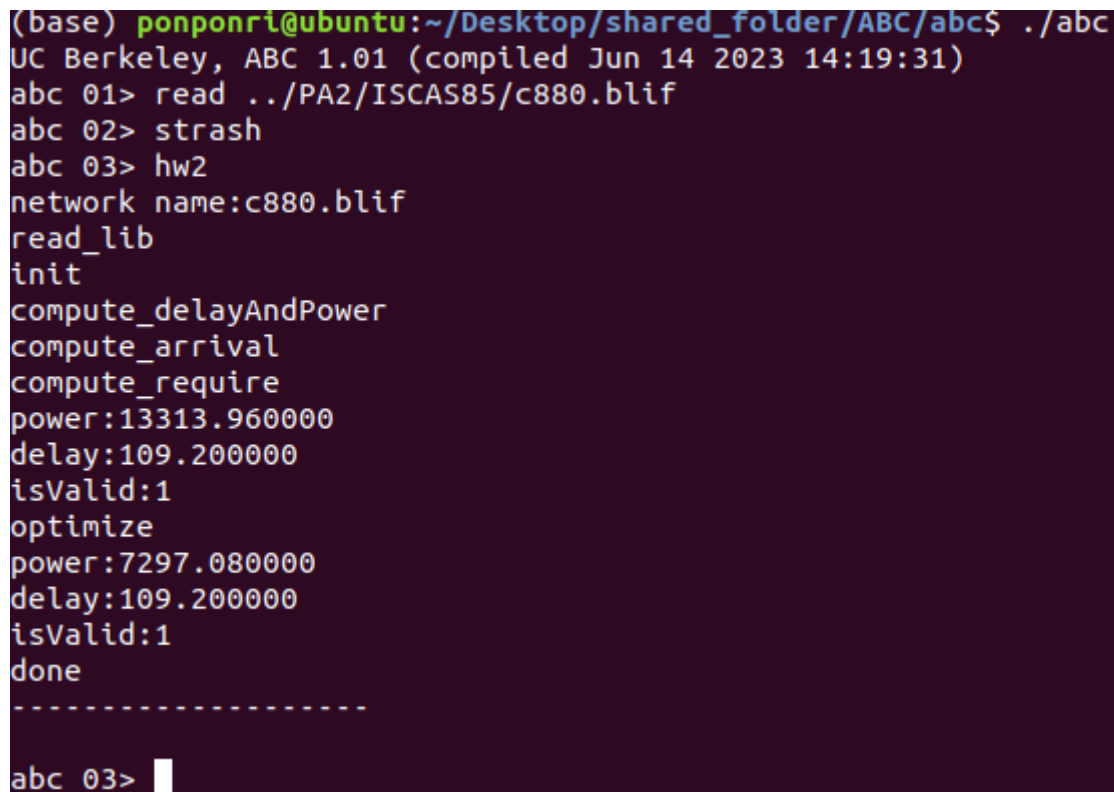
2. Run script with multiple network store in one folder: (output file with save at abc/results/filename.blif.mbench)

```
cd abc
./run_all.sh {input folder} # ex: ./run_all.sh ../PA2/ISCAS85/
```

Results

1. abc command mode

c880.blif



```
(base) ponponri@ubuntu:~/Desktop/shared_folder/ABC/abc$ ./abc
UC Berkeley, ABC 1.01 (compiled Jun 14 2023 14:19:31)
abc 01> read ../PA2/ISCAS85/c880.blif
abc 02> strash
abc 03> hw2
network name:c880.blif
read_lib
init
compute_delayAndPower
compute_arrival
compute_require
power:13313.960000
delay:109.200000
isValid:1
optimize
power:7297.080000
delay:109.200000
isValid:1
done
-----
abc 03> 
```

c880.blif.mbench

```
1 # Initial delay:109.200000
2 # Original power:13313.960000
3 # Optimized power:7297.080000
4 INPUT (c1gat)
5 INPUT (c8gat)
6 INPUT (g13gat)
7 INPUT (g17gat)
8 INPUT (g26gat)
9 INPUT (g29gat)
10 INPUT (g36gat)
11 INPUT (g42gat)
12 INPUT (g51gat)
13 INPUT (g55gat)
14 INPUT (g59gat)
15 INPUT (g68gat)
16 INPUT (g72gat)
17 INPUT (g73gat)
18 INPUT (g74gat)
19 INPUT (g78gat)
20 INPUT (c80gat)
21 INPUT (c85gat)
22 INPUT (c86gat)
23 INPUT (c87gat)
24 INPUT (c88gat)
25 INPUT (c89gat)
26 INPUT (c90gat)
27 INPUT (c91gat)
28 INPUT (c96gat)
29 INPUT (c101gat)
30 INPUT (c106gat)
31 INPUT (c111gat)
32 INPUT (c116gat)
33 INPUT (c121gat)
34 INPUT (c126gat)
35 INPUT (c130gat)
36 INPUT (c135gat)
37 INPUT (c138gat)
38 INPUT (c143gat)
39 INPUT (c146gat)
40 INPUT (c149gat)
```

2. script mode

../PA2/ISCAS85/

```
ponponri@ubuntu: ~/Desktop/shared_folder/ABC/abc
[22]- Stopped
(base) ponponri@ubuntu:~/Desktop/shared_folder/ABC/abc$ ./run_all.sh ../PA2/ISCAS85/
ABC command line: "read ../PA2/ISCAS85/c1355.blif; strash; hw2".
network name:c1355.blif
read_ltb
init
compute_delayAndPower
compute_arrival
compute_require
power:10696.720000
delay:102.200000
isValid:1
optimize
power:14759.680000
delay:102.200000
isValid:1
done
-----
ABC command line: "read ../PA2/ISCAS85/c1908.blif; strash; hw2".
network name:c1908.blif
read_ltb
init
compute_delayAndPower
compute_arrival
compute_require
power:20437.880000
delay:140.280000
isValid:1
optimize
power:13586.320000
delay:140.280000
isValid:1
done
-----
ABC command line: "read ../PA2/ISCAS85/c2670.blif; strash; hw2".
network name:c2670.blif
read_ltb
init
compute_delayAndPower
```

abc/results/

