HW lab assignment 1 - Crosstalk

Introduction

This note describes the hands-on lab exercise – Crosstalk - to be completed as part of the graduate course "Electronic Hardware System Design.

Lab assignment 1 will be graded and its weight is 25% of the final grade.

The assignment will be completed over three weeks with two 4-hour modeling and simulation exercise days and a 4-hour HW lab measurement exercise day (third week) on the test-board.

The deadline for submission of the assignment report – Crosstalk is 16th Dec. 2024.

The remaining part of the note describes:

- 1) The HW test board and info used for the exercise are on pages 2-4.
- 2) The task plan for the modeling and simulation exercise (part 1) is on pages 5-7.
- 3) The task plan for the measurement exercise (part 2) is on pages 8-9.
- 4) Guidelines for final lab report on page 10.

HW test board info

The HW test board¹ is shown in Figure 1 and the associated PCB stack-up is in Figure 2.



Figure 1: HW test board.

Layer	Туре	Cross Sec	tion	Cu (finished, inc. Plating)	Track Width	Track-track spacing
		[um]	[mil]	[um]	[um]	[um]
		10	0.4			
1				35	340	200
	Prepreg	180	7.1			
2				35		
	Laminate	200	7.9			
3				35		
	Prepreg	180	7.1			
4				35	217	200
	Laminate	200	7.9			
5				35	217	200
	Prepreg	180	7.1			
6				35		
	Laminate	200	7.9			
7				35		
	Prepreg	180	7.1			
8				35	340	200
		10	0.4			

Figure 2: Test-board - PCB stackup.

¹ Test-board is designed and developed by DTU – Electro.

A detailed schematic of the test-board/PCB design (*DTU-ExercisePCB_schematic*), and datasheet of the driver IC's (*Datasheet - sn74alvc244-DriverReceiverIC*) is associated with the HW exercise note and located in the *HW test board info* folder in Brightspace under the *Assignments* area.

The PCB is powered by USB (use an oscilloscope USB port).

The Supply voltage can be adjusted from 2.4V to 3.4V using the small potentiometer marked "VCC Adj. 2.4-3.4V". The supply voltage can be measured on probe point P45 marked "VCC" near the middle of the board.

The exercise PCB includes SN74ALVC244 octal buffers in the QFN package and the SOIC package. The outputs of the buffers Q1(QFN) and Q3(SOIC) are enabled using the jumpers on the left.

The input signal for the buffers is supplied by a 20Mhz clock. A clock fanout chip distributes the clock signal and is enabled by two jumpers on the left.

For each measurement that you make, only enable the outputs that you need, or else you will add ground bounce noise to your crosstalk measurement. (ground bounce will be explored in assignment 2)

Carefully study the circuit diagram to see which jumpers to enable for each measurement.

In the Crosstalk assignment we investigate the crosstalk of 3 possible transmission line configurations (remark the mutual capacitances are not negative – see lecture slides wrt topic):

1. Microstrip line

$$C (matrix) = \begin{bmatrix} 128,5 & -12,0 \\ -12,0 & 128,5 \end{bmatrix} \begin{bmatrix} \frac{pF}{m} \end{bmatrix}$$
$$L (matrix) = \begin{bmatrix} 283,4 & 52,2 \\ 52,2 & 283,4 \end{bmatrix} \begin{bmatrix} \frac{nH}{m} \end{bmatrix}$$

Propagation Speeds:

Mode 1: Differential(+-)
$$1.754630e+008 \text{ [m/s]} = 0.5853c \text{ Er(eff)} = 2.919$$

Mode 2: Common(++) $1.599689e+008 \text{ [m/s]} = 0.5336c \text{ Er(eff)} = 3.512$

2. Side-by-side Stripline

$$C (matrix) = \begin{bmatrix} 153.3 & -21.8 \\ -21.8 & 153.3 \end{bmatrix} \begin{bmatrix} \frac{pF}{m} \end{bmatrix}$$

$$L (matrix) = \begin{bmatrix} 318.5 & 45.3 \\ 45.3 & 318.5 \end{bmatrix} \begin{bmatrix} \frac{nH}{m} \end{bmatrix}$$

Propagation Speed: 1.445728e+008 [m/s] = 0.4822c Er(eff) = 4.300

3. Broadside Stripline

$$C (matrix) = \begin{bmatrix} 167,5 & -53,5 \\ -53,5 & 167,5 \end{bmatrix} \begin{bmatrix} \frac{pF}{m} \end{bmatrix}$$

$$L (matrix) = \begin{bmatrix} 318,0 & 101,4 \\ 101,4 & 318,0 \end{bmatrix} \begin{bmatrix} \frac{nH}{m} \end{bmatrix}$$

Propagation Speed: 1.445728e+008 [m/s] = 0.4822c Er(eff) = 4.300

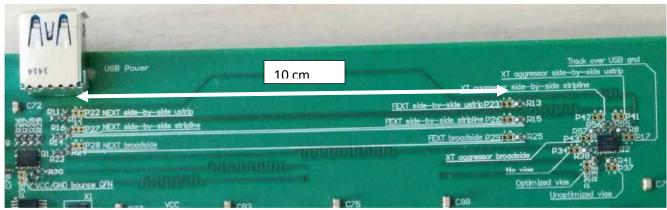


Figure 3: HW test board - Crosstalk test circuits.

At the top of the HW test-board (see Figure 1 and Figure 3) test circuits are designed and layout corresponding to the 3 cases.

Part 1 - Modelling and Simulations:

To perform the following task the HW PCB information (schematic, stack-up, real layout dimension), driver IC datasheet and IBIS model must be read and used.

Task 1.1

Draw the equivalent circuit model to be used to simulate the crosstalk in each of the 3 cases.

The model must include the driver circuit (linear model), package parasitics (simple model), transmission lines, and probe points, and receiver circuit (linear model).

Task 1.2

Find and estimate the values of the different parameters based on data from the HW test-board, PCB schematic, and the datasheet and IBIS model for the driver/receiver IC. Assume that the aggressor line is matched at the driver end (i.e. output impedance of the drive plus board-level series resistor is designed to match the characteristics impedance of the transmission line).

Task 1.3

For each of the transmission lines calculate the equivalent circuit model of the system (to be used in LTspice) of the coupled transmission lines. Assume T_{rise} is 500ps.

Task 1.4

From the datasheet - what are the minimum high input & output levels and the maximum low input & output levels (Hint: assume Vcc 3.3V +/-5%, and use the same max current load +/-12mA for both output low and high)

Min. output high level:mV
Max. output low level:mV
Max. input low level:mV
Min. input high level:mV
Based on these values, what are the noise margins in the low and high states?
Noise margin (Low state):mV
Noise margin (High state):mV

Task 1.5

Simulate (LTspice) for each of the transmission line configurations the circuit model (Driver 0-3.3V, $T_{rise} = 500ps$).

Document the voltage curves over time, at the driver and receiver ends of the aggressor line, and the near-end (NEXT) and far-end crosstalk (FEXT) at the victim line.

Determine the critical crosstalk level in the low state and high state (i.e. the two cases where quiet/victim line is low and high, respectively). The critical crosstalk level when the line is in a low (high) state is the maximum (minimum) voltage over the victim line due to crosstalk.

Side-by-side microstrip:

NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
Side-b	y-side stripline	<u>:</u>			
NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
Broads	side stripline:				
NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV

Is it acceptable (discuss)?

Remark - Here you should consider these cases:

- 1: the absolute values wrt max input low and min input high from task 1.4,
- 2: the delta noise pulses (difference between steady-state and critical levels) to the calculated noise margin in low and high states in task 1.4

Task 1.6

Determine crosstalk from the simple quantitative formulas in the textbook (remark – both the aggressor line and the victim line are not matched at the receiver ends:

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Side-b	<u>y-side microstri</u>	<u>p:</u>			
NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
Side-b	y-side stripline:				
NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
<u>Broad</u> :	side stripline:				
NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV

Does this match the simulation results in task 1.5?

Part 2 - Measurements.

Initial setup:

Connect coaxial probes to scope channels 1 and 2.

Task 2.1: Crosstalk side-by-side microstrip

Task 2.3: Crosstalk broadside stripline

NEXT:

Low state:

Adjust the supply voltage to 3.3V, measuring VCC using the VCC probe point (set probe to high impedance here).

Set both channels to 500hm, 21x attenuation (for measurement with 1000 Ohm series resistor and 500hm scope input. 1050/50=21). Why is this required?

For each measurement, remember to only enable the outputs that you need using the jumpers.

For each measurement, trigger the oscilloscope with the aggressor signal corresponding to the victim line that you are measuring.

<u>Place the probes with the correct polarity</u> else you may overload the oscilloscope USB output.

NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
	2.2: Crosstalk	side-by-side stripline			
	2.2: Crosstalk Low state:	side-by-side stripline Steady state level:	mV	Critical level:	mV
NEXT:		Steady state level:		Critical level:	
NEXT:	Low state:	Steady state level:			
NEXT: •	Low state:	Steady state level:	mV		mV

Steady state level: _____mV

Is it acceptable? (consider the same as the remark described in task 1.5)

Critical level: mV

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•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
Is it ac	cceptable? (co	nsider the same as the rer	nark descril	ped in task 1.5)	
	2.4: Vary supp	ly voltage hink crosstalk will change	with a 25%	reduction in VCC?	
	•	and measure crosstalk ag			
Side-b	y-side microstr	ip:			
NEXT:	,				
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
Side-b	y-side stripline	<u>:</u>			
NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	,		Critical level:	
•	High state:	Steady state level:	mV	Critical level:	mV
<u>Broads</u>	side stripline:				
NEXT:					
•	Low state:	Steady state level:	mV	Critical level:	mV
•	High state:	Steady state level:	mV	Critical level:	mV
FEXT:					
•	Low state:	Steady state level:		Critical level:	
•	High state:	Steady state level:	mV	Critical level:	mV

Is it acceptable? (consider the same as the remark described in task 1.5)

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Final lab-report

The final report for assignment 1 - Crosstalk must include answers to all the tasks above. Also, a section where the measurement results versus the simulations results are compared and discussed, including a discussion/analysis of potential reasons for mismatches (circuit models mismatches, the accuracy of measurements, error sources, etc.). Also, compare and discuss the results wrt the simple hand calculation formulas for NEXT and FEXT in the textbook. If possible/extra time, try to adjust simulation circuit models to obtain a better match.

The assignment report needs to be turned in to your group page in Brightspace. The deadline for submission of the report is 15th Dec. 2022.

One report per group as one PDF file named: "EHSD assignment 1 report - Crosstalk - Group X", where X corresponds to the group number (1 to 6) should be uploaded on Brightspace.

Revision history

Revison	Date	Who	Comment
1.0	28.10.2019	JKM	First release, 2019 version.
1.1	1.11.2020	JKM	second release
1.2	4.11.2021	HF	Third release
1.3	30.10.2023	HF	Forth release