ELECTRONIC HARDWARE SYSTEM DESIGN

INTRODUCTION TO ASSIGNMENT 1 AND MODELING HINTS

AARHUS UNIVERSITY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

EHSD
5 NOVEMBER 2024

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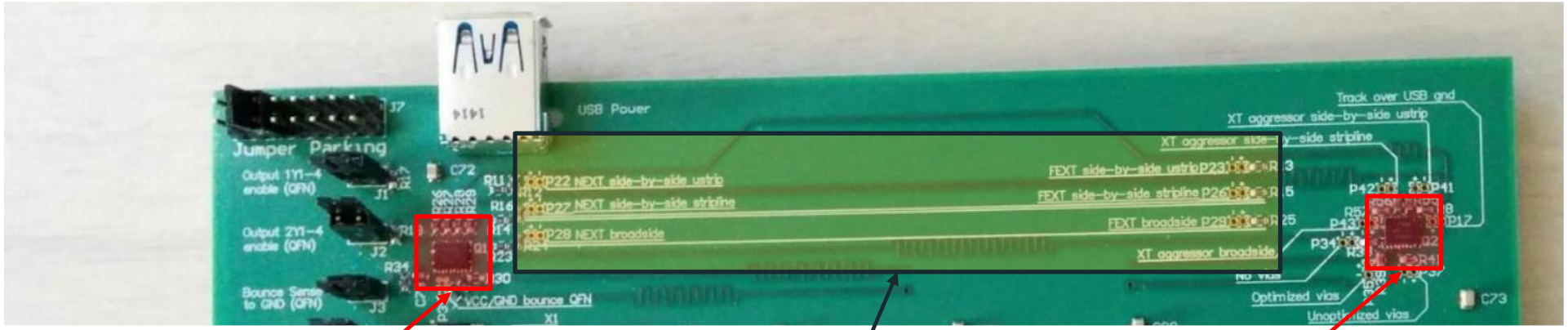
GENERAL INFORMATION

- Lab assignment 1 is about **Crosstalk effect** on real boards.
- Lab assignment 1 will be **graded** and its weight is **25% of the final grade**.
- The assignment will be completed **over three weeks** with
  1. Two 4hr **modeling and simulation** exercise days (two weeks)
  2. A 4hr **HW lab measurement exercise** day (third week) on the test-board.
- The **deadline** for submission of the assignment report – Crosstalk is **16th Dec. 2024**.
- **Decide about your group members**:
  - You should be divided into 6 groups **of up to 6 students**.
  - Please send me the names of your groupmates until **12th November**.

HW TEST BOARD

HW TEST BOARD MODELING



Driver

IC model: sn74alvc244
Package type: QFN

Datasheet – sn74alvc244-DriverReceiverIC.pdf

Receiver

IC model: sn74alvc244
Package type: QFN

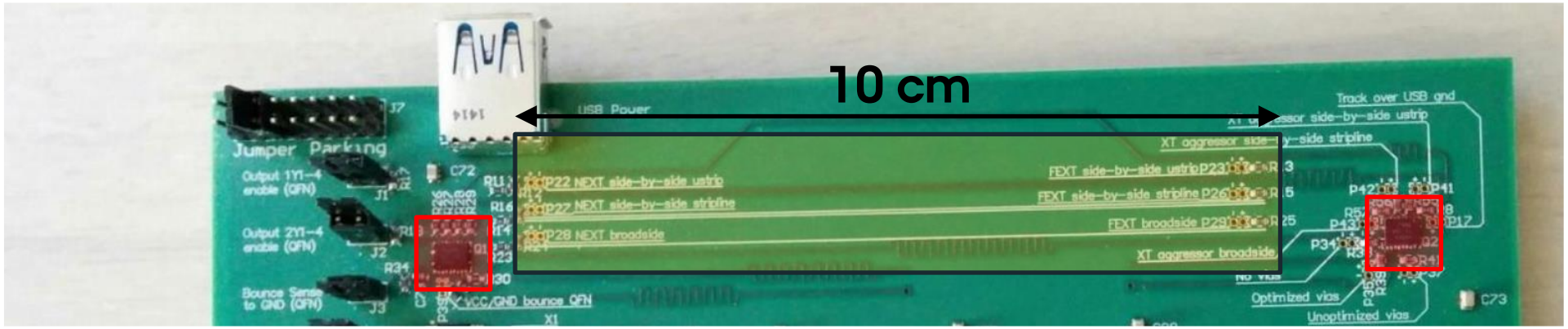
Datasheet – sn74alvc244-DriverReceiverIC.pdf

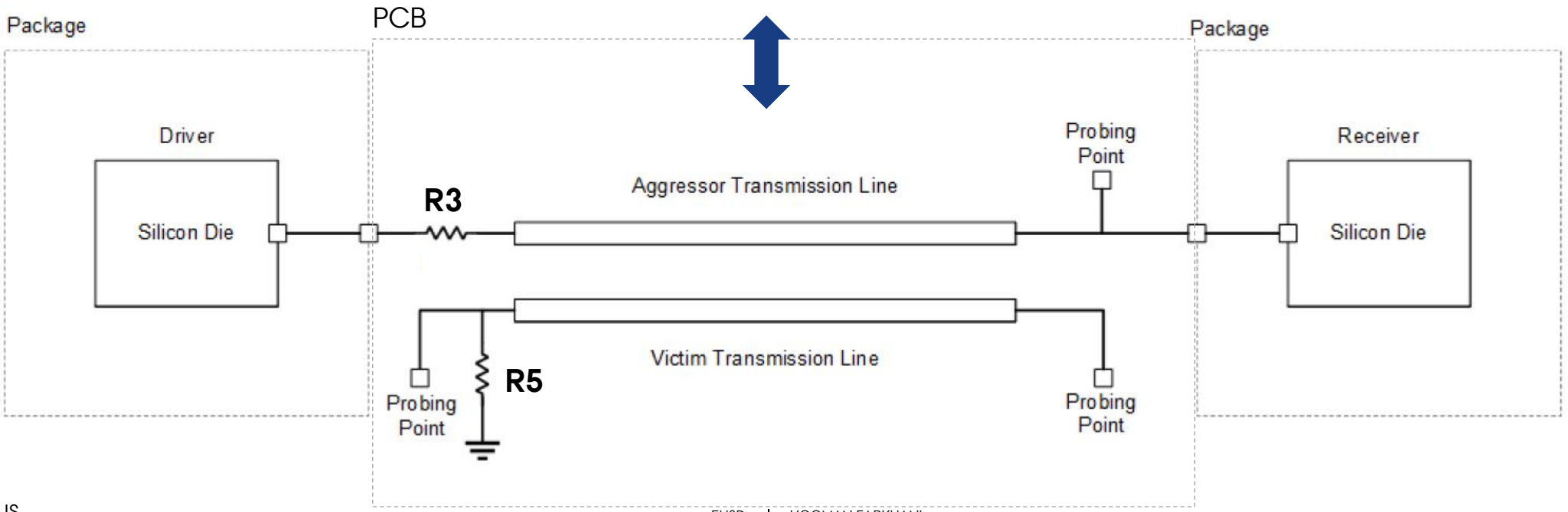
Transmission line:

- **Side by side Microstrip**
- **Side by side stripline**
- **Broad stripline**

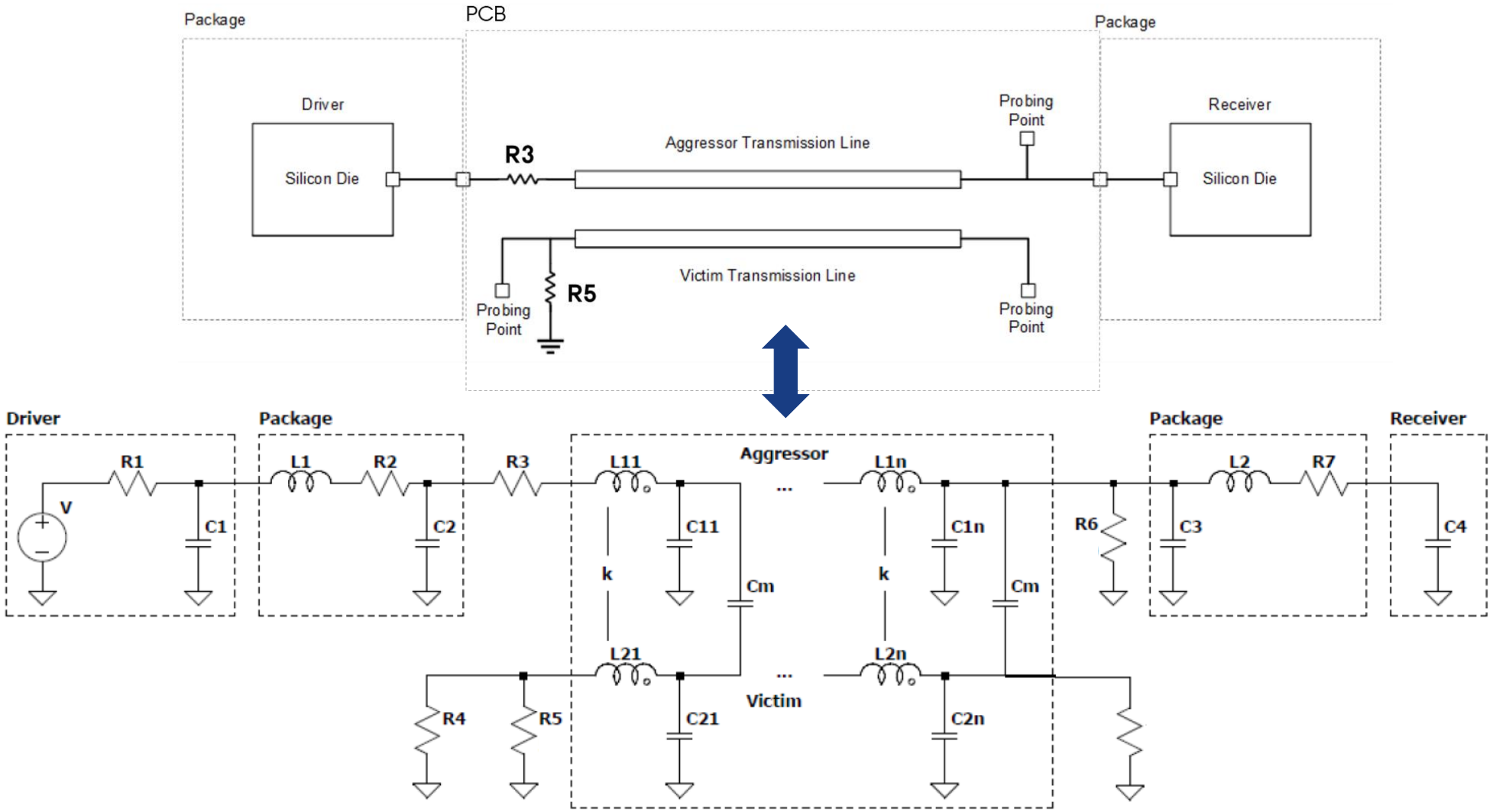
HW testboard
PCB_schematic DTU.pdf

HW TEST BOARD MODELING

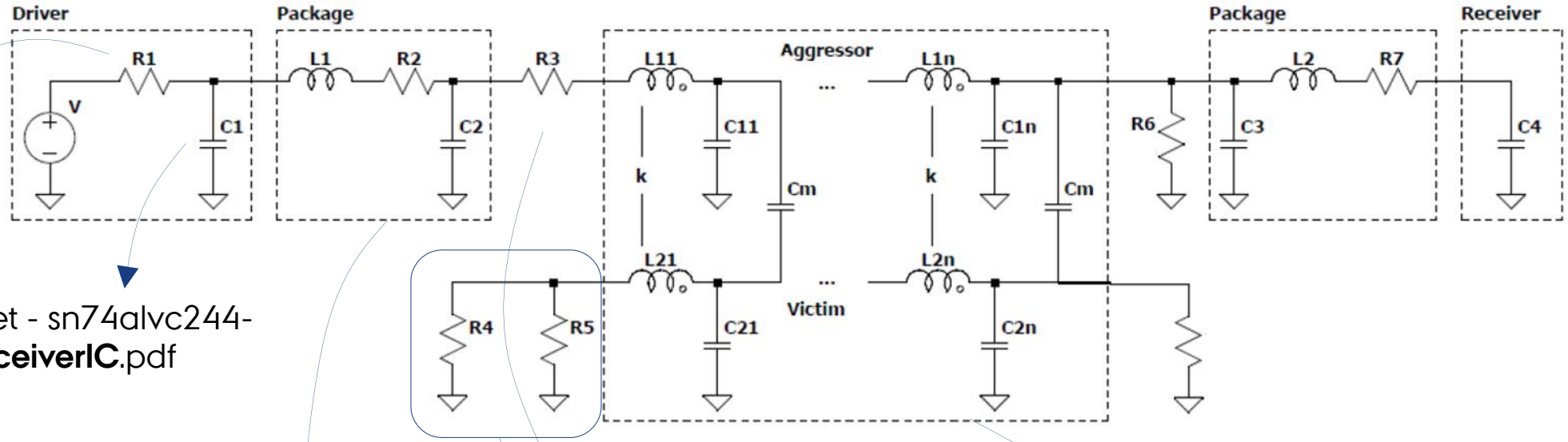




HW TEST BOARD MODELING



HW TEST BOARD MODELING



10.9 ohm

Datasheet - sn74alvc244-**DriverReceiverIC**.pdf

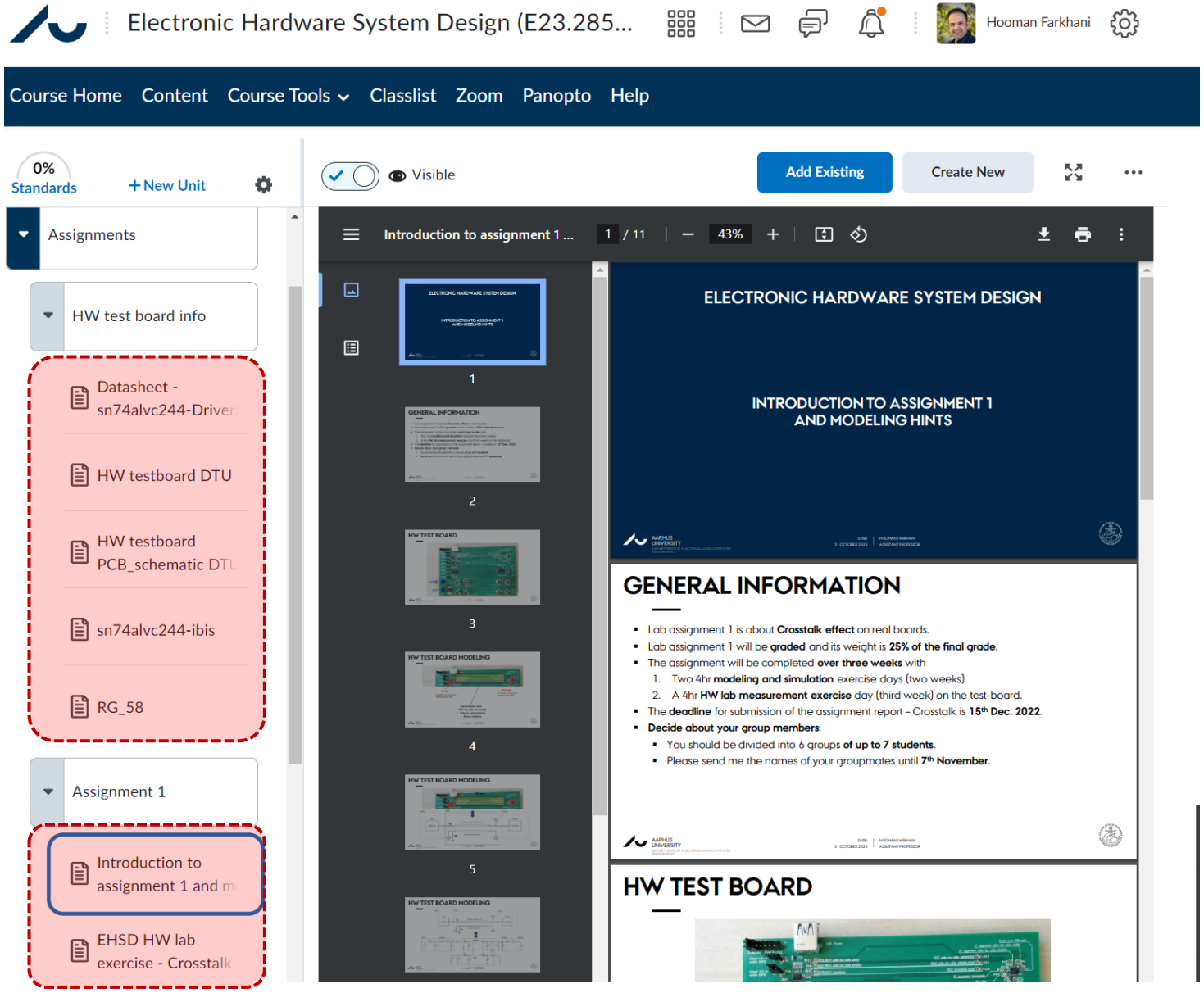
sn74alvc244-**ibis**.pdf

HW testboard PCB_**schematic DTU**.pdf

EHSD HW lab exercise - Crosstalk.pdf

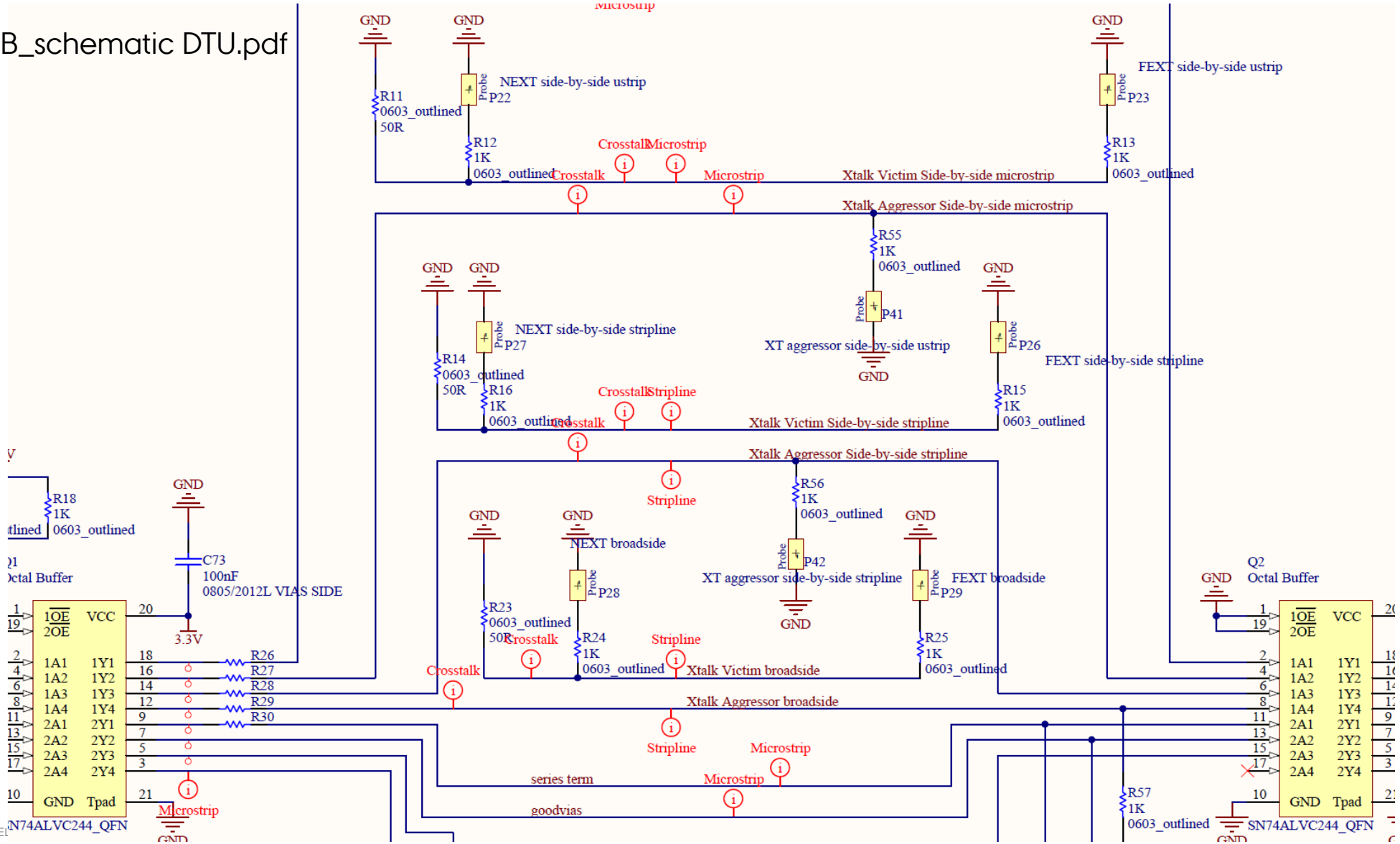
HW TEST BOARD MODELING

Required files can be found on Brightspace



HW TEST BOARD MODELING

HW testboard PCB_schematic DTU.pdf



CROSSTALK-INDUCED NOISE

Crosstalk magnitude and shape

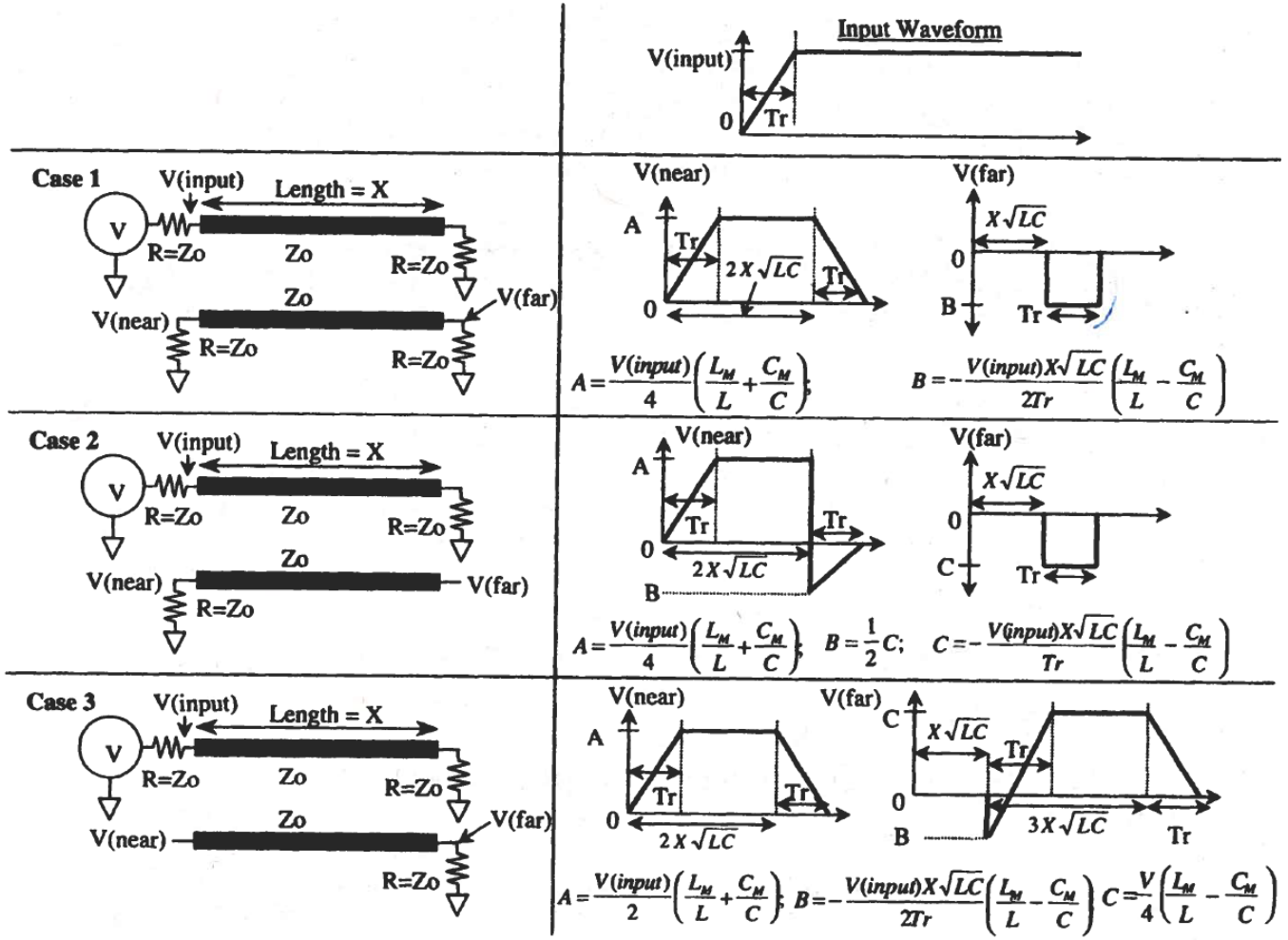
- Magnitude and shape of crosstalk depend on the amount of **coupling** and **termination scheme.**
- For hand-calculations the following formulas can be used (otherwise spice simulations) by the assumption that

$$TD = X\sqrt{LC} \geq 2T_r$$

- If non-ideal termination then the resultant crosstalk signal is calculated as

$$V_x = V_{crosstalk}\ (1 + \frac{R - Z_0}{R + Z_0})$$

where V_x is the adjusted crosstalk at the near-end/far-end, $V_{crosstalk}$ is the ideal termination crosstalk.



DeFalco, John, Reflection and crosstalk in logic circuit interconnections, IEEE Spectrum, 1970.

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