Introduction

This note describes the hands-on lab assignment 2 – GND/VCC bounce - to be completed as part of the graduate course "Electronic Hardware System Design".

In this assignment, we investigate the GND/VCC bounce (SSN/SSO) when several outputs switch simultaneously. We investigate the octal buffer chip (SN74ALVC244) package in two kinds of packaging options (see Figure 1):

- QNF
- SOIC

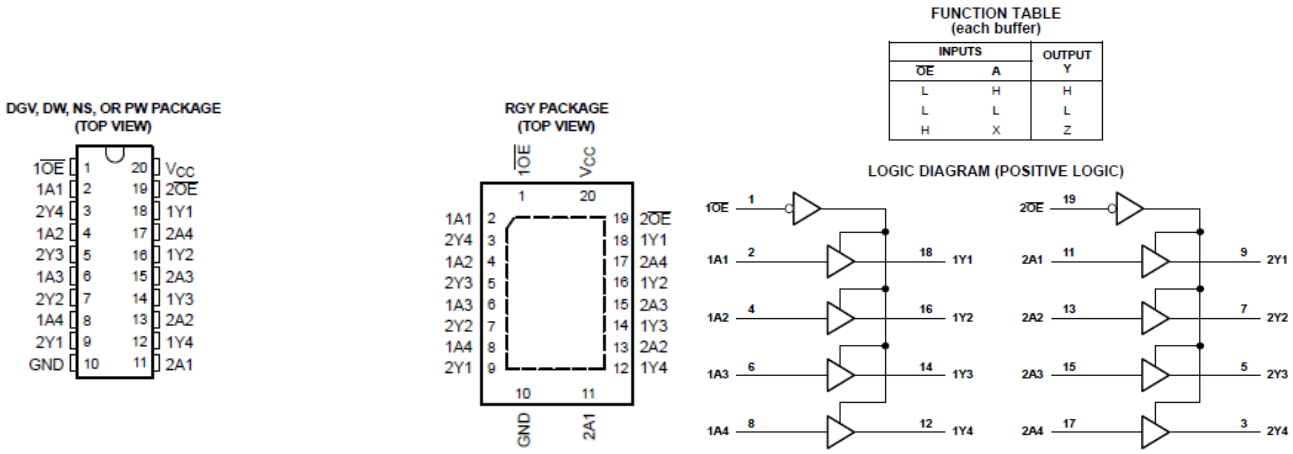

Figure 1: Buffer chip (SN74ALVC244) with two packing options. Left: SOIC package. Right: QFN package.

Lab assignment 2 will be graded and its weight is 25% of the final grade.

The exercise will be completed over two weeks with a 4-hour modeling and simulation exercise day (first week), and a 4-hour HW lab measurement exercise day (second week) on the test-board.

The deadline for submission of assignment 2 report – GND/VCC bounce is 23rd Dec. 2024.

The remaining part of the note describes:

1) The HW test board and info used for the exercise are on page 2.
2) The task plan for the modeling and simulation exercise (day 1) is on page 3.
3) The task plan for the measurement exercise (day 2) is on pages 4-6.
4) Guidelines for final lab report on page 7.

HW test board

The HW test board[1] is shown in Figure 2.

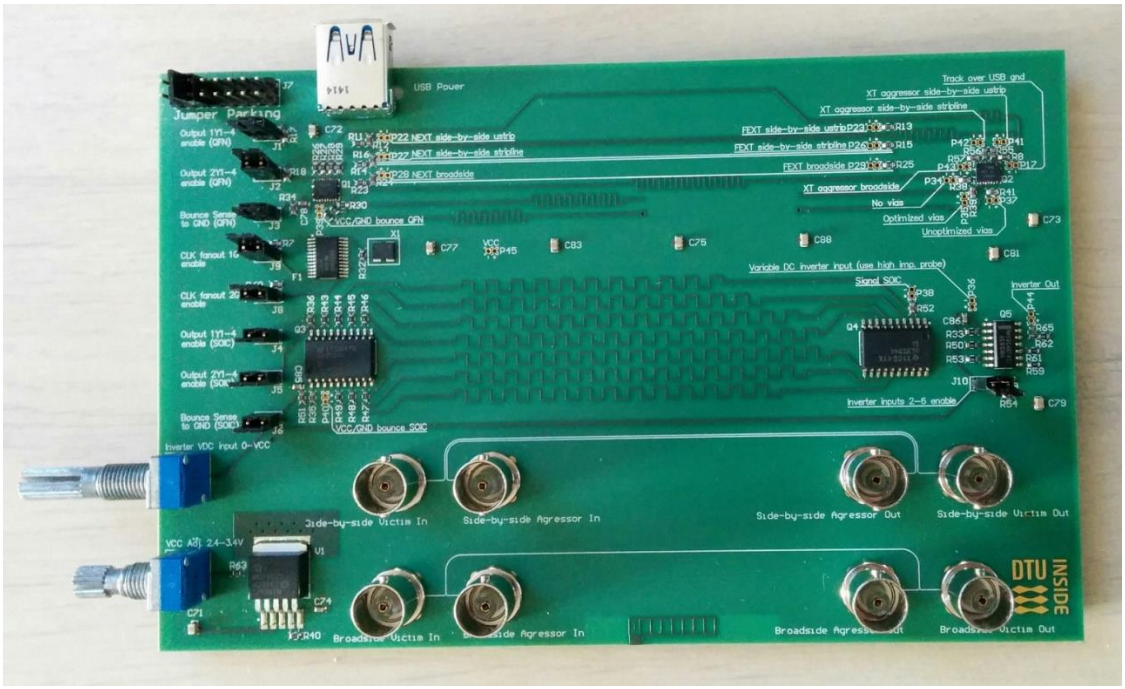

Figure 2: HW test-board

A detailed schematic of the test-board/PCB design (*DTU-ExercisePCB_schematic*), and datasheet of the driver IC's (*Datasheet - sn74alvc244-DriverReceiverIC*) is associated with the HW exercise note and located in the *HW test board info* folder in Brightspace under the *Assignments* area.

The PCB is powered by USB (use an oscilloscope USB port). The Supply voltage can be adjusted from 2.4V to 3.4V using the small potentiometer marked "VCC Adj. 2.4-3.4V". The current supply voltage can be measured on probe point P45 marked "VCC" near the middle of the board.

The exercise PCB includes SN74ALVC244 octal buffers in the QFN package and the SOIC package. The outputs of the buffers Q1(QFN) and Q3(SOIC) are enabled using the jumpers on the left.

The input signal for the buffers is supplied by a 20Mhz clock. A clock fanout chip distributes the clock signal and is enabled by two jumpers on the left.

By combining the enable settings of the clock fanout and the buffers, we can test ground/VCC bounce with either 7 outputs active, 3 outputs active or 1 output active.

To investigate the GND/VCC bounces the lab is divided into two exercises: a) Modelling and Simulation (day 1 - 4 hrs), and b) HW measuring (day 2 – 4 hrs).

[1] Test-board is designed and developed by DTU – Electro.

Day 1 – Modelling and Simulations:

To perform the following task the HW PCB information (schematic) and driver IC datasheet must be read and used.

Task 1.1
Draw a complete equivalent circuit model of the buffer chip including all the signals of the driver's outputs, GND and VCC supplies, the associated package parasitic's (capacitances and inductances) for each of the paths, and the (PCB) transmission lines including termination components.

Task 1.2
Determine from the IBIS model for the driver/receiver IC the inductances of the signal, GND and VCC pins for the QFN and SOIC packages.

Task 1.3
Simulate (LT-SPICE) for each of the package options in the circuit model when 1, 3 and 7 output buffer switches at the same time (Driver 0-3.3V, T_{rise} = 500ps). Consider, first how you model the CMOS output driver?

Document the voltage curves over time, at the driver end and receiver end of the transmission line of one of the switching outputs in each case (6 cases in total), including the quiet 8th output (not switching).

Determine:

QFN GND/VCC bounce, 1 output: **Switching line_____mV.** **Quiet line ..... mV**

QFN GND/VCC bounce, 3 outputs: **Switching line_____mV.** **Quiet line ..... mV**

QFN GND/VCC bounce, 7 outputs: **Switching line_____mV.** **Quiet line ..... mV**

SOIC GND/VCC bounce, 1 output: **Switching line_____mV.** **Quiet line ..... mV**

SOIC GND/VCC bounce, 3 outputs: **Switching line_____mV.** **Quiet line ..... mV**

SOIC GND/VCC bounce, 7 outputs: **Switching line_____mV.** **Quiet line ..... mV**

Acceptable? (related to noise margins)

Remark, what dc levels are the lines at? what happens if the lines levels (when stable) were at the Vout,low,Max, and Vout,high,Min values – still acceptable?.

Day 2 – Measurements.

Initial setup:
Connect coaxial probes to scope channels 1 and 2.

Adjust the supply voltage to 3.3V, measuring VCC with channel 1 probe using the VCC probe point (set probe to high impedance here).

Set channel 1 to 50Ohm, 1x attenuation.

Set channel 2 to 50Ohm, 21x attenuation (for measurement with 1000 Ohm series resistor and 50Ohm scope input. 1050/50=21).

Make sure that all jumpers on the left are in place, and that J10 in the middle is removed.

We are using scope channel 1 to measure the ground/VCC bounce – e.g. on P39("VCC/GND bounce QFN"). As you can see in the circuit diagram, we are measuring an output of the buffer that is NOT switching – this output is set to either high or low by a jumper.

Task 1: VCC/GND bounce 1 output
Remove jumper J1 ("Output 1y1-4 enable (QFN)"), J4 ("Output 1y1-4 enable (SOIC)") and J9 ("CLK fanout 1G enable").

Consult the circuit diagram – which channel (output) is now active on Driver QFN and Driver SOIC? Connect probe 2 to the active output probe point, and confirm the waveform is as expected. Use probe 2 as a trigger signal.

Confirm that jumper J3("Bounce sense to GND(QFN)") is in place. Connect probe 1 to P39("VCC/GND bounce QFN") and measure the ground bounce:
QFN GNDbounce, 1 output:_____mV

Remove jumper J3 and measure the VCC bounce:
QFN VCCbounce, 1 output:_____mV

Confirm that jumper J6("Bounce sense to GND(SOIC)") is in place. Connect probe 1 to P40 ("VCC/GND bounce SOIC") and measure the ground bounce:
SOIC GNDbounce, 1 output:_____mV

Remove jumper J6 and measure the VCC bounce:
SOIC VCCbounce, 1 output:_____mV

Acceptable?

Task 2: VCC/GND bounce 3 outputs

Place jumper J1 ("Output 1y1-4 enable (QFN)"), J4 ("Output 1y1-4 enable (SOIC)"). Ensure J9 ("CLK fanout 1G enable") is removed, and that J8("CLK fanout 2G enable") is in place.

Consult the circuit diagram – which channel (output) is now active on Driver QFN and Driver SOIC? Connect probe 2 to the active output probe point, and confirm the waveform is as expected. Use probe 2 as a trigger signal.

Confirm that jumper J3("Bounce sense to GND(QFN)") is in place. Connect probe 1 to P39("VCC/GND bounce QFN") and measure the ground bounce:

QFN GNDbounce, 3 outputs:_____mV

Remove jumper J3 and measure the VCC bounce:

QFN VCCbounce, 3 outputs:_____mV

Confirm that jumper J6("Bounce sense to GND(SOIC)") is in place. Connect probe 1 to P40 ("VCC/GND bounce SOIC") and measure the ground bounce:

SOIC GNDbounce, 3 outputs:_____mV

Remove jumper J6 and measure the VCC bounce:

SOIC VCCbounce, 3 outputs:_____mV

Acceptable?

Task 3: VCC/GND bounce 7 outputs

Place all the jumpers on the left. Confirm from the schematic, that all outputs should be enabled.

Connect probe 2 to the active output probe point, and confirm the waveform is as expected. Use probe 2 as a trigger signal.

Confirm that jumper J3("Bounce sense to GND(QFN)") is in place. Connect probe 1 to P39("VCC/GND bounce QFN") and measure the ground bounce:

QFN GNDbounce, 7 outputs:_____mV

Remove jumper J3 and measure the VCC bounce:

QFN VCCbounce, 7 outputs:_____mV

Confirm that jumper J6("Bounce sense to GND(SOIC)") is in place. Connect probe 1 to P40 ("VCC/GND bounce SOIC") and measure the ground bounce:

SOIC GNDbounce, 7 outputs:_____mV

Remove jumper J6 and measure the VCC bounce:

SOIC VCCbounce, 7 outputs:_____mV

Acceptable ?

Task 4: Inverter GND bounce self-oscillation

Q5 is a hex inverter, SN74ALVC04. The input is a DC voltage set by a potentiometer marked “Inverter VDC input 0-VCC”.

Confirm that jumper J10 is removed. Only one output on the inverter is active – vary the input using the potentiometer. Can you get the inverter output to oscillate?

Place jumper J10. All inverter outputs are active – vary the input using the potentiometer. Can you get the inverter output to oscillate? If so, why does it oscillate?

Final lab-report

The final lab report for the GND/VCC bounce lab must include answers to all the tasks above. You must discuss the results with respect to noise margins and VinL,max and VinH,min. Are they critical/acceptable? Also, a section where the measurement results versus the simulations results are compared and discussed, including a discussion/analysis of potential reasons for mismatches (circuit models mismatches, accuracy of measurements, etc.). If possible/extra time, try to adjust simulation circuit models to obtain a better match.

The lab report needs to be turned in via Brightspace.

One report per group as one PDF-file named: "EHSD lab report GND-VCC bounce - Group X" where X corresponds to the group number (1 to 6).

Revision history

Revision	Date	Who	Comment
1.0	10.11.2019	JKM	First release, 2019 version.
1.1	5.11.2019	HF	Second release.