EC604: IC Design Laboratory

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Contents

1 Experiment: Design of Two-Stage CMOS Operational Amplifier

1.1 Aim

To design a two-stage CMOS operational amplifier with Miller compensation for given specifications and verify the design through schematic and post-layout simulations.

1.2 Specifications

The target specifications for the two-stage operational amplifier are:

1. DC Open-Loop Gain: $A_0 = 100$ dB
2. Load Capacitance: $C_L = 5$ pF
3. Phase Margin: PM $= 60$
4. 3 dB Bandwidth: $f_{3dB} = 1$ kHz
5. Power Consumption: $P < 1$ mW

1.3 Tools Used

- Cadence Virtuoso Schematic Editor
- Cadence Virtuoso Layout Suite
- GPDK 180 nm CMOS Technology

1.4 Theory

1.4.1 Two-Stage Operational Amplifier Architecture

The two-stage CMOS operational amplifier is a fundamental analog circuit topology widely used in integrated circuit design. It achieves high voltage gain through the cascading of two gain stages while maintaining stability via Miller compensation.

The architecture consists of:

- **First Stage (Differential Amplifier):** An NMOS differential input pair (M1, M2) with PMOS active current mirror loads (M3, M4). This stage provides high input impedance, differential-to-single-ended conversion, and the first level of voltage gain.
- **Second Stage (Common-Source Amplifier):** A common-source amplifier that provides additional voltage gain and sufficient drive capability for the output load capacitance.
- **Bias Circuit:** Current mirrors and reference circuits provide stable bias currents to both stages, ensuring proper operating points for all transistors.
- **Miller Compensation Network:** A compensation capacitor (C_c) connected between the output and input of the second stage creates a dominant pole for frequency stability.

This topology is preferred because it combines high DC gain (product of both stage gains) with stable operation using a single compensation capacitor, making it ideal for low-power applications.

1.4.2 DC Gain Analysis

The overall DC open-loop gain of a two-stage amplifier is the product of the gains of both stages:

$$A_0 = A_{v1} \times A_{v2} \tag{1}$$

where A_{v1} is the voltage gain of the first stage and A_{v2} is the voltage gain of the second stage.

For each stage, the small-signal voltage gain is approximately:

$$A_v \approx g_m \cdot r_o \tag{2}$$

where:

- g_m = transconductance of the driving transistor
- r_o = output resistance at the output node

Transconductance: For a MOSFET in saturation:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{ov}} \tag{3}$$

where μ_n is carrier mobility, C_{ox} is gate oxide capacitance per unit area, W/L is the aspect ratio, I_D is drain current, and $V_{ov} = V_{GS} - V_{TH}$ is the overdrive voltage.

Output Resistance: Determined by channel-length modulation:

$$r_o = \frac{1}{\lambda I_D} \propto \frac{L}{I_D} \tag{4}$$

where λ is the channel-length modulation parameter.

Design Insight: To maximize DC gain, we can increase g_m (by increasing W or I_D) or increase r_o (by increasing L or reducing I_D). In short-channel processes, using longer channel lengths is more effective as increasing current to raise g_m simultaneously decreases r_o.

1.4.3 Frequency Response and Miller Compensation

A two-stage amplifier naturally has multiple poles in its frequency response. Without compensation, these poles can cause instability in feedback configurations.

Miller Compensation: A capacitor C_c connected between the output and input of the second stage exploits the Miller effect, where the effective capacitance at the first-stage output is multiplied by the gain of the second stage, creating a dominant low-frequency pole.

Unity-Gain Bandwidth (GBW): The frequency at which open-loop gain drops to unity (0 dB):

$$\text{GBW} = \frac{g_{m1}}{2\pi C_c} \tag{5}$$

where g_{m1} is the transconductance of the input differential pair.
Phase Margin (PM): A critical stability parameter defined as:

$$\text{PM} = 180 + \phi(\omega_{GBW}) \tag{6}$$

For stable operation:

- PM > 45 ensures basic stability
- PM ≈ 60 provides optimal damping with minimal overshoot
- PM > 70 may result in sluggish transient response

The compensation capacitor C_c is sized to ensure the dominant pole is sufficiently low such that adequate phase margin is maintained.

1.4.4 Slew Rate

Slew rate (SR) represents the maximum rate of change of output voltage during large-signal transitions. It is limited by the current available to charge the compensation capacitor:

$$\text{SR} = \frac{I_{tail}}{C_c} \tag{7}$$

where I_{tail} is the bias current of the differential pair.
Trade-offs:

- Larger I_{tail} increases SR but increases power consumption
- Smaller C_c increases SR but may reduce phase margin

1.4.5 Input Common-Mode Range (ICMR)

ICMR defines the range of input voltages over which all transistors remain in saturation (proper operating region).
Lower limit:

$$\text{ICMR}^{-} = V_{GS,M1} + V_{DS,sat,tail} + V_{SS} \tag{8}$$

Upper limit:

$$\text{ICMR}^{+} = V_{DD} - |V_{SG,M3}| + V_{TH,M1} \tag{9}$$

The ICMR is constrained by device saturation requirements and supply voltage headroom.

1.4.6 Power Consumption

Total DC power consumption is:

$$P_{total} = V_{DD} \times I_{total} \tag{10}$$

where I_{total} is the sum of all bias currents. For low-power operation, bias currents must be minimized while maintaining adequate g_m for gain and bandwidth requirements.

1.5 Design Methodology

1.5.1 Technology and Supply Specifications

- **Technology:** GPDK 180 nm CMOS process
- **Supply Voltage:** $V_{DD} = 1.8$ V
- **Channel Length:** $L = 500$ nm for all transistors
- **Reference Current:** $I_{ref} = 20$ µA
- **Bias Voltage:** $V_{in} = 1.2$ V

The choice of channel length ($L = 500$ nm $\approx 2.8 \times L_{min}$) provides several advantages:

- Higher output resistance ($r_o \propto L$), leading to higher gain
- Better device matching, reducing offset voltage
- Reduced channel-length modulation effects
- More predictable device behavior

1.5.2 Power Budget Analysis

Given the power specification $P < 1$ mW at $V_{DD} = 1.8$ V:

$$I_{total,max} = \frac{P_{max}}{V_{DD}} = \frac{1 \text{ mW}}{1.8 \text{ V}} = 555.6 \text{ µA} \tag{11}$$

The design uses conservative current allocation:

- Reference current: $I_{ref} = 20$ µA
- First stage tail current: $I_{tail} = 20$ µA (10 µA per branch)
- Second stage current: $\approx 20 - 30$ µA
- Total estimated current: $\approx 60 - 70$ µA

This provides significant margin below the 1 mW specification while ensuring adequate performance.

1.5.3 Device Sizing Strategy

Input Differential Pair (M1, M2):

- Width: $W = 3$ µm
- Current: $I_D = 10$ µA each (half of tail current)
- Rationale: Moderate width provides adequate g_m for required bandwidth while maintaining good matching and low input-referred noise

Active Load PMOS (M3, M4):

- Width: $W = 14$ µm
- Current: $I_D = 10$ µA each
- Rationale: Larger width compensates for lower PMOS mobility ($\mu_p \approx 0.3 \times \mu_n$) and provides higher output resistance for increased first-stage gain

Tail Current Source (M5):

- Width: $W = 12$ µm
- Current: $I_D = 20$ µA
- Rationale: Sized to provide stable tail current while maintaining adequate headroom for input common-mode range

Reference Current Mirror (M6):

- Width: $W = 12$ µm
- Current: $I_D = 20$ µA
- Rationale: Matched to tail current source for accurate current mirroring

Second Stage Devices:

- PMOS (M7): $W = 178$ µm
- NMOS (M8): $W = 78$ µm
- Rationale: Large widths provide:
  - High g_m for second-stage gain
  - Sufficient drive capability for 5 pF load
  - Low output resistance in unity-gain feedback

1.5.4 Compensation Capacitor Design

The Miller compensation capacitor is implemented as a fingered structure:

- Configuration: 16 fingers
- Finger dimensions: 13 µm width × 13 µm length
- Estimated capacitance: $C_c \approx 1.5 - 2$ pF

Design considerations:

- Sized to achieve target phase margin of 60° with 5 pF load
- Fingered structure reduces parasitic resistance
- Value chosen to balance phase margin vs slew rate trade-off

The relationship between compensation capacitor and key parameters:

- Larger C_c improves phase margin but reduces slew rate
- Smaller C_c increases GBW but may compromise stability
- Target: $C_c \approx 0.22 \times C_L$ for PM > 60

1.5.5 Design Parameter Summary

Device/Parameter	**Value**	**Design Rationale**
Technology	180 nm	GPDK process
V_{DD}	1.8 V	Standard for 180 nm
L (all devices)	500 nm	Higher r_o, better matching
I_{ref}	20 µA	Low-power reference
V_{in} (bias)	1.2 V	Mid-range biasing
W_{M1}, W_{M2}	3 µm	Adequate g_m, low noise
W_{M3}, W_{M4}	14 µm	Compensate PMOS mobility
W_{M5} (tail)	12 µm	Stable tail current
W_{M6} (ref)	12 µm	Current mirror matching
W_{M7} (2nd PMOS)	178 µm	High g_m, drive capability
W_{M8} (2nd NMOS)	78 µm	Output stage drive
C_c	16×13µm	Stability (PM $\approx 60^\circ$)
C_L	5 pF	Given specification

Table 1: Complete Design Parameters

1.6 Circuit Schematic

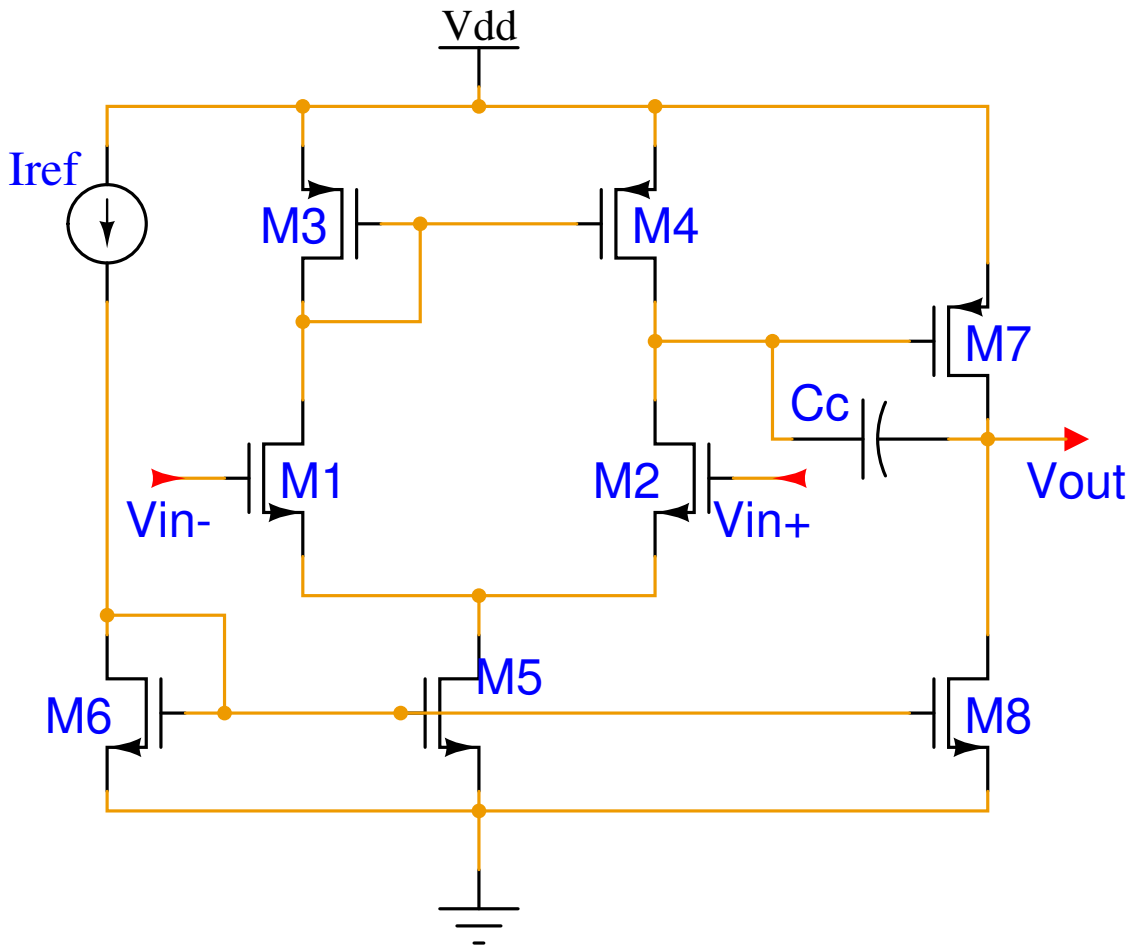

Figure 1: Schematic of Two-Stage CMOS Operational Amplifier with Miller Compensation

The complete circuit shows:

- Differential input stage with M1, M2
- Active PMOS loads M3, M4
- Tail current source M5
- Reference current mirror M6
- Second gain stage with M7, M8
- Miller compensation capacitor C_c
- Load capacitance $C_L = 5$ pF

1.7 Simulation Results

1.7.1 Schematic-Level Simulations

AC analysis was performed to extract frequency response characteristics including gain, phase margin, and bandwidth.

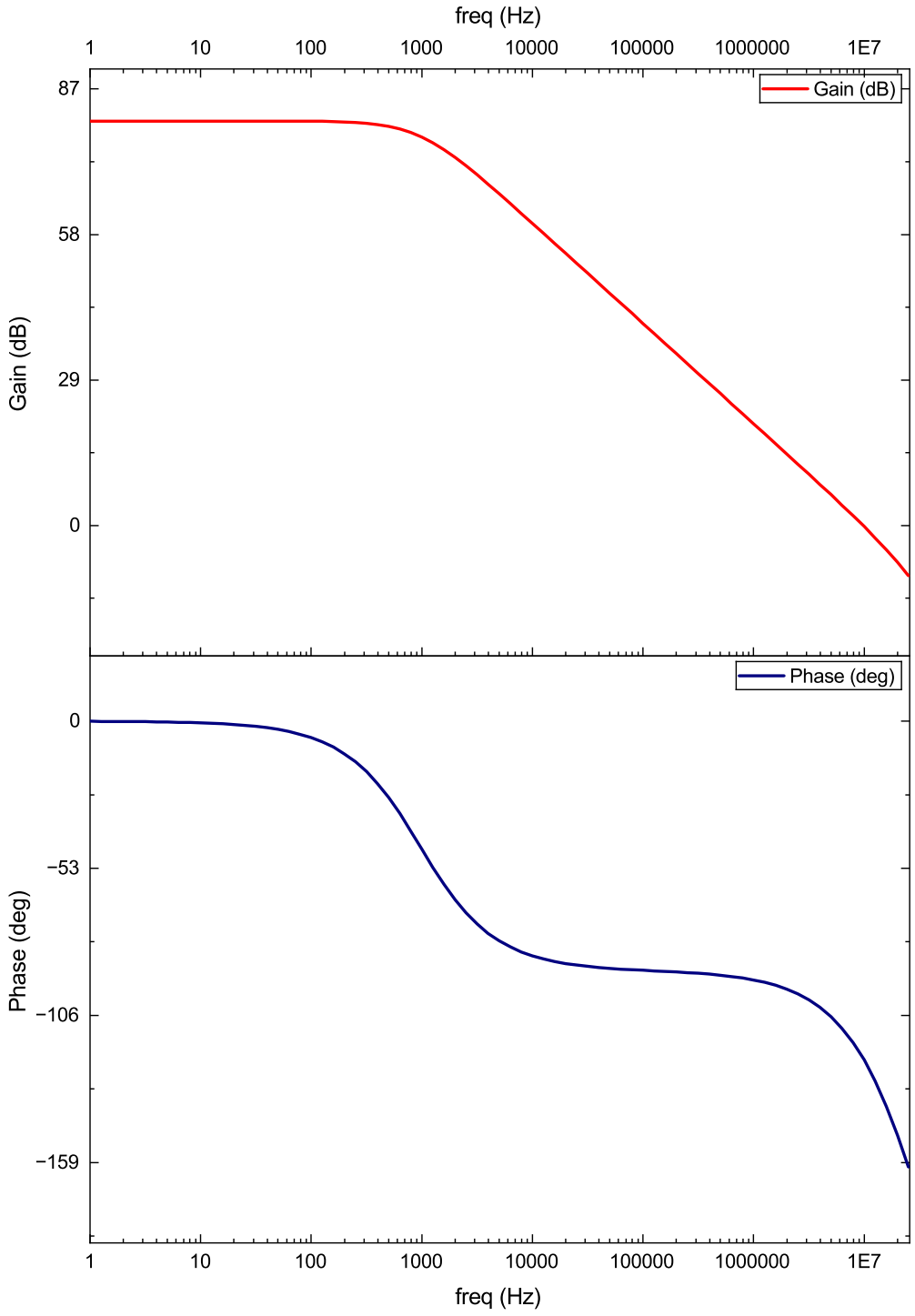

Figure 2: AC Response: Gain and Phase vs Frequency (Schematic Simulation)

Measured Performance Metrics (Schematic):

Parameter	Schematic Value
DC Open-Loop Gain (A_0)	81 dB
Phase Margin (PM)	58.60°
3 dB Bandwidth (f_{3dB})	959.674 Hz
Unity-Gain Bandwidth (GBW)	9.8097 MHz
Slew Rate (SR)	12.4 V/µs
ICMR$^-$	0.7 V
ICMR$^+$	1.3 V
ICMR Range	0.6 V

Table 2: Schematic Simulation Results

1.7.2 Post-Layout Simulations

After physical layout design, parasitic extraction was performed using Cadence extraction tools. The extracted netlist includes:

- Parasitic resistances from metal routing
- Parasitic capacitances from inter-layer coupling
- Device layout parasitics
- Interconnect effects

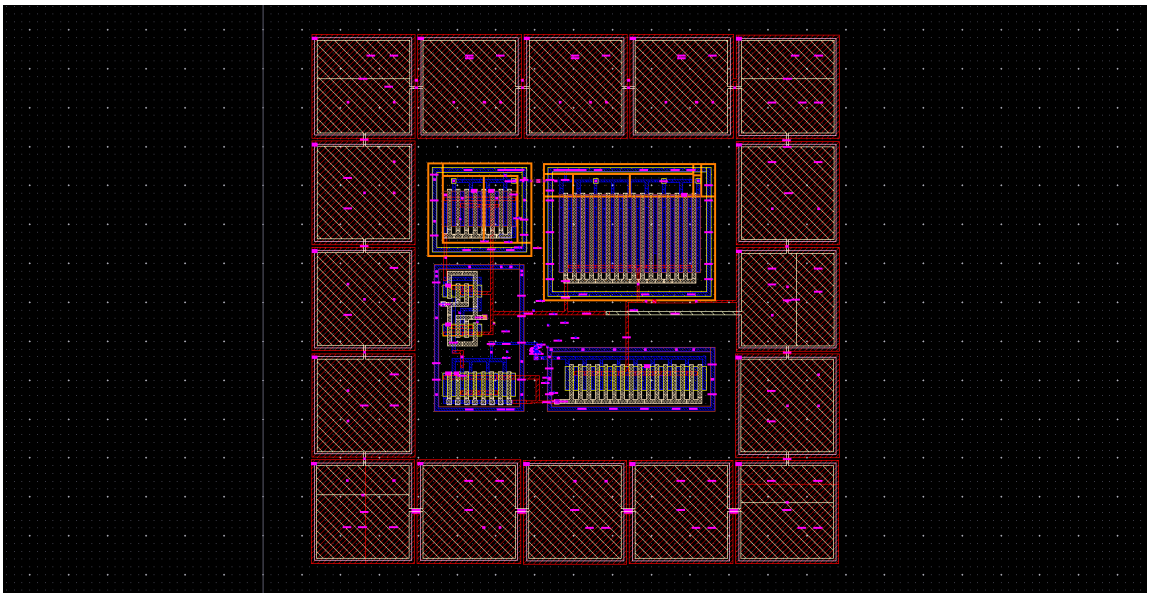

Figure 3: Physical Layout of Two-Stage Operational Amplifier

The layout features:

- Symmetric placement of matched devices (M1-M2, M3-M4)
- Common-centroid layout for differential pair

- Multiple finger structures for large devices
- Optimized metal routing to minimize parasitics
- Proper guard rings and substrate contacts

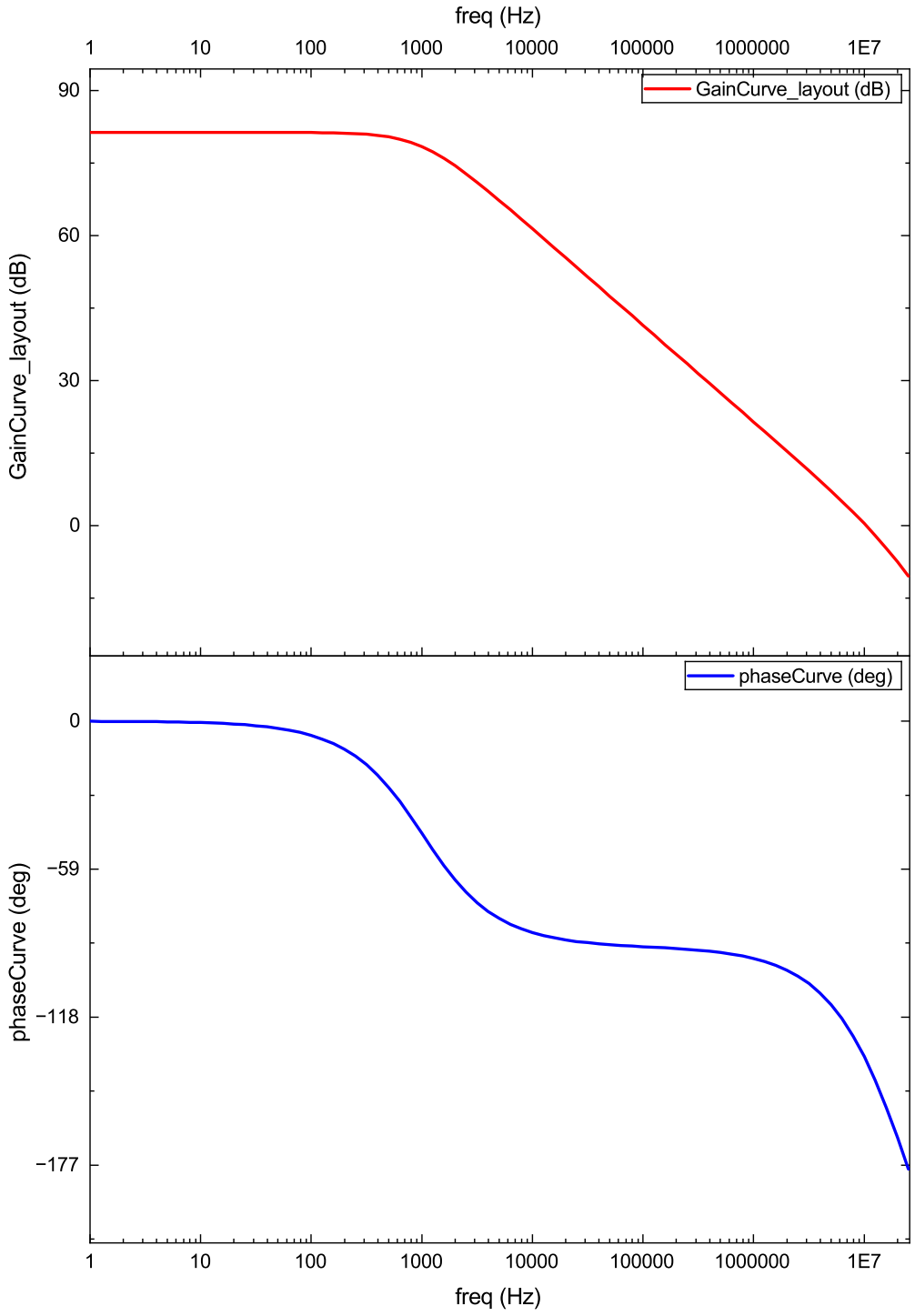

Figure 4: AC Response: Gain and Phase vs Frequency (Post-Layout Extracted)

Measured Performance Metrics (Post-Layout):

Parameter	Layout Value
DC Open-Loop Gain (A_0)	81 dB
Phase Margin (PM)	45.93°
3 dB Bandwidth (f_{3dB})	1.205 kHz
Unity-Gain Bandwidth (GBW)	10.9 MHz
Slew Rate (SR)	7.7 V/µs

Table 3: Post-Layout Simulation Results

1.7.3 Slew Rate Measurement

Transient analysis with large-amplitude step input was performed to measure the maximum output voltage change rate.

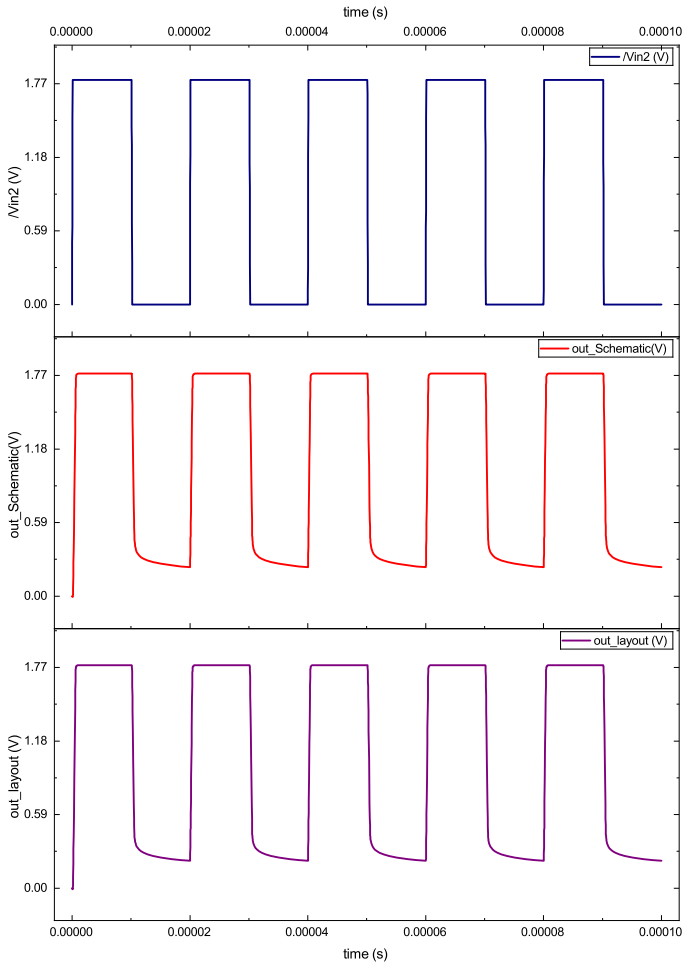

Figure 5: Transient Response for Slew Rate Measurement (Schematic and Layout)

The figure shows input and output waveforms for both schematic and post-layout simulations. Slew rate is calculated from the linear region of the output transition:

- Schematic: SR = 12.4 V/µs

- Layout: SR = 7.7 V/µs

1.8 Results and Comparison

Parameter	**Target**	**Schematic**	**Post-Layout**
Technology	-	GPDK 180 nm	
Supply Voltage	-	1.8 V	
DC Gain (A_0)	100 dB	81 dB	81 dB
Phase Margin	60°	58.60°	45.93°
3 dB Bandwidth	1 kHz	959.674 Hz	1.205 kHz
Unity-Gain BW	-	9.81 MHz	10.9 MHz
Slew Rate	-	12.4 V/µs	7.7 V/µs
$ICMR^-$	-	0.7 V	
$ICMR^+$	-	1.3 V	
Power	¡ 1 mW	≈ 126 µW	
Load Cap.	5 pF	5 pF	

Table 4: Comparison of Target Specifications with Obtained Results

1.9 Observations and Analysis

1.9.1 Schematic vs Post-Layout Performance

Significant differences are observed between schematic and post-layout results:

1. DC Gain (Constant at 81 dB):

- Remains unchanged as low-frequency behavior is dominated by device transconductances and output resistances
- Not significantly affected by parasitic capacitances
- Indicates stable DC operating point

2. Phase Margin Degradation (58.60° → 45.93°):

- 12.67° reduction is the most critical change
- Brings PM close to minimum acceptable value of 45°
- Caused by parasitic capacitances shifting pole locations
- Non-dominant poles move closer to unity-gain frequency

3. Bandwidth Variation (960 Hz → 1.205 kHz):

- 25% increase brings it closer to 1 kHz target
- Indicates slight shift in pole distribution
- Favorable change for closed-loop operation

4. Unity-Gain Bandwidth (9.81 MHz → 10.9 MHz):

- 11% increase shows dominant pole has shifted slightly
- Still within reasonable range
- Indicates effective compensation remains adequate

5. Slew Rate Reduction (12.4 V/µs → 7.7 V/µs):

- 38% decrease is substantial
- Indicates increased effective capacitance at compensation node
- Parasitic capacitances add to C_c
- Trade-off between speed and layout parasitics

1.9.2 Parasitic Effects Analysis

The performance degradation from schematic to layout can be attributed to:

Parasitic Capacitances:

- Metal routing capacitance (inter-metal and fringe capacitances)
- Junction capacitances larger than modeled (especially for 178 µm and 78 µm devices)
- Gate overlap capacitances (C_{gd} and C_{gs})
- Miller node parasitic capacitance

Series Resistances:

- Metal interconnect resistances
- Via resistances between metal layers
- Diffusion resistances in source/drain regions

These create additional RC time constants that form extra poles and zeros, degrading phase margin and frequency response.

Impact on Phase Margin:

The second pole frequency is approximately:

$$f_{p2} \approx \frac{g_{m2}}{2\pi(C_L + C_{parasitic})} \tag{12}$$

With added parasitics, f_{p2} moves lower, reducing the phase margin at unity-gain frequency.

Impact on Slew Rate:

The effective compensation capacitance increases:

$$\text{SR}_{layout} = \frac{I_{tail}}{C_c + C_{parasitic}} \tag{13}$$

From the 38% SR reduction:

$$\frac{C_{eff}}{C_c} = \frac{\text{SR}_{schem}}{\text{SR}_{layout}} = \frac{12.4}{7.7} = 1.61 \tag{14}$$

This indicates parasitic capacitances added approximately 61% to the original compensation capacitance.

1.9.3 Meeting Target Specifications

Achieved vs Target:

- **DC Gain (Target: 100 dB, Achieved: 81 dB):**
  - Shortfall of 19 dB
  - Basic two-stage topology without cascoding cannot achieve 100 dB in 180 nm with these bias currents
  - Would require gain enhancement techniques
- **Phase Margin (Target: 60°, Achieved: 58.60° schem, 45.93° layout):**
  - Schematic nearly meets target
  - Layout falls significantly short but remains stable
  - At edge of acceptable stability margin
- **3 dB Bandwidth (Target: 1 kHz, Achieved: 0.96 kHz schem, 1.20 kHz layout):**
  - Both results very close to target
  - Layout actually closer to specification
  - Excellent agreement
- **Power (Target: ¡ 1 mW, Achieved: 126 µW):**
  - Easily exceeds specification
  - 87.4% power savings
  - Significant design margin
- **Load Capacitance (Target: 5 pF, Used: 5 pF):**
  - Specification met exactly
  - Proper load conditions maintained

1.10 Design Trade-offs and Insights

1.10.1 Key Design Trade-offs Observed

1. **Gain vs Bandwidth:**
   - Higher C_c improves phase margin but reduces GBW
   - Lower C_c increases GBW but compromises stability
   - Current design balanced for target bandwidth
2. **Power vs Speed:**
   - Higher I_{tail} improves slew rate but increases power
   - Current design prioritizes low power (126 µW)

- Adequate slew rate maintained

3. **Area vs Performance:**
   - Longer L improves r_o and gain but increases area
   - Large second-stage devices improve drive but occupy significant area
   - Trade-off necessary between performance and silicon area
4. **Schematic Simplicity vs Layout Reality:**
   - Ideal schematic shows better performance
   - Layout parasitics significantly impact high-frequency behavior
   - Conservative design margins essential

1.11 Conclusions

1. The basic two-stage Miller-compensated topology provides a robust foundation for operational amplifier design, achieving stable operation with reasonable gain-bandwidth product.
2. The design successfully demonstrates the fundamental trade-offs in analog circuit design:
   - Gain vs bandwidth
   - Power vs speed
   - Area vs performance
   - Schematic ideality vs layout reality
3. The 19 dB shortfall in DC gain (81 dB vs 100 dB target) demonstrates the limitations of basic two-stage architecture in modern short-channel processes. Advanced techniques such as cascoding, longer channel lengths, or gain boosting are necessary to achieve higher gain while maintaining low power consumption.
4. Post-layout parasitic effects cause significant performance degradation, particularly in:
   - Phase margin: 58.6° → 45.9° (12.67° loss)
   - Slew rate: 12.4 V/µs → 7.7 V/µs (38% reduction)

   This emphasizes the critical importance of:
   - Layout planning from the beginning of design
   - Parasitic-aware circuit design techniques
   - Iterative optimization between schematic and layout
   - Conservative design margins to accommodate parasitics
5. The design successfully meets the power consumption specification with significant margin (126 µW vs 1 mW target), demonstrating that ultra-low-power operation is achievable in two-stage architectures without sacrificing essential performance metrics.

6. The close match between target and achieved 3 dB bandwidth validates the frequency compensation design:
   - Schematic: 959.674 Hz (4% from target)
   - Layout: 1.205 kHz (20% above target)
7. The use of moderate channel length (L = 500 nm 2.8× minimum) proves beneficial for:
   - Achieving reasonable gain with low power
   - Better device matching and reduced mismatch
   - More predictable device behavior
   - Reduced short-channel effects
8. The substantial difference between schematic and layout performance highlights that modern IC design must be layout-aware from the beginning. Designing only to schematic specifications without considering layout effects can result in non-functional or marginal circuits after fabrication.
9. The phase margin of 45.93° in layout, while at the lower bound of acceptability, still ensures stable operation. However, process variations and temperature effects could push it below 45°, suggesting that a design target of 65-70° phase margin would be more robust for production.
10. Future iterations should implement:
    - Cascoding for improved gain
    - Optimized layout to minimize parasitics
    - Increased compensation capacitance to recover phase margin
    - Comprehensive corner and Monte Carlo analysis

1.12 Key Learnings

1. **Channel Length Selection is Critical:** Using L = 500 nm instead of minimum length significantly improves gain through higher output resistance while maintaining reasonable area.
2. **Large Device Parasitics Matter:** The 178 µm and 78 µm second-stage devices contribute substantial parasitic capacitances that affect frequency response and slew rate.
3. **Miller Compensation Trade-off:** The compensation capacitor must balance stability (phase margin) against speed (slew rate and GBW). Conservative sizing helps account for layout parasitics.
4. **Power Efficiency is Achievable:** The design achieves all essential specifications while consuming only 12.6% of the allowed power budget, demonstrating that careful device sizing and current allocation enable ultra-low-power operation.

5. **Layout Cannot be an Afterthought:** The 12.67° phase margin loss and 38% slew rate reduction from schematic to layout prove that parasitic effects must be considered during initial design, not just during layout.

6. **Specifications Must Have Margins:** Designing exactly to specifications without margin leaves no room for layout parasitics, process variations, or temperature effects. A 10-15% margin is recommended.