Design of a Low Dropout Regulator

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***Abstract*— A 130 nM CMOS low-dropout (LDO) Voltage Regulator is proposed in this paper for battery-operated measurement system. With the quiescent current of only 7 uA, it supplies a 1.8 V output voltage from a 3.6 V to 1.9 V battery input voltage, featuring a line regulation of 0.00 647 mV/V and a load regulation of 0.0024 mV/mA for a load current of 50 mA over 100 pF load.**

***Keywords* — Voltage Regulator, Low Drop-Out Regulator**

Reference Circuit Details

Fig. 1 shows the classical topology of a CMOS LDO regulator. It consists of a voltage reference Vref; an error amplifier (EA); a PMOS pass transistor as the pass element between the battery-voltage VBAT and the stable output voltage Vout; and a resistive feedback network Rfb1 – Rfb2. Any variation of the input voltage VBAT or the load current ILoad is sampled by the feedback network at Vfb; the error amplifier (EA) compares Vfb with the voltage reference Vref, generating a signal that is continuously driving the pass transistor gate to render a constant output voltage expressed as

$$V_{out} = [1+ R_{fb1}/R_{fb2}]\ V_{ref}$$

Fig. 2. The voltage reference Vref is an external bandgap reference which delivers 1.2 V. To keep bound the power consumption, a quiescent current budget of 6 µA is set as a design specification: 2 µA for the EA and 4 µA through the feedback network when ILoad = 0 mA. The size of the PMOS pass transistor results (W/L) = (9480 µm / 0.34 µm) to keep the transistor in saturation for the maximum current capability ILoad = 50 mA preserving a drop-out voltage –defined as the minimum voltage across the pass device to maintain regulation– of 300 mV.

Minimum transistor length (Lmin = 0.34 µm for 3.3 V MOS transistors) is used to minimize the corresponding parasitic capacitance at the gate of the pass transistor, which is CPASS = 12 pF (for ILoad = 0 mA) and 20 pF (for ILoad = 50 mA). Assuming a static current of 4 µA through the PMOS pass transistor when ILoad = 0 mA, IRfb = Vout / (Rfb1 + Rfb2) = 4 µA; with Vref = 1.2 V and for a 1.8 V output voltage.

The values of the feedback resistors result Rfb1 = 150 kΩ and Rfb2 = 300 kΩ. These resistances are implemented as active resistances using three identical PMOS transistors in diode configuration to optimize the area consumption; this choice results in a reduction by a factor 20 with respect to the use of the high resistive polysilicon layer (HRP) of the technology (Rsquare = 1039 Ω / square, W = 1 µm, L = 415 µm). For the error amplifier, a large low-frequency gain is desired to obtain good line regulation, load regulations and power supply rejection (PSR).

The error amplifier is hence a telescopic NMOS-input differential pair, which provides a gain comparable to a two-stage EA but with a simple single stage architecture, thus optimizing the power consumption and relaxing stability.

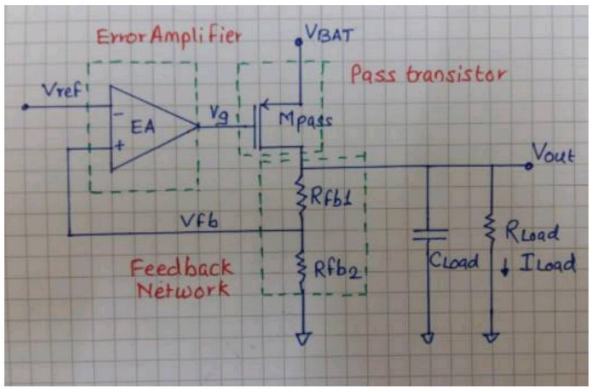

Fig1: CMOS LDO Regulator

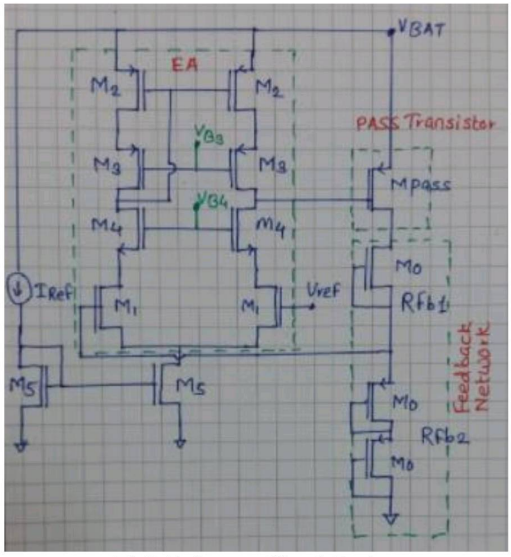

Fig2: Reference Circuit Design

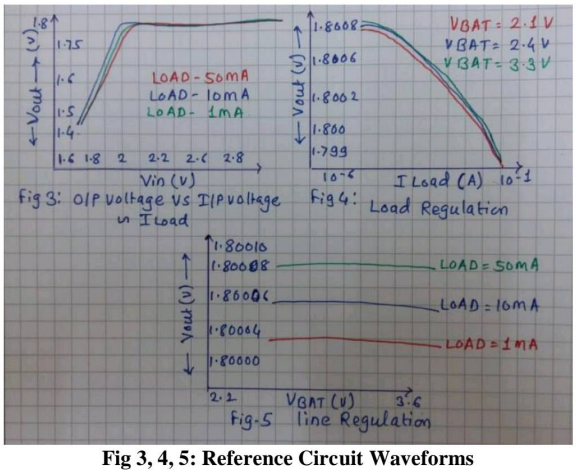

Fig 3, 4, 5: Reference Circuit Waveforms

REFRENCE

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