ECEN 5823-001
Internet of Things Embedded Firmware

Lecture #18

25 October 2018

Be Boulder.

University of Colorado Boulder

Agenda

- Class Announcements
- Memory for embedded applications

Class Announcements

- Quiz 8 due on Sunday, October 28th, at 11:59pm
  - This may be pushed to Wednesday, October 31st depending on how far I get in lecture on Thursday
- Course Project Proposal due Sunday, October 28th, at 11:59pm
- Based on class grades after mid-term, at this time no curve is planned

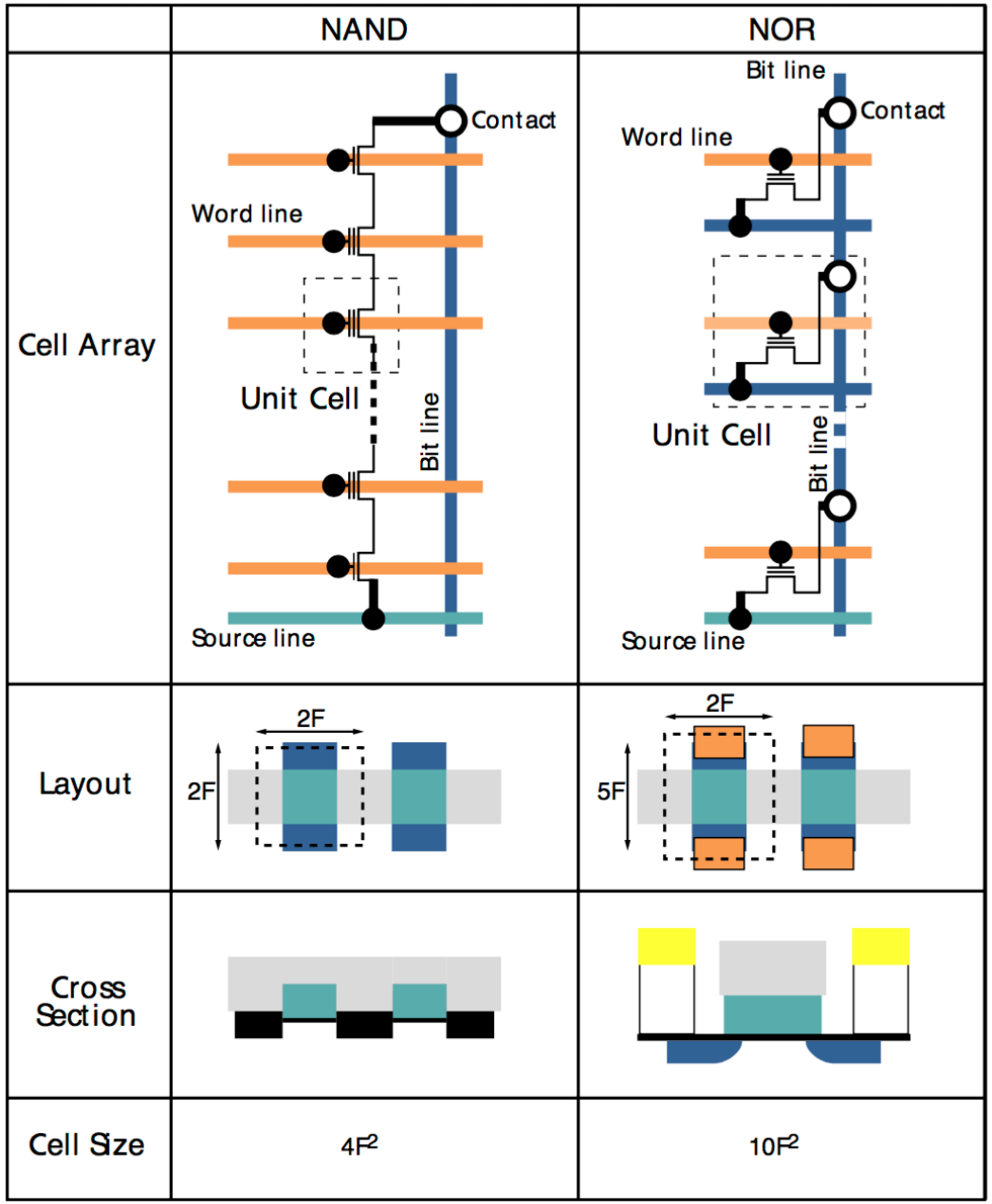
Differences between NOR and NAND Flash

- NOR
  - Quick random access to any memory location
  - 100% known good bits for the life of the part
  - Good for direct code execution
  - Fast program and erase cycles
  - Density: 1Mbit – 2Gbit
  - Larger cell and more expensive

- NAND
  - Slow initial access read access, then faster sequential reads
  - 98% bits are good when new and additional bits fail over time (ECC is required)
  - Good for data storage
  - Slower program and erase cycles
  - Density: 128Mbit – 1Tbit
  - Smaller cell and less expensive
  - SLC, MLC, TLC, 3d technologies

FLASH cell construction

- F = feature size
- NOR is 2.5x NAND cell size
- NAND Flash is very similar to a hard-disk drive. It is sector-based (page-based) and well suited for storage of sequential data. Random access can be achieved at the system level by shadowing the data to RAM, requiring RAM storage.

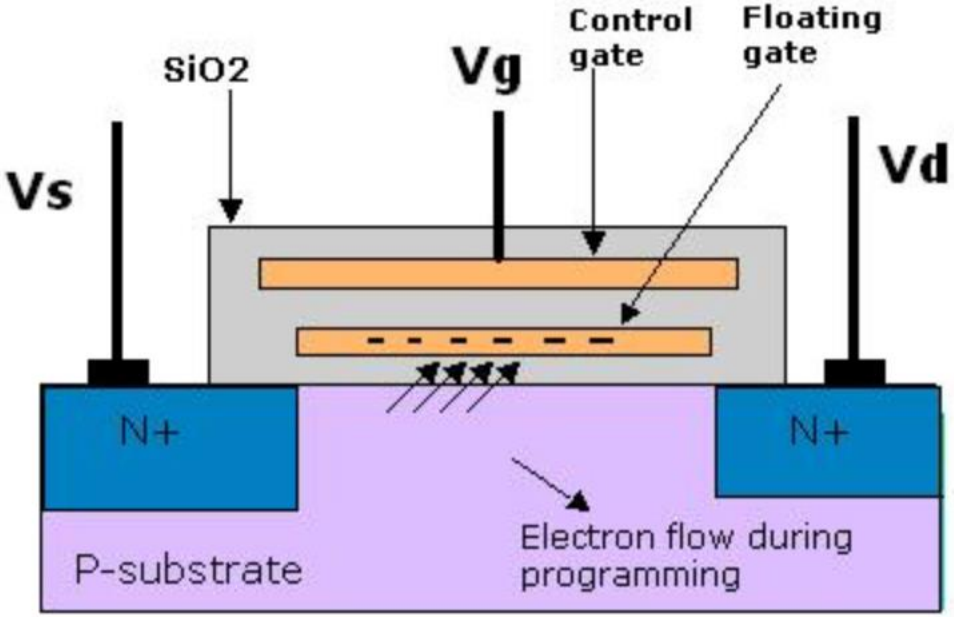


What type of FLASH for your controller

- Microcontroller
  - Smaller code size
  - NOR based
    - Fast random access to memory locations
    - Fast access times
    - All good bits
- Microprocessor or DSP
  - Larger code size
  - NAND based and moving to eMMC
    - Download executable code into SRAM for execution
    - Need ECC support to handle bad bits
    - Lower cost for larger code and storage requirements

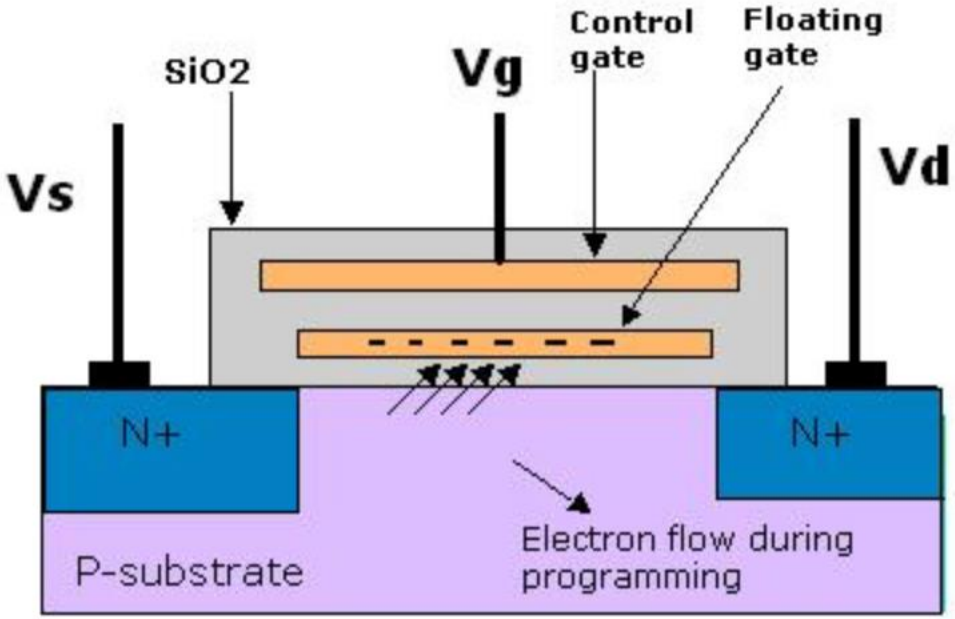
Basic NOR Gate (Working Principal)

- Flash stores the data by removing or putting electrons on its floating gate (see fig 5). Charge on floating gate affects the threshold of the memory element. When electrons are present on the floating gate, no current flows through the transistor, indicating a logic-0. When electrons are removed from the floating gate, the transistor starts conducting, indicating a logic-1. This is achieved by applying voltages between the control gate and source or drain.



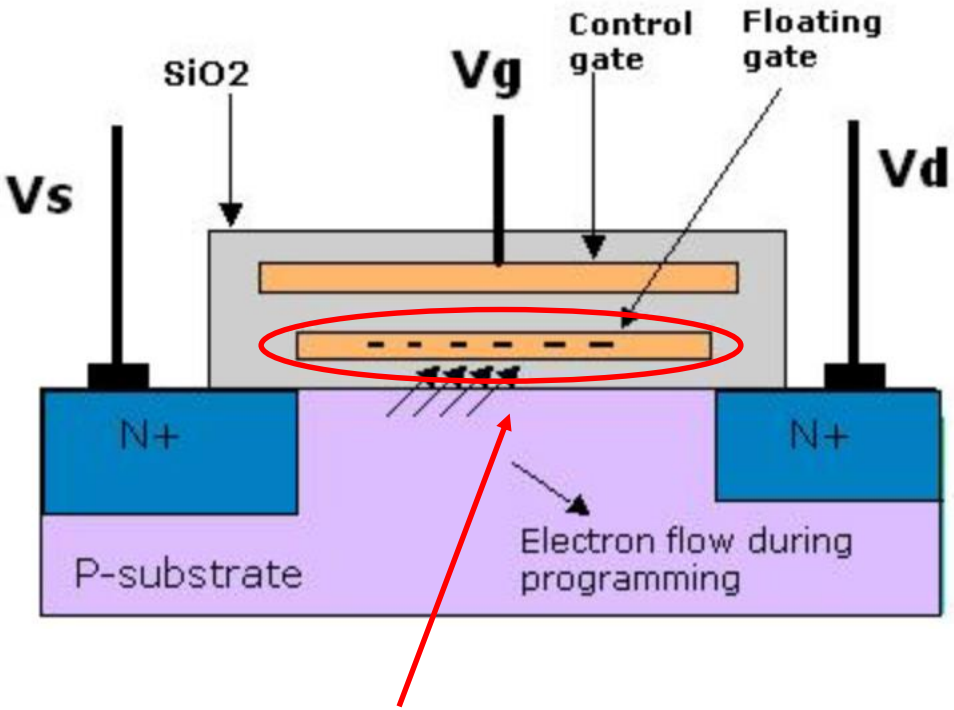
Basic NOR Gate (Erase Operation)

- The raw state of flash memory cells will be bit 1's, (at default state) because floating gates carry no negative charges. Erasing a flash-memory cell (resetting to a logical 1) is achieved by applying a voltage across the source and control gate (word line). The voltage can be in the range of -9V to -12V. And also apply around 6V to the source. The electrons in the floating gate are pulled off and transferred to the source by quantum tunneling (a tunnel current). In other words, electrons tunnel from the floating gate to the source and substrate.



Basic NOR Gate (Write Operation 1 of 3)

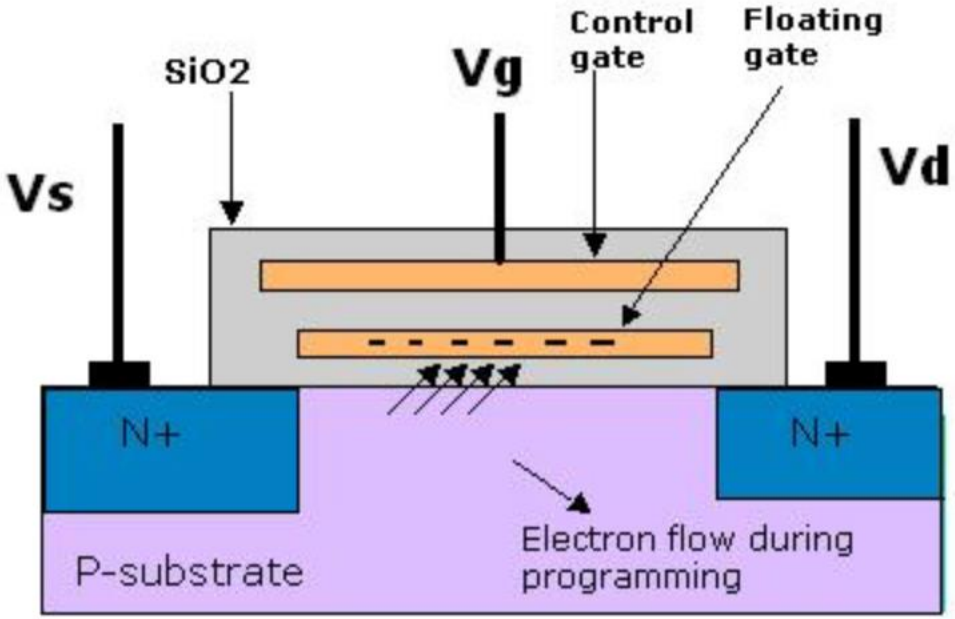
- A NOR flash cell can be programmed, or set to a binary "0" value, by the following procedure.
- While writing a high voltage of around 12V is applied to the control gate (word line). If high voltage around 7V is applied to Bit Line (Drain terminal), bit 0 is stored in the cell. The channel is now turned on, so electrons can flow from the source to the drain. Through the thin oxide layer electrons move to the floating gate. The source-drain current is sufficiently high to cause some high-energy electrons to jump through the insulating layer onto the floating gate, via a process called hot-electron injection.



Keeping the float gate charged correctly for reliability

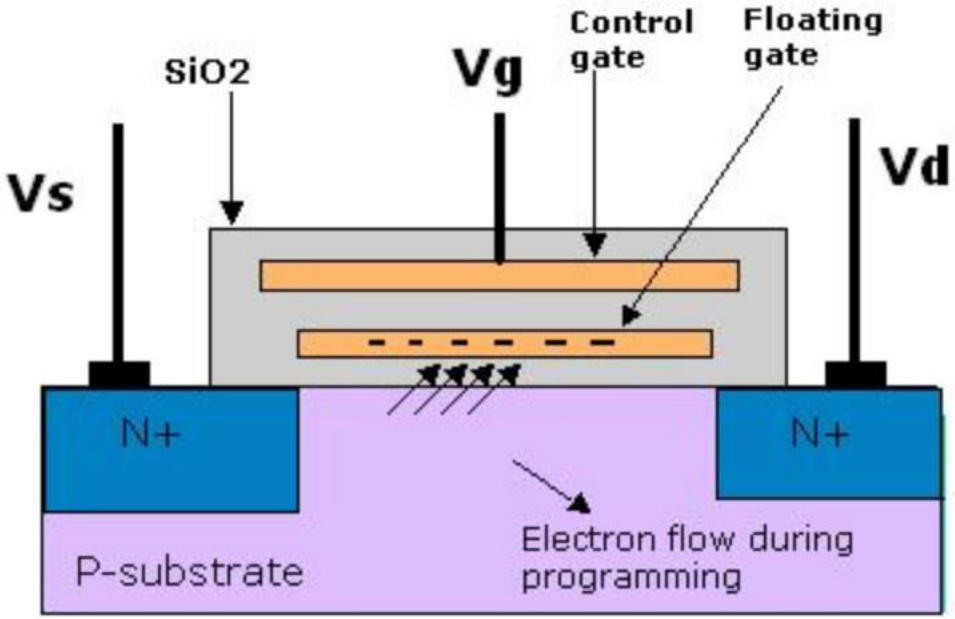
Basic NOR Gate (Write Operation 2 of 3)

- Due to applied voltage at floating-gate the excited electrons are forced through and trapped on other side of the thin oxide layer, giving it a negative charge on the floating gate. These negatively charged electrons act as a barrier between the control gate and the floating gate.



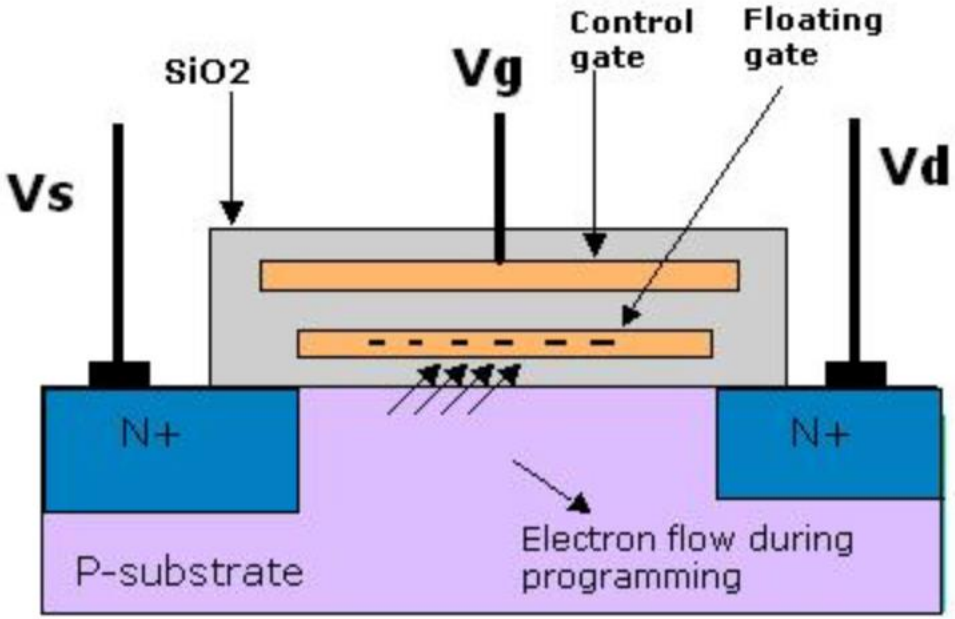
Basic NOR Gate (Write Operation 3 of 3)

- If low voltage is applied to the drain via the bit line, the amount of electrons on the floating gate remains the same, and logic state doesn't change, storing the bit 1. Since floating gate is insulated by oxide, the charge accumulated on the floating gate will not leak out, even if the power is turned off.
- A device called a cell sensor watches the level of the charge passing through the floating gate. If the flow through the gate crosses 50 percent threshold, it has a value of 1. When the charge passing through decline to below 50-percent threshold, than the value changes to 0.
- Because of the very good insulation properties of SiO2, the charge on the floating gate leaks away very slowly.



Basic NOR Gate (Read Operation)

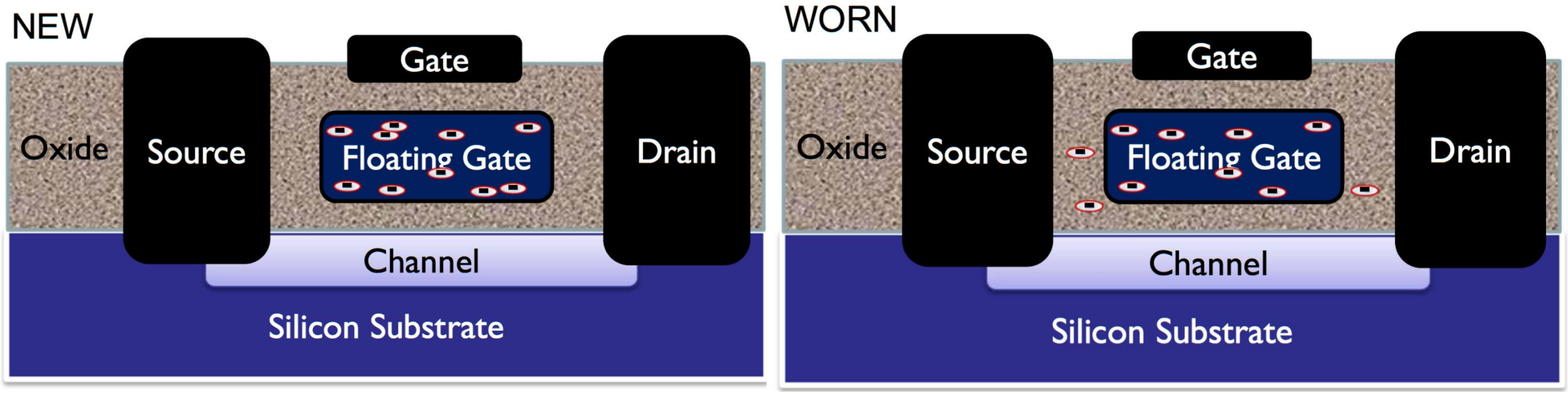
- Apply a voltage around 5V to the control gate and around 1V to the drain. The state of the memory cell is distinguished by the current flowing between the drain and the source.
- To read the data, a voltage is applied to the control gate, and the MOSFET channel will be either conducting or remain insulating, based on the threshold voltage of the cell, which is in turn controlled by charge on the floating gate. The current flow through the MOSFET channel is sensed and forms a binary code, reproducing the stored data.



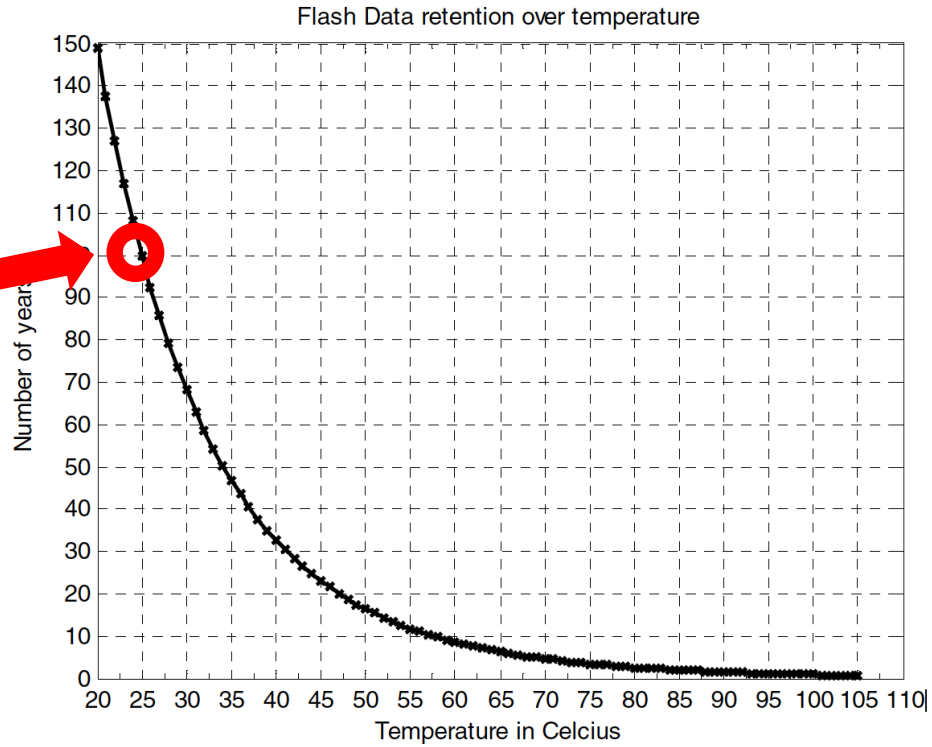
NOR failures due to over cycling Erase/Write operations

- Cycling Endurance
  - Each PROGRAM/ERASE operation can degrade the memory cell, and over time, the accumulation of cycles can prevent the device from meeting power, programming, or erasing specifications or from reading the correct data pattern.
- Data Retention
  - The dominant wear mechanism for charge loss and gain in NOR Flash memory occurs through electron trapping in the tunnel oxide of the Flash cell. This results in leakage through the insulator, and the damage primarily occurs during the ERASE/WRITE operations of a cell.

Flash memory wear-out: Electrons trapped in the tunneling oxide preventing a reliable read of a "0" or "1."



Data Retention versus Temperature



100 years at 25C

Data Retention errors increase as the leakage current increase electron migration with temperature. It can only happen to a floating gate which is positively charged. The value of a "0" can become a "1," and never a "1" to a "0"

Figure 1: Flash Data Retention vs Temperature for 170°C 420-Hour Test

The corner cases for 85°C and 105°C are slightly over 2 years and less than 9 months,

Data Retention vs Temperature dependency

- With higher temperatures, leakage current increases and, thus, the charge on the floating gate is reduced more quickly than at lower temperatures. This temperatures dependence follows the Arrhenius equation

$$AF = e^{-\frac{Ea}{k}\left(\frac{1}{T1} - \frac{1}{T2}\right)}$$

Where

AF = Acceleration factor
Ea = 0.6 eV = Activation energy
$k = 86.17 \times 10^{-6}$ = Speed constant
T1 = Temperature 1 (K)
T2 = Temperature 2 (K)

Example of data retention versus temperature

- At T_2 25C, the data sheet specifies data retention at 100 years
- At T_1 50C, what is the estimated data retention in years?
- 100 yrs / AF
- 100 yrs / $e^{-(\frac{0.6ev}{86.17x10-6})(\frac{1}{T1}-\frac{1}{T2})}$
- 100 yrs / $e^{-(\frac{0.6ev}{86.17x10-6})(\frac{1}{323}-\frac{1}{298})}$
- 100 yrs / $e^{1.8085}$
- 100 yrs / 6.101
- 16.39 yrs

NXP LPC15xx data sheet

Table 13. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	20	-	years
		not powered	20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC15xx user manual*).

Data Retention of the NXP LPC15XX at 125C operating?

- At T_2 105C (378K), the data sheet specifies data retention at 10 years
- At T_1 125C (398K), what is the estimated data retention in years?
- 10 yrs / AF
- 10 yrs / $e^{-(\frac{0.6ev}{86.17x10-6})(\frac{1}{T1}-\frac{1}{T2})}$
- 10 yrs / $e^{-(\frac{0.6ev}{86.17x10-6})(\frac{1}{398}-\frac{1}{378})}$
- 10 yrs / $e^{0.9257}$
- 10 yrs / 2.524
- 3.96 yrs

How to get desired data retention times for systems in elevated temperature with long life?

- Data Retention time is based on when the cell is written, so rewriting the cell before the Data Retention time becomes an issue will "restart" the Data Retention clock.
- Is this a good solution? Maybe.
  - Can you guarantee or design that over the life span of the product that the number of Erase/Program cycles specified will not be surpassed
  - Erasing a flash cell is a relatively a high current operation
    - Can the system provide the current required?
    - Does the battery have enough charge to meet the battery life cycle requirements?
  - Writing to the flash takes a relatively long time, and the processor is limited capabilities / resources during the flash erase, programming, and refreshes

Since the failure mechanism is a "0" being read as an erroneous "1", then the cell can be just re-programmed!

Example of the high current to program flash

- Silicon Labs' EFM32LG Leopard Gecko
- Typical current consumption without flash programming @ 14MHz HFRCO
  - EM0 = 3.02mA
  - EM1 = 1.11mA
  - EM2 = 0.0017mA
  - EM3 = 0.0013mA
  - Em4 = 0.0009mA

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{PERASE}	Page erase time		20	20.4	20.8	ms
t_{DERASE}	Device erase time		40	40.8	41.6	ms
I_{ERASE}	Erase current				7[1]	mA
I_{WRITE}	Write current				7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

[1]Measured at 25°C

High current of programming flash memory

- Possible solutions are:
  - Program or refresh FLASH only when connected to an external power source
  - Increase the current capability of the battery
  - Increase the charge or capacity of the battery
  - Manage power of the system
    - Example:
      - BLE Radio can consume 15mA during transmit
      - Writing to the flash consumes 7mA
      - Processor in EMO while writing to the FLASH is 3mA
      - Total current during these operations combined is 25mA
      - Only perform writing to the flash when the radio is turned OFF

Limiting peak current during FLASH programming or refresh to 10mA

High current of programming flash memory

- Silicon Labs' Leopard Gecko EFMLG32 write to flash example
- Worst case is a page erase plus a full page write
- Page size is 2048 bytes or 512 4-byte words
  - Erase page 20.8ms
  - Write 512*20uS 1.0ms
  - Total time of 21.8ms
- To minimize the current spike on the battery for a BLE application that programmed while operating, the ConnInterval or SlaveInterval should guarantee at least 21.8ms with the radio off to program the flash

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Limitations due to the number of erase cycles before failure

- Silicon Labs' EFM32LG Leopard Gecko
- If a page of the flash had to be updated 1 time per hour based for sensor readings
  - 24*365 = 8,760 /yr
  - Requires a "fresh" flash sector 2.25 years
- Or, a page of flash had to be updated every 1 minute
  - 60*24*365 = 525,600
  - Requiring a "fresh" flash sector every 13.89 days

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Limitations due to the number of erase cycles before failure

- Possible solutions
  - Allocate enough flash to insure enough good “flash” pages for the life of the product
  - Example:
    - The case of a flash page is updated every hour
    - The product is an industrial application with a lifecycle projection of 20 years
    - Number of pages pages based on the previous example = 20 yrs / 2.25 yrs/page
      - ~ 8.89 pages
    - Total amount of flash dedicated for this storage = 2,048 bytes/page * 8.89 pages
      - 18,207 bytes
    - Solution: Purchase a microcontroller that had an additional 9 pages of flash available to allocate for data logging
    - Solution: Utilize an external Flash

Limitations due to the number of erase cycles before failure

- Possible solutions
  - Allocate enough flash to insure enough good “flash” pages for the life of the product
  - Example:
    - The case of a flash page is updated every minute
    - The product is an industrial application with a lifecycle projection of 20 years
    - Number of days over product life cycle = 20 * 365 = 7240 days
    - Number of pages pages based on the previous example = 7240 / 13.89 ~ 8,864 pages
    - Total amount of flash dedicated for this storage = 2,048 bytes/page * 8,864 pages
      - 18,153,472 bytes
    - Solution: ~~Purchase a microcontroller that had 18MB of additional memory~~
    - Solution: External Flash or change product specifications

Writing to the flash takes a long time

- Silicon Labs' Leopard Gecko EFMLG32 write to flash example
- During writes to flash in the Leopard Gecko, no access to flash memory is allowed
  - Not even instructions to execute
  - It will stall the processor
- Must plan the write to flash when access to flash will not be required
- Page size is 2048 bytes or 512 4-byte words
  - Erase page 20.8ms
  - Write 512*20uS 1.0ms
  - Total time of 21.8ms
- Must plan writes when no time critical interrupts can occur
  - For BLE operations, it should be planned between Connection Events so the ConnInterval or ServerLatency should be greater than the time to write to flash

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Correction to TI application note SLAA334

- Let's take a look at the TI SLAA334 statement

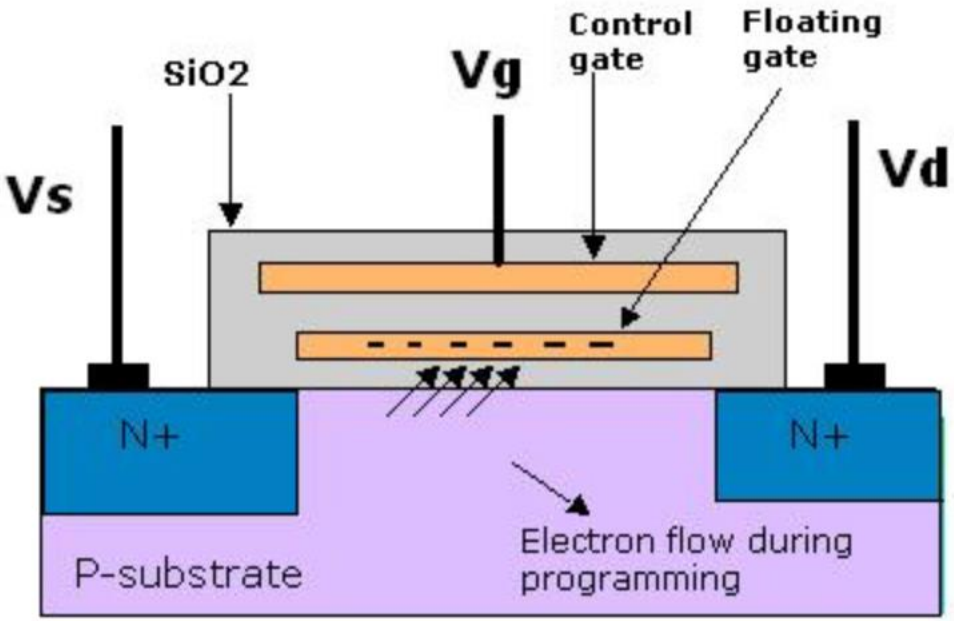
3.1 Data Retention

3.1.1 Leakage Mechanism

Data retention is limited by leakage current through the insulating oxide. Leakage can only occur if the floating gate is fully charged. Therefore, leakage only can flip an erased cell with the logic level 1 to a programmed cell with the logic level 0. According to Manabe [1], there are several phenomena that cause leakage.

Correction to TI application note SLAA334

- Let's think of a model of a NAND memory cell
- A "1" occurs when current flows from the source to the drain
- A "0" occurs when the free electrons in the substrate are moved and trapped in the floating gate, thus current cannot flow from the source to drain



Data Retention

In flash storage, data retention is the measure of how long the integrity of data can be guaranteed after being written to the flash drive without suffering from data corruption. Once a flash cell is charged, the electrons stored in the cell leak across the NAND gate over time, causing the charge on the cell to decrease. With enough leakage, the voltage level on the cell will drift into the neighboring region, causing the incorrect binary value to be read.

Because SLC flash memory is only divided into two voltage regions, it has more margin for charge loss before a bit flip occurs (a 0 becomes a 1), as shown in Figure 2.

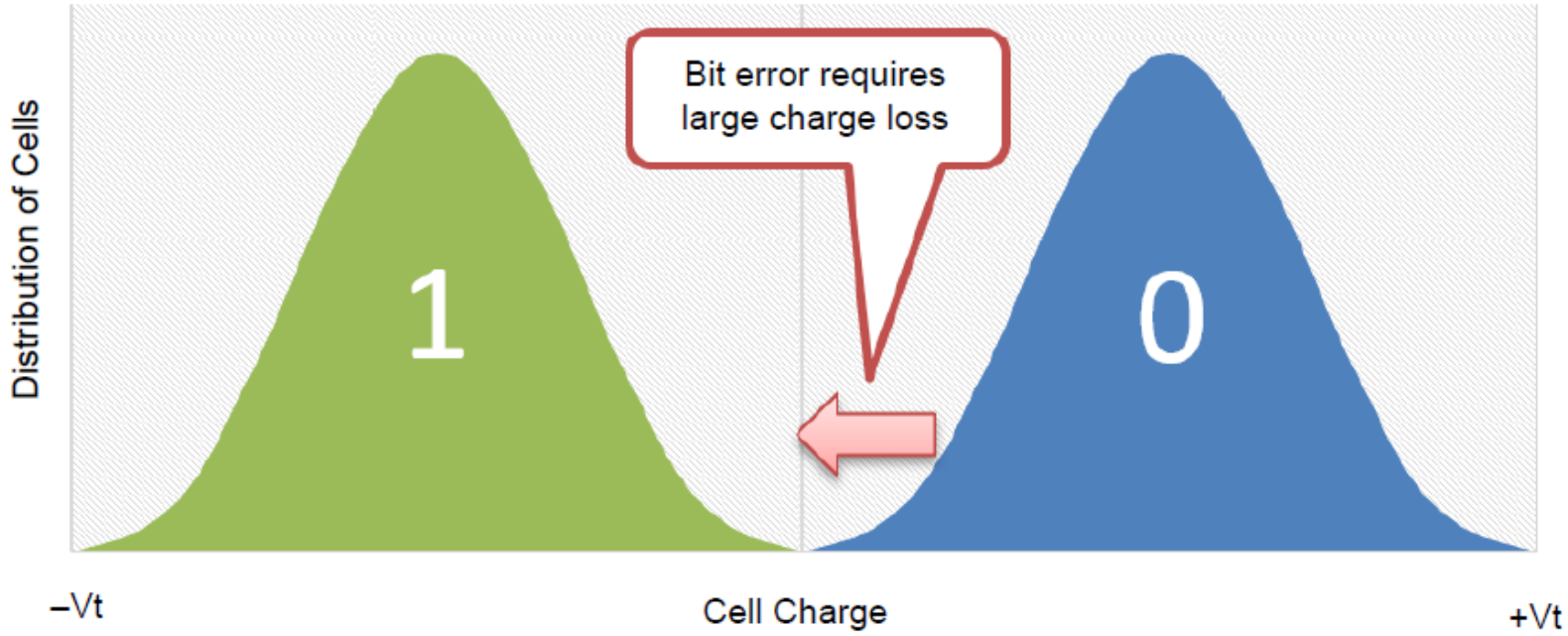


Figure 2 SLC Flash Data Storage

On the other hand, MLC can tolerate much less charge loss before data errors occur because it has a similar voltage range divided into four regions, as shown in Figure 3.

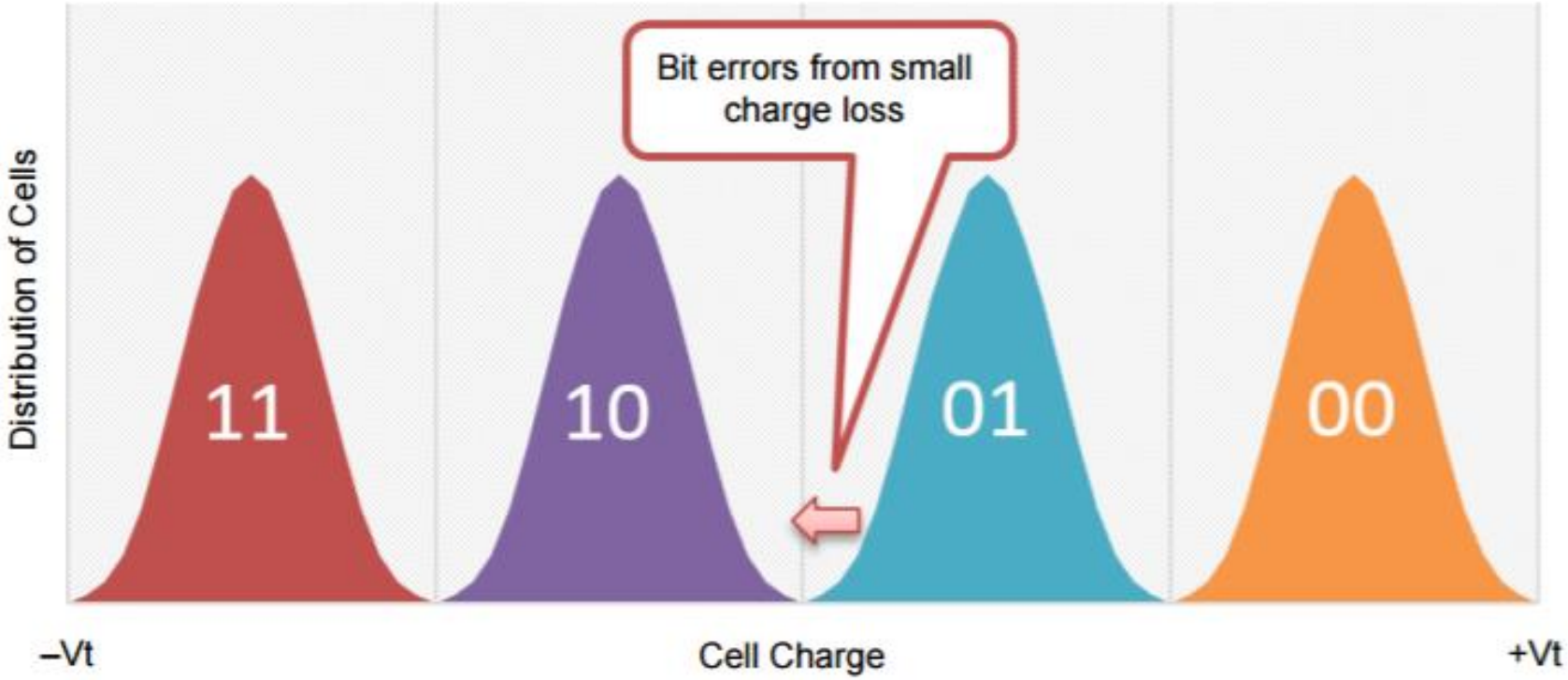
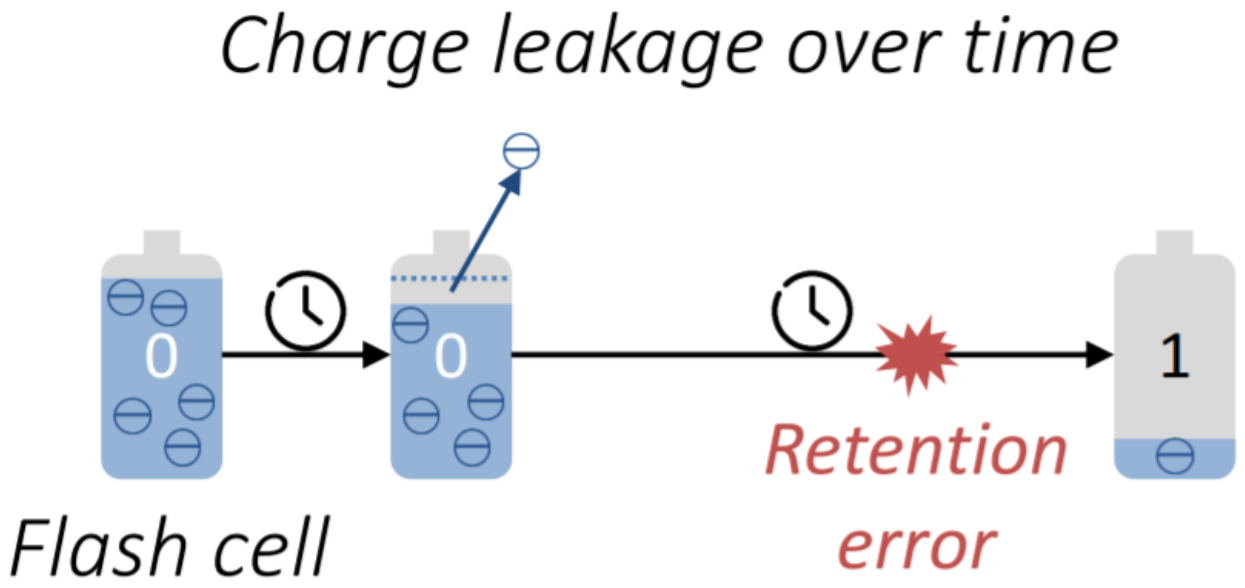


Figure 3 MLC Flash Data Storage

Retention Loss



One dominant source of flash memory errors [DATE '12, ICCD '12]

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