ECEN 5823-001
Internet of Things Embedded Firmware

Lecture #19

30 October 2018

Be Boulder.

University of Colorado Boulder

Agenda

- Class Announcements
- Helpful Bluetooth Mesh links
- Reading Assignment
- Project Proposal feedback
- Project Update #1
- Memory for embedded applications

Class Announcements

- Quiz 8 due on Wednesday, October 31st, at 11:59pm
- Quiz 9 due on Sunday, November 4th, at 11:59pm
- Course Project Update 1 due Sunday, November 4th, at 11:59pm

Bluetooth Mesh Helpful Links

- Silicon Labs create a Vendor Specific model to distribute the data across the MESH
  - https://www.silabs.com/community/wireless/bluetooth/knowledge-base.entry.html/2018/06/15/bluetooth_mesh_vendo-vwlm

- Silicon Labs' Knowledge Base List
  - https://www.silabs.com/community/wireless/bluetooth/knowledge-base.entry.html/2018/04/08/kba_master_list-MxiO

Reading Assignment

ECEN5823-001, -001B – Reading List
Internet of Things Embedded Firmware
Week 110

Note: There is a quiz this week. The material covered on the quiz will be from the last several chapters of the course textbook as well as the below readings and course lectures.

1. Silicon Labs' White Paper, "Bluetooth Mesh Technology Wireless Technology for the World of IoT.pdf"
    a. Pages 1 - 10
    b. Located on the Canvas week 10 reading assignment folder

Project Proposal Feedback

- If you were a Venture Capitalist, how would you like to see a proposal organized?

- I was looking for more detail on the services or clients than the sending the data from the sensors

- If you are not confident that you can do a Mesh network, I highly recommend that you rethink your project as a Bluetooth Smart project

Sensor Dev Kit feedback

Moisture sensor:

SEN-13322 ROHS Sparkfun		Qty: 2
SEN-13637	Sparkfun	Qty: 1

Rain sensor:

MOD-000HL83 Qty: 2

https://www.gearbest.com/other-accessories/pp_1802002.html?wid=1433363&currency=USD&vip=4444999&gclid=EAIaIQobChMIyv32rK2q3gIV1rjACh1mMwmpEAQYAiABEgKoQ_D_BwE

Smoke sensor:

MAX30105	Sparkfun	Qty: 1

Fingerprint sensor:

GT-521F32	Sparkfun	Qty: 1

Magnetometer:

MLX90393	Sparkfun	Qty: 3

Can you use the LMS303C, Sparkfun p/n BOB-13303

Sensor Dev Kit feedback

Light sensor:

SEN-14350	Sparkfun	Qty: 1
TSL2561	Adafruit	Qty: 1

Can the TSL2561 be used instead of the SEN-14350?

Air quality sensor:

CCS811	Adafruit	Qty: 2

Proximity sensor:

RFD77402	Sparkfun	Qty: 1
SI1143-M01-GMR	SiLabs	Qty: 1

What is the dev kit p/n for Si1143-M01-GMR?

Sensor Dev Kit feedback

Gesture sensor:

APDS-9960	Sparkfun	Qty: 2

Level Shifter:

13743	Sparkfun	Qty: 1

UV sesor:

VEML6075	Sparkfun	Qty: 1

ECEN 5823
Project Update #1 Assignment
Fall 2018

Project Update 1 assignment

Objective: To update the status and provide additional information on the Course Project in ECEN 5823, Fall 2018.

Note: You can use your course project proposal as a base for this project update.

Project Proposal Due Date: Sunday, November 11th, at 11:59pm via Canvas drop box

Team proposals: (Include and Provide update to the below items)

1. Describe what problem this project addresses
2. How does this project alleviate or solve the problem?
3. Functional block diagram of the team project
4. Summary of each individual project and how it plays a role in solving the problem
5. Project team members
6. Team project validation plan

Writing to the flash takes a long time

- Silicon Labs' Leopard Gecko EFMLG32 write to flash example
- During writes to flash in the Leopard Gecko, no access to flash memory is allowed
  - Not even instructions to execute
  - It will stall the processor
- Must plan the write to flash when access to flash will not be required
- Page size is 2048 bytes or 512 4-byte words
  - Erase page 20.8ms
  - Write 512*20uS 1.0ms
  - Total time of 21.8ms
- Must plan writes when no time critical interrupts can occur
  - For BLE operations, it should be planned between Connection Events so the ConnInterval or ServerLatency should be greater than the time to write to flash

Table 3.7. Flash

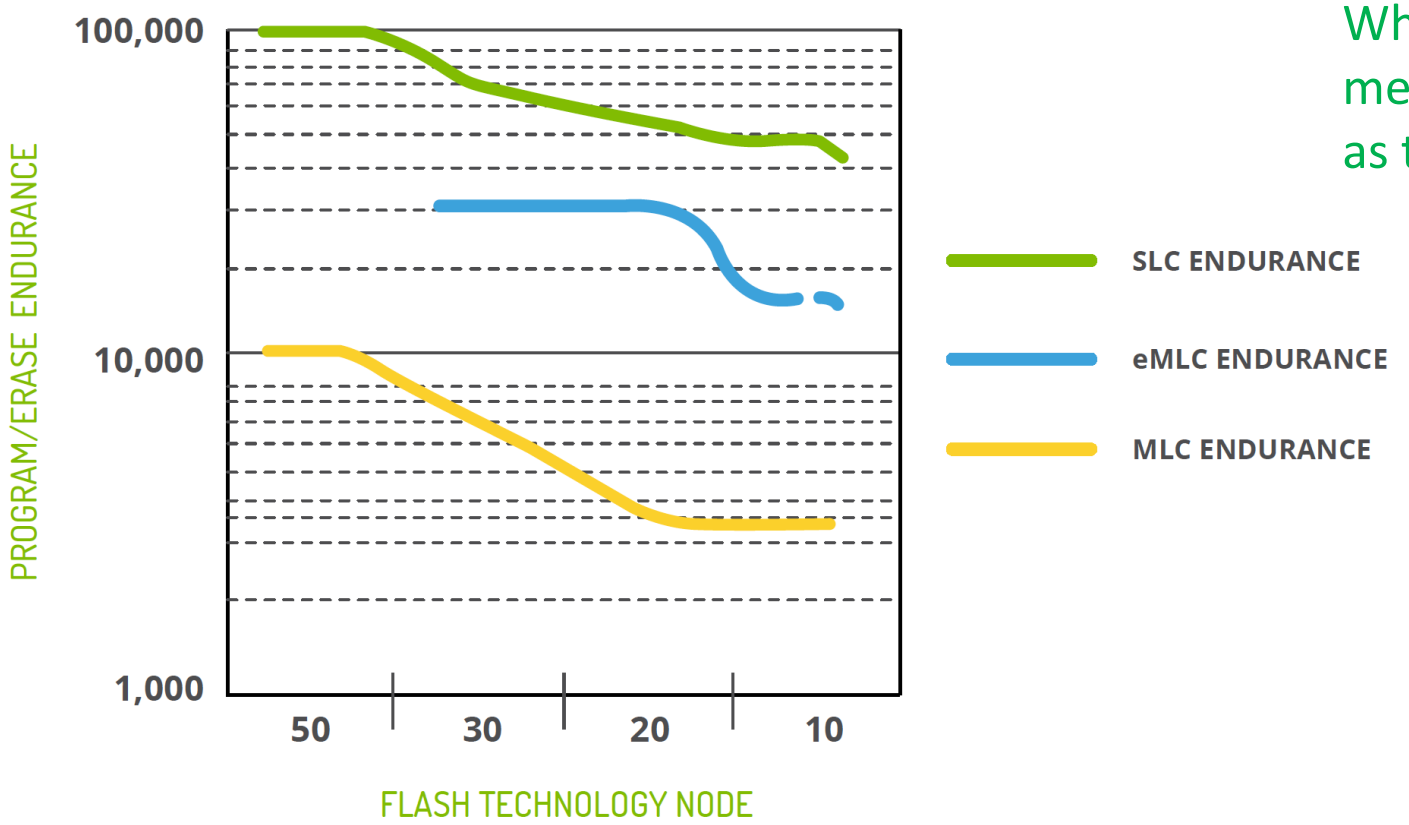
Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{PERASE}	Page erase time		20	20.4	20.8	ms
t_{DERASE}	Device erase time		40	40.8	41.6	ms
I_{ERASE}	Erase current				7[1]	mA
I_{WRITE}	Write current				7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

[1]Measured at 25°C

Writing to the flash takes a long time

- Solution: Find a time that critical interrupts can be turned off
  - In a BLE application, is there a time between ConnIntervals or ServerLatency?
  - Is there a time in the day that operation is not critical?
    - Example: micro converter on a solar panel during the solar panel daily wakeup
  - The product gets plugged in to charge
    - Example: A fit bit watch does not need to perform its primary role while plugged in to be charged
- Solution: Use an external Flash
  - External flash does not tie up a microcontroller's critical resources such as program memory
  - External flash such as eMMC have integrated algorithms to minimize data retention and other errors such as write disturb
  - External flash with the correct capacitance coupling can provide guaranteed write completion
  - Negative, an additional part resulting in higher part cost and board real estate

Endurance versus Moore's Law



Cactus Technologies

Why does non-volatile memory endurance go down as the feature size decreases?

Endurance goes down as the area to store the electrons in the floating gate gets smaller. Less electrons, less margin or separation between a "0" and a "1" state.

Cactus Technologies "SLC vs MLC NAND and The Impact of Technology Scaling White paper CTWP010"

NAND Technology types

- What are the different types of NAND memory technologies?
- SLC
  - Single Level Cell
  - Each NAND cell is one bit, or two states (0,1)
- MLC
  - Multi Level Cell
  - Each NAND cell represents two bits, or four states (0,1,2,3)
- TLC
  - Tertiary Level Cell
  - Each NAND cell represents three bits, or 6 states (0,1,2,3,4,5)
- 3d
  - Memory cells stacked on top of each other (3d)
  - Can be SLC or MLC

NAND Technology comparisons

- SLC
  - Relatively fast read and write capabilities
  - Good endurance
  - And relatively simple error correction algorithms
  - More expensive than MLC and TLC since one bit for the same area
- MLC
  - Twice the density of SLC, thus less cost per bit than SLC
  - Roughly 1/3 the speed of SLC
  - And, Roughly 1/10 the reliability of SLC
  - Most common flash today – good balance between cost and performance

NAND Technology comparisons

- TLC
  - 3x the density of SLC
  - Much lower performance
  - Reliability is lowest of all NAND types
  - Good for applications that have low amounts of writes such as MP3 players
- 3d NAND
  - Technology based on stacking NAND cells
  - Increases the number of layers and steps in the manufacturing process
  - Enables costs to continued to go lower
  - Reliability increased over standard MLC due to larger feature size, better insulating material, and charge trap design

NAND failure mechanisms

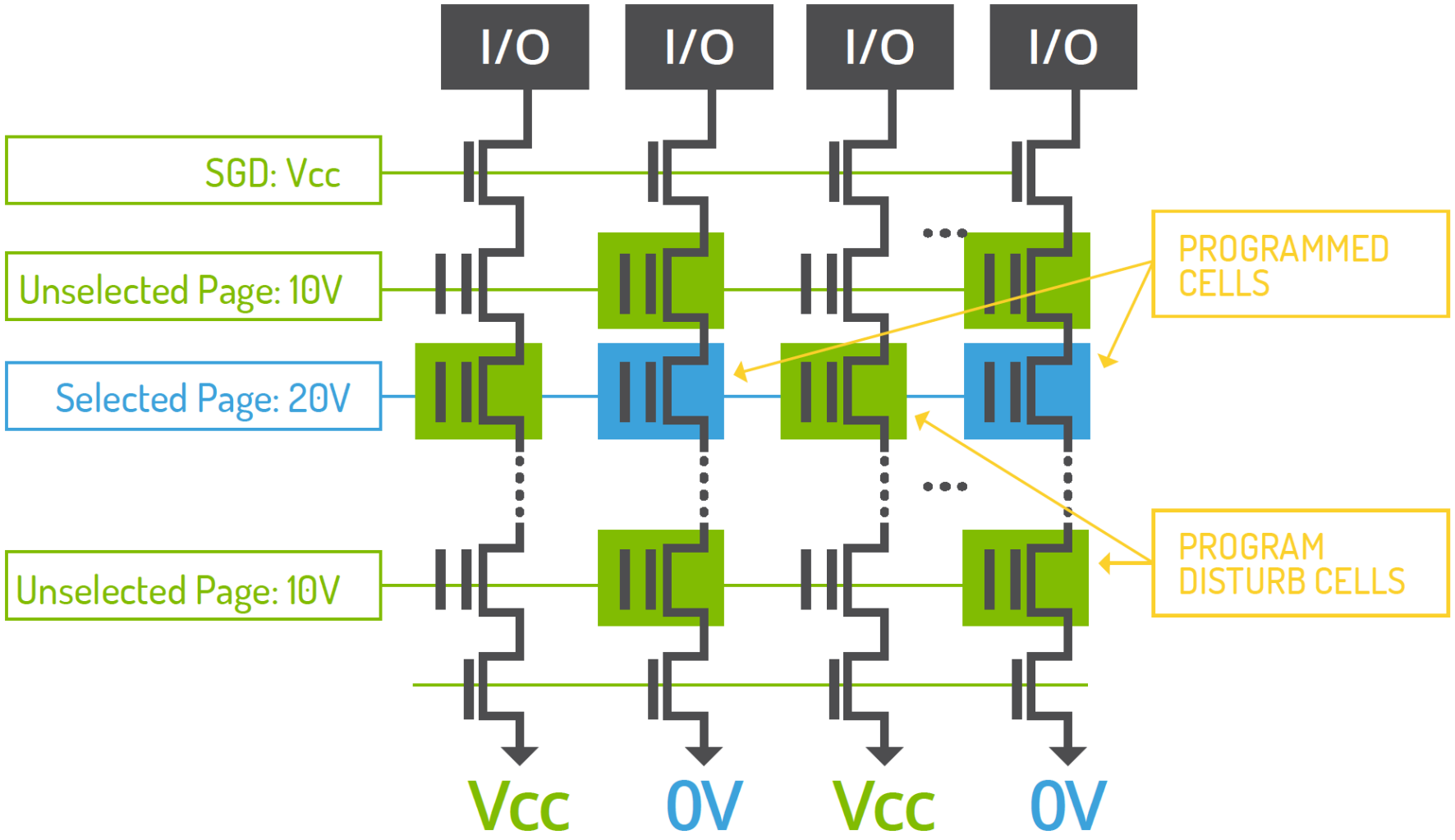
- Erase/Program cycle endurance
  - Same as NOR
- Data Retention
  - Same as NOR
- Reliability versus Moore's Law
  - Same as NOR
- Read Disturb
  - NAND failure mode
- Write Disturb
  - NAND failure mode

Write Disturb

Program disturb occurs in neighboring cells of the ones being programmed. This happens because the neighboring cells are exposed to voltage levels which are higher than normal. This setup causes these cells to appear to be weakly programmed. Fig.5 illustrations a representation of this problem:

A write disturbed error would result in a "1" bit going to a "0."

Why would MLC NAND be more sensitivity to write disturb errors?



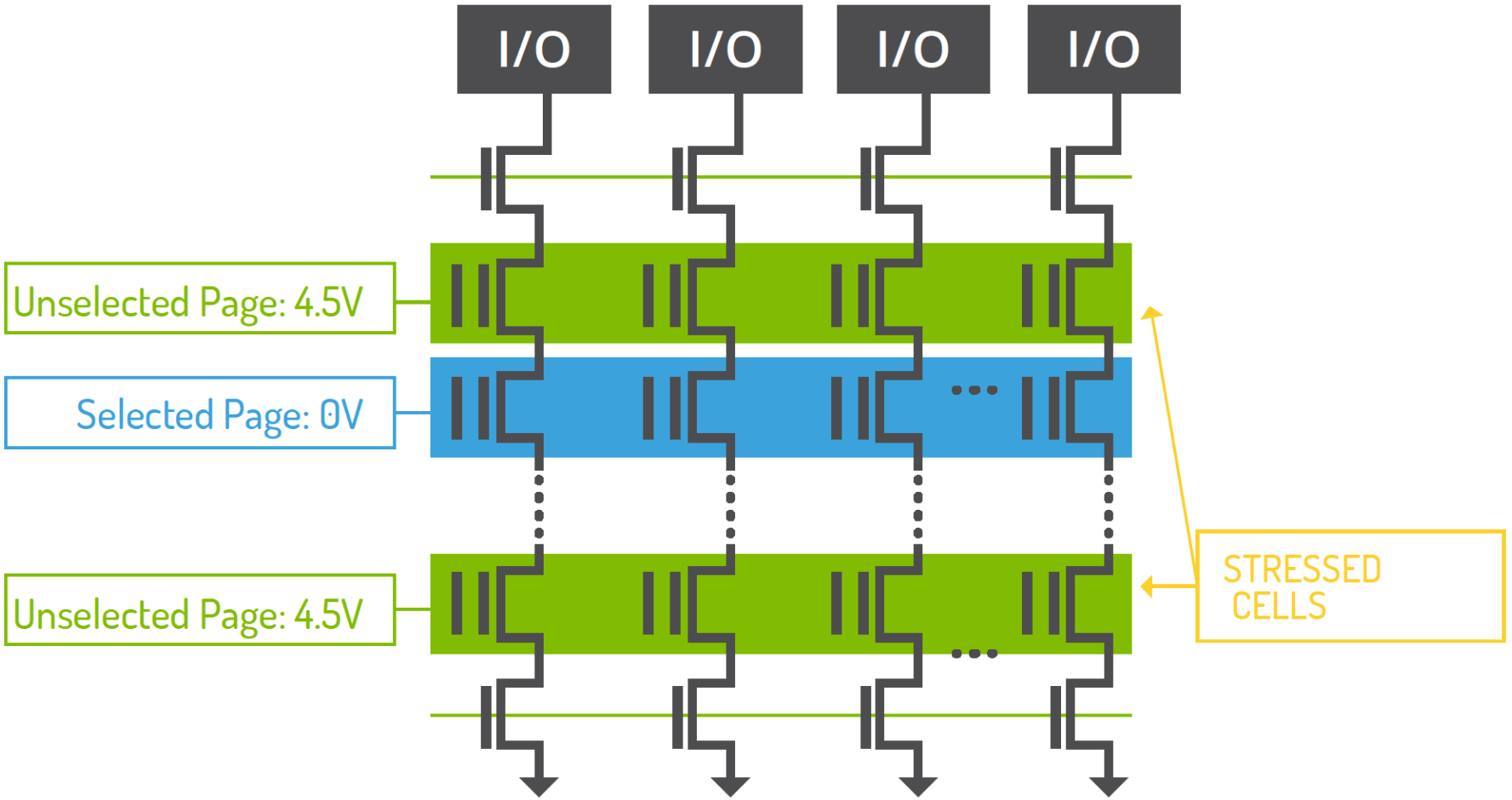
Cactus Technologies "SLC vs MLC NAND and The Impact of Technology Scaling White paper CTWP010"

Read Disturb

Read disturb happens in neighboring cells of the ones being read due to stray charge being coupled to the floating gates of the unselected cells. This problem is not as severe as write disturb but is getting worse as flash geometry shrinks. Fig. 6 illustrates this scenario:

A read disturbed error would result in a "1" bit going to a "0."

Read disturb errors only occur on the adjacent cells, and not the cell read.



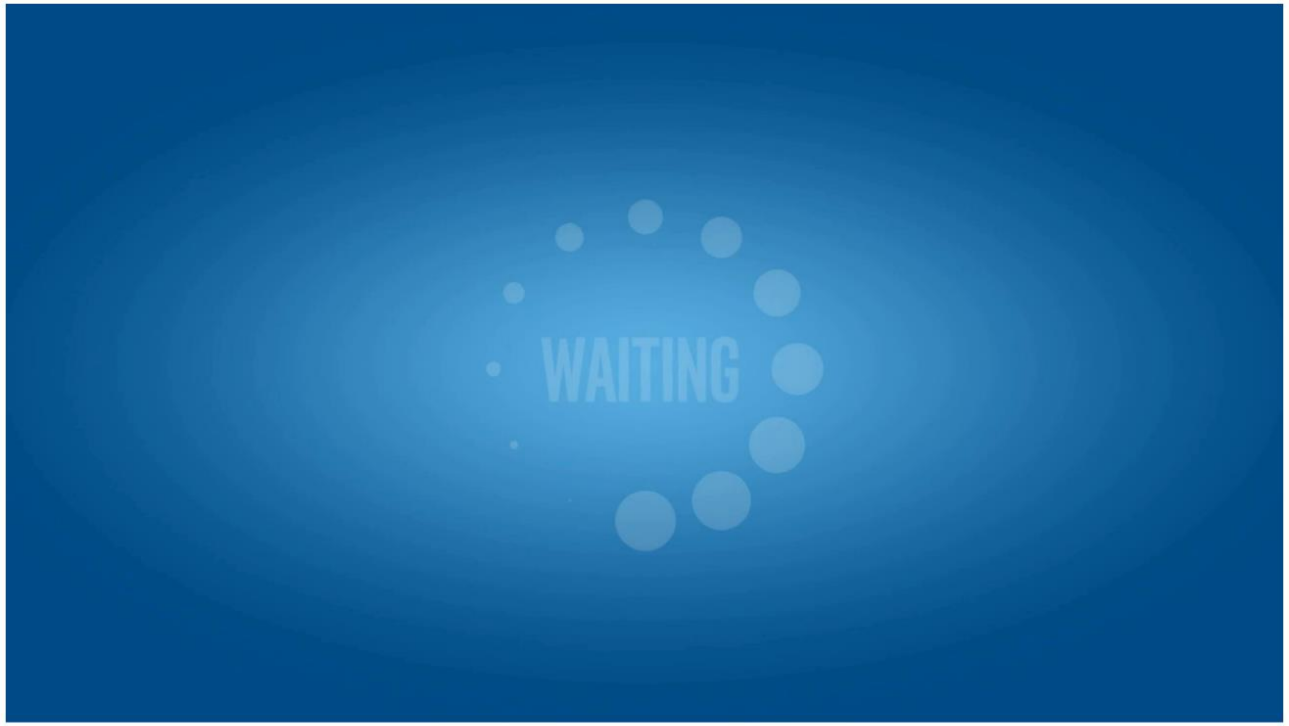
Dynamic (Global) Wear Leveling

- Dynamic wear leveling is a method of pooling the available blocks that are free of data and selecting the block with the lowest erase count for the next write. This method is most efficient for dynamic data because only the non-static portion of the NAND Flash array is wear-leveled. A system that implements dynamic wear leveling enables longer NAND Flash device life than a system that does not implement wear leveling.

Static Wear Leveling

- Static wear leveling utilizes all good blocks to evenly distribute wear, providing effective wear leveling and thereby extending the life of the device. This method tracks the cycle count of all good blocks and attempts to evenly distribute block wear throughout the entire device by selecting the available block with the least wear each time a program operation is executed. Static data is managed by maintaining all blocks within a certain erase count threshold. Blocks that contain static data with erase counts that begin to lag behind other blocks will be included in the wear-leveling block pool, with the static data being moved to blocks with higher erase counts.

Intel and Micron breaking the NAND technology limitations – 3D XPoint



3D XPoint™ Technology Revolutionizes Storage Memory

Intel engineers help shatter all the rules with 3D XPoint™ technology, a simple, stackable, and transistor-less design that creates fast, inexpensive, and nonvolatile storage memory with low latency to unleash your processor's true potential.

eMMC

- eMMC
  - Embedded MultiMediaCard Memory
  - MMC (MultiMediaCard)
    - Released in 1997 by SanDisk and Siemens AG
    - Based on NAND memory
    - Much smaller than other non-volatile cards in 1997 based on NOR Flash technology such as CompactFlash
  - Designed to solve NAND memory issues for the system designer
    - Perform ECC
    - Increase reliability
      - Static wear leveling
      - Dynamic (Global) wear leveling
    - System design becomes independent to NAND die changes resulting in ECC changes

Micron example of wear leveling benefits

- Consider a case without wear leveling. In a NAND Flash device with 4,096 total blocks and 2.5% allowable bad blocks in a system that updates 3 files comprised of 50 blocks each at a rate of 1 file every 10 minutes (or 6 files per hour), where a NAND host reuses the same 200 physical blocks for these updates, the NAND Flash device will wear out in under 1 year, leaving over 95% of the memory array unused.
- No wear leveling:

$$\text{Only 200 blocks are reused:} \frac{\text{10,000 cycles x 200 blocks}}{\text{50 blocks per file x 6 files per hour x 24 hours per day}} = \sim 278 \text{ days or } < 1 \text{ year}$$

Dynamic (Global) wear leveling example

- In a 4,096-block MLC device with a 10,000-cycle count, 75% static data, and a program and erase rate of 50 blocks every 10 minutes (or 6 files per hour), dynamic wear leveling results in device wear-out after approximately 4 years, with 75% of the blocks nearly unused.

$$\text{Wear leveling only dynamic data: } \frac{\text{10,000 cycles x 1,024 blocks}}{\text{50 blocks per file x 6 files per hour x 24 hours per day}} = \sim\text{1,422 days or <4 years}$$

Static wear leveling example

- Using the same example of a 4,096-block MLC device with a 10,000-cycle count, 75% static data, and a program and erase rate of 50 blocks every 10 minutes (or 6 files per hour), static wear leveling provides the best chance of extending the device life span beyond 15 years.

$$\text{Wear leveling static and dynamic data: } \frac{10{,}000 \text{ cycles x } 4{,}096 \text{ blocks}}{50 \text{ blocks per file x } 6 \text{ files per hour x } 24 \text{ hours per day}} = \sim 5{,}689 \text{ days or } > 15 \text{ years}$$

Preventing Read Disturbance

- InnoDisk Firmware is designed to resolve this issue by wear leveling and refresh (“re-charges”).
- With wear leveling feature, not only spread the program/erase count evenly on all blocks, but also can reduce the read access frequency to prevent Read Disturbance by reprogramming the data to different blocks.
- Alternatively, ECC (Error Correcting Code) can detect and fix the data where the electrical properties may have been altered by refresh. When error bits in a block reach a threshold of say 17 error bits out of 24 bits, the block is automatically refreshed. i.e. the data is deleted and re-written.
- This stops the controller from constantly reading blocks with too many error bits and prevents read disturbance.

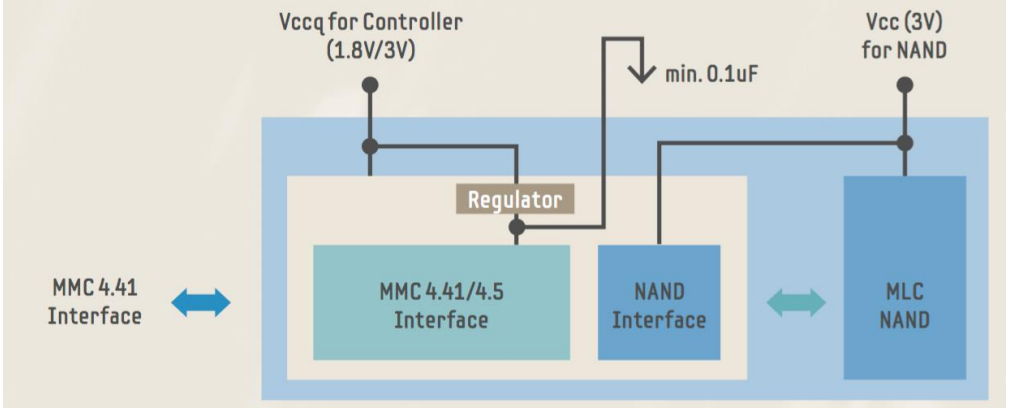
Wear Leveling Summary

Comparison [edit]

The following table compares static and dynamic wear leveling:[3]

Item	Static	Dynamic
Endurance	Longer life expectancy	Shorter life expectancy
Performance	Slower	Faster
Design Complexity	More complex	Less complex
Typical Use	SSDs[2]	USB Flash Drives

eMMC architecture



- eMMC memory is 2 die in one package
  - An EMMC controller
  - NAND memory
- eMMC advantages
  - Industry standard in both hardware and software
  - Enables the eMMC solution to be multi-source to enhance availability and reduce cost
  - Off loads the NAND management from the system firmware or hardware
  - System hardware and firmware does not need to change as NAND memory shrinks and changes ECC scheme – the change is supported by the eMMC controller

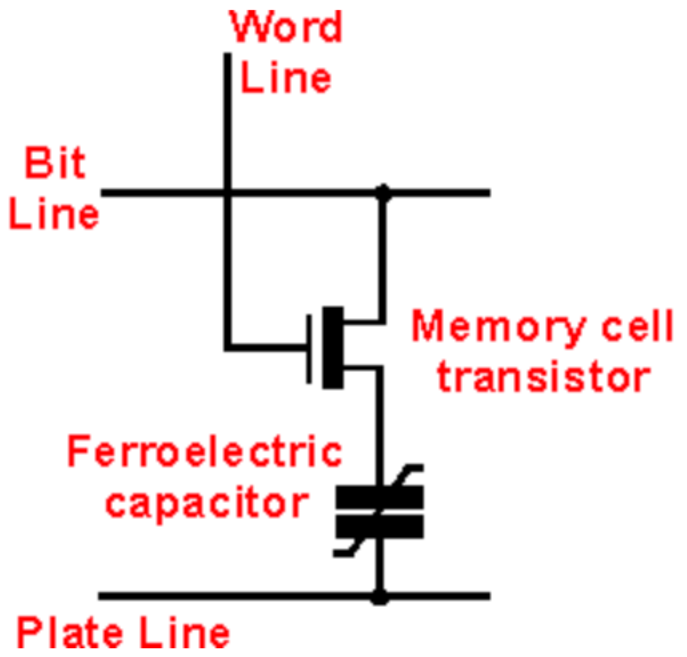
http://www.samsung.com/us/business/oem-solutions/pdfs/eMMC_Product%20Overview.pdf

Example of NAND management offload

- Hyperstone S8 NAND Management Features
  - hyReliability™ Flash Memory Management optimizing reliability, power fail safety, endurance, data retention, and performance
  - Read Disturb Management, dynamic data refresh to maximize data retention and refresh data subject to read disturbance
  - Static and Global Wear leveling to maximize write endurance
  - Bad Block Management
  - Complete Flash Translation Layer (FTL) for random Flash data access including mapping of logical block addresses (LBA) to physical block addresses (PBA)

FRAM

- Ferroelectric Random Access Memory (FRAM), also known as FeRAM or F-RAM, is a memory technology that combines the best of Flash and SRAM. It is non-volatile like Flash, but offers fast and low power writes, write endurance of 10^{15} cycles, code and data security that is less vulnerable to attackers than Flash/EEPROM



Basic Ferroelectric memory cell

Radio-Electronics.com "FRAM Ferroelectric Random Access Memory Tutorial"

- From the definition of a FRAM memory, how is this memory different than NAND?
- Being not electron base, what benefits could it provide?

http://www.ti.com/lsds/ti/microcontrollers_16-bit_32-bit/msp/ultra-low_power/msp430frxx_fram/what_is_fram.page?DCMP=ep-mcu-msp-fram-en&HQS=ep-mcu-msp-fram-b-lp-en#under

FRAM Technology

- Molecular Structure
  - FRAM is a random access memory, meaning that each bit is read and written individually. This non-volatile memory is similar in structure to DRAM, which uses one transistor and one capacitor (1T-1C), but FRAM stores data as a polarization of a ferroelectric material (Lead-Zirkonate-Titanate). As an electric field is applied, dipoles shift in a crystalline structure to store information.
  - The use of crystal polarization as opposed to charge storage enables state retention, lower voltage requirements (as low as 1.5V) and fast write speeds when compared against Flash, EEPROM and SRAM technologies used in typical microcontroller.

http://www.ti.com/lsds/ti/microcontrollers_16-bit_32-bit/msp/ultra-low_power/msp430frxx_fram/what_is_fram.page?DCMP=ep-mcu-msp-fram-en&HQS=ep-mcu-msp-fram-b-lp-en#under

FRAM – Molecular Structure

In contrast to the complex charge storage mechanism used in EEPROM and flash, FRAM stores information through the use of a spontaneous, stable electric dipole found in the ferroelectric crystal. Intrinsically, the dipole atom within a ferroelectric crystal has either positive or negative orientation, as shown in Figure 2-4.

Applying an electrical field polarizes the material by creating large regions of the crystal with Ti/Zr ions all oriented the same direction (domains). By applying a voltage of opposite polarity above the coercive voltage, the Ti/Zr ions will have enough energy to overcome the energy barrier in the center of the cell to move to the other low-energy site as Figure 2-5 illustrates.

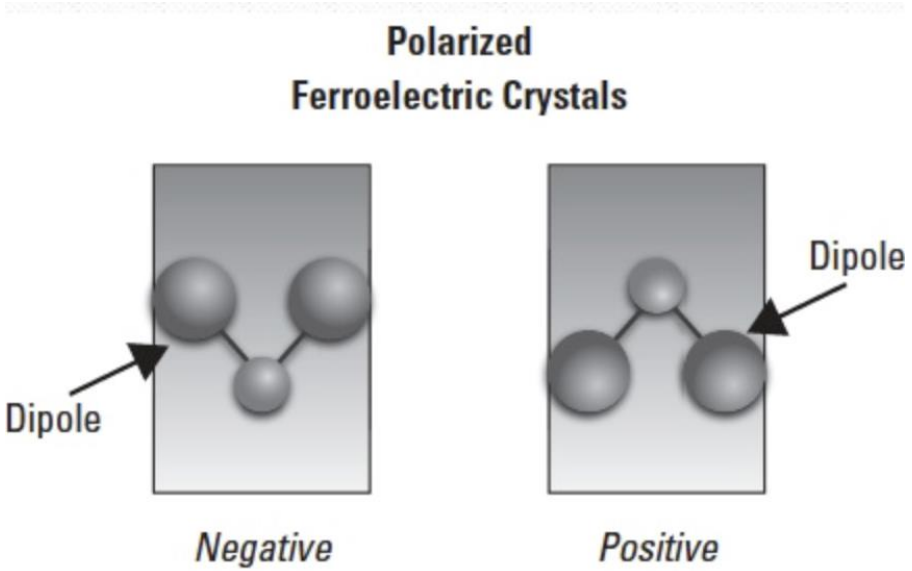


Figure 2-4. Dipole positions of ferroelectric crystals.

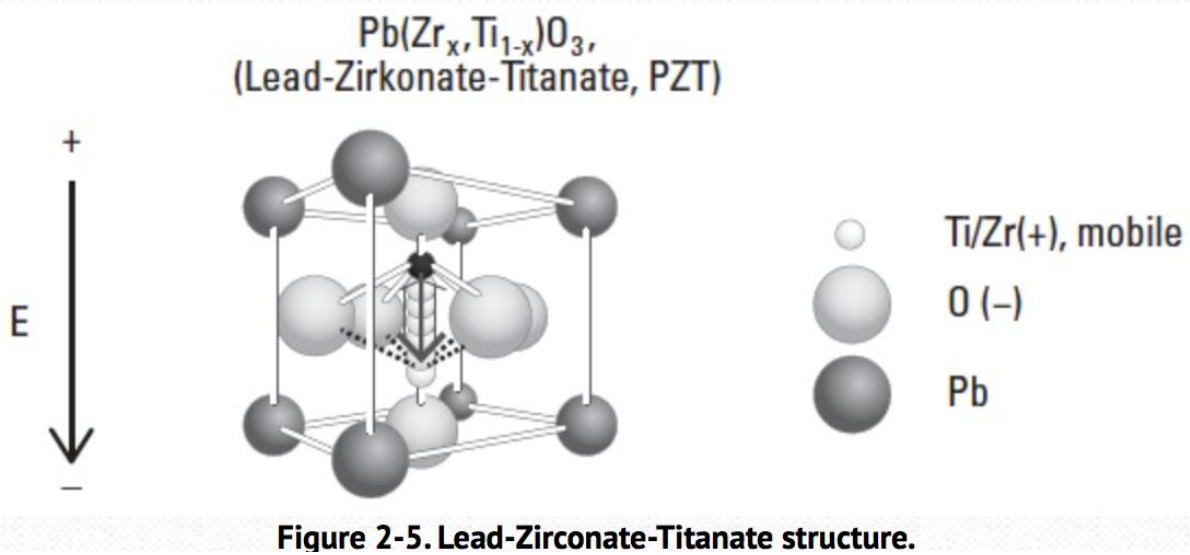


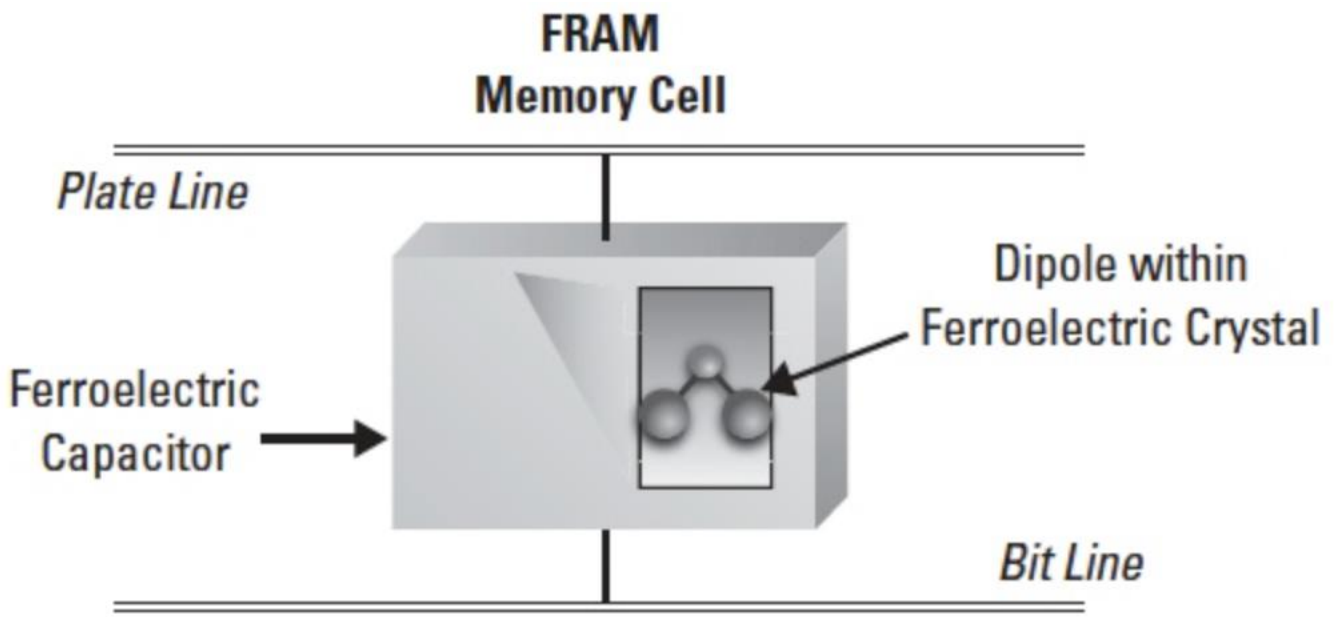
Figure 2-5. Lead-Zirconate-Titanate structure.

FRAM Technology

- Reliability/Security advantages of FRAM Technology
  - The lack of a charge pump removes a key vulnerability against physical attacks.
  - FRAM is also resistant to electric/magnetic fields as well as radiation. Since FRAM state is not stored as a charge, alpha particles are not likely to cause bits to flip and the FRAM Soft Error Rate (SER) is below detectable limits.
  - On top of this resistance to external interference, FRAM is anti-tearing, meaning power lost during a write/erase cycle will not cause data corruption.

http://www.ti.com/lsds/ti/microcontrollers_16-bit_32-bit/msp/ultra-low_power/msp430frxx_fram/what_is_fram.page?DCMP=ep-mcu-msp-fram-en&HQS=ep-mcu-msp-fram-b-lp-en#under

FRAM Read/Write Operations



- Read and write operations represent the fundamental way that data is accessed and stored in semiconductor memory.
- An FRAM memory cell consists of a ferroelectric capacitor containing crystalline PZT, which contain many ferroelectric domains, each of which has the same dipole orientation.
- The capacitor is connected to by a plate line and bit lines (see Figure 2-9) and a transistor switch to access the capacitor. For PZT materials, this is a titanium or zirconium ion in a lead/oxygen crystal lattice.

FRAM Read Operation

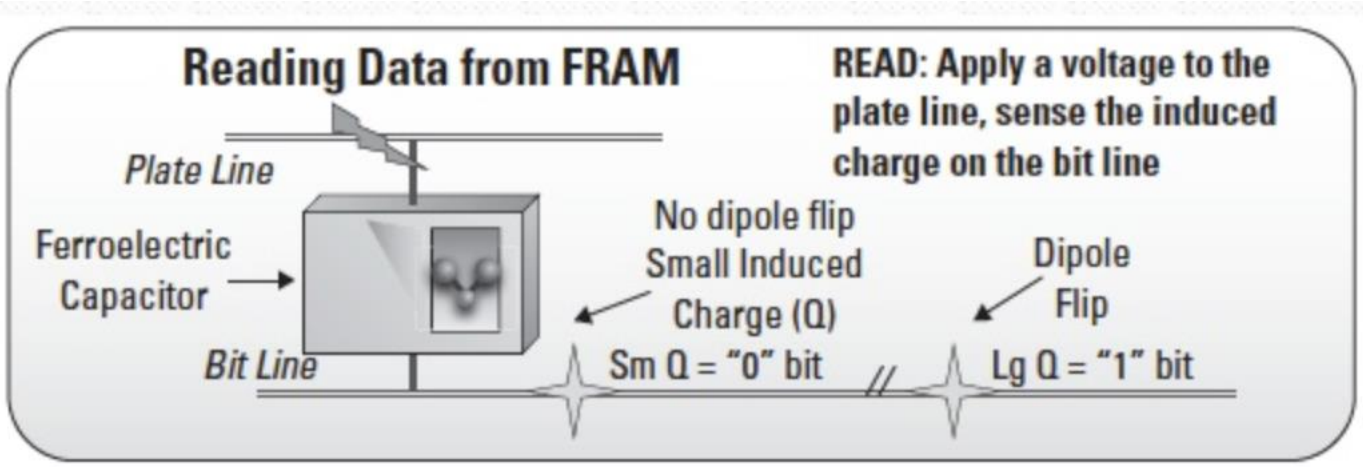


Figure 2-10. Reading a FRAM cell

- To read the data from a FRAM memory cell, a volt…d on the plate line; the key here is that you are al… …o a 0 state. If the voltage causes di… …on, then a large indu…
- If the orien… …ving voltage to the plate … …'t change and a small … …e bit line. So, in reading the data from an … …a small induced charge is a 0 bit and a large induced … …is a 1 bit (see Figure 2-10).

Potentially changing the state in order to perform a read, FRAM always requires a memory state refresh after a read.

FRAM Write Operation

- Writing to FRAM is also simple. To write a 1, you apply a voltage to the bit line to force a change in the orientation of the dipole to a positive 1 bit. To write a 0, you apply voltage to the plate line to move state to 0.

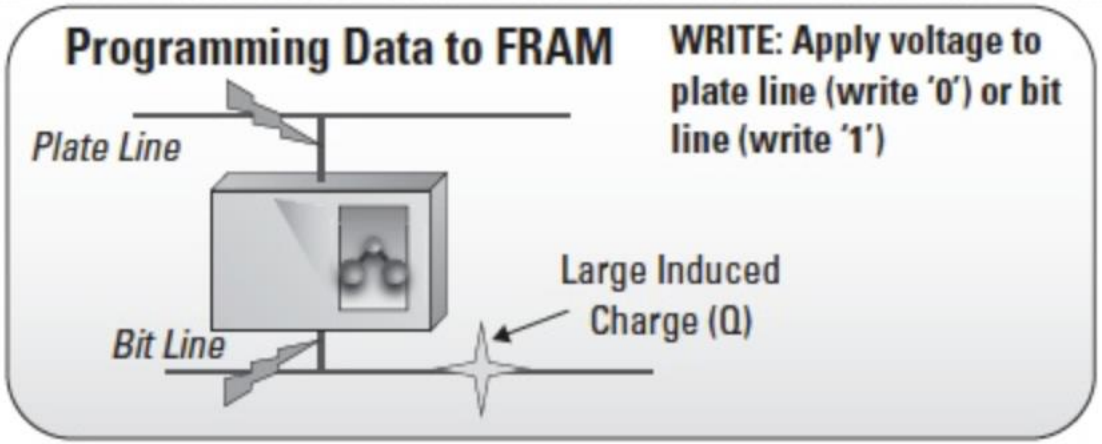


Figure 2-11. Writing to a FRAM cell.

FRAM memory comparisons

All-in-one: FRAM MCU delievers max benefits				
Specifications	**FRAM**	**SRAM**	**EEPROM**	**Flash**
Non-volatile *Retains data w/o power*	Yes	No	Yes	Yes
Write speed *(13 KB)*	10ms	<10ms	2 secs	1 sec
Average active Power [µA/MHz] *16 bit word access by the CPU*	100	<60	50,000+	230
Write endurance	10^{15}	Unlimited	100,000	10,000
Soft Errors	Below Measurable Limits	Yes	Yes	Yes
Bit-wise programmable	Yes	Yes	No	No
Unified Memory *Flexible code and data partitioning*	Yes	No	No	No

* Based on devices from Texas Instruments

http://www.ti.com/lsds/ti/microcontrollers_16-bit_32-bit/msp/ultra-low_power/msp430frxx_fram/what_is_fram.page?DCMP=ep-mcu-msp-fram-en&HQS=ep-mcu-msp-fram-b-lp-en#under

FRAM use cases

- Remote sensing or data logging
  - Lower energy
    - Fast writes
    - Low voltage and current is needed to change FRAM data
  - 10 billion times more cycles than Flash
- Over the air updates
  - Updating FRAM takes 100x less time and 250x less energy/bit
  - No pre-erase required
  - Data can be written on-the-fly
    - Data can be written to FRAM right out of the COMM channel, with no buffering required

http://www.ti.com/lsds/ti/microcontrollers_16-bit_32-bit/msp/ultra-low_power/msp430frxx_fram/what_is_fram.page?DCMP=ep-mcu-msp-fram-en&HQS=ep-mcu-msp-fram-b-lp-en#over-air

FRAM use cases (continued)

- Energy Harvesting
  - Low active duty cycle for non-volatile writes
    - Low average and peak write power leads to low average and peak power consumption of the MCU
  - Faster wakeup time
    - Variables stored in non-volatile FRAM Over the air updates
- Data Security
  - No charge pump needed
  - Resistance to external fields
    - Memory protected from some types of physical attacks
  - State retention on power fail, fast writes and 10 write cycles
    - FRAM is not susceptible to Soft Errors
    - Update security keys quickly and send notifications in case of certain state changes

http://www.ti.com/lsds/ti/microcontrollers_16-bit_32-bit/msp/ultra-low_power/msp430frxx_fram/what_is_fram.page?DCMP=ep-mcu-msp-fram-en&HQS=ep-mcu-msp-fram-b-lp-en#over-air

FRAM Advantages/Disadvantages

- **Advantages**
  - Lower power usage
  - Faster write performance
  - Much larger number of write-erase cycles
- **Disadvantages**
  - Lower storage density
  - Overall capacity limitation
  - Higher cost

The over riding disadvantage is cost. The FRAM cell structure is limited on how small the structure can be made. One limitation is that as structures become small, they tend to stop being ferroelectric. This effect is related to the ferroelectric's "depolarization field. ” Currently TI is building FRAM at 130nm linewidths where flash is being build in line widths as small as 16nm.

Radio-Electronics.com “FRAM Ferroelectric Random Access Memory Tutorial” and https://en.wikipedia.org/wiki/Ferroelectric_RAM#Density