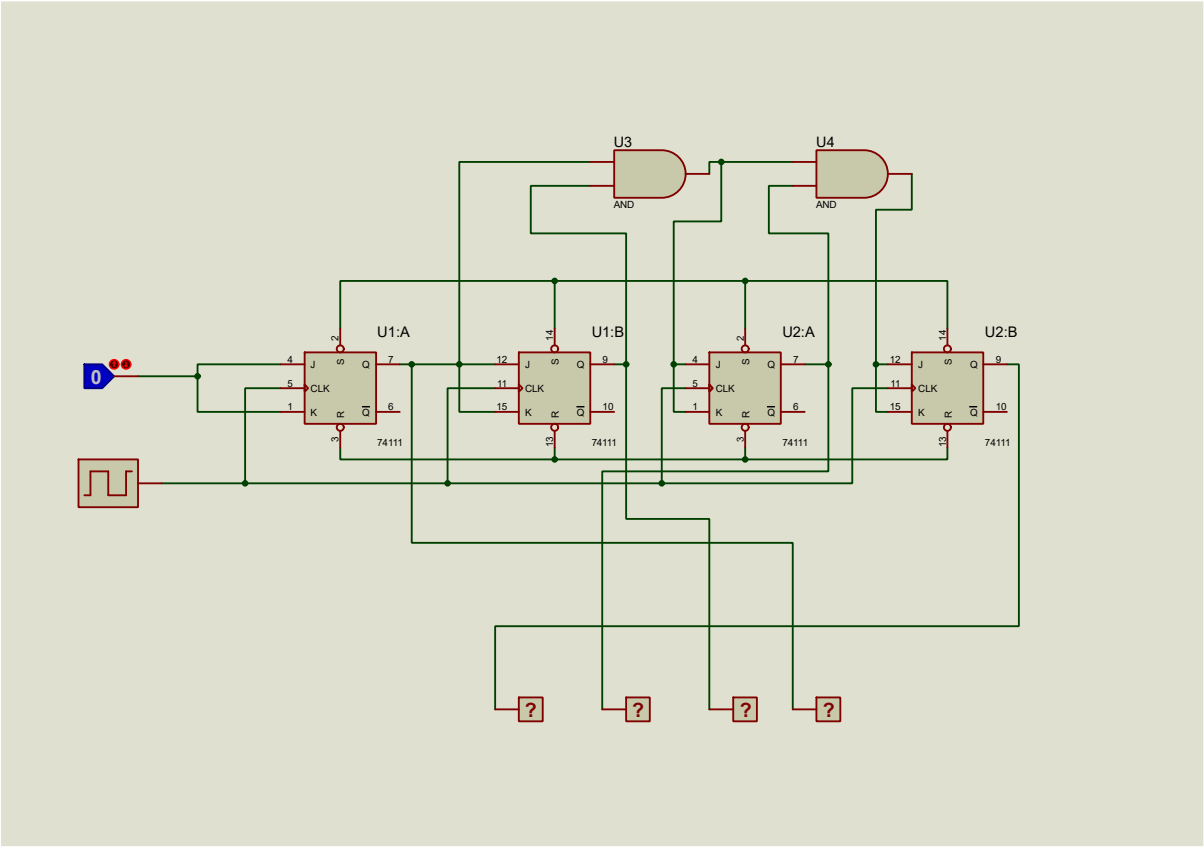
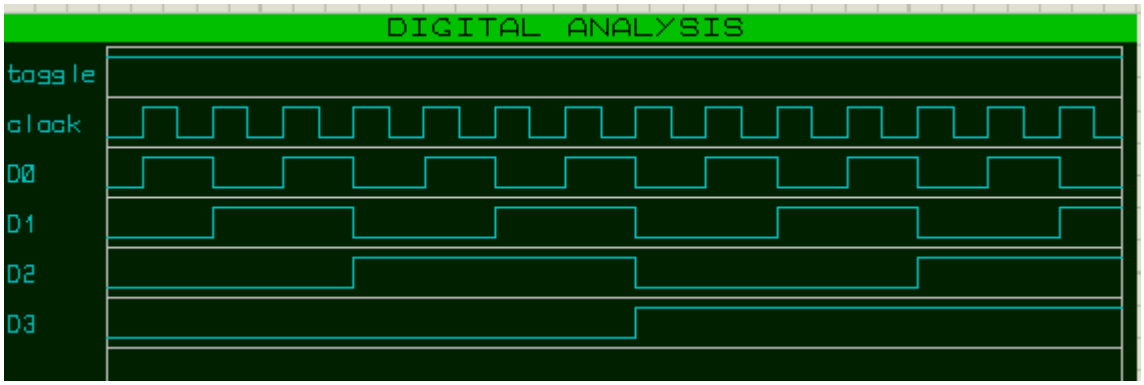
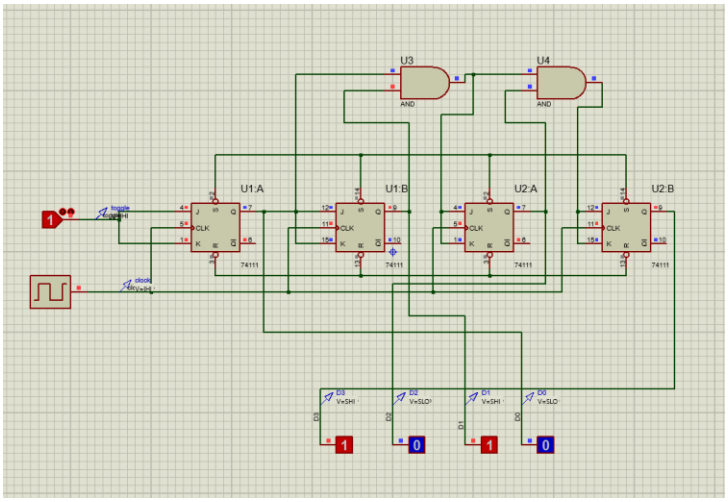
# Design, Simulation, and Implementation of a 4-bit Synchronous Binary Counter using JK flipflop

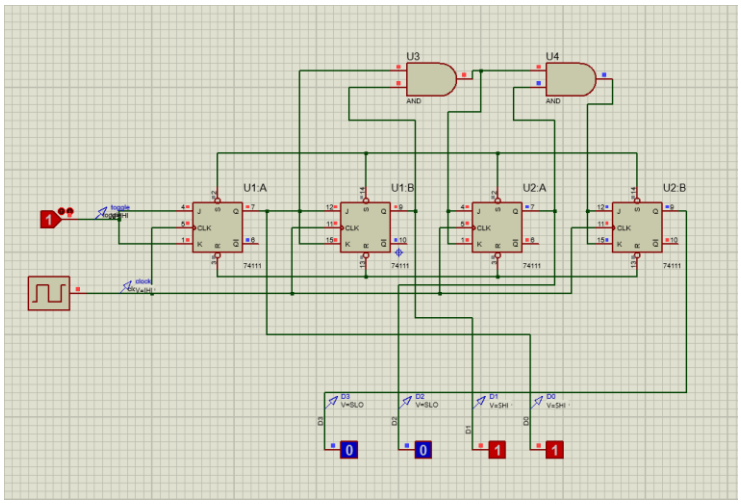
## Circuit diagram:



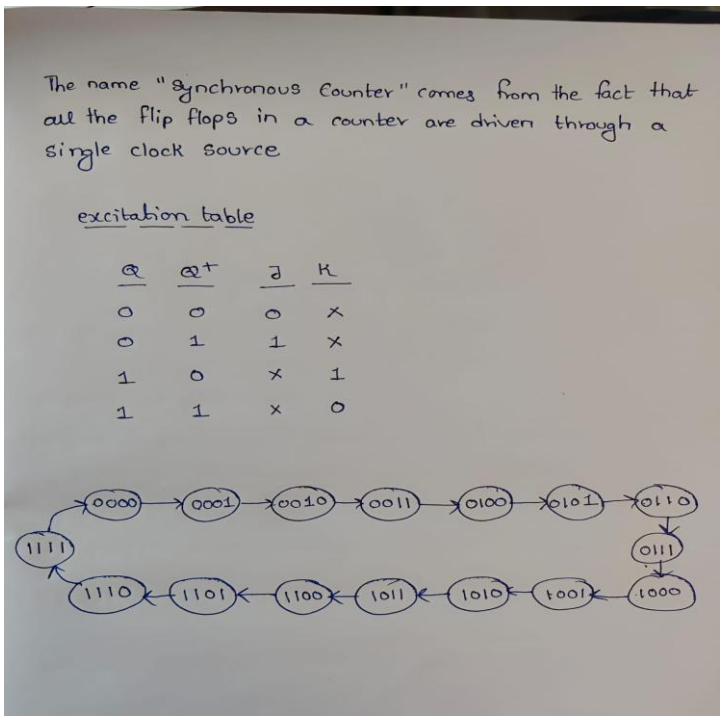

Outputs:





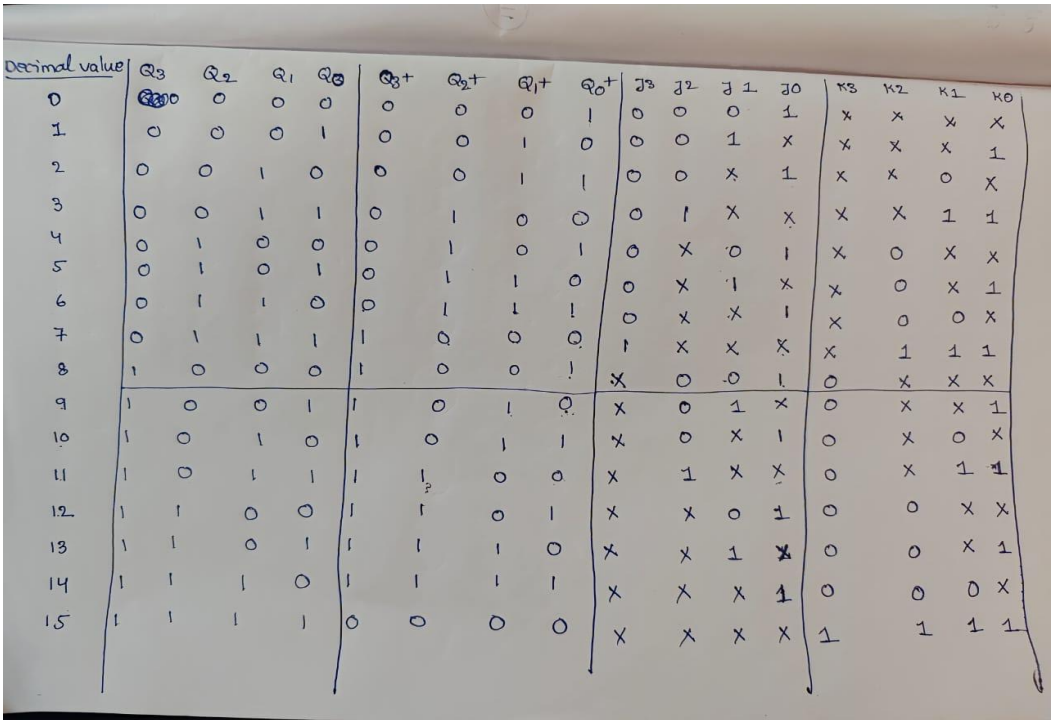

Theory work:



The name "synchronous counter" comes from the fact that all the flip flops in a counter are driven through a single clock source

excitation table

| Q | Q+ | J | K |
|---|---|---|---|
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | x |
| 1 | 0 | x | 1 |
| 1 | 1 | x | 0 |



| Decimal value | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | $Q_3+$ | $Q_2+$ | $Q_1+$ | $Q_0+$ | $J_3$ | $J_2$ | $J_1$ | $J_0$ | $K_3$ | $K_2$ | $K_1$ | $K_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | x | x | x | x |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | x | 1 | x | x | 0 | x |
| 3 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | x | 0 | 1 | x | 0 | x | x |
| 5 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | x | 1 | x | x | 0 | x | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | x | x | 1 | x | 0 | 0 | x |
| 7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | x | 0 | 0 | 1 | 0 | x | x | x |
| 9 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | x | 0 | 1 | x | 0 | x | x | 1 |
| 10 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | x | 0 | x | 1 | 0 | x | 0 | x |
| 11 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | x | 1 | x | x | 0 | x | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | x | x | 0 | 1 | 0 | 0 | x | x |
| 13 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | x | x | 1 | x | 0 | 0 | x | 1 |
| 14 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | x | x | x | 1 | 0 | 0 | 0 | x |
| 15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | x | x | x | x | 1 | 1 | 1 | 1 |