VISVESVARAYA TECHNOLOGICAL UNIVERSITY

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Mini Project Report

on

"Modelling and Simulation of Solar fed SPWM Operated Single Phase Inverter with Reduced Switches using MATLAB/SIMULINK"

Submitted in partial fulfillment for the requirement of

Mini Project [18ECMP68]

in

ELECTRONICS & COMMUNICATION ENGINEERING

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CERTIFICATE

This is to certify that, the VI Semester Mini Project work titled **"Modelling and Simulation of Solar fed SPWM Operated Single Phase Inverter with Reduced Switches using MATLAB/SIMULINK"** is carried out by **Amulya R [4MU20EC001]**, **Bhavana K [4MU20EC002]**, **Poorvi G.S [4MU20EC005]**, and **Akshata M Ulligeri [4MU21EC400]**, bonafide students of **Mysuru Royal Institute of Technology, Mandya**, in partial fulfillment for the requirement of Mini Project [18ECMP68] in the Department of Electronics & Communication Engineering, of the Visvesvaraya Technological University, Belagavi, during the year 2022-2023. The Mini project report has been approved as it satisfies the academic requirements with respect to the Mini Project work prescribed for the Bachelor of Engineering Degree.

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DECLARATION

We Amulya R, Bhavana K, Poorvi G.S, and Akshata M Ulligeri students of VI semester Bachelor of Engineering in Electronics and Communication Engineering, MRIT, Mandya, hereby declare that, this dissertation work titled "Modelling and Simulation of Solar fed SPWM Operated Single Phase Inverter with Reduced Switches using MATLAB/SIMULINK" has been carried out independently under the guidance of **ROOPA M**, Assistant Professor, Department of Electronics and Communication Engineering, MRIT, Mandya in partial fulfillment of the requirements for Mini Project [18ECMP68] in Bachelor of Engineering in Electronics and Communication Engineering, affiliated to Visvesvaraya Technological University (VTU), Belagavi during the Academic year 2022-2023.

We further declare that, this mini project has not been submitted with this dissertation either in part or full to any other university or institution for the award of other degree or any fellowship.

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ABSTRACT

Multilevel inverter's (MLI) have gained significant recognition in the field of high-power conversion due to its reduced voltage stress across the power semiconductor switches and low total harmonic distortion (THD) in the output voltage waveform. MLI's incorporates a large number of semiconductor switches and isolated dc sources, which increases its cost and complexity and reduces the reliability. In the proposed configuration of MLI's offers a reduced numbers of controlled switches as compared to conventional topologies. Reduction in switches reduces the cost, size, complexity and enhance the overall performance of the proposed topologies. Multicarriers pulse width modulation (MCPWM) strategy is adopted for generating the switching pulses. The detailed simulation study of the proposed topology for 7 level multi-level inverter model will be carried with the help of MATLAB/SIMULINK.

KEYWORDS: DC-AC power converters(inverters), Multi-level inverter's (MLI), Multicarrier pulse width modulation (MCPWM), Photovoltaic system (PV), Total harmonic distortion (THD).

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Chapter 1

Introduction

Nowadays the world community relies heavily on non-renewable energies, but just after the big oil crisis the use of renewable energy has greatly increased and has become the main interest of many countries for its many advantages such as: minimal impact on the environment, renewable generators requiring less maintenance than traditional ones and it has also a great financial impact on economy. Power electronic devices play a major role in the conversion and control of electric power, especially to extract power from renewable energy Sources Conversion of DC to AC power can be done with the help of inverters (single phase or three phases).

Inverters are the electronic devices that convert the direct current power into alternating power by using semiconductor switches like MOSFET, BJT, IGBT, GTO etc. Highly efficient inverters can be used in uninterrupted power supply, high voltage and medium voltage motor drives, FACTS, traction, and for harnessing renewable energy like wind, solar etc. But the conventional inverters are very high in cost, their efficiency is poor and they have very high switching losses. These disadvantages can be overcome by using cascaded multilevel inverters

Earlier inverters were made up to two levels, but with the advancement and research in the field has led to the development of multilevel inverters of higher orders like 05, 07, 09, and 11. The main advantage of increasing the level is that, it eliminates the harmonics and hence is very handy in reducing the total harmonic distortion of the inverter. These inverters can be designed using topology like diode clamped, cascaded H-bridge, flying capacitor topology. Multilevel inverter provides high quality output waveform. The efficiency of these inverters can be enhanced if they are operated at higher switching frequency with lower number of switches in system.

The involvement of modern power electronics converters in the emerging technology is essential for the electrical system in the current era. Multilevel inverter (MLI) is invented long year ago with the traditional popular topology Cascaded H-Bridge inverters (CHB-MLIs). The basic concept of a multilevel converter is to use a series of power semiconductor switches that properly connected to several lower dc voltage sources to synthesize a near sinusoidal stair

case voltage waveform.

The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency. It synthesis the multilevel output voltage waveform with the advantages of reduced voltage stress across the semiconductor devices and lower total harmonic distortion for the increase in levels.

Thus, the multilevel inverters (MLI) were developed Multilevel power conversion is used to provide more than two voltage level to achieve smoother and less Distorted dc to ac power conversion and it can generate A multiple-step voltage waveform with less distortion, Less switching frequency and higher efficiency. To fulfill the goals associated with applications of cascaded H-bridge multilevel inverters, design and implementation of their switching technique plays the key role. Reducing harmonics is one of the most important requirements associated with control of cascaded H-bridge multilevel inverters. Thus, study on switching patterns for this topology have attracted the attention of researchers.

The control method of cascaded H Bridge multilevel is more convenient than other multilevel inverter because it does not have any clamping diode and flying capacitor the cascaded inverter is used for large automotive electric drives. However, the requirement of a greater number of switches and separate dc source for each cell becomes a problem especially at higher level. Cascaded H-bridge multilevel inverter consists of separate dc links for each H-bridge cell, so it is easily controllable. The pulse-width modulation (PWM) control is the most efficient technique of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. By properly controlling the switching pattern, Total Harmonic Distortion (THD) can effectively be reduced. Several well-known switching techniques have been introduced over the past two decades to control the output voltage of the inverter while minimizing THD of the output waveform. These techniques include sinusoidal pulse width modulation (SPWM).

The cascaded multi-level control method is very easy to build a circuitry when compared to other multi-level inverters, because it does not require any clamping diode and flying capacitor. There are two PWM methods mainly used in multi-level inverter control strategy, one is fundamental switching frequency and another one is high switching frequency.

In this work, the different parameters like (voltage, current, THD) in single phase full bridge inverter, 7-level cascaded multi-level inverter with reduced number of switches are presented. The researchers have taken a problem to analyse and understand the effectiveness of 7-level multi-level inverter with reduced number of switches using MATLAB/SIMULINK.

Simulink is a MATLAB-based graphical programming environment for modelling, simulating and analysing multidomain dynamical systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries. The simulation has been carried out using MATLAB/Simulink software. The comparative results of the harmonic analysis for different levels have been obtained in MATLAB/SIMULINK.

1.1 Introduction to Inverters

The inverter is an electrical device that converts DC input supply to symmetric AC voltage of standard magnitude and frequency at the output side. It is also named as DC to AC converter. An ideal inverter input and output can be represented either in a sinusoidal and non- sinusoidal wave forms. If the input source to the inverter is a voltage source, then the inverter is said to be called a voltage source inverter (VSI) and if the input source to the inverter is a current source, then it is called as current source inverter (CSI). Inverters are classified into 2 types according to the type of load being used i.e., single-phase inverters, and three-phase inverters. Single-phase inverters are further classified into 2 types of half-bridge inverter and full-bridge inverter. A full bridge single phase inverter is a switching device that generates a square wave AC output voltage on the application of DC input by adjusting the switch turning ON and OFF based on the appropriate switching sequence.

The basic inverter full bridge circuit diagram is as shown in fig. (1.1).

Multilevel Inverter: Multilevel inverters have been widely used in many applications since the technology is advantageous to increase the converter capability as well as to improve the output voltage quality. Multilevel inverters are able to produce a staircase output wave- form, that is more approaching sinusoidal and produce less number of harmonics compare to the conventional inverter output voltage. The multilevel inverter can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency.

It should be noted that the lower switching frequency means lower switching loss and higher

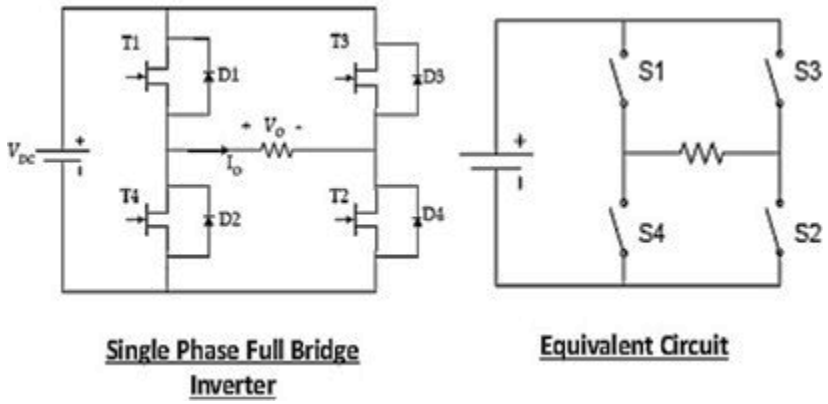

Figure 1.1: Basic Inverter diagram

efficiency is achieved. Multilevel inverters are of three types.

1. Diode clamped multilevel inverter
2. Flying capacitors multilevel inverter
3. Cascaded H- bridge multilevel inverter

The basic multilevel inverter circuit diagram and its output wave forms are as shown in fig. (1.2a) and fig. (1.2b).

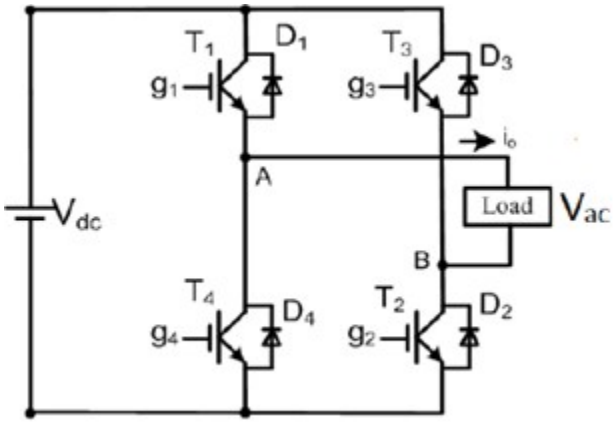

Fig. (1.2a)

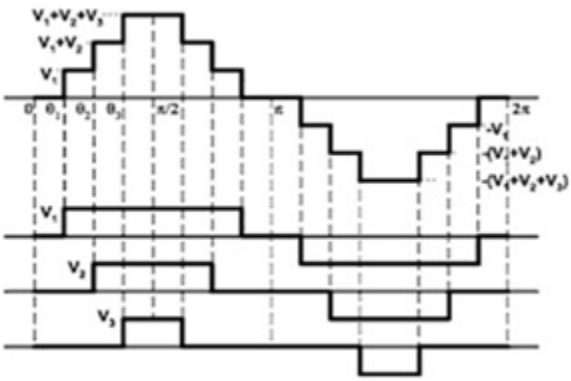

Fig. (1.2b)

Cascaded H-Bridge Multilevel Inverter: The cascaded H-bride multilevel inverter is to use capacitors and switches and requires less number of components in each level. This topology consists of a series of power conversion cells and power can be easily scaled. The combination of capacitors and switches pair is called an H-bridge and gives the separate input DC voltage for each H-bridge. The cascaded H-Bridge multilevel inverter circuit is as shown in fig.(1.3).

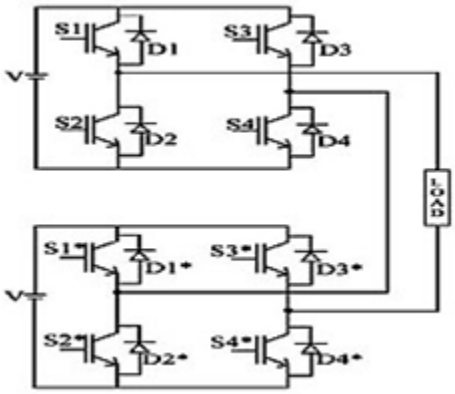

Figure 1.3: Cascaded H-Bridge multilevel inverter

It consists of H-bridge cells and each cell can provide the three different voltages like zero, positive DC, and negative DC voltages. One of the advantages of this type of multi-level inverter is that it needs less number of components compared with diode clamped and flying capacitor inverters. The price and weight of the inverter are less than those of the two inverters. Soft-switching is possible by some of the new switching methods. Multilevel cascade inverters are used to eliminate the bulky transformer required in case of conventional multi-phase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. But these require a large number of isolated voltages to supply each cell.

Benefits of Cascaded H-bridge MLI configuration are given below:

1. Stepped waveform with improved quality which reduced electromagnetic compatibility.
2. It results modularity of control.
3. The same number levels in output voltage with this configuration can be obtained with less switches when compared with the other type configurations of multi-level inverters.
4. This inverter can draw input current with reduced distortions.
5. Less weight and price is comparatively less.
6. It eliminates the bulky transformer required.

Demerits of Cascaded H-bridge MLI configuration are as listed:

1. Communication between full bridges must achieve synchronization with the reference carrier wave forms.
2. This requires that the power source voltage for separate conversions, and thus to be somewhat limited applications.

Applications of Cascade H-Bridge Multilevel Inverter:

1. Motor filters, active filters.
2. Electric vehicle drives.
3. DC power source utilization.
4. Power factor compensators.
5. Inerface with renewable energy resources.

The multilevel based cascaded H bridge inverter requires a greater number of cascaded cells which increase the levels in output voltage waveform with independent DC voltage sources for each bridge. It is a simple method to generate a waveform closer to the **sine wave** as shown in fig.(1.4). The total harmonic distortion in the output voltage can be improved and then the output must be filtered to meet desired requirements related to THD.

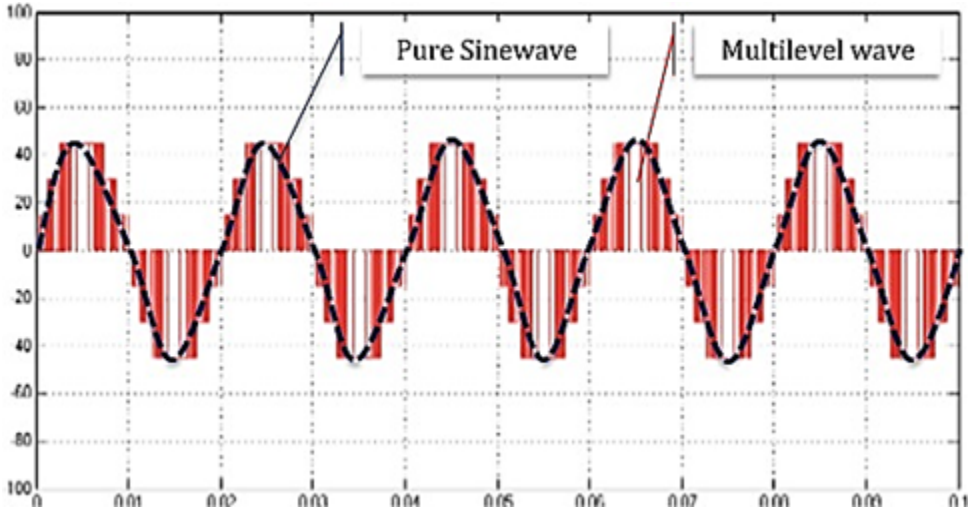

Figure 1.4: Multilevel output wave form of inverter

Pulse Width Modulation[PWM]: Pulse-width modulation (PWM), is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate. The longer the switch is on compared to the off periods, the higher the total power supplied to the load. PWM is particularly suited for running inertial loads such as motors, which are not as easily affected by this discrete switching, because their inertia causes them to react slowly.

The PWM switching frequency has to be high enough not to affect the load, which is to say that the resultant waveform perceived by the load must be as smooth as possible. According to different PWM technique:-

1. Simple pulse width modulation (SPWM)
2. Multiple pulse width modulation (MPWM)
3. Sinusoidal pulse width modulation (SinPWM)

Sinusoidal Pulse Width Modulation[SPWM]: Sinusoidal pulse width modulation is a method of pulse width modulation used in inverters. An inverter produces an AC output voltage from a DC input by using switching circuits to simulate a sine wave by producing one or more square pulses of voltage per half cycle. If the widths of the pulses are adjusted as a means of regulating the output voltage, the output is said to be pulse width modulated. With sinusoidal or sine weighted pulse width modulation, several pulses are produced per half cycle. The pulses near the edges of the half cycle are always narrower than the pulses near the center of the half cycle such that the pulse widths are proportional to the corresponding amplitude of a sine wave at that portion of the cycle. To change the effective output voltage, the widths of all pulses are increased or decreased while maintaining the sinusoidal proportionality.

Sinusoidal PWM is a typically Triangular method (natural sampling) PWM technique. In this PWM technique, the sinusoidal AC voltage (modulating or reference V_{ref}) is compared with the high-frequency amplitude of the triangular wave (carrier wave (V_C)). A simple analogue comparator can be used. Basically an analogue method. Its digital version, known as REGULAR sampling is widely used in industry. Carrier wave (V_C) in real time to determine switching states for each pole in the inverter. After comparing, the switching states for each pole can be determined on the following rules:

- Voltage reference (V_{ref}) $>$ Triangular carrier (V_C): Upper switch is turned On (pole voltage=$\frac{V_{dc}}{2}$).
- Voltage reference (V_{ref}) $<$ Triangular carrier (V_C): Lower switch is turned On (pole voltage=$-\frac{V_{dc}}{2}$).

The output waveform of the comparator in terms of the pulse generated are as shown in fig. (1.5). Here, the peak-to-peak value of the triangular carrier wave is given as the DC-link voltage (V_{dc}).

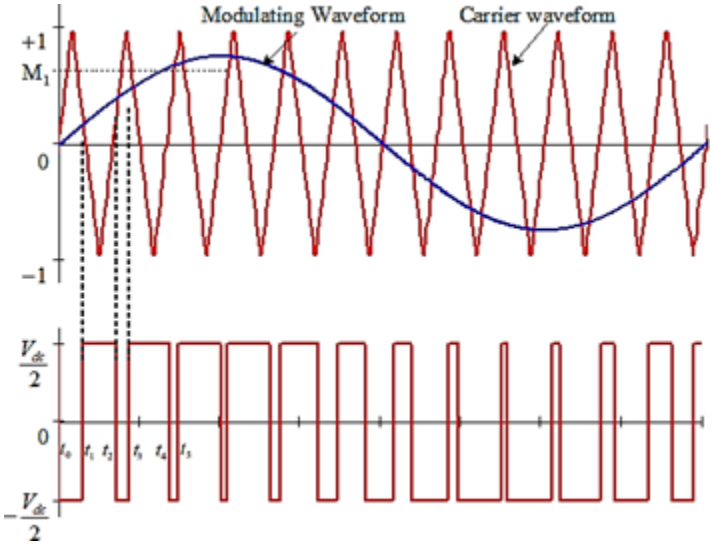

Figure 1.5: Pulse generation

In this PWM technique, the necessary condition for linear modulation is that the amplitude of the voltage reference (V_{ref}) must remain below the peak of the triangular carrier (V_C), i.e., ($V_{ref} \leqslant \frac{V_{dc}}{2}$). Since this PWM technique utilizes a high-frequency carrier wave for voltage modulation, this kind of PWM technique is called a carrier-based PWM technique. Especially, this carrier-based technique is called SPWM, since the reference is given as the shape of a sine wave.

Advantages of SPWM:

1. Low power consumption.
2. High energy efficient upto 90%.
3. High power handling capability.
4. No temperature variation-and aging-caused drifting of degradation in linearity.
5. Easy to implement and control.
6. Compatible with today's digital microprocessors.

1.2 Methodology

The electrical energy obtained from the PV array system at constant voltage is fed to inverter circuit. The inverter circuit may consists of cascaded, H-bridge circuits which may be used for different output levels. The switching operation of an inverter circuit is carried by generating a pulse from the concept of multi-carrier pulse width modulation.

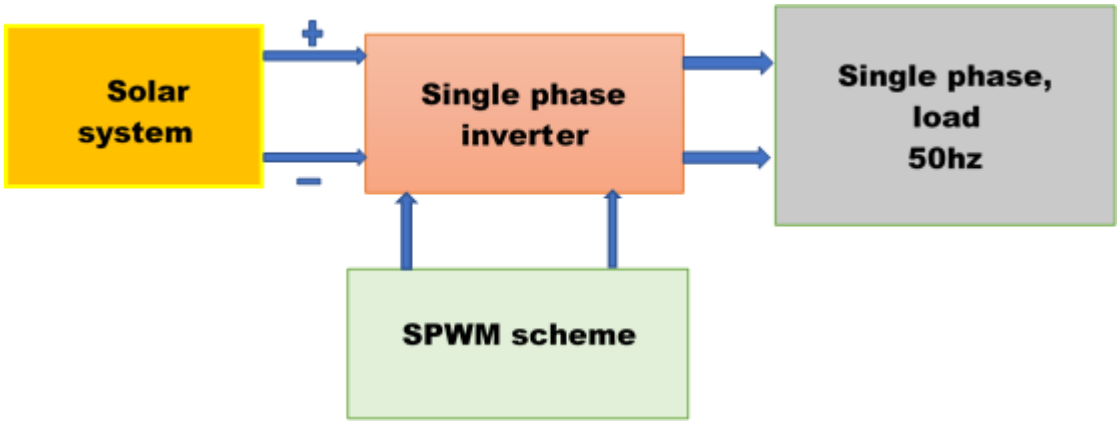

Figure 1.6: Typical block diagram of multi-level inverter

The general block diagram of a single-phase inverter which is fed from solar system is shown in figure (1.6).

A series connected set of multi-level inverter blocks will achieve a stepped waveform. Each of the power DC sources is equal to V_{dc}; hence the circuit is also described as a symmetrical multi-level inverter. Hence more power sources, more steps in the waveform. Hence, sinusoidal wave inverter leading to less power losses, consequently less heat generation.

The circuit diagram of 7-level, cascaded H-bridge inverter and 7-level output voltage waveform are as shown in figure (1.7) and figure (1.8).

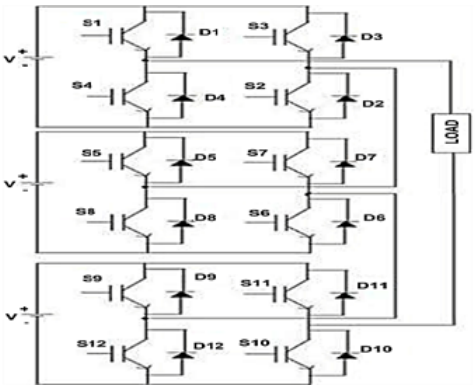

Fig.(1.7): 7-level cascaded H-bridge inverter

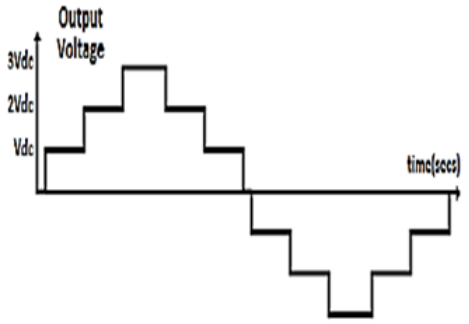

Fig.(1.8): 7-level output voltage waveform

But, in the present work, the 7-level multi-level inverter is operated with reduced components or devices, and hence the gate driver circuits required for semiconductor switches also reduces and there by reducing the complexity of the overall circuit.

1.3 Objectives

The main object of the project is to modelling, simulation, and analysis of solar based 7-level multi-level inverter with reduced number of switches. So the objectives are to understand the behavior of the following.

- Generation of multi-level pulse width modulation [PWM].
- Modelling and simulation of 3-level inverter.
- Modelling and simulation of 5-level inverter.
- Modelling and simulation of 7-level inverter.
- Modelling and simulation of 7-level inverter with reduced number of switches.
- To compare the inverter output waveforms of different levels, to validate the performance of the inverters.

1.4 Software Description

MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment, where problems and solutions are expressed in familiar mathematical notation, data analysis, exploration, and visualization. Modelling and simulation are the use of models as a basis for simulations to develop data utilized for managerial or technical decision making. In the computer application of modelling and simulation a computer is used to build a mathematical model which contains key parameters of a physical model. Simulation modelling is the process of creating and analysing a digital prototype of a physical model to predict its performance in the real-world simulation modelling which is used to help designers and engineers understand whether, under what conditions, and in which way a physical system could fail and what loads it can withstand.

1.5 Organization of the dissertation

Chapter 2 describes the literature review which presents the idea about basics inverters, multilevel inverters, and their different controlling schemes using PWM's. There are many researches have presented the modeling of multilevel inveters of different concept or techniques in reduction of total harmonic distortion and hence quality of output of an inverter is in-

creased.

Chapter 3 explains an overview of inverters and its working procedure. Here it is discussed about the working principle of single-phase full bridge inverter with the block diagram. Also described the different multilevel inverters and the concept of cascaded H-bridge multilevel inverters. It also provides information on control schemes used to operate the semiconductor devices like MOSFET's/IGBT's (Switches) and selected one of the technique as phase deposition of SPWM which is best suited for decreasing THD at output voltage of an inverter.

Chapter 4 gives the design and modeling of single-phase cascaded H-bridge multilevel inverters. The consideration of different output voltage levels of inveters such as three, five, seven, and nine level are explained with their switching states and generation of pulses required to turn-On the devices. Also presented the modeling of these multilevel inverters using MATLAB/SIMULINK.

Chapter 5 presents the Simulation results and discussions in reduction of THD & hence improvement of power quality at the output of an inverter and further improvement required in the work about reduction of switches, switching losses with advanced PWM techniques.

Chapter 6 gives the Conclusion of work executed and it's limitations. Also future enhancement of the work with different advance techniques are also mentioned.

Chapter 2

Literature Review

The literature review presents the idea about existing system and their problems. There are many researches have presented the modeling of different multilevel inveters with sinusoidal pulse width modulation, and the reduction in total harmonic distortion to improve the power quality at output of an inverters with reduced number of devices, in order to decrease cost, size and complexity of generating switching pulses.

2.1 Technical Journal and Conference Papers

1 C. DhanamJayulu, Sanjeevkumar Padmanaban, Jens Bo Holm-Nielsen, Frede Blaabjerg, "Design and implementation of a single phase 15-level inverter with reduced components for solar PV applications" [2021]. This paper proposes the detailed comparison of single-phase multi-level inverter with reduced components for solar PV applications with existing MLI's. The proposed inverter can improve efficiency and reduce losses, cost, and complexity of overall system.

2 Munesh Kairon, Raj Kiran, Rahul Mishra, "Photovoltaic based a 7-level multi-level inverter with reduced number of switches" [2017]. This paper presents a multi-level inverter concept with reduced number of switches to decrease the voltage stress and losses in semiconductor devices, when they are made On/Off. The smaller number of semiconductor switches used in MLI's circuit becomes less complex, the size and installation area reduce.

3 Thiyagarajan Venkatraman, Somasundaram Periasamy, "Multi-level Inverter Topology with Modified Pulse Width Modulation and Reduced Switch Count" [2018]. This paper proposes a new inverter topology with minimum switches, which generates a large numbers of output voltage levels. The major advantages of the presented topology are minimum number of power switches, minimum cost, reduction in installation area and less switching losses. Comparative analysis of the proposed inverter topology with earlier presented topologies shows that the performance of the proposed topology is improved as compared with conventional and other recently developed topology. The performance

of the presented inverter has been analysed by simulation, using MATLAB.

4 G. Nageswara Rao, K. Chandra Sekhar, P. Sanganeswararaju, "An Effective Technique for Reducing Total Harmonics Distortion of Multi level Inverter" [April-2018]. In this paper, an adaptive neuro fuzzy interference system (ANFIS) is proposed for eliminating voltage harmonics present in the multi-level inverter. It is achieved by reducing the total harmonic distortion (THD) present in the multi-level inverter output voltage. Here, the voltage variation of the multi-level inverter is determined from the actual load voltage and the reference voltage. The voltage variations at different time intervals have been applied to the ANFIS. According to the voltage variations, the switching angles can be generated from the interference system. These switching angles can make the multi-level inverter output voltage with reduced THD.

Chapter 3

Inverter

3.1 Introduction

The inverter is an electrical device that converts DC input supply to symmetric AC voltage of standard magnitude and frequency at the output side. It is also named as DC to AC converter. An ideal inverter input and output can be represented either in a sinusoidal and non-sinusoidal waveforms. If the input source to the inverter is a voltage source, then the inverter is said to be called a Voltage source inverter (VSI) and if the input source to the inverter is a current source then it is called as Current source inverter (CSI). The simple block diagram of an inverter is shown in figure.(3.1).

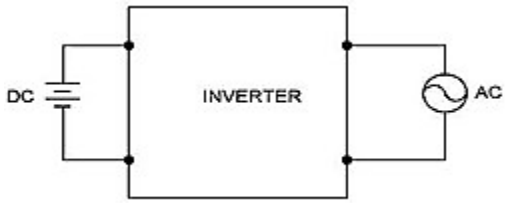

Figure 3.1: Block diagram of an inverter

Inverters are classified into 2 types according to the type of load being used i.e, single-phase inverters, and three-phase inverters. Single-phase inverters are further classified into 2 types of half-bridge inverter and full-bridge inverter. A full bridge single phase inverter is a switching device that generates a square wave AC output voltage on the application of DC input by adjusting the switch turning ON and Off based on the appropriate switching sequence. The inverters can generate only two levels in the output voltage. Hence, the output voltage contains more harmonics. The Pulse width modulated (PWM) strategy is Used to reduce the low frequency harmonic components for the two level output voltage. Inverters are classified based on output voltage(output waveform) of an inverter & the amplitude of ac voltage required to generate and type of load connected across the output of an inverter. According to the output waveform:

1. Square wave inverter
2. Modified sine wave inverter
3. Sine wave inverter.

According to the type of load:

1. **Single phase inverter:** If the load is a single phase, the inverter used to run the load that is the single phase inverter. There are two types:-
   - ★ Half bridge inverter
   - ★ Full bridge inverter
2. **Three phase inverter:** Generally, three phase AC supply used in industries and the load is three-phase. In this case, a three-phase inverter used to run this load. Here, six diodes and six thyristors are used. According to the conduction time of thyristor, this inverter divides into two types:-
   - ♦ 120^o mode of conduction
   - ♦ 180^o mode of conduction

Applications of Inverter: Some of the applications of an inverter include:

- ► When the main power is not available, an uninterrupted power supply (UPS) uses battery and inverter.
- ► The power inverter used in the HVDC transmission line. It also used to connect two asynchronous AC systems.
- ► The output of the solar panel is DC power. The solar inverter used to convert DC power into AC power.
- ► It can convert the low-frequency AC power to a higher frequency which used in induction heating.
- ► The inverter produces variable output voltage by using a control unit (close- loop inverter). The speed of inverter controlled by supplying variable voltage. For example, it used in the refrigerator compressor motor, rail transport, induction motor speed control, electric vehicle.

3.2 Multilevel inverter

Though PWM inverters reduce the harmonics for the output voltage, they have many disadvantages; hence power electronic researchers are moving towards multilevel inverters (MLI). To improve the voltage profile and efficiency of the overall system, multilevel inverters (MLIs) are introduced. In multilevel inverters the voltage at the output terminal is generated from several DC voltage levels fed at its input. With the invention of multilevel inverters, the power rating of the device was increased owing to the number of levels and the device count was reduced when compared to conventional models. Which is also a very important alternative in the area of energy control. Multi-level inverters are able to produce a staircase output waveform as no of level increases the Total Harmonic Distortion [THD] can be reduced. Multilevel inverters are classified into four types.

1. Flying Capacitor Multi-Level Inverter
2. Diode-Clamped Multi-Level Inverter.
3. Hybrid Multi-Level Inverter.
4. Cascade H-Bridge Multi-Level Inverter.

The number of levels of inverter can be defined as the number of steps or constant voltage values that can be generated by the inverter between the output terminal and any arbitrary internal reference node within the converter. The inverters with voltage level 3 or more are referred as multilevel inverters. Multilevel inverters have become attractive recently particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage.

3.3 Cascade H-bridge multi-level inverter

The cascaded H-bride multilevel inverter is to use capacitors and switches and requires less number of components in each level. This topology consists of a series of power conversion cells and power can be easily scaled. The combination of capacitors and switches pair is called an H-bridge and gives the separate input DC voltage for each H-bridge. Multilevel cascade inverters are used to eliminate the bulky transformer required in case of conventional multi-phase

inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. But these require many isolated voltages to supply each cell. To fulfil the goals associated with applications of cascaded H-bridge multilevel inverters, design and implementation of their switching technique plays the key role. Reducing harmonics is one of the most important requirements associated with control of cascaded H-bridge multilevel inverters.

Cascaded H-Bridge Multilevel Inverters [CHB-MLIs] shown in Fig.(3.2) are formed by the back to back series connection of two or more single-phase H-bridge inverters, hence as the name suggest cascade. Each cascade H-bridge corresponds to voltage source in each bridge. Therefore, a single H-bridge converter is able to generate three different voltage levels and series connection of N such bridges will be able to produce $(2N+1)$ levels in the output of the inverter. This series connection is known as cascaded H-bridge multilevel inverter.

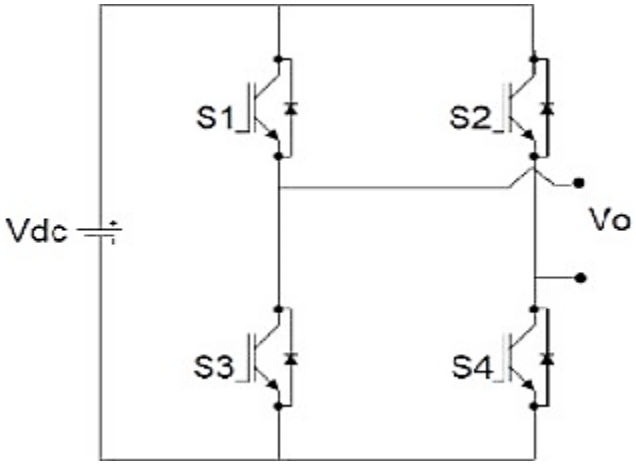

Figure 3.2: Single phase full bridge inverter

3.3.1 Single pulse Modulation

The output voltage from single phase cascaded H-bridge inverter is shown in figure (3.3). When this waveform is modulated, the output voltage is of the form. It consists of a pulse of width 2d located symmetrically about $\frac{\pi}{2}$ and another pulse located symmetrically about $\frac{3\pi}{2}$. The range of pulse width 2d varies from 0 to π, that is $0 < 2d < \pi$. The output voltage is controlled by varying the pulse width 2d. This shape of the output voltage is called as **Quasi square wave.**

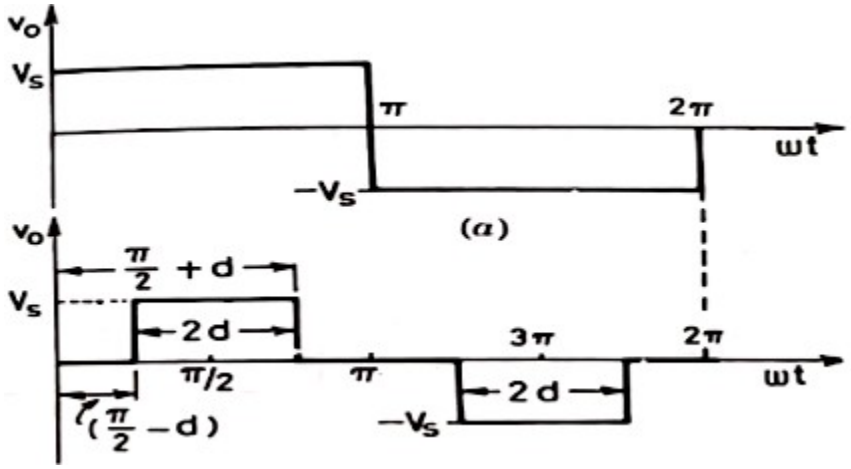

Figure 3.3: Single-pulse modulation

Fourier analysis is as under:

$$b_n = \frac{2}{\Pi}\int_{(\pi/2-d)}^{(\pi/2+d)} V_s sin(n\omega t).d(\omega t)$$

$$b_n = \frac{4V_s}{n\pi}\left[sin\frac{n\pi}{2}\right] sinnd \tag{3.1}$$

Positive and negative half cycles of V_0 are symmetrical about $\frac{\pi}{2}$ and $\frac{3\pi}{2}$ respectively. In addition, these half cycles are also identical. As a result, coefficient $a_n = 0$. Thus the waveform can be described by Fourier series as

$$v_0 = \sum_{n=1,3,5..}^{\infty} \frac{4V_s}{n\pi} sin\frac{n\pi}{2}\,(sinnd)\, sinn\omega t \tag{3.2}$$

$$v_0 = \frac{4V_s}{\pi}\left[sind.sin\omega t - \frac{1}{3}sin3d.sin\omega t + \frac{1}{5}sin5d.sin5\omega t\right] \tag{3.3}$$

When pulse width 2d is equal to its maximum value of π radians, then the fundamental component of output voltage, from equation (3.3) has a peak value of

$$v_{01m} = \frac{4V_s}{\pi} \tag{3.4}$$

For pulse width other than $2d = \pi$ radians, the peak value of fundamental component is $\frac{4V_s}{\pi} sind$. If nd is made equal to π or d=$\frac{\pi}{n}$ or if pulse width is made equal to $2d = \frac{2\pi}{n}$, shows that nth harmonic is eliminated from the inverter output voltage. For example, for eliminating third harmonic, pulse width of 2d must be equal to $\frac{2\pi}{3} = 120^o$.

The peak value of nth harmonic from equation (3.2) is

$$v_{0nm} = \frac{4V_s}{n\pi} sinnd \tag{3.5}$$

from equations (3.4) and (3.5)

$$\frac{v_{0nm}}{v_{01m}} = \frac{sinnd}{n} \tag{3.6}$$

In equation (3.6), note that v_{01m} is the peak value of the fundamental component of square voltage waveform of width $2d = \pi$. The ratio is plotted for n=1(plot of sind), n=3(plot of sin $\frac{3d}{3}$), n=5,7 for different pulse widths. It is seen from these curves that when fundamental component is reduced to 0.5 for 2d=60^o, the amplitude of third harmonic is $\frac{1}{3} sin90^o$=0.33. When fundamental component is reduced to about 0.143, all three harmonics (3,5,7) become almost comparable to the fundamental. This shows that in this method of voltage control, a great deal of harmonic content is introduced in the output voltage, particularly at low output voltage levels.

The rms value of output voltage from figure (5.2) is,

$$V_{0r} = \left[\frac{V_s^2.2d}{\pi}\right]\left(\frac{1}{2}\right) \quad = V_s\left[\frac{2d}{\pi}\right]\left(\frac{1}{2}\right) \tag{3.7}$$

To acquire the spectrum of the output voltage (THD), the Fast Fourier Transform (FFT) is applied. The THD is calculated using the following equation (3.8):

$$\text{Total harmonic distortion} = \frac{\sqrt{\sum_{x=1}^{\infty} v_n^2}}{v_1} \tag{3.8}$$

Where: 'n' is the harmonic order. v_n is the root mean square (RMS) value of the n^th harmonic component . v_1 is the (RMS) value of the fundamental component.

While using H-bridge inverter various problems have been faced and these problems can be solved using cascading the H-bridge inverters. Summary of the problems associated with H-bridge inverter and their solution of the problem is given in the table (3.1).

Table 3.1: Comparison between H-bridge MLI and cascaded H-bridge MLI

Sl	H-bridge inverter demerits	Solution using cascade MLI
1	High electrical stress on device	More than one semiconductor switches in series is used. Hence electrical stress divide across all.
2	High total harmonic distortion	Low voltage appears across any switch so low harmonics are generated due to switching
3	Radio interference	Comparatively low voltage and current is chopped so radio interference is low.
4	Due to high THD, large, costly and complex filter circuit is required.	THD is low, so simple circuit can be used.
5	High cost of switching device, because of higher voltage rating	As low voltage will appear across each device, cost of devices will somewhat less.

3.4 Pulse width modulation (PWM)

Inverter output voltage additionally may be adjusted with the aid of workout a control within the inverter itself. Pulse-width modulation (PWM), is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load On and Off at a fast rate. The longer the switch is On compared to the off periods, the higher the total power supplied to the load. Pulse width modulation is the most usually used approach to manipulate the output voltage of inverter, the numerous techniques are:

1. Single Pulse Width modulation (single PWM)
2. Multiple Pulse Width Modulation (MPWM)
3. Sinusoidal Pulse Width Modulation (SPWM)
4. Modified Sinusoidal Pulse Width Modulation (MSPWM)

3.5 Sinusoidal pulse width modulation (SPWM)

The term SPWM stands for “Sinusoidal pulse width modulation” is a technique of pulse width modulation used in inverters. An inverter generates an output of AC voltage from an input of

DC with the help of switching circuits to reproduce a sine wave by generating one or more square pulses of voltage per half cycle. If the size of the pulses is adjusted, the output is said to be pulse width modulated. With this modulation, some pulses are produced per half cycle. The pulses close to the ends of the half cycle are constantly narrower than the pulses close to the center of the half cycle such that the pulse widths are comparative to the equivalent amplitude of a sine wave at that part of the cycle. To change the efficient output voltage, the widths of all pulses are amplified or attenuated by keeping the sinusoidal proportionality. With pulse width modulation, only the On-time of the pulses are changed during the amplitudes.

Triangular multi-carrier technique analysis: This topology uses triangular signals with high frequency as carriers as shown in figure (3.4) and constantly compares them to a sinusoidal signal to generate pulses and all the carrier waves should have similar frequency and the same peak.

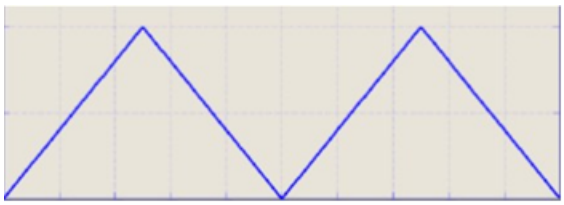

Figure 3.4: Triangular carrier waveform

The above triangular waveform may expressed in time domain function as follows.

$$U(t) = \begin{cases} \dfrac{t}{(T/2)} & 0 \leqslant t \leqslant T/2 \\ \dfrac{(T-t)}{(T-T/2)}.A & T/2 \leqslant t \leqslant T \end{cases} \tag{3.9}$$

where, ‘A’ is the amplitude and ‘T’ is the time period of the carrier signal.

In Multi-Pulse modulation(MPM), the pulse width is equal for all the pulses. But in SPWM, the pulse width is a sinusoidal function of the angular position of the pulse in a cycle as shown in figure (3.5). In this Sinusoidal PWM technique, the sinusoidal AC voltage reference V_{ref} is compared with the high-frequency triangular carrier wave V_c in real time to determine switching states for each pole in the inverter. The intersection of V_c & V_{ref} waves determines the switching instants and commutation of the modulated pulse. The carrier and reference waves are mixed in a comparator as in figure 3.5(a).

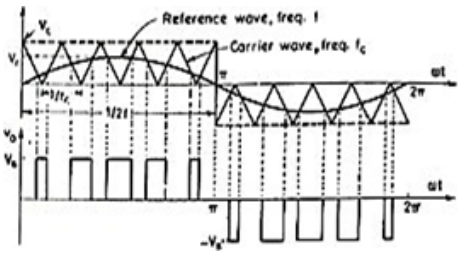

Fig. 3.5(a)

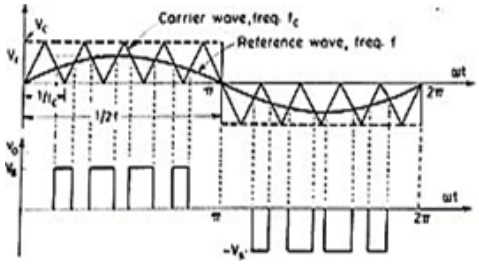

Fig. 3.5(b)

When sinusoidal wave has magnitude higher than the triangular wave, the comparator output is high, otherwise it is low. The comparator output is processed in a trigger pulse generator in such a manner that the output voltage wave of the inverter has a pulse width in agreement with the comparator output pulse width. When triangular carrier wave has its peak coincident with zero of the reference sinusoidal, there are $N = \frac{f_c}{2f}$ pulses per half cycle. Figure 3.5(a), has five pulses. In case Zero of the triangular wave coincides with zero of the reference sinusoidal, there are (N-1) pulses per cycle; figure 3.5(b) has $\left(\frac{f_c}{2f} - 1\right)$, i,e. four, pulses per half cycle.

The ratio of V_r/V_c is called the *modulation index* (MI) and it controls the harmonic content of the output voltage waveform. The magnitude of fundamental component of output voltage is proportional to MI, but MI can never be more than unity. Thus the output voltage is controlled by varying MI.

Harmonic analysis of the output modulated voltage waveform reveals that SPWM has the following important features:

1. For $MI < 1$, largest harmonic amplitude in the output voltage are associated with harmonics of order $f_c/f \pm 1$ or $2N \pm 1$, where N is the number of pulses per half cycle. Thus, by increasing the number of pulses per half cycle, the order of dominant harmonic frequency can be raised, which can then be filtered out easily. In figure 3.5(a), N=5, therefore harmonics of order 9 and 11 become significant in the output voltage. It may be noted that the highest order of significant harmonic of a modulated voltage wave is centered around the carrier frequency f_c.

   It is observed form above that as N is increased, the order of significant harmonic increases and the filtering requirements are accordingly minimized. But higher value of N entails higher switching frequency of thyristors. This amounts to more switching losses and therefore an impaired inverter efficiency. Thus a compromise between the filtering

requirements and inverter efficiency should be made.

2. For MI greater than one, lower order harmonics appear, since for $MI > 1$, pulse width is no longer a sinusoidal function of the angular position of the pulse.

3.5.1 PWM Dispositions

There are different categories of sinusoidal pulse width Modulation technique such as Phase disposition (PD), Phase opposite disposition (POD), Alternative phase opposite disposition (APOD) and phase shifted disposition. The difference between POD and PD techniques is that carriers above zero are 180^o phase shifted with those below the zero. The alternative phase opposite disposition is quite different from the two above in which the carriers are alternately phase shifted. According to this system, different multi-carrier modulation techniques are used and the performances are analyzed to obtain the fruitful results.

1. Phase Disposition (PD-PWM): In Phase Disposition concept, all the carrier signals are in same phase.

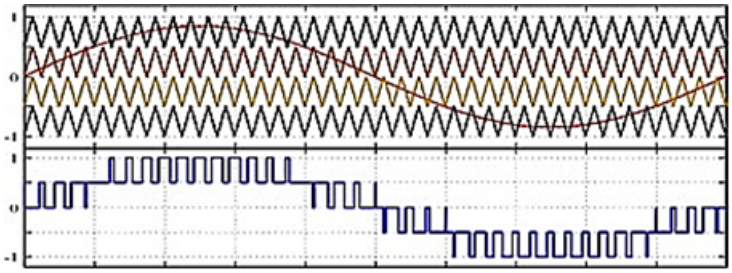

Figure 3.6: Triangular carrier waveform for PD-PWM

2. Phase Opposition Disposition (POD-PWM): In Phase Opposition Disposition all the carrier signals above the zero are out of phase with those below the zero by 180^o.

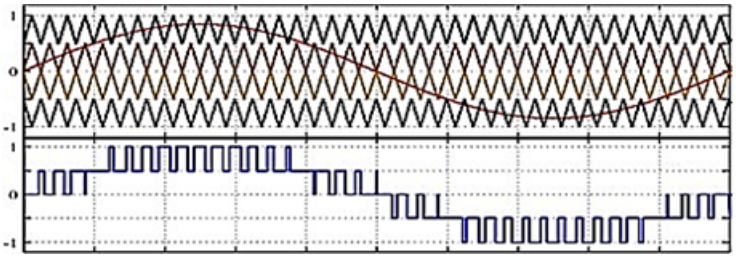

Figure 3.7: Triangular carrier waveform for POD-PWM

3. Alternative Phase Opposition Disposition (APOD-PWM): In Alternate Phase Opposition Disposition all the adjacent carrier signals are out of phase by 180^o.

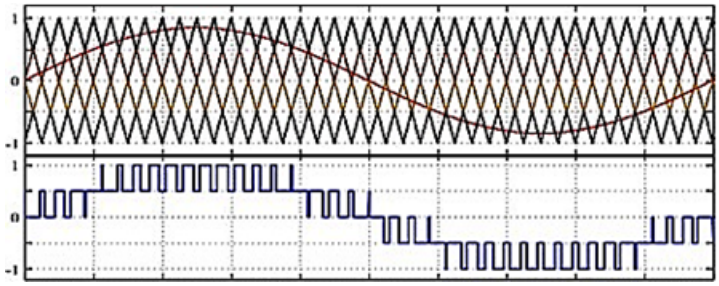

Figure 3.8: Triangular carrier waveform for APOD-PWM

Many researcher proved that, Phase disposition (PD) PWM is the most used method because it gives the lowest harmonic distortion compared to the other techniques and hence the PD is adopted in the present work.

3.6 Reduced Switches Multilevel Inverter

The proposed topology has a set series connected smaller multilevel inverter blocks shown below. Switch S_1 and should be conducting S_2 at different instances in order to prevent any short-circuit across the voltage source, that is when switch S_1 (S_2 off) is turned ON and the output will be equal to V_{dc} and when switch S_2 is turned on (S_1 off) output voltage will be zero.

The proposed topology as a set of series connected smaller multi-level inverter blocks as shown in figure (3.9).

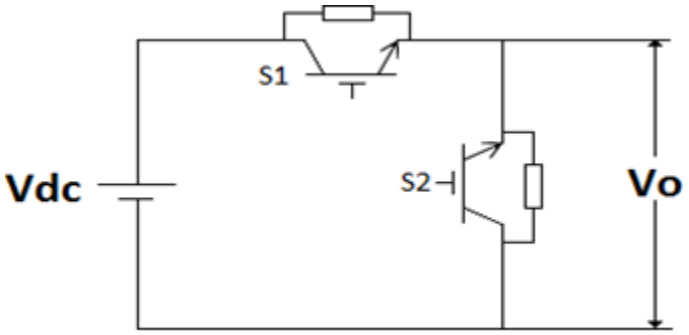

Figure 3.9: Basic multi-level inverter block

A series connected set of basic multilevel inverter blocks will achieve a stepped waveform.

Each of the power DC sources used is equal to V_{dc}; hence the circuit can also be described as a symmetrical multilevel inverter. Hence more power sources, more steps in the waveform. A more sinusoidal wave inverter will power devices and loads with more accuracy, leading to less power losses, consequently less heat generation. In this paper a 7-level inverter will be simulated in MATLAB/Simulink.

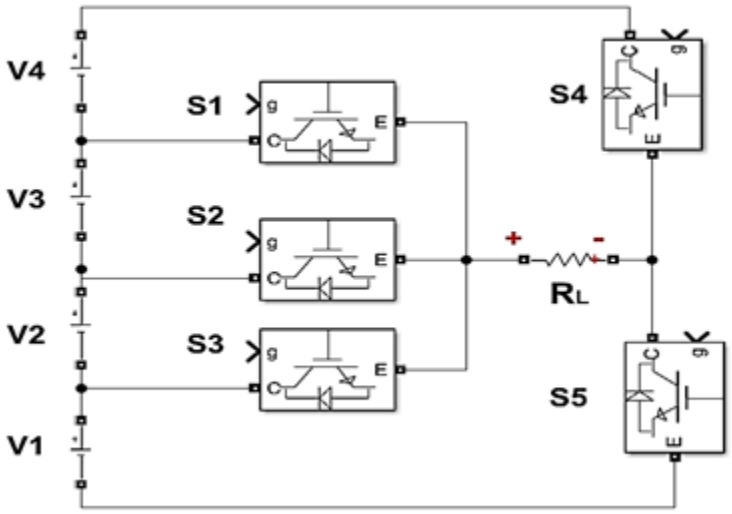

Figure 3.10: 7-level proposed topology.

Each smaller multilevel unit will produce a voltage of V_{dc}, therefore the V_o (overall maximum output voltage) will be equal to $3V_{dc}$. To create both positive and negative voltage levels an H-bridge is added to the circuit. Three levels will appear in the positive half, three levels in the negative half, and including the zero level, a total of 7 levels can be generated. In figure (10), the total switch count is 5 for a seven level inverter, whereas for a conventional cascaded multilevel inverter it would be 12. With seven switches being omitted in this topology, the gate driver circuit count also drops down by three, reducing the complexity of the overall circuit.

In the H-bridge, switches in the same leg should not conduct simultaneously, appropriate gate pulses should be given in order prevent short circuit condition. The primary objective of this paper is to minimize the number power semiconductor devices of the conventional cascaded multilevel inverter. Each switch requires its own gate driver circuit. One can observe that with this suggested topology the number of switches utilized is less than the conventional cascaded multilevel inverter. It reduces the installation area, gate drivers needed, and consequently the cost of the whole setup.

Chapter 4

Design and Modelling of multilevel inveters

4.1 Introduction

Multilevel converters (or inverters) have been used for dc-to-ac power conversion in high power applications such as utility and large motor drive applications. Multilevel inverters provide more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. There are three major multilevel topologies: cascaded, diode-clamped, and capacitor-clamped.

For the number of levels (M) or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. However, for M>3 and applications involved in active power transfer, such as motor drives, these multilevel converters all require either isolated dc power sources or a complicated voltage balancing circuit and control to support and maintain each voltage level. In this aspect, the three existing multilevel converters are neither operable nor complete for real (active) power conversion because they all depend on outside circuits for voltage balancing. The purpose of this paper is to increase the voltage level to achieve sinusoidal waveform & compare different voltage level by increasing the level through simulation.

The multilevel inverters perform power conversion in multi-level voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability Considering these advantages multilevel inverters have been gaining considerable popularity in recent years. Comparing with two level inverter system having the same power, multilevel inverters has the advantages that the lower harmonic components on the output voltages, Electro Magnetic Interference (EMI) problem could be decreased much as given in Table (3.1). Due to these merits, many studies about multilevel inverters have been performed at simulation level.

4.2 Generation of single pulse modulation

Let us consider carrier signal as Saw tooth and reference signal as DC voltage as in figure (4.1a). These are compared and the pulse waveform is obtained. Figure (4.1b) shows how single pulse modulated (SM) output is generated, this modulation gives quasi-square wave output of single pulse of output voltage during each half cycle. The ratio of Saw tooth signal amplitude (A_c) and DC signal amplitude (A_r) is called Modulation.

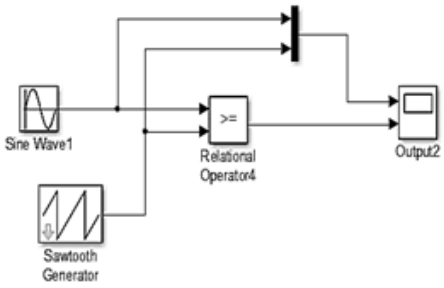

Fig.(4.1a): Circuit of Pulse generation

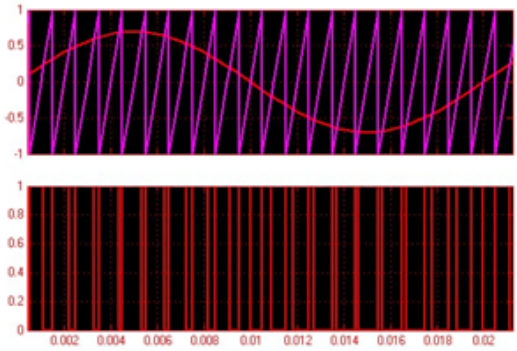

Fig.(4.1b): Generation of triggering pulse output

4.3 Single-phase, Three-level, Cascaded H-bridge multilevel inverter

A full-bridge voltage source-inverter can be considered as shown in figure (4.2) with representing load by only resistance. The circuit is operated by switching S_1, S_2, S_3, and S_4. The switches S_1&S_2, and S_3&S_4 are switched On and Off at a calculated duty cycle. When S_1 & S_2 are connected, the input voltage V_s appears across the load. If S_3 & S_4 are connected the voltage across the load is $-V_s$.

The operation of single-phase cascaded H-bridge inverter with resistive load is explained as follows: Let 'm' is the level of output voltage, 'α' is the switching angle of switches (Power semiconductor devices) and 'n' is the number of full bridges required to obtain the required output levels of an inverter, then

$$\text{The number of bridges required, } \quad n = \frac{(m-1)}{2} \tag{4.1}$$

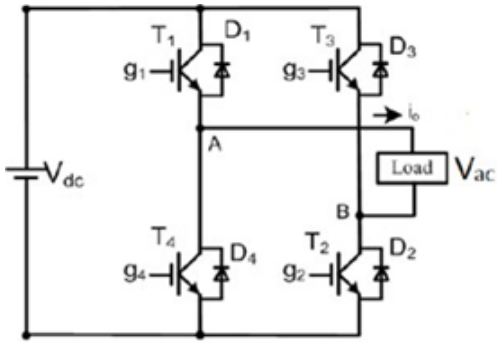

Figure 4.2: Circuit diagram of 3 level H-bridge inverter

The switching angle of switches are

$$\alpha = i * \frac{180^o}{m} \tag{4.2}$$

where 'i' an integer, i,e. i=1, 2, 3, 4, ... (m-1)/2.

Hence, for m=3, we get number of bridge required as 1 with four semiconductor devices as switches arranged in H-bridge form.

Table 4.1 can be considered the operation table for a single-phase, 3 level, H-bridge Inverter.

Table 4.1: Switching States for 3 level

Sl	S_1	S_2	S_3	S_4	V_{out}
1	Off	Off	Off	Off	0
2	On	On	Off	Off	V_s
3	Off	Off	Off	Off	0
4	Off	Off	On	On	$-V_s$
3	Off	Off	Off	Off	0

The figure (4.3) shows the pulse generation to the switches S_1, S_2, S_3 and S_4, by comparing the carrier signal (Triangular waveform) and the reference signal (Sinusoidal waveform). The pulse to be generated by comparing the two triangular wave with positive half cycle of the sinusoidal waveform and the remaining two triangular wave with negative half cycle of the sinusoidal waveform. Thus, Quasi square output voltage waveform is generated.

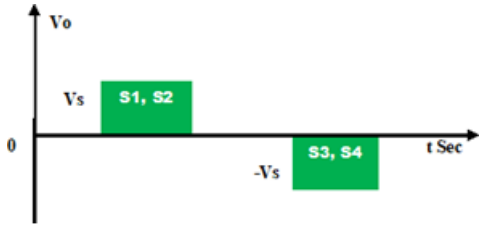

Figure 4.3: Pulse generated using carrier signal and reference signal

4.3.1 Modeling of Three-level inverter

Figure (4.4) shows Matlab/Simulink model of pulse generation required to turn On and turn Off the semiconductor devices. The carrier, modulating and command signals using SPWM method are produced in the sub-system.

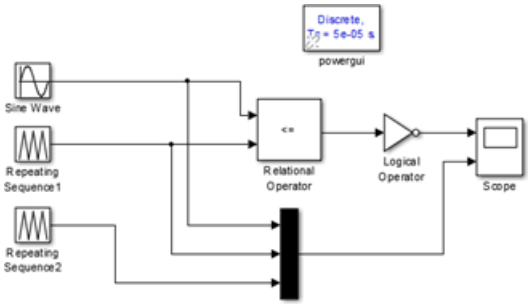

Figure 4.4: Simulink model for Pulse generation

Three level H-bridge inverter is modeled with the help of MATLAB/SIMULINK by SPWM technique. Simulink model for 3 level inverter is as shown in figure (4.5).

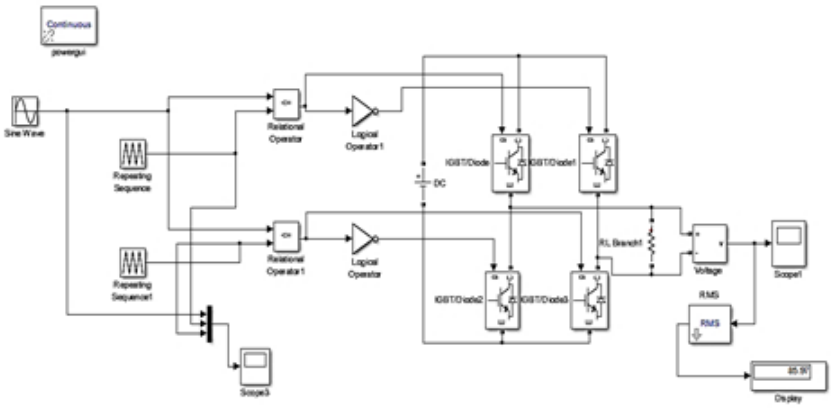

Figure 4.5: Simulink model of single-phase, Three-level, H-bridge inverter

4.4 Single-phase, Five-level, Cascaded H-bridge multilevel inverter

A full-bridge voltage source-inverter can be considered as shown in figure (4.6) with representing load by only resistance. The circuit is operated by two H-bridge cascaded across load with an input source of equal value V_s. The switches S_1, S_2,..... S_8 are switched On and Off at a calculated duty cycle.

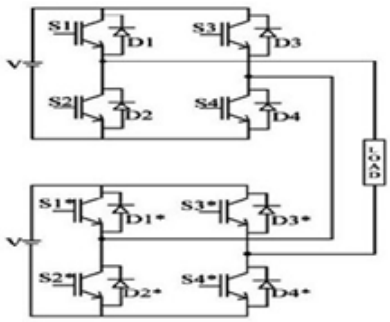

Figure 4.6: Circuit diagram of 5 level H-bridge inverter

The operation of single-phase, 5 level, cascaded H-bridge inverter with resistive load is explained as follows: Let 'm' is the level of output voltage, 'α' is the switching angle of switches (Power semiconductor devices) and 'n' is the number of full bridges required to obtain the required output levels of an inverter, then

$$\text{The number of bridges required, } n = \frac{(m-1)}{2} \tag{4.3}$$

The switching angle of switches are

$$\alpha = i * \frac{180^o}{m} \tag{4.4}$$

where 'i' an integer, i,e. i=1, 2, 3, 4, ... (m-1)/2.

Hence, for m=5, we get number of bridge required as 2 with eight semiconductor devices as switches arranged in H-bridge cascaded form.

The figure (4.7) shows the pulse generation to the switches S_1, S_2,..... S_8, by comparing the carrier signal (Triangular waveform) and the reference signal (Sinusoidal waveform). The

pulse to be generated by comparing the two triangular wave with positive half cycle of the sinusoidal waveform and the remaining two triangular wave with negative half cycle of the sinusoidal waveform. Thus, five level output voltage waveform is generated.

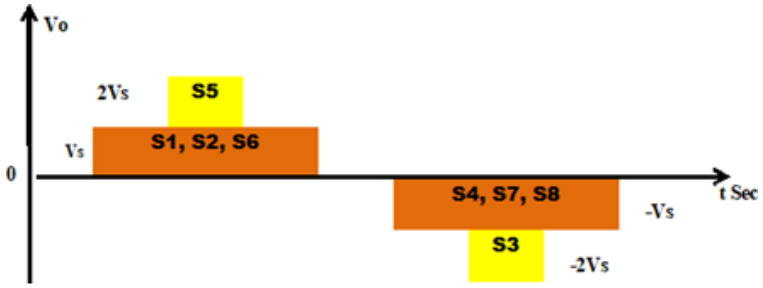

Figure 4.7: Pulse generated using carrier signal and reference signal

Table 4.2 can be considered the operation table for a single-phase, 5 level, cascaded H-bridge Inverter.

Table 4.2: Switching States for 5 level

Sl	Bridge 1 (On)	Bridge 2 (On)	V_{out} (volts)
1	- - - - - -	- - - - - -	0V
2	S_1, S_2	S_6	V_s
3	S_1, S_2	S_5, S_6	$2V_s$
4	S_1, S_2	S_6	V_s
5	- - - - - -	- - - - - -	0V
6	S_4	S_7, S_8	$-V_s$
7	S_3, S_4	S_7, S_8	$-2V_s$
8	S_4	S_7, S_8	$-V_s$

4.4.1 Modeling of Five-level inverter

Figure (4.8) shows Matlab/Simulink model of pulse generation required to turn On and turn Off the semiconductor devices. The carrier, modulating and command signals using SPWM method are produced in the sub-system.

Five level H-bridge inverter is modeled with the help of MATLAB/SIMULINK by SPWM technique. Simulink model for 5 level inverter is as shown in figure (4.9).

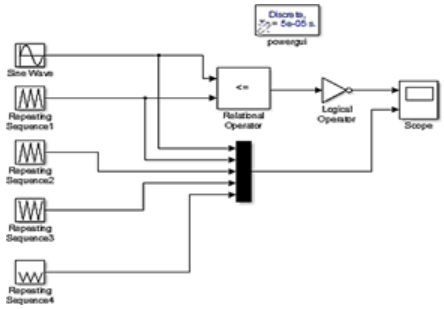

Figure 4.8: Simulink model for Pulse generation

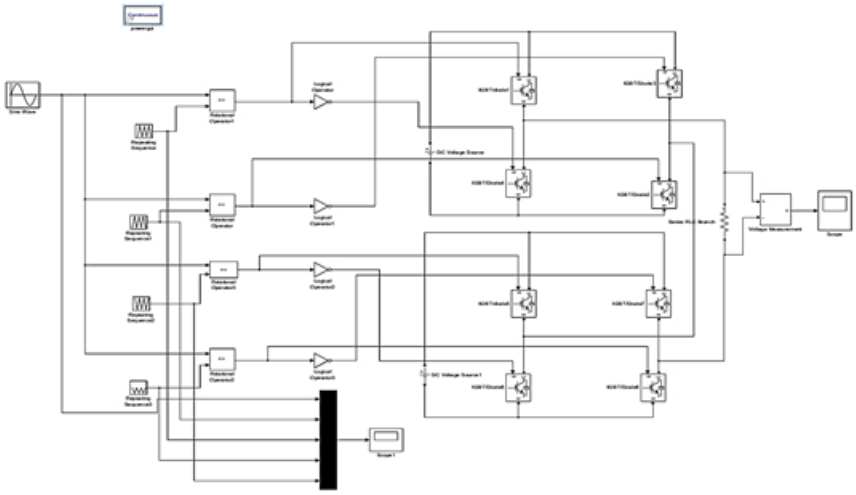

Figure 4.9: Simulink model of single-phase, Five-level, H-bridge inverter

4.5 Single-phase, Seven-level, Cascaded H-bridge multilevel inverter

A full-bridge voltage source-inverter can be considered as shown in figure (4.10) with representing load by only resistance. The circuit is operated by three H-bridge cascaded across load with an input source of equal value V_s. The switches S_1, S_2, S_3,..... S_{12} are switched On and Off at a calculated duty cycle.

The operation of single-phase, 7 level, cascaded H-bridge inverter with resistive load is explained as follows: Let 'm' is the level of output voltage, 'α' is the switching angle of switches (Power semiconductor devices) and 'n' is the number of full bridges required to obtain the required output levels of an inverter, then

$$\text{The number of bridges required, } n = \frac{(m-1)}{2} \tag{4.5}$$

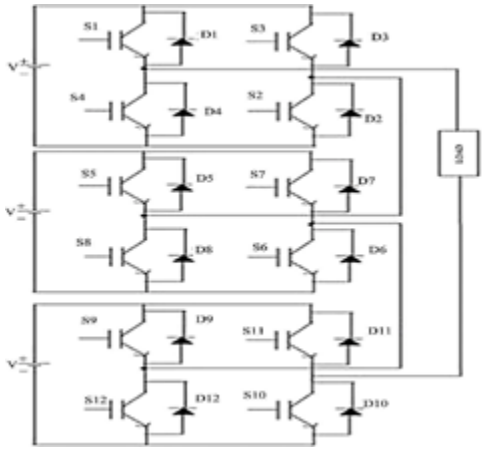

Figure 4.10: Circuit diagram of 7 level H-bridge inverter

The switching angle of switches are

$$\alpha = i * \frac{180^o}{m} \tag{4.6}$$

where 'i' an integer, i,e. i=1, 2, 3, 4, ... (m-1)/2.

Hence, for m=7, we get number of bridge required as 3 with twelve semiconductor devices as switches arranged in H-bridge cascaded form.

The figure (4.11) shows the pulse generation to the switches S_1, S_2, S_3,.....,S_{11}, S_{12}, by comparing the carrier signal (Triangular waveform) and the reference signal (Sinusoidal waveform). The pulse to be generated by comparing the two triangular wave with positive half cycle of the sinusoidal waveform and the remaining two triangular wave with negative half cycle of the sinusoidal waveform. Thus, seven level output voltage waveform is generated.

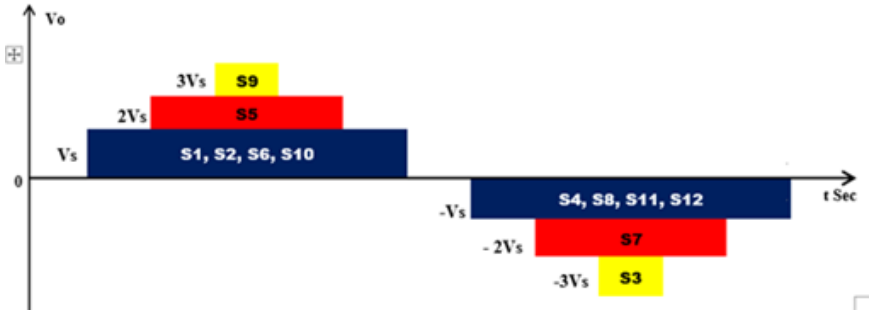

Figure 4.11: Pulse generated using carrier signal and reference signal

Table 4.3 can be considered the operation table for a single-phase, 7 level, cascaded H-bridge Inverter. The switches of the respective H-bridges are made On and Off.

Table 4.3: Switching States for 7 level

Sl	Bridge 1 (On)	Bridge 2 (On)	Bridge 3 (On)	V_{out} (volts)
1	- - - - - -	- - - - - -	- - - - - -	0V
2	S_1, S_2	S_6	S_{10}	V_s
3	S_1, S_2	S_5, S_6	S_{10}	$2V_s$
4	S_1, S_2	S_5, S_6	S_9, S_{10}	$3V_s$
5	S_1, S_2	S_5, S_6	S_{10}	$2V_s$
6	S_1, S_2	S_6	S_{10}	V_s
7	- - - - - -	- - - - - -	- - - - - -	0V
8	S_4	S_8	S_{11}, S_{12}	$-V_s$
9	S_4	S_7, S_8	S_{11}, S_{12}	$-2V_s$
10	S_3, S_4	S_7, S_8	S_{11}, S_{12}	$-3V_s$
11	S_4	S_7, S_8	S_{11}, S_{12}	$-2V_s$
12	S_4	S_8	S_{11}, S_{12}	$-V_s$

4.5.1 Modeling of Seven-level inverter

Figure (4.12) shows Matlab/Simulink model of pulse generation required to turn On and turn Off the semiconductor devices. The carrier, modulating and command signals using SPWM method are produced in the sub-system.

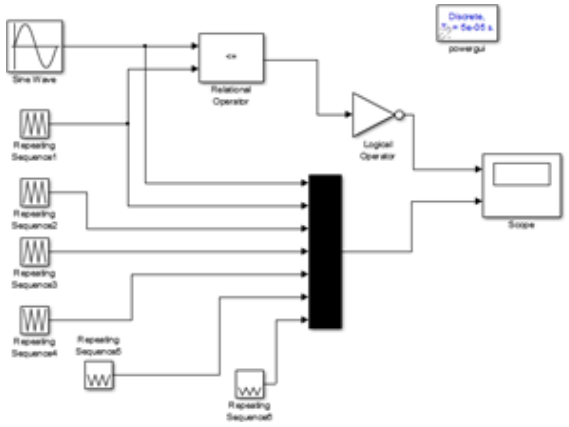

Figure 4.12: Simulink model for Pulse generation

Seven level H-bridge inverter is modeled with the help of MATLAB/SIMULINK by SPWM technique. Simulink model for 7 level inverter is as shown in figure (4.13).

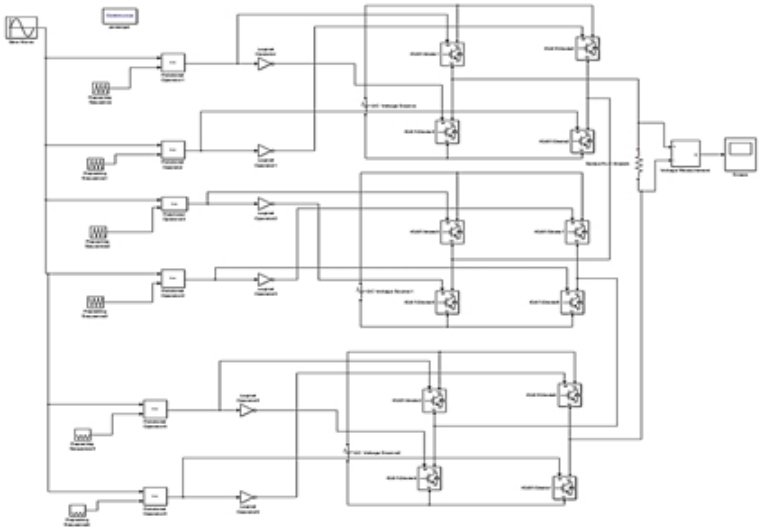

Figure 4.13: Simulink model of single-phase, seven-level, H-bridge inverter

4.6 Single-phase, Seven-level, Reduced Switches inverter

Each smaller multilevel unit will produce a voltage of V_{dc}, therefore the V_o (overall maximum output voltage) will be equal to $3V_{dc}$. To create both positive and negative voltage levels an H-bridge is added to the circuit. Three levels will appear in the positive half, three levels in the negative half, and including the zero level, a total of 7 levels can be generated. In figure (4.14), the total switch count is 5 for a seven level inverter, whereas for a conventional cascaded multilevel inverter it would be 12. With seven switches being omitted in this topology, the gate driver circuit count also drops down by three, reducing the complexity of the overall circuit.

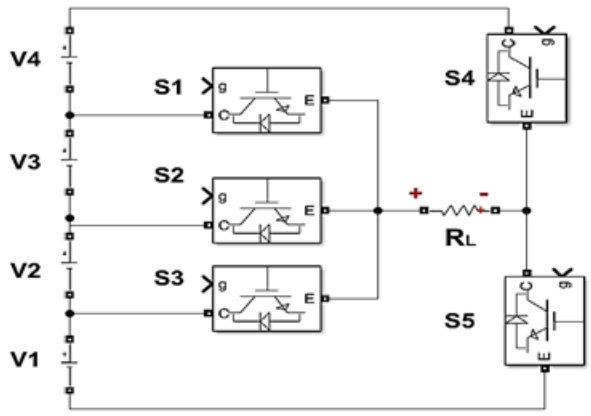

Figure 4.14: Circuit diagram of 7-level inverter with reduced switches

The figure (4.15) shows the pulse generation to the switches S_1, S_2, S_3, S_4, and S_5, by comparing the carrier signal (Triangular waveform) and the reference signal (Sinusoidal waveform). The pulse to be generated by comparing the two triangular wave with positive half cycle of the sinusoidal waveform and the remaining two triangular wave with negative half cycle of the sinusoidal waveform. Thus, seven level output voltage waveform is generated.

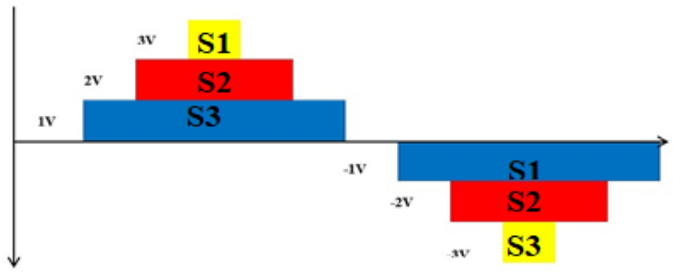

Figure 4.15: Pulse generated using carrier signal and reference signal

Table 4.4 can be considered the operation table for a single-phase, 7-level, reduced switches Inverter. The switches of the respective modes are made On and Off to achieve level of output voltages.

Table 4.4: Switching States for 7-level, reduced switches

Sl	S_1	S_2	S_3	S_4	S_5	V_{out} (volts)
1	- - -	- -	ON	- -	ON	V_1
2	- - -	ON	- - -	- -	ON	V_1+V_2
3	ON	- -	- - -	- -	ON	$V_1+V_2+V_3$
4	ON	- -	- - -	ON	- - -	$-V_4$
5	- - -	ON	- - -	ON	- - -	$-(V_3+V_4)$
6	- - -	- -	ON	ON	- - -	$-(V_2+V_3+V_4)$

4.6.1 Modeling of Seven-level, Reduced Switches inverter

Figure (4.16) shows Matlab/Simulink model of pulse generation required to turn On and turn Off the semiconductor devices. The carrier, modulating and command signals using SPWM method are produced in the sub-system.

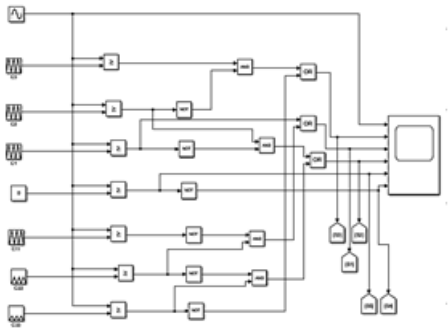

Figure 4.16: Simulink model for Pulse generation

Seven level, reduced switches inverter is modeled with the help of MATLAB/SIMULINK by SPWM technique. Simulink model for 7-level inverter is as shown in figure (4.17).

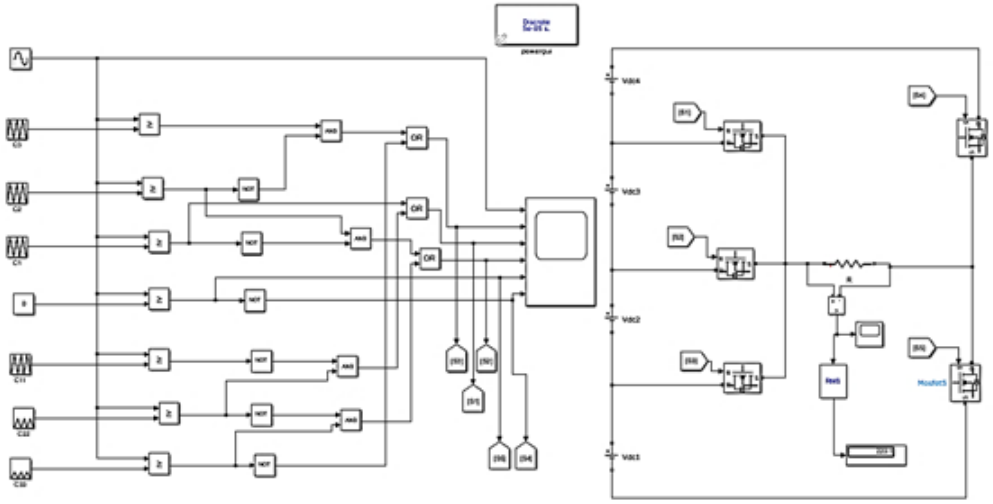

Figure 4.17: Simulink model of single-phase, 7-level, reduced switches inverter

4.7 Solar fed Seven-level, Reduced Switches inverter

To achieve solar fed 7-level, reduced switches inverter of figure (4.14) is to replace the DC sources(batteries) by designed solar array at the input of an inverter as shown in figure (4.18). Here the solar array is designed to produce approximately 100 V with maximum current of 7.35 Amp and maximum power output from solar array is around 853.18 watts.

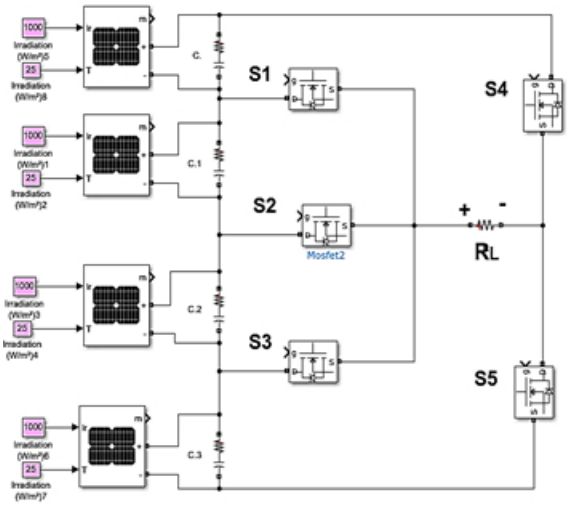

Figure 4.18: Circuit diagram of Solar fed 7-level, reduced switches inverter

Solar fed 7-level, reduced switches inverter is modeled with the help of MATLAB/SIMULINK by SPWM technique. Simulink model for the same is as shown in figure (4.19).

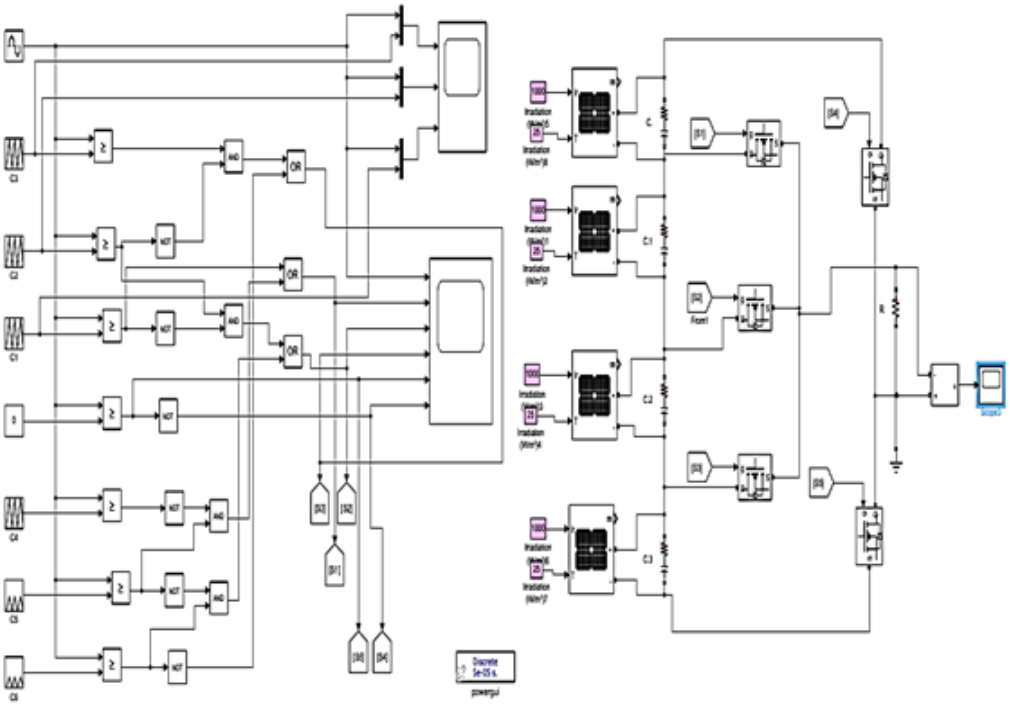

Figure 4.19: Simulink model of single-phase, Solar fed, 7-level, reduced switches inverter

Chapter 5

Simulation & Results

All researches work that has gone on inverter circuit configuration mainly in reducing the switches at higher voltage levels, by reducing switches/total harmonic distortion (THD) and increasing voltage levels to reduce filter cost and harmonic content. Here three, five and seven levels Cascaded H-bridge MLI are referred to simulate using MATLAB/Simulink and with these references the 7-level reduced switches inverter and Solar fed 7-level reduced switches inverter are analyzed.

As per the theory discussed in chapter 3 and chapter 4 simulations are carried out for different cascaded multilevel inverter to obtain SPWM pulses, output voltage(V_o) and FFT analysis is done in MATLAB/SIMULINK to obtain THD. The GUI plots are used for the Fast Fourier Transforms (FFT) analysis to determine the Total Harmonic content (THD).

THD Analysis: The analysis total harmonic distortion (THD), is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave. THD calculations can be obtained from the SIMULINK. The switching pattern used in this project for all of the multilevel inverters is Sinusoidal PWM technique. In this method the switching angles for switches should be calculated in such a way that the dominant harmonics are eliminated (minimized).

$$\%\ \text{THD} = \frac{\sqrt{V_1^2+V_2^2+V_3^2+V_4^2+V_5^2+V_6^2.....+V_n^2}}{V_1} * 100 \tag{5.1}$$

Where, V_1 is fundamental voltage magnitude, V_2 is magnitude of 2^{nd} harmonic, V_3 is magnitude of 3^{rd} harmonic,..... V_n is magnitude of n^{th} harmonic.

The formula above shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal. Higher the percentage, more distortion that is present on the mains signal.

5.1 Single-phase, three-level inverter

Three level cascaded H-bridge multilevel inverter modeling in MATLAB/SIMULINK was shown in figure (4.5) which has a bridge, produces three level voltage. The following parameters are used: V_s = 100V, f_c = 5 kHz,f_m = 50 Hz and load resistance of 10Ω. Here, the Phase disposition PWM carriers are generated as shown in figure (5.1).

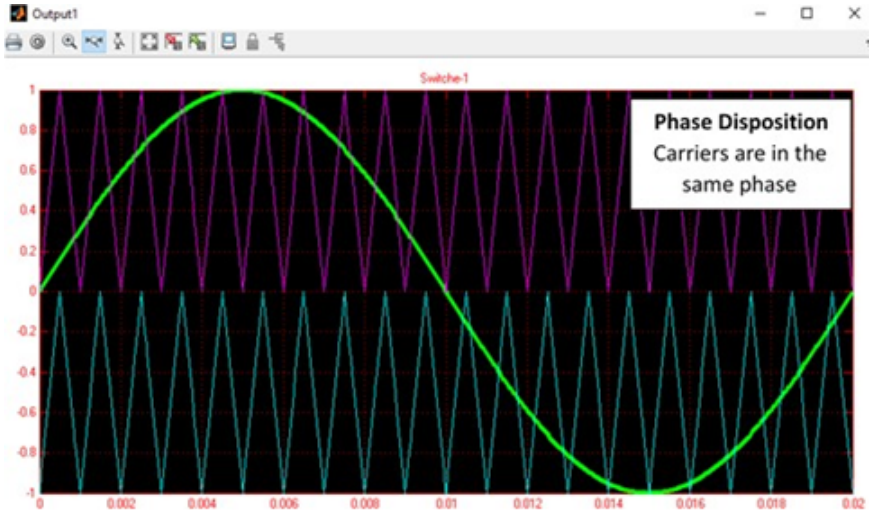

Figure 5.1: Carrier arrangements for SPWM

Simulated control techniques, output Voltage and FFT waveform analysis for the 3 level CHB-MLI are presented in figures (5.2 to 5.4).

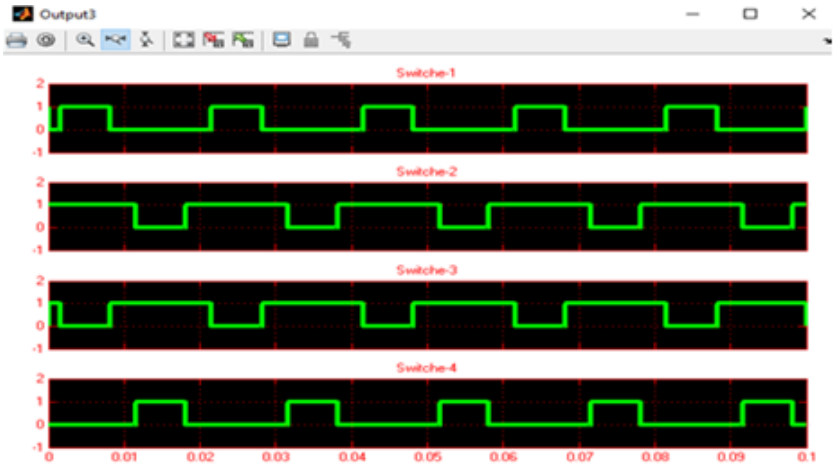

Figure 5.2: Switching pulses for 3-level inverter

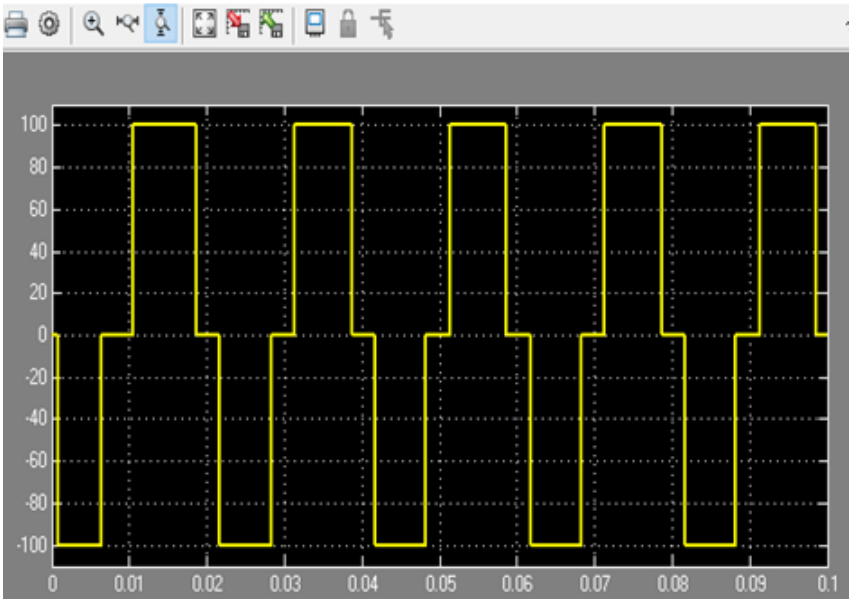

Figure 5.3: Output voltage of 3-level inverter

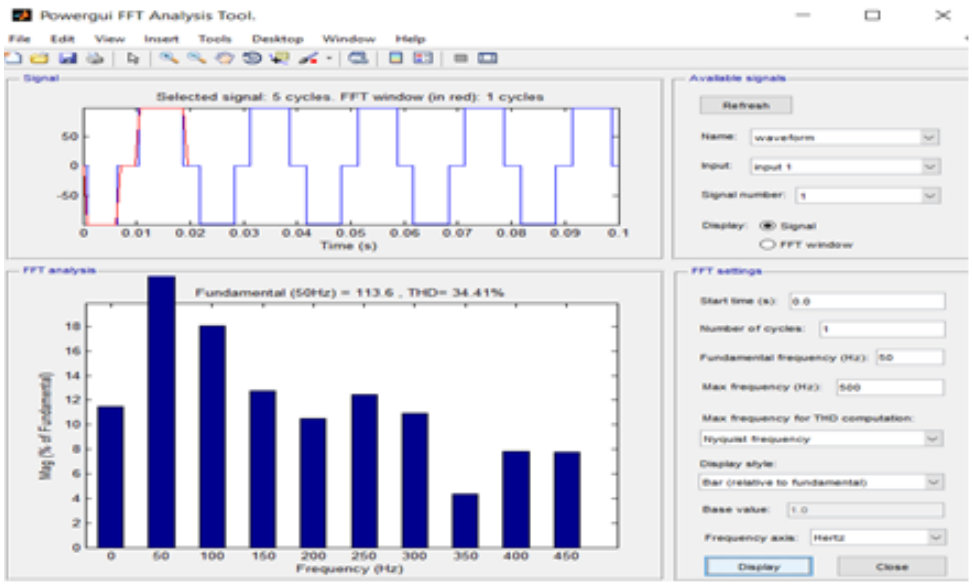

Figure 5.4: % THD of 3-level inverter

The output voltage of three level inverter is generated in Matlab/Simulink software is demonstrated in figure (4.4). Figure (5.3) shows the graph plotted between output voltage V_o & time and the r.m.s value of the output voltage obtained is 85.97 V. The output is stepped and consists of three levels. From the Fast Fourier Transform (FFT) analysis of three level inverter, it is obeserved that the total harmonic distortion (THD) is 34.41% as in figure (5.4).

5.2 Single-phase, five-level inverter

Five level cascaded H-bridge multilevel inverter modeling in MATLAB/SIMULINK is shown in figure (4.9) which has two bridges, produces five level voltage. The following parameters are used: V_s = 100V, f_c = 5 kHz,f_m = 50 Hz and load resistance of 10Ω. Here, the Phase disposition PWM carriers are generated as shown in figure (5.5).

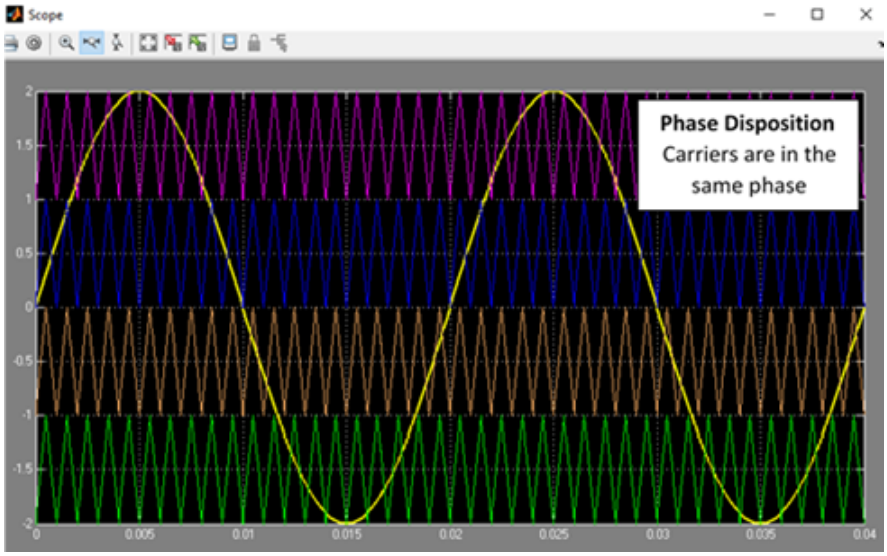

Figure 5.5: Carrier arrangements for SPWM

The Simulated control techniques, output Voltage and FFT waveform analysis for the 5 level CHB-MLI are presented in figures (5.6 to 5.8).

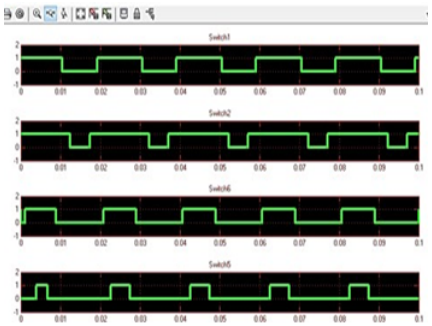

Fig. 5.6: Switching pulses for 5-level inverter (a)

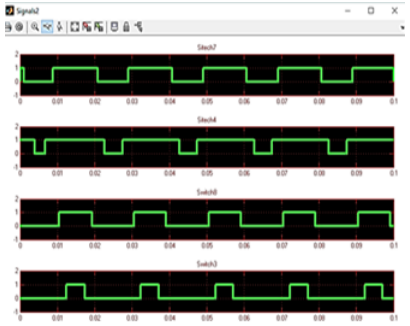

Fig. 5.6: Switching pulses for 5-level inverter (b)

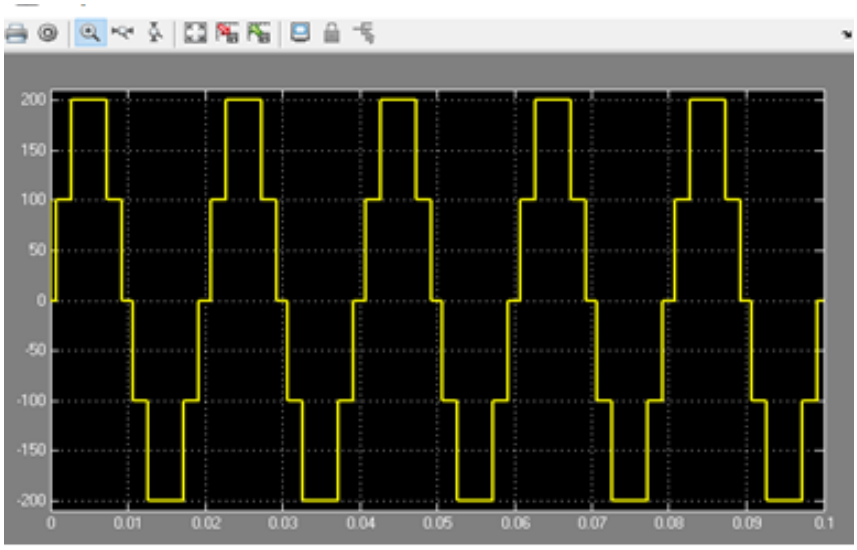

Figure 5.7: Output voltage of 5-level inverter

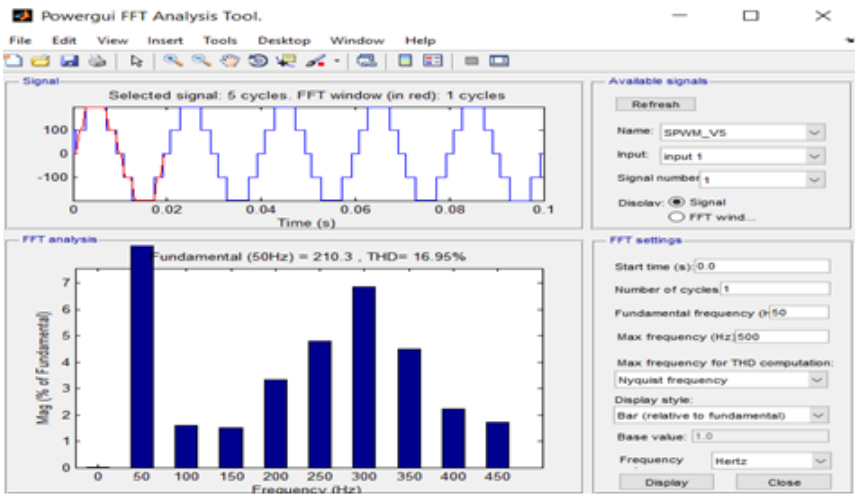

Figure 5.8: % THD of 5-level inverter

The output voltage of five level inverter is generated in MATLAB/Simulink software is demonstrated in figure (4.9). Figure (5.7) shows the graph plotted between output voltage V_o & time and the r.m.s value of the output voltage obtained is 154.3V. The output is stepped and consists of five levels. From the Fast Fourier Transform (FFT) analysis of five level inverter, it is observed that the total harmonic distortion (THD) is 16.95% as in figure (5.8).

5.3 Single-phase, Seven-level inverter

Seven level cascaded H-bridge multilevel inverter modeling in MATLAB/SIMULINK was shown in figure (4.13) which has three bridges, produces seven level voltage. The follow-

ing parameters are used: V_s = 100V, f_c = 5 kHz,f_m = 50 Hz and load resistance of 10Ω. Here, the Phase disposition PWM carriers are generated as shown in figure (5.9).

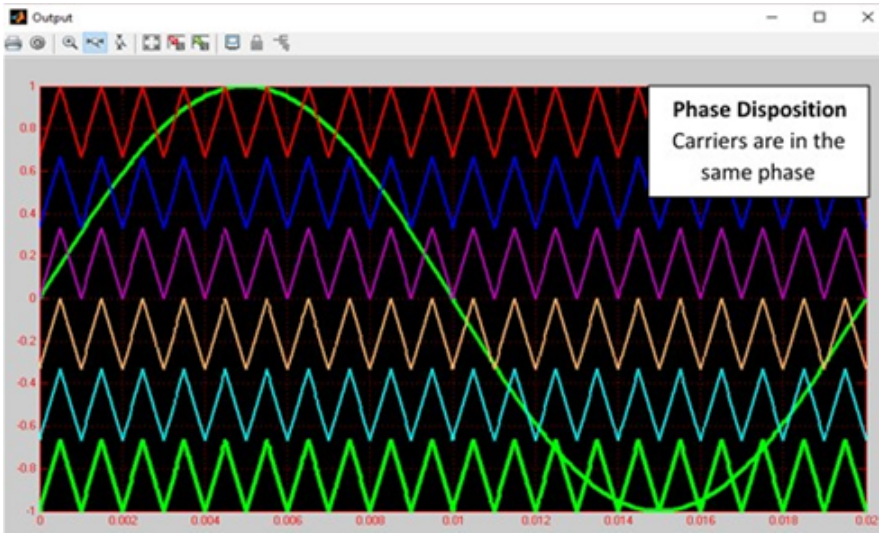

Figure 5.9: Carrier arrangements for SPWM

Simulated control techniques switching the devices for the 7-level, MLI are presented in figures (5.10 to 5.12).

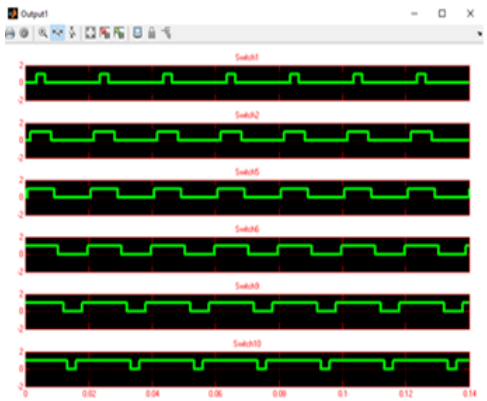

Fig. 5.10: Switching pulses for 7-level inverter (a)

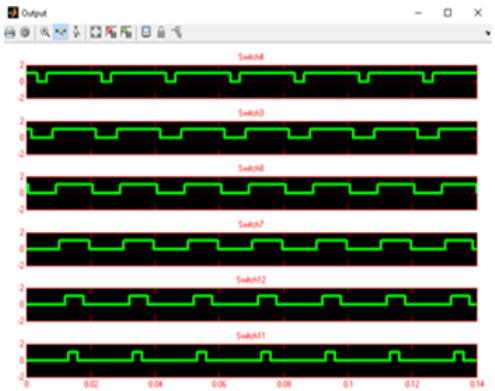

Fig. 5.10: Switching pulses for 7-level inverter (b)

The output voltage of seven level inverter is generated in Matlab/Simulink software is demonstrated in figure (4.13). Figure (5.11) shows the graph plotted between output voltage V_o & time and the r.m.s value of the output voltage obtained is 232.2V. The output is stepped and consists of seven levels. From the Fast Fourier Transform (FFT) analysis of seven level inverter, it is observed that the total harmonic distortion (THD) is 14.21% as in figure (5.12).

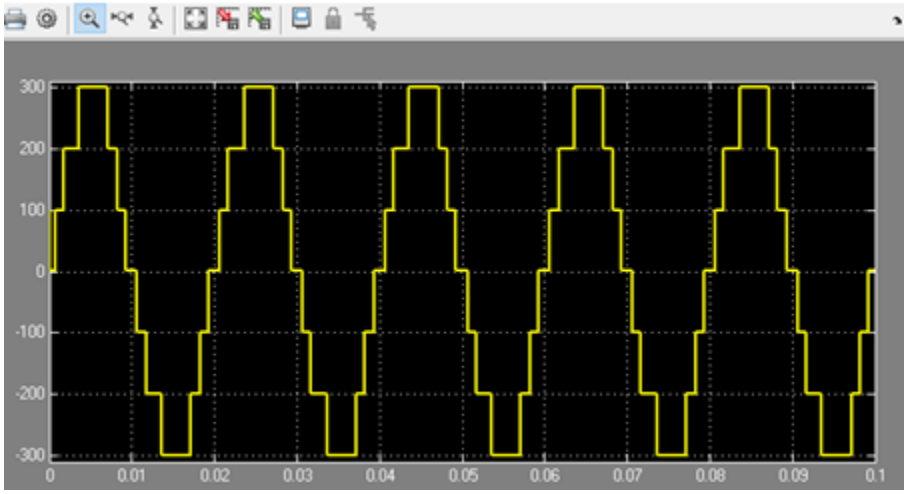

Figure 5.11: Output voltage of 7-level inverter

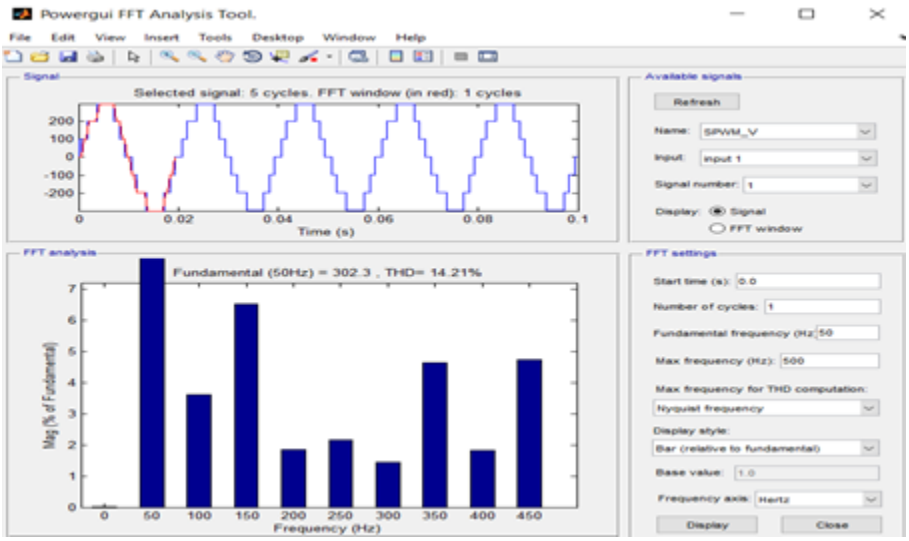

Figure 5.12: % THD of 7-level inverter

5.4 Single phase, Seven-level, Reduced Switches inverter

Seven level, reduced switches multilevel inverter modeling in MATLAB/SIMULINK is shown in figure (4.17) which has five switches to produces seven level output voltage. The following parameters are used: V_s = 100V, f_c = 5 kHz,f_m = 50 Hz and load resistance of 10Ω. Here, the Phase disposition PWM carriers are generated as shown in figure (5.13).

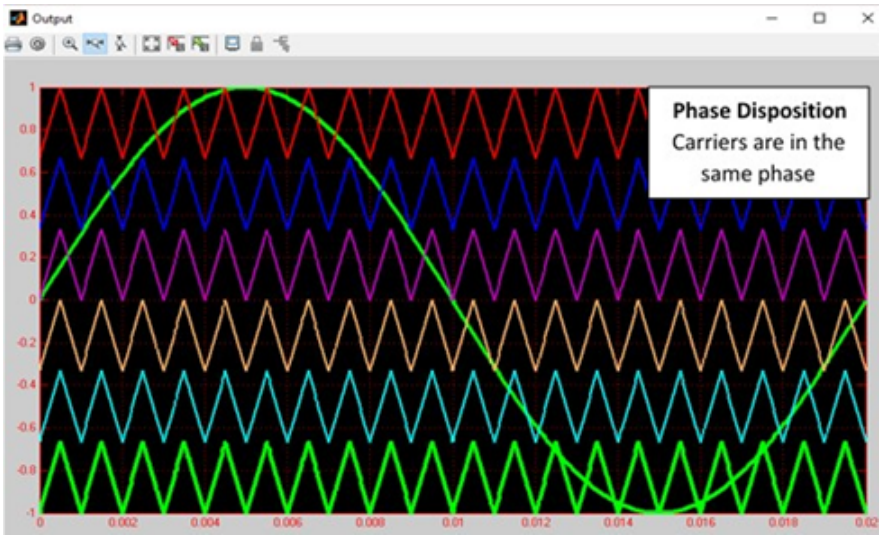

Figure 5.13: Carrier arrangements for SPWM

Simulated control techniques switching the devices for the 7-level, reduced switches are presented in figure (5.14).

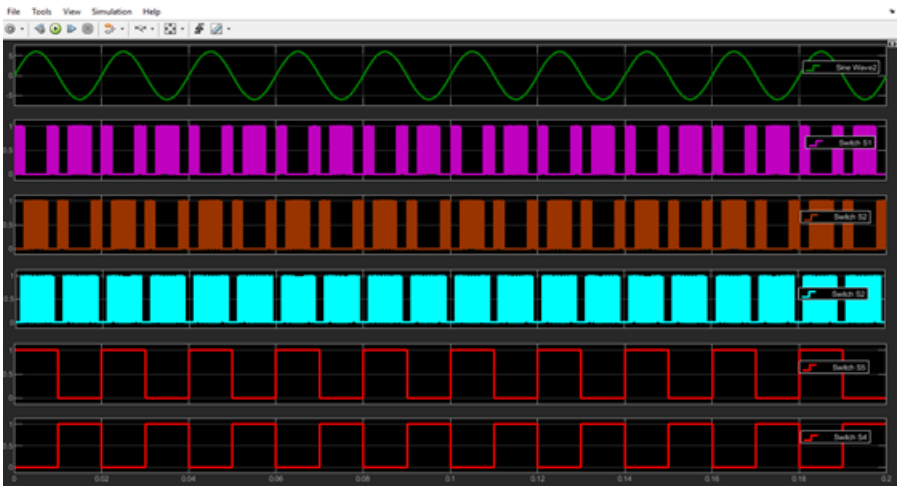

Figure 5.14: Switching pulses for 7-level, reduced switch inverter

The output voltage of seven level,reduced switch inverter is generated in Matlab/Simulink software is demonstrated in figure (4.17). Figure (5.15) and figure (5.16) shows the graph plotted between output voltage V_o & time and the Fast Fourier Transform (FFT) analysis for total harmonic distortion.

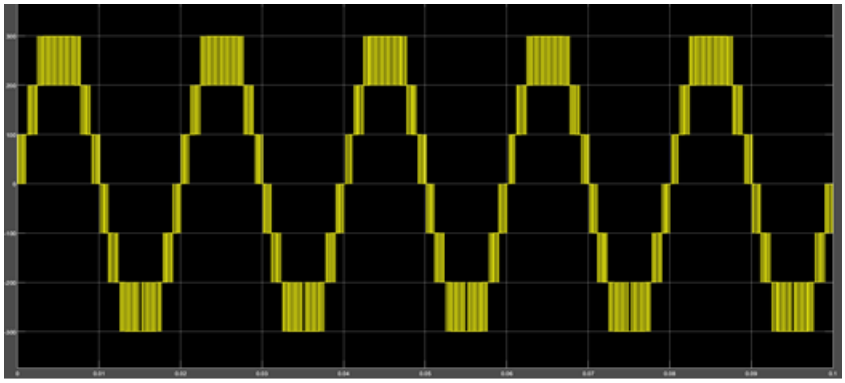

Figure 5.15: Output voltage of 7-level,reduced switch inverter

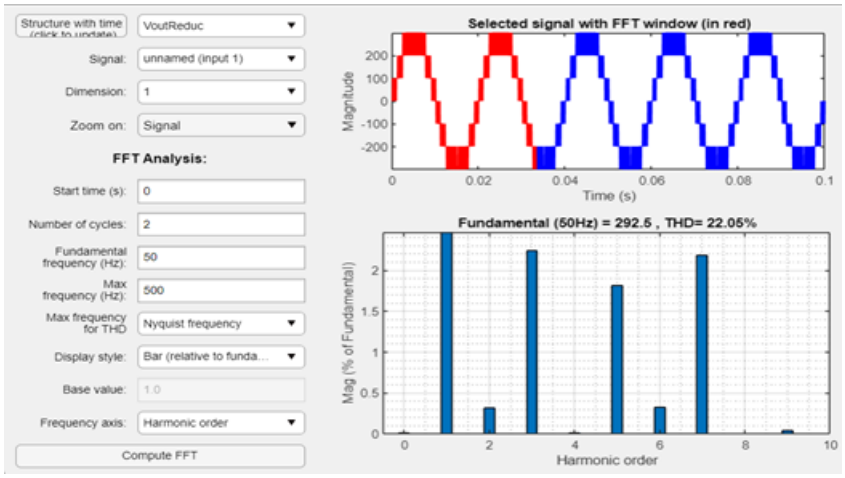

Figure 5.16: % THD of 7-level, reduced switch inverter

5.5 Solar fed,single phase, Seven-level, Reduced Switches inverter

Solar fed, Seven level, reduced switches multilevel inverter modeling in MATLAB/SIMULINK is shown in figure (4.18) which has five switches to produces seven level output voltage. The following parameters are used: The input to an inverter from solar pv array is approximately of voltage V_s = 100V, and f_c = 5 kHz,f_m = 50 Hz & load resistance of 10Ω.

The output voltage of solar fed, seven level, reduced switch inverter is generated in Matlab/Simulink software is demonstrated in figure (4.19). Figure (5.17) and figure (5.18) shows the graph plotted between output voltage V_o & time and the Fast Fourier Transform (FFT) analysis for total harmonic distortion.

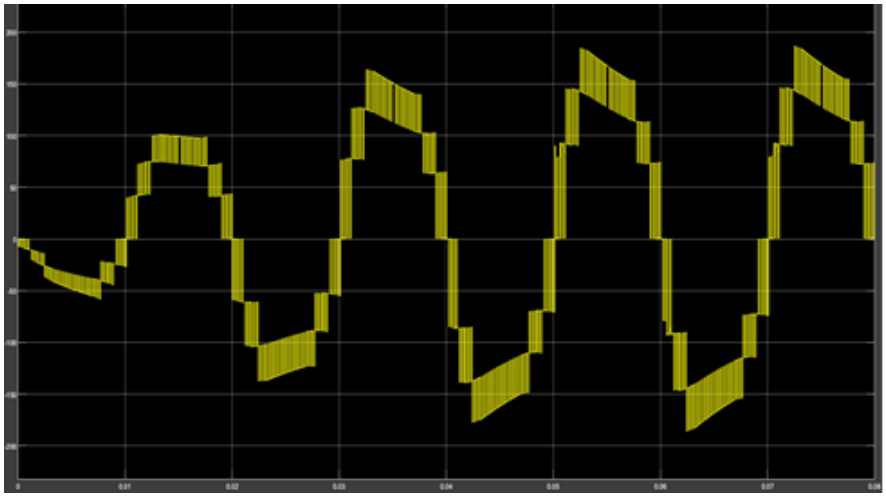

Figure 5.17: Output voltage of 7-level inverter

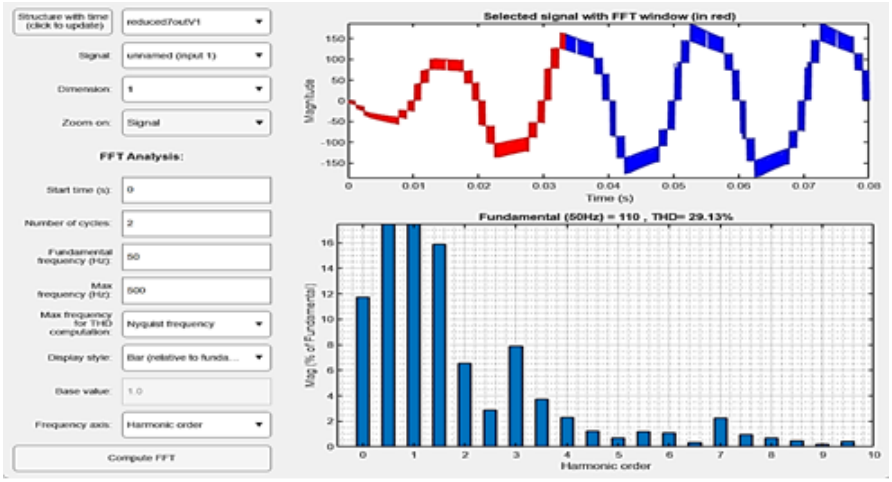

Figure 5.18: % THD of 7-level inverter

Chapter 6

Conclusion & Enhancement

6.1 Conclusion

Photovoltaic based applications are increasing day by day. Since most of the electrical application are in AC, so some efficient Power Electronics DC to AC converters are required for converting photovoltaic DC output to AC. The electrical converter is therefore very interesting for renewable energy conversion systems, because it increases the efficiency, while maintaining stable dynamics under the effect of a non-linear or unbalanced load.

A new 7-level inverter has been designed with a reduced number of components for solar PV applications was proposed in this work. The proposed inverter produces higher output voltage levels with a lesser number of circuit components. The proposed inverter has 5 switches triggered by using Sinusoidal-Pulse-Width Modulation technique. Four DC voltage source was provided with reduced losses, high efficiency. A single phase Photovoltaic Array fed MLI with Reduced number of Semiconductor Switches is simulated in MATLAB / SIMULINK environment.

6.2 Future Enhancement

In practice, the basic single-phase, full bridge inverter produces output voltage of square wave form (called 'two level') with highest % THD of 40.48 %. The present developed cascaded H-bridge multilevel inverters are satisfactory in reduction of THD, but still higher than the IEEE standard % THD $\leq$ 5 %. So in order to bring down this % THD to IEEE standard for the improvement of power quality at output of an inverter which is closet to AC sinusoidal wave form, the reduced switch multilevel inverters are required to adopt:-

1. Increase in output voltage levels.
2. Advanced modulation techniques like
   (a) Trapezoidal modulation.
   (b) Harmonic injected modulation.

(c) Delta modulation.

(d) Staircase modulation.

3. Total harmonic distortion can be further reduced by using filter circuit. This circuit also reduces the number of switches and sources, but increases the cost and size of an inverter.

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Chapter 7

Reference