Computer Aided Digital System Design
(99-00-1)
Dr. Hajar Falahati

Homework 3: Behavioral Modeling **Deadline:** 1399/10/2 23:59			
Problem	**Definition**	**Credit**	**Your Mark**
P1	**Cary Look Ahead**	**30**	
P2	**Protein Detection**	**45**	
P3	**Elevator**	**20**	
P4	**Timing**	**40**	
Total		**140**	

Required File:
Upload a zip file titled as "CAD-HW3- *Student numberi- …- Student numberj"*.

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1- Cary Look Ahead [30 points]

Design a 4-bit adder which follows the carry look ahead mechanism.

i. Implement the adder in Verilog (behavioral level). [10 points]
ii. Implement the adder logic using the combinational gates. [10 points]
iii. Implement the adder in Verilog (gate level). [10 points]

2- Protein Detection (LDLD, MST) [45 points]

BLAST, Basic Local Alignment Search Tool, is a heuristic-based sequencing technique which finds all similar sequences in a data base. BLAST is able to find the most similar DNA sequences or proteins for a given unknown sequence. Sequencing is widely used in detecting the new genome, organism, virus, and is
an important step in finding the medicine.

i. Is BLAST a software or a hardware approach? Support your answer. [10 points]
ii. Introduce a new hardware-based approach for sequencing in at least one paragraph. [10 points]
iii. Draw a protein sequence detector FSM which detects both LDLD and MST proteins, i.e., amino acid sequences. You have to implement one FSM. [15 points]
iv. Implement the protein sequence detector FSM in Verilog (behavioral modeling). [10 points]

3- Elevator [20 points]

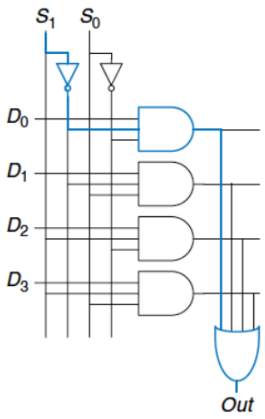
Consider the elevator in quiz 1 and implement the control unit which:

i. Turns on the elevator to go to the requested floor/s.
ii. Turn off the elevator.
iii. Monitors the temperature and manage the air conditioner to keep the temperature between 24-26℃.

4- Timing [40 points]

Consider the bellow circuit and timing characteristics. Suppose that each input comes from a pose-edge D-FF and the output goes to a pose-edge D-FF.

i. Calculate the delay of critical path.
ii. What is the maximum frequency of the circuit?
iii. Does this circuit satisfy the timing requirements? If no, fix the issue.
iv. Suppose the maximum clock period can be 300 ps, fix the circuit to satisfy the clock constraints.



Gate	T_{pd} (ps)	T_{cd} (ps)
NOT	30	20
2-input AND	40	30
3-input AND	50	40
4-input OR	60	50
Tristate (input to output)	35	25
Tristate (enable to output)	25	15
FF (clock to output)	40	20
T_{setup}	60	
T_{hold}	120	
T_{skew}	40	