p2.

Q1. Sequential → not all cases of conditions are covered (no else statement), always statement is set ~~or~~ not on all inputs and right hand side signals.

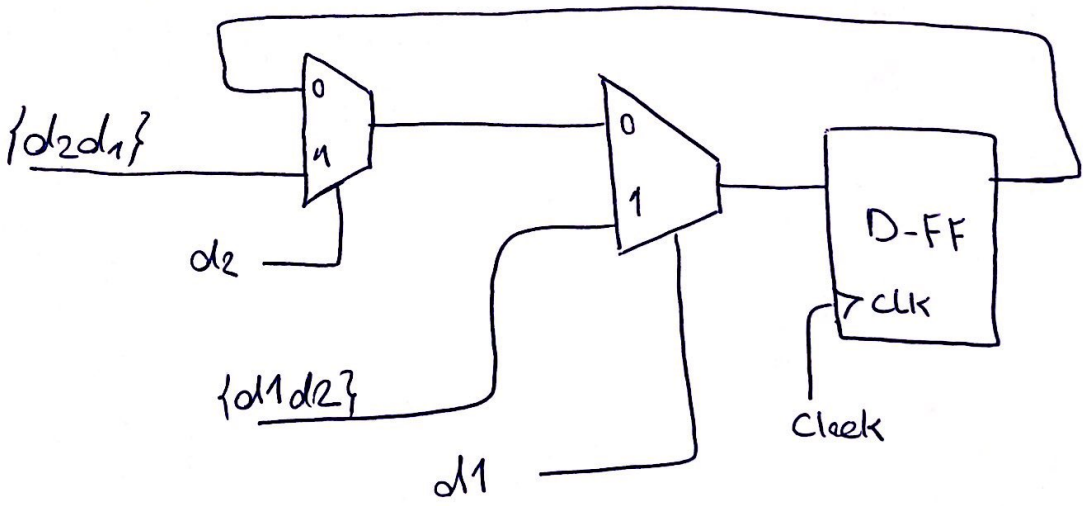
→ if data_in1 and data_in2 both be zeros, data0 is not changed ~~data~~ → so we need memory → sequential

↳ data_in2 not is sensivity list.

Q2. Concat in synthesis → just some changes in the wires, sythesizable.

d1	d2	d0
0	0	Same as befor
0	1	d2d1
1	x	d1d2

expansion by d1; → for mux



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P2.

Q3.

① $a = (E3)_{16} = (1110\_0011)_2$

$b = (1)_{10} = (0001)_2$ &b = And bitwise b = 0

$c = (3)_8 = (0011)_2$ |C = or bitwise C = 1

$a \Leftarrow \{1110\_0011, 0, 1\} = 1110\ 001101$

$a = 1000\ 1101$ ⇐ first 8 bits are ← 10 bit ← taken and assigned to a

② $a[0] \Leftarrow \wedge a[7:6] \Rightarrow a[0] = \wedge\{11\} = 0$

$a[7:6] \leftarrow$ non-blocking ←

↳ from the last $a = 1110\ 0011$

So ①② => after one clk cycle : $a = \{1000\ 1100\}$ ✓

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