Computer-Aided Design

99-00-1

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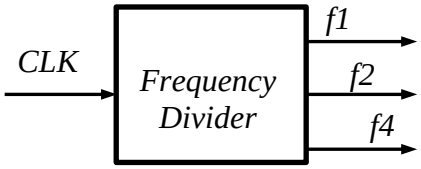
Final 1399/11/04 150 minutes

Problem	Definition	Credit	Your Mark
P1	**Verilog Coding & Synthesis**	**50**	
P2	**Code Analysis**	**25**	
P3	**SPLD**	**15**	
P4	**Modular Coding**	**20**	
Total		**110**	

1. **The exam time is 150 minutes.**
2. **Check the exam problems and ask your questions during the first 5 minutes.**
3. **Do not ask any question after 5 minutes!**
4. **The exam is open book!**
5. **Write the final answer clearly.**
6. **Write all your work. It helps you to get some portions of credits.**
7. **Good Luck**

P1. Verilog Coding and Synthesis [50 points]

Consider a sequential frequency divider which generates three signals with different frequencies. The frequencies of *f1*, *f2*, and *f3* are 1, ½, and ¼ of *CLK* frequency, respectively.



Q1. [20 points] Write a behavior-level Verilog. Your implementation instances two modules:

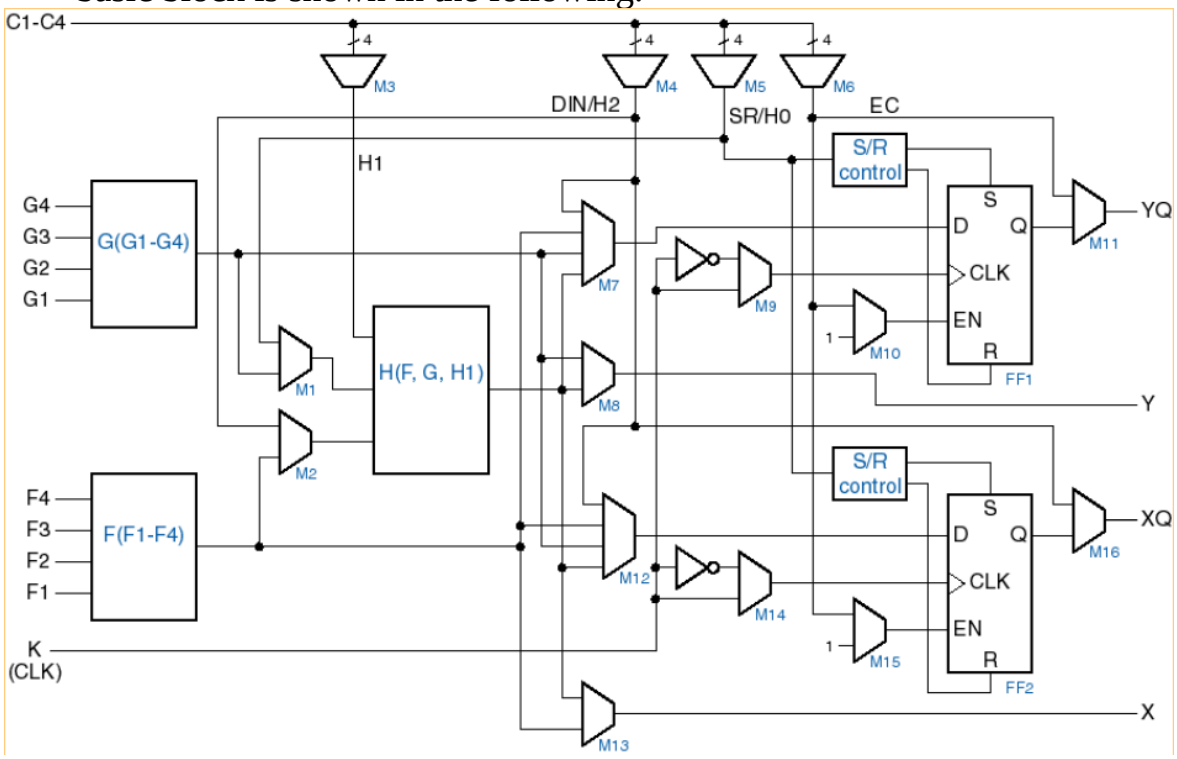
a. "calculate-next-state": a gate-level module to calculate the next state.

b. "calculate-output": a dataflow-level module to calculate the outputs *f1*, *f2*, and *f3*.

Q2. [10 points] Write a test module and check the validity of your code.

Q3. [10 points] Synthesis the frequency divider module using the logic gates and FFs. Suppose you have any kinds of logic gates and J-K FFs.

Q4. [10 points] Synthesis the frequency divider module using the FPGA whose basic block is shown in the following.



P2. Code Analysis [25 Points]

Consider the following codes and answer the questions:

Q1. [5 points] Does the following code implement a combinational or sequential circuit? Support your response

```
Module sample1 (input clk, input dataIn1, input dataIn2, output reg [1:0] dataO);
    always @ (posedge clk, data_in1)
            if (data_in1)
         dataO = {dataIn1, dataIn2};
           else if (data_in2)
        dataO = {dataIn2, dataIn1};

 endmodule
```

Q2. [10 points] Suppose you have all the logical gates and FFs, synthesis the sample 1.

Q3. [10 points] What is the output of the following code after one CLK cycle and the initial value of a = 8'hE3, b = 4'd1, and c = 4'o 3

```
Module sample2 (input clk, input [3:0] b, input [3:0] c, output reg [7:0] a);
    always @ (negedge clk)
        begin
                a <= {a, &b, |c};
                a[0] <= ^a [7:6];
         end
 endmodule
```

P3. Simple Programmable Logic Device [15 points]

Q1. [5 points] Draw a PAL-based SPLD to implement 3-input functions (i.e, $f(x1, x2, x3)$). The PAL consists of two 2-input OR. The OR outputs and their complements are sent back to the PAL.

Q2. [10 points] Implement these two functions on the PAL with minimum number of resources.

$$f1(x1, x2, x3) = x1\,\overline{x2}\,\overline{x3} + \overline{x1}\,x2\,\overline{x3} + x1\,x2\,\overline{x3} + x3\,x1 + x3\,x2$$

$$f2(x1, x2, x3) = x1\,\overline{x3} + x2\,\overline{x3} + \overline{x1}\,\overline{x2}\,x3$$

P4. Modular Coding [20 points]

Complete the following module to calculate the Fibonacci number using function.

$$F(n) = F\,(n-1) + F(n-2) \qquad F(1) = 1\,,\;\; F\,(2) = 1$$

```
module Fibonacci (input [2:0] n, output [4:0] Fibo);




endmodule
```