Computer Aided Design
Assignment №4

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0 Team

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1 SPLD: Simple Programmable Logic Device

1.1 ROM

We use a 4 to 16 decoder to produce all minterms, then we check the minterms corresponding to numbers dividable by 3 and minterms corresponding to numbers not dividable by 3.

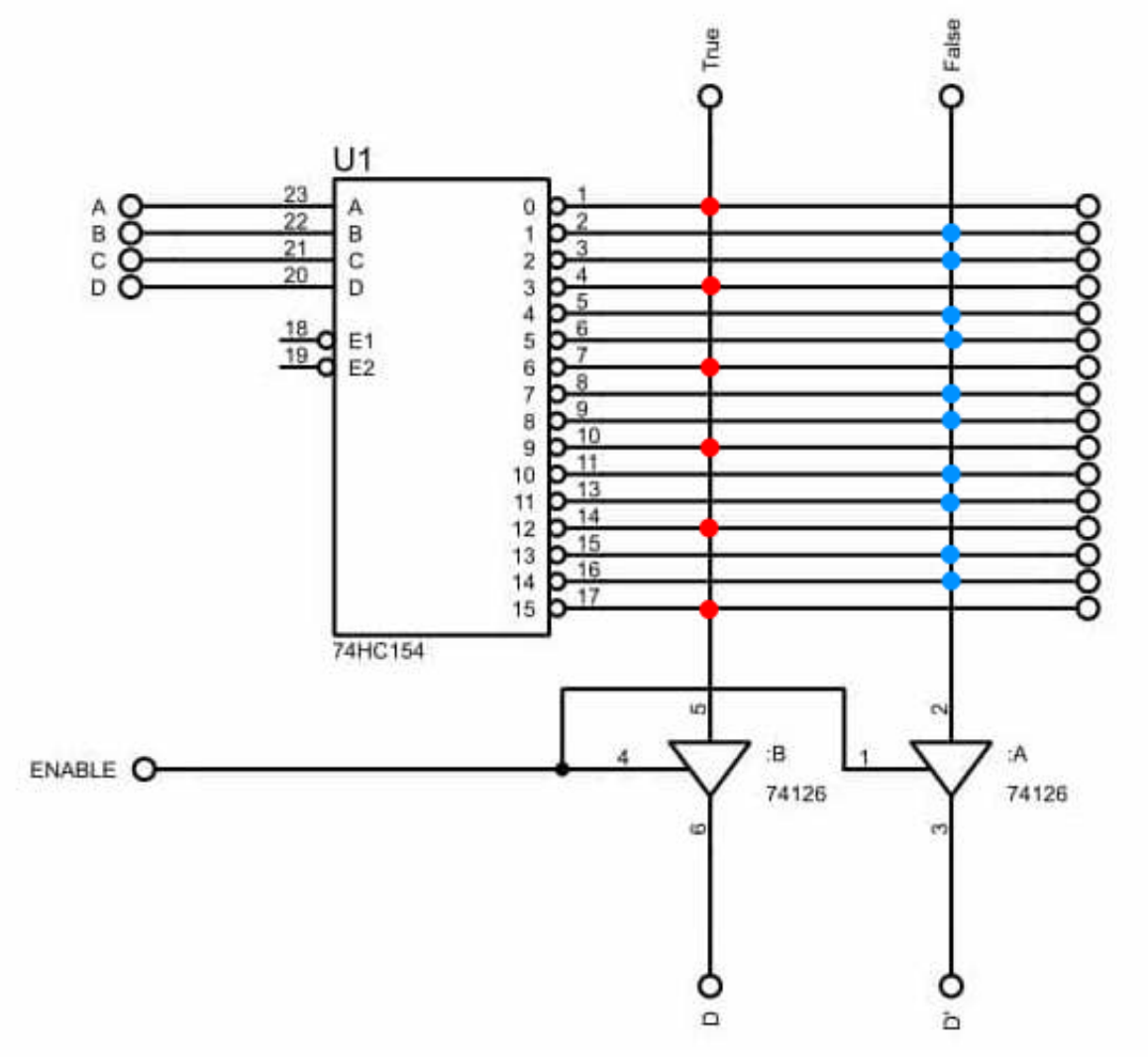

Figure 1: ROM

1.2 Programmable Logic Array: PLA

We use 6 AND gates to produce minterms and then use a single OR gate for the final result.

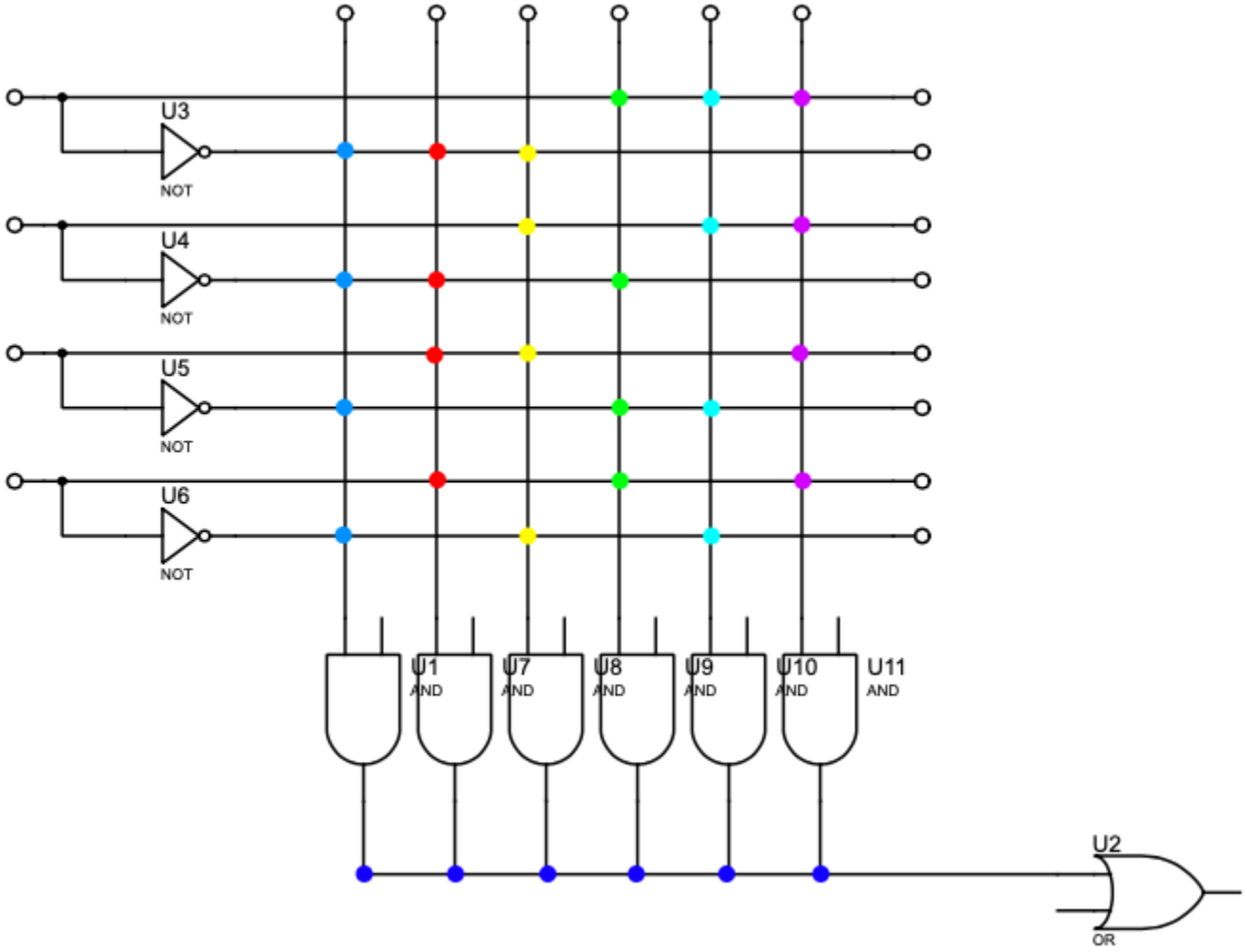

Figure 2: PLA

1.3 Programmable Array Logic: PAL

There are 4 OR gates, each calculating a result (F1 to F4) respectively.

Result of each OR gate is propagated back to the device, noted by F1 to F4, and their inverts are also calculated.

$$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + ABCD$$

$$\Rightarrow F = AB(CD + \bar{C}\bar{D}) + \bar{A}\bar{B}(CD + \bar{C}\bar{D}) + A\bar{B}\bar{C}D + \bar{A}BC\bar{D}$$

$$\Rightarrow F_1 = CD + \bar{C}\bar{D}$$

$$\Rightarrow F_2 = ABF_1 + \bar{A}\bar{B}F_1$$

$$\Rightarrow F_3 = A\bar{B}\bar{C}D + F_2$$

$$\Rightarrow F_4 = \bar{A}BC\bar{D} + F_3$$

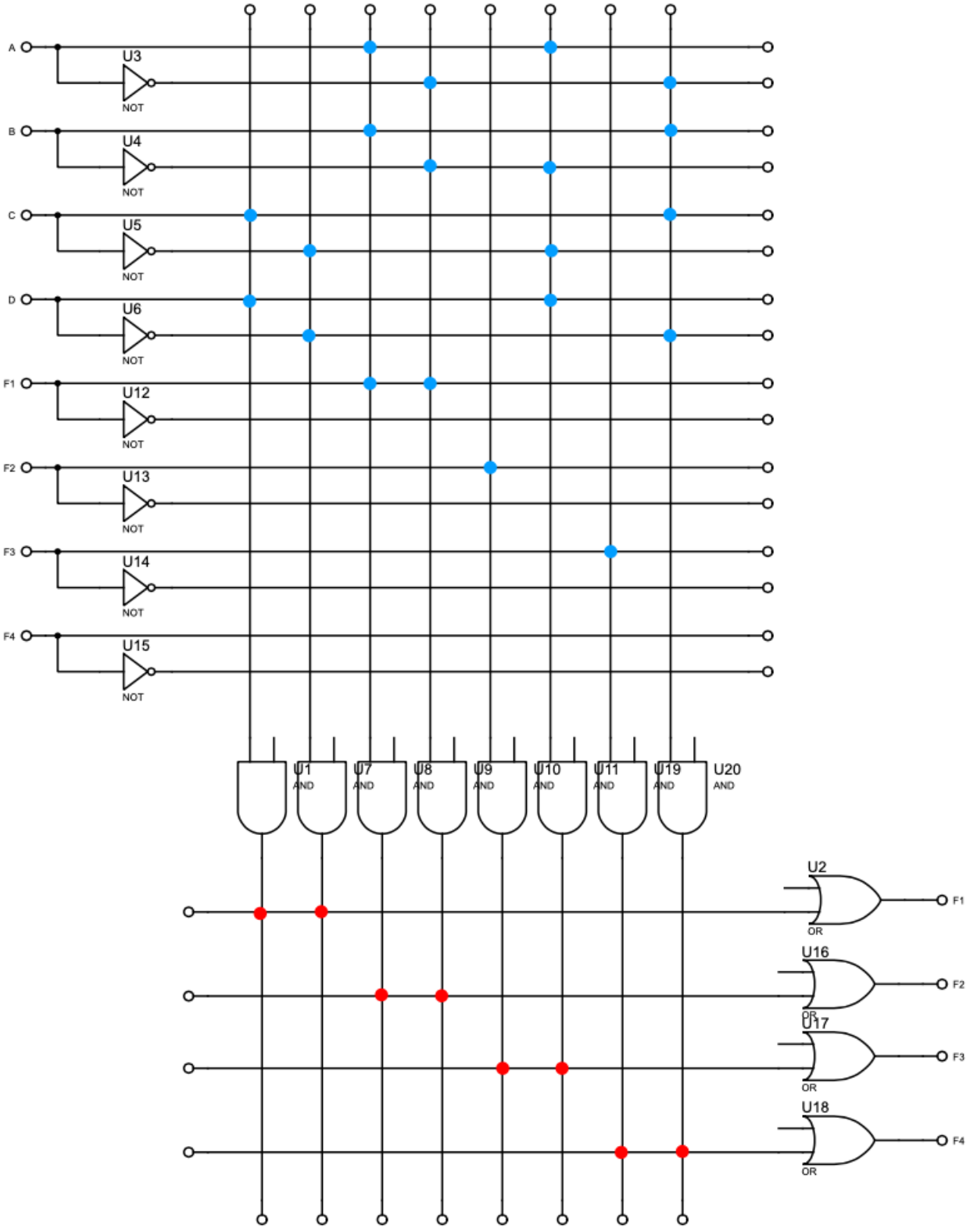
A
B
C
D
F1
F2
F3
F4
U3
U4
U5
U6
U12
U13
U14
U15
NOT
U1
U7
U8
U9
U10
U11
U19
U20
AND
U2
U16
U17
U18
OR
F1
F2
F3
F4

Figure 3: PAL

2 FPGA Synthesis

2.1

2.2 Implement the function on the following mux-based FPGA

$$f = B + (A + \bar{C}).(\bar{A} + \bar{B} + \bar{C})$$
$$f = B + A\bar{A} + A\bar{B} + A\bar{C} + \bar{A}\bar{C} + \bar{B}\bar{C} + \bar{C}\bar{C}$$
$$f = B + A\bar{B} + \bar{C}(A + \bar{A}) + \bar{B}\bar{C} + \bar{C}$$
$$f = B + A\bar{B} + \bar{C} + \bar{B}\bar{C}$$
$$f = B + A\bar{B} + \bar{C}(\bar{B} + 1)$$
$$f = B + A\bar{B} + \bar{C}$$

expand f wrt B:

$$f = B(1 + \bar{C}) + \bar{B}(A + \bar{C})$$
$$f = B + \bar{B}(A + \bar{C})$$
$$f1 = A + \bar{C}$$
$$f2 = 1$$

expand f1 wrt C:

$$f1 = C(A) + \bar{C}$$

Select lines and inputs:
S3 = B
SA = C
SB = 0
S0 = 0, S1 = B
A0 = 1, A1 = A
B0 = 1, B1 = 0

3 Synthesis Rules

3.1

`n` and `i` should be declared (e.g. `integer n = 4;`). There's an `end` missing. Using the first output (`M[i]`) as input to the next function can cause timing error. Also the code is not in a module and none of the variables have been declared (e.g. as I/O, reg, etc.).

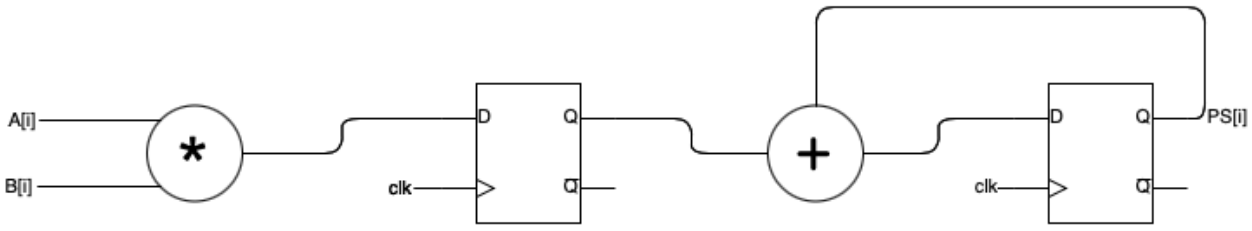

Figure 4

3.2

The circuit is sensitive to both `clk` and `dataIn1` which is not right. There's no `else` which will create redundant memory. We should also use non-blocking statements (`<=` instead of `=`). And output should be `reg`.

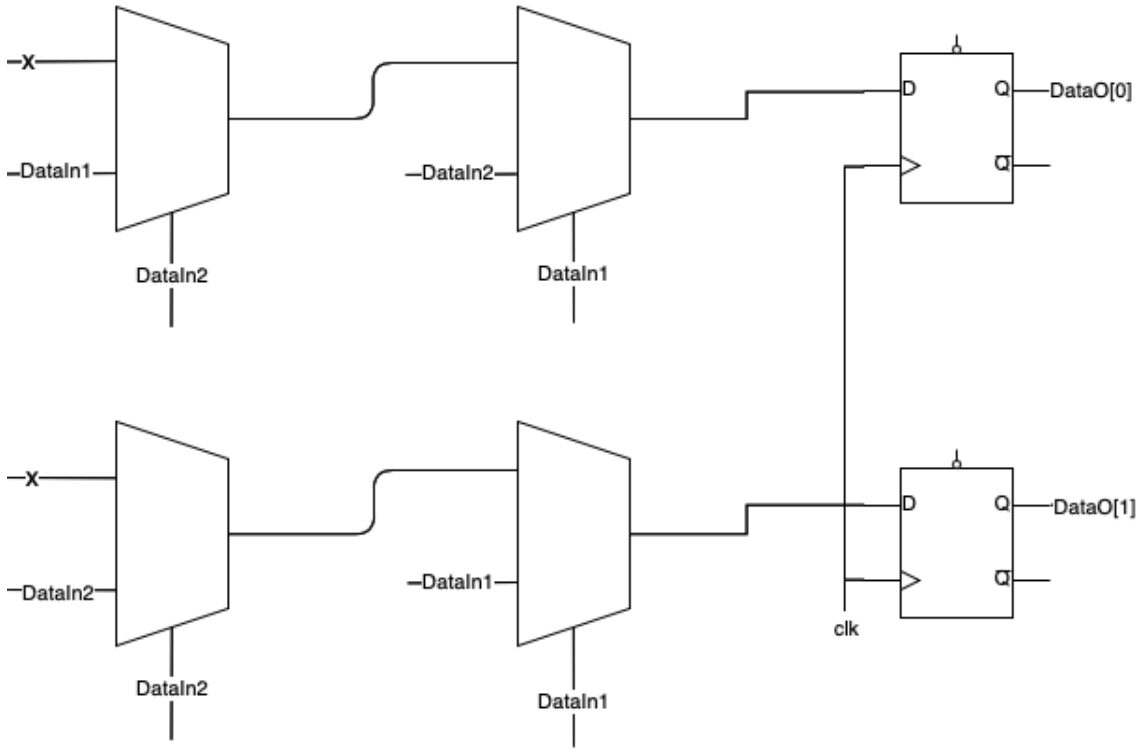

Figure 5