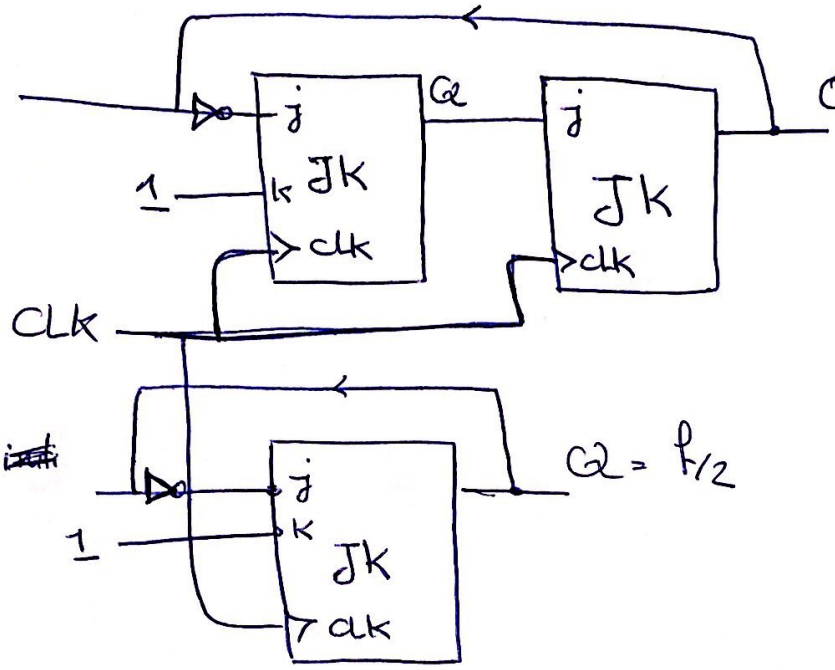
P1.

Q3. We cannot make a gated clock signal

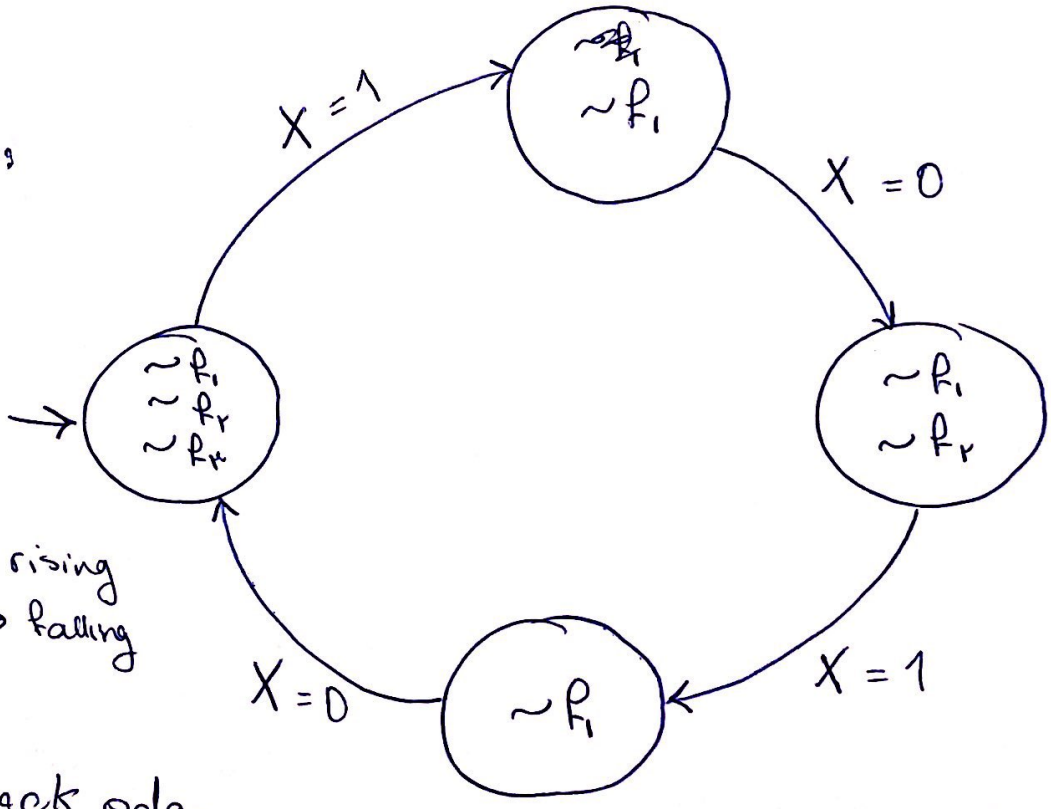
Clock must stay as the golden signal → No gates, direct connection to all FFs.



* k are always High
j is connected to Q and inverted.

Q21.

fsm:



X = 1 → rising
X = 0 → falling

X = Clock edge

↳ Both Rising and Falling