Theme: Next Generation Computing

Sub-Theme: Data Speculation through Value or Address Prediction

Superscalar processors use data speculation to reorder instruction execution for maximizing instruction-level parallelism. Data speculation techniques attempt to hide long latencies of load operations by either predicting their memory addresses or values. The goal of this research subject is to explore novel data speculation techniques through load-value prediction or memory-address prediction.

We are aiming to analyze different data speculation techniques on CPUs targeting mobile benchmarks and applications. Through innovative ideas, we would like to explore new load value prediction and address prediction techniques geared towards an aggressive superscalar design. The following list of expected deliverables is open to discussion.

- Design documents of new concepts of cache technologies and algorithms
- Prototype samples in source code
- Patents with Samsung (if agreed)
- Detailed quarterly progress reports summarizing accomplishments.
- Joint publication in International conferences and journals with Samsung Electronics (if agreed)

We are interested in the following research questions. These questions are not exhaustive but different research questions are open to discuss with research partners.

- In current mobile workloads, what are the sources of locality and predictability of data and memory addresses?
- In a state-of-the-art processor, how can spatial and temporal locality be exploited for data speculation to improve instruction-level parallelism?

- What are efficient algorithms for accurate load value or address prediction on mobile workloads?
- How can value or address prediction be architected for a state-of-the-art processor with minimal power and area overhead?
- What are efficient mechanisms to verify correctness of predicted load values or predicted memory addresses in a state-of-the-art processor.
- What mechanisms can reduce the frequency and overhead of pipeline flushes due to incorrect speculation?
- What meta-storage is required for making accurate predictions, such as history of values and addresses, instruction context?
- How do the prediction algorithms designed as part of this proposal compare with current state-of-the-art prediction algorithms?
- How do value prediction algorithms designed as part of this proposal compare with the results of the 1st Value Prediction Championship held with ISCA-45?
- What are efficient techniques to co-ordinate load address predictors with hardware data prefetchers?

※ The topics are not limited to the above examples and the participants are encouraged to propose original idea.

※ Funding : Up to USD $100,000 per year