1 Incredible ISA Design (very hard)

We want to design a datapath and control FSM for a 4-bit processor with 10-bit instructions that can perform the below operations.

Opcode	**Operands**	**Operation**
00	DR, SR1, SR2, imm2	DR <= (SR1 NAND SR2) + imm2
01	DR, SR, addr4,	DR <= M[SR + addr4][3:0]
10	SR, DR, addr4	M[DR + addr4] <= SR
11	DR, trap, sign, jmp4	If trap == 1, halt. If trap == 0, sign == 0, DR >= 0, PC <= PC + jmp4. If trap == 0, sign == 1, DR < 0, PC <= PC + jmp4.

Assume the processor has 4-bit registers R0 through R3 and PC, 10-bit register IR, 2^4 memory locations, and 10-bit memory addressability. Assume all values that can be stored in registers are signed 4-bit integers.

(a) Create a FSM diagram for this ISA's control FSM. You do not have to write out control signals or next-state expressions. The fetch and decode stage should be very similar to the LC-3.

(b) Create a diagram representing the datapath for this ISA. Again, this should be structured similarly to the LC-3.

(c) In this new ISA, write a program that takes a 4-bit signed integer at M[xF][3:0] and make it positive if it is negative. Assume PC = x0 and all registers are initialized to x0.