HKN ECE 120 Midterm 3 Worksheet

Serialized Design (Review)

Problem 1

Consider one bit-slice of a full adder.

a. How many bits need to be passed between each bit slice? What are they?

b. If we wanted to serialize this design and add 1 bit at a time, how many D flip-flops would we need to store these signals?

c. Implement a serialized binary adder, adding 1 bit at a time.

d. Assume we instead wanted to add 4 bits (1 hexadecimal) at a time. Would any signals be different?

e. Implement a serialized binary adder, adding 4 bits at a time.

Problem 2

Consider a serialized circuit that takes a sequence of bits, 1 bit at a time, and outputs the same sequence of bits but is delayed by 2 bits and inverted. For example, assuming inputs and outputs are taken at the start of each clock cycle, if the input is 100101101100, then the output is XX0110100100.

a. How many bits do we need to store between each clock cycle?

b. Implement this circuit using D flip-flops.

c. Can we also implement this circuit using a shift register?

Problem 3

In 50 words or less, what are the advantages and disadvantages of serialization over bit-slicing?

Finite State Machines

Problem 1

Suppose we wanted to create a Moore FSM that has two outputs Z and O. Z is 1 if and only if the input contains three or more consecutive zeroes, and O is 1 if and only if the input contains three or more consecutive ones.

a. How many unique states do we need for this finite state machine? How many bits do we need to represent all states?

b. Draw a state diagram for this FSM, showing all states used.

c. Create a truth table for this FSM. For unused states, write X.

d. Use K-maps or another method to derive next-state expressions for this FSM.

e. Implement this FSM using D flip-flops.

Problem 2

Suppose we wanted to create a Mealy FSM that represents an elevator in a building with 6 floors, 1 through 6. It takes two clock cycles for the elevator to move between floors. The input is a 3-bit unsigned integer $I_2I_1I_0$ and the output is a single bit F that is 1 when the elevator has reached the correct floor and 0 when it has not. You may assume that the input is always between 1 and 6 (inclusive).

a. How many unique states do we need for this finite state machine? How many bits do we need to represent all states?

b. Draw a state diagram for this FSM, showing all states used. You may also use comparisons ($=, <, >$). (Hint: it might be helpful to enumerate the states in a way that preserves the 3-bit floor)

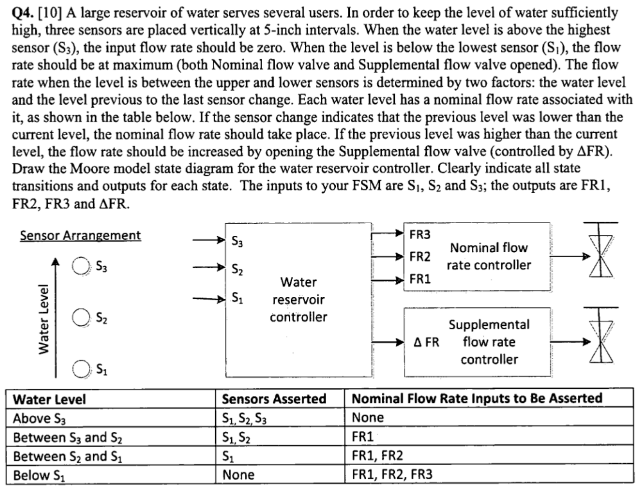
c. Create a truth table for this FSM, defining new intermediate variables for your comparisons. For unused states, write X.

d. Use K-maps or another method to derive next-state expressions for this FSM.

e. Implement this FSM using D flip-flops and a 3-bit digital comparator, with outputs for $A > B$, $A = B$, and $A < B$. Feel free to use adders, MUXes, buses, or any other component covered earlier in the course.

Problem 3

Taken from HDLBits "Design a Moore FSM"



Q4. [10] A large reservoir of water serves several users. In order to keep the level of water sufficiently high, three sensors are placed vertically at 5-inch intervals. When the water level is above the highest sensor (S_3), the input flow rate should be zero. When the level is below the lowest sensor (S_1), the flow rate should be at maximum (both Nominal flow valve and Supplemental flow valve opened). The flow rate when the level is between the upper and lower sensors is determined by two factors: the water level and the level previous to the last sensor change. Each water level has a nominal flow rate associated with it, as shown in the table below. If the sensor change indicates that the previous level was lower than the current level, the nominal flow rate should take place. If the previous level was higher than the current level, the flow rate should be increased by opening the Supplemental flow valve (controlled by ΔFR). Draw the Moore model state diagram for the water reservoir controller. Clearly indicate all state transitions and outputs for each state. The inputs to your FSM are S_1, S_2 and S_3; the outputs are FR1, FR2, FR3 and ΔFR.

Sensor Arrangement
Water Level
S_3
S_2
S_1
S_3
S_2
S_1
Water reservoir controller
FR3
FR2
FR1
Nominal flow rate controller
Δ FR
Supplemental flow rate controller

Water Level	Sensors Asserted	Nominal Flow Rate Inputs to Be Asserted
Above S_3	S_1, S_2, S_3	None
Between S_3 and S_2	S_1, S_2	FR1
Between S_2 and S_1	S_1	FR1, FR2
Below S_1	None	FR1, FR2, FR3

Memory

Problem 1

a. What is memory addressability? What is the difference between memory addressability and a memory address?

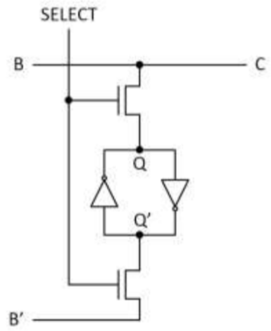
b. What is the purpose of the chip select signal in a RAM block?

c. What is the purpose of the write enable signal in a RAM block?

d. Describe the process to read from a RAM block. Detail the signal values:

e. Describe the process to write from a RAM block. Detail the signal values:

Problem 2



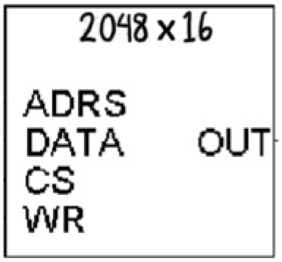
a. What should we apply to Select, B and B' in order to read the value Q to C?

b. What should we apply to Select, B and B' in order to hold a value Q?

c. What should we apply to Select, B and B' in order to write a 0 to Q?

d. What should we apply to Select, B and B' in order to write a 1 to Q?

Problem 3



For each of the combinations below, select and draw those that can be used to build a 2048 x 12 RAM using only the parts given. If not possible, explain why. Assume that logic 0 and 1 signals are available and that the chip select and write enable are active-high.

a. Two 1024 x 6 RAMs and one 4:1 multiplexer

b. Four 512 x 12 RAMs and a 2:4 priority encoder

c. Two 2048 x 6 RAMs

d. Four 512 x 3 RAMs and two 4:1 multiplexers

LC-3 ISA

Problem 1

Review Questions. Answer for the LC-3 ISA.

a. How many bits are used to address memory? What is the memory address space?

b. How many bits of data are stored at each memory space/what is the memory addressibility?

c. What is the bus width?

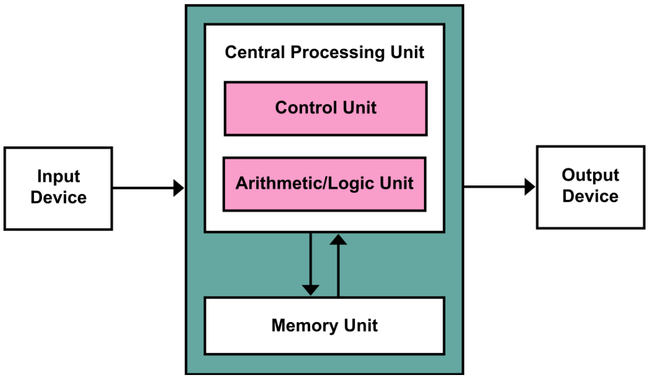
d. How many registers are in the register file? How wide are they?

e. How many other registers are there? How wide are they?

f. How do we control which signals are sent to the system bus?

Problem 2

Consider the Von Neumann Architecture.



a In 50 words or less, explain the role of the control unit.

b In 50 words or less, explain the role of the ALU.

c For the LC-3 ISA, what does the control unit correspond to?

d For the LC-3 ISA, what are the inputs and outputs?

Problem 3

Tracing LC-3. Refer to Patt and Patel Figure C.2.

a Write down the control signals for states 18, 33, 35, and 32 in the following tables. Use X for unused signals.

State	LD.BEN	LD.MAR	LD.MDR	LD.IR	LD.PC	LD.REG	LD.CC
18							
33							
35							
32							

State	GateMARMUX	GateMDR	GateALU	GatePC	MARMUX	PCMUX
18						
33						
35						
32						

State	ADDR1MUX	ADDR2MUX	DRMUX	SR1MUX	ALUK	MIO.EN	R.W
18							
33							
35							
32							

b What are the components of the instruction processing cycle for LC-3?

c What does each state correspond to in the instruction processing cycle?

d Suppose we wanted to make a new state that performs the following operation: $R6 \longleftarrow R6 + \text{PC}$, set CC. Write down the control signals that are needed and what they should be.

Problem 4

Implementing a new instruction, including control signals.

We want to implement the following instruction:
PC $\longleftarrow$ PC + M[BaseR + PCOffset6] + 1

Note: the +1 is to accommodate state 18.
Note 2: In the very rare case that you actually read the textbook, pretend Appendix C.6.3 did not exist.

a We know that LC-3 has one unused opcode, the opcode 1101. When this opcode is decoded, suppose that the LC-3 FSM enters state 48 (110000). How many FSM states will this instruction need? What will each state do? Assign them in the 48-55 range.

b How will each instruction transition to each other state? Draw a state diagram.

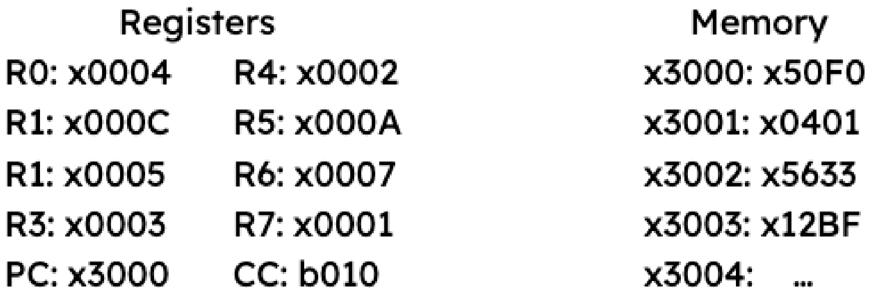
c Using K-maps or another method, write an expression for the next state transition. (Hint: $S_5S_4S_3 = 110$, and memory ready is the signal R. you can work with the 4 bits $RS_2S_1S_0$)

d Using a similar table as in Problem 3a, write down the control signals for each state.

e Trace through your instruction with the following instruction:
1101 000 101 000111
Assume PC = x3001, R5 = x2000, and M[x2007] = x8EED.
What is PC after the instruction completes and before the next execution of state 18?

LC-3 Assembly

Problem 1



Registers		Memory
R0: x0004	R4: x0002	x3000: x50F0
R1: x000C	R5: x000A	x3001: x0401
R1: x0005	R6: x0007	x3002: x5633
R3: x0003	R7: x0001	x3003: x12BF
PC: x3000	CC: b010	x3004: ...

1. Starting at address x3000, the LC-3 processor will continue until the instruction at x3003 finishes executing. What are the values in each of the registers below?

R0: __________

R1: __________

R2: __________

R3: __________

PC: __________

CC: __________

2. Write a complete list of the sequence of values taken by the MAR register as the LC-3 processes these instructions. Use only as many lines as are necessary.

#1: x3000 (initial value)

#2: ____________________

#3: ____________________

#4: ____________________

#5: ____________________

#6: ____________________

#7: ____________________

#8: ____________________

Problem 2

Write an LC-3 Assembly program that compares two numbers in R2 and R3 and puts the larger number into R1. If the numbers are equal, then R1 is set equal to 0. Use as many lines as necessary.

x3000: ____________________

x3001: ____________________

x3002: ____________________

x3003: ____________________

x3004: ____________________

x3005: ____________________

x3006: ____________________

x3007: ____________________

x3008: ____________________

x3009: ____________________

x300A: ____________________

x300B: ____________________

x300C: ____________________

x300D: ____________________

x300E: ____________________

x300F: ____________________

x3010: ____________________

x3011: ____________________

x3012: ____________________

Problem 3

Write two LC-3 Assembly programs that executes a bitwise OR operation and a bitwise XOR operation respectively on R4 and R5 and puts the result in R1. How might you extend these to support NOR and XNOR?

OR

x3000: ____________________

x3001: ____________________

x3002: ____________________

x3003: ____________________

x3004: ____________________

x3005: ____________________

XOR

x3000: ____________________

x3001: ____________________

x3002: ____________________

x3003: ____________________

x3004: ____________________

x3005: ____________________

x3006: ____________________

x3007: ____________________

x3008: ____________________

x3009: ____________________

x300A: ____________________

x300B: ____________________

x300C: ____________________

Problem 4

a. Assuming LC-3 now has 32 registers, we want to increase the number of registers that we can specify in the LC-3 ADD instruction to 32. Is there a problem with this? Explain.

b. A memory's addressibility is 64 bits. What does that tell you about the size of the MAR and MDR, given a 64-bit ISA and 2^{20} memory locations?

c. Say we have a memory consisting of 256 locations, and each location contains 16 bits. How many bits are required for the address for a byte-addressable system? Explain.