HKN ECE 342 Final Worksheet - Cramming Carnival

DC Analysis

Transistor Parameters

MOSFETs:

$$\mu_n C_{ox} = 100\ \mu\text{A/V}^2;\ V_{TN} = 1\ \text{V}$$

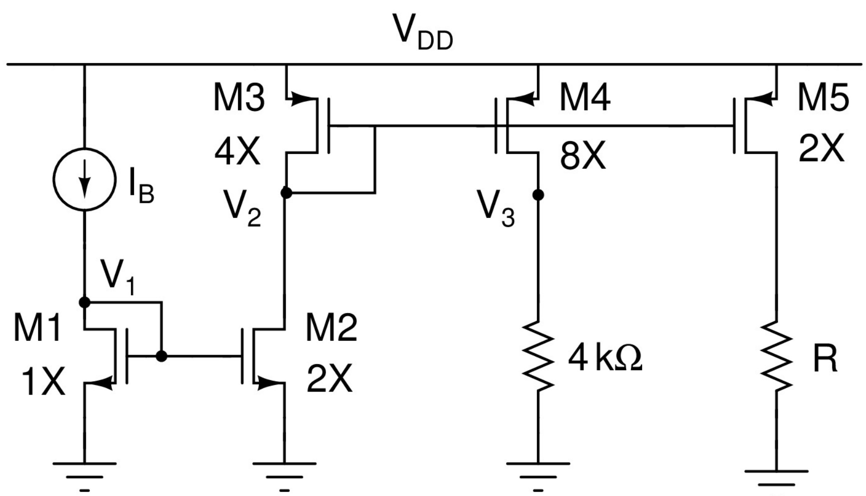
$$\mu_p C_{ox} = 50\ \mu\text{A/V}^2;\ |V_{TP}| = 1\ \text{V}$$

BJTs:

$$\beta = 99; V_{\text{BE,on}} = 0.7\ \text{V}$$

Problem 1

For this problem, refer to the circuit below. Use $V_{DD} = 5$ V, $I_B = 200\ \mu$A, 1X $= \frac{100}{1}$.

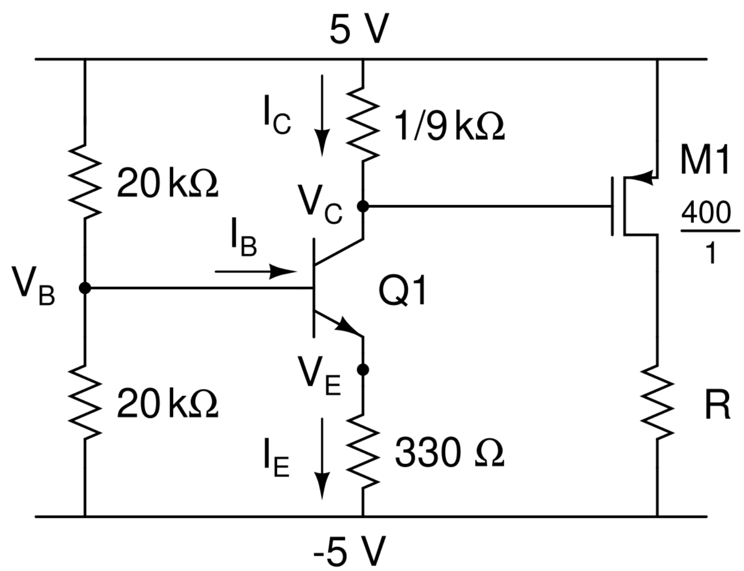


(a) Determine the DC voltages V_1, V_2, and V_3.

(b) Determine the value of R such that M5 is biased at the edge of saturation.

Problem 2

For this problem, refer to the circuit below.



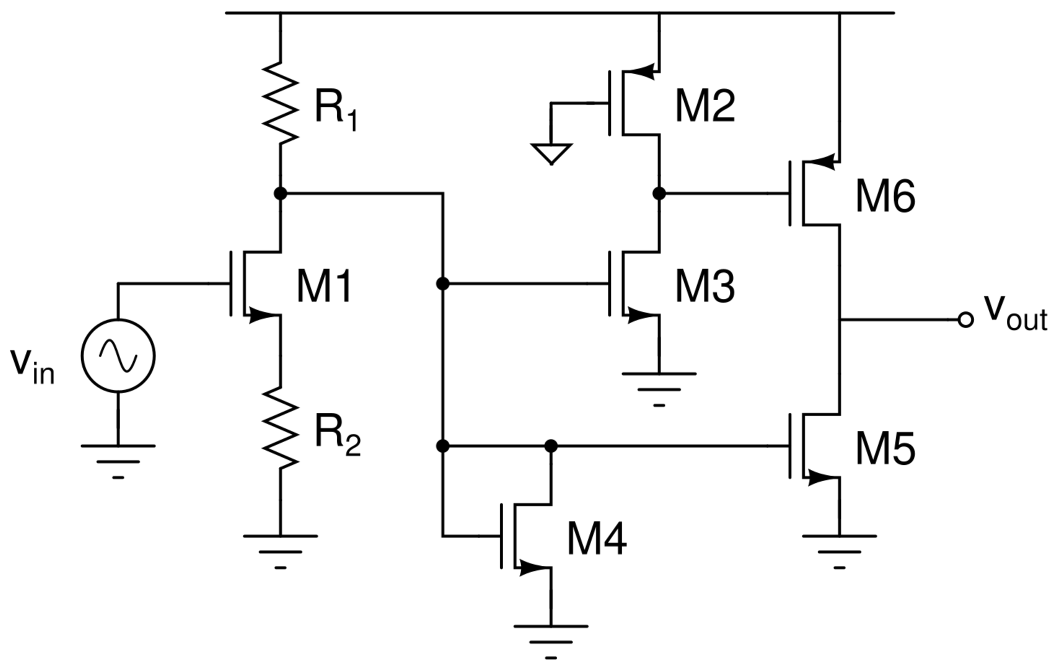
(a) Determine the DC currents and voltages V_B, V_E, V_C, I_B, I_E, and I_C of Q1. What is its region of operation?

(b) Determine the value of R such that M1 is biased at the edge of saturation.

Small-Signal Analysis

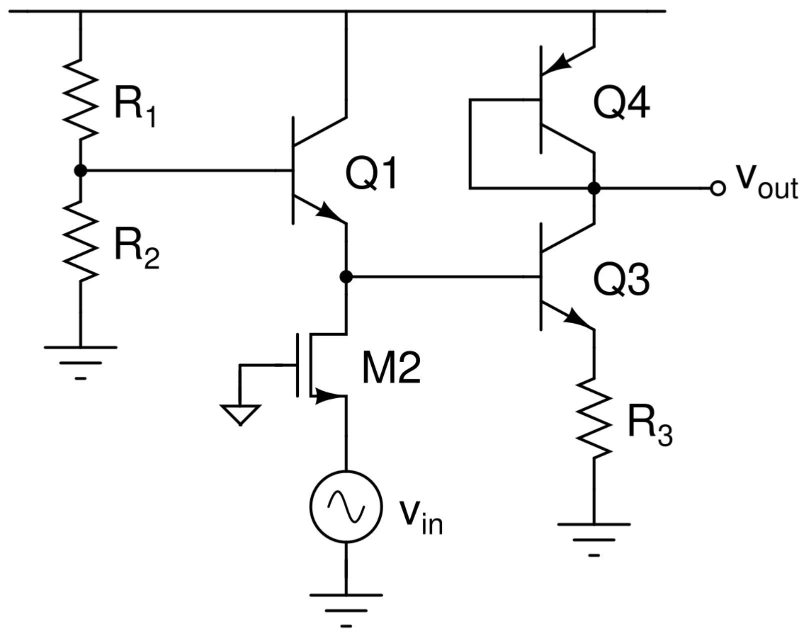
Problem 1

Determine the values of G_M, R_{OUT}, and $A_v = v_{out}/v_{in}$ of this amplifier. Assume all MOSFETs are biased in saturation. Do not assume $r_{ds} = \infty$, though you can assume $g_m r_{ds} >> 1$.



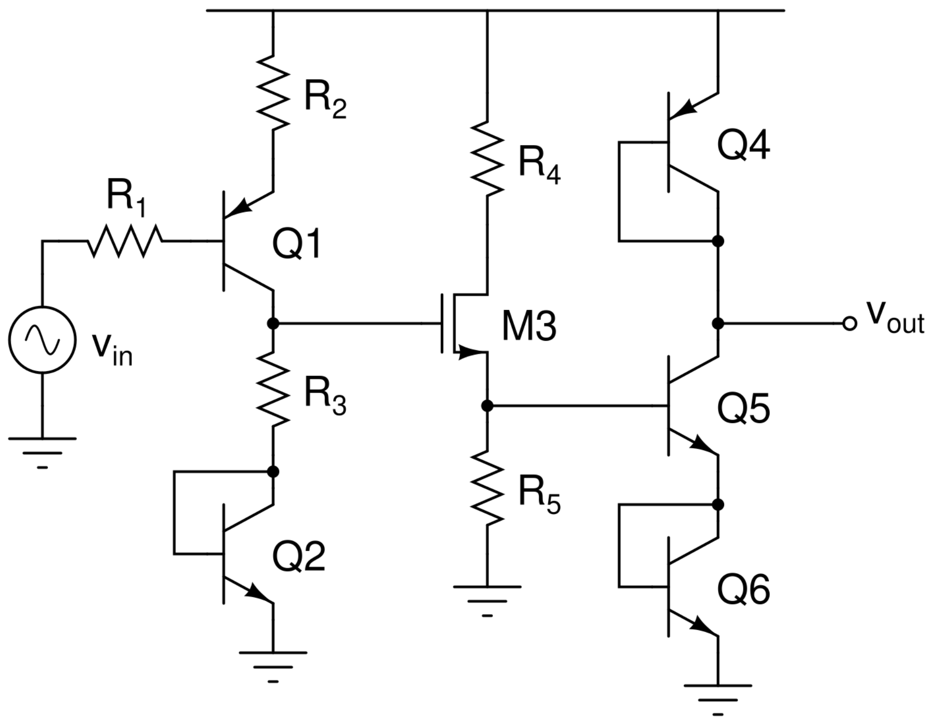
Problem 2

Determine the values of G_M, R_{OUT}, and $A_v = v_{out}/v_{in}$ of this amplifier. Assume all MOSFETs are biased in saturation, all BJTs are biased in forward active mode, $r_{ds} \neq \infty$, $r_0 = \infty$, and $g_m r_{ds} \gg 1$.



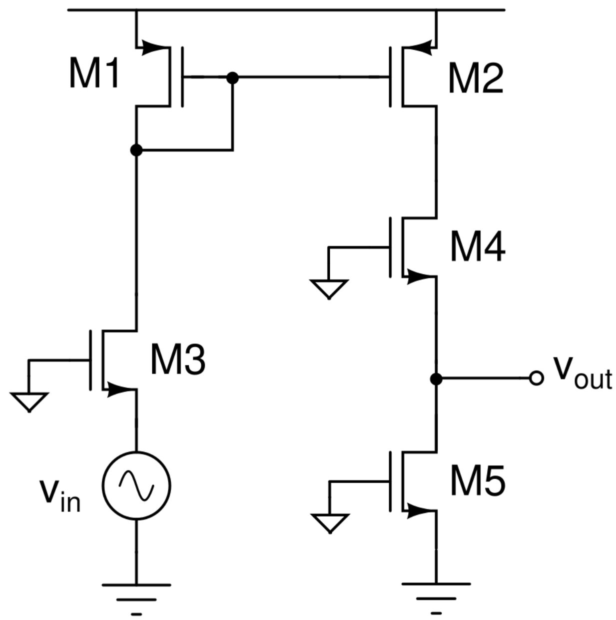
Problem 3

Determine the values of G_M, R_{OUT}, and $A_v = v_{out}/v_{in}$ of this amplifier. Assume all MOSFETs are biased in saturation, all BJTs are biased in forward active mode, $r_{ds} \neq \infty$, $r_0 = \infty$, and $g_m r_{ds} \gg 1$.



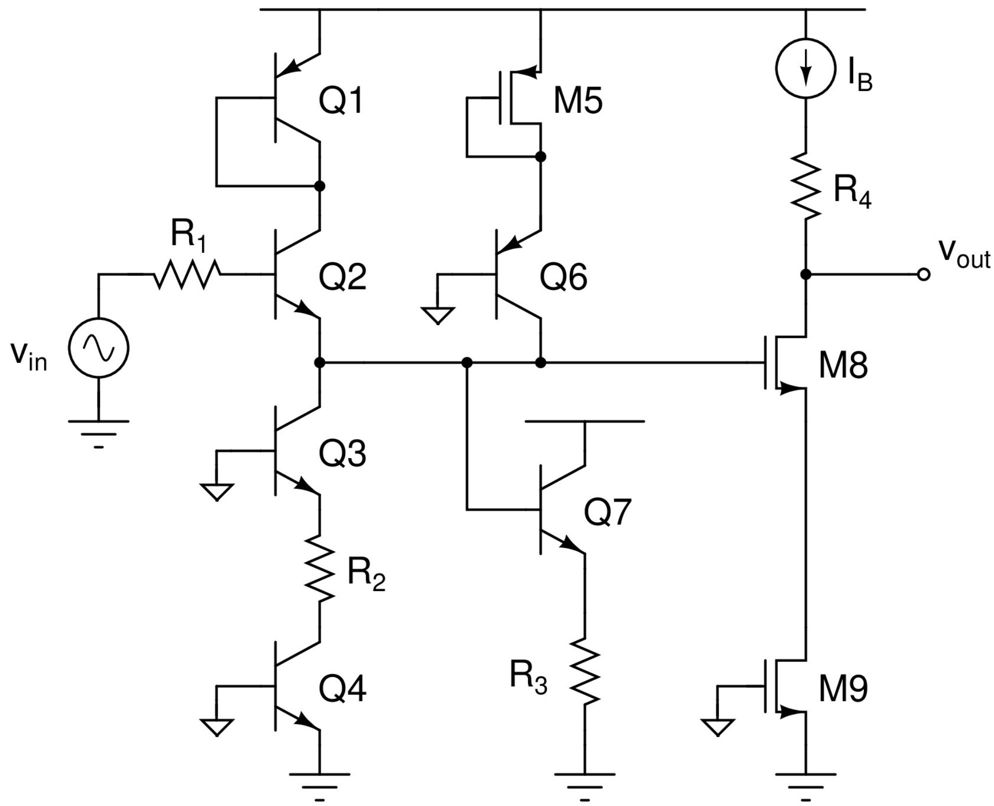
Problem 4

Determine the values of G_M, R_{OUT}, and $A_v = v_{out}/v_{in}$ of this amplifier. Assume all MOSFETs are biased in saturation. Do not assume $r_{ds} = \infty$, though you can assume $g_m r_{ds} >> 1$.



Problem 5

Determine the values of G_M, R_{OUT}, and $A_v = v_{out}/v_{in}$ of this amplifier. Assume all MOSFETs are biased in saturation, all BJTs are biased in forward active mode, $r_{ds} \neq \infty$, $r_0 = \infty$, and $g_m r_{ds} \gg 1$.



Bode Plots

Problem 1

For the following amplifier transfer functions, **(i)** plot the magnitude response, **(ii)** determine the unity gain frequency, and **(iii)** plot the phase response:

(a)

$$H(s) = \frac{10^4}{s(1 + s/10^3)}$$

(b)

$$H(s) = \frac{2000\left(1 + s/10^2\right)}{(1 + s/10)\,(1 + s/10^3)\,(1 + s/10^4)}$$

(c)

$$H(s) = \frac{4000(1 + s/10^2)}{(1 + s/10)(1 + s/10^4)^2}$$

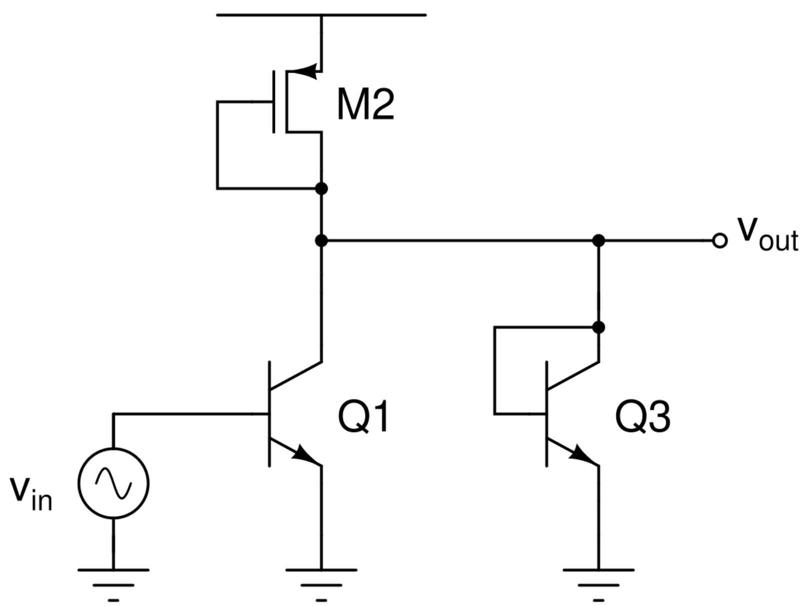
Problem 2

For each of the amplifier transfer functions in Problem 1, determine the incremental output voltage response $v_{out}(t)$ to an incremental input voltage $v_{in}(t) = 10\cos(10^3 \cdot t)$ mV.

Open Circuit Time Constants

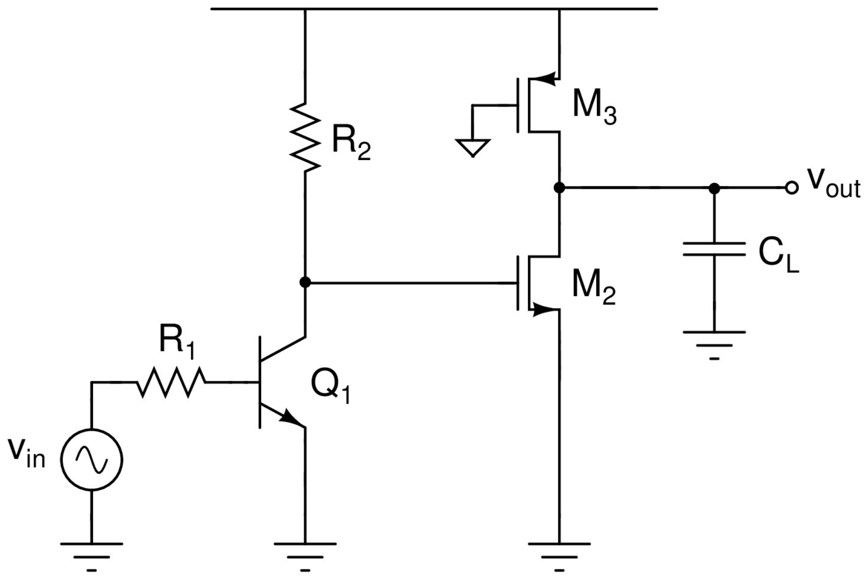
Problem 1

Use the open-circuit time constant method to estimate the -3 dB frequency, $\omega_{-3\mathrm{dB}}$, of this amplifier. Consider C_{gs}, C_{gd}, C_{π}, C_{μ}, and r_{ds}. Ignore r_0.



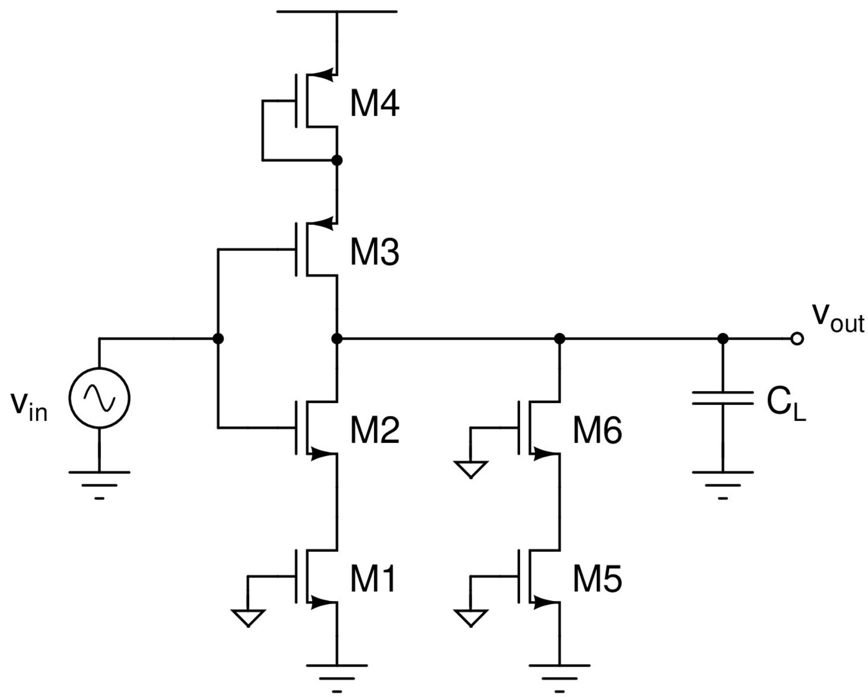
Problem 2

Use the open-circuit time constant method to estimate the -3 dB frequency, $\omega_{-3\text{dB}}$, of this amplifier. Consider C_{gs}, C_{gd}, C_{π}, C_{μ}, and r_{ds}. Ignore r_0.



Problem 3

Use the open-circuit time constant method to estimate the -3 dB frequency, $\omega_{-3\text{dB}}$, of this amplifier. Consider C_{gs}, C_{gd}, C_{π}, C_{μ}, and r_{ds}.



CMOS Logic Circuits

For each part, design and draw the schematic of a CMOS logic gate that implements the Boolean expression. In each schematic, label the size of each transistor such that the worst case delays of the pull-up and pull-down networks are equivalent to those of a standard minimum-sized inverter with $(W/L)_P/(W/L)_N = 2$. Inverted inputs are not available.

(a) $Z_1 = \overline{(A + B) \cdot C}$

(b) $Z_2 = \overline{(A \cdot B \cdot C) + (D \cdot E)}$

(c) $Z_3 = \overline{A} \cdot (\overline{B} + \overline{C} + \overline{D})$