HKN ECE 120 Midterm 2 Worksheet

CMOS Logic

Problem 1

Draw the CMOS network for the following expressions:

a. $Z = A'$

b. $Z = (A \cdot B)'$

c. $Z = (A + B)'$

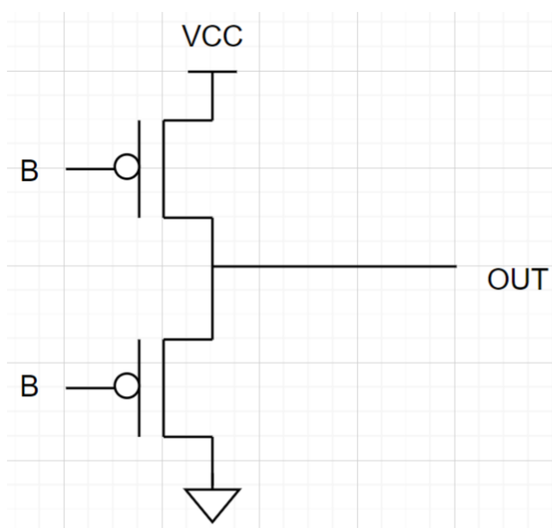
d. $Z = ((A + B) \cdot C)'$

e. $Z = ((B \cdot C) + A)'$

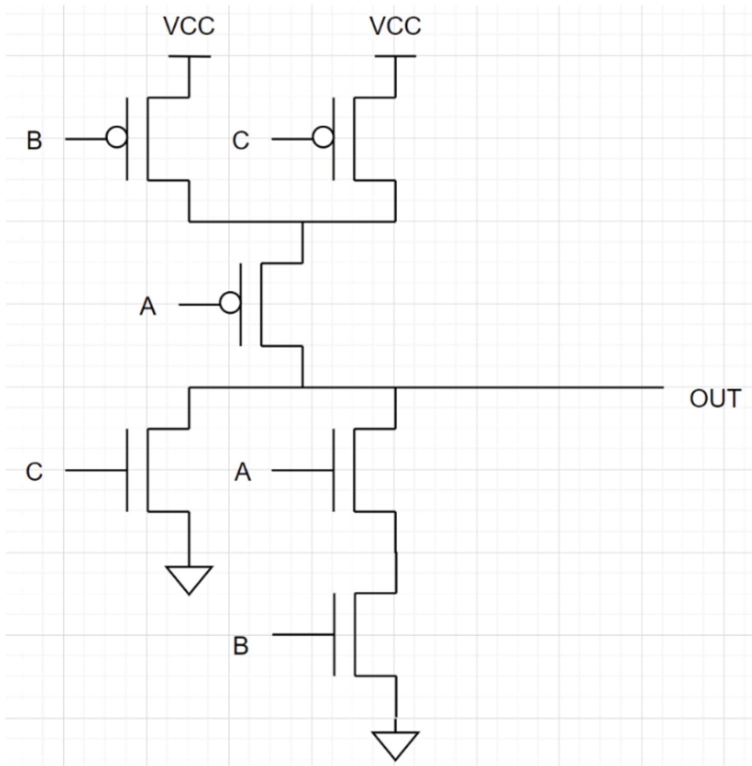
Problem 2

Are these valid CMOS networks? If not, explain why.

a.



b.



Boolean Expressions, Algebra, & Optimization

Problem 1

Simplify the following expressions:

a. $F(A, B, C) = (A + B) \cdot (B' + C) \cdot (A + C)$

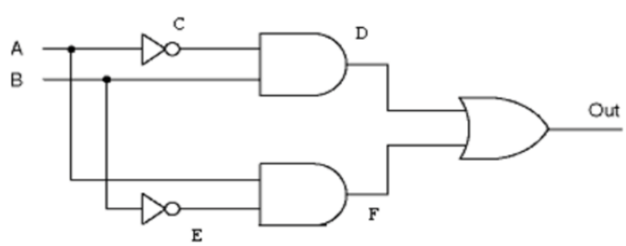
b. $F(A, B, C) = A'BC + ABC + ABC' + AB'C$

c. $F(A, B, C) = A' \cdot (A + B) + (A + B) \cdot (A + B')$

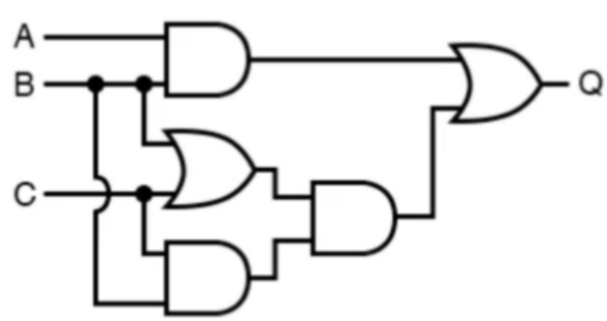
Problem 2

True or False:

a. The delay for the following expression is 2.



b. The area for the following expression is 7.



K-maps, SOP & POS Expressions

Problem 1

Use K-maps or simplification to find the minimal SOP and POS expressions for the following, then draw them in NAND/NOR form:

a.

B	**C**	**D**	**Z**
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	X
1	1	1	1

b.

A	**B**	**C**	**D**	**Z**
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	X
0	1	1	1	X
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

Adders, ALUs, and Bit-Slicing

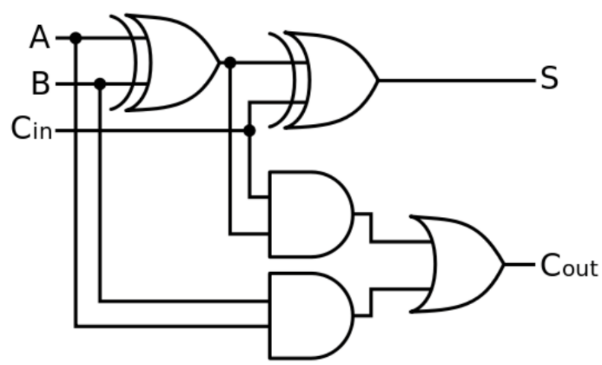
Problem 1

Remember that the logical output for one slice of a full adder is:

A	**B**	**Cin**	**Cout**	**S**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

a. Find an expression for Cout and S using AND and OR gates.

b. Consider the digital circuit:



Verify that it is equivalent to your expression.

Problem 2

Build each of these circuits using only adders, inverters, and fixed inputs (1 or 0). Do not account for overflows unless otherwise noted.

a. For two 4-bit unsigned integers $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$, calculate the 5-bit unsigned integer $S_4S_3S_2S_1S_0 = A + B$.

b. For two 4-bit two's complement integers $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$, calculate the 4-bit two's complement integer $S_3S_2S_1S_0$ where $S = A - B$.

c. For three 3-bit two's complement integers $A_2A_1A_0$, $B_2B_1B_0$, $C_2C_1C_0$, calculate $S_2S_1S_0 = A + A - B - C$.

Problem 3

Assume an ALU that takes two 8-bit integers A and B as input and can calculate AB (AND),

a. How many bits is the output S?

b. How many bits must the control signal be?

c. Is the ALU logically complete? Assume you have 0 and 1 available.

d. (Optional) Draw out the full circuit diagram for this ALU, using basic logic gates, MUXs, decoders, and full adders.

Problem 4

In 50 or fewer words, explain the advantages and disadvantages of bit-slicing over optimizing for many variables.

Multiplexers

Problem 1

Write down the truth table for a 2-to-1 multiplexer. Write an expression for the output, and implement the 2:1 MUX using AND gates, OR gates, and inverters.

Problem 2

Using the same process (you may not need the truth table), implement a 4:1 MUX using AND gates, OR gates, and inverters.

Problem 3

Implement a 4:1 MUX using three 2:1 MUXs.

Problem 4

Implement a 8:1 MUX using two 4:1 MUXs and a 2:1 MUX.

Decoders

Problem 1

In 20 words or less, what does a decoder do?

Problem 2

Implement a 2x4 decoder using AND gates, OR gates, and inverters.

Problem 3

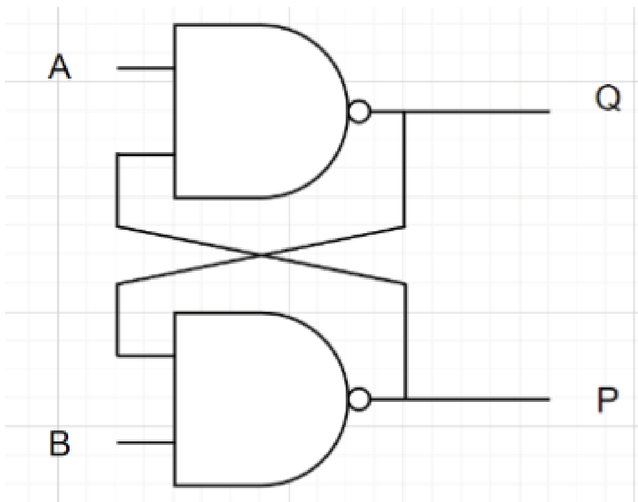
Implement a 4x16 decoder using five 2x4 decoders. (Hint: you should use the ENABLE pin)

Latches & Flip-Flops

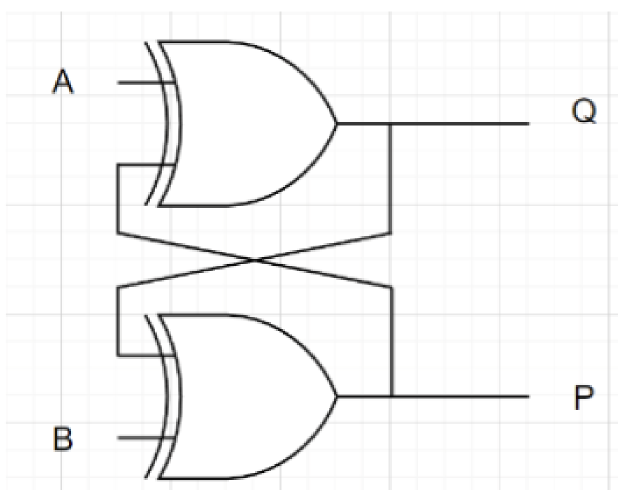
Problem 1

Find the stable states of the following latches:

a.



b.

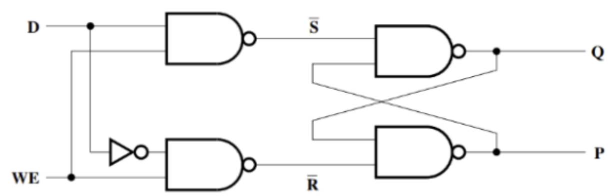


c. Which latch is more viable for data storage?

Problem 2

Explain the process of storing a bit of data in a D latch.

a gated D latch (stores a single bit)



Problem 3

Explain the difference between a D latch and a D flip-flop.

Problem 4

Implement a 4-bit register using D flip-flops.

Problem 5

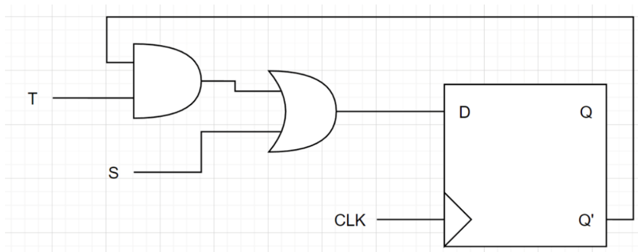
Implement a 4-bit shift register with MSB load using D flip-flops.

Problem 6

Implement a 4-bit circular shift register with 4-bit load using D flip-flops.

Problem 7

Consider this digital circuit below.



Assume at the start, $Q = 0$. Trace and fill out the table below. T and S signals are given in the table.

Clock Cycle #	Q	T	S	Qnext
0	0	1	0	
1		1	0	
2		0	0	
3		0	0	
4		0	1	

Problem 8

What are timing hazards? What are a few ways we can design around them? (Lumetta 2.6.3-2.6.5)

Serialized Design

Problem 1

Consider one bit-slice of a full adder.

a. How many bits need to be passed between each bit slice? What are they?

b. If we wanted to serialize this design and add 1 bit at a time, how many D flip-flops would we need to store these signals?

c. Implement a serialized binary adder, adding 1 bit at a time.

d. Assume we instead wanted to add 4 bits (1 hexadecimal) at a time. Would any signals be different?

e. Implement a serialized binary adder, adding 4 bits at a time.

Problem 2

Consider a serialized circuit that takes a sequence of bits, 1 bit at a time, and outputs the same sequence of bits but is delayed by 2 bits and inverted. For example, assuming inputs and outputs are taken at the start of each clock cycle, if the input is 100101101100, then the output is XX0110100100.

a. How many bits do we need to store between each clock cycle?

b. Implement this circuit using D flip-flops.

c. Can we also implement this circuit using a shift register?

Problem 3

In 50 words or less, what are the advantages and disadvantages of serialization over bit-slicing?