
STM32
CubeMX

1. Description

1.1. Project

Project Name	Nucleo-H745
Board Name	NUCLEO-H745ZI-Q
Generated with:	STM32CubeMX 6.9.2
Date	02/07/2024

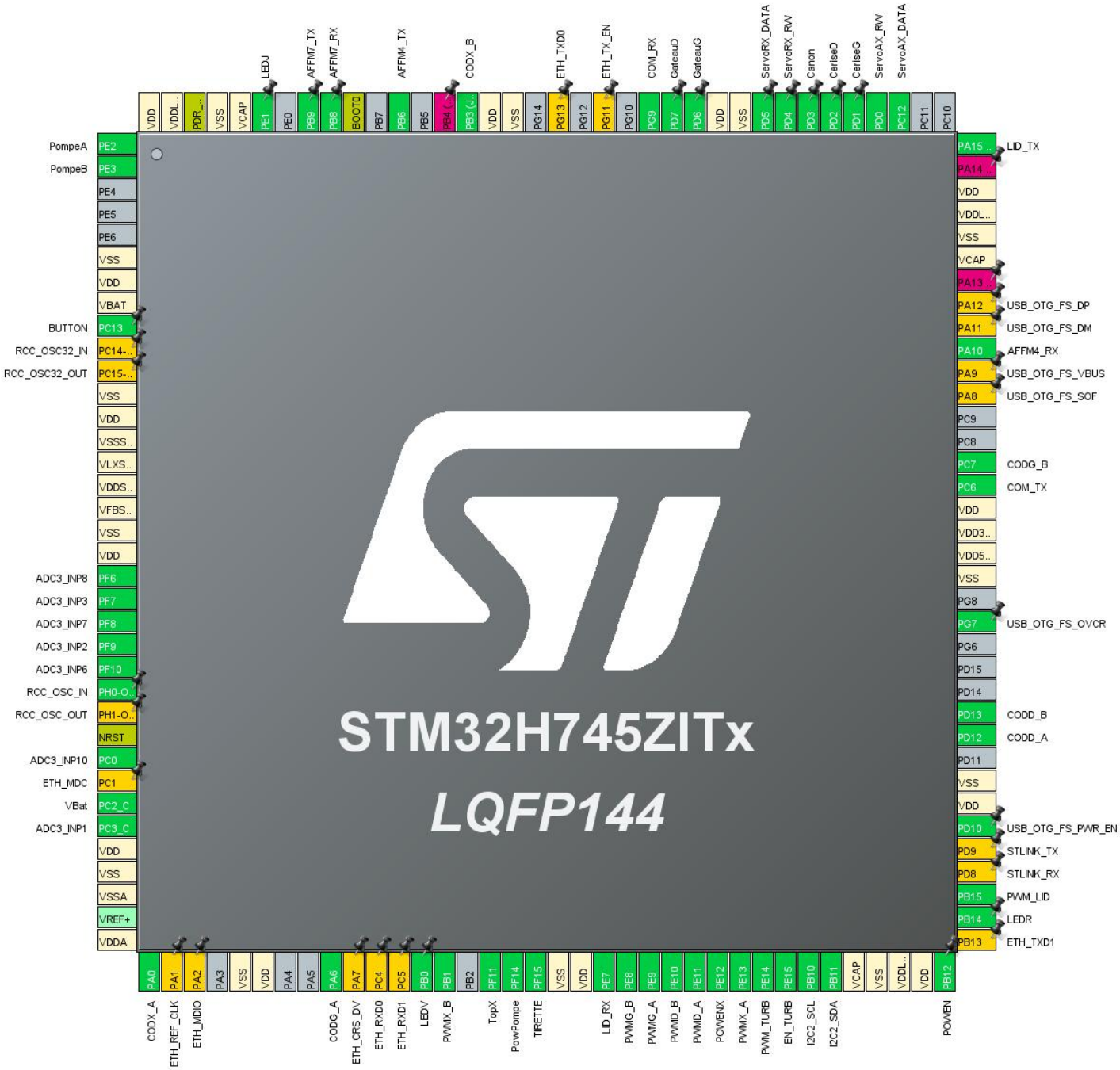
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	PompeA
2	PE3 *	I/O	GPIO_Output	PompeB
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
9	PC13 *	I/O	GPIO_Input	BUTTON
10	PC14-OSC32_IN (OSC32_IN) **	I/O	RCC_OSC32_IN	
11	PC15-OSC32_OUT (OSC32_OUT) **	I/O	RCC_OSC32_OUT	
12	VSS	Power		
13	VDD	Power		
14	VSSSMPS	Power		
15	VLXSMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
18	VSS	Power		
19	VDD	Power		
20	PF6	I/O	ADC3_INP8	
21	PF7	I/O	ADC3_INP3	
22	PF8	I/O	ADC3_INP7	
23	PF9	I/O	ADC3_INP2	
24	PF10	I/O	ADC3_INP6	
25	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
26	PH1-OSC_OUT (PH1) **	I/O	RCC_OSC_OUT	
27	NRST	Reset		
28	PC0	I/O	ADC3_INP10	
29	PC1 **	I/O	ETH_MDC	
30	PC2_C	I/O	ADC3_INP0	VBat
31	PC3_C	I/O	ADC3_INP1	
32	VDD	Power		
33	VSS	Power		
34	VSSA	Power		
36	VDDA	Power		
37	PA0	I/O	TIM2_CH1	CODX_A
38	PA1 **	I/O	ETH_REF_CLK	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PA2 **	I/O	ETH_MDIO	
41	VSS	Power		
42	VDD	Power		
45	PA6	I/O	TIM3_CH1	CODG_A
46	PA7 **	I/O	ETH_CRS_DV	
47	PC4 **	I/O	ETH_RXD0	
48	PC5 **	I/O	ETH_RXD1	
49	PB0 *	I/O	GPIO_Output	LEDV
50	PB1	I/O	TIM1_CH3N	PWMX_B
52	PF11 *	I/O	GPIO_Input	TopX
53	PF14 *	I/O	GPIO_Output	PowPompe
54	PF15 *	I/O	GPIO_Input	TIRETTE
55	VSS	Power		
56	VDD	Power		
57	PE7	I/O	UART7_RX	LID_RX
58	PE8	I/O	TIM1_CH1N	PWMG_B
59	PE9	I/O	TIM1_CH1	PWMG_A
60	PE10	I/O	TIM1_CH2N	PWMD_B
61	PE11	I/O	TIM1_CH2	PWMD_A
62	PE12 *	I/O	GPIO_Output	POWENX
63	PE13	I/O	TIM1_CH3	PWMX_A
64	PE14	I/O	TIM1_CH4	PWM_TURB
65	PE15 *	I/O	GPIO_Output	EN_TURB
66	PB10	I/O	I2C2_SCL	
67	PB11	I/O	I2C2_SDA	
68	VCAP	Power		
69	VSS	Power		
70	VDDLDO	Power		
71	VDD	Power		
72	PB12 *	I/O	GPIO_Output	POWEN
73	PB13 **	I/O	ETH_TXD1	
74	PB14 *	I/O	GPIO_Output	LEDR
75	PB15	I/O	TIM12_CH2	PWM_LID
76	PD8 **	I/O	USART3_TX	STLINK_RX
77	PD9 **	I/O	USART3_RX	STLINK_TX
78	PD10 *	I/O	GPIO_Output	USB_OTG_FS_PWR_EN
79	VDD	Power		
80	VSS	Power		
82	PD12	I/O	TIM4_CH1	CODD_A

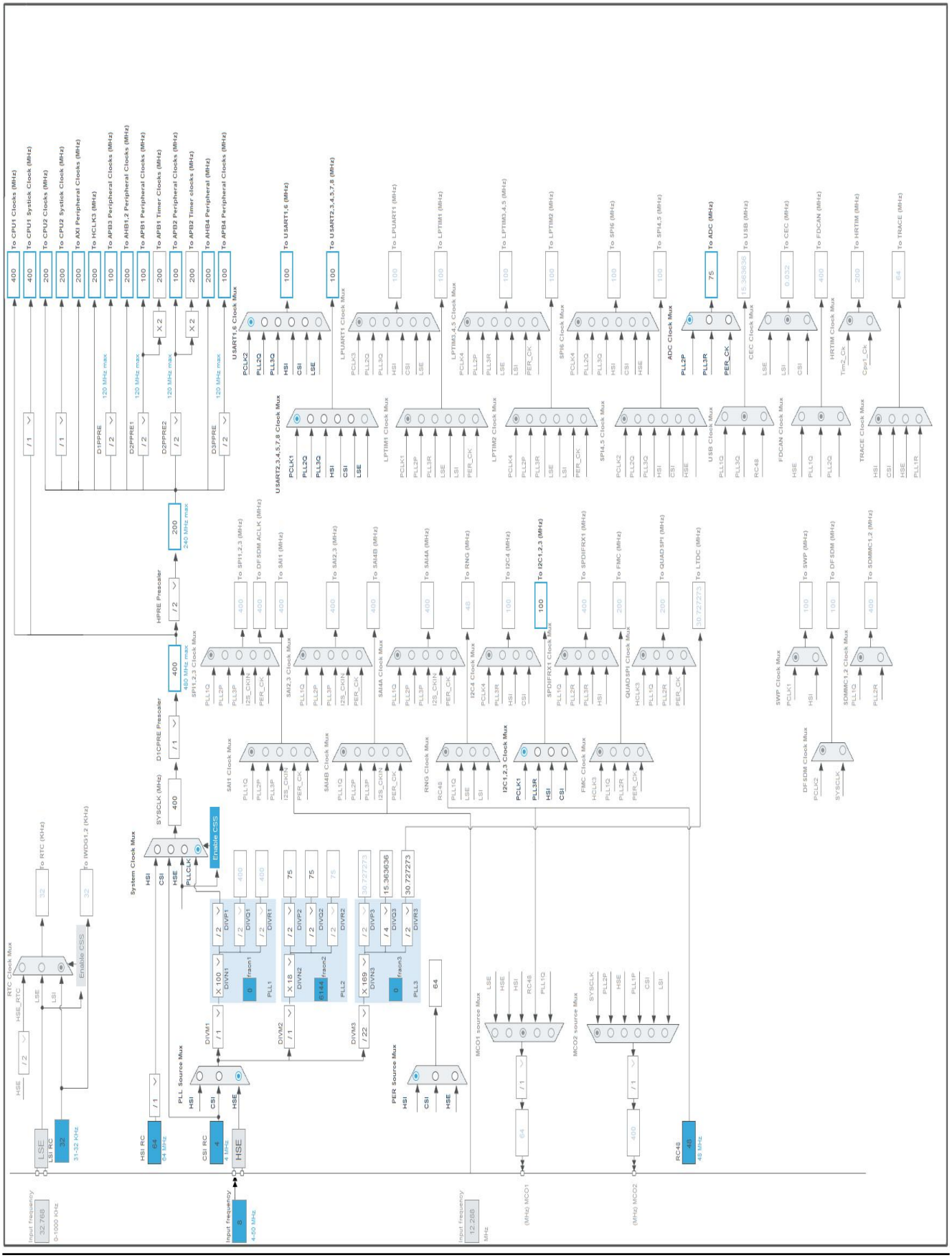
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
83	PD13	I/O	TIM4_CH2	CODD_B
87	PG7	I/O	GPIO_EXTI7	USB_OTG_FS_OVCR
89	VSS	Power		
90	VDD50_USB	Power		
91	VDD33_USB	Power		
92	VDD	Power		
93	PC6	I/O	USART6_TX	COM_TX
94	PC7	I/O	TIM3_CH2	CODG_B
97	PA8 **	I/O	USB_OTG_FS_SOF	
98	PA9 **	I/O	USB_OTG_FS_VBUS	
99	PA10	I/O	USART1_RX	AFFM4_RX
100	PA11 **	I/O	USB_OTG_FS_DM	
101	PA12 **	I/O	USB_OTG_FS_DP	
102	PA13 (JTMS/SWDIO)	I/O		
103	VCAP	Power		
104	VSS	Power		
105	VDDLDO	Power		
106	VDD	Power		
107	PA14 (JTCK/SWCLK)	I/O		
108	PA15 (JTDI)	I/O	UART7_TX	LID_TX
111	PC12	I/O	UART5_TX	ServoAX_DATA
112	PD0 *	I/O	GPIO_Output	ServoAX_RW
113	PD1 *	I/O	GPIO_Input	CeriseG
114	PD2 *	I/O	GPIO_Input	CeriseD
115	PD3 *	I/O	GPIO_Output	Canon
116	PD4 *	I/O	GPIO_Output	ServoRX_RW
117	PD5	I/O	USART2_TX	ServoRX_DATA
118	VSS	Power		
119	VDD	Power		
120	PD6 *	I/O	GPIO_Input	GateauG
121	PD7 *	I/O	GPIO_Input	GateauD
122	PG9	I/O	USART6_RX	COM_RX
124	PG11 **	I/O	ETH_TX_EN	
126	PG13 **	I/O	ETH_TXD0	
128	VSS	Power		
129	VDD	Power		
130	PB3 (JTDO/TRACESWO)	I/O	TIM2_CH2	CODX_B
131	PB4 (NJTRST)	I/O		
133	PB6	I/O	USART1_TX	AFFM4_TX

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
135	BOOT0	Boot		
136	PB8	I/O	UART4_RX	AFFM7_RX
137	PB9	I/O	UART4_TX	AFFM7_TX
139	PE1 *	I/O	GPIO_Output	LEDJ
140	VCAP	Power		
141	VSS	Power		
142	PDR_ON	Reset		
143	VDDLDO	Power		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Nucleo-H745
Project Folder	C:\Users\robot\Desktop\pgm\Robot2024\Nucleo-H745
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	M4-0x400
Minimum Stack Size	M4-0x800

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC3_Init	ADC3
5	MX_TIM1_Init	TIM1
6	MX_TIM2_Init	TIM2
7	MX_TIM3_Init	TIM3
8	MX_TIM4_Init	TIM4
9	MX_TIM6_Init	TIM6
10	MX_TIM8_Init	TIM8
11	MX_TIM13_Init	TIM13

Rank	Function Name	Peripheral Instance Name
12	MX_UART4_Init	UART4
13	MX_UART5_Init	UART5
14	MX_USART2_UART_Init	USART2
15	MX_USART6_UART_Init	USART6
16	MX_FREERTOS_Init	FREERTOS_M7
17	MX_I2C2_Init	I2C2

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	MX_TIM5_Init	TIM5
4	MX_TIM12_Init	TIM12
5	MX_UART7_Init	UART7
6	MX_USART1_UART_Init	USART1
7	MX_FREERTOS_Init	FREERTOS_M4
8	MX_TIM14_Init	TIM14

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745ZITx
Datasheet	DS12923_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

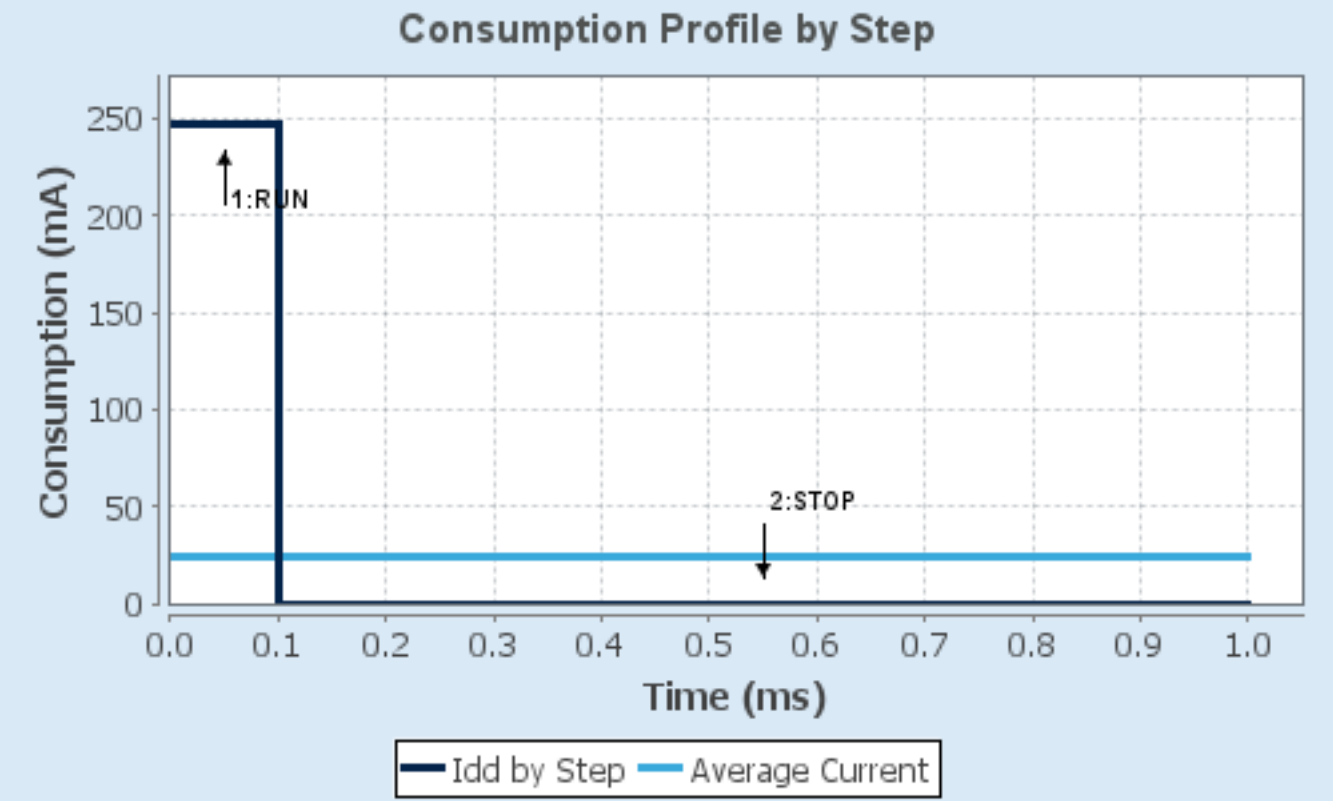
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_IPs_ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
250
200
150
100
50
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC3

mode: IN0

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

mode: IN6

mode: IN7

mode: IN8

IN10: IN10 Single-ended

mode: Temperature Sensor Channel

mode: Vrefint Channel

2.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D3

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**4 ***
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 0

Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel Vrefint ***
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Rank	**3 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Rank	**4 ***
Channel	**Channel 1 ***
Sampling Time	**64.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.2. I2C2

I2C: I2C

2.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0

Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

2.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range

2.4. SYS

Timebase Source: TIM17

2.4.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

2.5. SYS_M4

Timebase Source: TIM15

2.5.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

2.6. TIM1

Clock Source : Internal Clock
Channel1: PWM Generation CH1 CH1N
Channel2: PWM Generation CH2 CH2N
Channel3: PWM Generation CH3 CH3N
Channel4: PWM Generation CH4

2.6.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	**5000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High

CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	**5000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	**5000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.7. TIM2

Combined Channels: Encoder Mode

2.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

2.8. TIM3

Combined Channels: Encoder Mode

2.8.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0xFFFF
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

2.9. TIM4

Combined Channels: Encoder Mode

2.9.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0xFFFF
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

2.10. TIM5

Clock Source : Internal Clock

2.10.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0xFFFFFFFF
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

2.11. TIM6

mode: Activated

2.11.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

2.12. TIM8

Clock Source : Internal Clock

2.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

2.13. TIM12

mode: Clock Source

Channel2: PWM Generation CH2

2.13.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.14. TIM13

mode: Activated

2.14.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

2.15. TIM14

mode: Activated

2.15.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

2.16. UART4

Mode: Asynchronous

2.16.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.17. UART5

Mode: Single Wire (Half-Duplex)

2.17.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	**1000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.18. UART7

Mode: Asynchronous

2.18.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.19. USART1

Mode: Asynchronous

2.19.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4

Power Domain:	D2

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.20. USART2

Mode: Single Wire (Half-Duplex)

2.20.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	**57600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.21. USART6

Mode: Asynchronous

2.21.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.22. FREERTOS_M4

Interface: CMSIS_V1

2.22.1. Config parameters:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemD2Clock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled

QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled
Memory management settings:	
Memory Allocation	**Static ***
Hook function related definitions:	
USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled
Run time and task stats gathering related definitions:	
GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled
Co-routine related definitions:	
USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2
Software timer definitions:	
USE_TIMERS	Disabled
Interrupt nesting behaviour configuration:	
LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5
Added with 10.2.1 support:	
MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

2.22.2. Include parameters:

Core(s) Settings:	
Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2
Include definitions:	
vTaskPrioritySet	Enabled

uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.22.3. Advanced settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

2.23. FREERTOS_M7

Interface: CMSIS_V1

2.23.1. Config parameters:

Core(s) Settings:

Context(s):	Cortex-M7

Initialized Context:	Cortex-M7
Power Domain:	D1

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	**Static ***

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

2.23.2. Include parameters:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.23.3. Advanced settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ADC3	PF6	ADC3_INP8	Analog mode	No pull-up and no pull-down	n/a		Cortex-M7	D3
	PF7	ADC3_INP3	Analog mode	No pull-up and no pull-down	n/a		Cortex-M7	D3
	PF8	ADC3_INP7	Analog mode	No pull-up and no pull-down	n/a		Cortex-M7	D3
	PF9	ADC3_INP2	Analog mode	No pull-up and no pull-down	n/a		Cortex-M7	D3
	PF10	ADC3_INP6	Analog mode	No pull-up and no pull-down	n/a		Cortex-M7	D3
	PC0	ADC3_INP10	Analog mode	No pull-up and no pull-down	n/a		Cortex-M7	D3
	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	VBat	Cortex-M7	D3
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a		Cortex-M7	D3
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	**Pull-up ***	Low		Cortex-M7	D2
	PB11	I2C2_SDA	Alternate Function Open Drain	**Pull-up ***	Low		Cortex-M7	D2
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
TIM1	PB1	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWMX_B	Cortex-M7	D2
	PE8	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWMG_B	Cortex-M7	D2
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWMG_A	Cortex-M7	D2
	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWMD_B	Cortex-M7	D2
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWMD_A	Cortex-M7	D2
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWMX_A	Cortex-M7	D2
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_TURB	Cortex-M7	D2
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODX_A	Cortex-M7	D2
	PB3	TIM2_CH2	Alternate Function	No pull-up and no pull-	Low	CODX_B	Cortex-M7	D2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	(JTDO/TRACESWO		Push Pull	down				
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODG_A	Cortex-M7	D2
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODG_B	Cortex-M7	D2
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODD_A	Cortex-M7	D2
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODD_B	Cortex-M7	D2
TIM12	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_LID	Cortex-M4	D2
UART4	PB8	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	AFFM7_RX	Cortex-M7	D2
	PB9	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	AFFM7_TX	Cortex-M7	D2
UART5	PC12	UART5_TX	Alternate Function Open Drain	**Pull-up ***	**Very High ***	ServoAX_DATA	Cortex-M7	D2
UART7	PE7	UART7_RX	Alternate Function Push Pull	**Pull-up ***	Low	LID_RX	Cortex-M4	D2
	PA15 (JTDI)	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LID_TX	Cortex-M4	D2
USART1	PA10	USART1_RX	Alternate Function Push Pull	**Pull-up ***	Low	AFFM4_RX	Cortex-M4	D2
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	AFFM4_TX	Cortex-M4	D2
USART2	PD5	USART2_TX	Alternate Function Open Drain	**Pull-up ***	**High ***	ServoRX_DATA	Cortex-M7	D2
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM_TX	Cortex-M7	D2
	PG9	USART6_RX	Alternate Function Push Pull	**Pull-up ***	Low	COM_RX	Cortex-M7	D2
Single Mapped Signals	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a			
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a			
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a			
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low			

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX		
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_TX		
	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PA9	USB_OTG_FS_VBUS	n/a	n/a	n/a			
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low			
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PompeA	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PompeB	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTTON	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDV	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PF11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TopX	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PowPompe	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PF15	GPIO_Input	Input mode	**Pull-down ***	n/a	TIRETTE	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	POWENX	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN_TURB	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-	Low	POWEN	Cortex-M7*	Cortex-M7*

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
				down			Cortex-M4	Cortex-M4
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDR	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS_PWR_EN	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PG7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_FS_OVCR	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ServoAX_RW	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CeriseG	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CeriseD	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Canon	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	ServoRX_RW	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	GateauG	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	GateauD	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDJ	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4

* Initialized context

3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC3	DMA1_Stream0	Peripheral To Memory	Low

ADC3: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
USART2 global interrupt	true	4	0
TIM8 update interrupt and TIM13 global interrupt	true	10	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	5	0
UART4 global interrupt	true	6	0
UART5 global interrupt	true	3	0
USART6 global interrupt	true	11	0
TIM17 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
CM4 send event interrupt for CM7	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
ADC3 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream0 global interrupt	false	true	true
USART2 global interrupt	false	true	true
TIM8 update interrupt and TIM13 global interrupt	false	true	true
TIM8 trigger and commutation interrupts and TIM14 global interrupt	false	true	true
UART4 global interrupt	false	true	true
UART5 global interrupt	false	true	true
USART6 global interrupt	false	true	true
TIM17 global interrupt	false	true	true

3.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
USART1 global interrupt	true	11	0
TIM8 trigger and commutation interrupts and	true	12	0

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM14 global interrupt			
UART7 global interrupt	true	3	0
TIM15 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM5 global interrupt	unused		
CM7 send event interrupt for CM4	unused		
FPU global interrupt	unused		
HSEM2 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.4. NVIC2 Code generation

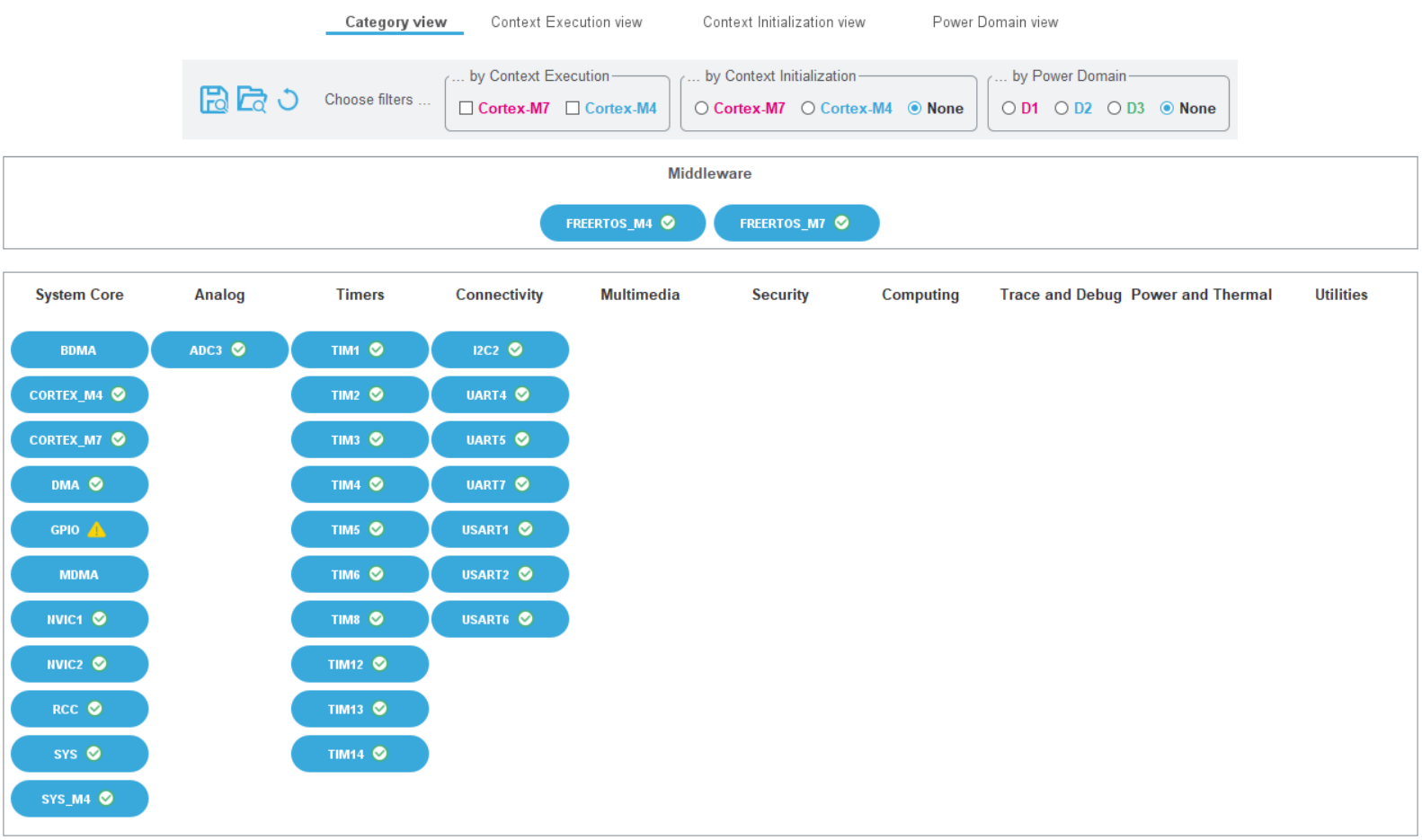
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
USART1 global interrupt	false	true	true
TIM8 trigger and commutation interrupts and TIM14 global interrupt	false	true	true
UART7 global interrupt	false	true	true
TIM15 global interrupt	false	true	true

*** User modified value**

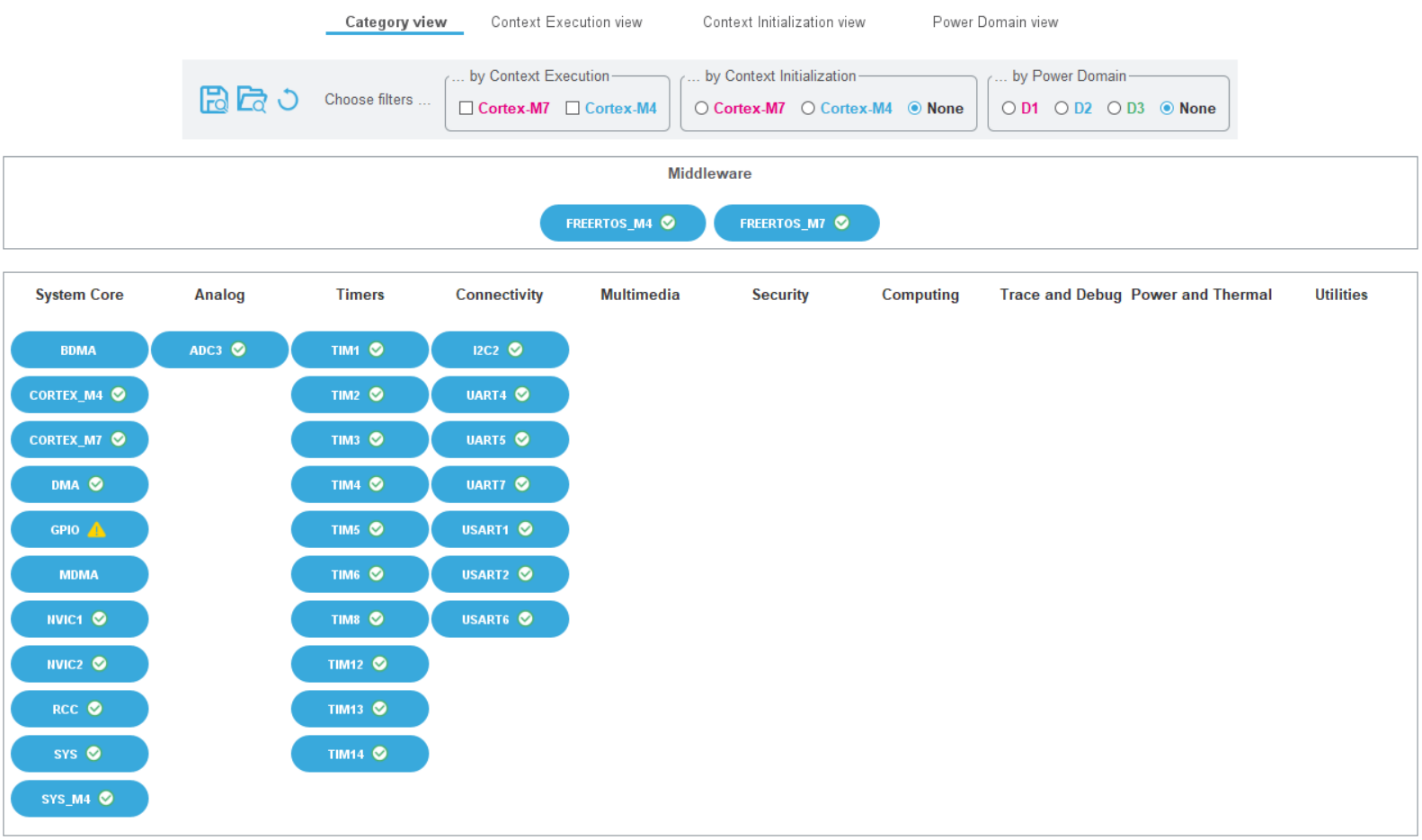
4. System Views

4.1. Category view

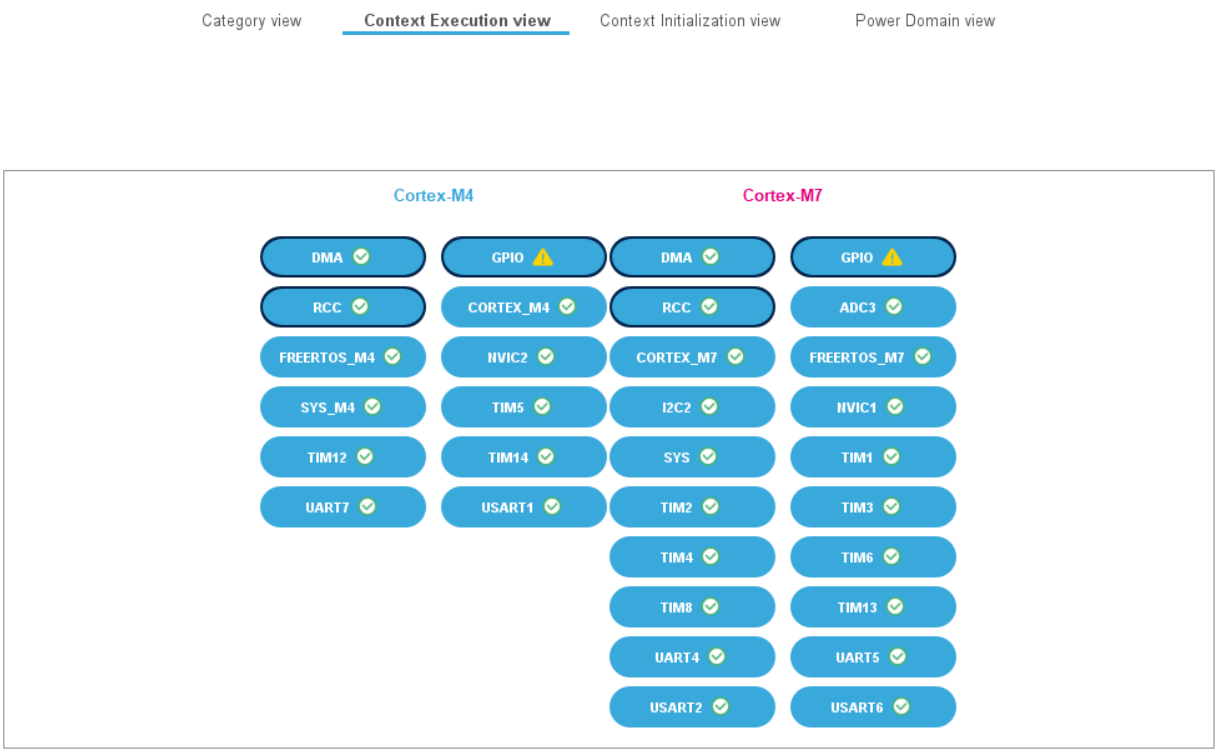
4.1.1. Current



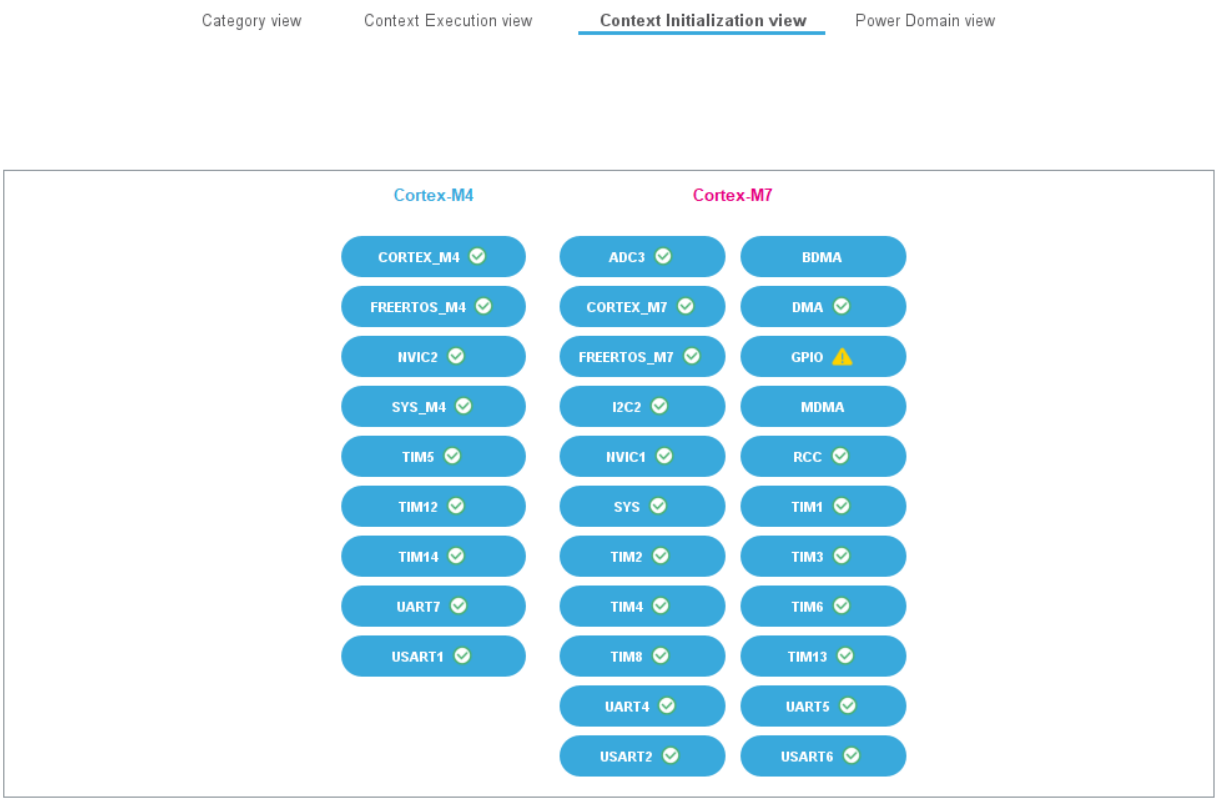
4.1.2. Without filters



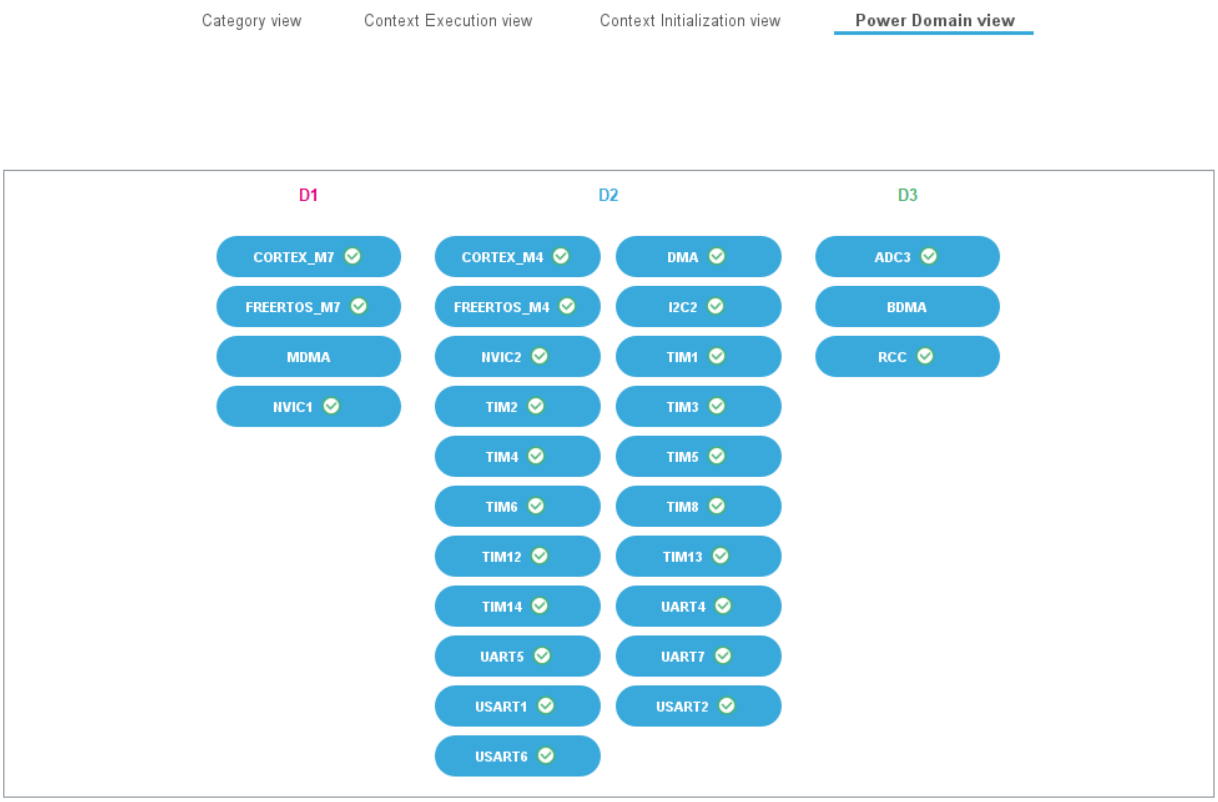
4.2. Context Execution view



4.3. Context Initialization view



4.4. Power Domain view



5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7vl.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an2834-how-to-get-the-best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4938-getting-started-with-stm32h74xig-and-stm32h75xig-hardware-development-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4996-hardware-jpeg-codec-peripheral-in-stm32f7677xxx-and-stm32h743534555475750a3b3b0xx-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5020-digital-camera-interface-dcmi-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5033-stm32cube-

	mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-thermal-management-guidelines-for-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5200-getting-started-with-stm32h7-series-sdmmc-host-controller-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5224-stm32-dmamux-the-dma-request-router-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an5543-enhanced-methods-to-handle-spi-communication-on-stm32-devices-stmicroelectronics.pdf
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	redundancy-check-in-stm32h7-series-flash-memory-interface-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5293-migration-guide-from-stm32f7-series-to-stmh74x75x-stm32h72x73x-and-stmh7a37bx-devices-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5156-introduction-to-stm32-microcontrollers-security-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4838-introduction-to-memory-protection-unit-management-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5348-introduction-to-fdcan-peripherals-for-stm32-product-classes-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4230-random-number-generation-validation-using-nist-statistical-test-suite-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5342--error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1202_freertos_guide-freertos-guide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1602_semihosting_in_truestudio-how-to-do-semihosting-in-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1801_stm32cubeprogrammer_in_truestudio-installing-stm32cubeprogrammer-in-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/atollic_editing_keyboard_shortcuts-atollic-editing-keyboard-shortcuts-stmicroelectronics.pdf
Application Notes for related Tools	https://www.st.com/resource/en/application_note/iar_to_atollic_truestudio_migration_guide-truestudio-for-arm-migration-guide-iar-embedded-

& Software	workbench-to-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/stm32cubemx_installation_in_truestudio-stm32cubemx-installation-in-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4323-getting-started-with-stemwin-library-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4435-guidelines-for-obtaining-ulcsaiec-607301603351-class-b-certification-in-any-stm32-application-stmicroelectronics.pdf
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Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4657-stm32-inapplication-programming-iap-using-the-usart-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4841-digital-signal-processing-for-stm32-microcontrollers-using-cmsis-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4891-stm32h72x-stm32h73x-and-singlecore-stm32h74x75x-system-architecture-and-performance-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5001-stm32cube-expansion-package-for-stm32h7-series-mdma-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5014-stm32h7x3-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf

Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5054-secure-programming-using-stm32cubeprogrammer-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5056-integration-guide-for-the-xcubesbsfu-stm32cube-expansion-package-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5360-getting-started-with-projects-based-on-the-stm32mp1-series-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5361-getting-started-with-projects-based-on-dualcore-stm32h7-microcontrollers-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5394-getting-started-with-projects-based-on-the-stm32l5-series-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5418-how-to-build-a-simple-usbpd-sink-application-with-stm32cubemx-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5426-migrating-graphics-middleware-projects-from-stm32cubemx-540-to-stm32cubemx-550-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5534-stm32h735gdk-firmware-upgrade-for-atbased-emw3080-wifi-module-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5564-getting-started-with-projects-based-on-dualcore-stm32wl-microcontrollers-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4865-lowpower-timer-lptim-applicative-use-cases-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5698-adapting-the-

for related Tools & Software	xcubestl-functional-safety-package-for-stm32-iec-61508-compliant-to-other-safety-standards-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5731-stm32cubemx-and-stm32cubeide-threadsafe-solution-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5450-stm32h7a37b3-lines-and-stm32h7b0-value-line-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4502-stm32-smbuspmbus-expansion-package-for-stm32cube-stmicroelectronics.pdf
Design Notes & Tips	https://www.st.com/resource/en/design_tip/dt0117-microphone-array-beamforming-in-the-pcm-and-pdm-domain-stmicroelectronics.pdf
Errata Sheets	https://www.st.com/resource/en/errata_sheet/es0445-stm32h745747xig-and-stm32h755757xi-device-limitations-stmicroelectronics.pdf
Datasheet	https://www.st.com/resource/en/datasheet/dm00600954.pdf
Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0214-stm32-cortexm4-mcus-and-mpus-programming-manual-stmicroelectronics.pdf
Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0253-stm32f7-series-and-stm32h7-series-cortexm7-processor-programming-manual-stmicroelectronics.pdf
Reference Manuals	https://www.st.com/resource/en/reference_manual/rm0399-stm32h745755-and-stm32h747757-advanced-armbased-32bit-mcus-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1163-description-of-wlcsp-for-microcontrollers-and-recommendations-for-its-use-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1204-tape-and-reel-shipping-media-for-stm32-microcontrollers-in-bga-packages-stmicroelectronics.pdf
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