Physical Design of CMOS Integrated Circuits

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References

- John P. Uyemura, “Introduction to VLSI Circuits and Systems,” 2002.
  - Chapter 5

Goal

- Understand how to physically design (manually draw) CMOS integrated circuits (ICs)

Custom Design Flow

Design specification

Schematic design (Transistor-level netlist)

Layout (physical) design

DRC (Design Rule Check)

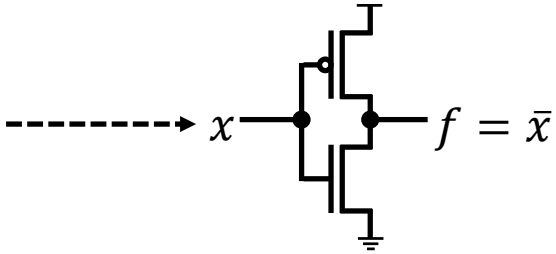
LVS (Layout vs. Schematic)

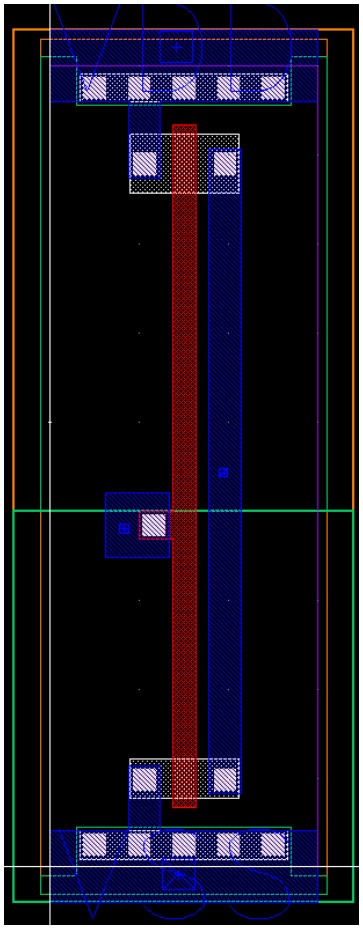
RC extraction

Characterization

Library

An inverter (spec: width, height, ...)



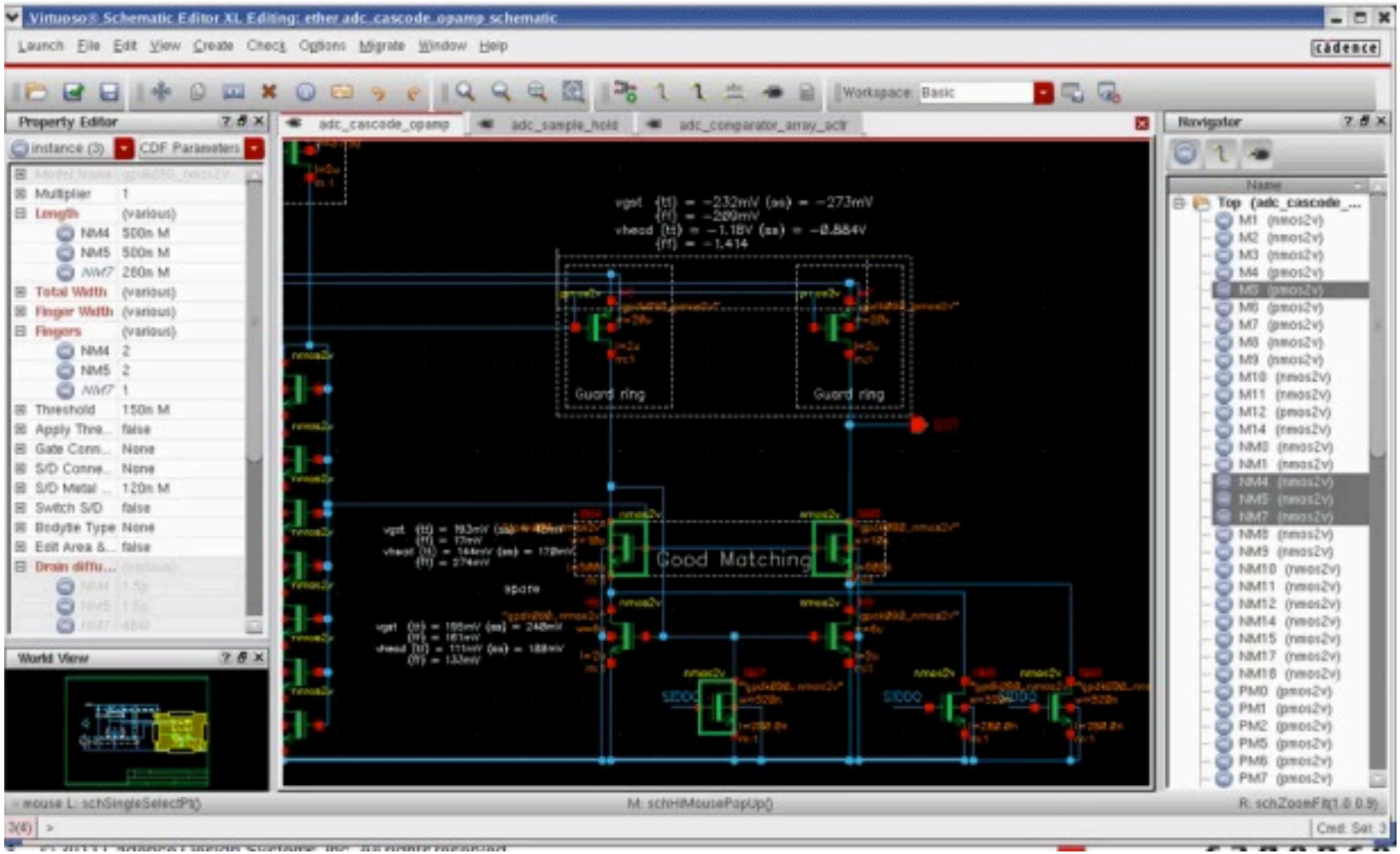


SPICE-level netlist

Timing/power info.

Schematic Editor

- Cadence Virtuoso



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Layout Editor

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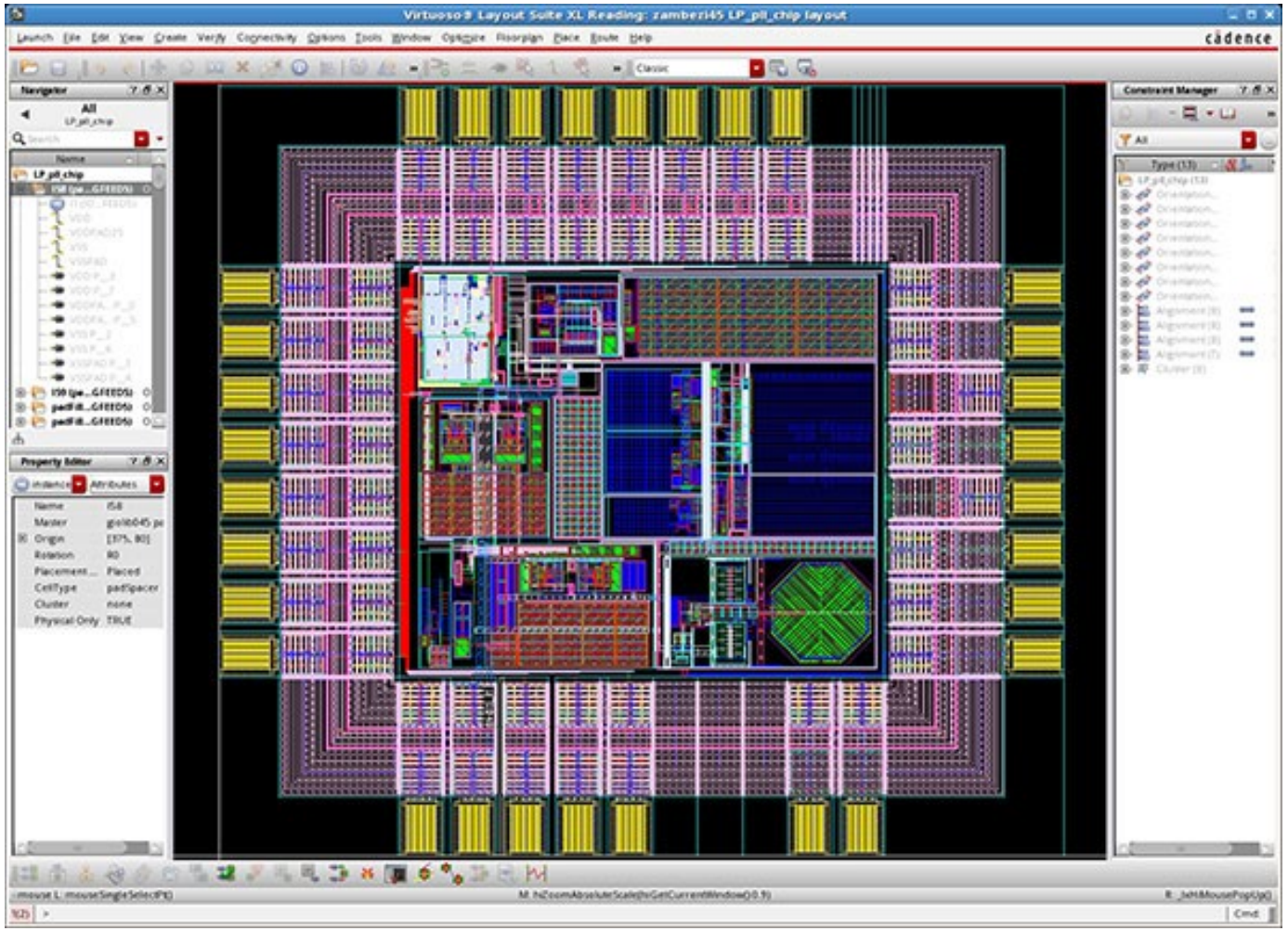

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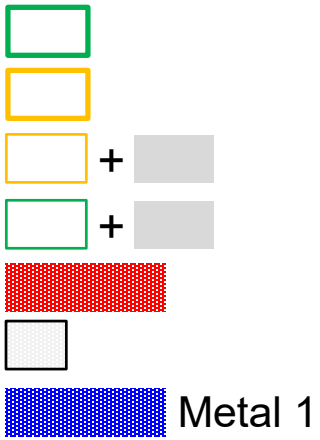
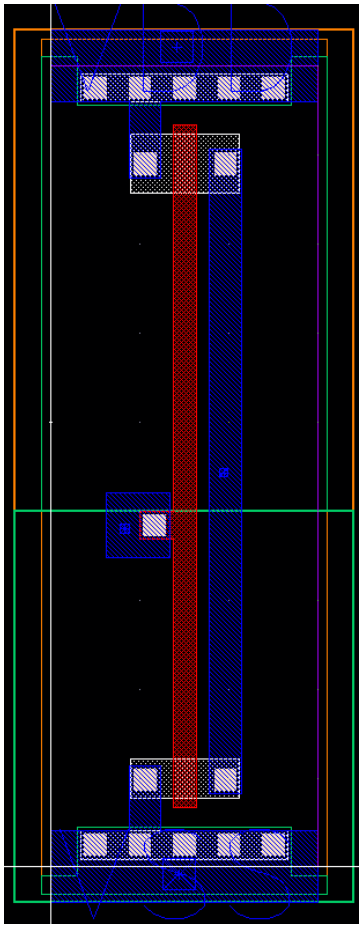
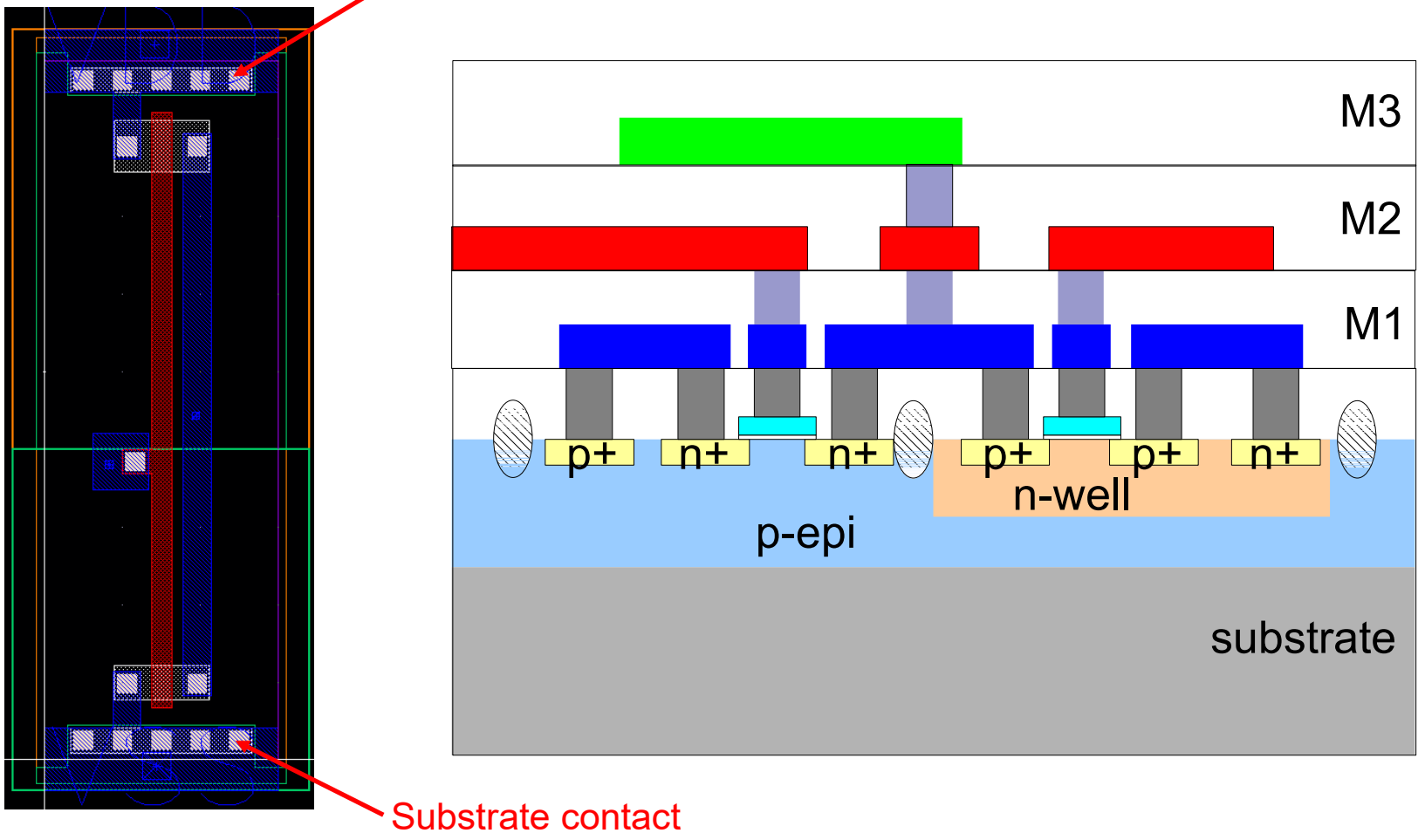
Layout Design

- Draw polygons (rectilinear objects) in each layer
  - Rectangles
  - Paths
- Layers (Real)
  - n-well
  - p-well
  - Active (n+ = ndiff)
  - Active (p+ = pdiff)
  - Poly
  - Contact
  - Metal (m1, m2, m3, ...)
  - Via (v12, v23, v34, ...)
- Layers (Virtual)
  - Cell boundary
  - Labels
  - Pins





Inverter

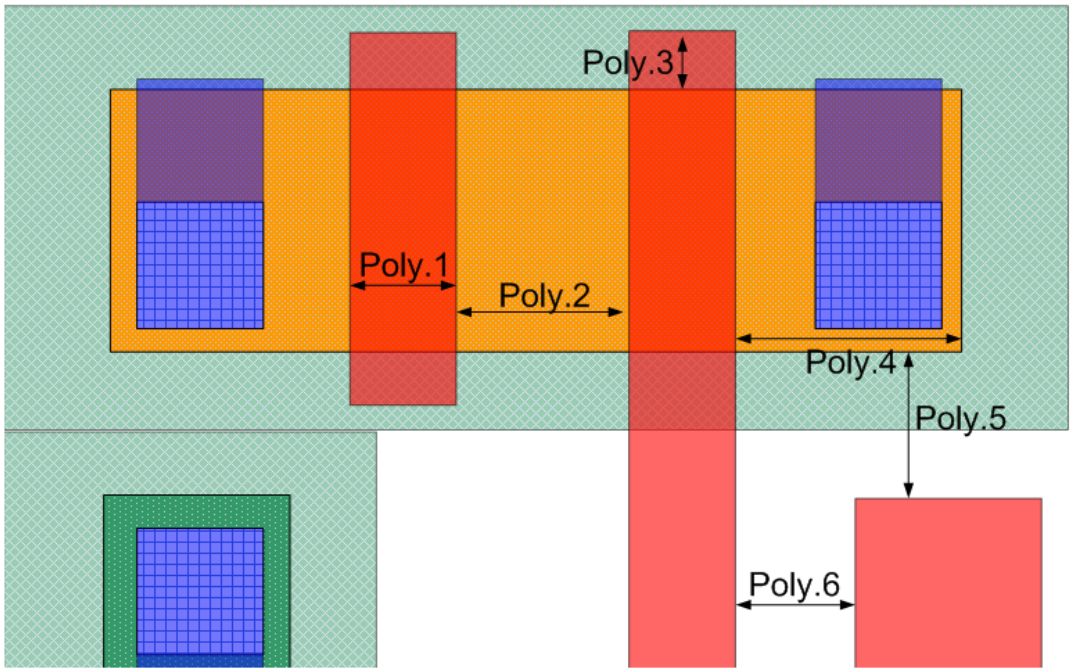

Substrate contact
M3
M2
M1
p+
n+
n+
p+
p+
n+
n-well
p-epi
substrate
Substrate contact

Design Rules
http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

- Poly

FreePDK45:PolyRules

Rule	Value	Description
POLY.1	50 nm	Minimum width of poly
POLY.2	140 nm	Minimum spacing of poly AND active
POLY.3	55 nm	Minimum poly extension beyond active
POLY.4	70 nm	Minimum enclosure of active around gate
POLY.5	50 nm	Minimum spacing of field poly to active
POLY.6	75 nm	Minimum Minimum spacing of field poly

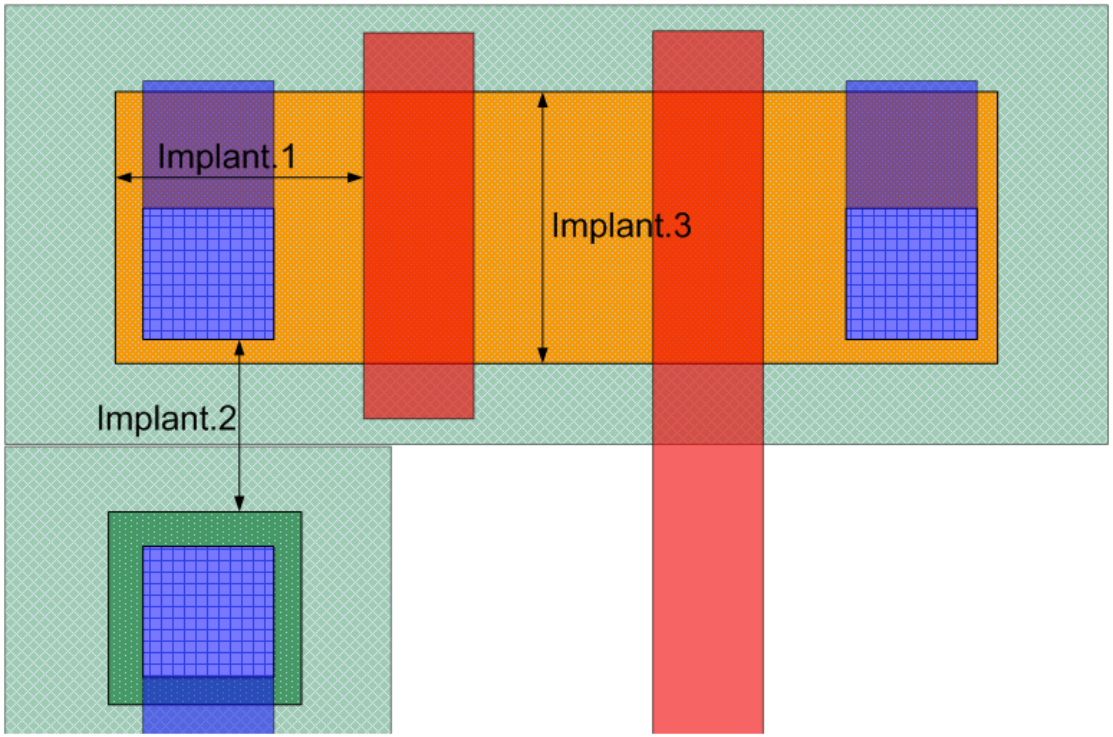


Design Rules
http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

- Implant

FreePDK45:ImplantRules

Rule	Value	Description
IMPLANT.1	70 nm	Minimum spacing of nimplant/ pimplant to channel
IMPLANT.2	25 nm	Minimum spacing of nimplant/ pimplant to contact
IMPLANT.3/4	45 nm	Minimum width/ spacing of nimplant/ pimplant
IMPLANT.5	none	Nimplant and pimplant must not overlap

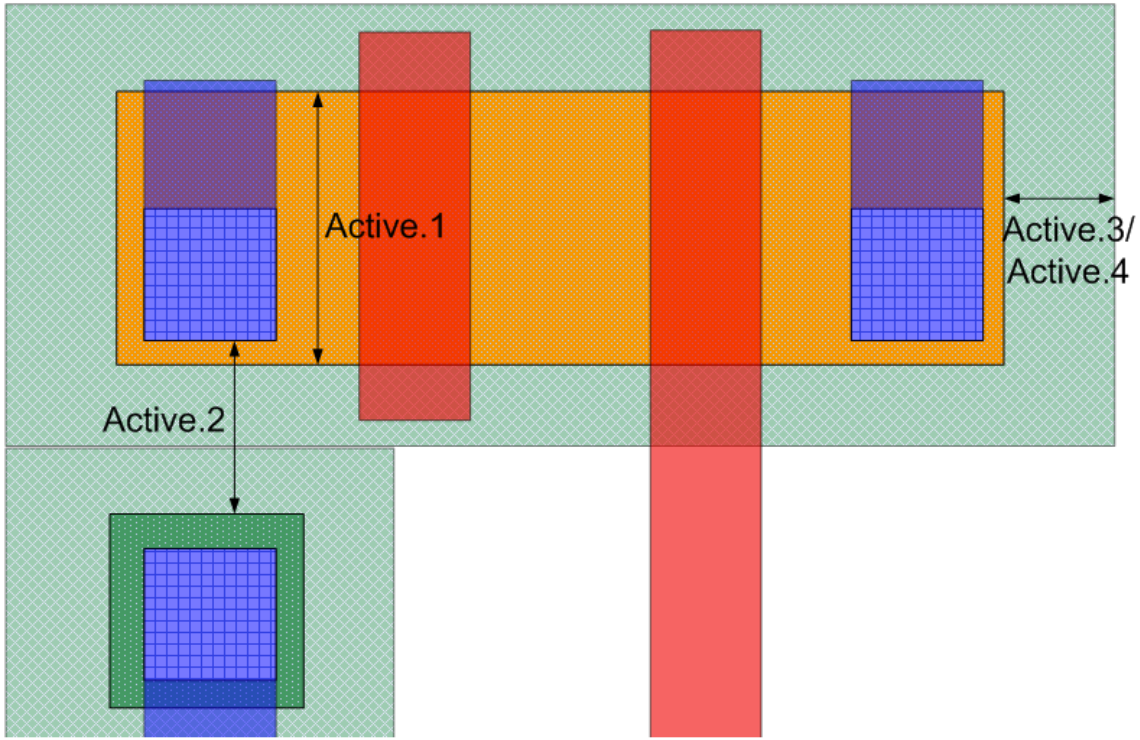


Design Rules
http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

- Active

FreePDK45:ActiveRules

Rule	Value	Description
ACTIVE.1	90 nm	Minimum width of active
ACTIVE.2	80 nm	Minimum spacing of active
ACTIVE.3	55 nm	Minimum enclosure/spacing of nwell/pwell to active
ACTIVE.4	none	saveDerived: active must be inside nwell or pwell

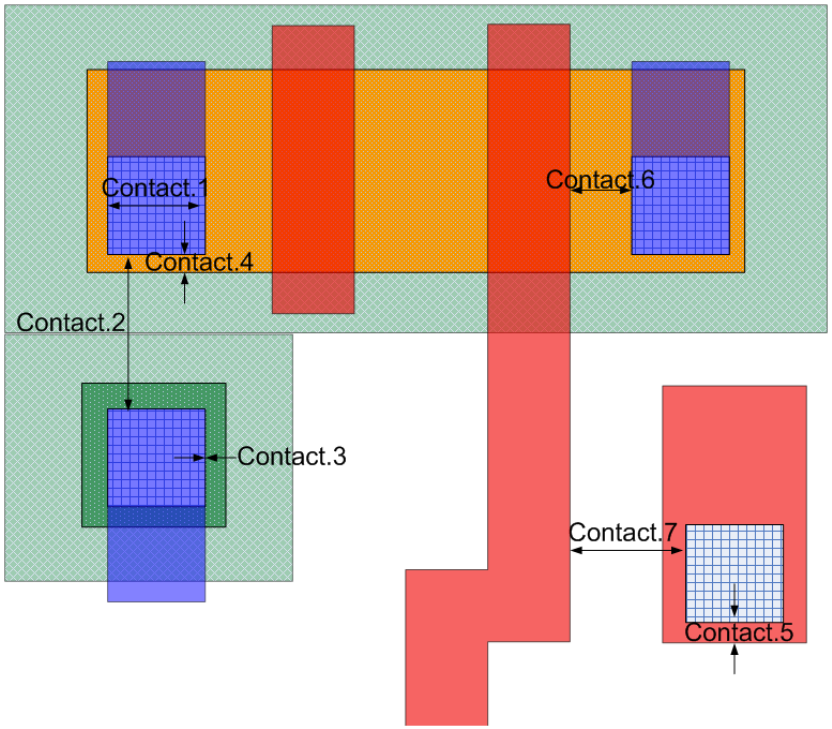


Design Rules
http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

- Contact

FreePDK45:ContactRules

Rule	Value	Description
CONTACT.1	65 nm	Minimum width of contact
CONTACT.2	75 nm	Minimum spacing of contact
CONTACT.3	none	saveDerived: contact must be inside active or poly or metal1
CONTACT.4	5 nm	Minimum enclosure of active around contact
CONTACT.5	5 nm	Minimum enclosure of poly around contact
CONTACT.6	35 nm	Minimum spacing of contact and gate
CONTACT.7	90 nm	Minimum spacing of contact and poly

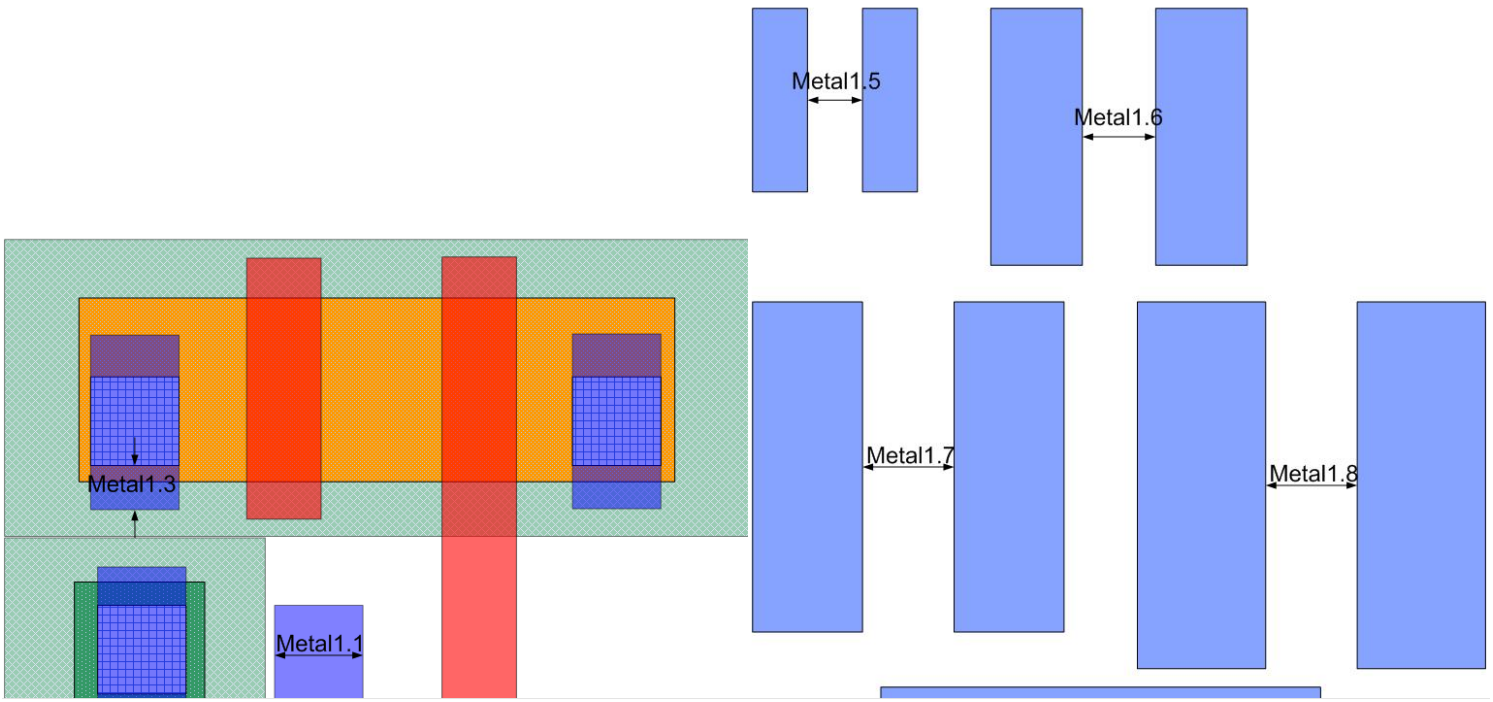


Design Rules
http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

- Metal 1

FreePDK45:Metal1Rules

Rule	Value	Description
METAL1.1	65 nm	Minimum width of metal1
METAL1.2	65 nm	Minimum spacing of metal1
METAL1.3	35 nm	Minimum enclosure around contact on two opposite sides
METAL1.4	35 nm	Minimum enclosure around via1 on two opposite sides
METAL1.5	90 nm	Minimum spacing of metal wider than 90 nm and longer than 900 nm
METAL1.6	270 nm	Minimum spacing of metal wider than 270 nm and longer than 300 nm
METAL1.7	500 nm	Minimum spacing of metal wider than 500 nm and longer than 1.8um
METAL1.8	900 nm	Minimum spacing of metal wider than 900 nm and longer than 2.7 um
METAL1.9	1500 nm	Minimum spacing of metal wider than 1500 nm and longer than 4.0 um



Design Rules
http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

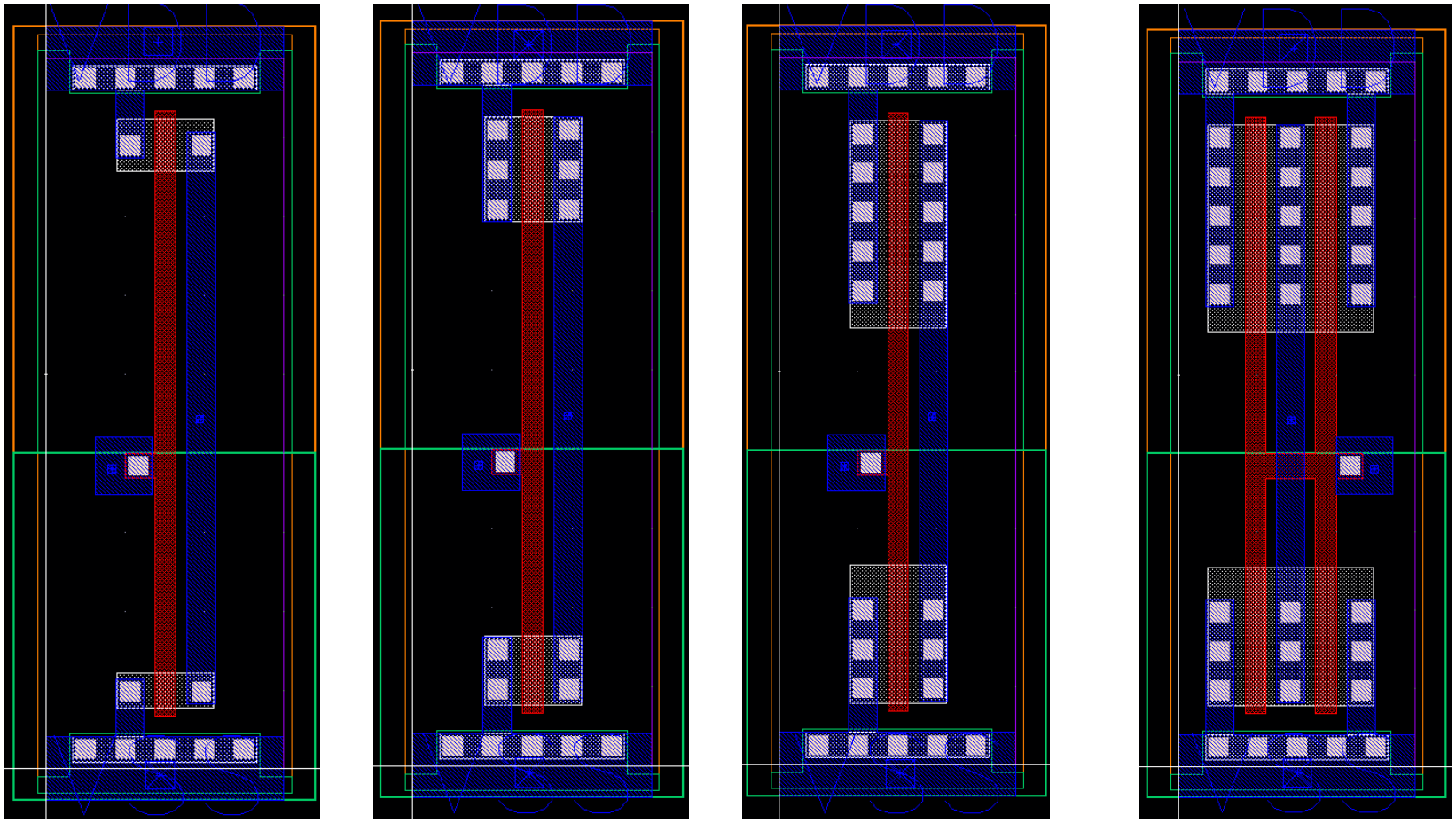
- Via12

FreePDK45:Via1Rules

Rule	Value	Description
VIA1.1	65 nm	Minimum width of via1
VIA1.2	75 nm	Minimum spacing of via1
VIA1.3	none	saveDerived: via1 must be inside metal1
VIA1.4	none	saveDerived: via1 must be inside metal2

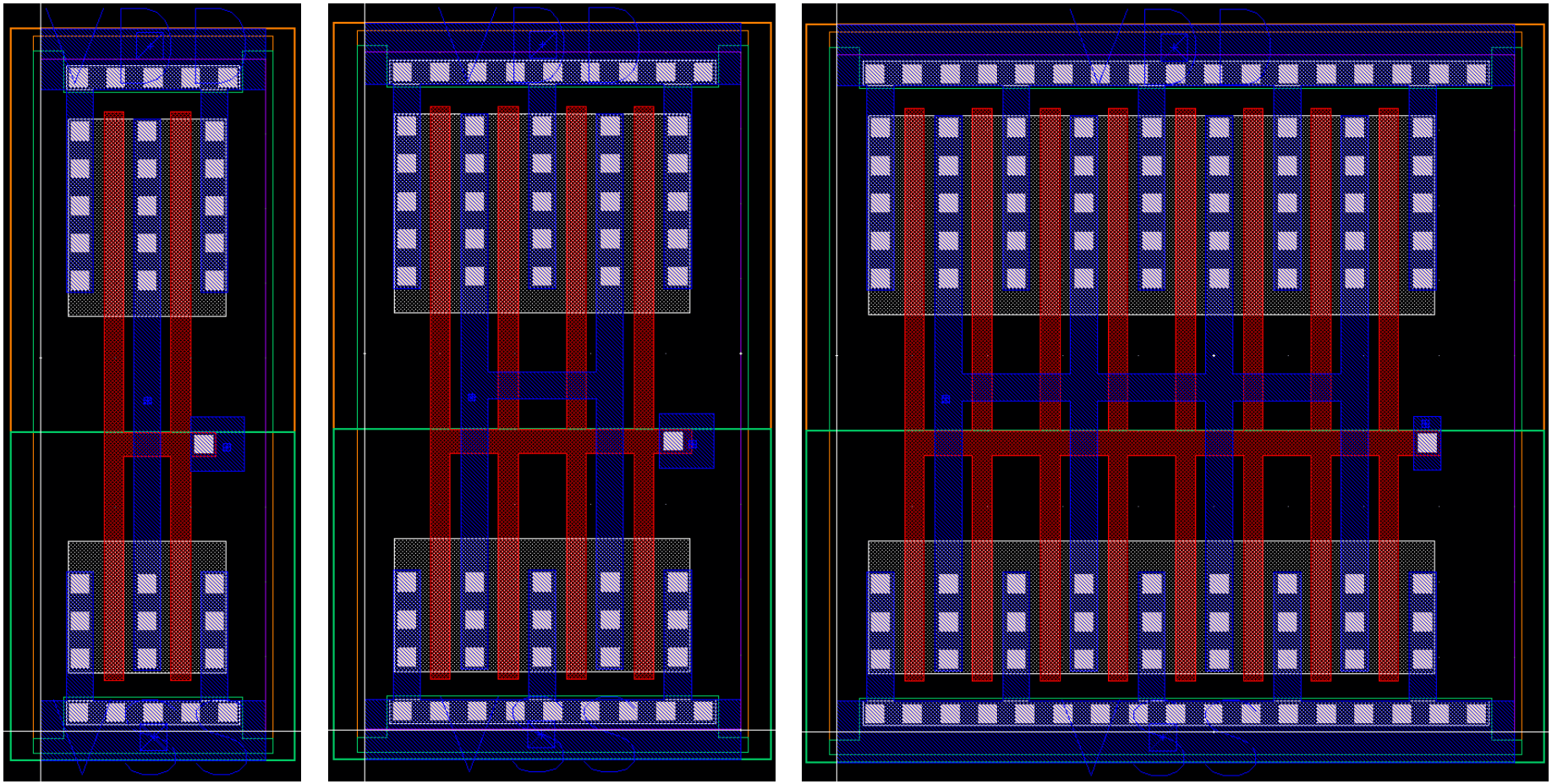
Layouts

- INV_X1, INV_X2, INV_X4, INV_X8



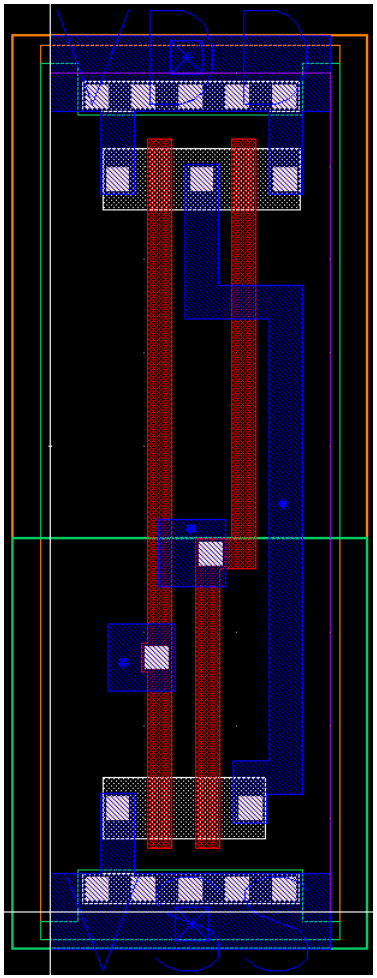
Layouts

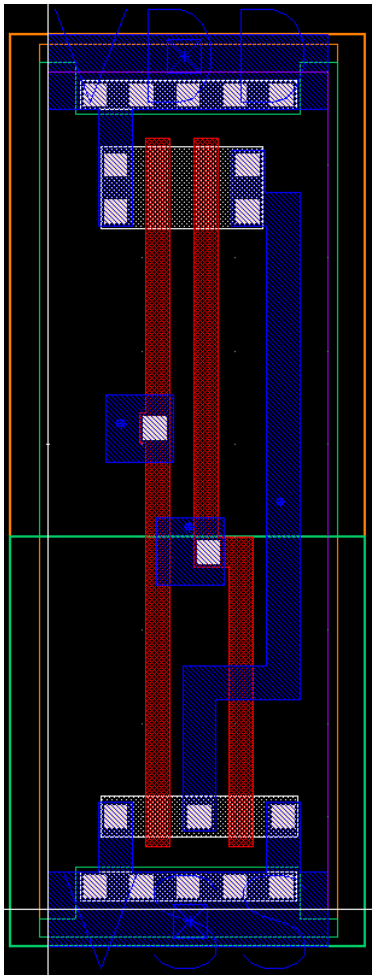
- INV_X8, INV_X16, INV_X32



Layouts

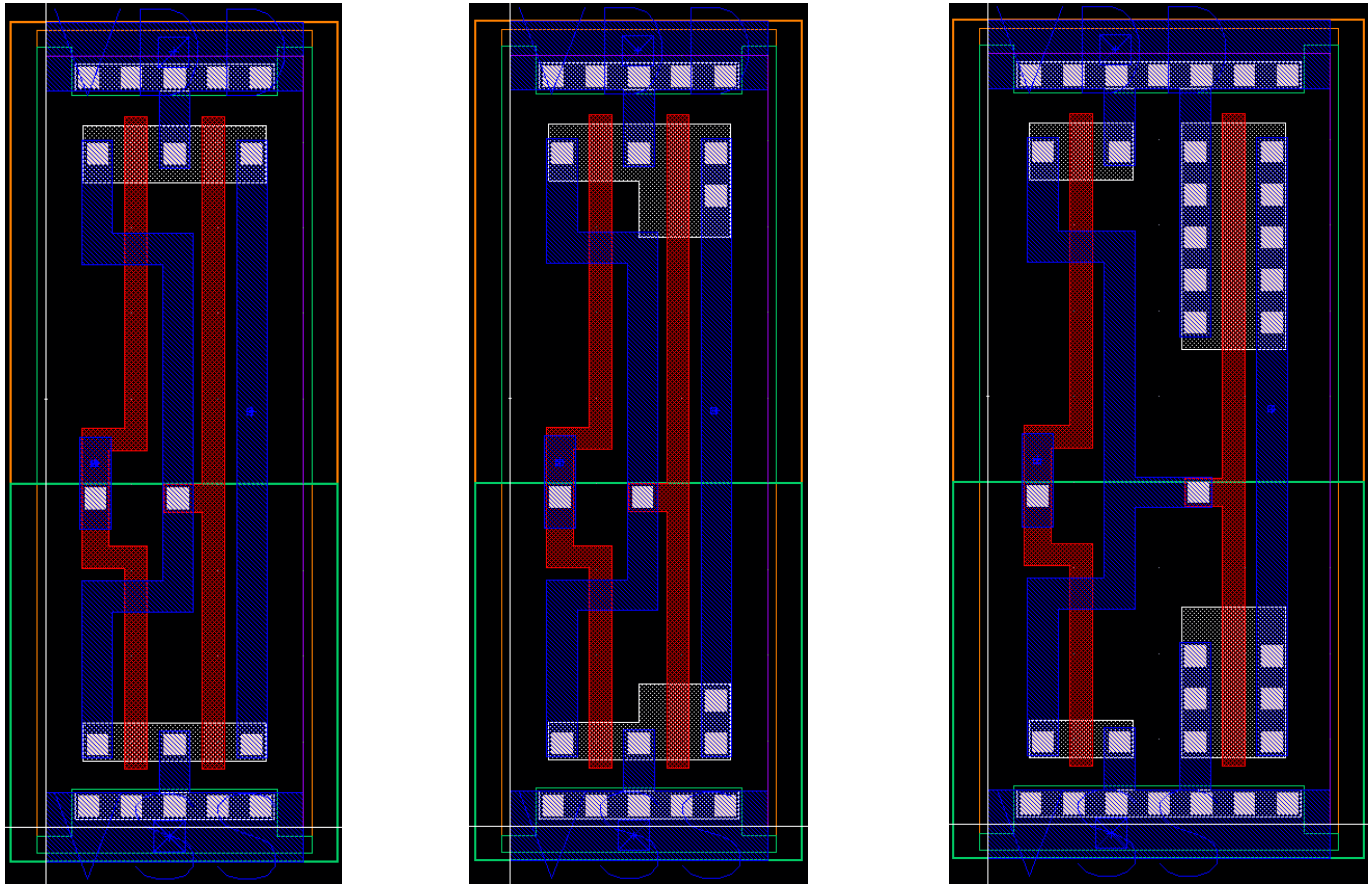
- NAND2_X1, NOR2_X1





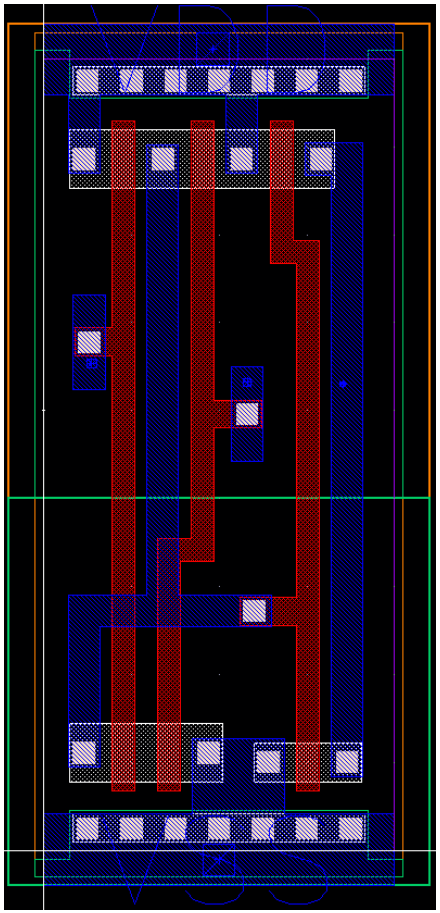
Layouts

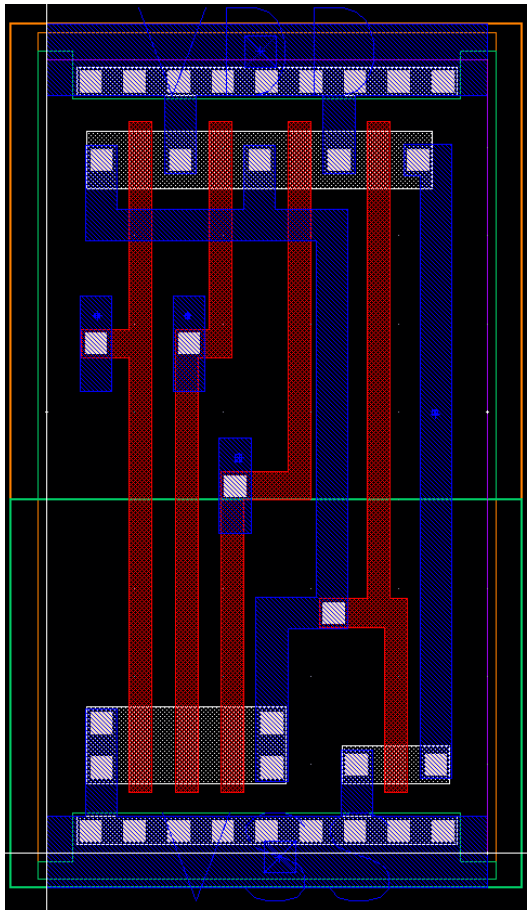
- BUF_X1, BUF_X2, BUF_X4

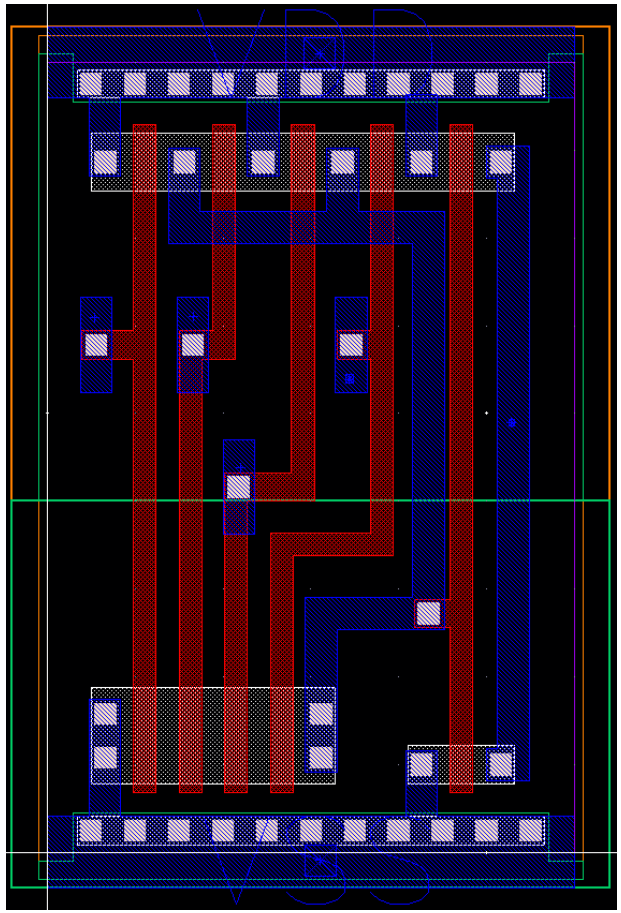


Layouts

- AND2_X1, AND3_X1, AND4_X1

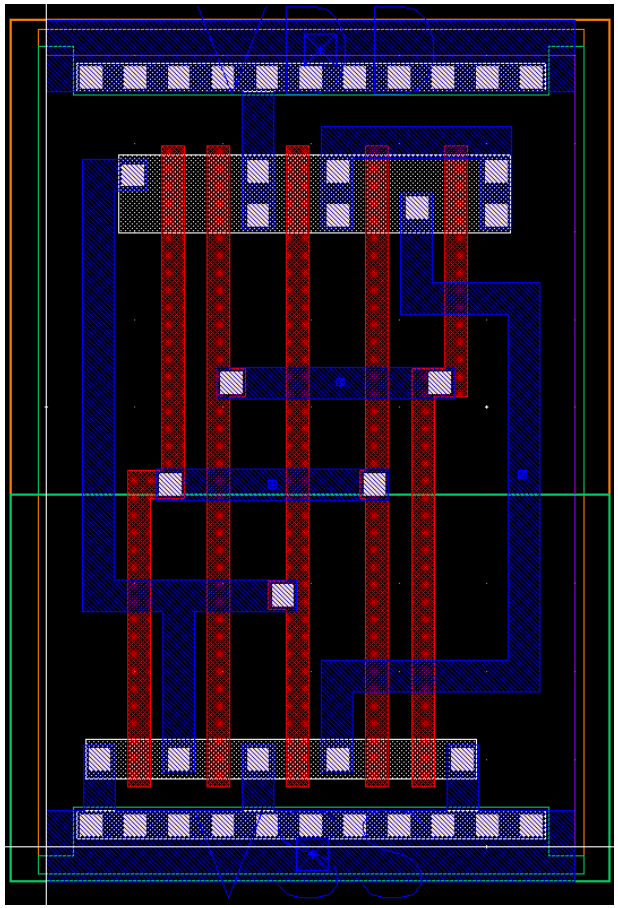


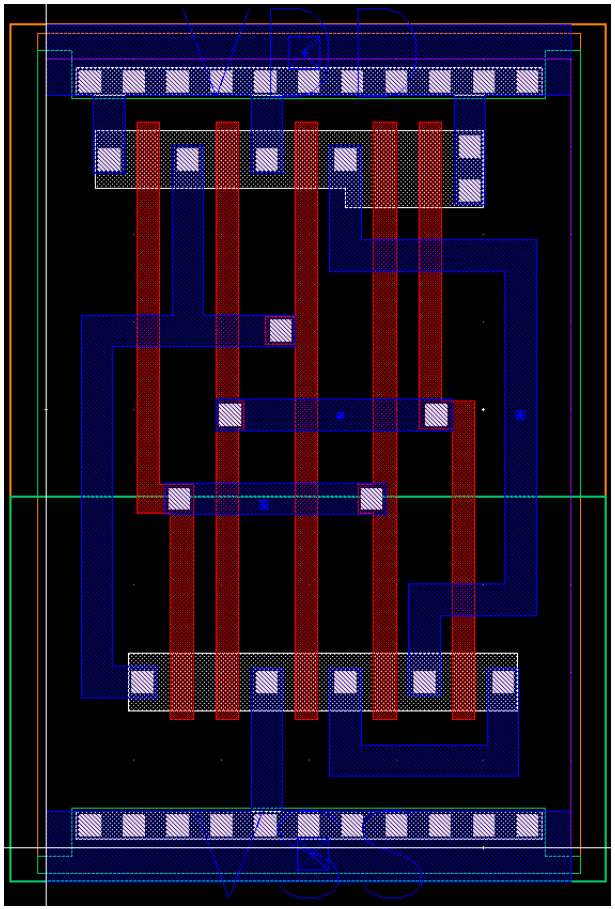




Layouts

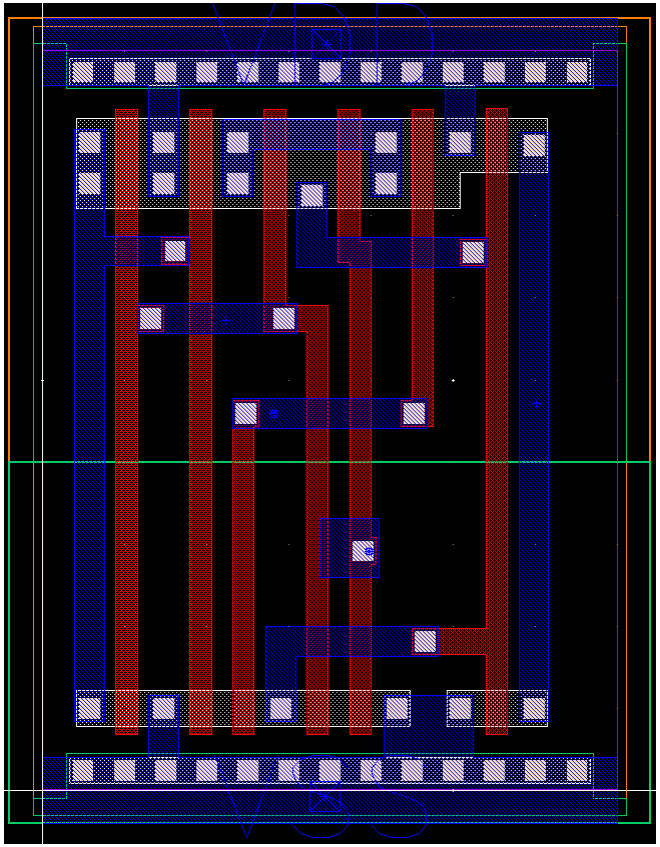
- XOR2_X1, XNOR2_X1





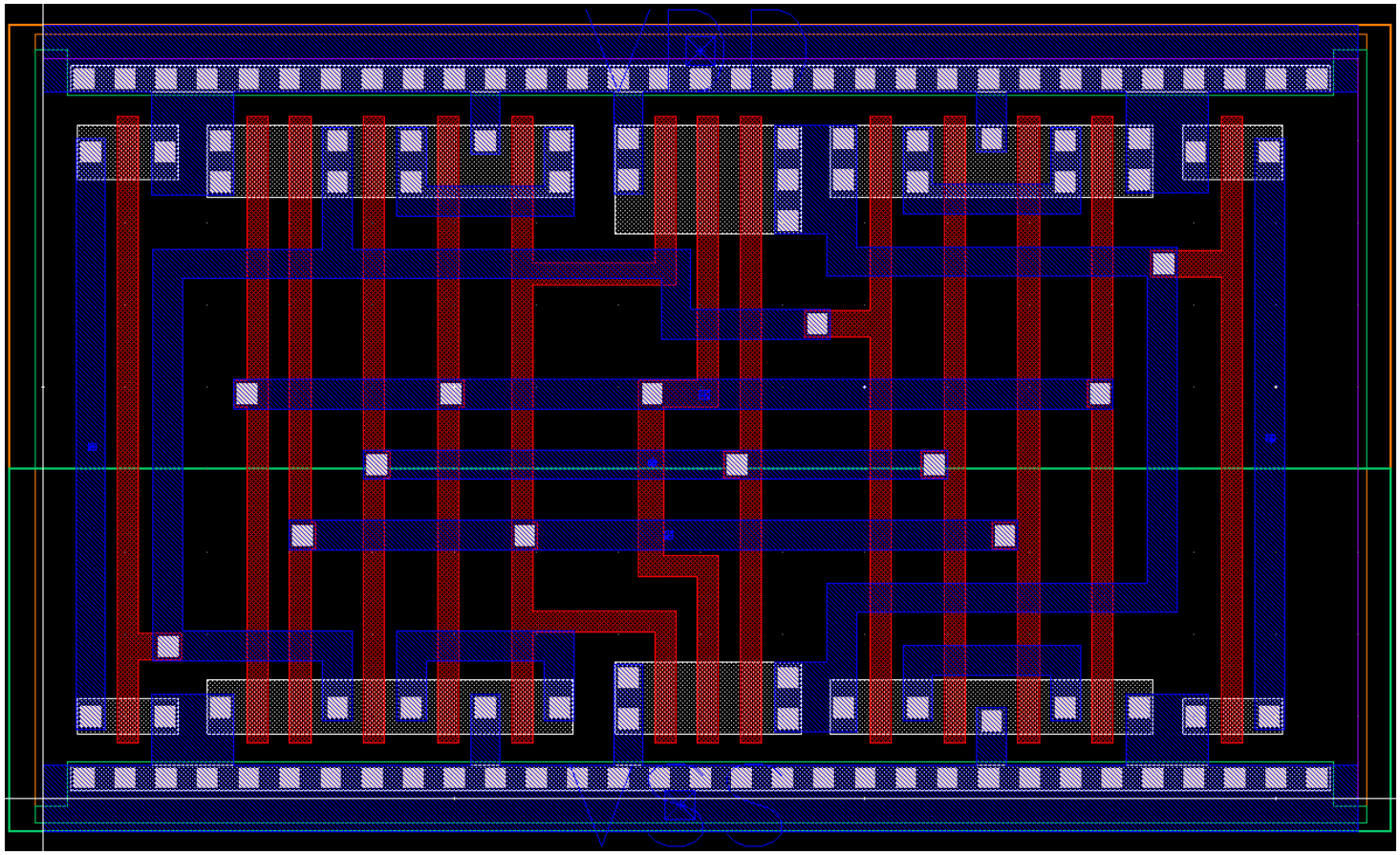
Layouts

- MUX2_X1



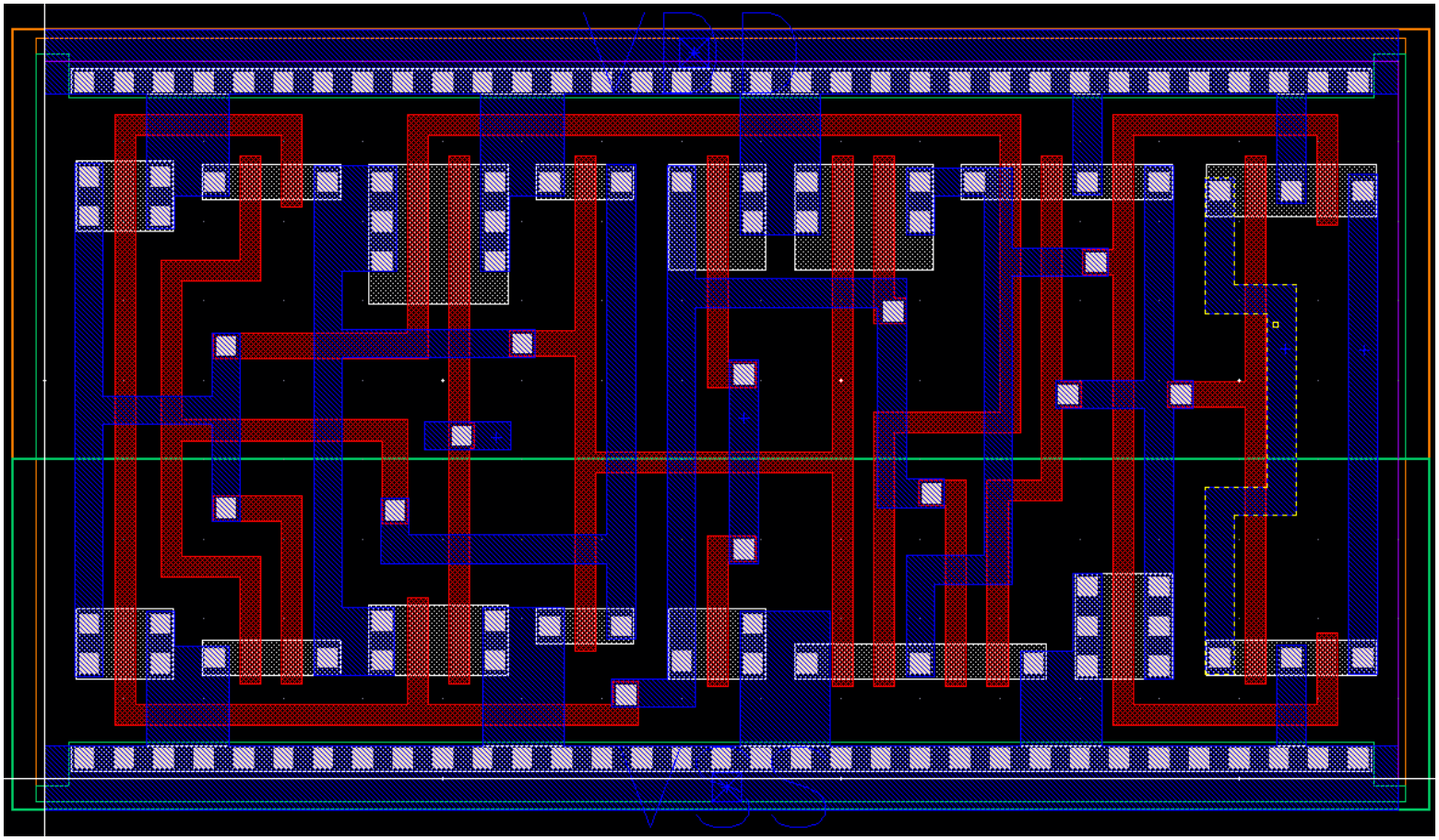
Layouts

- FA_X1 (Full adder)



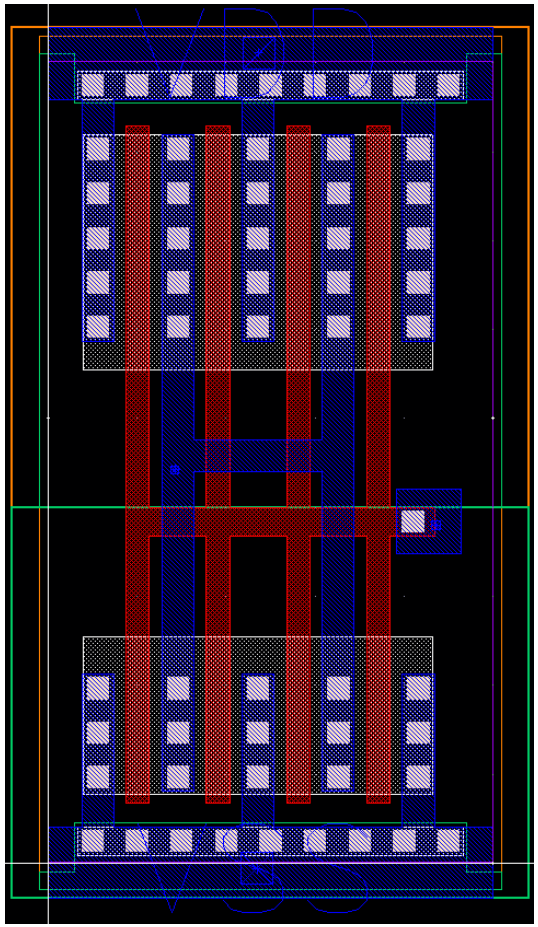
Layouts

- DFF_X1 (D F/F)



Transistor Folding (A Layout Technique)

- INV_X16

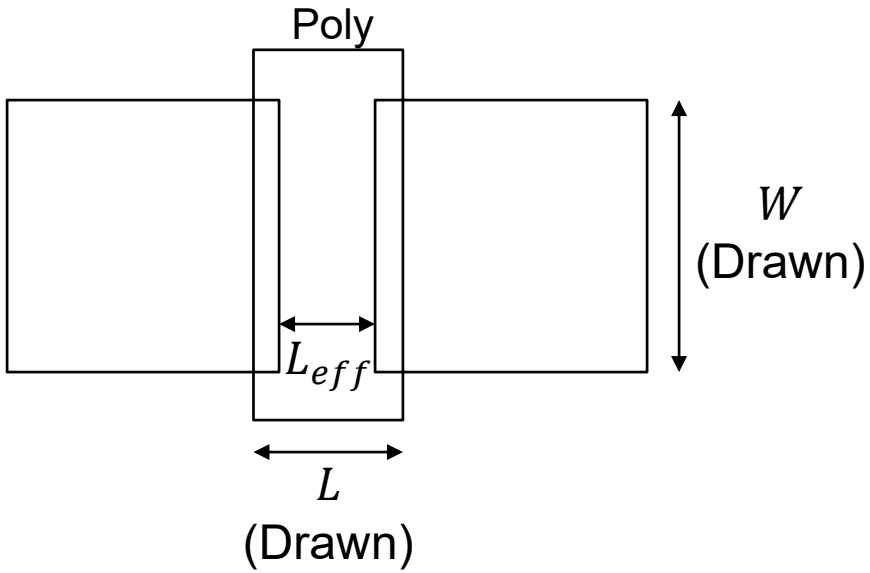


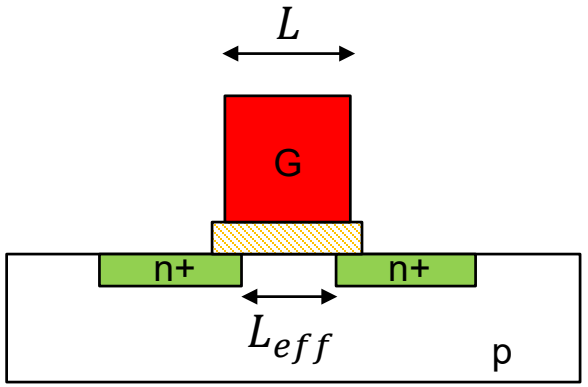
Layout Generation

- Draw a layout.
  - Output: GDSII format
- Design rule check (DRC)
- Prepare a schematic (netlist).
  - A text file
- Layout vs. Schematic (LVS)
  - Layout → netlist 1
  - Schematic → netlist 2
  - LVS checks whether netlist 1 is equal to netlist 2.
- Parasitic RC extraction
  - Output: A SPICE netlist with parasitic RC
- Timing/power simulation and characterization

Channel Length and Width

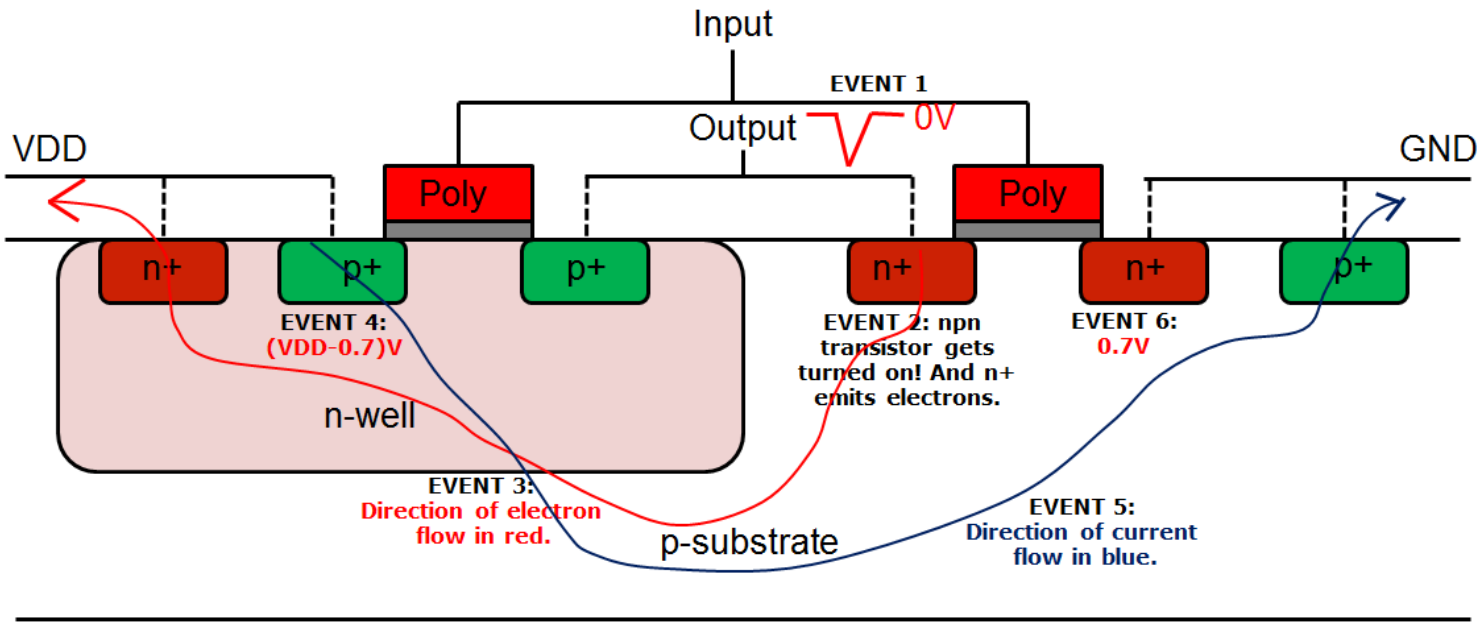
- $L_{eff} = L - \Delta L$
  - L_{eff}: effective channel length
  - L: drawn channel length
- $W_{eff} = W - \Delta W$





Terminologies

- Twin-tub technology
  - Two separate wells are created.
    - n-well for pFETs
    - p-well for nFETs
- Latch-up



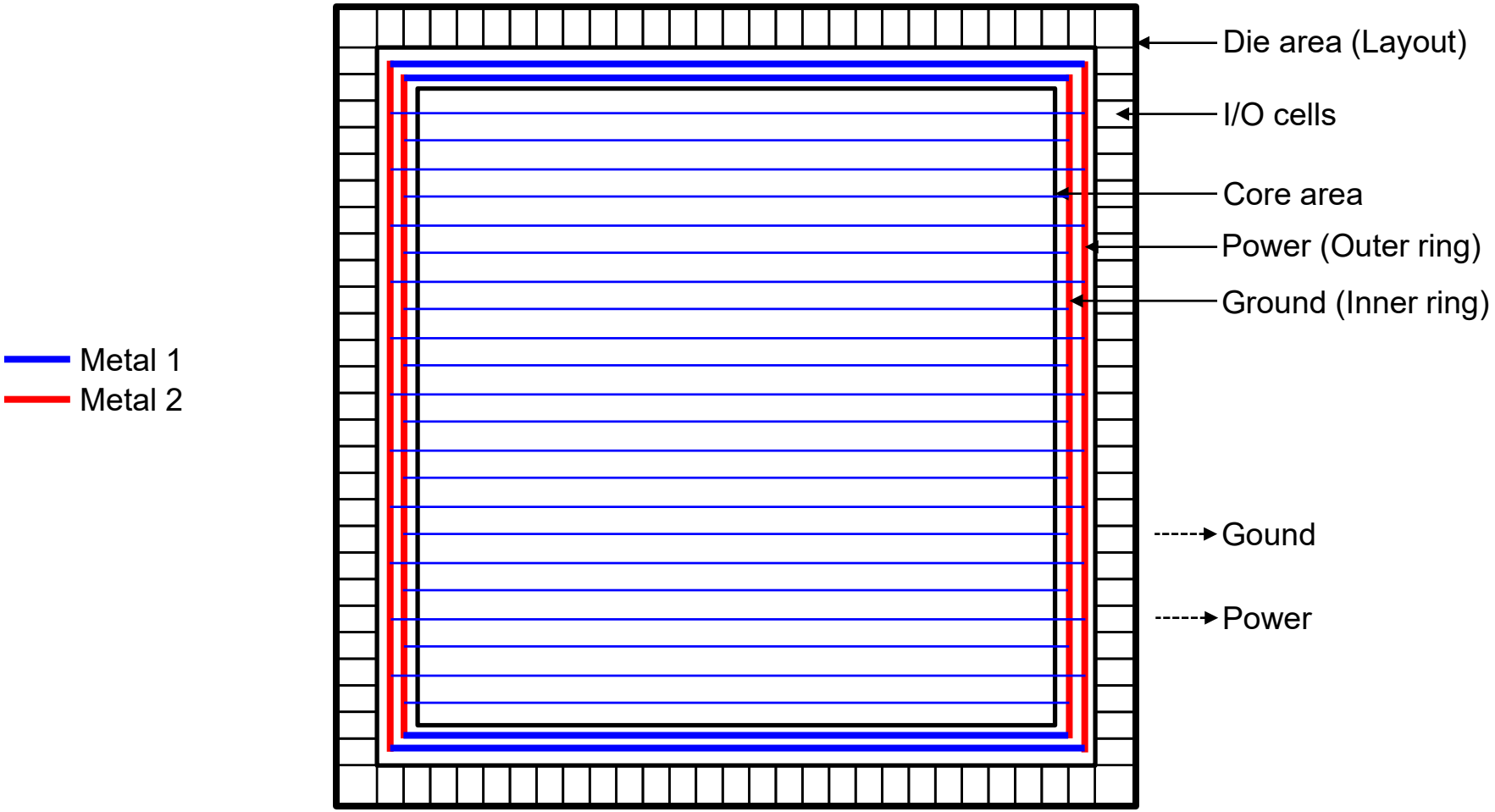
Source: http://vlsi-soc.blogspot.com/2014/10/latch-up-in-cmos.html

Digital VLSI Design

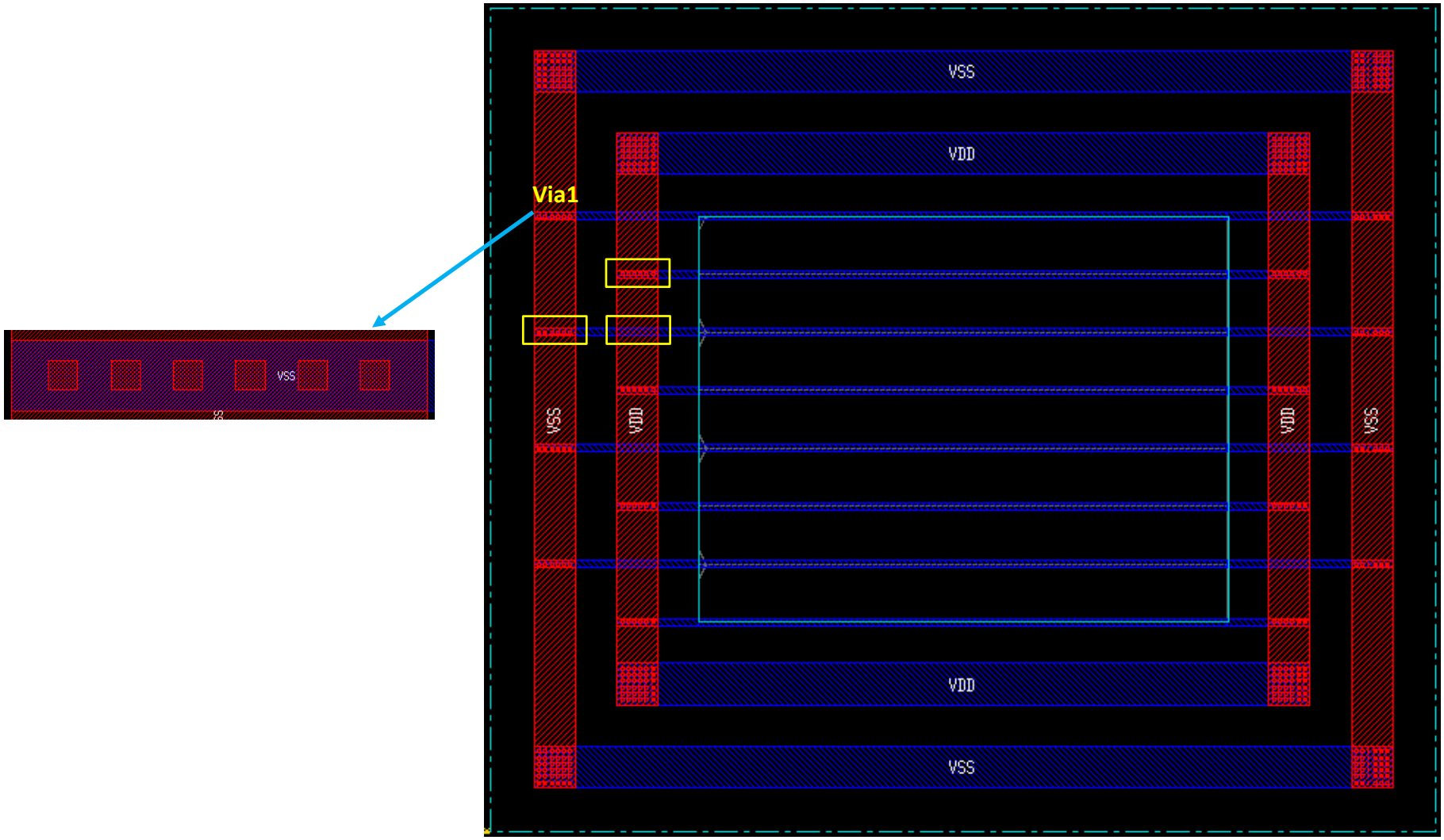
- Placement
  - Places transistors in a layout.
- Routing
  - Power/Ground
    - Connect all the V_{DD} lines to V_{DD}.
    - Connect all the V_{SS} lines to V_{SS}.
    - Reduce IR drop.
  - Clock
    - Connect all the clock sinks to a main clock source pin.
    - Achieve zero skew.
  - Signal

Standard Cell-Based Digital VLSI Design

- Power/Ground routing



Standard Cell-Based Digital VLSI Design



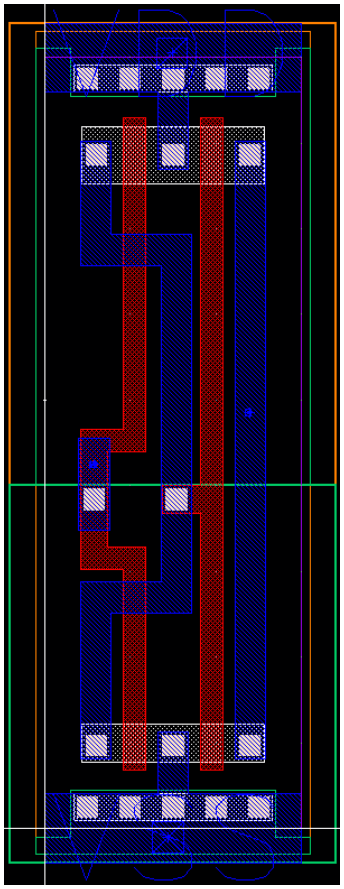
Standard Cell-Based Digital VLSI Design

- Standard cells
  - have a fixed height.
  - have different widths.
  - have ports (input/output pins) generally in the Metal 1 layer.
  - have some obstacles in the Metal 1 layer (for internal routing).

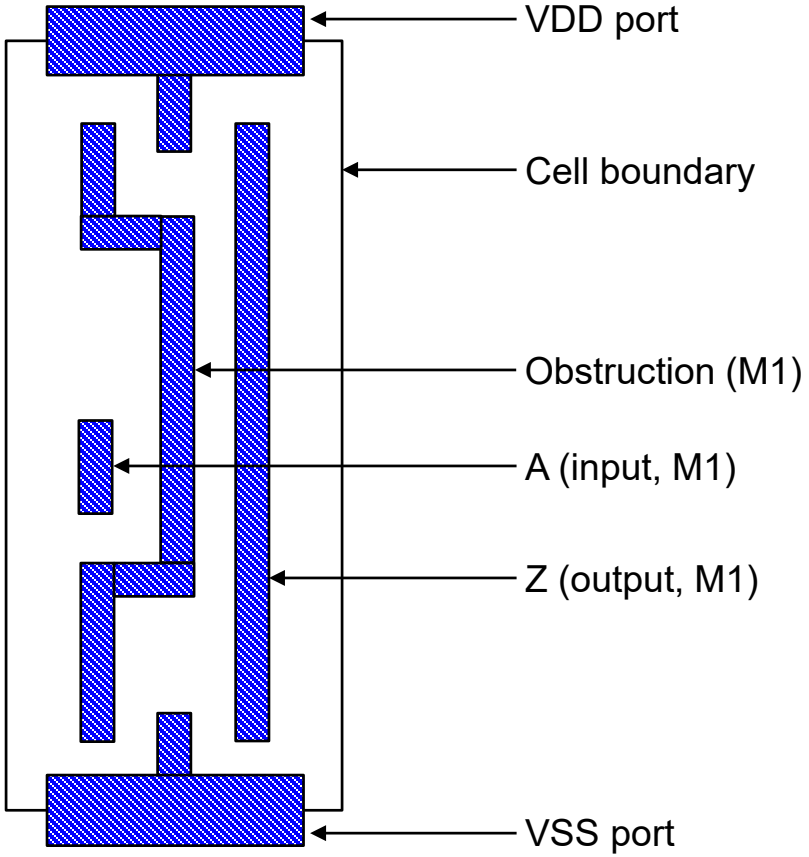
- Routing
  - uses only metal and via layers (doesn't use any other layers).
  - routes the standard cell ports and primary I/O ports based on a given netlist.

Standard Cell-Based Digital VLSI Design

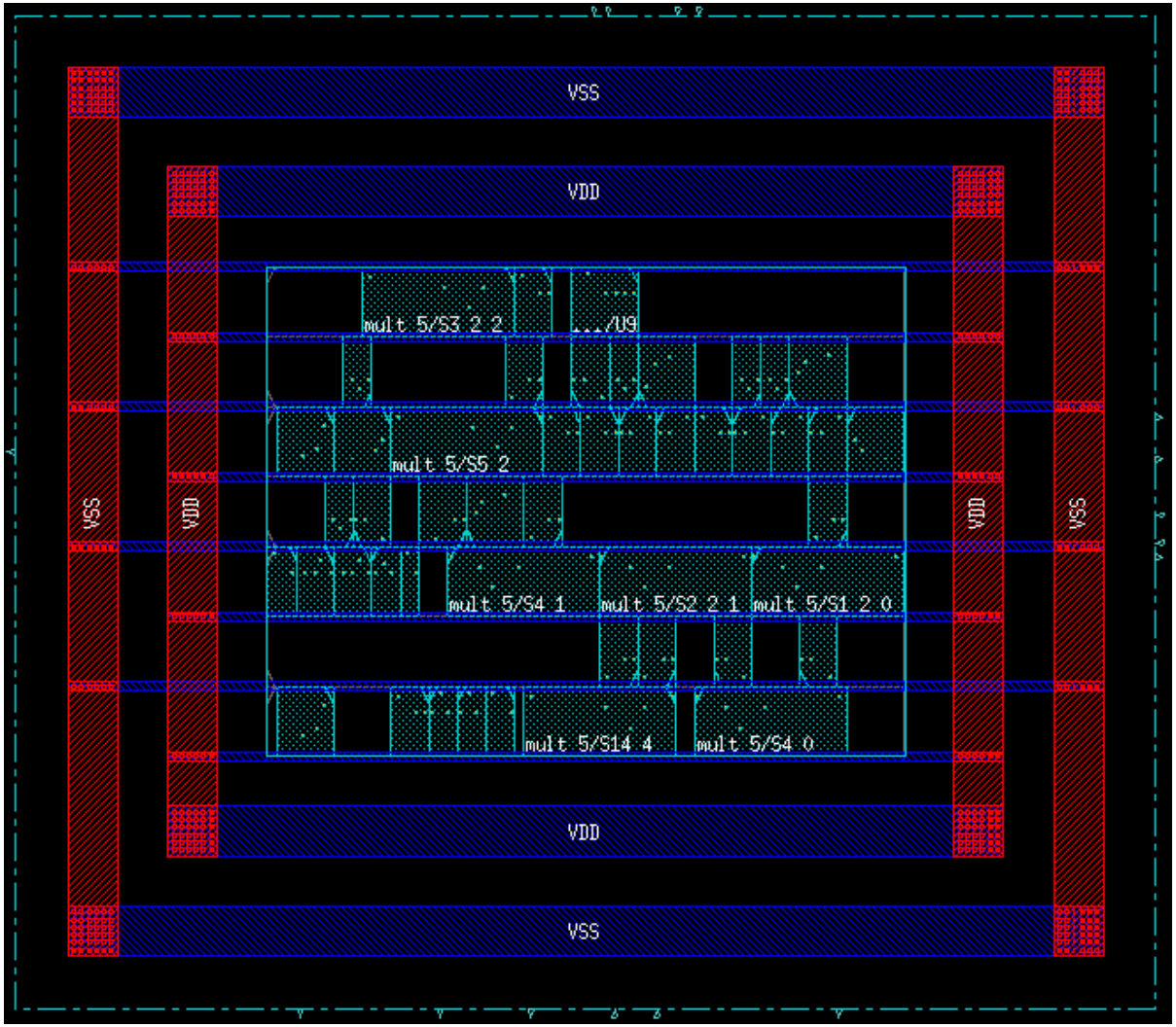
- BUF_X1



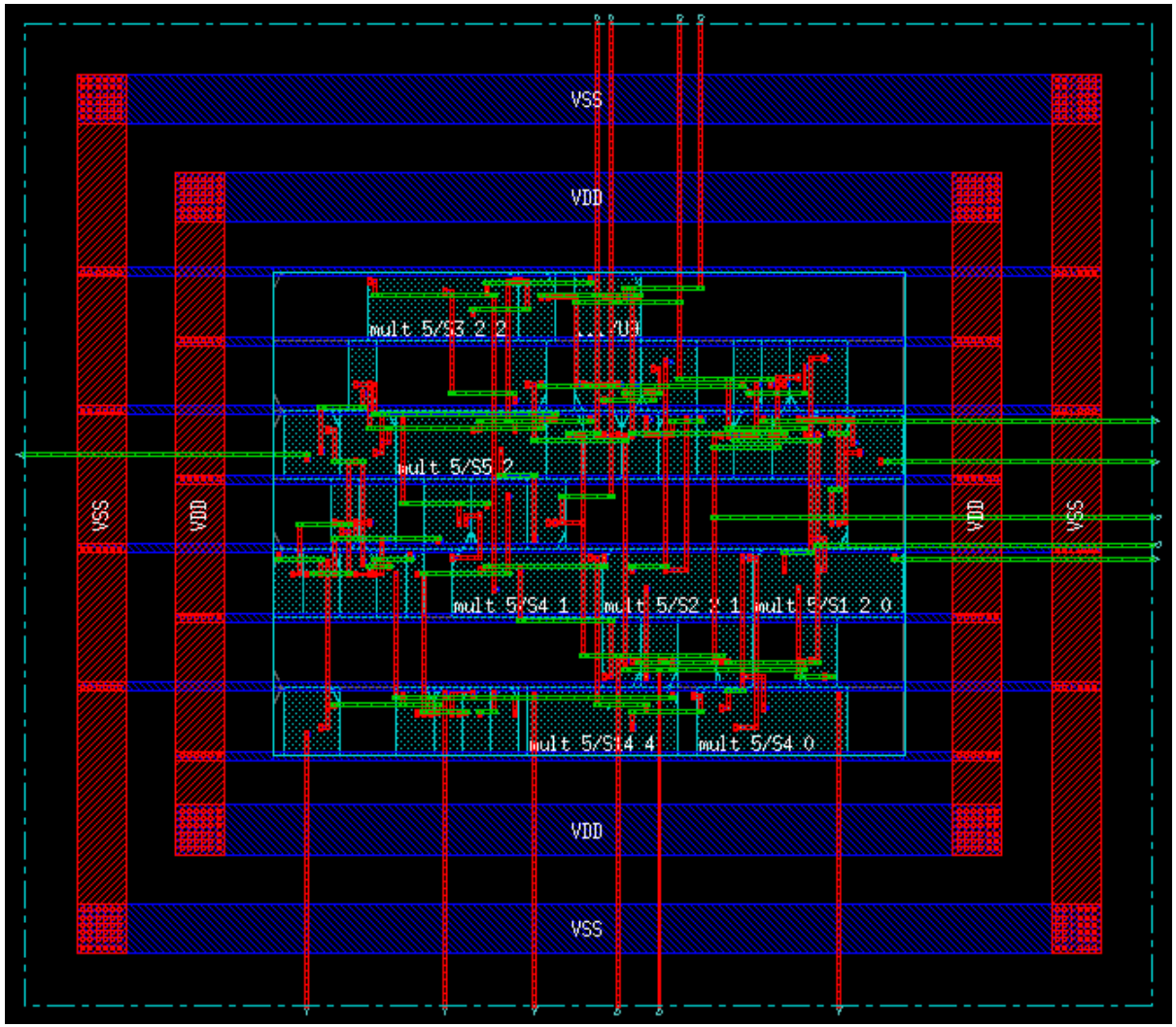
Layout



Automatic Placement



Automatic Routing



FET Sizing

- Theory
  - $\boldsymbol{I \approx \mu \cdot c_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_G - V_T) \cdot V_{DS}}$
  - $\boldsymbol{R = \frac{1}{\beta \cdot (V_G - V_T)} \propto \frac{L}{W}}$
- Motivation 1
  - pFETs and nFETs have different mobility values.
    - $\mu_n > \mu_p$
  - Thus, if an nFET and a pFET networks have the same transistor sizes, their delay values are different.
- Motivation 2
  - Minimum-size FETs might not provide enough drive strength.
- Goal
  - Achieve perfectly-balanced delay values (from Motivation 1).
  - Satisfy delay constraints (from Motivation 2).
- Mobility ratio
  - $\boldsymbol{\mu_n = r \cdot \mu_p \; (r > 1)}$
  - $\boldsymbol{R_p = r \cdot R_n}$

FET Sizing

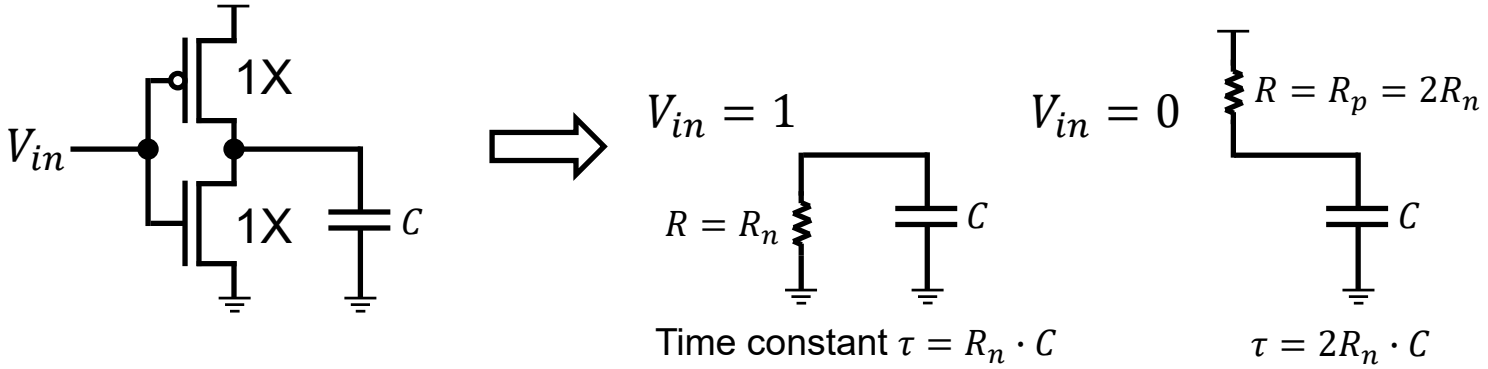
- Theory
  - $I \approx \mu \cdot c_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_G - V_T) \cdot V_{DS}$
  - $R = \frac{1}{\beta \cdot (V_G - V_T)} \propto \frac{L}{W}$
  - The drive strength (current) is
    - proportional to W
    - inversely proportional to L
  - The input capacitance is proportional to L and W.
  - If L increases
    - The input capacitance goes up.
    - The drive strength goes down (or the output resistance goes up).
    - The cell area goes up.
    - Thus, do not increase L (i.e., **use the minimum channel length**).
  - If W increases
    - The input capacitance goes up.
    - The drive strength goes up (or the output resistance goes down).
    - The cell area goes up.
    - If the input capacitance overhead is small, upsizing FETs reduces the delay of the downstream net.

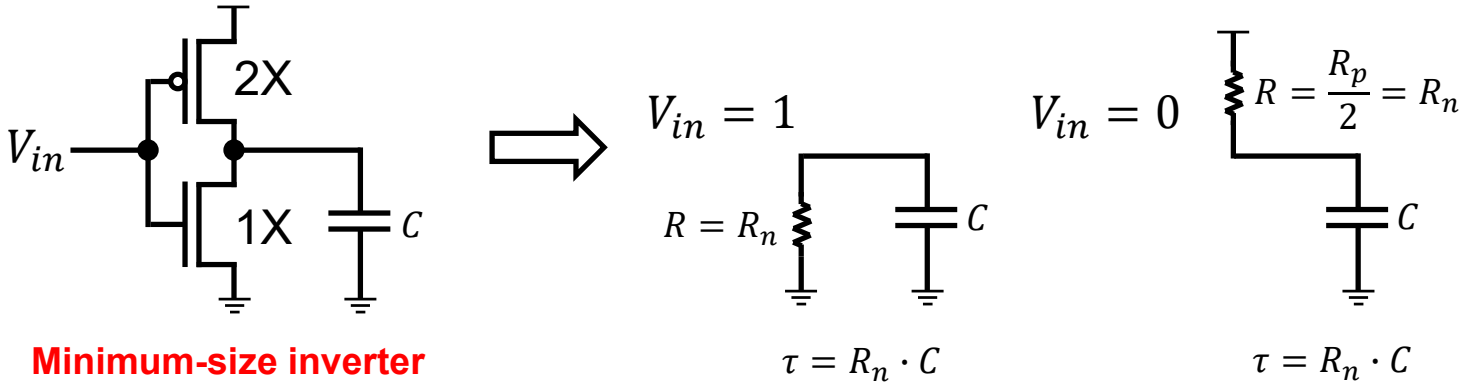
FET Sizing

- Theory
  - The FET width cannot be reduced infinitely (design rules).
  - Suppose the minimum transistor length and width are L_0 and W_0, respectively.
  - Then,
    - Minimum-size nFET = $\left(\frac{W_0}{L_0}\right)_n$: This is a 1X nFET.
      - Resistance: R_n
    - Minimum-size pFET = $\left(\frac{W_0}{L_0}\right)_p$: This is a 1X pFET.
      - Resistance: R_p
- Transistor upsizing
  - If the size of an nFET is $\left(\frac{k \cdot W_0}{L_0}\right)_n$, it is a kX nFET.
    - Resistance: $\frac{R_n}{k}$
  - If the size of a pFET is $\left(\frac{k \cdot W_0}{L_0}\right)_p$, it is a kX pFET.
    - Resistance: $\frac{R_p}{k}$

FET Sizing (Matching)

- Example: Inverter
  - $\mu_n = \mathbf{2} \cdot \mu_p$ (i.e., $R_p = 2R_n$)

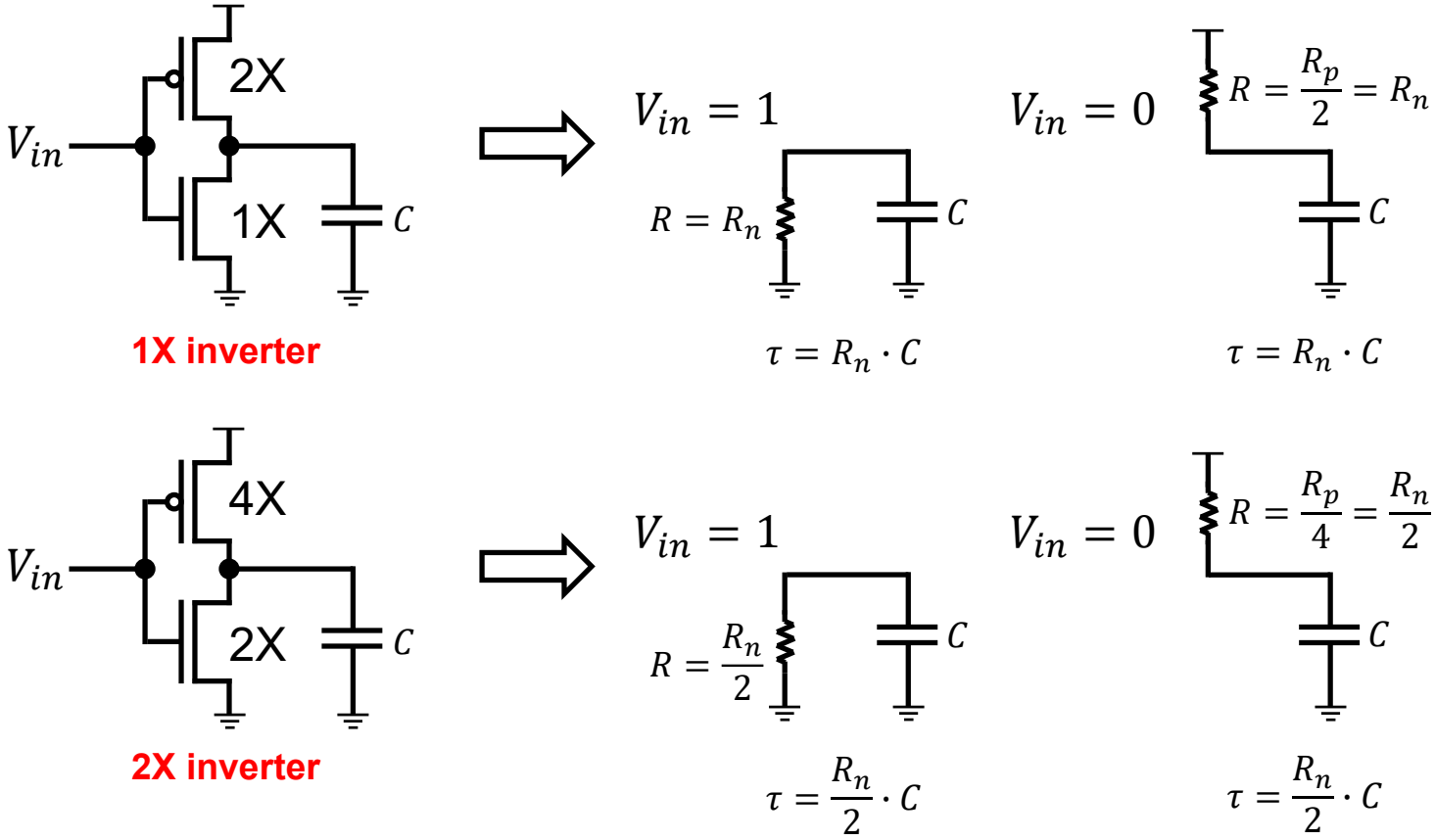




Minimum-size inverter

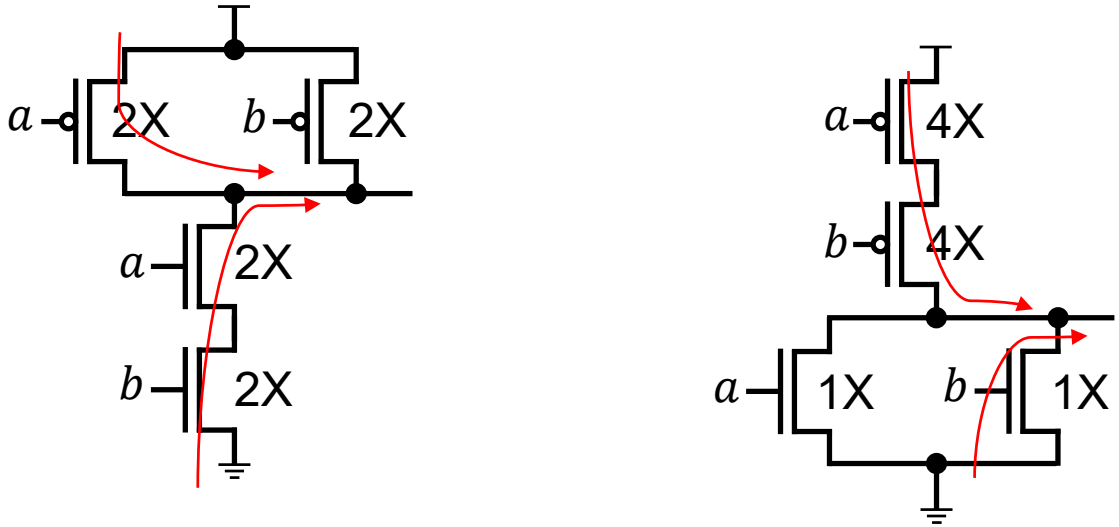
FET Sizing (Delay Reduction)

- Example: Inverter
  - $\mu_n = \mathbf{2} \cdot \mu_p$ (i.e., $R_p = 2R_n$)



FET Sizing

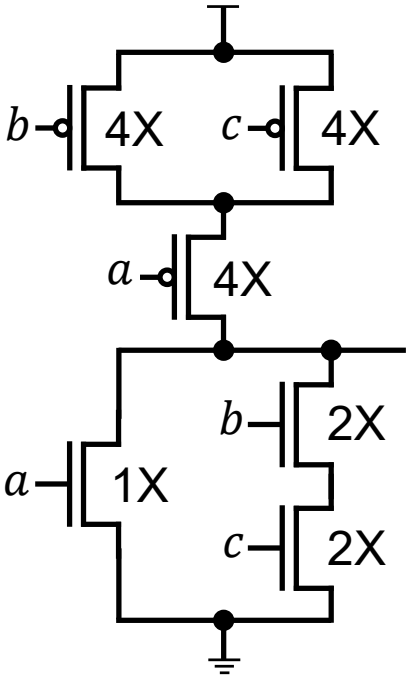
- NAND2_X1, NOR2_X1



FETs are sized for the worst-case signal path.

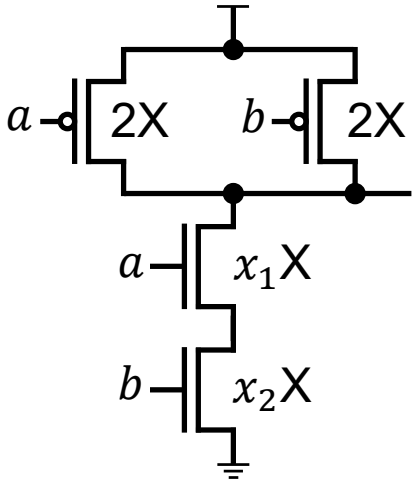
FET Sizing

- $f = \overline{a + b \cdot c}$ (1X)



FET Sizing – Analytical Approach

- NAND2_X1
  - pFETs: Each should be 2X.
  - nFETs
    - If a is upsized to x_1X and b is upsized to x_2X ($x_1, x_2 > 1$)
      - Resistance of a: $\frac{R_n}{x_1}$
      - Resistance of b: $\frac{R_n}{x_2}$
    - The total resistance should be R_n.
      - $\frac{R_n}{x_1} + \frac{R_n}{x_2} = R_n \Rightarrow \frac{1}{x_1} + \frac{1}{x_2} = 1$
    - For instance, $(x_1, x_2) = (2,2), \left(3, \frac{3}{2}\right), \left(4, \frac{4}{3}\right), \ldots$
    - We want to minimize the total area.
      - Min. $x_1 + x_2$

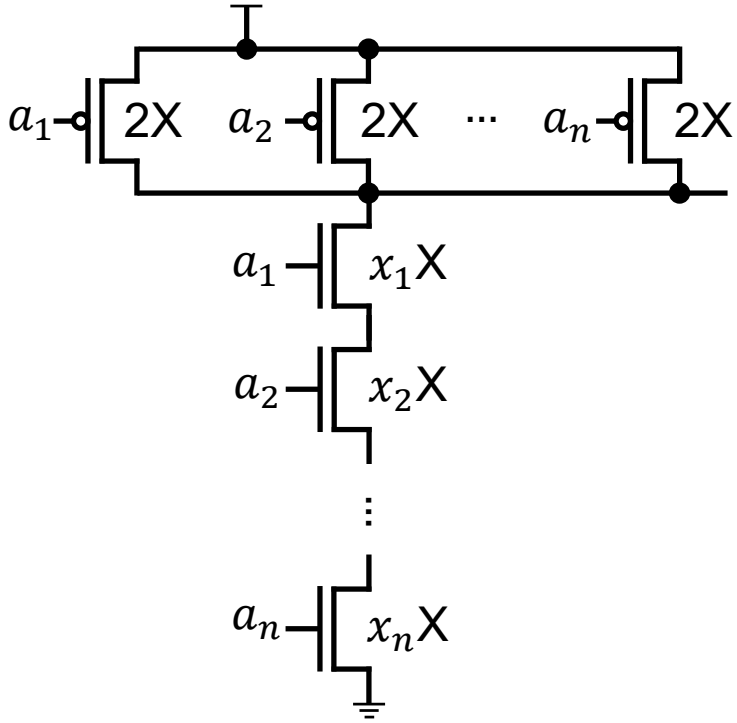


FET Sizing – Analytical Approach

- Problem
  - Minimize $f(x_1, x_2) = x_1 + x_2$ under the following constraints.
    - $x_1, x_2 > 1$
    - $\frac{1}{x_1} + \frac{1}{x_2} = 1$
  - Solve
    - $\frac{1}{x_1} + \frac{1}{x_2} = 1 \Rightarrow x_2 = \frac{x_1}{x_1 - 1}$
    - $f(x_1, x_2) = x_1 + x_2 = x_1 + \frac{x_1}{x_1 - 1} = f(x_1) = \frac{{x_1}^2}{x_1 - 1}$
    - $f'(x_1) = \frac{2x_1(x_1 - 1) - {x_1}^2}{(x_1 - 1)^2} = \frac{{x_1}^2 - 2x_1}{(x_1 - 1)^2}$
    - Thus, f is minimized when $x_1 = 2$. In this case, x_2 is also 2.

FET Sizing – Analytical Approach

- NAND_Xn (n-input NAND gate)
  - pFETs: Each should be 2X.
  - nFETs
    - If a_i is upsized to x_iX ($x_i > 1$)
      - Resistance of a_i: $\frac{R_n}{x_i}$
    - The total resistance should be R_n.
      - $\sum_{i=1}^{n} \frac{R_n}{x_i} = R_n \Rightarrow \frac{1}{x_1} + \frac{1}{x_2} + \cdots + \frac{1}{x_n} = 1$
    - We want to minimize the total area.
      - Min. $\sum_{i=1}^{n} x_i = x_1 + x_2 + \cdots + x_n$



FET Sizing – Analytical Approach

- Problem
  - Minimize $f(x_1, x_2, \dots, x_n) = x_1 + x_2 + \cdots + x_n$ under the following constraints.
    - $x_i > 1$
    - $\frac{1}{x_1} + \frac{1}{x_2} + \cdots + \frac{1}{x_n} = 1$
  - Solve
    - Let $\frac{1}{x_i} = y_i$. Then, the problem becomes as follows:
      - Minimize $f(y_1, \dots, y_n) = \frac{1}{y_1} + \cdots + \frac{1}{y_n}$
      - $y_i < 1$
      - $y_1 + \cdots y_n = 1$
    - $y_n = 1 - (y_1 + \cdots + y_{n-1})$
    - $f(y_1, \dots, y_n) = \frac{1}{y_1} + \cdots + \frac{1}{y_n} = f(y_1, \dots, y_{n-1}) = \frac{1}{y_1} + \cdots + \frac{1}{y_{n-1}} + \frac{1}{1-(y_1+\cdots+y_{n-1})}$
    - Solve $\frac{\partial f}{\partial y_1} = 0, \dots, \frac{\partial f}{\partial y_{n-1}} = 0$.
    - $\frac{\partial f}{\partial y_i} = -\frac{1}{{y_i}^2} + \frac{1}{\left(1-(y_1+\cdots+y_{n-1})\right)^2} = 0$
      - $y_i = 1 - (y_1 + \cdots + y_{n-1}) \Rightarrow y_i = y_n$
    - Thus, f is minimized when $y_1 = y_2 = \cdots = y_n$, i.e., $x_1 = x_2 = \cdots = x_n$.
    - As a result, $x_1 = x_2 = \cdots = x_n = n$.