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Semi-Dynamic and Dynamic Flip-FLops with Embedded Logic

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Introduction

This paper describes a family of semi-dynamic and dynamic edge-triggered flip-flops to be used with static and dynamic circuits, respectively [1][2]. The flip-flops provide both short latency and the capability of incorporating logic functions with minimum delay penalty, properties which make them very attractive for high-performance microprocessor design. The flops described herein are used in the UltraSPARC-III microprocessor [3].

A Semi-Dynamic Flip-Flop

A. Basic Operation

A block diagram of a semi-dynamic flip-flop (SDFF) is shown in Fig. 1. The circuit is composed of a dynamic front-end and a static back-end, hence its designation. The flop samples input D and produces output QB, which is the logic complement of D. The circuit operates as follows. On the falling edge of clock CK, the flop enters the *precharge phase*. Node X is precharged high, cutting off node Q from the input stage. The static latch INV5-6 holds the previous logic level of Q and QB. Since CKD is also low during precharge, node S remains high holding transistor N1 on. The *evaluation phase* begins with the rising edge of clock CK. If input D is low (i.e., the flop is latching a zero) node X would remain high, held by the INV3-4 latch. Node Q would either remain low or will be discharged through transistors N4-5, driving QB high (See Fig. 2a). Three gate delays after CK rises, node S will be driven low, turning transistor N1 off. This *shut-off* operation will prevent a subsequent low-to-high transition of D from discharging node X. This feature provides the flip-flop its edge-triggered nature.

If input D were high prior to evaluation (i.e., the flop is latching a one), node X would be discharged through the pulldown path N1-3. The static latch INV3-4 would hold the value of X even if input D were subsequently driven low. The high-to-low transition of X will turn transistor P2 on, driving Q high and output QB low (See Fig. 2b). The falling transition of X would also force node S to remain high, preventing the shut-off of transistor N1, which is unnecessary after node X has been discharged.

B. Conditional Shutoff

Notice that by using a NAND gate coupled to node X and CKD, the shutoff of the pulldown path is conditioned to the state of input D. If D is high prior to evaluation, signal CKD is blocked and no shutoff is performed. This feature allows reducing the sampling window by about one inverter delay, which means a shorter hold time for the flip-flop and a better input noise rejection.

C. Simulation Results

Fig. 3 shows spice waveforms for the flip-flop of Fig. 1. Results were obtained in a 0.25um technology at 1.6V, 105°C, and typical devices. The latency of the flip-flop at zero setup time is 188ps for the low-to-high input transition, and 185ps for the high-to-low input transition. Notice that setup time is zero, and it can be even slightly negative. Worst-case hold time is 130ps.

Embedding Logic Functions

One important advantage of SDFF is that scan circuitry can be added to the basic design with nearly zero hit in performance, in contrast to the flip-flop reported in [1]. Yet, another main advantage is that logic functions can be easily incorporated in its dynamic front-end. In fact, most logic functions available in Domino logic can also be built into this flop, such as wide OR functions, multiplexors, and complex gates. As an example, Fig. 4 shows a SDFF with embedded MUX2 logic. If SEL1 is high and SEL0 is low, input D1 is selected and latched. Otherwise, input D0 is latched. While the latency of the flip-flop is slightly increased, the merging allows the elimination of one gate delay from a critical path leading to the flip-flop (See timing numbers in TABLE 1).

A Dual Rail Dynamic Flip-Flop

A dual-rail dynamic version of this flip-flop (DFF) is shown Fig. 5. The flop samples input data D and produces dual-rail outputs Q and QB. By using a dynamic flip-flop, the time penalty associated with driving dynamic logic with static flops is avoided, since the flop outputs are also monotonic.

The circuit operates as follows. On the falling edge of clock, the flip-flop enters the *precharge* phase. Nodes X and Y are precharged high, while outputs Q and QB are predischarged low; transistors N6, N7, P2, and P3 are all off, while transistors N1 and N3, the *shut-off* devices, are both on. On the rising edge of clock, the flip-flop enters the *evaluation* phase. If input D is high, node X will be discharged, causing output Q to go high, transistor N3 to shut off, and P3 to turn on. Node Y will remain high, held by transistor P3 which operates as a *keeper*, forcing output QB to remain low. If D goes from high to low while CK is still high, transistor N6 will hold node X at ground. The shut-off transistor N3, which is off, will prevent node Y from discharging. If input D is low, node Y will be discharged, causing output QB to go high and Q to remain low.

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The purpose of inverters INV2-3 and INV4-5 is to reduce the load on the critical nodes X and Y. This minimizes the flip-flop latency at the expense of a larger hold time. Similarly to SDFF, DFF can also incorporate logic functions. As an example, Fig. 6 shows a DFF with embedded MUX2 logic.

Table 1 provides a summary of the speed characteristics of the flip-flops discussed in this paper. This includes: SDFF (Fig. 1), MUX2_SDFF (Fig. 4), SFF, which is a conventional pseudo-static master-slave flip-flop [4] using transmission gates and week feedback inverters, and SFF + static MUX2 gate (not shown). Compared to SFF, SDFF is about 33% faster. In addition, SDFF is about half the size, presents half the clock load, and requires a single clock phase.

Conclusion

This paper describes a family of semi-dynamic and dynamic edge-triggered flip-flops which are part of the UltraSPARC-III microprocessor. They provide short latency, reduced clock load, a good interface to static and dynamic logic, and can easily incorporate logic functions with minimum delay penalty, eliminating one gate delay from a critical path. These flip-flops have played an integral roll in meeting the UltraSPARC-III cycle time goal.

References

[1] H. Partovi, et al., "Flow-through latch and edge-triggered flip-flop hybrid elements," *ISSCC Digest of Technical Papers*, pp. 132-139, February 1996.

[2] N. B. Gaddis, J. R. Butler, A. Kumar, W. J. Queen, "A 56-entry instruction reorder buffer," *ISSCC Digest of Technical Papers*, pp. 212-213, February 1996.

[3] G. Lauterbach, "UltraSPARC-III an ultra-high clock rate SPARC for scalable systems," *Microprocessor Forum*, San Jose, CA, October 1997.

[4] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective*, Prentice Hall, 1996, pp. 349-350.

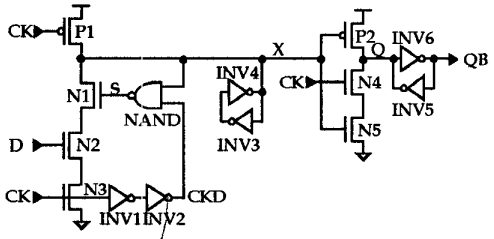

Fig. 1. Edge-triggered semi-dynamic flip-flop (SDFF)

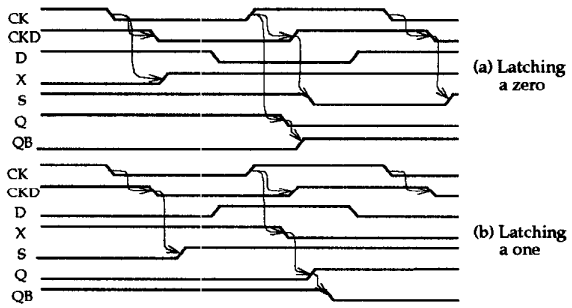

Fig. 2. Timing diagram for SDFF

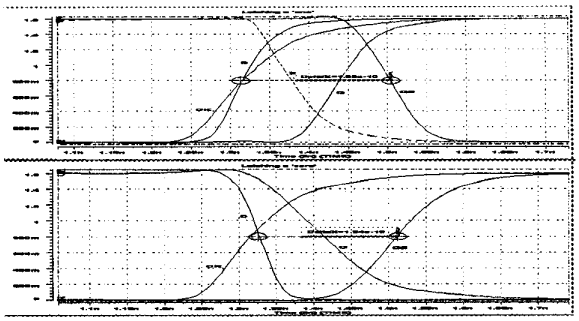

Fig. 3. Spice waveforms for SDFF

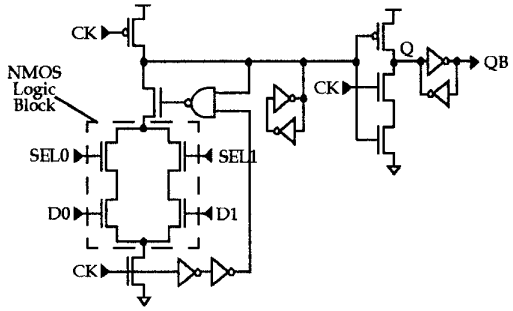

Fig. 4. SDFF with embedded MUX2 logic (MUX2_SDFF)

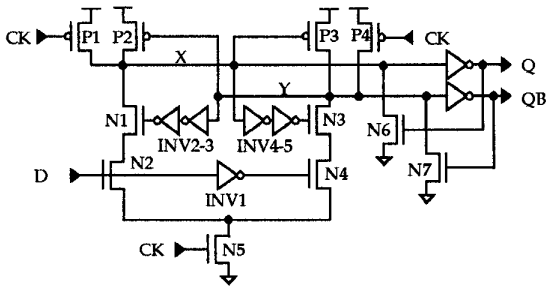

Fig. 5. Edge-triggered dual-rail dynamic flip-flop (DFF)

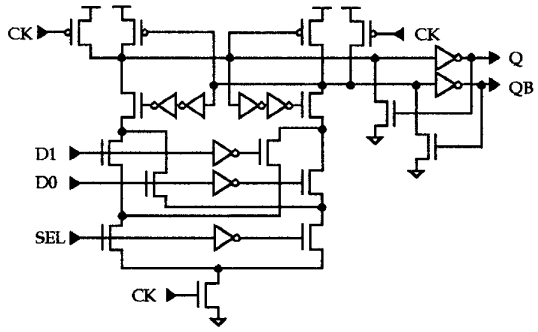

Fig. 6. DFF with embedded MUX2 logic (MUX2_DFF)

TABLE 1. Speed Comparison of SDFF versus SFF

Flip-Flop Type	Latency	Speedup
SDFF	188ps	1.6
SFF	300ps	1.0
MUX2_SDFF	230ps	2.1
MUX2 + SFF	480ps	1.0