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Low-Power Pulse-Triggered Flip-Flop Design With Conditional Pulse-Enhancement Scheme

Yin-Tsung Hwang, Jin-Fa Lin, and Ming-Hwa Sheu

***Abstract*—In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. First, the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Various postlayout simulation results based on UMC CMOS 90-nm technology reveal that the proposed design features the best power-delay-product performance in seven FF designs under comparison. Its maximum power saving against rival designs is up to 38.4%. Compared with the conventional transmission gate-based FF design, the average leakage power consumption is also reduced by a factor of 3.52.**

***Index Terms*—Flip-flop, low power, pulse-triggered.**

I. Introduction

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power [1]. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations [2]–[5]. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulsewidth control in the face of process variation and the configuration of pulse clock distribution network [4].

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse

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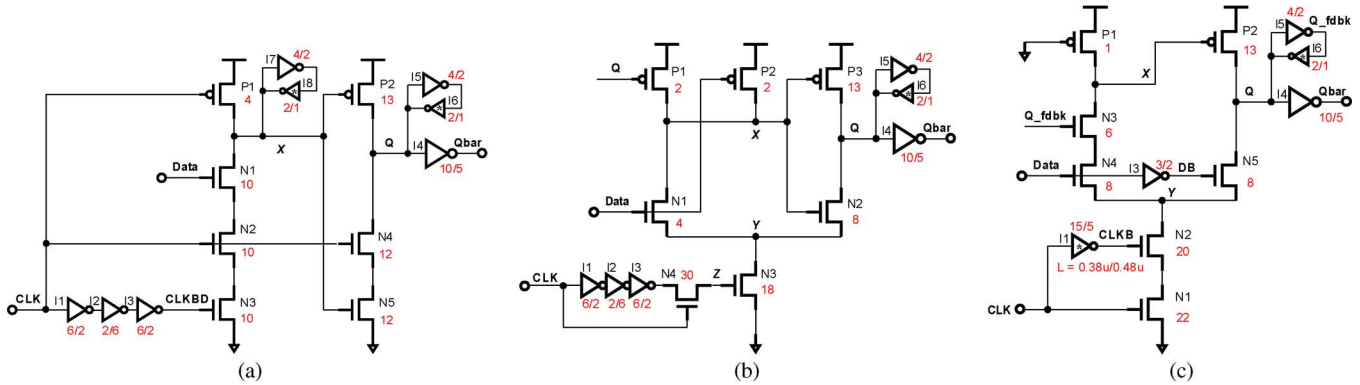


Fig. 1. Conventional pulse-triggered FF designs. (a) ip-DCO [6]. (b) MHLLF [11]. (c) SCCER [12].

generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied [7]–[10]. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulsewidth control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced. This gives rise to competitive power and power–delay–product performances against other P-FF designs.

II. Proposed Implicit-Type P-FF Design With Pulse Control Scheme

A. Conventional Implicit-Type P-FF Designs

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named ip-DCO, is given in Fig. 1(a) [6]. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

Fig. 1(b) shows an improved P-FF design, named MHLLF, by employing a static latch structure presented in [11]. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero. This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node X is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1". Fig. 1(c) shows a refined low power P-FF design named SCCER using a conditional discharged technique [9], [12]. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a)) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X [12]. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

B. Proposed P-FF Design

The proposed design, as shown in Fig. 2, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 2, the upper part latch design is similar to the one employed in SCCER design [12]. As opposed to the transistor stacking design in Fig. 1(a) and (c), transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate [13], [14] to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design [11], where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.

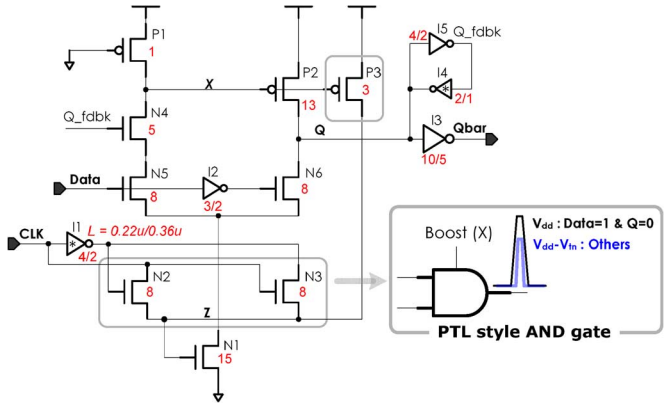


Fig. 2. Schematic of the proposed P-FF design with pulse control scheme.

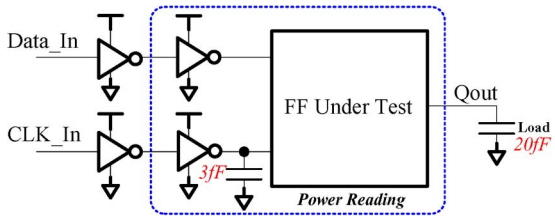


Fig. 3. Simulation setup model.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node X is pulled high most of the time. It steps in when node X is discharged to $|\mathrm{V_{TP}}|$ below the $\mathrm{V_{DD}}$. This provides additional boost to node Z (from $\mathrm{V_{DD}}-\mathrm{V_{TH}}$ to $\mathrm{V_{DD}}$). The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path.

The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulsewidth enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

III. Simulation Results

To demonstrate the superiority of the proposed design, postlayout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the three P-FF designs shown in Fig. 1 (ip-DCO [6], MHLLF [11], SCCER [12]), another P-FF design called conditional capture FF (CCFF) [7], and two other non-pulse-triggered FF designs, i.e., a sense-amplifier-based FF (SAFF) [2], and a conventional transmission gate-based FF (TGFF). The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0 V. Since pulsewidth design is crucial to the correctness of data capturing as well as the power consumption, the pulse generator logic in all designs are first sized to function properly across process variation. All designs are further optimized subject to the tradeoff between power and D-to-Q delay, i.e., minimizing the product of the two terms.

Fig. 3 shows the simulation setup model. To mimic the signal rise and fall time delays, input signals are generated through buffers. Considering the loading effect of the FF to the previous stage and the clock tree, the power consumptions of the clock and data buffers are also included. The output of the FF is loaded with a 20-fF capacitor. An extra capacitance of 3 fF is also placed after the clock buffer. To illustrate the merits of the presented work, Fig. 4 shows the simulation waveforms of the proposed P-FF design against the MHLLF design. In the proposed design, pulses of node Z are generated on every rising edge of the clock. Due to the extra voltage boost from transistor P3, pulses generated to capture input data "1" are significantly enhanced in their heights and widths compared with the pulses generated for capturing data "0" (0.84 V versus 0.65 V in height and 141 ps *versus* 84 ps in width). In the MHLL design, there is no such differentiation in their pulse generation. In addition, no signal degradation occurs in the internal node X of the proposed design. In contrast, the internal node X in MHLLF design is degraded when Q equals to "0" and data equals to "1". Node Q thus deviates slightly from an intact value "0" and causes a DC power consumption at the output stage. From Fig. 4, the height of its pulses at node Z is around 0.68 V. Furthermore, node Z is floating when clock equals "0" and its value drifts gradually.

To elaborate the power consumption behavior of these FF designs, five test patterns, each exhibiting a different data switching probability, are applied. Five of them are deterministic patterns with 0% (all-zero or all-one), 25%, 50%, and 100% data transition probabilities, respectively. The power consumption results are summarized in Table I. Due to a shorter discharging path and the employment of a conditional pulse enhancement scheme, the power consumption of the proposed design is the lowest in all test patterns. Take the test pattern with 50% data transition probability as an example, the power saving of proposed design ranges from 38.4% (against the ip-DCO design) to 5.6% (against the TGFF design). This savings is even more pronounced when operating at lower data switching activities, where the power consumption of pulse generation circuitry dominates. Because of a redundant switching power consumption problem at an internal node, the ip-DCO design has the largest power consumption when data switching activity is 0% (all 1).

Fig. 5 shows the curves of power-delay-product $\mathrm{PDP_{DQ}}$ (delay from D to Q) versus setup time (for 50% data switching activity). The $\mathrm{PDP_{DQ}}$ values of the proposed design are the smallest in all designs when the setup times are greater than -60 ps. Its minimum $\mathrm{PDP_{DQ}}$ value occurs when the setup time is -53.9 ps and the corresponding D-to-Q delay is 116.9 ps. The CCFF design is ranked in the second place in this evaluation with its optimal setup time as -67 ps. The setup time of the conventional TGFF design is always positive and has the smallest $\mathrm{PDP_{DQ}}$ value when the setup time is 47 ps. In general, the MHLLF design has the worst $\mathrm{PDP_{DQ}}$ performance due to the drawback of its latch structure. Fig. 6(a) shows the best $\mathrm{PDP_{DQ}}$ performance of each design under different data switching activities. The proposed design takes the lead in all types of data switching activity. The SCCER and the CCFF designs almost tie in the second place. Fig. 6(b) shows the $\mathrm{PDP_{DQ}}$ performance of these designs at different process corners under the condition of 50% data switching activity. The performance edge of the proposed design is maintained as well. Notably, the MHLLF design has the worst $\mathrm{PDP_{DQ}}$ performance especially at the SS process corner due to a large D-to-Q delay and the poor driving capability of its pulse generation circuit.

Table I also summarizes some important performance indexes of these P-FF designs. These include transistor count, layout area, setup time, hold time, min D-to-Q delay, optimal PDP, and the clock tree

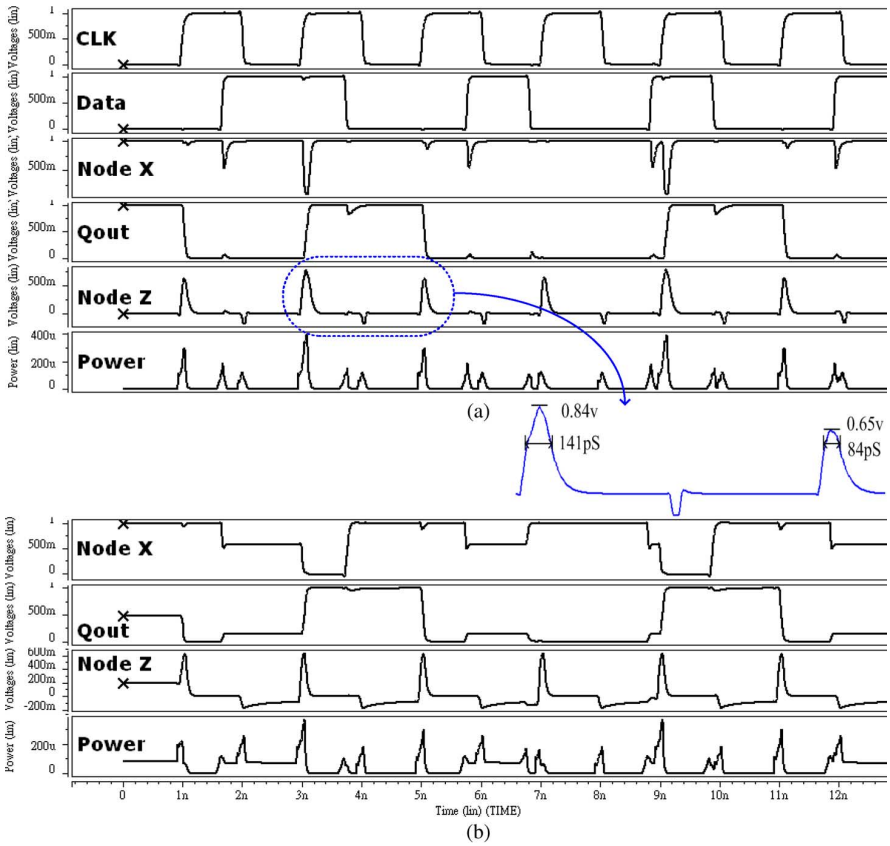


Fig. 4. Simulation waveforms of (a) proposed and (b) MHLLF designs.

TABLE I
FEATURE COMPARISON OF VARIOUS P-FF DESIGNS

P-FF	ip-DCO	MHLFF	SCCER	CCFF	TGFF	SAFF	**Proposed**
Number of Transistors / Layout Area (μm^2)	23 / 91.88	19 / 93.02	17 / 80.07	26 / 89.29	20 / 69.31	17 / 75.37	19 / 79.17
Setup Time (pS)	-35.8	8.3	-58.1	-51.6	51.1	-9.3	-39.7
Hold Time (pS)	47.4	82.2	59.3	64.5	24.5	39.9	85.1
Min. Data to Q Delay(pS)	118.75	177.01	112.90	121.30	211.35	136.06	107.24
Clock Tree Power µW	10.24	7.82	12.58	7.95	9.27	8.521	8.03
Average Power (100% Activity) µW	42.20	35.96	36.27	35.72	33.042	35.287	31.11
Average Power (50% Activity) µW	35.54	27.61	28.46	26.77	23.997	26.562	22.65
Average Power (25% Activity) µW	32.22	23.42	24.14	22.23	19.474	21.72	18.02
Average Power (0% all-one) µW	40.33	18.74	19.25	15.18	14.557	16.552	12.92
Average Power (0% all-zero) µW	17.5	18.97	19.40	19.18	14.915	16.692	12.90
Optimal Power-Delay-Product (50% Activity) fJ	4.22	4.89	3.19	3.22	5.07	3.61	2.65

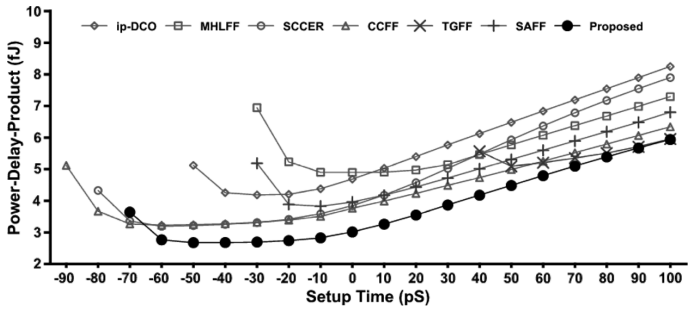
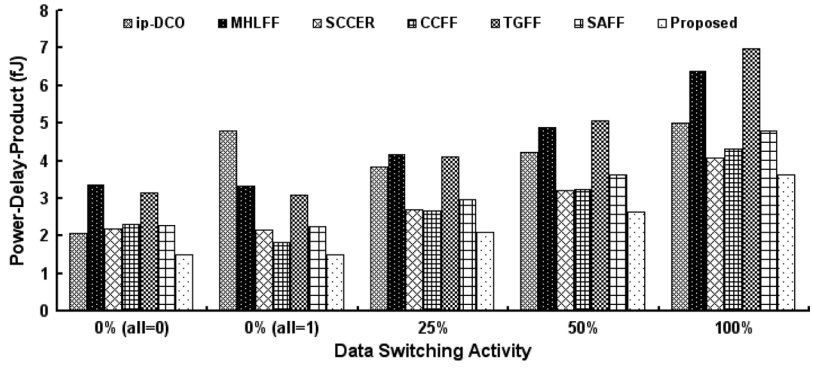
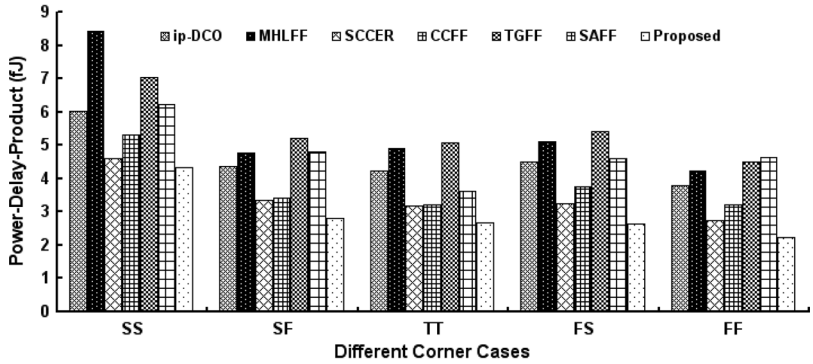


Fig. 5. Power–delay (D-to-Q)-product *versus* setup time.

power. Although the transistor count of the proposed design is not the lowest one, its actual layout area is the smaller than all but the TGFF design. The MHLLF design exhibits the largest layout area because of an oversized pulse generation circuit. Following the measurement methods in [15], curves of D-to-Q delay versus setup time and C-to-Q delay versus hold time are simulated first. Setup time is defined as the point in the curve where D-to-Q delay is the minimum. Hold time is measured at the point where the slope of the curve equals -1. The proposed design features the shortest minimum D-to-Q delay. Its hold time is longer than other designs because the transistor (P3) for the pulse enhancement requires a prolonged availability of data input. The power drawn from the clock tree is calculated to evaluate the impact of FF loading on the clock jitter. Although the proposed FF design requires clock signal connected to the drain of transistor N2, the drawn current is not significant. Due to complementary switching behavior of N2 and N3, there exists no signal path from the entry of the clock signal to either V_{DD} or G_{ND}. The clock tree is only liable for charging/discharging node Z. The optimal PDP value of the proposed design is also



(a)



(b)

Fig. 6. Power–delay-product performances under (a) different data switching activities and (b) different processor corners at 50% data switching activity.

TABLE II
LEAKAGE POWER COMPARISON IN STANDBY MODE (μW)

FF design / (CLK, Data)	(0,0)	(0,1)	(1,0)	(1,1)
ip-DCO	3.737	1.317	0.834	1.364
MHLFF	3.656	0.666	2.161	0.763
SCCER	0.639	1.208	0.779	0.823
CCFF	1.511	2.623	2.551	2.072
TGFF	1.991	1.766	2.114	1.631
SAFF	8.092	5.864	1.537	1.743
Proposed	0.444	0.481	0.582	0.624

significantly better than other designs. The simulation results show that the clock tree power of the proposed design is close to those of the two leading designs (MHLFF and CCFF) and outperforms ip-DCO, SCCER, TGFF, and SAFF, where clock signals connected to gates of the transistors only. The setup time is measured as the point where the minimum PDP value occurs. The setup times of these designs vary from -67 to $+47$ ps. Note that although the optimal setup time of the proposed design is -53.9 ps, its PDP value is lowest in all designs for any setup time greater than -60 ps. The D-to-Q delay and the hold time are calculated subject to the optimal setup time. The D-to-Q delay of the proposed design is second to the SCCER design only and outperforms the conventional TGFF design by a margin of 44.7%. The hold time requirement seems to be slightly larger due to a negative setup time. This number reduces as the setup time moves toward a positive value.

Table II gives the leakage power consumption comparison of these FF designs in a standby mode (clock signal is gated). For a fair comparison, we assume the output Q as "0" when input data is "1" to exclude the extra power consumption coming from the discharging of the internal node X. For different clock and input data combinations, the proposed design enjoys the minimum leakage power consumption, which is mainly attributed to the reduction in the transistor sizes along the discharging path. The SAFF design experiences the worst leakage power consumption when clock equals "0" because its two precharge pMOS transistors are always turned on. Compared to the conventional TGFF design, the average leakage power is reduced by a factor of 3.52. Finally, to show the robustness of the proposed design against the process variations, Table III compiles the changes in the width and the height of the generated discharge pulses under different process corners. Although significant fluctuations in pulsewidth and height are observed, the unique conditional pulse-enhancement scheme works well in all cases.

TABLE III
PULSE GENERATION AGAINST PROCESS VARIATION (pS/V)

Corner Case	SS	SF	TT	FS	FF
Data = 0	180.1/0.45	92.9/0.61	84.7/0.65	83.1/0.63	50.0/0.77
Data = 1	375/0.51	167.5/0.86	141.3/0.84	145.4/0.87	87.7/1.04

IV. CONCLUSION

In this paper, we devise a novel low-power pulse-triggered FF design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Simulation results indicate that the proposed design excels rival designs in performance indexes such as power, D-to-Q delay, and PDP. Coupled with these design merits is a longer hold-time requirement inherent in pulse-triggered FF designs. However, hold-time violations are much easier to fix in circuit design compared with the failures in speed or power.

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Area-Efficient Parallel FIR Digital Filter Structures for Symmetric Convolutions Based on Fast FIR Algorithm

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***Abstract*—Based on fast finite-impulse response (FIR) algorithms (FFAs), this paper proposes new parallel FIR filter structures, which are beneficial to symmetric coefficients in terms of the hardware cost, under the condition that the number of taps is a multiple of 2 or 3. The proposed parallel FIR structures exploit the inherent nature of symmetric coefficients reducing half the number of multipliers in subfilter section at the expense of additional adders in preprocessing and postprocessing blocks. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area; in addition, the overhead from the additional adders in preprocessing and postprocessing blocks stay fixed and do not increase along with the length of the FIR filter, whereas the number of reduced multipliers increases along with the length of the FIR filter. For example, for a four-parallel 72-tap filter, the proposed structure saves 27 multipliers at the expense of 11 adders, whereas for a four-parallel 576-tap filter, the proposed structure saves 216 multipliers at the expense of 11 adders still. Overall, the proposed parallel FIR structures can lead to significant hardware savings for symmetric convolutions from the existing FFA parallel FIR filter, especially when the length of the filter is large.**

***Index Terms*—Digital signal processing (DSP), fast finite-impulse response (FIR) algorithms (FFAs), parallel FIR, symmetric convolution, very large scale integration (VLSI).**

I. INTRODUCTION

Due to the explosive growth of multimedia application, the demand for high-performance and low-power digital signal processing (DSP) is getting higher and higher. Finite-impulse response (FIR) digital filters are one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems used in cellular wireless communication. Furthermore, when narrow transition-band characteristics are required, the much higher order in the FIR filter is unavoidable. For example, a 576-tap digital filter is used in a video ghost canceller for broadcast television, which reduces the effect of multipath signal echoes. On the other hand, parallel and pipelining processing are two techniques used in DSP applications, which can both be exploited to reduce the power consumption. Pipelining shortens the critical path by interleaving pipelining latches along the datapath, at the price of increasing the number of latches and the system latency, whereas parallel processing increase the sampling rate by replicating hardware so that multiple inputs can be processed in parallel and multiple outputs are generated at the same time, at the expense of increased area. Both techniques can reduce the power consumption by lowering the supply voltage, where the sampling speed does not increase. In this paper, parallel processing in the digital FIR filter will be discussed. Due to its linear increase in the hardware implementation cost brought by the increase of the block size L, the parallel processing technique loses its advantage in practical implementation. There have been a few papers

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