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## **Comparative performance evaluation of dynamic and static flip-flops**

### **Course Project**

#### ***Abstract:***

This project presents to evaluate the energy and delay of implicit-pulsed, data-close-to-output, semi-dynamic hybrid flip-flop (ip-DCO), hybrid latch-flip-flop (HLFF), semi-dynamic edge-triggered flip-flop (SDFF) and time-borrowing master-slave flip-flop (tb-SMS) designed in 65nm techniques. In particular, the comparison strategy includes the energy consumption, the data to Q delay, energy-delay product and total width. I suppose to find a way to choose the design of high-speed and energy-efficient in the critical path or majority path via research characteristics of different Flip-Flop. All the simulations were based on the tsmcN65 library in the Cadence.

**Keywords:** High speed, VLSI, flip-flops, power dissipation, master-slave, transmission-gate.

## **I. INTRODUCTION**

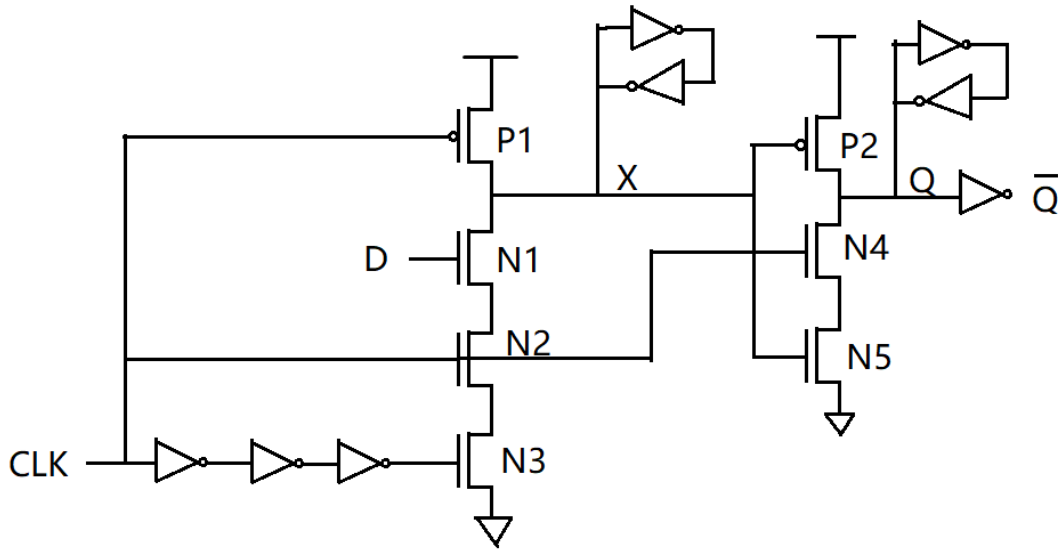
As the CMOS manufacturing technology improved and portable electronic devices universal, the high-speed and low-energy design microprocessor and sequential logic circuits, such as registers, memory elements, counters etc., are thirstily needed by the market. In order to achieve a design that is both high-performance while also being power-efficient, various classes of flip-flops have been proposed. Understanding and selecting the appropriate choice of flip-flop for a particular application is difficult, since it involves a large number of existing topology, and depends on area, power dissipation and transistor sizing. In specific, efficient topology and good layout design is necessary to achieve reliable results that are usable in practical design.

In this paper, I hope to via comparing different single-edge triggered Flip-Flop to aid designers choosing appropriate Flip-Flop applicated on the particular circuit. The organization of the paper is as follows: The section II, describes the function of different Flip-Flop. The section III, presents a comparison of several types of single edge-triggered flip-flops, describing the key differences in terms of both performance and power. Section IV concludes the paper.

## II. SINGLE EDGE-TRIGGERED FLIPFLOPS

### a. Implicit-pulsed, data-close-to-output, semi-dynamic hybrid flip-flop (ip-DCO)

Figure 1 shows the basic construction of ip-DCO. When the clock is low, the flip-flop is in the precharge phase. Node X is precharged to the level of the power supply, and node Q holds its previous value. The transistor N2 and N4 are off while N3 and P1 are on. On the rising edge of the clock, the flip-flop enters the evaluation phase. Here, two periods are distinguished. In the first period, the pulse is active and the circuit is in the sampling (or transparent) mode. At this moment, the transistors N2 and N4 turn on while N3 stays on for three inverter delays. The value of output Q is determined by the value of input D. Once internal node X is discharged, due to its precharge nature, it will stay low until the next clock cycle. In the second period, the pulse is inactive. The sampling of D is disabled, so X and Q will retain the values they acquired during the sampling period. Notice that any subsequent change at D after the sampling period will have no effect on Q.

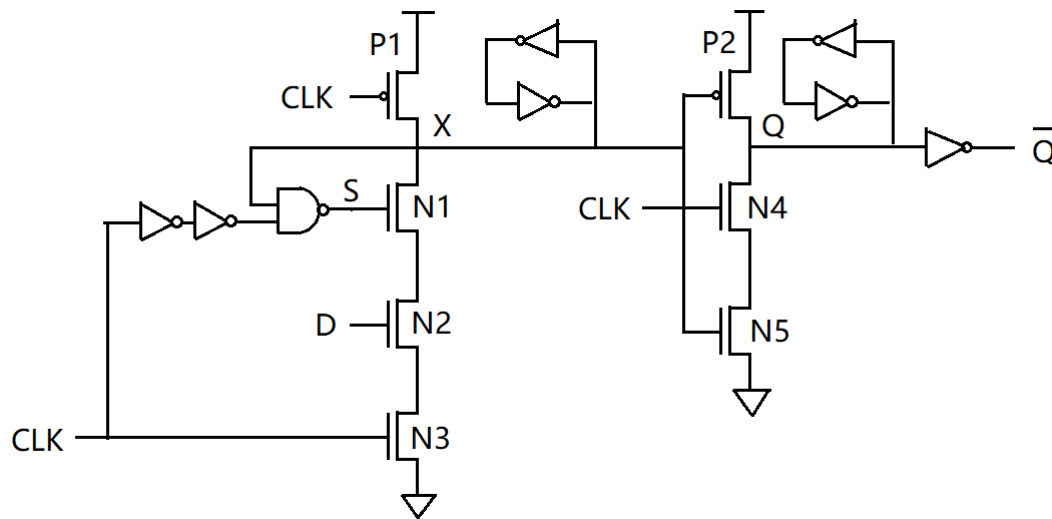


**Figure 1.** Implicit-pulsed semi-dynamic hybrid flip-flop (ip-DCO)

### b. Semi-Dynamic Flip-Flop (SDFF)

As figure 2 shows, when the clock is low, the flip-flop is in the precharge phase. Node X is precharged to VDD, and node Q holds its previous value. On the rising edge of the clock, the flip-flop enters the evaluation phase. Here, two periods are distinguished. In the first period, the pulse is active and the circuit is in the sampling (or transparent) mode. The value of output Q is determined by the value of input D. Once internal node X is discharged, due to its precharge nature, it will stay low until the next clock cycle. In the second period, the pulse is inactive. The sampling of D is disabled, so X and Q

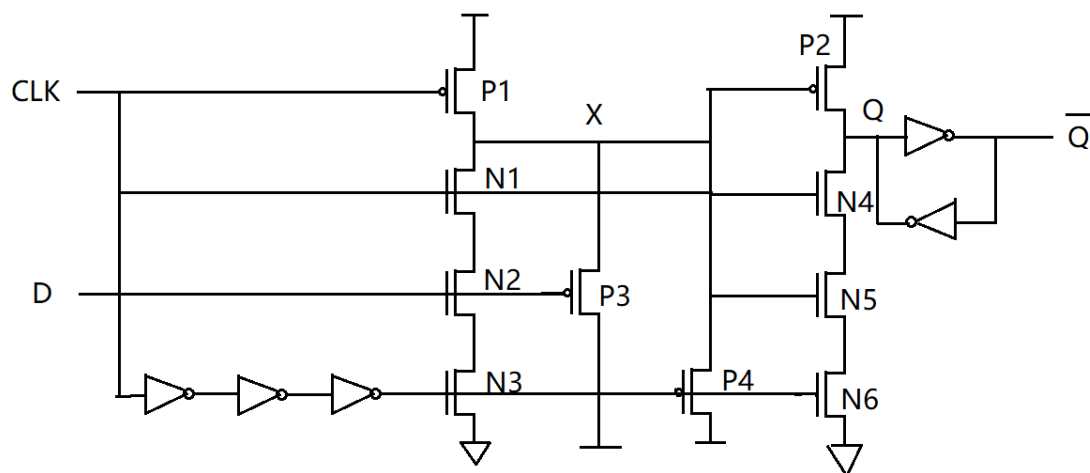
will retain the values they acquired during the sampling period. Notice that any subsequent change at D after the sampling period will have no effect on Q.



**Figure 2.** Semi-dynamic edge-triggered flip-flop (SDFF)

### c. Hybrid Latch Flip-Flop (HLFF)

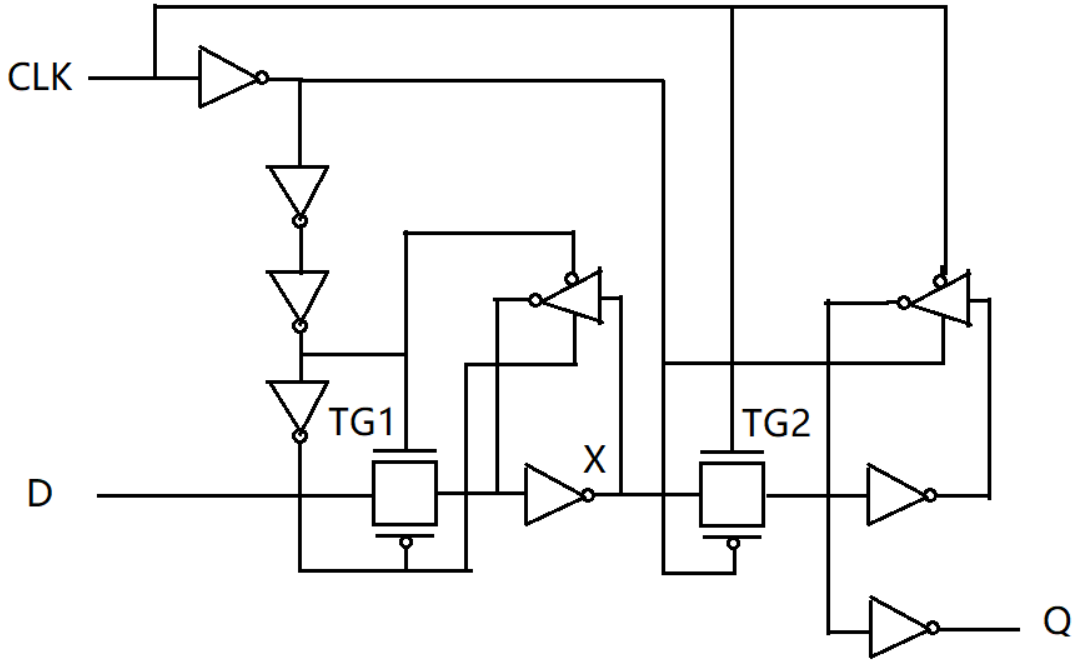
Figure 3 shows the basic construction of HLFF. Before the rising edge of the clock, the node X precharged to VDD and node Q holds the previous data, since the transistor N1 and N4 are off while N3, N6, and P1 are on. At the rising edge of the clock, the transistor N1 and N4 turn on while N3 and N6 stay on for three inverter delays. During this period the flip-flop is transparent and the data is sampled into the latch. When the transition of CKDB is low, the node X is decoupled from D, either it stays in that logic or begins to precharge to VDD by P4. The node X is completely precharged to hold the value of X to VDD at the negative edge of the clock.



**Figure 3.** Hybrid Latch Flip-Flop (HLFF)

#### d. Time-borrowing master-slave (tb-SMS)

This type of flip-flops samples the data either at the positive edge or negative edge of the clock. This conventional flip-flop is constructed based on master and slave latches. In this configuration the output of the master latch is the input of the slave latch, and the output of the slave latch provides the output of the flip-flop. when the clock is low or negative edge, TG2 is off while the master stage a transmission gate TG1 is incorporated to receive the data input D. At the rising edge of the clock, TG1 is off while the slave stage a transmission gate TG2 is on. The value of output Q is determined by the value of node X.



**Figure 4.** Time-borrowing master-slave (tb-SMS)

### III. Comparisons

An implicit-pulsed, data-close-to-output, semi-dynamic hybrid flip-flop (ip-DCO, schematic in Figure 1) is compared with three other previously reported implicit-pulsed, Semi-dynamic edge-triggered flip-flop (SDFF), Hybrid Latch Flip-Flop (HLFF), and Time-borrowing master-slave (tb-SMS). The energy vs. delay characteristics of these four semi-dynamic flops is shown in Figure 5, while Figure 6 plots the energy\*delay product ( $E \cdot D$ ) as a function of delay. Figure 7 summarizes the comparison in terms of D-Q delay, minimum  $E \cdot D$  product point, total device width, and total energy. For an equal energy per cycle of 20fJ, ip-DCO offers 37% ~ 43.11% better D-Q delay than tb-SMS, HLFF, and SDFF. However, the classic static master slave Flip-Flop tb-SMS is the most energy-efficient among these four. It provides 9% ~ 48.39% better minimum

$E \cdot D$  value than ip-DCO, HLFF, and SDFF. And tb-SMS consumes 32% ~ 48.01% smaller energy than the others at a target D-Q delay of 70ps. The reason is ip-DCO, HLFF, and SDFF are dynamic Flip-Flop, the circuit will consume heavy power in the precharge phase. On the other hand, tb-SMS is static circuit.

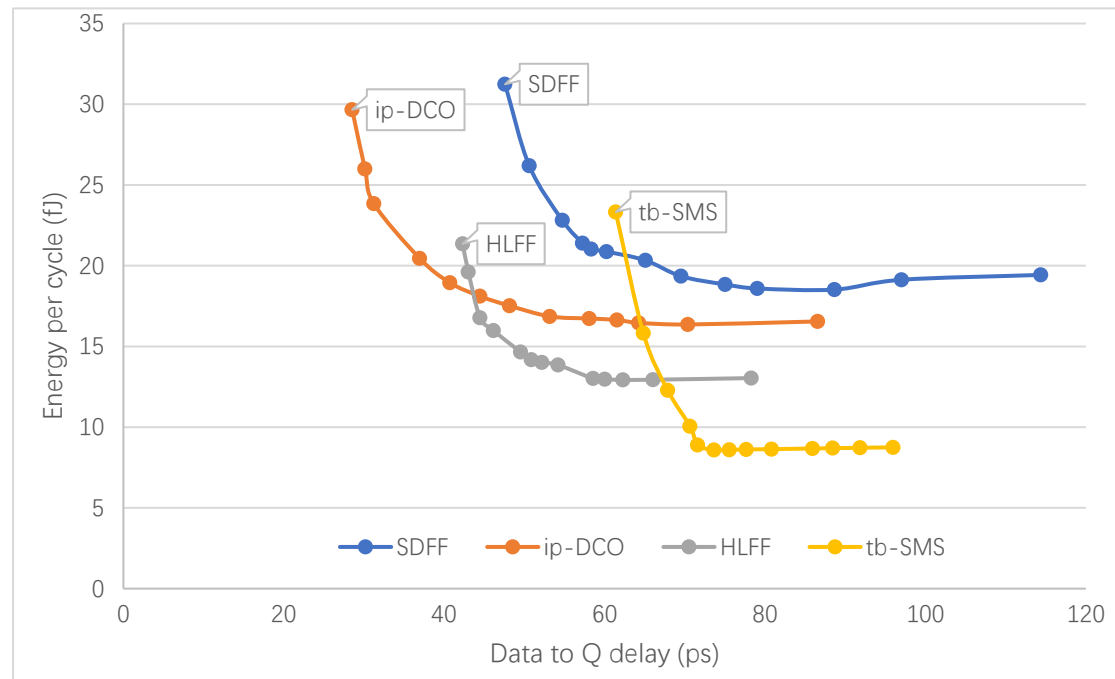


Figure 5. Energy vs. delay.

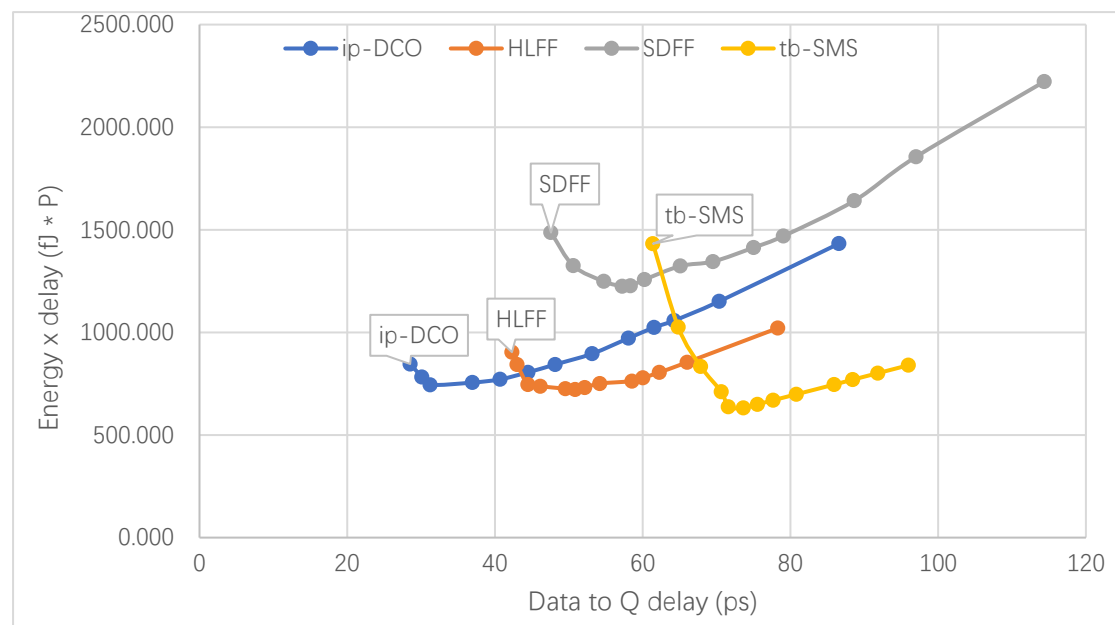


Figure 6. Energy\*delay product.

	% D-Q	% E*D	% total W	% total E
SDFF	ref	ref	ref	ref
ip-DCO	43.11% better	39.23% better	43.21% better	15.45% better
HLFF	35.23% better	41.11% better	40.12% better	32.09% better
tb-SMS	5.83% better	48.39% better	59.26% better	48.01% better

Figure 7. Comparison of D-Q delay @ E/cycle of 20fJ, min E\*D, and total W, total E @ D-Q of 60ps.

## IV. Conclusion

Based on figures 5 to 7, it is not hard to answer the questions below.

Among all the above flip-flops which one is the fastest? The ip-DCO is the fastest. Is the fastest design most energy efficient? No. The most energy efficient is tb-SMS. Which one you should use in high-speed operation? The ip-DCO should be used in high-speed operation. Which one should be used for majority of the data paths? The tb-SMS should be used for majority of the data paths. Because they are energy efficient.

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