Dual Edge Triggered Flip-Flops for Noise Blocking and Application to Signal Delay Detection

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Abstract— **Conventional edge triggered flip-flops sample a data signal synchronizing with single clock edge. If a noise signal occurs around the clock edge, flip-flops result in malfunction. Then, we have proposed dual edge triggered flip-flops to solve this problem. The flip-flop has highly ability to prevent sampling a noise signal on a data line because it samples the data signal synchronizing with both of the rising edge and the falling edge. In this paper, we design a new circuit of the dual edge triggered flip-flops to improve circuit size, power consumption, and operation speed. In addition, we apply the dual edge triggered flip-flops to signal delay detection.**

Keywords-edge triggered flip-flops; clock edge; data line; noise; synchronous circuits; signal delay;

I. INTRODUCTION

In very deep submicron technology of CMOS process, noise caused by energy particles and signal transition affects circuit operation. Temporary errors caused by single event transient (SET) become a serious problem [1]. As the voltage pulse width caused by SET becomes wider, the occurrence probability of the logic error in the circuit becomes higher. Also, as the operating frequency becomes higher, probability to sample the SET pulse by flip-flops (FFs) will be higher. Furthermore, single event (SE) causes the crosstalk noise [2]. As the supply voltage becomes lower, effects of SE are more remarkable and the crosstalk noise pulse becomes wider. These signal noises cause the transient voltage pulse, and the circuit will result in malfunction if the noise pulse is propagated through the circuit as an erroneous logical value [3]. In this paper, we aim to prevent effects of the noise pulse (voltage pulse) caused by various noise sources on the data signal line. We target edge triggered flip-flops (ET-FFs) synchronizing with the clock signal of the pulse type.

Space redundancy and time redundancy [4]-[8] are often used to prevent noise effects. Space redundancy needs two or more same circuits. This method samples the data signal with two or more flip-flops. Sampled data are compared each other and the noise signal is detected. This method accompanies area overhead of circuits. The time redundancy method samples the data signal several times at different timing by changing data feeding timing or clock timing. The noise signal is detected by the comparator. However, the noise pulse wider than the sampling interval is not detected because the noise signal is sampled at several times. On the hand, noise reduction methods have been proposed [9], [10]. The amplitude of the noise signal is reduced by mask effect or filter effect, but these methods have problems of a signal propagate speed and an area overhead.

We have proposed the dependable ET-FF which can block the transient noise pulse on the data signal line [11]. There are two clock edges of rising and falling edges in one clock cycle. Sampling the data signal at both edges can prevent to sample the transient noise pulse, FFs can block the noise signal. We call this kind of ET-FFs dual edge triggered flip-flops (DET-FFs). DET-FF can adjust the noise pulse width to be blocked by changing the clock pulse width.

Moreover, effects caused by signal delay have become a serious problem in very deep submicron technology [12]. The circuit results in malfunction if the circuit samples an incorrect value caused by signal delay and its value propagates to the circuit output. In this paper, we extend the DET-FF function to detect and correct signal delay by path delay faults and transition delay faults [13], [14].

Razor FF [15] and Canary FF [16] are proposed to detect timing error. In Razor FF, the clock signal applied to the shadow latch is delayed than that of the main FF and timing errors are detected by the comparator. If the timing error is detected at the main FF, the value of the main FF is recovered by the correct value in the shadow latch incurring one clock cycle penalty. Depending on occurrence frequency of the timing error, the operating voltage is controlled by the DVS system to optimize operation. Canary FF detects timing error by the comparator and needs the delay element in the data signal line. The main FF can predict the timing error since Canary FF encounters the timing error before the main FF. If Canary FF encounters the timing error, the error is prevented since the operating voltage is controlled by the DVS system to optimize operation. However, these methods accompany area over head because of circuit replication. In this paper, we proposed a method of signal delay detection and correction at real time (i.e., processing for detection/correction is carried out within the same clock cycle as delay occurrence) without voltage control.

This paper is organized as follows. Section 2 explains the outline of DET-FF. Section 3 shows the circuit structure of a newly designed DET-FF. Section 4 compares and evaluates new DET-FF and other ET-FFs. Section 5 explains application to signal delay detection. Section 6 describes consideration

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about application to signal delay detection. Finally, Section 7 concludes this paper.

II. OUTLINE OF DET-FF

This paper targets ET-FFs and transient voltage pulses caused by various noise sources (SET, crosstalk) on the data signal line. The purpose of DET-FF is to prevent sampling the transient noise pulse as a correct data signal at the clock edge. We assume the clock signal of the positive pulse, in this paper. Hence, the clock signal is the pulse signal which has the falling edge after the rising edge in one cycle. The data signal and the noise pulse are the positive logic and the positive pulse, respectively. The proposed method can apply to the negative logic and the negative pulse.

Signal noise occurs incidentally in the circuit and the system, and it generates the transient voltage pulse on the data signal line. Noise source exists widely inside and outside of circuits and systems. Generally, we do not have a method to predict the occurrence of the noise with accuracy. Hence, it is difficult to predict and prevent the occurrence of the noise. There are studies of a VLSI layout method to prevent and reduce the occurrence of the noise. However, perfect noise elimination is difficult because of various noise sources. As we consider that noise occurs incidentally, we consider that reasonable measures against the noise are preventing effects of the noise at the circuit level, not preventing noise occurrence itself.

The conventional ET-FF samples data signal synchronizing with single clock edge. Therefore, if a noise signal occurs around the clock edge, ET-FF results in malfunction since ET-FF samples the noise pulse and outputs an incorrect value. By comparing data signal values sampled at multiple times, it is possible to distinguish the correct data signal from the noise pulse. As a result, we can prevent that FF samples the incorrect data value. The clock signal has two clock edges of rising and falling in one cycle. We have proposed DET-FF which samples the data signal synchronizing with two clock edges of rising and falling.

DET-FF judges the sampled data signal the correct data when values sampled by two edges are equal (Fig. 1: (1), (2)). On the other hand, DET-FF judges the sampled data signal the noise pulse and keeps a previous output value when values sampled by two edges are not equal (Fig. 1: (3),(4)). Moreover, DET-FF outputs a warning signal W when DET-FF judges the sampled data signal the noise pulse. Table 1 shows the DET-FF functions. States (1), and (2) in the table mean that DET-FF samples the correct data signal. In this case, DET-FF outputs and keeps the sampled value of data signal (Table 1: (1), (2)). For the other cases, DET-FF keeps the previous value because of the noise pulse (Table 1: (3), (4)) or the hold state (Table 1: (hold)).

III. CIRCUIT STRUCTURE OF NEWLY PROPOSED DET-FF

DET-FF had a problem of area overhead because we used the 1st stage of the conventional ET-FF to sample data signal in previously proposed DET-FF (DET-FF_1) [11]. Then, we implement a newly DET-FF (DET-FF_2) to improve a circuit size. Figure 2 shows its circuit structure and Fig. 3 shows the warning circuit of DET-FF_2. The part surrounded by the dotted line in Fig. 2 is an improved data sampling part. We use transmission gates to make the circuit size smaller. C-element compares the signal at S1 sampled at the rising edge with the signal at S2 sampled at the falling edge. We applied the clock signal in C-element. The output of DET-FF must synchronize with the falling clock edge. If the clock signal is not applied to C-element, the value of S2, that is the previous cycle's value and the value of S1, which is the present cycle's value are inputted to C-element. Therefore, it is possible to cause a problem that the output 'Q' changes synchronizing with the rising edge.

The warning circuit in Fig. 3 outputs the warning signal 'W' if values of S1 and S2 are not equal. The warning circuit must output the signal after the value of S2 is fixed because the warning circuit outputs the warning signal by comparing S1 with S2. Therefore, we used the delayed clock signal 'Cd' in the warning circuit so that the warning circuit outputs the signal after the value of S2 was fixed. And we applied the delayed clock signal in the warning circuit because we prevent comparing the value of S2, that is the previous cycle's value and the value of S1, that is the present cycle's value.

IV. COMPARISON AND EVALUATION

We verified performances of following four FFs on circuit simulation using parameters of 1.8V-0.18μm. Four FFs are DET-FF_2, DET-FF_1, a circuit which has the DET-FF function realized by combining two conventional ET-FF (combined circuit), Canary FF. We verified performance of DET-FF_2 under process variations of the threshold voltage and the transistor size from -30% to +30%. DET-FF_2 showed an incorrect response in case of the transistor size of -30% because the input signal to the C-element is delayed. However, this problem is solved by delaying the clock signal supplied to the C-element.

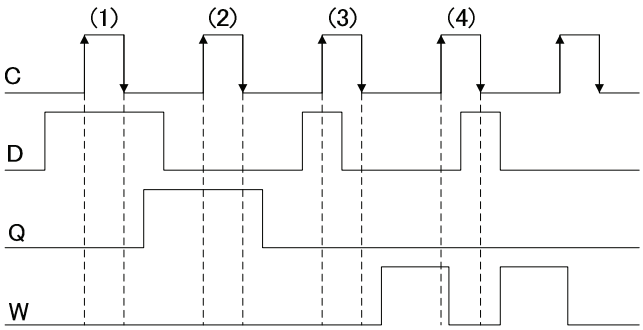

Figure 1. Operation of DET-FF

TABLE I. SATATE TABLE

State	1st-edge		2nd-edge		Output		W
	C	D	C	D	Q	QB	
(1)	↑	1	↓	1	1	0	0
(2)	↑	0	↓	0	0	1	0
(3)	↑	1	↓	0	No change		1
(4)	↑	0	↓	1	No change		1
(hold)	↓	X	↑	X	No change		0
(hold)	0	X	0	X	No change		0
(hold)	1	X	1	X	No change		0

X = {0, 1}

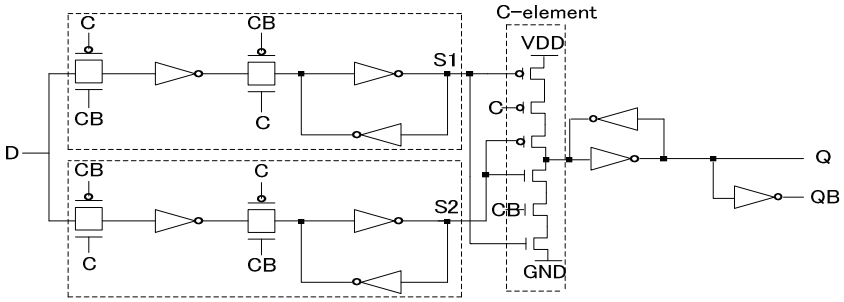

Figure 2. DET-FF_2

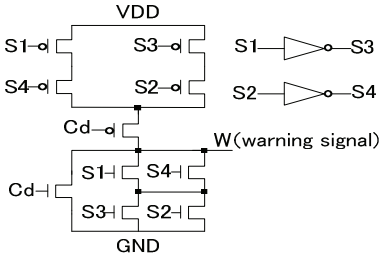

Figure 3. Warning circuit

TABLE II. AC CHARACERISTICS AND NOISE CHARACTERISTICS

			DET-FF_2 proposed	DET-FF_1	Combined	Canary FF	Conventional FF positive	Conventional FF negative
# transistors (FF body)			32	60	84	52	26	26
# transistors (warning)			10	12	16	6	-	-
minimum clock pulse width	tw	[ns]	0.185	0.351	0.358	-	-	-
setup time	tsu	[ns]	0.123	0.019	0.025	0.024(+Δ)	0.025	0.100
hold time	th	[ns]	-0.036	0.106	0.048	-0.005	-0.004	0.048
propagation delay of Q	tpQ	[ns]	0.363	0.493	0.701	0.271	0.241	0.245
energy	E	[pW]	2.922(1.775)	3.120	3.264(1.319)	0.582(+Δ)	0.271	0.724
ED product	ED	[pW･ns]	1.061(0.644)	1.538	2.288(0.924)	0.158	0.065	0.177
propagation delay of warning	tpW	[ns]	0.472	0.474	0.502	0.350	-	-
minimum noise width	twn	[ns]	0.168	0.231	0.171	depend on Δ	-	-
minimum noise amplitude	Vn	[V]	1.131	1.008	1.009	-	-	-

Δ depends on delay elements

A. Circuits Size

We proposed DET-FF_2 of Fig. 2 in order to make circuit size smaller than DET-FF_1 that consists of 60 transistors. DET-FF_2 consists of 32 transistors. We could make the circuit size smaller by improving the data sampling part since DET-FF_1 consists of 60 transistors. The DET-FF_2 size was improved by 47% (=28/60). The combined circuit consists of 84 transistors and Canary FF consists of 52 transistors. Moreover, both of them require delay elements.

B. Performance

Table 2 shows AC characteristics and noise characteristics. Responses of DET-FF are different depending on the type of the noise pulse and the generation timing of the noise pulse. Table 2 also shows power consumption and energy delay (ED) product which include power consumption of the delay element and the delay clock generation. Values in parenthesis ( ) do not include power consumption of the delay elements and the delay clock generation.

The noise pulse width blocked by DET-FF depends on the clock pulse width 'tw'. For instance, for tw=0.185 ns, DET-FF can block the noise pulse from 0.168 ns to 0.185 ns (+tsu+th) and then the blocked noise pulse width is adjusted by the clock pulse width. Figure 4 shows the relationship of the clock pulse width and the blocked noise pulse width. We find that the noise pulse width blocked by DET-FF is proportional to the clock pulse width.

The minimum operating period 'T' of DET-FF_2 is calculated as follows; T=tw+tsu+max(th,tpQ,tpW)=0.185 ns+0.123 ns+0.472 ns=0.780 ns. Therefore, the maximum operating frequency of DET-FF_2 itself is approximately 1.282 GHz. DET-FF_2 carried out speed up because the maximum operating frequency of DET-FF_1 is approximately 892MHz. DET-FF_2 was speeded up by 30%(=390/1282).

The power consumption of DET-FF_1 is 3.120 pW. On the other hand, DET-FF_2 is 2.922 pW. As the power consumption of DET-FF_2 includes the power of the delay clock generation, DET-FF_2 is the lower power consumption. The power consumption of DET-FF_2 was reduced by 6%(=0.198/3.120) (43%=(1.345/3.120)). The ED product indicates performance of a circuit from the viewpoint of speed and power. The ED product represents the product of the propagation delay of output and the power consumption per one cycle, in this paper. From Table 2, the ED product of DET-FF_2 is 1.061 pW･ns and DET-FF_1 is 1.538 pW･ns. DET-FF_2 is superior to DET-FF_1 for ED product. The combined circuit is globally inferior to both of DET-FFs. For the application of DET-FF to signal delay detection and correction, we verified that DET-FF can correct signal delay effects.

Though Canary FF is superior to DET-FF for AC characteristics, its function is only to predict timing error, it cannot prevent effects of error itself. Thus, as Canary FF has different purpose with DET-FF, we cannot simply compare performances of those FFs.

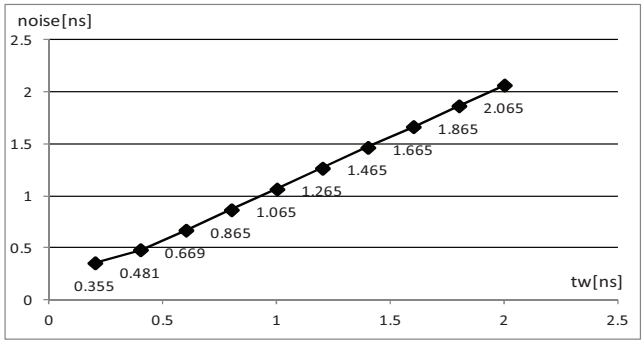

Figure 4. Relationship of the clock pulse width and the blocked noise width

V. APPLICATION TO SIGNAL DELAY DETECTION

In this section, we explain application to signal delay detection and correction by extending the function of DET-FF. Originally, though we have proposed DET-FF in order to block noise effects, in this section, we consider the application of DET-FF by extending its function in order to detect signal delay and correct signal delay. Note that we assume the environment without noise generation in this section. DET-FF can detect signal delay itself because DET-FF outputs the warning signal when signal values sampled at the rising edge and the falling edge are not equal. Then, the output 'Q' of DET-FF keeps previous value (Fig. 5). The output value is always kept just one clock cycle after data mismatching. Hence, we consider even if signal delay occurs during two edges, the delay can be corrected by adding the function to inverse forcibly the output value of DET-FF. Signal delay caused by path delay faults and transition delay faults are the object in this paper. Moreover, we treat both of increasing delay (Fig. 5 D_inc) and decreasing delay (Fig. 5 D_dec).

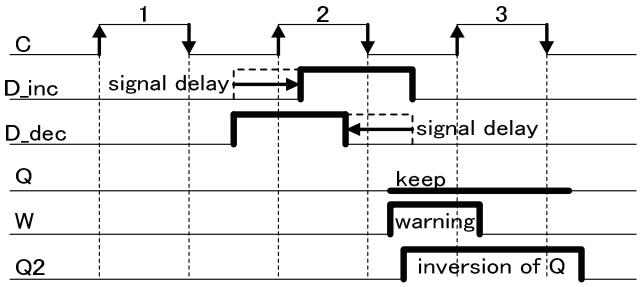

Figure 5. Example of application to signal delay

Figure 5 shows the example of the basic operation of application to signal delay. When signal delay occurs at data signal of 2nd clock signal, the output 'Q' of DET-FF keeps a previous value because values sampled at the rising edge and the falling edge are different each other (D_a and D_b). Then, DET-FF detects signal delay by outputting the warning signal 'W'. At this time, inverting the output value of Q, the delayed signal is corrected (Q2 output).

Figure 6 shows a DET-FF circuit applied to signal delay. We added an XOR circuit of Fig. 7 in order to implement the function which makes the output value inverse by using the warning signal. The XOR circuit is a comparator and is fed by Q and W. The transmission gate using the delayed clock is added into the XOR in order to prevent that the value of Q is propagated directly to Q2 when the clock signal is a high level and the warning signal is low level. At this time, however, Q2 should be inverted originally (Fig. 8(a)). If there is no transmission gate, the Q value propagates to the Q2 output directly (Fig. 8(b)). Thus, the transmission gate is added. This problem occurs because the warning signal is synchronizing with the rising edge. The keeper circuit is added at the output of the XOR in order to keep the value of Q2 because Q2 becomes a high impedance state when the delayed clock signal is a high level and the warning signal is a low level (i.e., two transmission gates turn off and Q cannot propagate anywhere).

We verified the circuit functions of Fig. 6 on circuit simulation (Fig. 9). Areas (n1), (n2), and (n3) are corresponding to area (n) which is the correct data signal of a high level. In area (n1), the value of Q is a high level. In area (n2), the value of W is a low level. In area (n3), Q2 is a high level. So, Q2 is correct output.

In area (s), we assume the data signal with increasing delay (i.e., the slow transition faults from low to high or the path delay fault). Areas (s1), (s2), and (s3), are corresponding to area (s). In area (s1), the value of Q is a low level, which means DET-FF keeps the previous value. Since the value of W is a high level in area (s2), Q2 becomes a high level because Q2 is inverted by the high level signal of W. Thus, the circuit of Fig. 6 can correct the effects of data signal delay.

Similarly, we assume the data signal with decreasing delay in area (f) (i.e., the fast transition fault from high to low). Areas (f1), (f2), and (f3), are corresponding to area (f). In area (f1), the value of Q is a low level. Since, the value of W is a high level in area (f2), Q2 becomes a high level, which is inverted by the signal W. Thus, the decreasing delay signal is also corrected by the circuit of Fig. 6.

As shows here, if there is the delay fault, a circuit cannot catch the correct data and outputs an erroneous value (e.g., Q of Fig. 9). It is possible that the proposed method can output the correct value because of signal correction (e.g., Q2 of Fig. 9). Note that the proposed method cause delay time Δ for data processing. However, by using the corrected output Q2 instead of Q, relative signal change is the same as the original data signal.

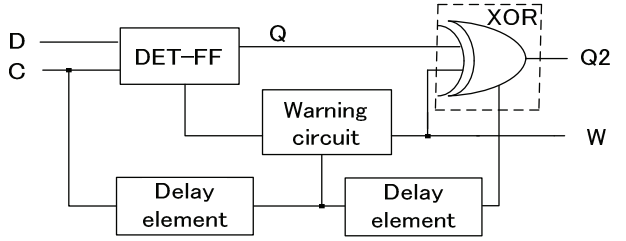

Figure 6. The circuit applied to signal delay

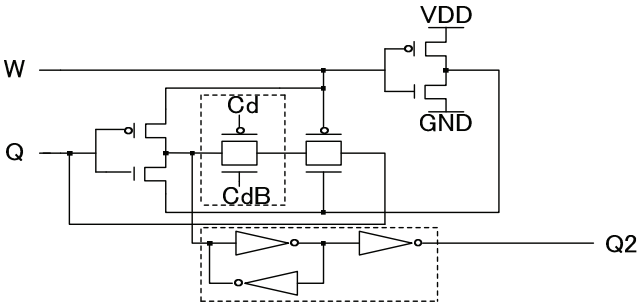

Figure 7. XOR circuit

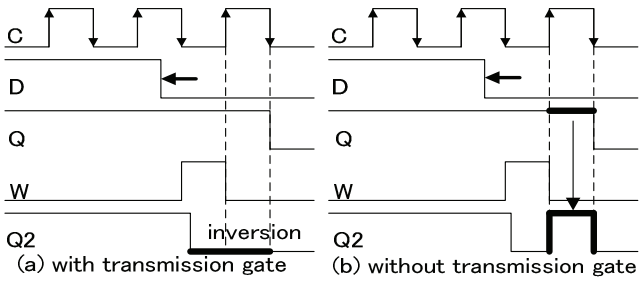

Figure 8. Timing chart of Q2 output

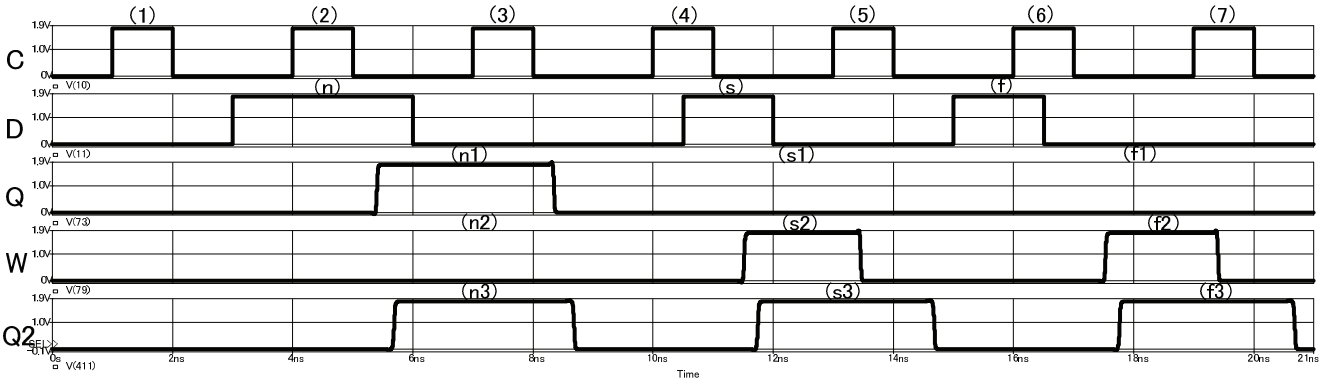

Figure 9. Simuration results

TABLE III. AC CHARACTERISTICS

			proposed	Razor	Canary
# transistors *			56	62	46
minimum clock pulse width	tw	[ns]	0.185	0.140	0.144
setup time	tsu	[ns]	0.121	0.151	0.092
hold time	th	[ns]	-0.064	-0.068	-0.026
propagation delay of Q	tpQ	[ns]	0.430	0.280	0.254
propagation delay of warning	tpW	[ns]	0.545	0.355	0.291
propagation delay of Q2	tpQ2	[ns]	0.767	-	-
propagation delay of Q2(correct)	tpQ2	[ns]	0.801	next cycle	-
energy *	E	[pW]	2.084	1.879	1.516
ED product *	E・tpQ	[pW・ns]	0.896	0.526	0.385
function	delay detection		✓	✓	✓
	signal correrction		✓	✓	non

* exclude delay elements and the delayed clock circuit

VI. CONSIDERATION OF SIGNAL DELAY DETECTION

In this section, we discuss application to signal delay detection.

A. Evaluation of Performance

We verified performances of the circuit which has the function of signal delay detection/correction on circuit simulation using parameters of 1.8V-0.18μm. Table 3 shows their AC characteristics and compares performances with Razor FF and Canary FF which are implemented by the master-slave FF. Responses of the circuit are different depending on types of signal delay and timing. When the circuit corrects signal delay, tpQ2 is 0.801 ns. On the other hand, when the circuit does not correct the data signal, tpQ2 is 0.767 ns. The value of tpQ2 increases a little by 34 ps that corresponds to the processing time for signal correction. Values in Table3 are values excluding power consumed by the delay element and the delay clock generation. Razor FF and Canary FF are superior to the proposed circuit in operation speed and energy but the proposed circuit can only correct signal delay at the present clock cycle.

The range of signal delay which DET-FF can detect and correct is adjusted by changing the clock pulse width. We assume that delay from setup time (tsu) of the rising edge is ΔD1. The range of signal delay which DET-FF can detect and correct is tsu<ΔD1<(tw-falling_su) because DET-FF detects and corrects the data signal changing between the rising edge and the falling edge (Fig. 10 (a)). Similarly, assuming that delay from the hold time (th) of the falling edge is ΔD2. The range of signal delay which DET-FF can detect and correct is th<ΔD2<(tw-rising_h) because the data signal changes between the rising edge and the falling edge (Fig. 10 (b)).

Figure 11 shows the relationship of the clock pulse width and the maximum range of signal delay which DET-FF can detect and correct. We find that range of signal delay which DET-FF can detect and correct is proportional to the clock pulse width.

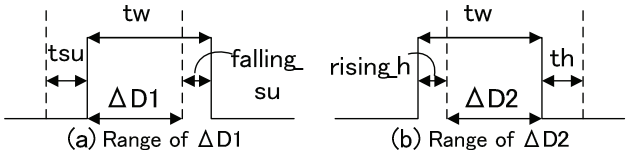

Figure 10. Range of ΔD1 and ΔD2

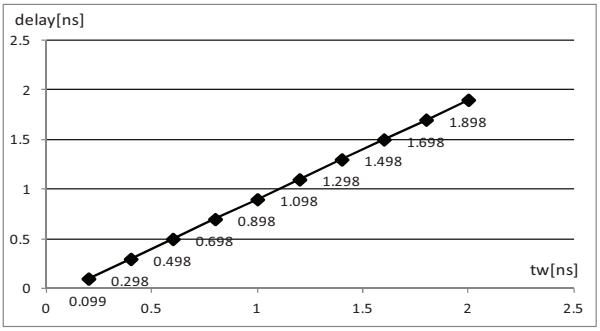

Figure 11. Relationship of the clock pulse width and the detected/corrected signal delay range

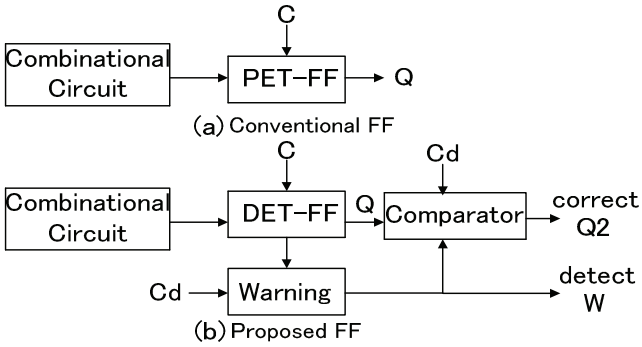

Figure 12. Circuit models

B. Evaluation of Penalty

DET-FF which has the function of delay detection and correction constantly makes propagation delay increase as a penalty, than conventional ET-FFs. Propagation delay of the conventional positive ET-FF is tpQ in Fig. 12 (a). This propagation delay corresponds to the time of output transitions from the rising edge of the clock signal. On the other hand, propagation delay of DET-FF which has function of delay detection and correction is tpQ2 in Fig. 12 (b). This propagation delay corresponds to the time of output transitions from the falling edge of the clock signal. This delay is calculated as follows; (processing time of DET-FF + processing time of the warning circuit + processing time of the comparator)=0.430 ns+0.115 ns+0.256 ns=0.801 ns. In this section, we assume the conventional positive ET-FF. Therefore, penalty of delay time of DET-FF is (tpQ2- tpQ)+tw=(0.801 ns-0.241 ns)+tw=0.560 ns+tw. The relative signal transition is same as the circuit in Fig. 11(a) but DET-FF always generates propagation delay of 0.560 ns.

C. Detection of Setup and Hold Violation

In this paper, we proposed the application of DET-FF to detection and correction of signal delay caused by path delay faults and transition delay faults. As shown in Fig. 13, setting the additional clock signal for DET-FF to the setup time and/or the hold time of the conventional ET-FF, the proposed circuit will detect and correct timing violation of the data signal for the conventional ET-FF. However, we need to generate another clock signal for DET-FF.

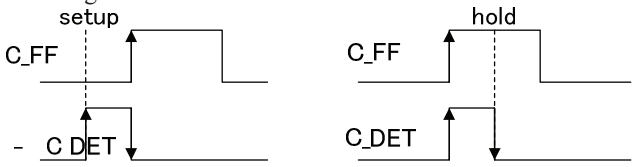

Figure 13. Example of clock timing for detecton of setup and hold violation

VII. CONCLUSION

In this paper, we proposed the new circuit structure of DET-FF which can block the noise pulse by utilizing two clock edges in one clock cycle and considered application to signal delay by extending the function of DET-FF.

We improved the sampling part of the previous DET-FF. As a result, size of DET-FF was improved by 47%. Moreover, we could improve power consumption by 6%(43%) and operation speed by 30%. For the application of DET-FF to signal delay detection and correction, we verified that DET-FF can correct signal delay effects. However, DET-FF requires the data signal with an enough width as a correct data signal.

We consider applying the similar dependable method for other types of FFs in future works. Moreover, we need to consider a highly reliable method targeting both of noise blocking and signal delay detection.

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