## C 1541   Service Manual

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### Product Specification

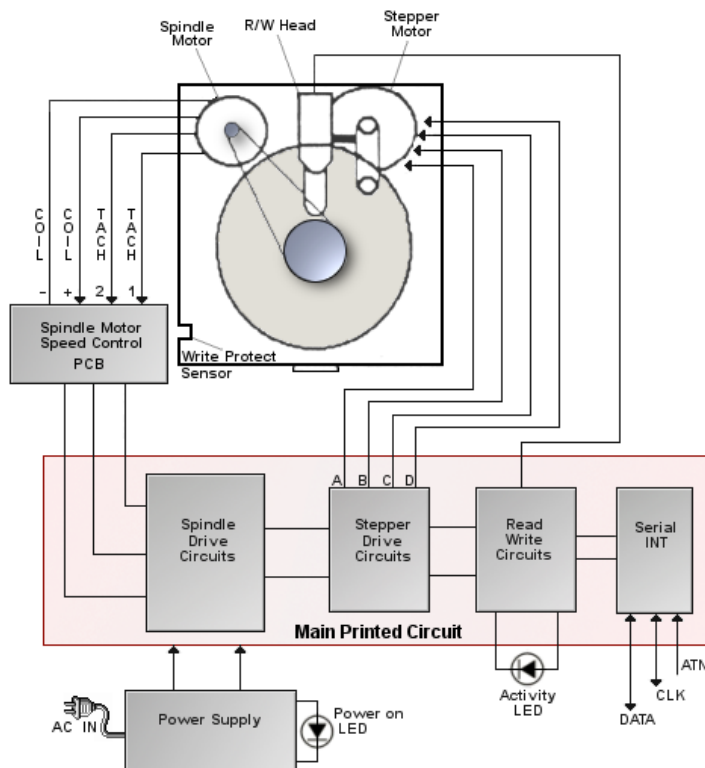| | |
|---|---|
| General Description: | The C1541 Disk Drive is an external 5-¹/₄ inch floppy diskette recorder, offering high-speed and capacity for programs and data. It is an intelligent device, containing its own microprocessor, RAM, ROM and operating systems software for faster speed of throughput and memory efficiency in the computer |
| Maximum Storage: | 170K of data (formatted) - 35 tracks |
| Media: | 5-1/4 Inch floppy disk. Single sided, single density, soft sectored (double density can be used, but not needed) |
| Input/Output: | Commodore serial interface<br>Second serial port for chaining a second drive or printer |
| Controller: | MOS 6502 microprocessor - 1 MHz clock |
| Memory: | 2K RAM, 16K ROM |
| Data Transfer Rate: | 400 Bytes/sec |
| File Types: | Program, sequential, relative, random-access and user |
| Number of Files: | Up to 144 different files per diskette |
| Computers: | C64, VIC 20, SX64, Educator 64, Plus/4, C16 |
| Media Compatibility: | 2031, 4040, C1551, C1571 |
| Power Requirements: | 120 Volts AC, 60Hz - integral power supply with external 1 Amp fuse |
| Power Consumption: | 30 Watts maximum |

### Block Diagramm

Spindle Motor    R/W Head    Stepper Motor

C O I L −   C O I L +   T A C H 2   T A C H 1

Spindle Motor Speed Control PCB

Write Protect Sensor

A B C D

Spindle Drive Circuits    Stepper Drive Circuits    Read Write Circuits    Serial INT

**Main Printed Circuit**

AC IN   Power Supply   Power on LED

Activity LED

ATN
CLK
DATA

**Care and Maintenance**

- DO NOT use MAGNETIZED tools when repairing or adjusting a disk drive.
- DO NOT place a disk drive near any device which generates "noise" e.g., - motors, radios televisions.
- DO NOT stack drives upon each other or in any way inhibit air flow around the unit. HEAT BUILD-UP can cause disk failures.
- Periodically CLEAN the read/write head with 90% isopropyl alcohol and a cotton swab. CHECK load pad for excess wear. Clean or replace as necessary.
- Take the following precautions when handling a diskette:
  ALWAYS store a diskette in its jacket.
  Use ONLY felt-tip pens when writing on the label of a diskette.
  Do not bend or physically damage a diskette.
  Do not place a diskette in the area of a magnetic field.
  Do not attempt to clean a diskette.
  Do not touch the exposed area of a diskette.
- DIAGNOSTIC and ADJUSTMENT procedures are outlined in detail on the diagnostic disk (Commodore Part #31405101). A manual has been added to the diagnostic package. It contain descriptions of testing procedures and adjustment methods.

**Overview**

The drive itself an independent memory device. THe drive is composed of a media clamp rotating mechanism, a head positioning mechanism and an eject mechanism. All positioning operations, excluding insertion and removal of diskettes, are controlled by the internal guide mechanism. Closing the front door causes the media clamp mechanism to operate. Two operations are performed in the following order:

a) The diskette is centered.
b) The diskette is clamped and retained between the spindle and the hub.

The spindle and hub rotates at 300 r.p.m. through a closed/loop control circuit employing a D.C motor/tachometer. It is important that the relationship between the head and the media is maintained correctly during operation. For this purpose, a pressure pad is used to hold and press down the media (about 12g) from the opposite side of the head. This head assembly is coupled by a metal band to a four base stepping motor which performs the track positioning. One step of the stepping motor corresponds to a 1/2 track movement. The control circuit on the logic board selects the direction and number of steps to the desired track.

The Read/Write head uses a glass-bonded, ferrite/ceramic head. Track-to-track erasing is accomplished by the straddle erase method. The surface of the Read/Write head is mirror-ground to minimize wear of the head and media. Also, the head is designed in such a way that the maximum signal can be obtained from the media surface.

The spindle drive motor operates on 12 VDC and turns the spindle, through a belt drive, at 300 revolutions per minute. The speed of the drive motor is controlled by a feedback signal from a tachometer, which is housed in the drive motor assembly. The feedback signal controls a servo amp that supplies the 12 VDC drive current.

**Flash Code**

The 1541, upon power-up, goes through its own internal diagnostic. If an electronic problem is detected, it's indicated by flash code. The led's will blink a number of times, pause, and then flash again until the problem is corrected.

| Number of flashes | Possible failure |
|---|---|
| 2 | Zero page |
| 3,4 | DOS ROM's |
| 5,6,7,8 | RAM |

Circuitry associated with these components can also cause the failure code. Therefore, it should be suspected as the next possible defect.

**Circuit Theory**

The Power Supply
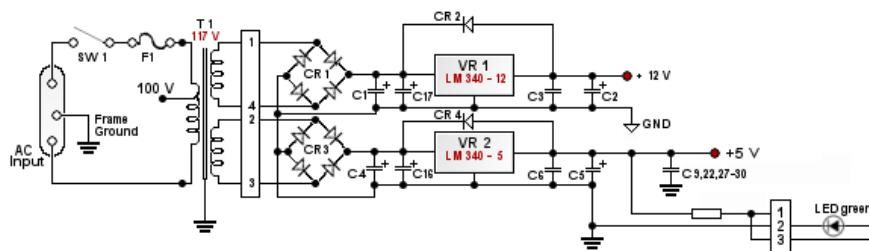


The input AC voltage is controlled by switch 1 (SW1). Disk circuit protection is provided by fuse 1 (F1). If SW1 is closed, the AC voltage input is applied to the primary winding of transformer one (T1). T1 steps down th AC input voltage into two smaller AC voltages. The top secondary AC output (approx. 16VRMS) is converted to DC by the Full Wave Bridge Rectifier CR1. The DC output of CR1 is regulated at 12VDC by VR1. The bottom secondary AC output of T1 (approx. 9VRMS) is converted to DC by the Full Wave Rectifier CR3. The DC output of CR3 is regulated at +5VDC by VR2. High frequency filtering is provided by C1 and C3 for the 12VDC supply, and C4, C6 to C9, C22, C27 to C30 for the 5VDC supply. Low frequency filtering is provided by C17 and C2 for the 12VDC supply, and C5 and C16 for the 5VDC supply.

The Reset Circuit

The output of the exclusive 'or' gate UD3 pin 6 will be "low" until C46 has charged through R25. Once the voltage across C46 reaches 2 volts, the output of UD3 pin 6 will go "high". This occurs when the disk is powered on, or a reset pulse is generated by a device connected to the serial bus. The reset pulse on the serial bus interface is input on, pin 6 of P2 or P3. This "low" to "high" going pulse on pin 6 of UD3 is input to the microprocessors reset interrupt input. This causes a restart on reset routine to be executed giving control of the disk drive operation to the Disk Operating System (DOS).

The Clock Circuits

Crystal Y1 outputs a 16Mhz clock signal. THis is input to UD5 on pin 8. UD5 is configured as a ÷ 16 frequency divider. The output of UD5 pin 12 is a 1 MHz clock signal used as the system clock (Phase 0) for the microprocessor. UE6 is a programmable counter ( ÷ 16, ÷ 15, ÷ 14, ÷ 13) that outputs a varying frequency clock used to compensate for the difference in recording area/sector for sectors on inner tracks (Trks 1,2,3) as compared to sectors on out most tracks (Trks 33,34,35). The area/sector for inner tracks is less than the area/sector for out most tracks, so the recording clock frequency is increased when writing on inner tracks to keep the flux density constant. This clock output is on pin 12 of UE6.

| Tracks | Clock Frequency | | Divide By |
|---|---|---|---|
| 1-17 | 1.2307 | MHz | 13 |
| 18-24 | 1.1428 | MHz | 14 |
| 15-30 | 1.0666 | MHz | 15 |
| 31-35 | 1 | MHz | 16 |

Microprocessor Control of RAM and ROM

UB3 and UB4 are 8192 x 8 bit ROMS that store the Disk Operating System (DOS). UB3 resides at memory locations $C000-$DFFF. UB4 resides at memory locations $E000-$FFFF. UC5 and UC6 decodes the addresses output from the microprocessor when selecting these ROMS. UB2 is a 2048 x 8 bit RAM. UB2 resides at memory locations $0000-$07FF. This memory is used for processor stack operations, general processor housekeeping, use program storage, and 4 temporary buffer areas. UC5, UC6 and UC7 decode the addresses output from the processor when selecting RAM.

The Serial Interface

UC3 is a 6522 Versatile Interface Adapter (VIA). Two parallel ports, handshake control, programmable timers, and interrupt control are standard features of the VIA. Port B signals (PB0-PB7) control the serial interface driver ICs (UB1 and UA1). CLK and DATA signals are bidirectional signals connected to pins 4 and 5 of P2 and P3. ANT (Attention) is an input on pin 3

of P2 and P3 that is sensed at PB7 and CA1 of UC3 after being inverted by UA1. ATNA (Attention Acknowledge) is an output from PB4 of UC3 which is sensed on the data line pin 5 of P2 and P4 after being exclusively "ored" by UD3 and inverted by UB1. UC3 is selected by UC7 pin 7 going "low" when the proper address is output from the processor. UC3 resides at memory locations $1C00-$1C0F.

### Microprocessor R/W and Motor Control Logic

UC2 is a VIA also. During a write operation the microprocessor passes the data to be recorded to Port A of UC2. The data is then loaded into the PLA parallel port (YB0-YB7). The PLA contains a shift register which converts the parallel data into serial data. The PLA generates signals on pins 2, 3, 4, and 40 which control the write amplifier circuits on D-IN input on pin 24 of the PLA. The PLA shift register converts serial data into parallel data that is latched at the parallel port (YB0-YB7). The register converts serial data into parallel data that is latched at the parallel port (YB0-YB7). The microprocessor reads the parallel data that is latched at the parallel port (YB0-YB7). The microprocessor reads the parallel PLA output by reading Port A of UC2 when BYTE READY on pin 39 goes "low." The stepper motor is controlled by two outputs on port B of UC2 (STP0, and STP1). A binary four count is developed from these two lines, driving the four phases of the stepper motor. The PLA converts STP0 and STP1 into four outputs that represent one of the four states in the count (Y0,Y1,Y2,Y3). The Spindle motor is controlled by the output MTR of UC2. The PLA inverts this signal. It is then passed to the motor speed control pcb. UC2 pin 14 is an input that monitors the state of the write protect sensor, and pin 13 is an output that controls the activity light (RED LED). UC7 decodes the addresses output from the processor when selecting UC2. UC2 resides at memory locations $1800-$180F.

### Read/Write Control Logic

During a write operation, UD3 converts parallel data into serial data. The output on pin 9 is input to 'NAND' gate UF5 pin 4. UF5 outputs the serial data on pin 6 at the clock rate determined by input signal on pin 5. The output clocks the D flip flop UF6. The outputs of UF6, Q and _Q, drive the write amplifiers. During a read operation, data from the read amplifiers is applied to the CLR input of counter UF4. The outputs, C and D, are shaped by the 'NOR' gate UE5. UE5 outputs the serial data on pin 1, then it is converted to parallel data by UD2. The output of UD2 is latched by UC3. The serial bits are counted by UE4, when 8 bits have been counted, UF3 pin 12 goes "low", UC1 pin 10 goes "high", and UF3 pin 8 goes "low" indicating a byte is ready to be read by the processor. UC2 monitors the parallel output of UD2, when all 8 bits are "1", the output pin 9 goes "low" indicating a sync bit has been read.

### Read Amplifier Circuits

When data is recorded on the disk, a "1" bit is represented on the disk by a change in direction of magnetic flux, caused by a change in direction of current passed through the R/W coil in the R/W head. When a "0" bit is to be recorded, no change in current flow direction occurs, causing the direction of the magnetic flux to remain the same on the disk.

When data is being read from the disk, CEMF is induced into the R/W coil by the magnetic fields on the disk, causing current flow which is detected by the read amplifiers. Current flow through the R/W coil will forward bias wither CR16 or CR17, depending on the direction. Q7 and CR14 must be forward biased. The first amplifier UF3, senses this current flow from the R/W coil on one of the inputs and amplifies it. L9, L10, L11, L12 and C45 act as a low pass filter, suppressing noise on the amplified output. UF4 is a differential amplifier which amplifies the difference of the two input signals from the filter section. UE4 is a peak detector. The output of UE4 will pulse "high" when a "1" is read. This signal is then reconstruction of the data recorded. The Time Domain Filter, UD4, times out when a "1" bit has been read, so unwanted "1" bits are not added to the actual data. The One Shot UD4 generates the correct data pulse width so the PLA can convert the data to parallel for processor control.

### Write Amplifier Circuits

During a write operation, B must be "high". This forward biases Q7 and CR14. If _B goes "low", Q3 and Q6 become forward biased. If Q goes "low", Q5 and CR15 become forward biased, passing current flow through R/W 1. If _Q goes "low", Q4 and CR18 become forward biased, passing current flow through R/W 2. When a write operation occurs, the ERASE coil is energized by forward biasing Q6. This demagnetizes the outer edges of the track, preventing data on one track from bleeding into the next track.

### Power Up/Down Write Protection

This circuit prevents erroneous data from being written on the disk during power up/down sequences. During a power up, the 12VDC supply is not applied to the R/W coils and amplifier circuits before the processor has control of the logic. During a power down the 12VDC supply is removed from the R/w coils and amplifier circuits before the processor loses control of the logic. Q1 acts as a series pass transistor, biased to regulate the 12VF output to the R/W coils and Amplifier circuits. Q2 is a feedback amplifier monitoring the 5VDC supply. CR5 develops a precise reference voltage for Q2. L8 and C15 delay the 12VDC supply.

### Spindle Motor Control Circuits

_MTR output from the PLA is active "low". This signal is passed, through the current driver UD2, to the motor control PCB. When _MTR is "low," Q1 is biased off, and Q2, Q3, and Q4 are biased on, allowing current flow through the spindle motor coil. Attached to the shaft of the spindle motor is an inductive tachometer that generates low level AC voltages, as the motor spins. The output of the tachometer is rectified by CR1-CR4. IC 1 monitors the output of the rectifier and adjusts the bias to Q2, which changes the bias on Q3 and Q4 to regulate motor current for a constant velocity. VR1 is a manual speed adjustment. The speed can be adjusted by watching the 60Hz
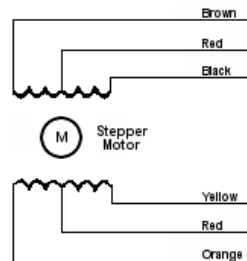
strobe as the adjustment is made or loading the system test from the diagnostic disc. The Newtronics Motor Speed PCB is electronically the same as the ALPS Motor Speed PCB, but some of the discrete components have been integrated.
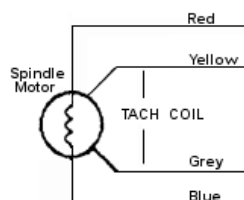
**Troubleshooting Guide**

Always check for latest ROM/ECO upgrade. If socketed IC is suspected bad, be to check socket with ohmmeter.

| Symptom | Possible Solution |
|---|---|
| No LED's on power up. | Is Power cord plugged into wall outlet correctly? |
| | Is Power cord plugged in the disk drive correctly? |
| | Check line fuse. |
| | Check power switch. |
| | Check clock on 6502 pin 37. |
| | Check +5 and +12 volt lines. |
| Error LED flashes on power up. | Check all RAM and ROM locations. |
| Error LED stays on all the time. | Check 6502 microprocessor. |
| | Check ROMs. |
| Drive motor runs continuously and red LED stays on. | Check +12V. |
| | Check 6502, logic gates, logic array. |
| Drive motor runs continuously and red LED stays off. | Check Rom |
| | Check drive motor PCB. |
| Drive motor runs continuously with no red or green LED's. | Check VR2 (5V Regulator) |
| | Check Power Transformer. |
| After the drive warms up the motor runs continuously. | Check 6522s. |
| | Check motor control PCB. |
| Loads programs with red LED flashing. | Check drive speed. |
| | Check stepper motor. |
| Loading is intermittent. | Check ROMs. |
| | Check drive alignment. |
| Does not load when hot or LED flashed 3 times. | Check ROMs. |
| Searches with LED flashing continuously. | Check ROMs. |
| Searching with no red LED. | Check 6522s, logic gates, logic array. |
| Message 'FILE NOT FOUND' is displayed | Clean drive head w/alcohol. |
| | Check 0 stop adjustment. |
| | Check alignment. |
| Drive fails to read. | Check the 311, 9602, and 592s. |
| | There are two +12 volt sources for stepper output |
| | and read circuit, make sure both are good. |

**Resistance Checks**



Stepper Motor

32 ohms end to centertap
64 ohms end to end

Spindle Motor — TACH COIL

Motor coil = 17 ohms
Tach coil = 175 ohms (rest)
Tach coil = 135-190 ohms (motion)
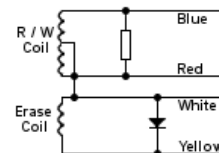
R/W Coil — Erase Coil

R/W end to end = 32.4 ohms
R/w end to centertap = 16.3 ohms
Erase coil end to end = 10.5 ohms

**Casework/Accessory Parts List**

| | | |
|---|---|---|
| 1540/1541 | Top Case (IVORY) | C 1540014-01 |
| 1540/41 | Bottom Case (IVORY) | C 1540015-00 |
| 1541 | Top Case (BROWN) | C 1540014-03 |
| 1541 | Bottom Case (IVORY) | 1540015-03 |
| Shield Cover | | 1540013-03 |
| LED Assembly | | C 1540013 |
| Self Adhesive Foot | | C 950150-02 |
| 1540 Nameplate | | C 1540016-02 |
| 1541 Nameplate | | C 1540052-00 |
| Power Cord Assembly | | C 903508-04 |
| 6 PIN DIN Cable | | C 1515001-01 |
| User'S Manual | | C 1540031-03 |
| Demo Diskette | | C 1540024-01 |

**Model Indentification**

PCB Assy # 1540008-01
- Schematic # 1540001
- Original "Long" Board
- Has 4 discreet 2114 RAMs
- ALPS Drive only

PCB Assy # 1540048
- Schematic # 1540049
- Referred to as the CR board
- Changed to 2048 x 8 bit RAM pkg.
- A 40 pin Gate Array is used
- Alps Drive (-01)
- Newtronics Drive (-03)

PCB Assy # 250442-01
- Schematic # 251748
- Termed the 1541 A
- Just one jumper change to accommodate both types of drive

PCB Assy # 250446-01
- Schematic # 251748 (See Notes)
- Termed the 1541 A-2
- Just one jumper change to accommodate both types of drive

Note: The simplest way to identify which drive you have is by door assembly. Alps is made with a "push down" door and Newtronics has a "flipper" type door.

**Device Number Change**

The 1540 and 1541 drives are shipped from the factory se for device # 8. The channel can be hardware altered to # 9, 10, or 11 by two methods:

1) Refer to appropriate board layout drawing for the location of the pads provided for this purpose. The device change pads must be CUT to alter the channel number and re-soldered if another change is needed later.
2) The preferred method to alter the device number is to lift certain pins of the 6522 chip. The IC should always be socketed, so removal of the chip is simple. Once removed, the proper pin can be carefully bent to eliminate it from the circuit. If another change is needed, simply remove the I.C. and re-install with the pin back in place.

| PCB Assy # | Location | Device # | Lift Pin |
|---|---|---|---|
| 1540008 | UAB1 | 9 | 15 |
| 1540048,251748 | UC3 | 10 | 16 |
| and 251834 | UC3 | 11 | 15 and 16 |