AURIX 2G Power Management System

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IFCN ATV SMD GC SAE MC

Agenda

1. Power Supply and Control
2. Power Management
3. Monitoring and Reset
4. Power Consumption

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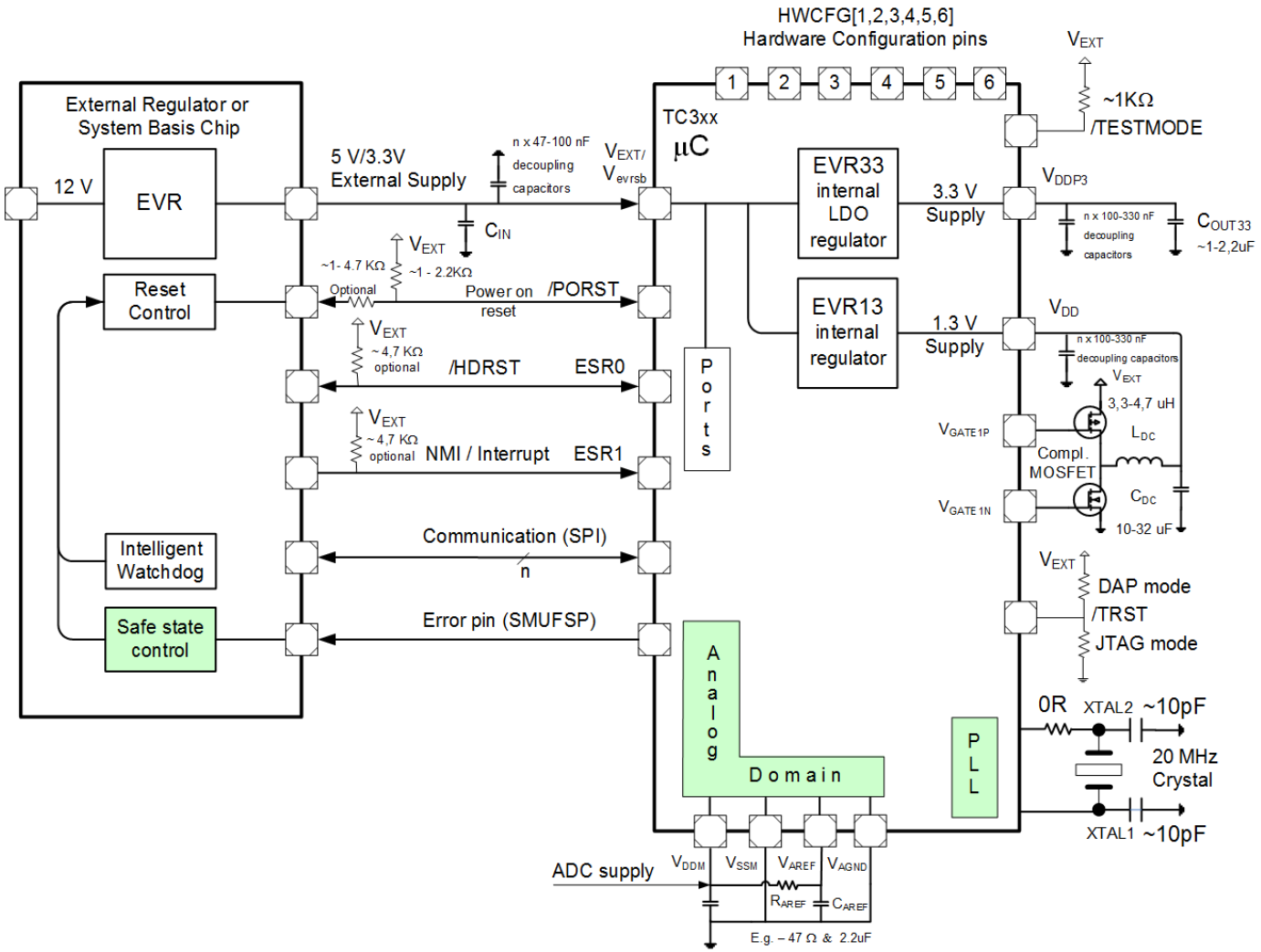
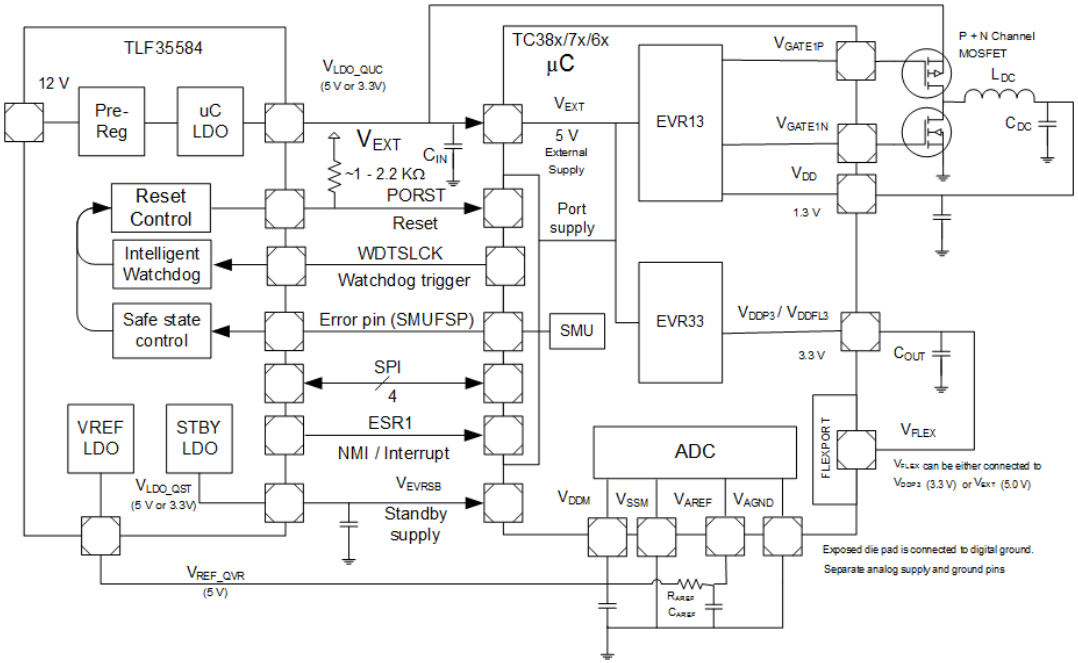
Power Supply and Control
Standard Interface to External regulator



Power Supply and Control
Standard Interface to TLF35584 regulator

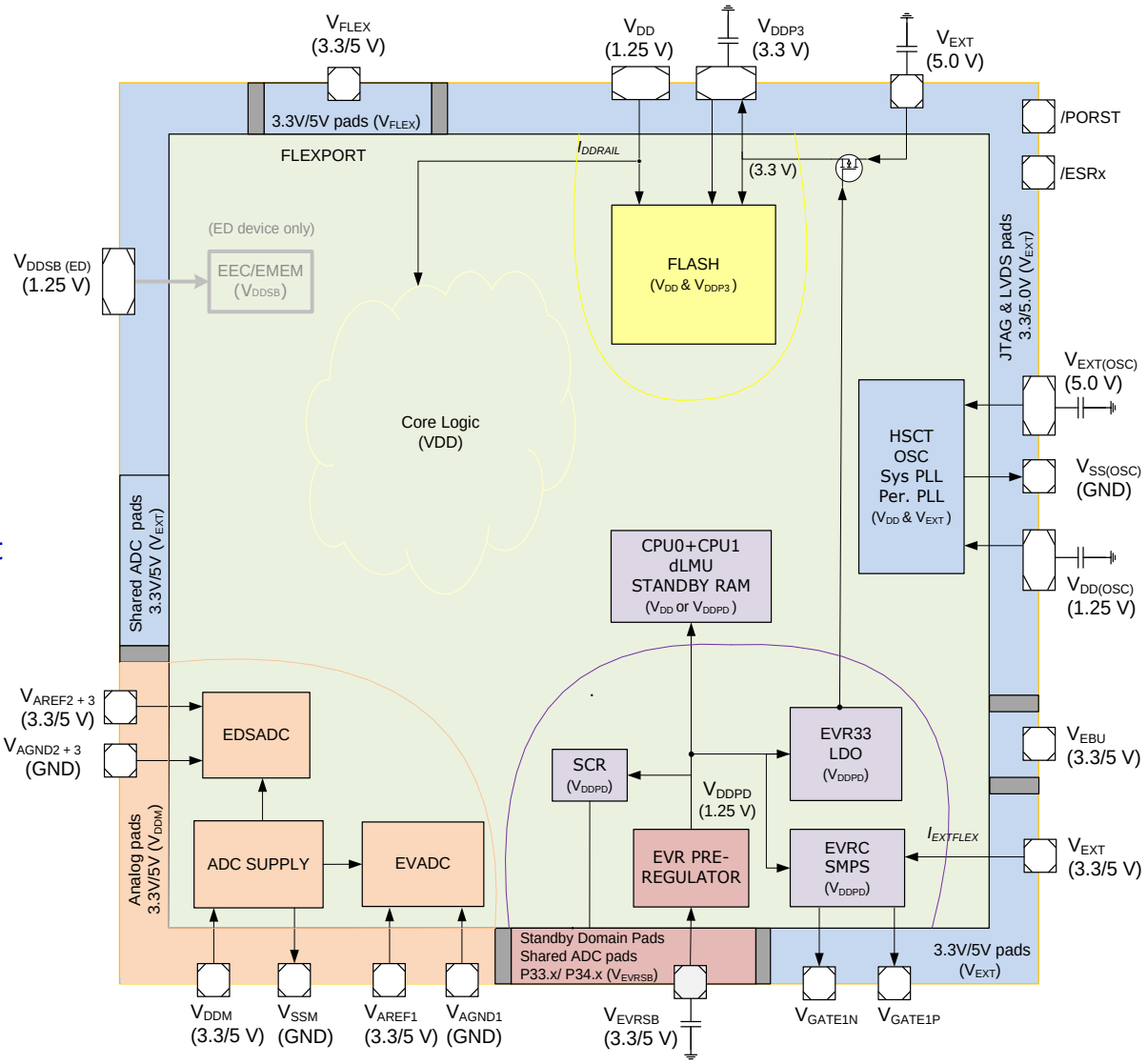
- Standard interface
  - Reset monitoring for 5V/3.3V Vext
  - **Single**, Dual or Triple rail supplies
  - Separate analog domain supply
  - Separate standby domain supply
  - SPI configuration interface
  - NMI interface (error interrupt) + SPI
- Safety relevant enhancements
  - Q/A watchdog supporting query-response mechanism
  - Safe State Control
    - Supervision of regulators
    - Watchdogs – WWD and FWD
    - Fail safe pin of µC. Fail Safe pin is connnected to secondary voltage monitors routed from uC to regulator.



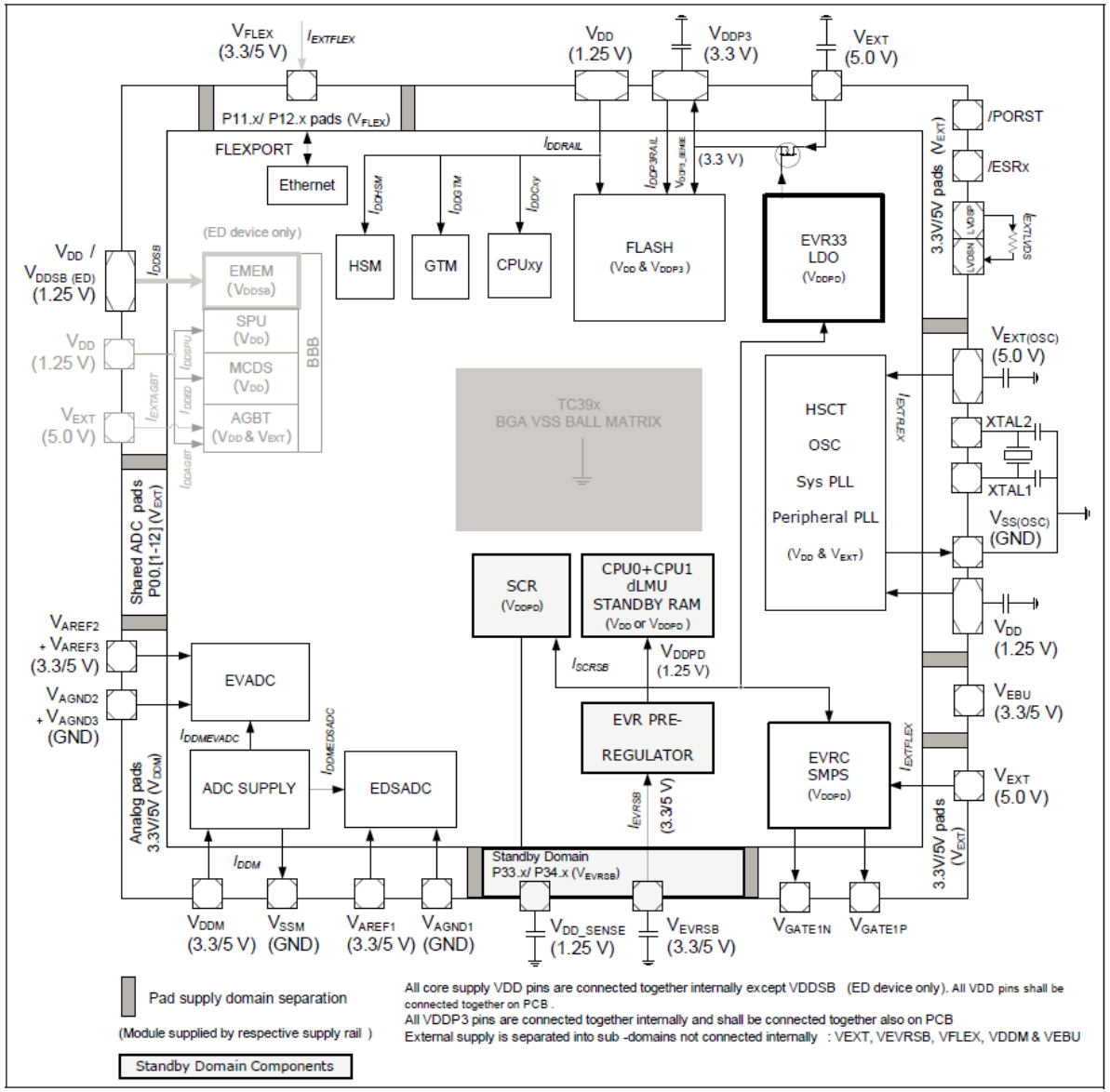
TC3xx
Power Domains

- 5V / 3.3V VEVRSB Standby Domain
  - VDDPD Standby Domain (Regulators, Start-up / Safety modules, PMS, SCR)
  - Standby Pads (P33, P34)
  - CPU0 and CPU1

    dLMU Standby RAM
- 5V / 3.3V VEXT Pad domain
  - All Pads / Ports, Shared pads
  - OSC, HSCT
- 5V / 3.3V VFLEX, VEBU independent and isolated Pad domains
- 5V / 3.3V VDDM ADC domain
  - EVADC, DSADC, ADC pads
- 3.3V VDDP3 Flash domain
  - Flash Programming
- 1.25V VDD domain
  - Core domain (CPUs,..)
  - Flash Read Sense
- 1.25V VDDSB (ED domain, EMEM)



TC39x
Supply Pins and Module Connectivity



Embedded Voltage Regulators
Features at a glance

- Supply modes (What should external regulator supply?)
  - Single source 5V supply
    - 5V + 10 % - 20%
  - Single source 3.3V supply
    - 3.3V ± 10 %
  - Legacy tri-supply mode also supported for backward compatibility.
    - 5V + 10 % - 20%
    - 3.3V ± 10 %
    - 1.25V ± 10 %
  - Dual supply modes
- Supply topologies (How should the internal voltages be generated?)
  - Linear / Low dropout mode (LDO)
  - Switch mode DC –DC regulator mode (SMPS)
- System modes (Does the supply requirements change with system modes?)
  - Normal Run
  - Sleep Mode (Target < 10 mA) - Selective Clock gating carried out
  - Standby Mode (Target < 50 uA) (3.0V @ V_{EXT}) - Only Standby Domain is powered

Embedded Voltage Regulators
Features at a glance

- Higher tolerance to external 5V supply voltage drops upto 3.0V (Eg. Engine Cranking phase).. Compliance to LV 124 specification…
- Compensation against transient load changes to minimize voltage over/under-shoots.
  - Current ramps limited to 50mA / 100us @ Startup to have reduced load jumps on external regulator.
  - No power sequencing required between supplies incase of dual/triple supply modes.
- Capability to drive additional external non-inductive 3.3 V loads from internal devices.
- Mixed IO system
  - 5V or 3.3V Flexport (upto 18 pins) with a dedicated separate supply pin
  - 5V or 3.3V ADCs
- Idle Request Acknowledge Reset Sequence to avoid corruption of RAM contents after a reset in case of non-power related failures. Eg: /PORST assertion
- Bidirectional PORST : PORST capable of driving upto a max of 13 mA incase of Supply undervoltage events

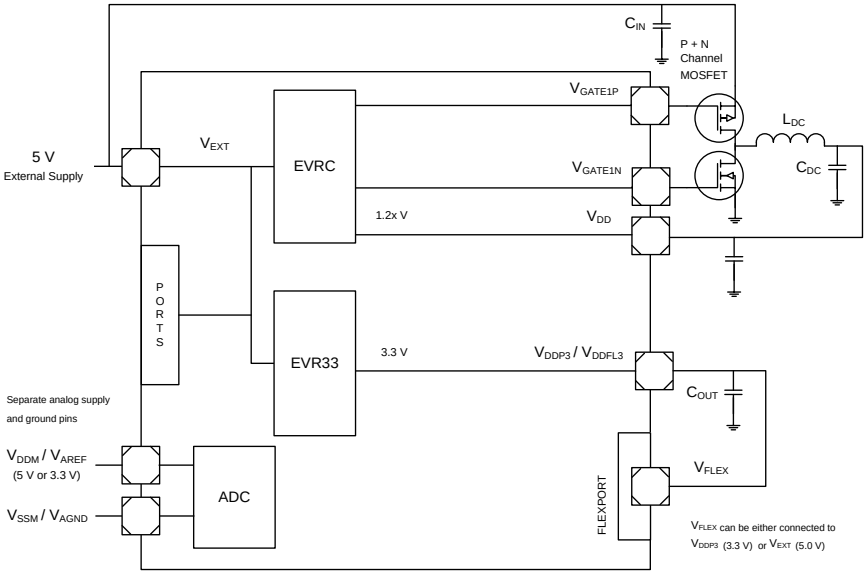
TC3xx
Salient features

	TC39x TC38x	TC37x TC36x	TC35x
Dual / Triple Ext. Supply	5V / 3,3V ± 10% External supply range. Single, dual & triple supply as in AURIX. Separate VDDM / VAREF supply for ADC		
EVRC Core Regulator	LC DC DC (Efficiency η=72%+) (0.8 MHz and 1.8 MHz nominal switching frequency) 3,3uH - 4,7uH inductor + 6,8 -10uF input cap +10 - 22uF output cap		
	Static accuracy target = 2% over PVT + 12mV ripple in case of SMPS		
Nominal VDD Set point range	TC3xx VDD nominal voltage = 1,25V ± 10% 1,2 V up to 1,3 V in steps of 5 mV in case of TC3xx		
EVR33 3,3V regulator	LDO with internal pass devices. 1 uF buffer capacitor. Internal regulator static accuracy target = 2% over PVT		
VDDP3 Range & Tolerance	3,3V ± 10%. No voltage scaling. Static accuracy = 2%		
Primary supply monitors	Bi-directional PORST concept as in A1G. Configurable (1% - 2%) voltage and time hysteresis. Default reset threshold < -10%		
Secondary supply monitors	Internal dedicated Secondary monitors with static accuracy = 2% over PVT. Configurable averaging filter VEXT(3.3V/5V), VDDP3(3.3V), VDD(1.3V), VDDM(3.3V/5V), VEVRSB(3.3V/5V) & VDDPD(1.3V)		

	TC33x	TC32x
EVRC Core Regulator	SC DC DC . 1uF flying cap + 10uF i/p cap 300 mA current capability with 72% efficiency. Upto 450 mA capability with less efficiency.	
	Static accuracy target = 2% over PVT + 12mV ripple in case of SMPS	

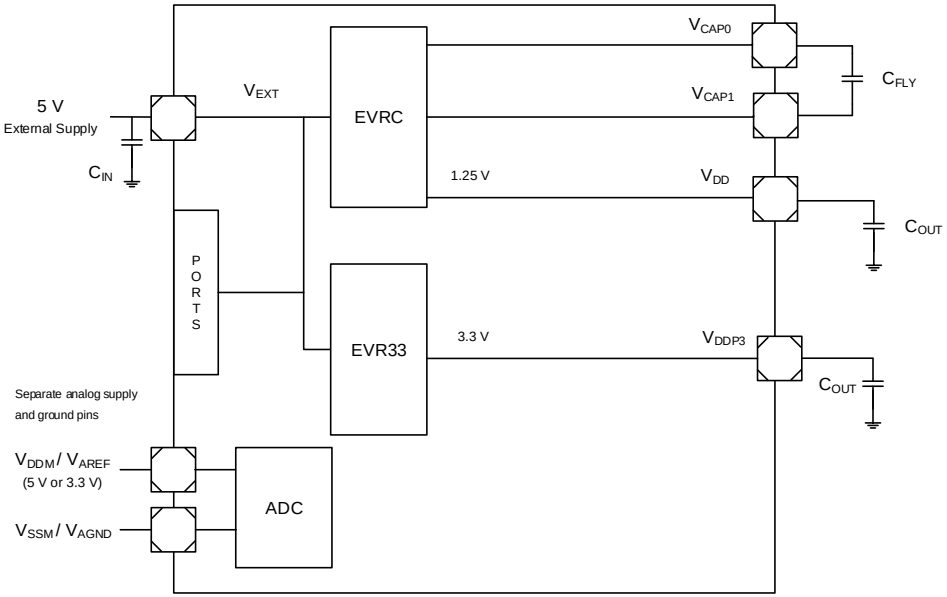
TC3xx
Regulator Support

	TC39x 3.3V / 5V	TC38x 3.3V / 5V	TC37x 3.3V / 5V	TC36x TC35x 3.3V / 5V	TC33x TC32x 3.3V / 5V
EVR12	LC DC DC 3,3 - 4,7uH inductor + 6,8-10uF i/p cap +10-22uF o/p cap				SC DC DC 10 uF + 1 uF
EVR33	LDO with internal pass devices. 1 uF capacitor.				



Exposed die pad is connected to digital ground.

EVR Switch mode topology a1 v 0.5



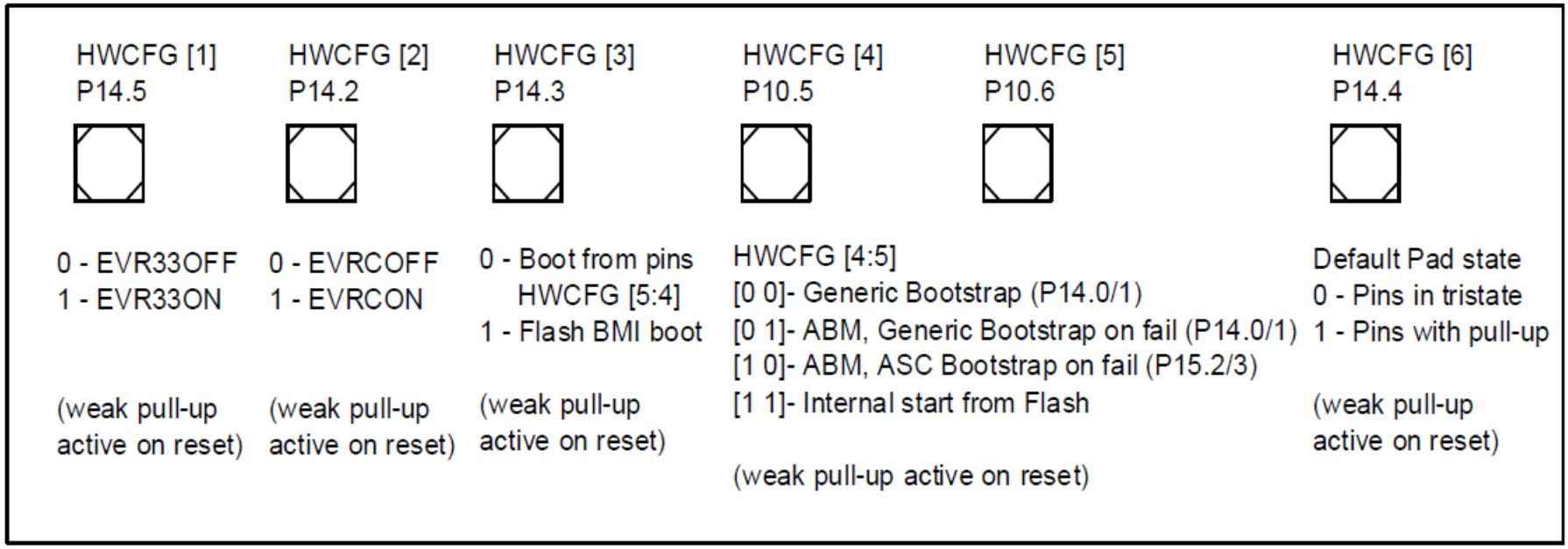
Exposed die pad is connected to digital ground.

EVR Switch mode topology a2 v 0.6

TC3xx
Salient features

	TC39x	TC38x	TC37x
Infrastructure	Enhanced High Precision Bandgap shared by PMS, ADC,Flash & LVDS with better accuracy. Enhanced DTS continuously active with inherently better accuracy. Enhanced 100 MHz back-up clock with trimming support to meet CAN requirements		
Load Jumps	+-150 mA jump with 100us settling time. < (IDD_real / 3) reset jump +-200 mA incase of LBIST, +-100 mA incase of MBIST Droop compensation implemented in regulators.		
Line Jumps	upto 50 V/ms with overshoot/undershoot on external supplies limited to ±10% for internal EVR regulators. 300 V/ms under evaluation.		
Sleep mode	15 - 20 mA @ Tj =25°C and fSPB/fSRI ~ 1 MHz		
Standby mode	150 uA like in AURIX. Standby mode with Standby RAM, an integrated wake-up timer and Standby Controller.		
Standby RAM	4x 32 Kbytes Standby RAM. Standby VEVRSB pin available also in LQFP packages.		
TLF ext. regulator enhancements	Voltage Scaling support, Configurable reset under / over voltage thresholds, FSP pin, SPI interface with CRC support.		

Supply Mode Selection
HWCFG [x] + TESTMODE



1.) HWCFG [1:6] has weak internal pull-up active at start-up if the pin is left unconnected.

- HWCFG[1:3, 6] has weak pull-up active at start-up if pin is left unconnected.
- If HWCFG[6] is left unconnected or externally pulled high, then HWCFG[4:5] pins have weak internal pull-ups active at start-up.
- If HWCFG[6] is connected to ground, then HWCFG[4:5] pins are tristated.
- In addition for TESTMODE pin (P20.2) additional external strong pull-up to Vext of 1 - 4.7kOhm is recommended.

Supply Mode Selection
HWCFG [2,1] + VGATE1P/N

No.	HWCFG [2,1][1]	VGATE1P[2] VGATE1N[3]	Supply Pin Voltage Level / Source[4]	Selected Supply Scheme[5]
a.)	11_B	VGATE1P/ VGATE1N connected to gate of P- /N-ch. MOSFET.	VEXT & VEVRSB = 5.0 V external supply. VDDM = VAREFx = 5V or 3.3V external supply. VFLEX = 5 V or 3.3 V. VDDP3 and VDDFL3 supplied by EVR33. VDD supplied by EVRC.	5 V single source supply. EVRC in SMPS mode. EVR33 in LDO mode. 5 V or 3.3 V ADC domain. 5 V or 3.3 V Flexport domain. Standby Mode supported.
d.)	01_B	Overlapped P32.1 / P32.0 port pins may be used as standard GPIO.	VEXT & VEVRSB = 5.0 V external supply. VDDM = VAREFx = 5V or 3.3V external supply. VFLEX = 5 V or 3.3 V. VDDP3 and VDDFL3 supplied by EVR33. VDD = 1.25 V external supply.	5 V & 1.25 V external supply. EVRC inactive. EVR33 in LDO mode. 5 V or 3.3 V ADC domain. 5 V or 3.3 V Flexport domain. Standby Mode is supported and 1.25V supply shall be switched off by external regulator after Standby state is entered.
e.)	10_B	VGATE1P/VGATE1N connected to gate of P- /N-ch. MOSFET.	VEXT,VEVRSB,VDDP3,VFLEX and VDDFL3 = 3.3V external supply. VDDM = VAREFx = 5V or 3.3V external supply. VDD supplied by EVRC.	3.3 V single source supply. EVRC in SMPS mode. EVR33 inactive. 5 V or 3.3 V ADC domain. 3.3 V Flexport domain. Standby Mode supported.
			VEXT & VEVRSB = 5.0 V external supply. VDDP3, VFLEX and VDDFL3 = 3.3V external supply. VDDM = VAREFx = 5V or 3.3V external supply. VDD supplied by EVRC.	5 V & 3.3 V external supply. EVRC in SMPS mode. EVR33 inactive. 5 V or 3.3 V ADC domain. 5 V or 3.3 V Flexport domain. Standby Mode is supported and 3.3V supply shall be switched off by external regulator after Standby state is entered.
h.)	00_B	Overlapped P32.1 / P32.0 port pins may be used as standard GPIO.	VEXT & VEVRSB = 5.0 V external supply. VDDM = VAREFx = 5V or 3.3V external supply. VFLEX = 5 V or 3.3 V.external supply. VDDP3 and VDDFL3 = 3.3V external supply. VDD = 1.25 V external supply.	5 V, 3.3 V and 1.25 V are supplied externally. EVRC and EVR33 inactive. 5 V or 3.3 V ADC domain. 5 V or 3.3 V Flexport domain. Standby Mode is supported and 3.3V and 1.25V supplies shall be switched off by external regulator after Standby state is entered.

Supply Mode Selection indication

PMSWSTAT

Standby and Wake-up Status Register **($00D4_H$)** **LVD Reset Value: 000A 0000$_H$**

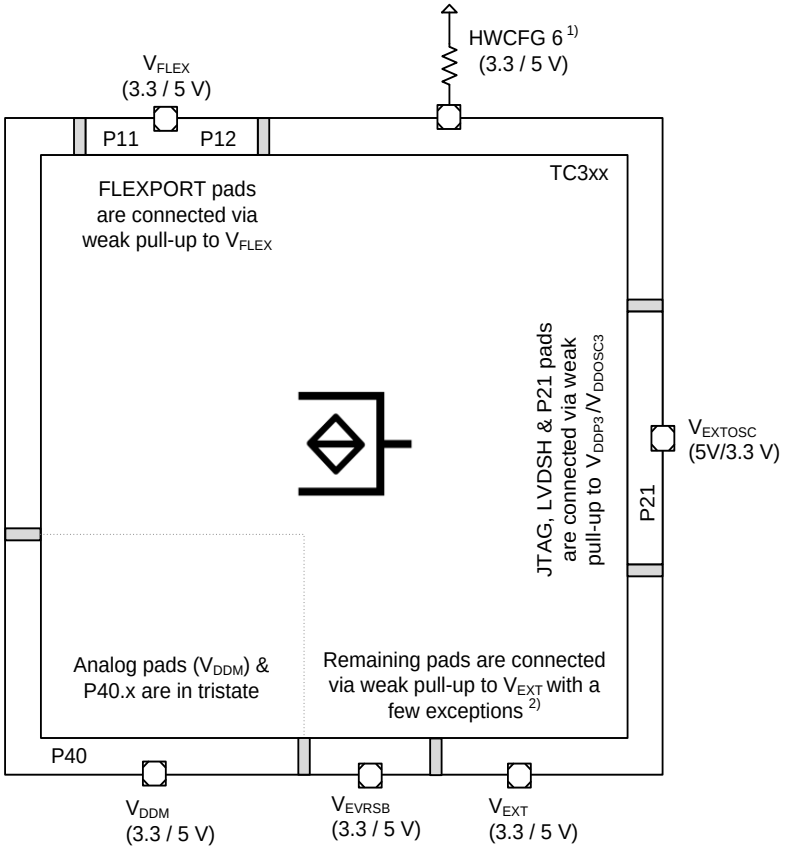
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	
PINBINT	PINAINT	ESR1INT	ESR0INT	0	WUTMODE	WUTRUN	WUTEN	0				PORSTREQ	SCRCLK	SCRST	SCR
rh	rh	rh	rh	r	rh	rh	rh	r				rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				PORSTDF	0		ESR0TRIST	TESTMODE	TRIST	HWCFG5	HWCFG4	0	HWCFGEVR		0
r				rh	r		rh	rh	rh	rh	rh	r	rh		r

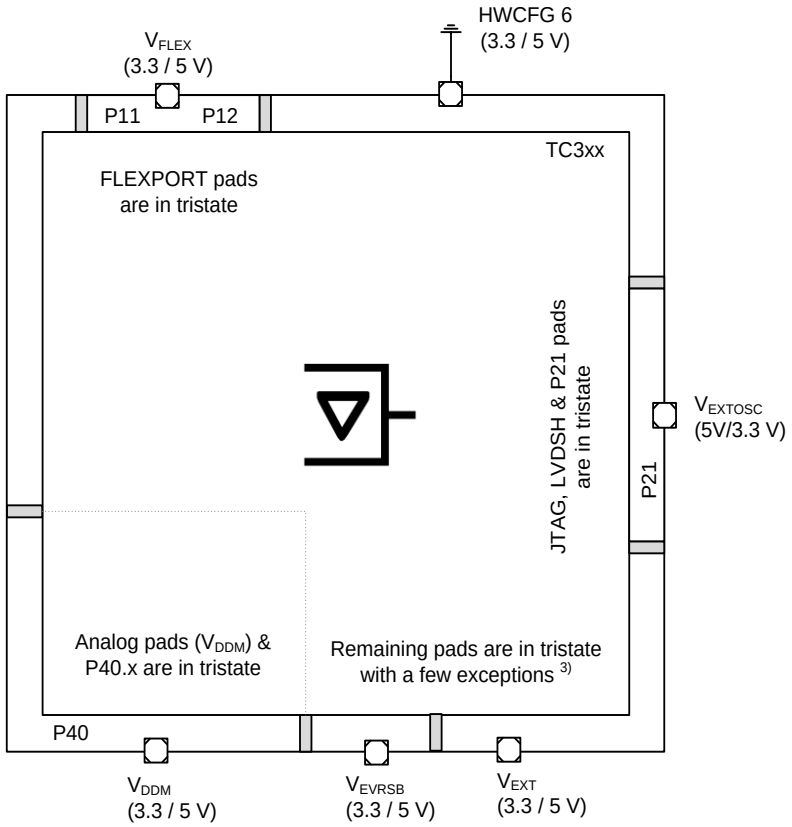
HWCFGEVR	2:1	rh	**EVR Hardware Configuration status** This bit field indicates the supply configuration latched by the EVR from HWCFG[2:1] during a cold startup based on which EVRx regulators are consequently started. The latched configuration is used during STANDBY-RUN transition to reselect EVR mode. 00_B EVRC inactive, EVR33 inactive. 01_B EVRC inactive, EVR33 active. 10_B EVRC active, EVR33 inactive. 11_B EVRC active, EVR33 active.

Port Pins in Tristate or with Pull-up

Port pins with Pull-up active by default



Port pins in Tristate by default



1.) HWCFG [6] has weak internal pull-up active at start-up if the pin is left unconnected.

2.) If HWCFG [6] is left unconnected or is externally pulled high, weak internal pull-ups are active at port pins during and after reset. Exceptions are P32.0 (pull-down), P33.8 (tristate), P40.x (tristate), reset (PORST, ESR0) and JTAG pins.

3.) If HWCFG [6] is connected to ground, port pins are predominantly in tristate during and after reset. Exceptions are P32.0 (pull-down), reset (PORST, ESR0) and JTAG pins. External pull devices required for HWCFG pins.

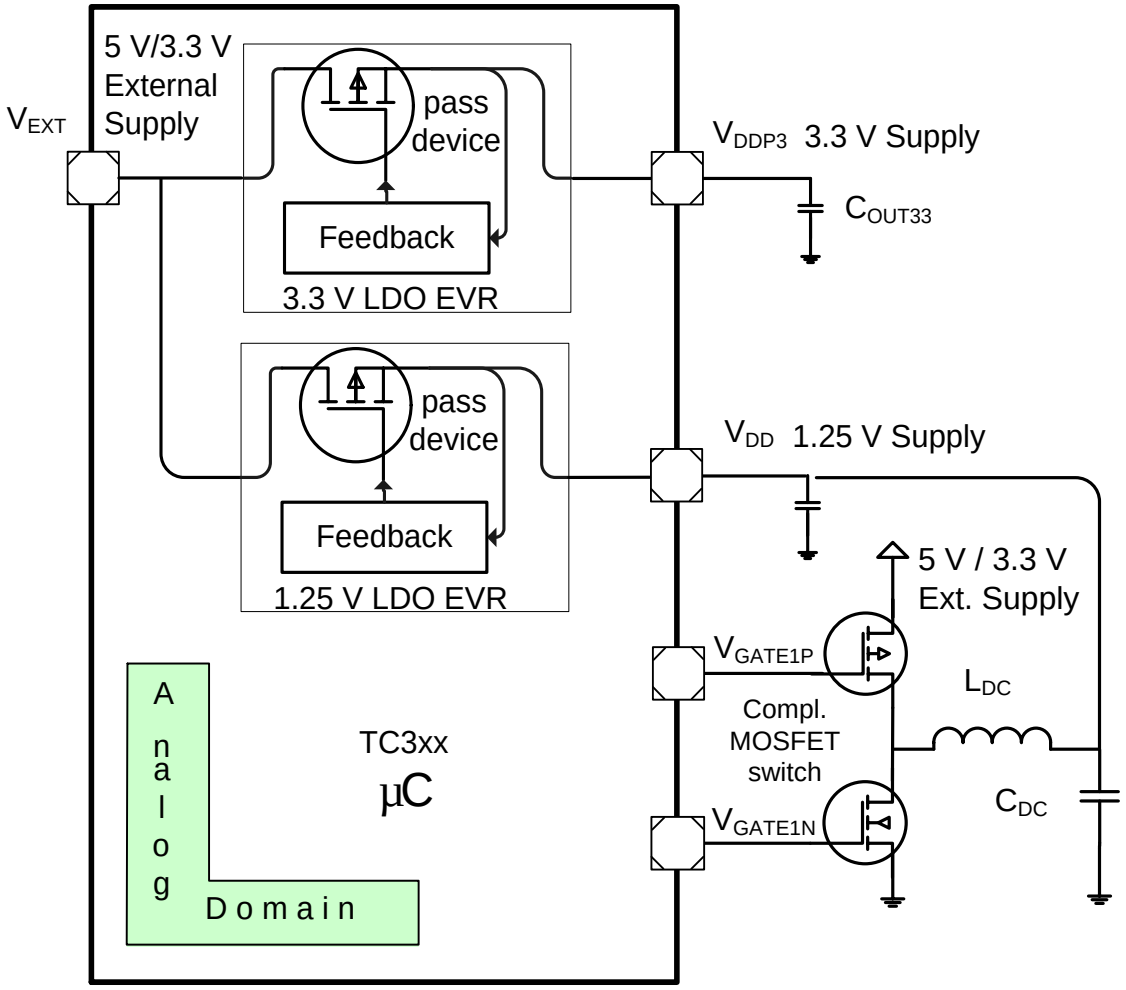
Embedded voltage regulator topologies
Single source supply

- TC39x / TC38x / TC37x/ TC36x

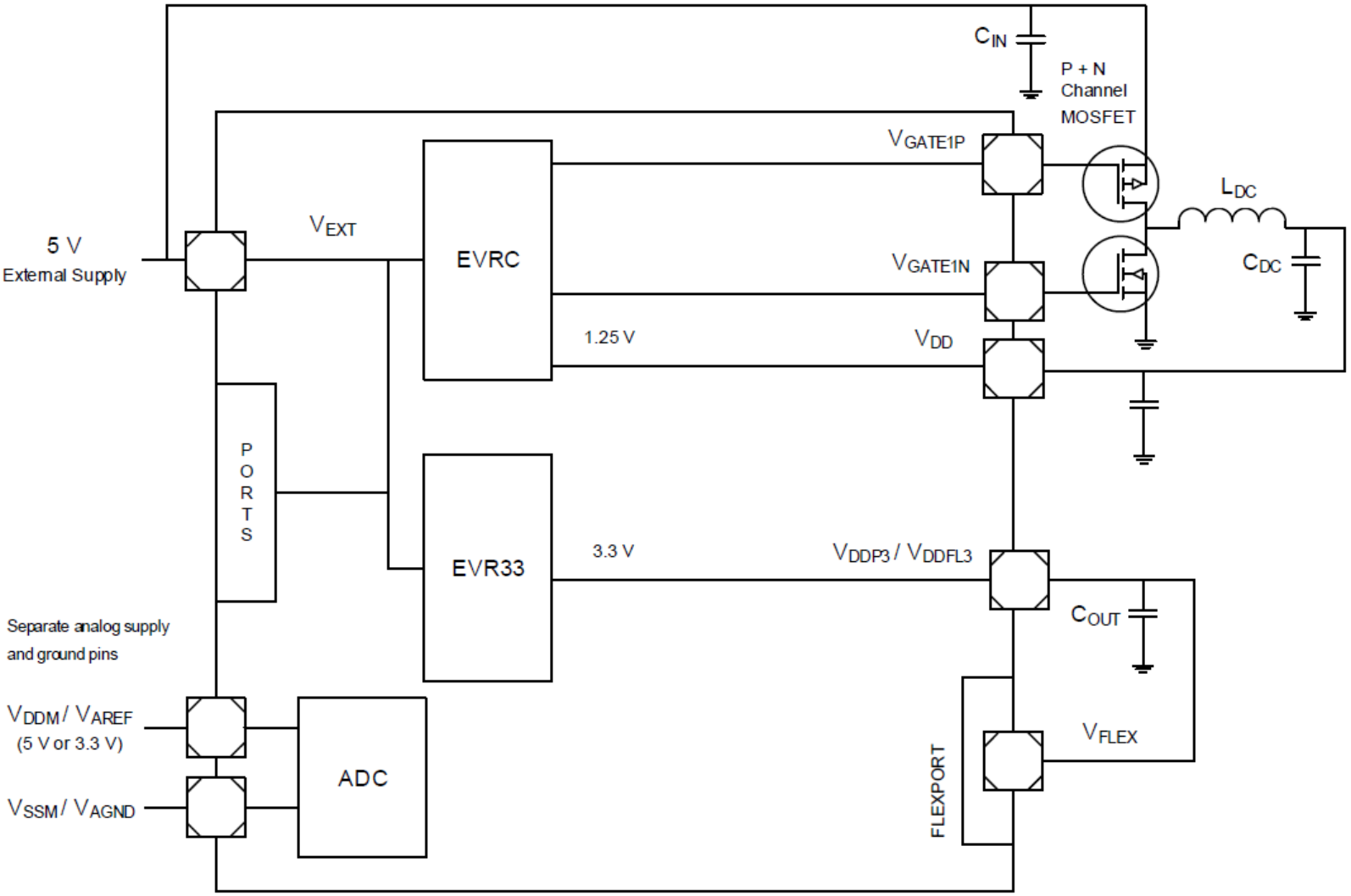
  (I_{EXT} = **I_{dd} / 3** + I_{ddp3} + I_{ADC})

  Substantial current consumption reduction

  - 1.25V SMPS regulator
    - **80% power conversion efficiency**
    - **Compliance to EMI/EMC BISS limits**



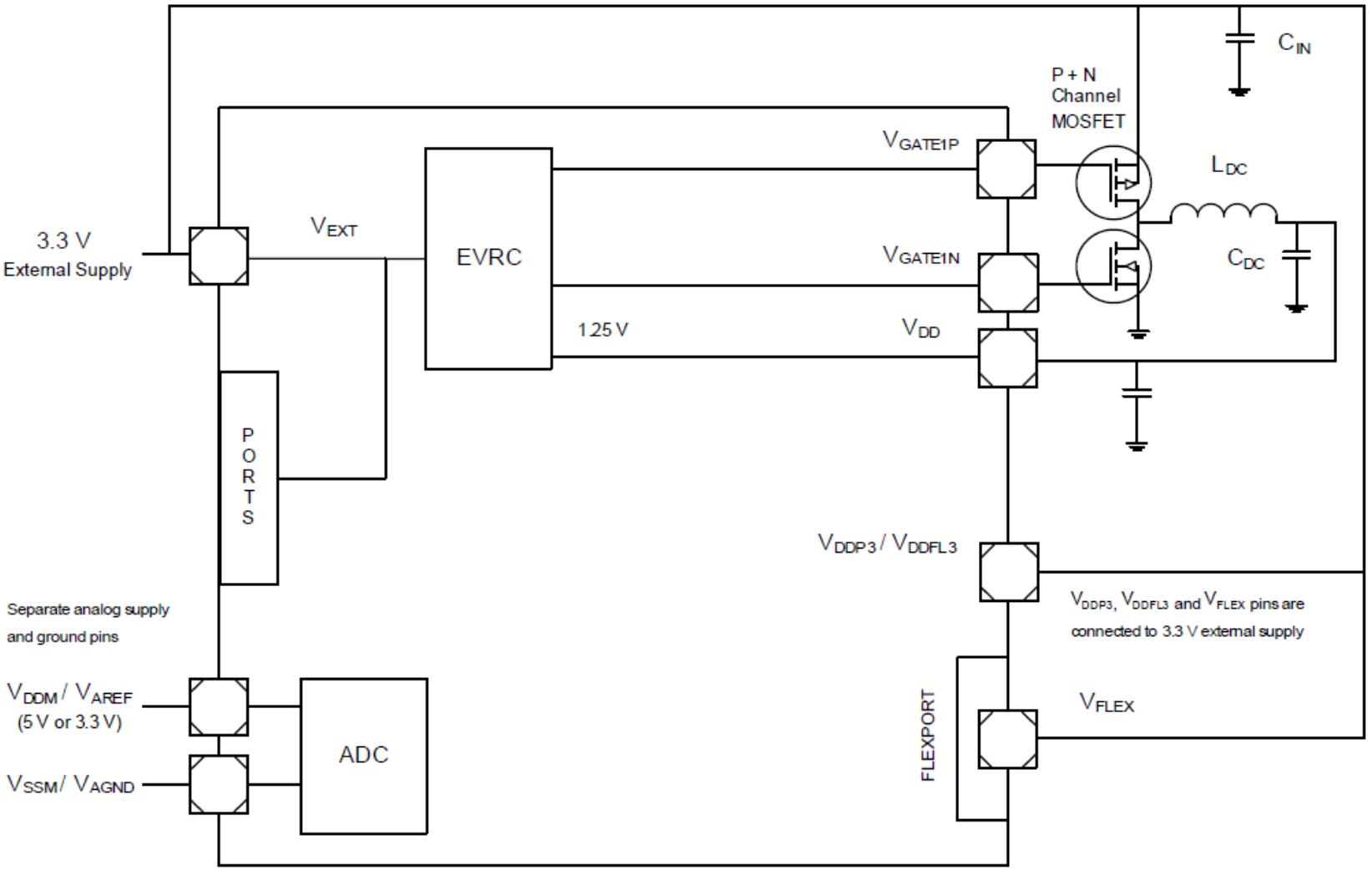
Single supply mode – 5V



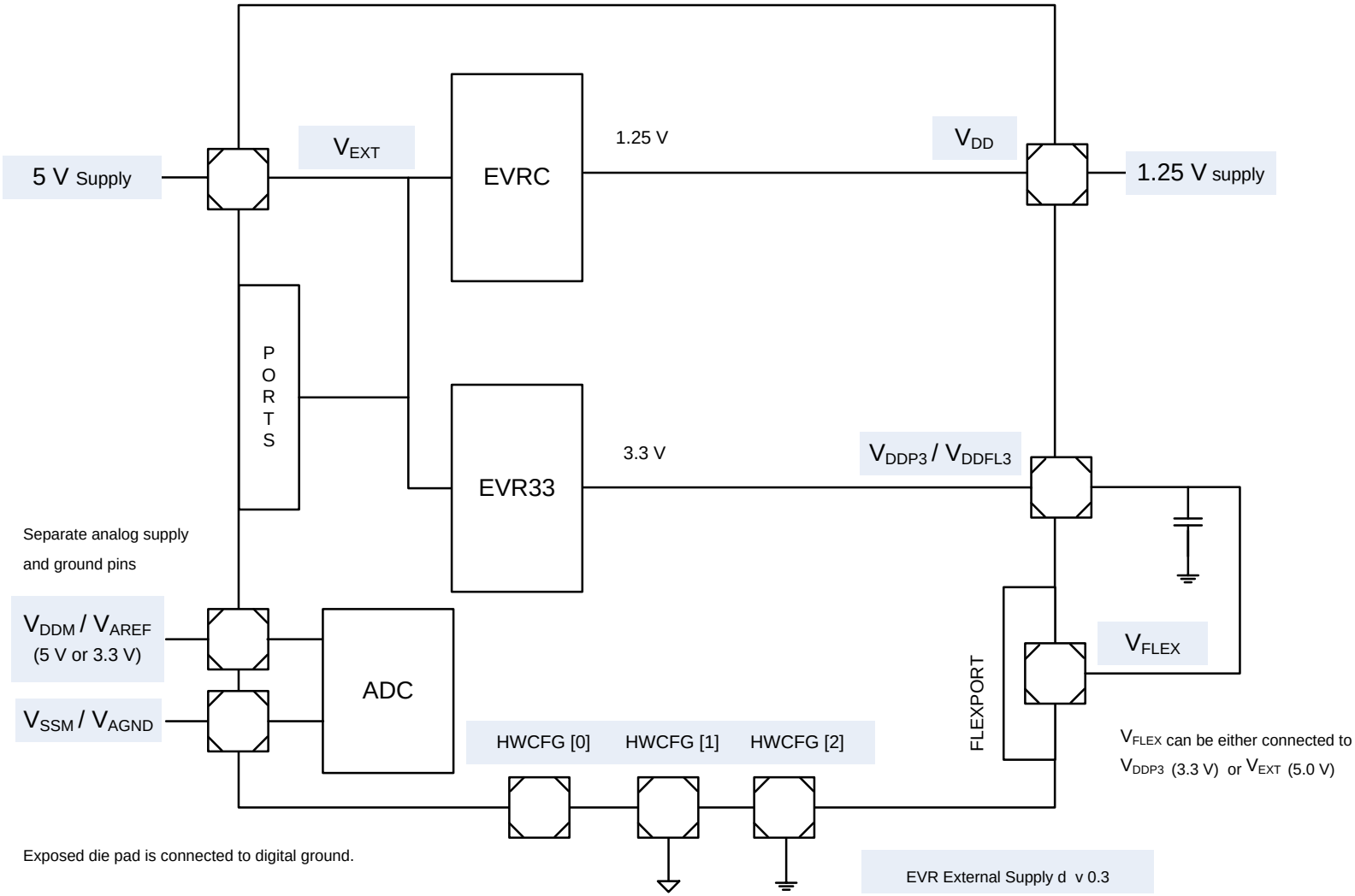
Exposed die pad is connected to digital ground.

EVR Switch mode topology a1 v 0.6

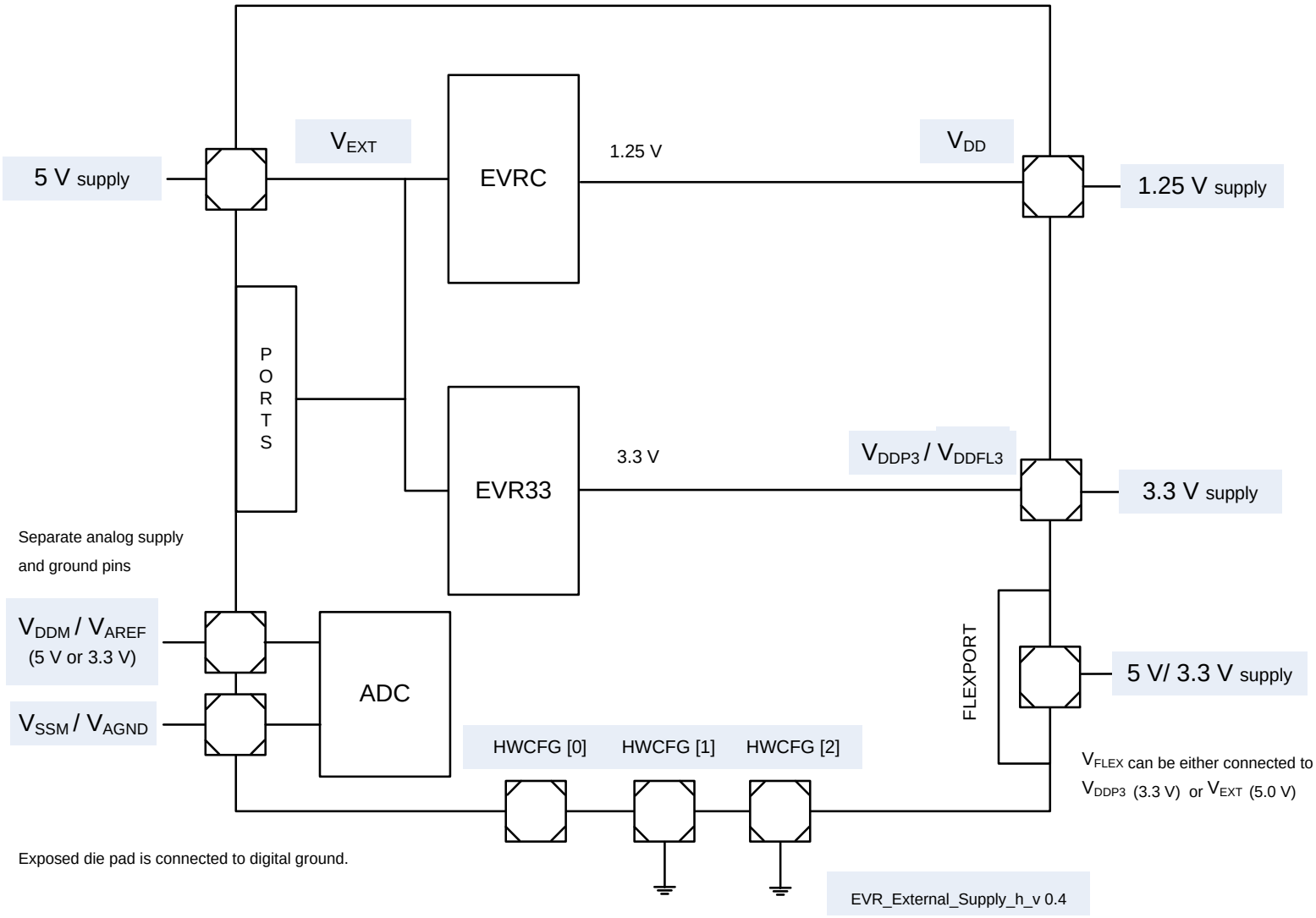
Single supply mode – 3.3V



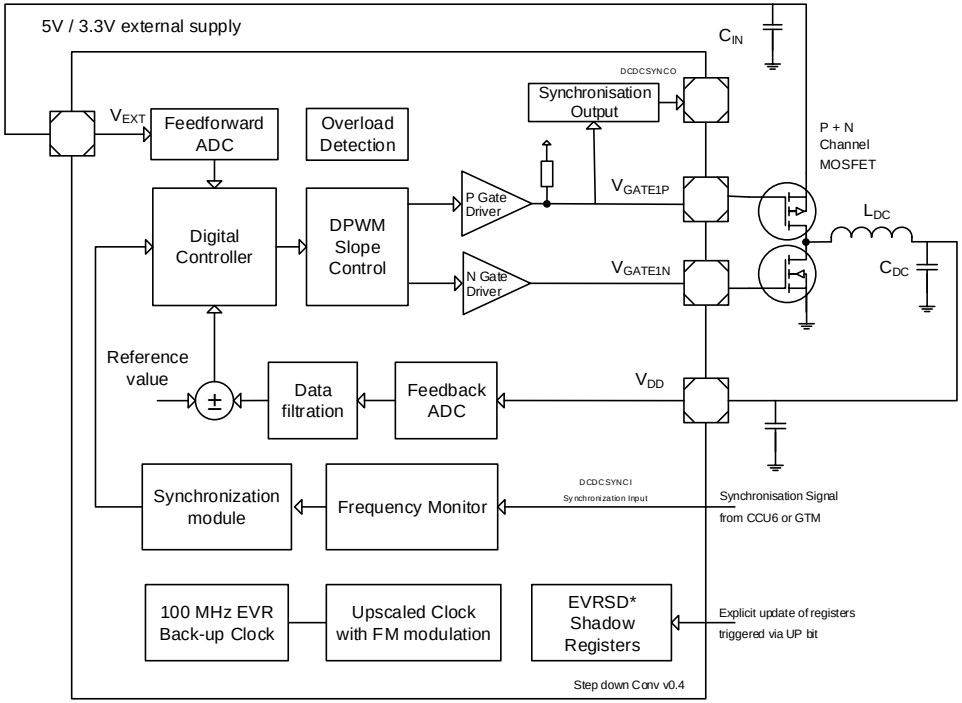
Dual Supply Mode
5V & 1.3V externally supplied



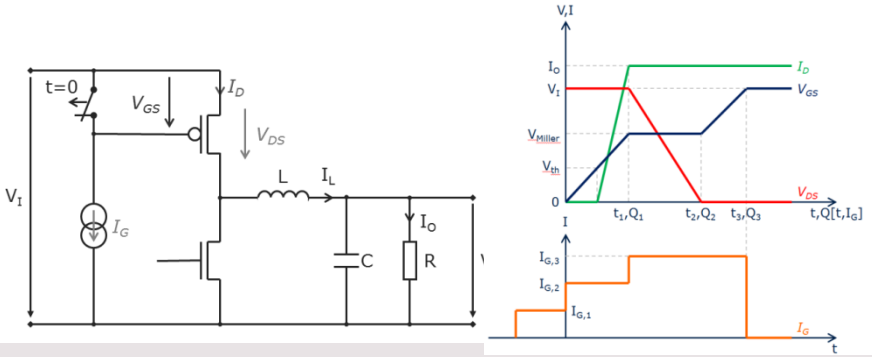
Tripple Supply Mode
5V, 3.3V and 1.3V externally supplied



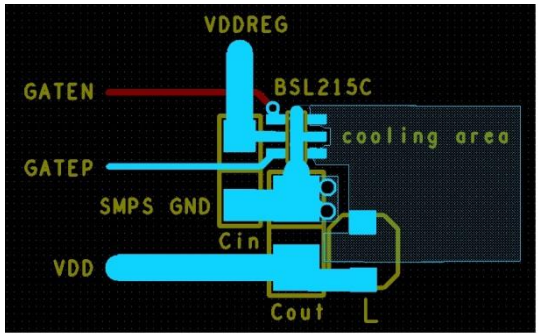
TC3xx
EVRC LC DCDC regulator



- App Note AP32344 – SMPS regulator



- Characteristics
  - 0.8 MHz /1.8 MHz nominal switching frequency
  - ~ 72 % efficiency
  - Improved dynamic response < 6%
  - Voltage Droop on Load Jumps
- Configurability of drive strength, slew rate, frequency and other parameters to comply to EMI/EMC requirements.
- External Components
  1. P + N Channel Complementary MOSFET
     - BSL215C, BSZ215C, NXP MOSFETs
     - Level shifter + MOSFET driver
  2. Inductor/Coil 3.3 - 4,7 uH
  3. Capacitor 10 - 22 uF (32uF @0.8MHz)



TC3xx
EVRC External Components Reference

Table 5 EVRC Regulator Component Reference and Register Settings (continued)

No.	Condition	Register Update Sequence (Modes a & e)	Components (Package)
3.)	IDD < 1,5A fDCDC = 1,8 MHz VEXT < 3.63/5.5 V	EVRSDCOEFF6 (Driver) = 0088 $1B02_H$ EVRSDCOEFF7 (Driver) = 0000 $D8A6_H$ EVRSDCOEFF8 (Driver) = 0088 $1B02_H$ EVRSDCOEFF9 (Driver) = 0000 $D8A6_H$ EVRSDCTRL7 (Driver) = 0000 $02C8_H$ EVRSDCTRL0.UP = 1_B wait 20 us check EVRSDCTRL0.UP bit is cleared. EVRSDCTRL7.DRVSLOMODE = 00_B EVRSDCTRL0.UP = 1_B wait 20 us check EVRSDCTRL0.UP bit is cleared. **EVRSDCTRL0 (Freq., Spreading) = 2036 0002_H** EVRSDCTRL1 (PWM mode) = 0B69 0708_H **EVRSDCOEFF0 (PWM mode) = 3508 $73B6_H$** EVRSDCOEFF1 (PWM mode) = 0294 $6C46_H$ EVRSDCTRL2 (LP mode) = 0036 $033B_H$ EVRSDCTRL3 (LP mode) = 0B69 0810_H EVRSDCOEFF2 (LP mode) = 3408 $710E_H$ EVRSDCOEFF3 (LP mode) = 0294 $6C44_H$ EVRSDCTRL4 (Start mode) = 0036 0009_H EVRSDCTRL5 (Start mode) = 0B69 0808_H EVRSDCTRL6 (Open Loop) = 0023 $1C94_H$ EVRSDCOEFF4 (Start mode) = 1B08 $23B6_H$ EVRSDCOEFF5 (Start mode) = 0294 $6C44_H$ EVRSDCTRL8 (FBADC) = 1121 $048E_H$ EVRSDCTRL9 (FFADC) = 0000 0434_H EVRSDCTRL10 (Short) = 0000 0000_H EVRSDCTRL11 (Droop) = 1207 0909_H EVRSDCTRL0.UP = 1_B check EVRSDCTRL0.UP bit is cleared. check EVRSTAT.SDVOK is set.	Complementary MOSFET - BSZ15DC02KD / BSZ215C Inductor (3.3 uH) - CLF6045NIT-3R3N-D or LTF5022T-3R3N2R5-H/D (long term availability not assured) or RLF7030T-3R3M4R1-T or SLF7045T-3R3M2R1 or TFM252012ALMA3R3MTAA (under analysis) Output Capacitor (22 uF) - CGA6P1X7R1C226M - 2 x CGA6M3X7R1C106K Input Capacitor (10 uF) - CGA6M3X7R1C106K

Table 5 EVRC Regulator Component Reference and Register Settings (continued)

No.	Condition	Register Update Sequence (Modes a & e)	Components (Package)
4.)	IDD < 1,5 A fDCDC = 0.8 MHz VEXT < 3.63/5.5 V	EVRSDCOEFF6 (Driver) = 0088 $1B02_H$ EVRSDCOEFF7 (Driver) = 0000 $D8A6_H$ EVRSDCOEFF8 (Driver) = 0088 $1B02_H$ EVRSDCOEFF9 (Driver) = 0000 $D8A6_H$ EVRSDCTRL7 (Driver) = 0000 $02C8_H$ EVRSDCTRL0.UP = 1_B wait 20 us check EVRSDCTRL0.UP bit is cleared. EVRSDCTRL7.DRVSLOMODE = 00_B EVRSDCTRL0.UP = 1_B wait 20 us check EVRSDCTRL0.UP bit is cleared. **EVRSDCTRL0 (Freq., Spreading) = 207C 0002_H** EVRSDCTRL1 (PWM mode) = 0B69 0708_H **EVRSDCOEFF0 (PWM mode) = 3408 7236_H** EVRSDCOEFF1 (PWM mode) = 0294 $6C46_H$ EVRSDCTRL2 (LP mode) = 0036 $033B_H$ EVRSDCTRL3 (LP mode) = 0B69 0810_H EVRSDCOEFF2 (LP mode) = 3408 $710E_H$ EVRSDCOEFF3 (LP mode) = 0294 $6C44_H$ EVRSDCTRL4 (Start mode) = 0036 0009_H EVRSDCTRL5 (Start mode) = 0B69 0808_H EVRSDCTRL6 (Open Loop) = 0023 $1C94_H$ EVRSDCOEFF4 (Start mode) = 1B08 $23B6_H$ EVRSDCOEFF5 (Start mode) = 0294 $6C44_H$ EVRSDCTRL8 (FBADC) = 1121 $048E_H$ EVRSDCTRL9 (FFADC) = 0000 0434_H EVRSDCTRL10 (Short) = 0000 0000_H EVRSDCTRL11 (Droop) = 1207 0909_H EVRSDCTRL0.UP = 1_B check EVRSDCTRL0.UP bit is cleared. check EVRSTAT.SDVOK is set.	Complementary MOSFET - BSZ15DC02KD / BSZ215C Inductor (4.7 uH) - CLF6045NIT-4R7N-D or LTF5022T-4R7N2R0-H/D (long term availability not assured) or RLF7030T-4R7M3R4-T or SLF7045T-4R7M2R1 **Output Capacitor (22 uF + 10uF)** - CGA6P1X7R1C226M + CGA6M3X7R1C106K Input Capacitor (10 uF) - CGA6M3X7R1C106K

› Refer Application Note for further details : AP32344 TC3xx SMPS regulator

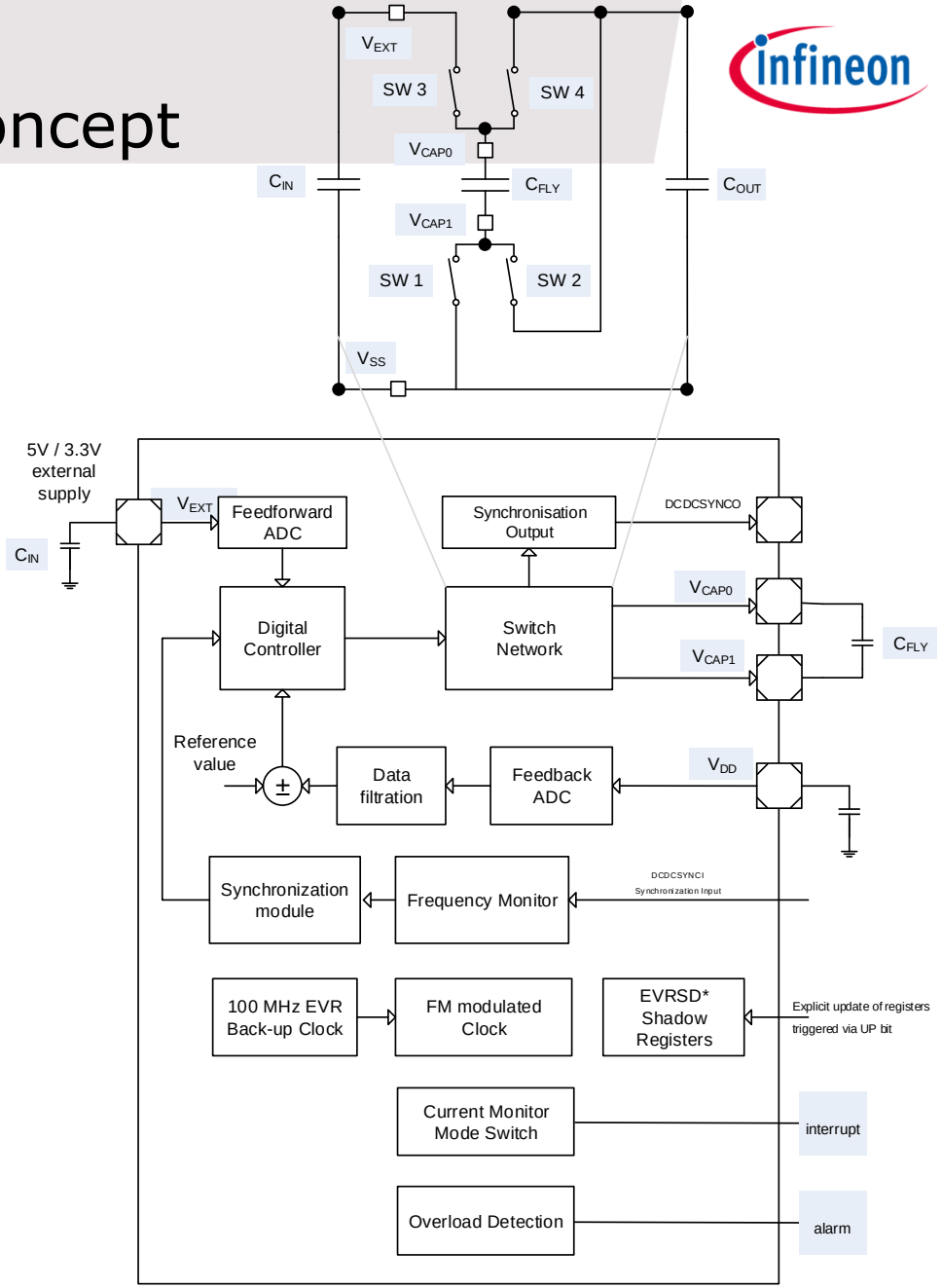
TC3xx
EVR SC DCDC regulator concept

- 72% conversion efficiency feasible from 3.3V/ 5V to 1,25V with single flying capacitor

$I_{TOTDCDC} = I_{DD}/3$ (~80% of I_{TOT}) + I_{DDP3} + I_{EXT}

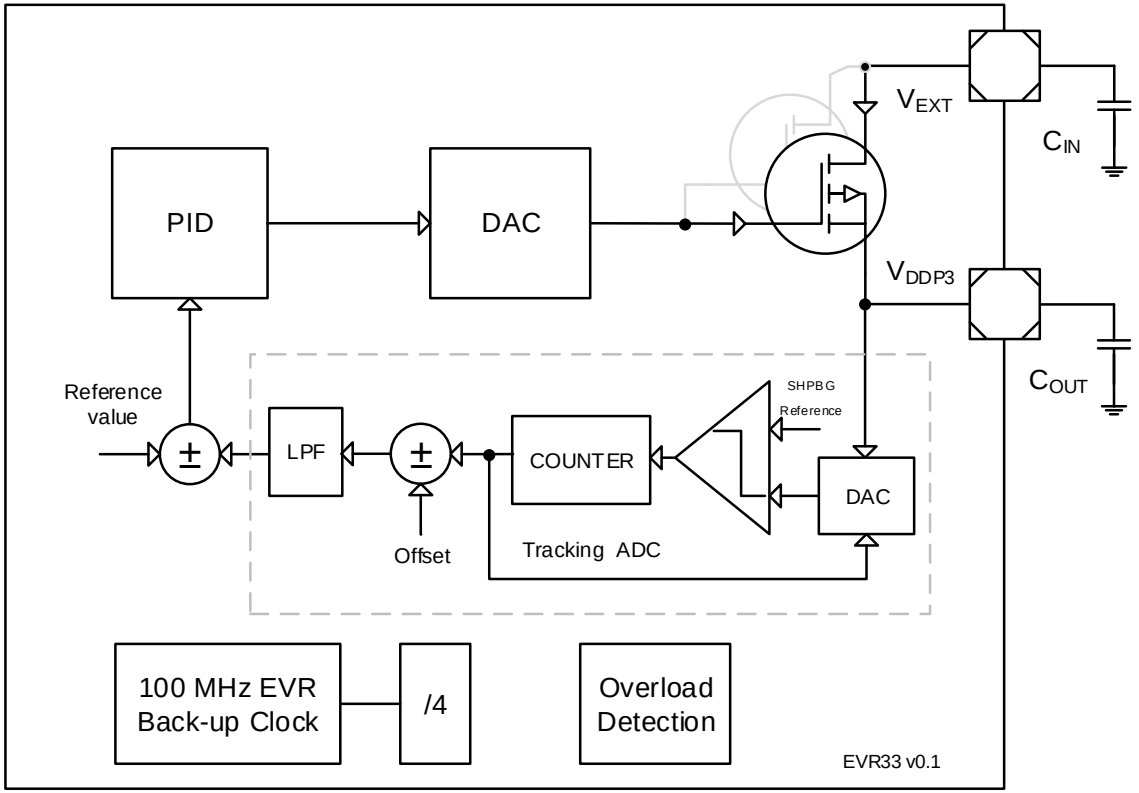
$I_{TOTDCDC}$ = (40% - 45%) * I_{TOT}

- A single 10uF EVRC stabilization capacitor required for IDD ~ 300mA. 450 mA with bypass SCDCDC concept.
- Load regulation and response is better. Minimal undershoot on a reset. Droop compensation allows adjusting the output voltage before triggering the reset load jump.
- BISS limit compliance achieved by using FM modulated switching techniques and variable drive strength and slew rate control of the switches with a trade-off to efficiency.
- Heat generation (uC) < 600mW. Exposed pad may not be required for thermal reasons. SCDCDC switches distributed into sub-switches for better controllability and to avoid local hotspots



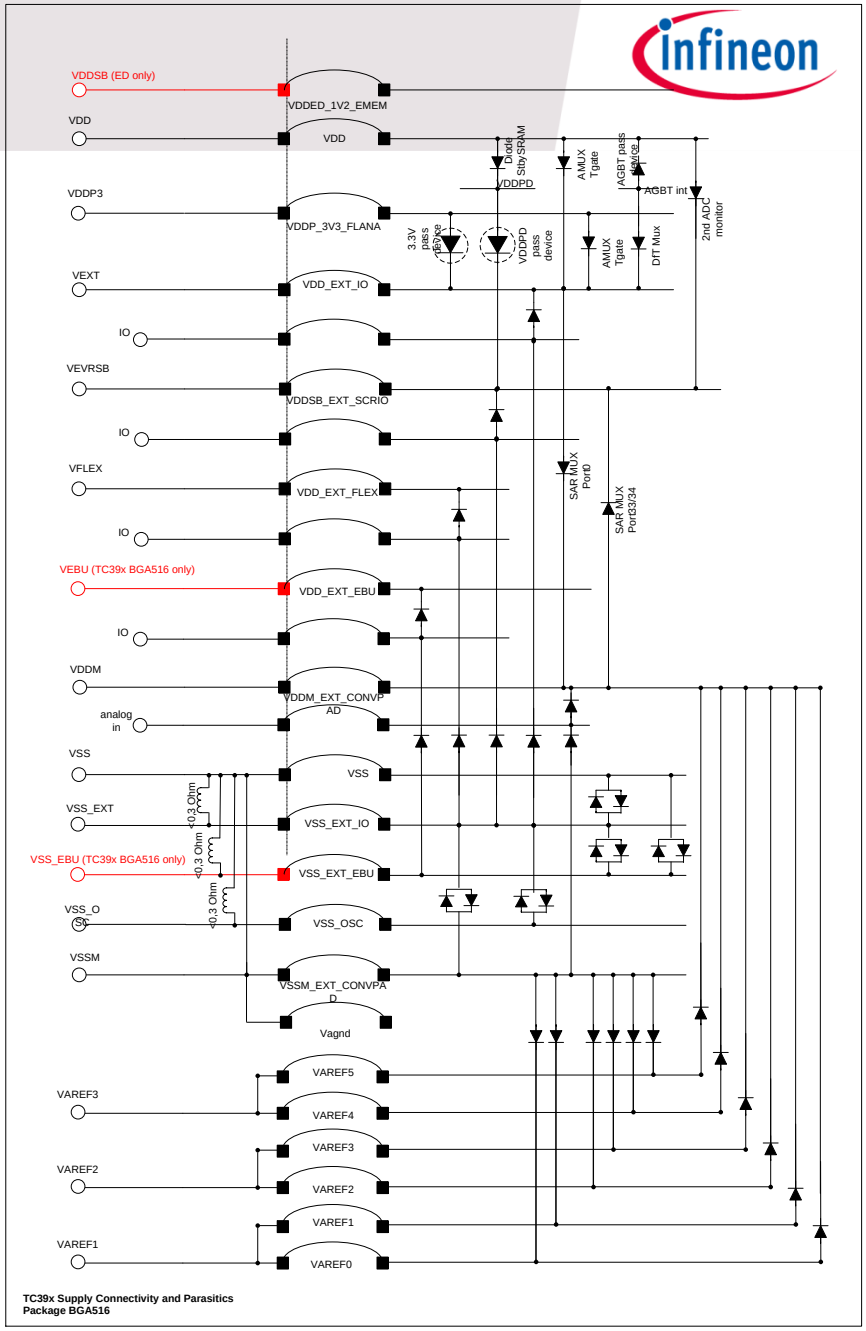
TC3xx
EVR33 LDO regulator concept

- EVR33 generates the 3.3V VDDP3 supply requires for Flash from 5V VEXT supply.
- EVR33 implemented as LDO with distributed pass devices (>10) and COUT = 1 uF (IDDP3 < 60mA).
- A maximum load current of 100 mA is supported.
- Static accuracy = ± 2% ; Dynamic load response = ± 5%.



TC3xx
Internal Parasitics

- All power domains are protected against neighboring domains by ESD elements
- The IO pins have diode-like structures to supply and from ground.
- In case of overvoltage, current should be limited with external resistor to comply with maximum currents of digital and analog pins in general.
- No power sequencing is required for TC3xx devices during startup / shutdown the transients. However injection currents need to be limited.
- The structures are designed to be injection tolerant to ~ 3 times the maximum current consumption of the respective supply domain.



TC39x Supply Connectivity and Parasitics
Package BGA516

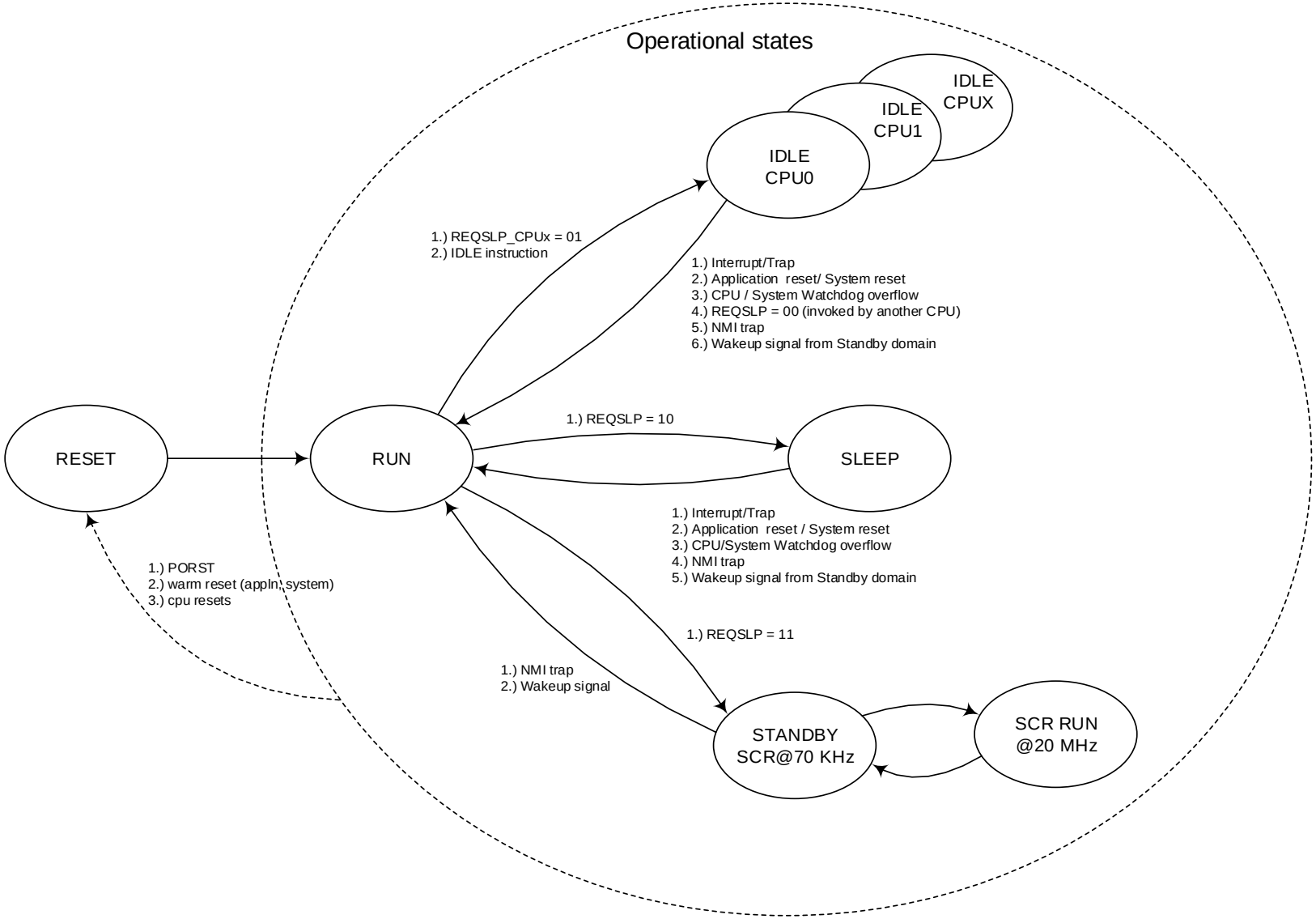
Agenda

1. Power Supply and Control
2. Power Management
3. Monitoring and Reset
4. Power Consumption

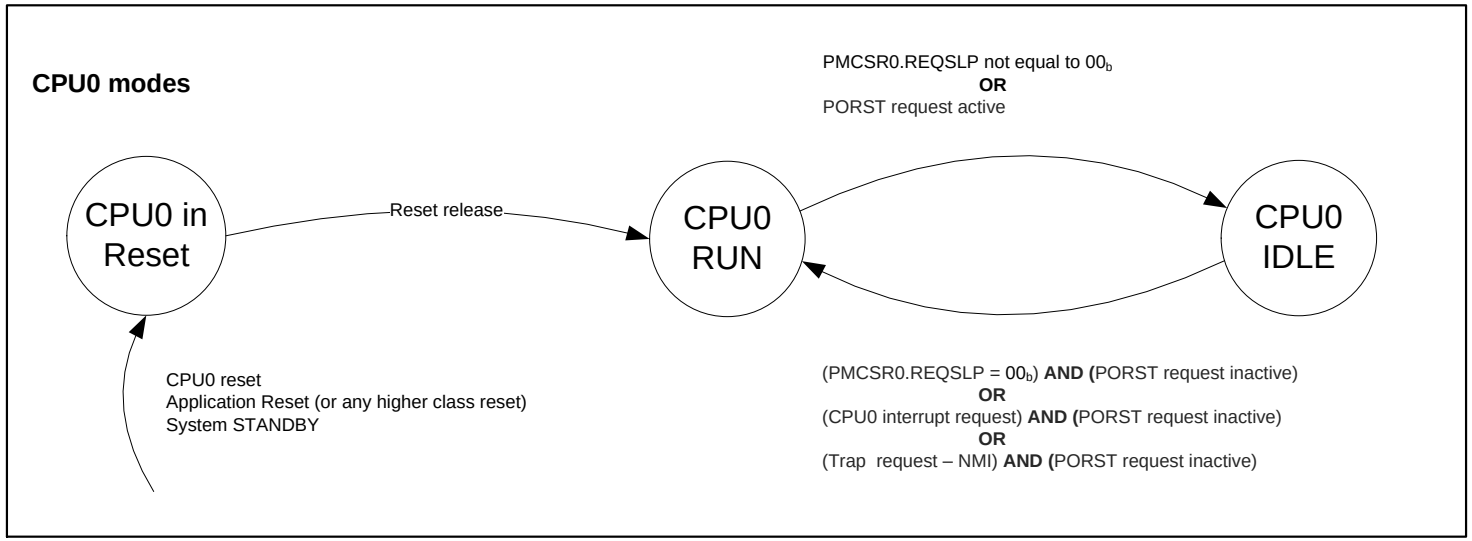
Power Management
Idle, Sleep & Standby modes

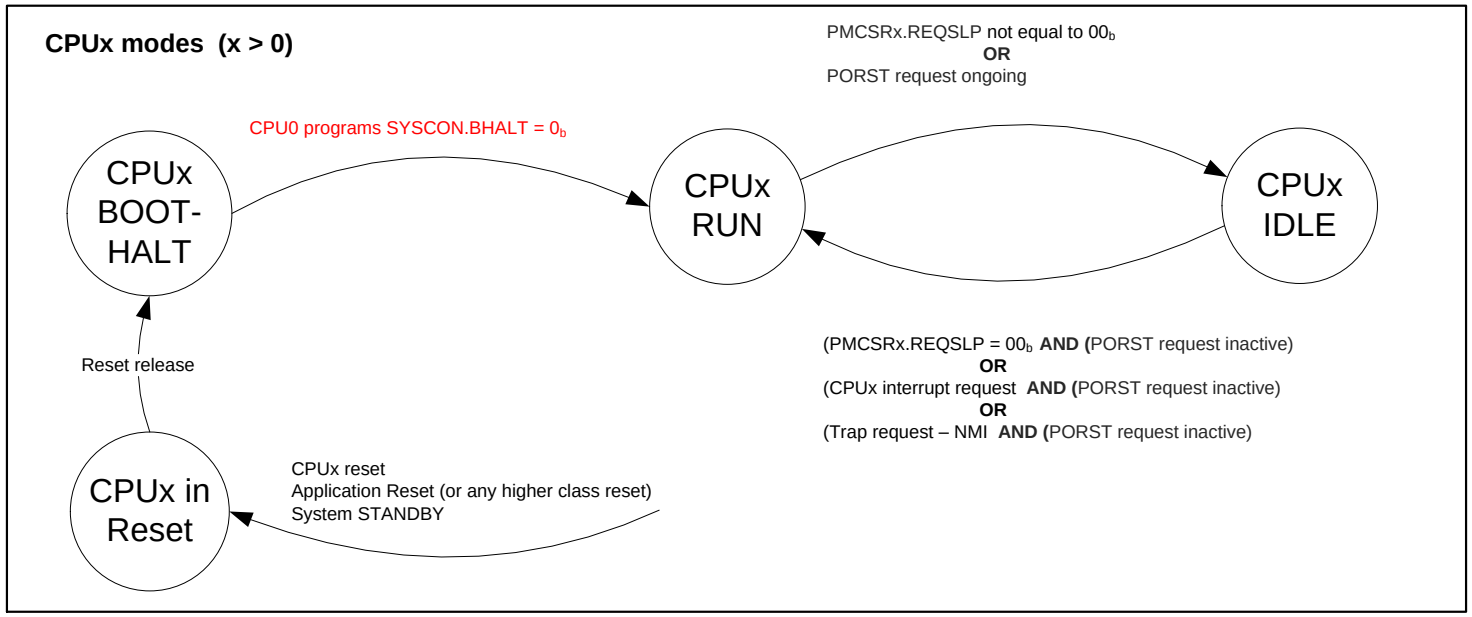
Mode / Current	Description	Entry / Exit
CPUx RUN	Normal operation	
CPUx IDLE 20-100 mA / CPU	The CPU clock is disabled. DMI/PMI memories accessible. All Peripherals remain active.	Entry via Software, SMU Exit on CPUx Interrupt, Trap, Reset Entry / Exit duration : Few cycles
SYSTEM SLEEP >15 mA @ Tj=85°C	Peripheral Clocks are gated if configured in CLC register. All CPUs are set to Idle.	Entry via Software Exit on CPUx Interrupt, Trap, Reset Entry / Exit duration : Few cycles
SYSTEM STANDBY 150 uA @ Tj=55°C SCR< 5mA @20MHz	Main domain is powered off. Standby RAM may be active 8-bit SCR may be active	Entry via SW, NMI Exit on edge detection on NMI/pins, PORST assertion Incase of separate standby supply pin •Entry on V_{EXT} supply ramp-down •Wakeup on V_{EXT} supply ramp-up Entry duration ~ 1.2us UV detection +3 cycles Exit via normal boot ~ 2 ms

Power Management
System modes



Power Management
CPU modes

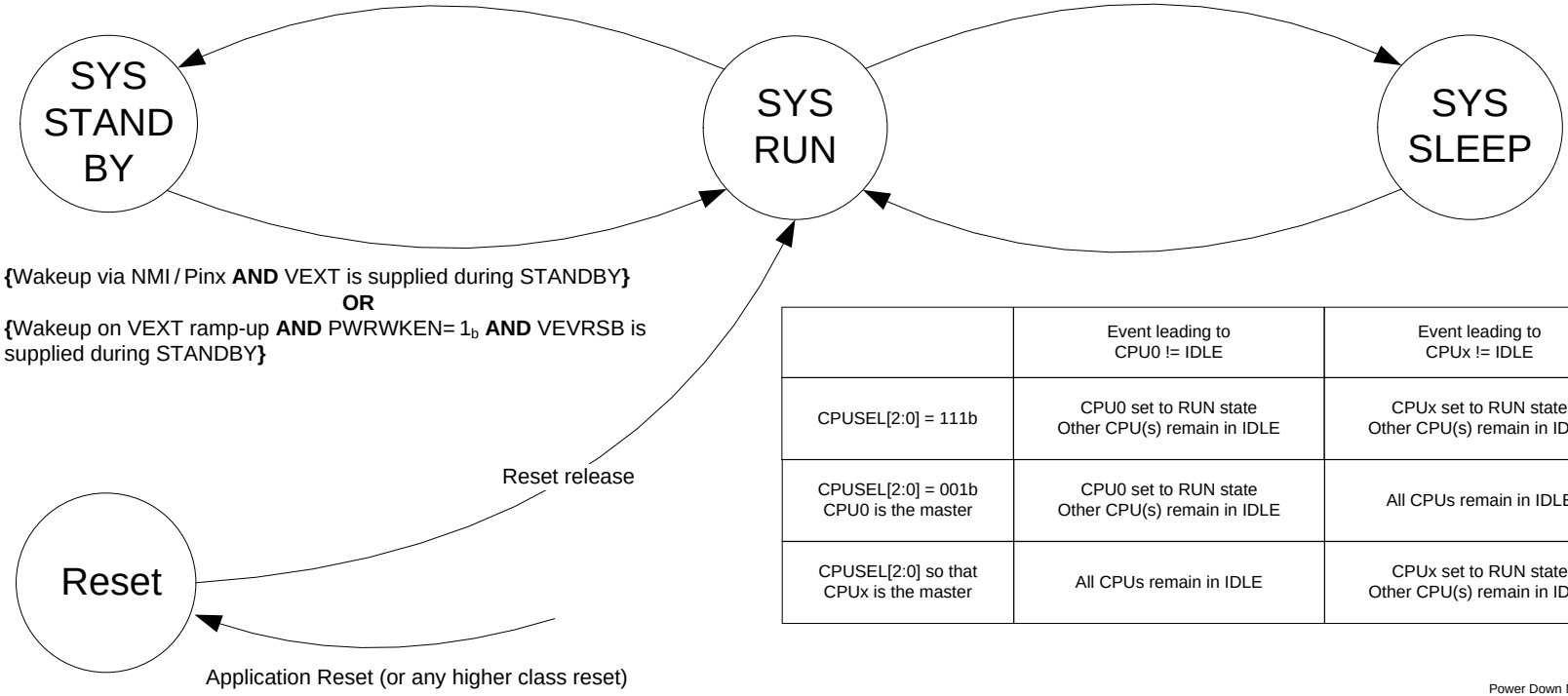




Power Management
System modes

{CPUSEL = 111_b **AND** STBYEV = 000_b **AND** PMCSRx.REQSLP **=** 11_b (x = any CPU)}
OR
{CPUx set as Master in CPUSEL **AND** STBYEV = 000_b **AND** PMCSRx.REQSLP$_b$ **=** 11_b}
OR
{VEVRSB is supplied during STANDBY **AND** VEXTSTBYEN = 1_b **AND** VEXT is ramped down during STANDBY and has currently reached configured SWDUV undervoltage threshold **}**
OR
{VEVRSB is supplied during STANDBY **AND** VDDSTBYEN = 1_b **AND** VDD is ramped down during STANDBY and has currently reached configured EVRCUV undervoltage threshold **}**
OR
{STBYEV = 100_b **AND** NMI / ESR1 is asserted externally**}**

{CPUSEL = 111_b **AND** PMCSRx.REQSLP **=** 10_b (x = any CPU)}
OR
{CPUx set as Master in CPUSEL **AND** PMCSRx.REQSLP$_b$ **=** 10_b}



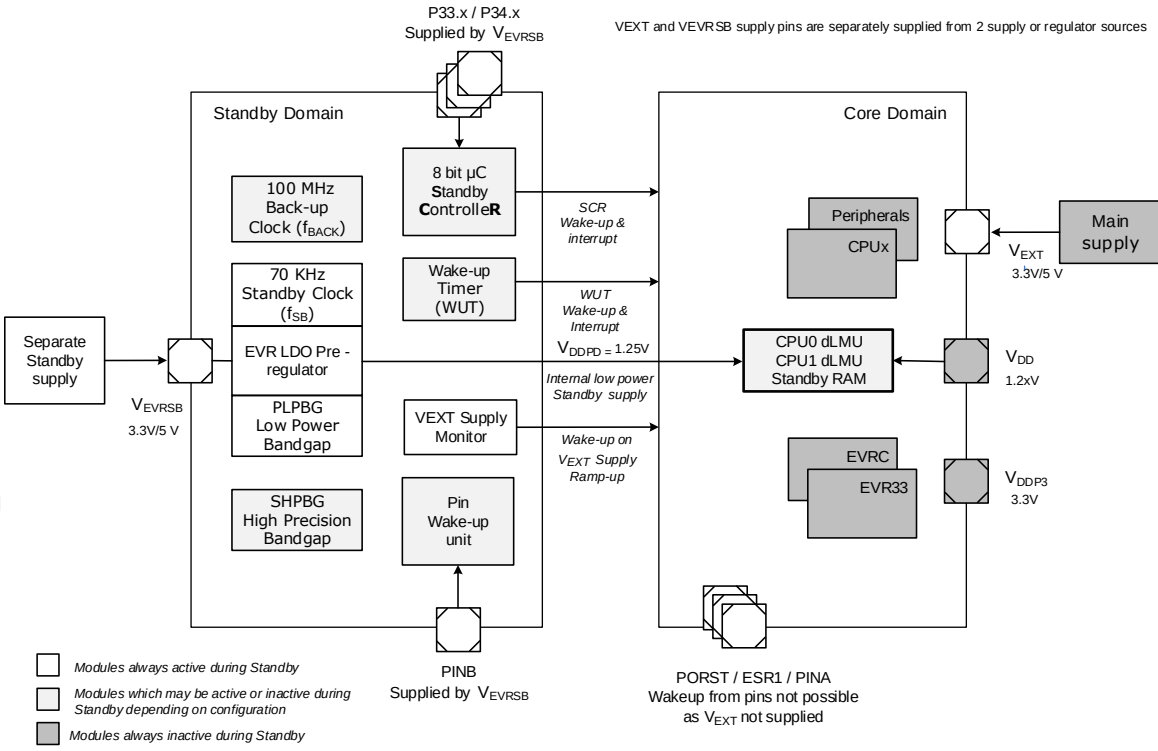
{Wakeup via NMI / Pinx **AND** VEXT is supplied during STANDBY**}**
OR
{Wakeup on VEXT ramp-up **AND** PWRWKEN= 1_b **AND** VEVRSB is supplied during STANDBY**}**

	Event leading to CPU0 != IDLE	Event leading to CPUx != IDLE
CPUSEL[2:0] = 111b	CPU0 set to RUN state Other CPU(s) remain in IDLE	CPUx set to RUN state Other CPU(s) remain in IDLE
CPUSEL[2:0] = 001b CPU0 is the master	CPU0 set to RUN state Other CPU(s) remain in IDLE	All CPUs remain in IDLE
CPUSEL[2:0] so that CPUx is the master	All CPUs remain in IDLE	CPUx set to RUN state Other CPU(s) remain in IDLE

Power Down Modes _v6

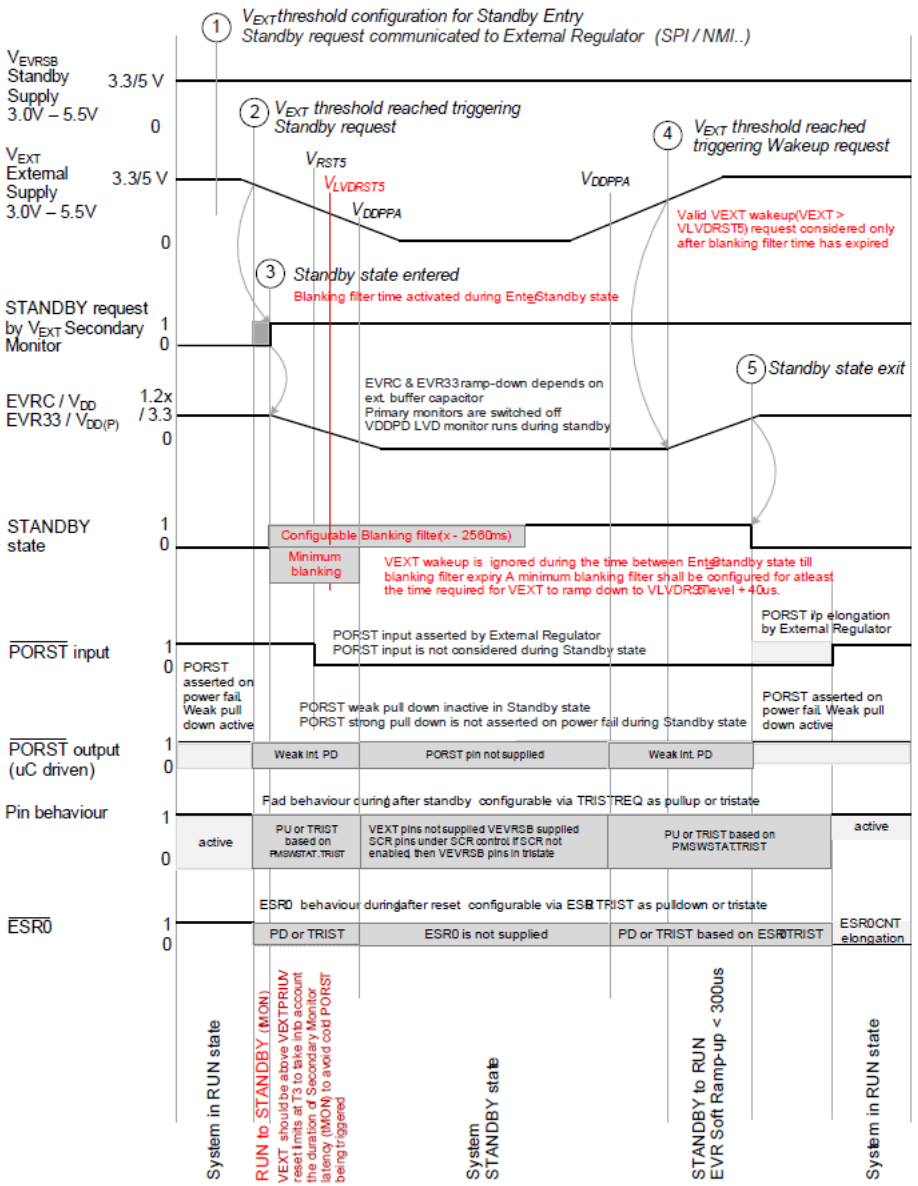
Power Management Standby Domain

- Constitutes
  - Standby RAM - CPU0 DLMU
  - Infrastructure components : Pre-regulator, 70 kHz clock …
  - Wakeup unit to detect edge on ESR1/CAN/ASC pins
  - Wake-up timer (WUT)
  - Integrated Standby Controller
- Separate Standby supply pin VEVRSB in all packages to supply Standby Pads, Standby RAM, SCR, …
- Standby entry and exit via VEXT supply ramp-up/down, Pins/NMI, SW/WUT …
- Standby current
  - <150 uA at T_junction = 25°C
- Wakeup time resolution of 70kHz or 70kHz/2^10
  - 14.3 us resolution : 14.3 us - 240 s range
  - 14.3ms resolution : 14.3ms - 2.7 days range



Power Management Standby Entry/Exit

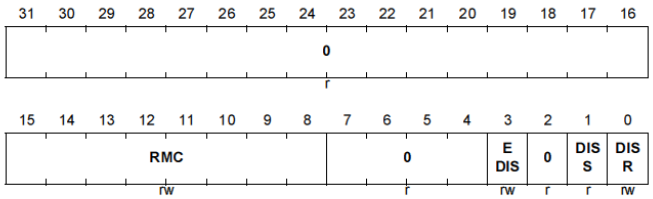
- System may enter Standby Mode on following events if so configured:
  - On a SW Standby request issued by setting PMCSRx.REQSLP= 11_B by the master CPU.
  - On a secondary undervoltage event during VEXT or VDD supply ramp-down.
  - On an NMI / ESR1 assertion event.
- System may exit Standby mode on following events
  - when VEXT supply ramps up.
  - when a Wake-up edge is detected on selected pins / ESR1 incase VEXT remains supplied
  - when a Wake-up request is issued by the 8 bit standby controller incase VEXT remains supplied
  - when PORST assertion is detected incase VEXT remains supplied



Power Management
Sleep Mode

- Entry
  - Modules Clocks would be gated if the module CLC.EDIS bit is configured to enable Sleep Mode.
  - Sleep request issued.

<>_CLC
Clock Control Register (00_H) Reset Value: $0000\ 0003_H$



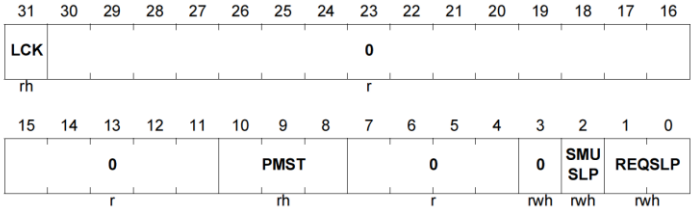
Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
RMC	[15:8]	rw	**8-bit Clock Divider Value in RUN Mode**
0	[31:16], [7:4], 2	r	**Reserved** Read as 0; should be written with 0.

REQSLP	[1:0]	rwh	**Idle Mode and Sleep Mode Request** 00_B Request CPU Run Mode 01_B Request CPU Idle Mode 10_B Request System Sleep Mode 11_B Request System Standby Mode [RfQ00092] In Idle Mode or Sleep Mode, these bits are cleared in response to an interrupt for the CPU, or when bit 15 of the corresponding System Watchdog Timer (bit WDTSSR.TIM[15]) or CPU Watchdog Timer count register (bit WDTCPUxSR.TIM[15]) changes from 0 to 1. In Standby Mode, these bits are cleared on wake-up.

PMCSR0
Power Management Control and Status Register
($0D4_H$) Reset Value: $0000\ 0100_H$

PMCSR1
Power Management Control and Status Register
($0D8_H$) Reset Value: $0000\ 0100_H$

PMCSR2
Power Management Control and Status Register
($0DC_H$) Reset Value: $0000\ 0100_H$



Agenda

1. Power Supply and Control
2. Power Management
3. Monitoring and Reset
4. Power Consumption

TC3xx
Supply Rails & Monitoring

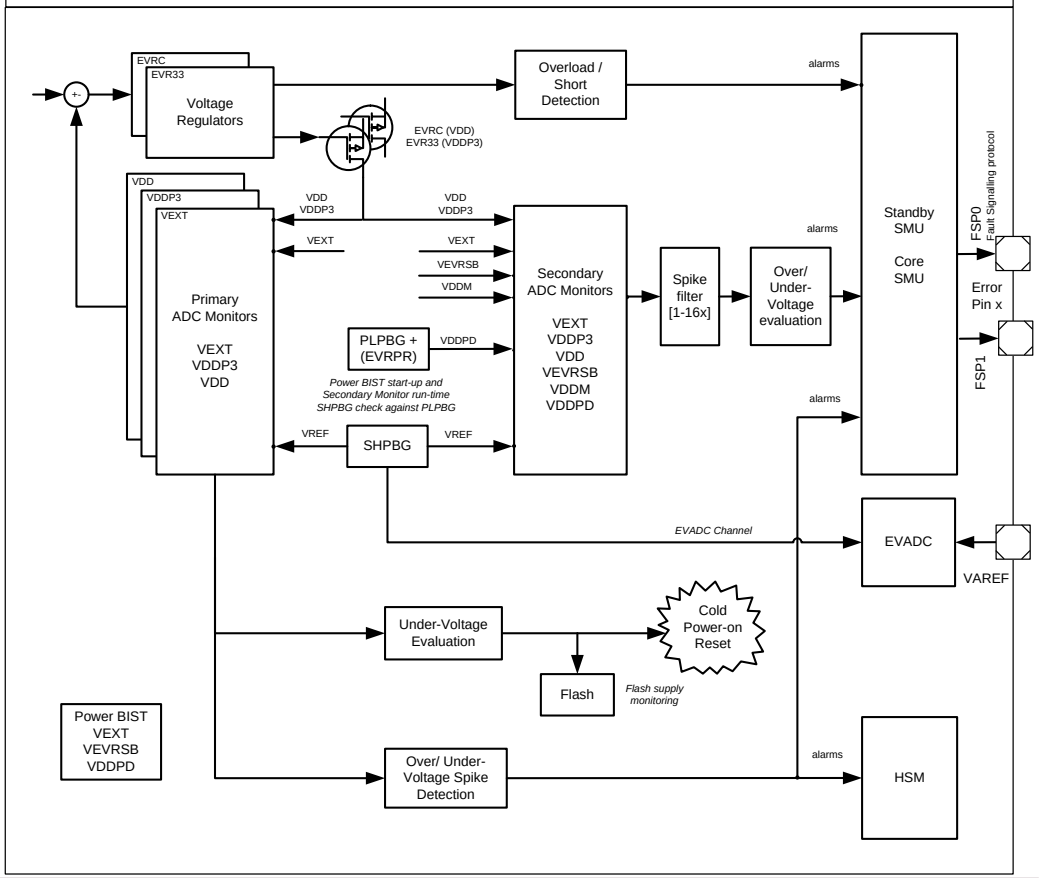
PRIMARY MONITORS
- VEXT External supply
- VDDP3 supply or EVR33 output
- VDD supply or EVRC output

Short / Overload Detection
- EVR33 short to supply / ground
- EVRC short to supply / ground

SECONDARY MONITORS
- VEXT External supply OV&UV
- VDDP3 supply or EVR33 OV&UV
- VDD supply or EVRC OV&UV
- VDDPD Pre-Reg supply OV&UV
- VDDM ADC supply OV&UV
- VEVRSB Standby supply OV&UV

EVADC BANDGAP MONITORING
- VDDPD / SHPBG (using EVADC)

Power Built In Self Tests
- VEXT OV/UV
- VDDPD OV/UV (PLPBG vs SHPBG OV / UV)
- VEVRSB OV/UV



Embedded Voltage Regulators
Voltage Monitoring and Reset

- Primary Undervoltage monitoring carried out on all supplies on non configurable thresholds violation of which leads to reset
  - 5V or 3.3V primary reset @ 2.97 – xV
  - 3.3V primary reset @ 2.97 - xV
  - 1.25V primary reset @ 1.13 – xV
- Secondary Over and Undervoltage monitoring based on a second bandgap. Configurable thresholds for Secondary Over and Undervoltage monitoring
  - Configurable 5V or 3.3V external supply secondary monitoring between 2.97 – 5.5 V
  - 3.3V monitoring between 2.97 – 3.63 V
  - 1.25V monitoring between 1.13 – 1.375 V
- Bandgap Monitoring
  - 2 Bandgaps based on different topologies located in different domains are compared against each other

RSTSTAT
Reset Status Register (050_H) Reset Value: $0001\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						SWD	EVR33	EVR13	0		CB3	CB1	CB0	OCDS	PORST
r						rh	rh	rh	r		rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								STM2	STM1	STM0	SW	SMU	0	ESR1	ESR0
r								rh	rh	rh	rh	rh	r	rh	rh

EVRSTAT
EVR Status Flag Register ($0B0_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

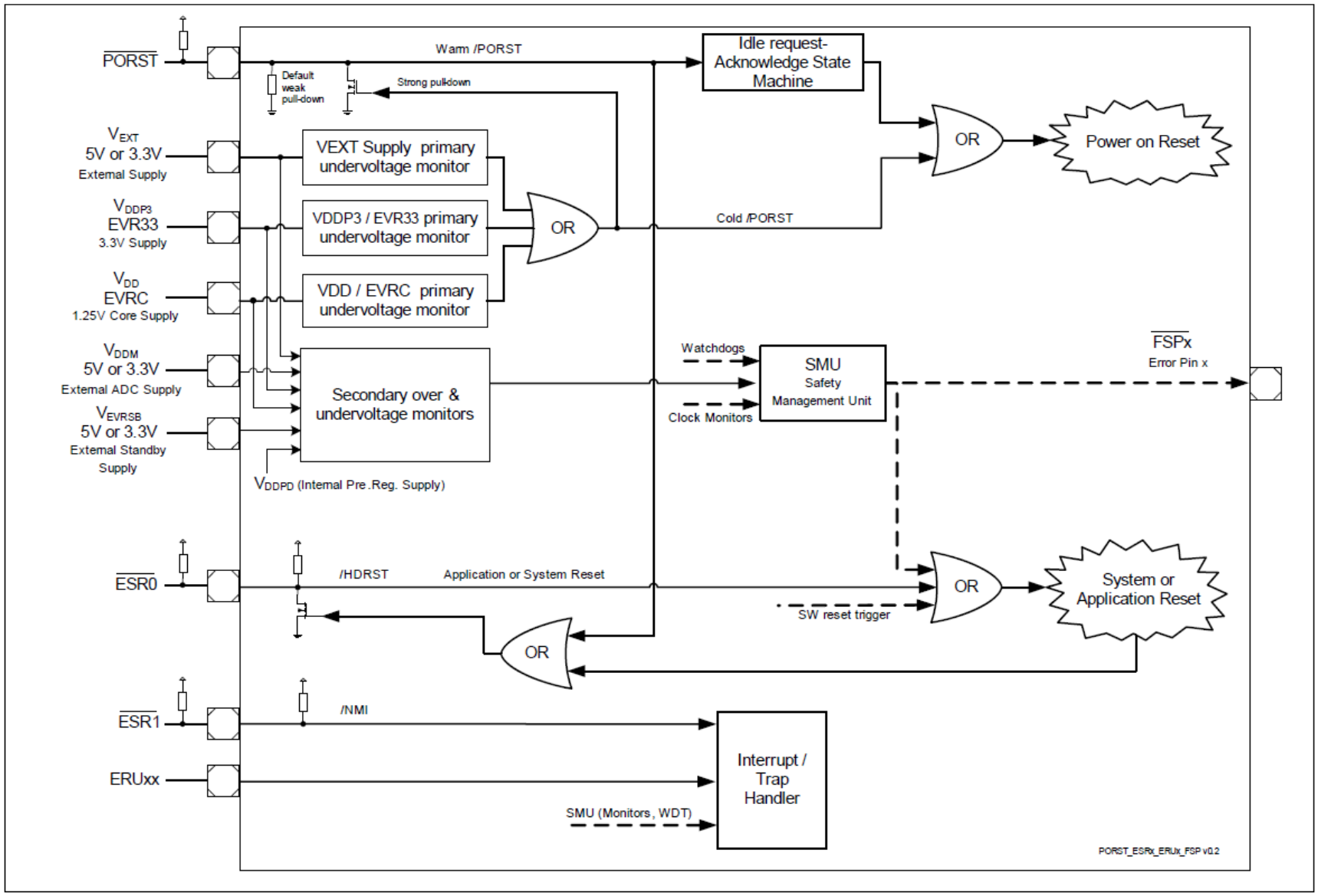
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				STBYREG	BGPROK	0	EXTPASS13	UVSWD	UV33	UV13	OVSWD	OV33	0	OV13	0
r				rw	rh	rh	rh	rh	rh	rh	rh	rh	r	rh	r

EVRADCSTAT
EVR ADC Status Register ($19C_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL	0							ADCSWDV							
rh	r							rh							

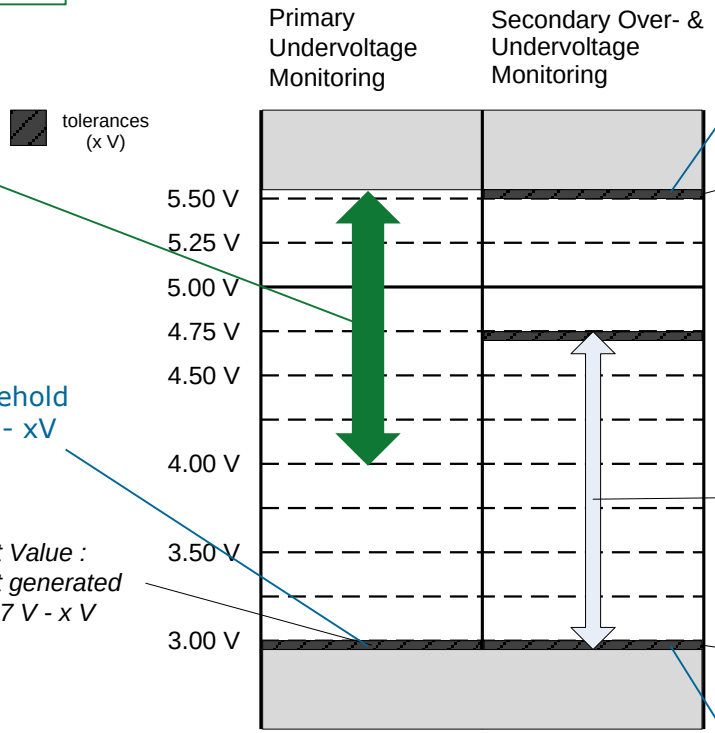
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC33V								ADC13V							
rh								rh							

TC3xx
Voltage Monitoring and Reset Pins



External Supply
Internal Monitoring Mechanisms

Functional range
• **4.0V to 5.5V**



Overvoltage monitoring
- Overvoltage monitoring is based on a second band-gap
- Default after reset : **interrupt at 5.5V + x V**
- The monitor could be later programmed to trigger a reset.
- The threshold is not configurable

V_{DDP5}	SR	4.5	5.0	5.5	V	operation range all pad parameters for AL are valid
		4.0	-	4.5	V	PT crank range; reduced pad parameters for TTL operation are valid
		2.97	-	4.0	V	Body crank range; reduced pad parameters for TTL operation are valid

- Incase of V_{EXT} > 4.0V, both 1.25V and 3.3V internal regulators are functional.
- Incase of V_{EXT} > 3.0V, 1.25V regulator is functional. Incase the voltage drops upto 3.0V (cranking) , it should be taken care to switch off the 3.3V LDO regulator.

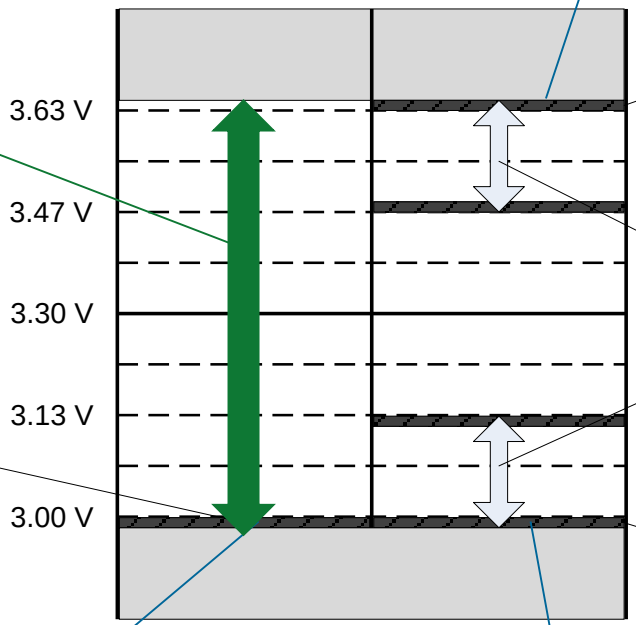
Undervoltage monitoring
- Undervoltage monitoring is based on a second band-gap
- Default after reset : **interrupt at 2.97 - x V**
- The monitor could be later programmed to trigger a reset.
- The threshold is configurable between (2.97-x) - 4.75 V

x V – Production Tolerances/Trimming on the threshold values have to be additonally considered

EVR33 – 3.3V Supply
Internal Monitoring Mechanisms

Functional range
• **2.97V to 3.63V**

Overvoltage monitoring
• Overvoltage monitoring is based on a second band-gap
• Default after reset : **interrupt at 3.63V + x V**
• The monitor could be later programmed to trigger a reset.
• The threshold is configurable between 3.47 – (3.65+x) V



EVR33 Voltage Monitor

Reset Value:
Interrupt generated
at EVR33OVVAL=
3.63 V + x V

EVR33OVVAL range
= 3.47 – (3.63 V + x V)

EVR33UVVAL range
= (2.97 V - x V) – 3.13 V

Reset Value :
Reset generated
at 2.97 V - x V

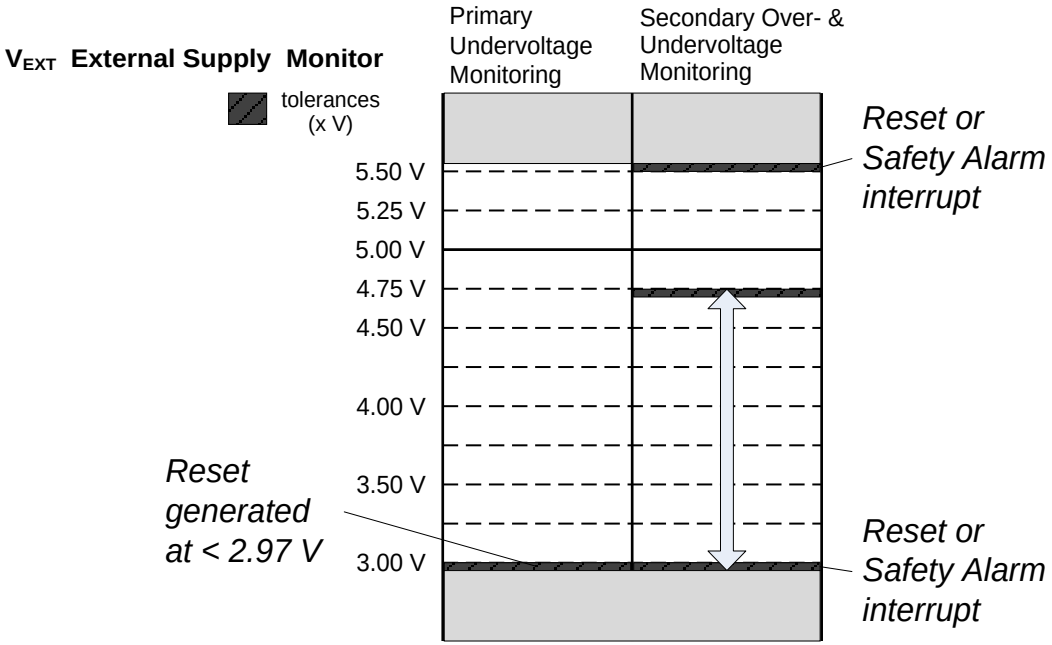
Reset Value :
Interrupt generated
at EVR33UVVAL=
2.97 V - x V

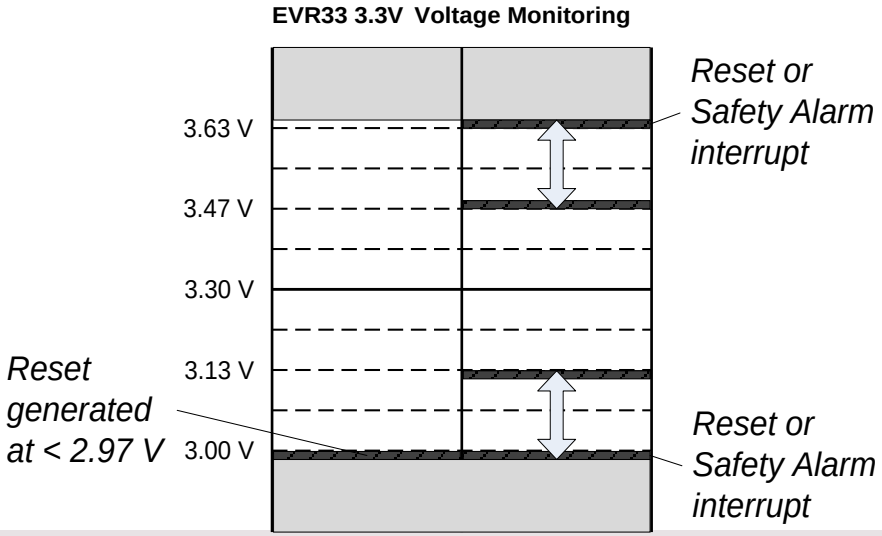
Primary Reset threhold
trimmed @ 2.97 - xV

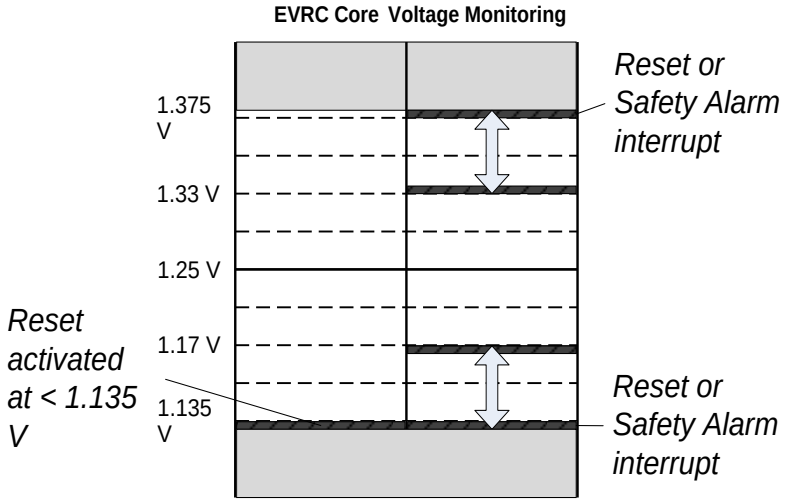
Undervoltage monitoring
• Undervoltage monitoring is based on a second band-gap
• Default after reset : **interrupt at 2.97 - x V**
• The monitor could be later programmed to trigger a reset.
• The threshold is configurable between (2.97-x) - 3.13 V

x V – Production Tolerances/Trimming on the threshold values have to be additonally considered

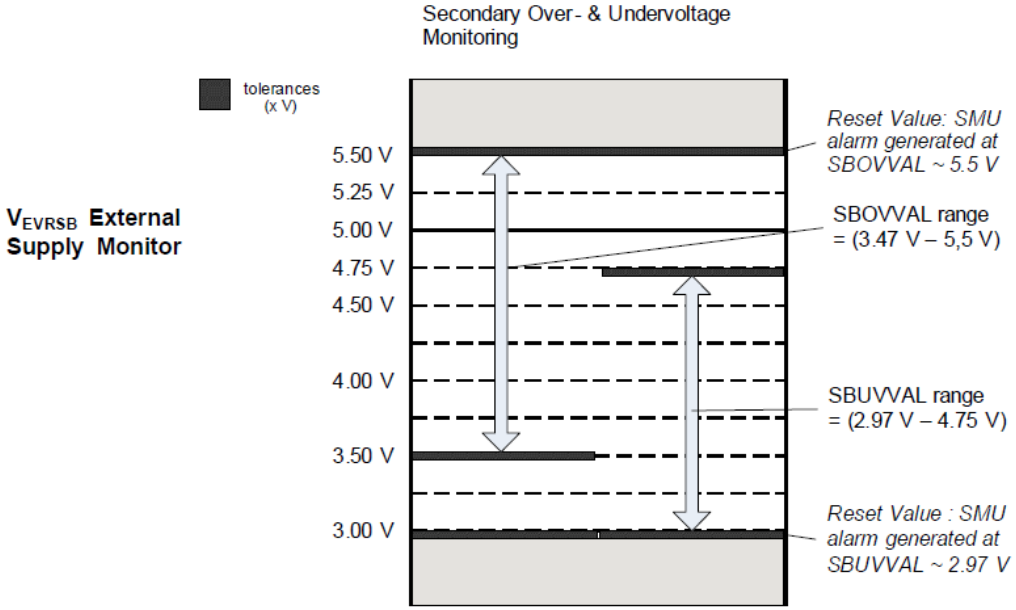
Power Supply and Control
Voltage Monitoring and Supply Range

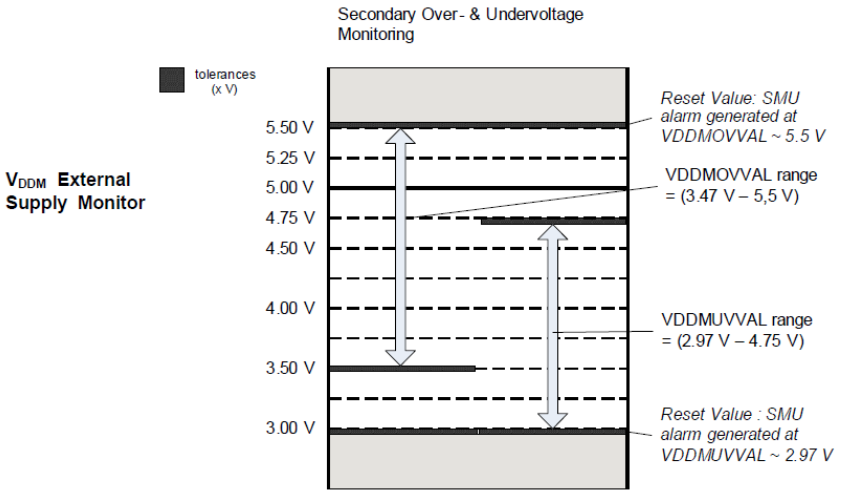


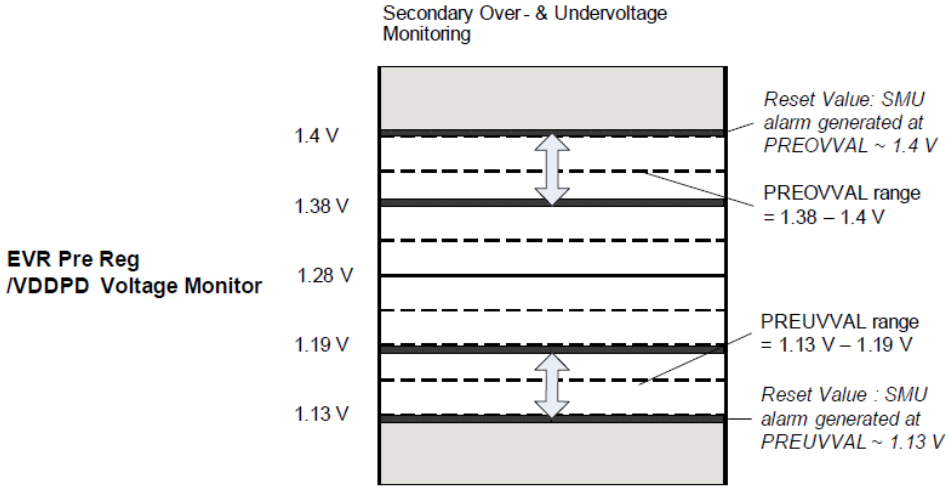




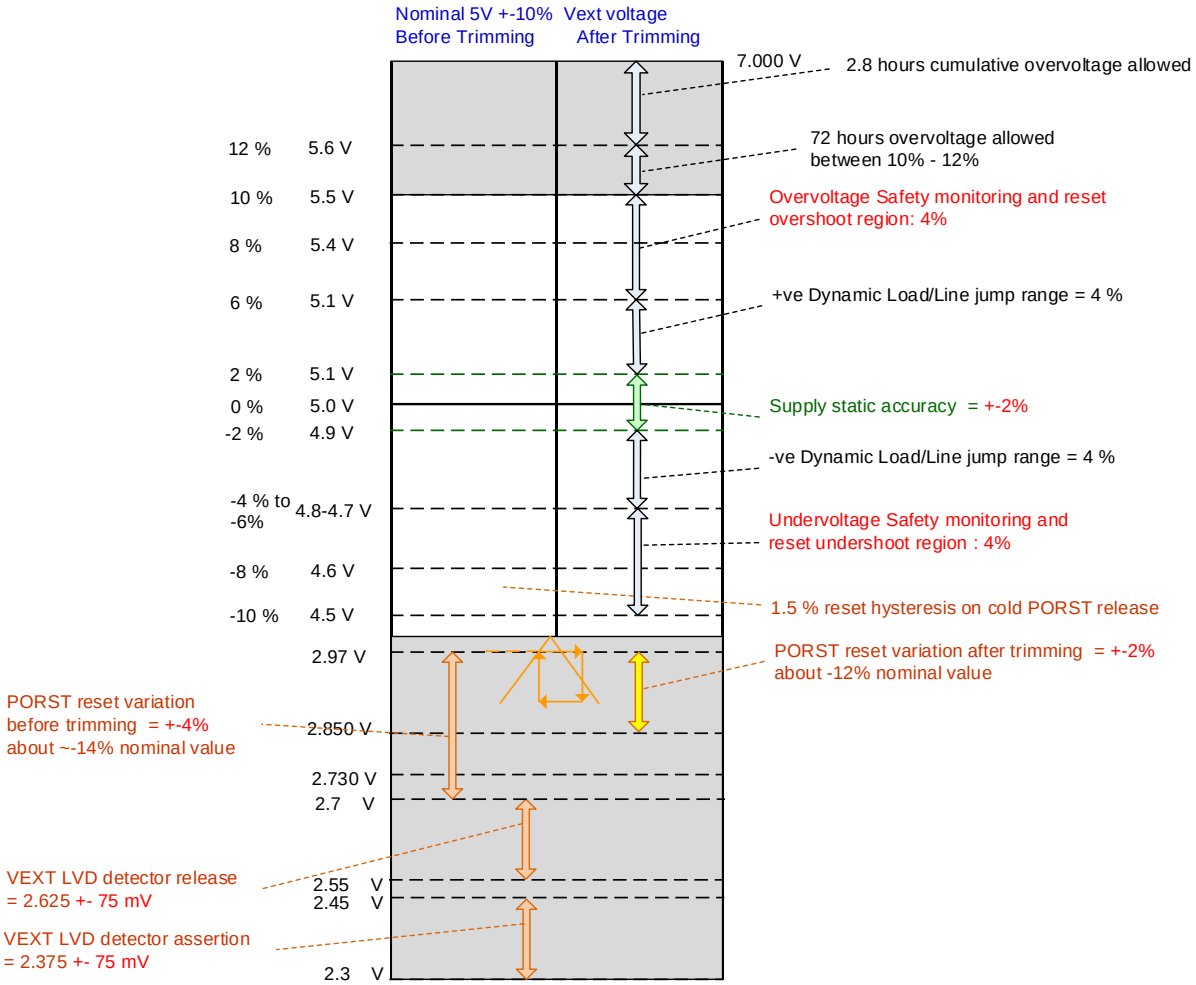
Power Supply and Control
Voltage Monitoring and Supply Range







AURIX TC3xx
VEXT Voltage Profile



VEXT Range and Lifetime Profile 1

(Triangular Pulse forms)

5.6 V - 7.0 V - 2.8 hours

5.5 V - 5.6 V - 72 hours

5.4 V - 5.5 V - 5 % of lifetime

5.1 V - 5.4 V - 15 % of lifetime

4.9 V - 5.1 V - 60 % of lifetime

4.6 V - 4.9 V - 15 % of lifetime

4.5 V - 4.6 V - 5 % of lifetime

VEXT Range and Lifetime Profile 2 (evaluation ongoing)

(Rectangular Pulse forms)

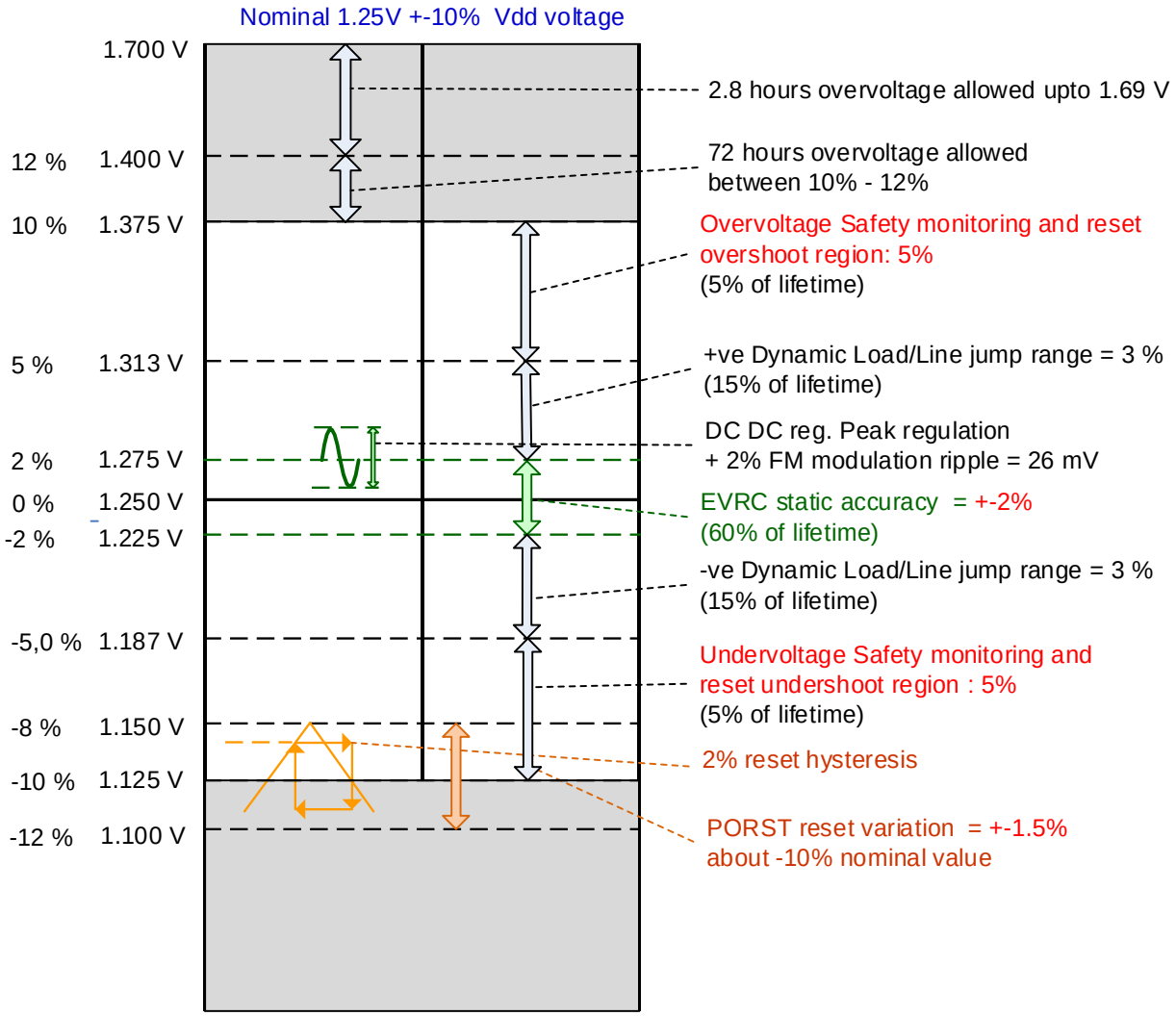
5.6 V – 6.5 V - 60 hours with additional failure rate impact of < 1PPM

5.3 V - 5.6 V - 100 hours

4.7 V - 5.3 V - 100 % of lifetime

4.5 V - 4.7 V -

AURIX TC3xx
VDD Core Voltage Profile



VDD Range and Lifetime Profile 1

1.400 V-1.700V – 2.8h (300us pulses cumulated)

1.375 V-1.400 V - 72 hours

1.313 V-**1.375 V** - 5 %

1.275 V-1.313 V - 15 %

1.225 V-1.275 V - 60 %

1.187 V-1.225 V - 15 %

1.125 V-1.187 V - 5 %

VDD Range and Lifetime Profile 2 (evaluation ongoing)

(Rectangular Pulse forms)

1.400 V-1.625V - 60 hours with additional failure rate impact of < 1PPM

1.325 V-1.400V - 72 hours

1.175 V-1.325V - 100 % of lifetime

1.125 V-1.175 V -

Agenda

1. Power Supply and Control
2. Power Management
3. Monitoring and Reset
4. Power Consumption

TC39x Power Supply Current

∑ Sum of all currents (incl. $I_{EXTRAIL}$+$I_{DDMRAIL}$+$I_{DDx3RAIL}$+I_{DD})	I_{DDTOT} CC	-	-	1536	mA	real power pattern; T_J=150°C
		-	-	1720	mA	real power pattern; TJ=160°C
∑ Sum of all currents with DC-DC EVRC regulator active [3]	$I_{DDTOTDC3}$ CC	-	-	980	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V; T_J=160°C
∑ Sum of all currents with DC-DC EVRC regulator active [3]	$I_{DDTOTDC5}$ CC	-	-	670	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 5V; T_J=160°C
∑ Sum of all currents (SLEEP mode)	I_{SLEEP} CC	-	-	25	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB}$ = 1 MHz via LPDIV divider; T_J = 25°C
∑ Sum of all currents (STANDBY mode) drawn at V_{EVRSB} supply pin	$I_{STANDBY}$ CC	-	-	150 [4]	µA	64 KB Standby RAM block active. SCR inactive. Power to remaining domains switched off. T_J = 25°C; V_{EVRSB} = 5V
Maximum power dissipation	PD SR	-	-	3220	mW	max power pattern
		-	-	2500	mW	real power pattern

Power Calculation Sheet

This is the excel sheet AURIX2G_Power_Calc_1.4.7. Please read the “readme” page first.

Input				Datasheet / Reference Values (Real Pattern) Please update the latest values from datasheet.							Output							
Input parameter	Allowed Range / Values / Modules available	Input Value	Unit	Datasheet / Reference Parameters Real Pattern Current Consumption	Modules active /Value	IDD	IDDP3	IEXT / IFLEX / IEVRSB	IDD M	Unit	Output Parameter	IDD	IDDP3	IEXT / IFLEX / IEVRSB	IDDM	Value / Total	Unit	Estimation Accuracy
Ambient Temperature (Ta)	55°C - 125°C	115,9	[°C]	Maximum Junction Temperature		165				[°C]								
Package	SAL, SAK or Bare Die			Maximum Package Temperature		150				[°C]								
RTH_JA of ECU	application dependent	12	[K/W]															
RTH_JB at balls / pins in contact with P	application dependent		[K/W]															
Max Allowed PCB temperature	application dependent	MAX	[°C]								Actual Pin / Ball Temperature (Tb)							
Typical or **M**aximum (FF) leakage	T or M	M		Total IDDRAIL = Static (IDDPORST) + Dynamic (IDDDYN) @ Tj=150°C		1450				[mA]	Actual Junction Temperature (Tj)					150,0	[°C]	
VDD Voltage incl. +ve tolerance	1.25V + 2% upto + 10%	1,275	[V]	Static leakage @ Tj=150°C (IDDPORST)		655				[mA]	Static Leakage current	662					[mA]	±20%
Device		TC39xB		Dynamic current contribution (IDDDYN = IDDRAIL - IDDPORST)		795				[mA]	Dynamic Current	819					[mA]	±20%
Main System / SRI bus frequency	40MHz - 300MHz	300	[MHz]	SRI dynamic base load current w/o CPUs, Flash @ 300 MHz (IDDSRI_w/oCPU,Flash)		66				[mA]	SRI current w/o CPUs	66					[mA]	±20%
SPB or Peripheral bus frequency	40MHz - 100MHz	100	[MHz]	SPB dynamic base load current w/o SPB peripherals contribution below (IDDSPB)	60	20				[mA]	SPB current w/o GTM and SPB peripherals below	20					[mA]	±20%
CPU5 frequency(CPU5DIV)	0MHz - 300MHz	300	[MHz]															
CPU5 IPC rate	0,6(real) - 1,2(max)	0,6	[IPC]	CPU5 current (IDDC50) real (IPC = 0.6)	1	40				[mA]	CPU5 current	40					[mA]	±10%
CPU4 frequency(CPU4DIV)	0MHz - 300MHz	300	[MHz]															
CPU4 IPC rate	0,6(real) - 1,2(max)	0,6	[IPC]	CPU4 current (IDDC40)	1	40				[mA]	CPU4 current	40					[mA]	±10%
CPU3 frequency(CPU3DIV)	0MHz - 300MHz	300	[MHz]															
CPU3 Lockstep Active	Y or N	Y		CPU3 lockstep (IDDC31-IDDC30)	1	40				[mA]	CPU3 lockstep current	40					[mA]	±10%
CPU3 IPC rate	0,6(real) - 1,2(max)	0,6	[IPC]	CPU3 current (IDDC30)	1	40				[mA]	CPU3 current	40					[mA]	±10%
CPU2 frequency (CPU2DIV)	0MHz - 300MHz	300	[MHz]															
CPU2 Lockstep Active	Y or N	Y		CPU2 lockstep (IDDC21-IDDC20)	1	40					CPU2 lockstep current	40					[mA]	±10%
CPU2 IPC rate	0,6(real) - 1,2(max)	0,6	[IPC]	CPU2 current (IDDC20)	1	40				[mA]	CPU2 current	40					[mA]	±10%
CPU1 frequency (CPU1DIV)	0MHz - 300MHz	300	[MHz]															
CPU1 Lockstep Active	Y or N	Y		CPU1 lockstep (IDDC11-IDDC10)	1	40				[mA]	CPU1 lockstep current	40					[mA]	±10%
CPU1 IPC rate	0,6(real) - 1,2(max)	0,6	[IPC]	CPU1 current (IDDC10)	1	40				[mA]	CPU1 current	40					[mA]	±10%
				CPUx lockstep (IDDCx1-IDDCx0) max (IPC = 1.2) @ 300														

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