AURIX 2G Queued Serial Peripheral Interface(QSPI) Overview

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Overview

- SPI overview.
- QSPI Introduction
- QSPI Clocking & Baud rate generation
- Frame Timing
- Configuration & Queue concept
- User Interface (FIFO registers usage)
- FIFO interrupts

TC2XX vs TC3XX

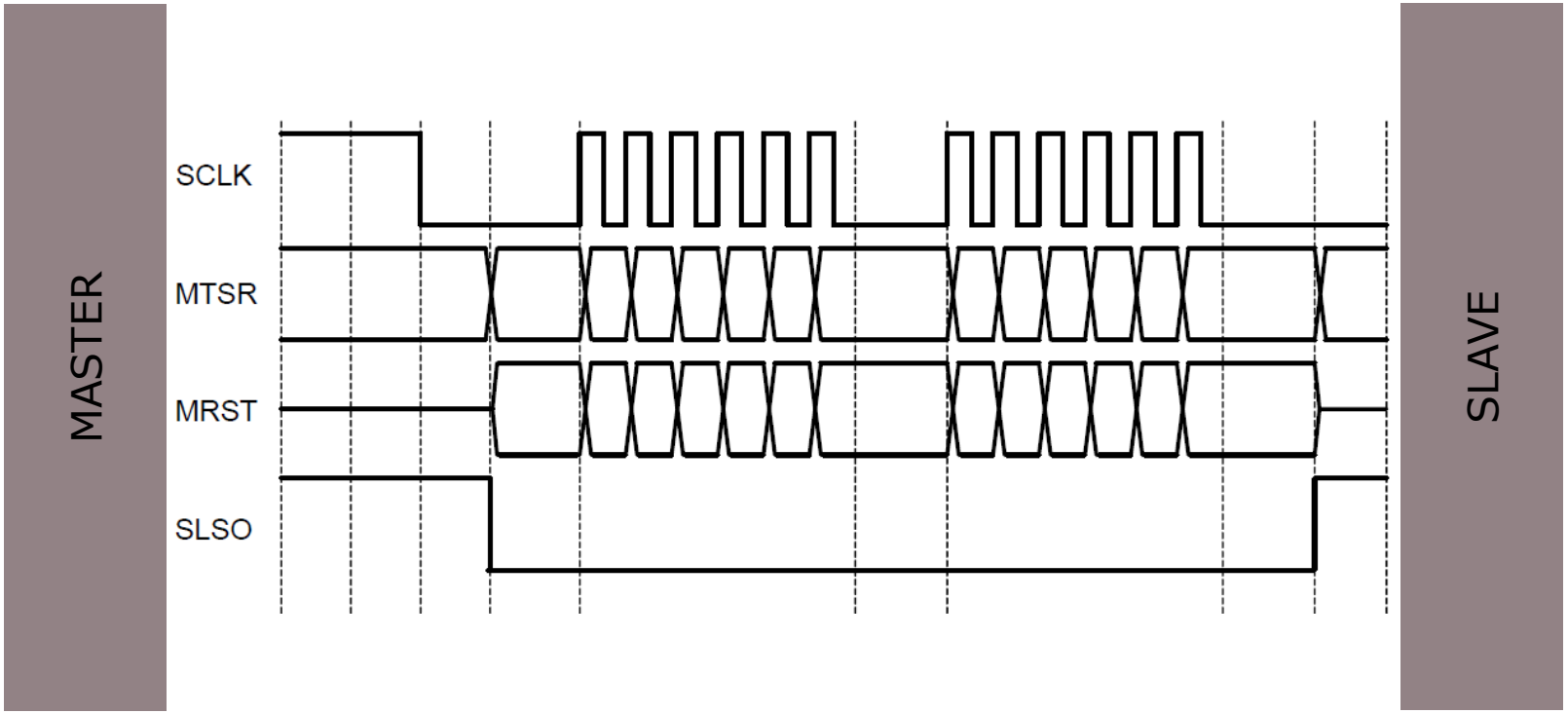
- Baud rates generated from the ***peripheral PLL***, asynchronous to the system PLL.
  - Clock has to be enabled/configured in the CCU – **different from A1G!!**

- New mode: **Move Counter Mode**
  - Basically Continuous mode with short data, but without the need for the extra BACON for the last word.

Agenda

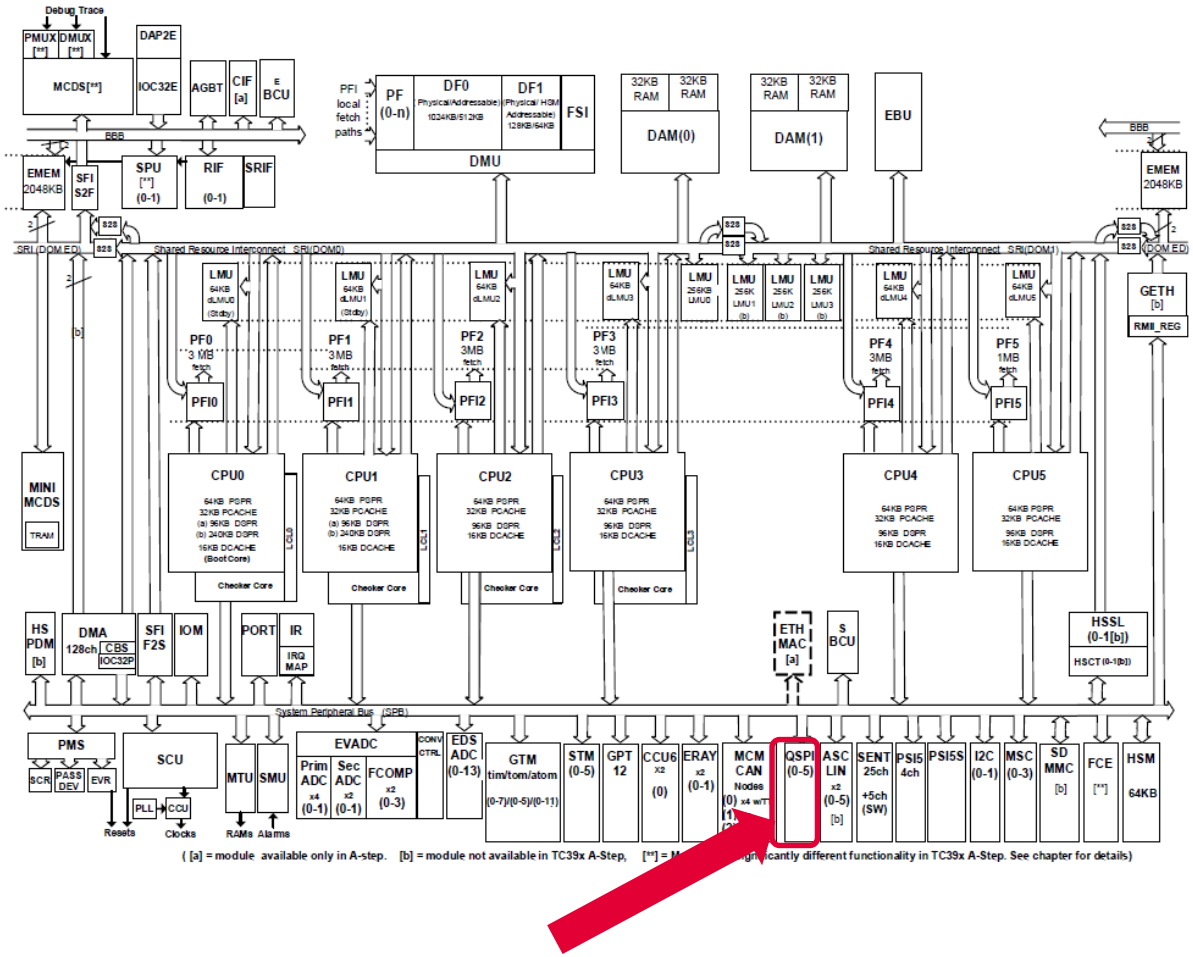
1. QSPI Overview
2. QSPI Features
3. QSPI Clocking & Baud rate generation
4. QSPI Frames
5. Concepts of QSPI
6. QSPI User Interface
7. QSPI FIFO Interrupts (and move modes)
8. Conclusion

Serial Peripheral Interface (SPI)

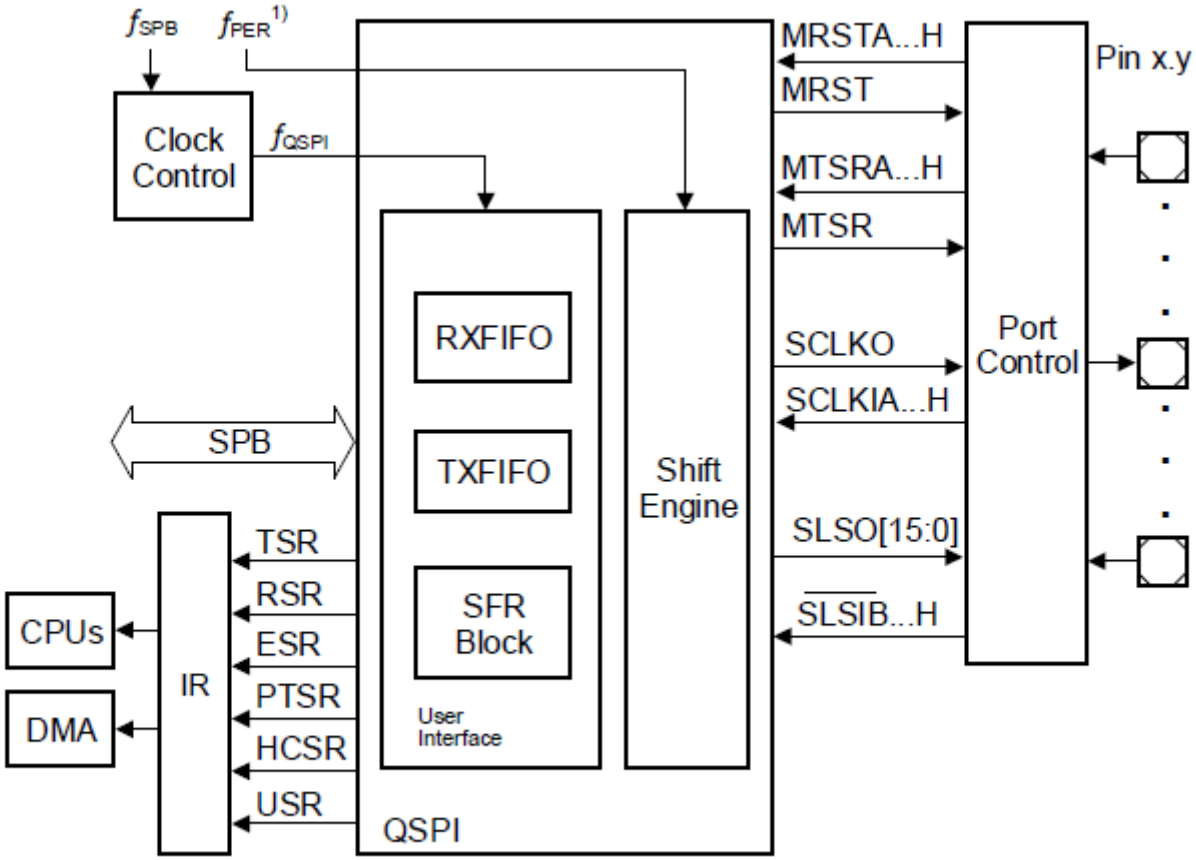


QSPI: Infineon's SPI controller

- Block Diagram of TC39x
- 6 QSPI instances, each addressed separately on the SPB.
- Each QSPI Instance: Upto 16 Channels



QSPI Block Diagram



1) f_{PER} is the frequency originating from the peripheral PLL, referred to as f_{QSPI} in the SCU.CCU (Clock Control Unit) chapter.

QSPI_Intro+.vsd

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QSPI Features

- Master and Slave full duplex operation.
- 4x32-bit Tx and Rx FIFOs
- Flexible Frame Length
  - Short Data mode (2-32 Bits)
  - Long Data Mode (Upto 32 Bytes)
  - Continuous mode (Long data)
  - Extra Large Data (XXL): Up-to 65536 bytes.
- Flexible Frame format
  - Different polarities, phases
  - Shift direction (MSB, LSB)
  - Parity
  - Big endian (Byte swap)
- Flexible Timing
  - Programmable delays, duty cycle, data sampling.
  - Buad- generation: Upto 50Mbps (Max. supported depends on the pads)
  - SLSO timing.

QSPI Features (Contd..)

- "Q"SPI: Queue Support
  - Configuration and data: Via the same Queue (Tx or Rx FIFO)
  - Depending on the Slave, the configuration can be different. (In next slides)

- Interrupt signals
  - FIFO events, Errors and Phase transitions.
  - 6 interrupts per QSPI module.
  - Easy programmability with DMA.

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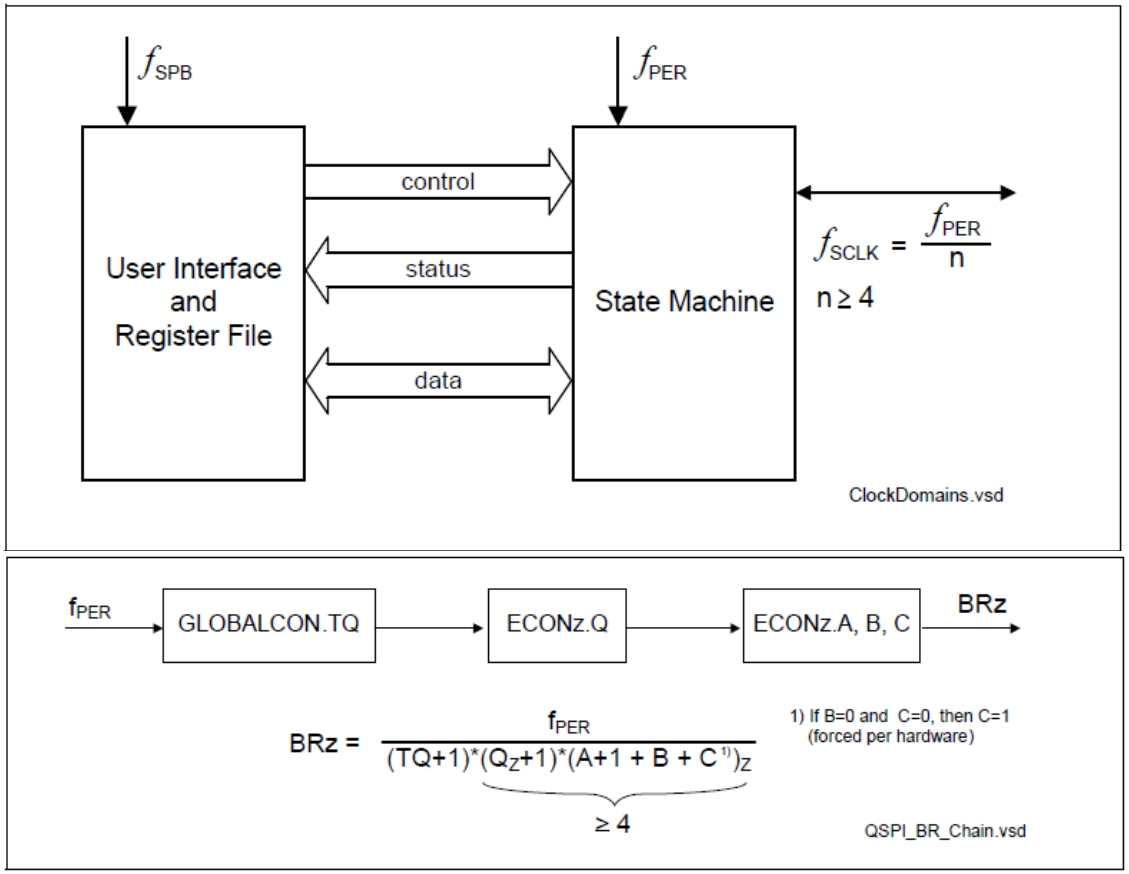
QSPI Clock Sources



CCUCON1
CCU Clock Control Register 1 (034_H) Reset Value: $1010\ 0002_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LCK	0	CLKSELQSPI		QSPIDIV				0		CLKSELMSC		MSCDIV			
rh	rw	rw		rw				rw		rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				0				PLL1DIVDIS	0	CLKSELMCAN		MCANDIV			
rw				rw				rw	rw	rw		rw			

- f_{SPB} & $f_{SOURCEQSPI}$ from CCU
  - To be configured via CLKSELQSPI & QSPIDIV in CCUCON1 Register.
- ECONz: ECON0-ECON7.
- 8 Registers for 16 Channels.
- Configuration of Baud-Rate for each channel:
  - CH0-7: ECON0-7
  - CH8-15 ⇔ CH0-7

QSPI Baudrate

- Baudrate settings
  - Channel specific Time Quanta setting in reg ECONz

Q	[5:0]	rw	**Time Quantum** Defines the time quantum length used by A, B, and C to define the baud rate and duty cycle. 000000_B 1 000001_B 2 …B … 111111_B 64

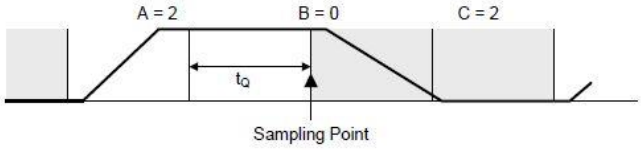
A	[7:6]	rw	**Bit Segment 1** Length expressed in T_Q time units 00_B 1 01_B 2 10_B 3 11_B 4

B	[9:8]	rw	**Bit Segment 2** Length expressed in T_Q time units 00_B 0 01_B 1 10_B 2 11_B 3

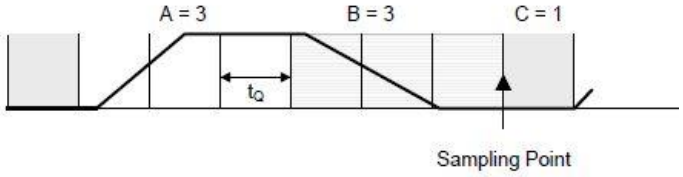
C	[11:10]	rw	**Bit Segment 3** Length expressed in T_Q time units 00_B 0 (if B=0, than C is minimum 1 per hardware) 01_B 1 10_B 2 11_B 3

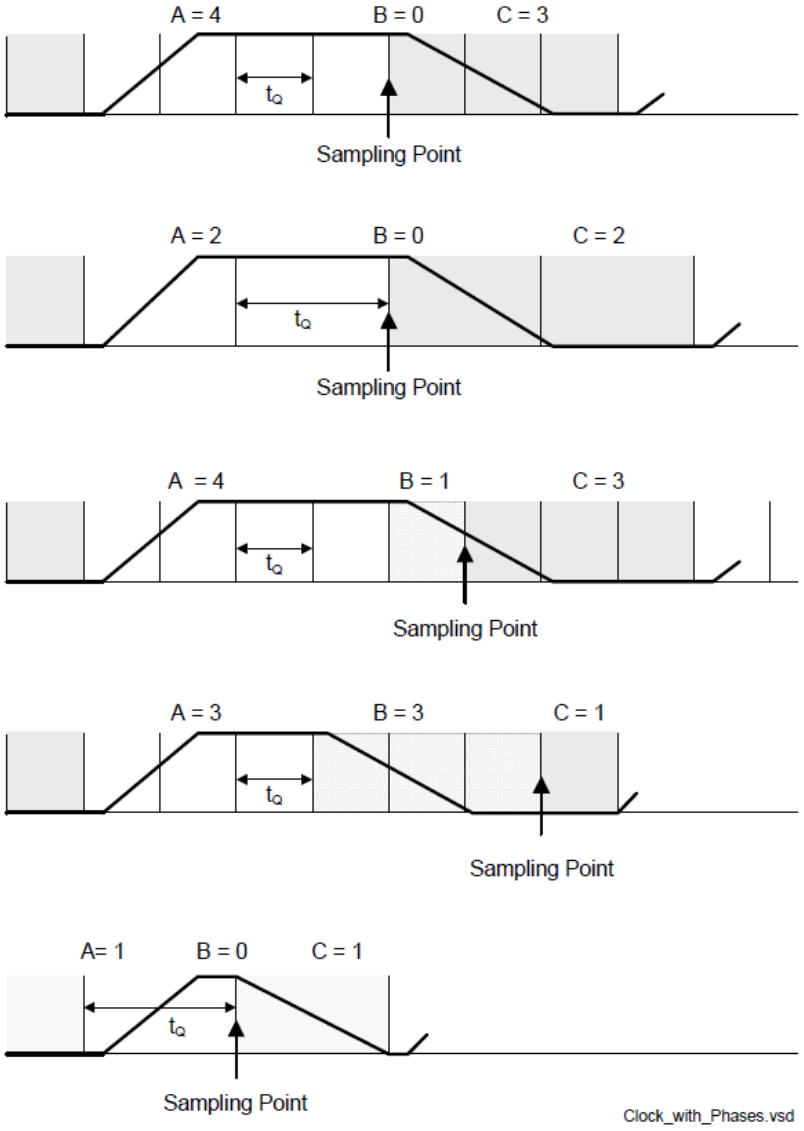
QSPI Shaping of Bit Timing

- Duty Cycle: [A, B+C]
- Sampling: B->C transition.
- ECON TQ / A / B / C impact
  - Symmetrical clock, mid point samplin

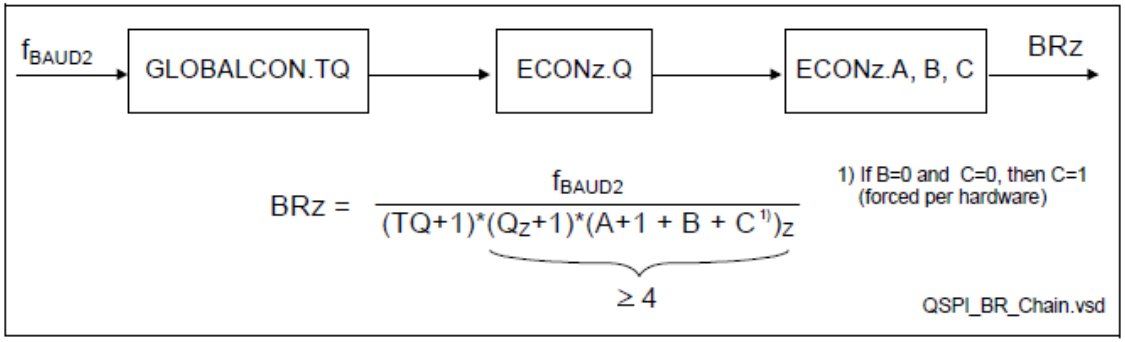


  - Asymmetrical clock, end point samplir





QSPI Baudrate (again..)



- GLOBALCON

TQ	[7:0]	rw	**Global Time Quantum Length** [RfQ00220] Common n-divider scaling the baud rates of all channels in direction of higher or lower baud rates. Must not be changed during a running transaction. 0_D division by 1 1_D division by 2 …$_D$ … 255_D division by 256

- ECONz

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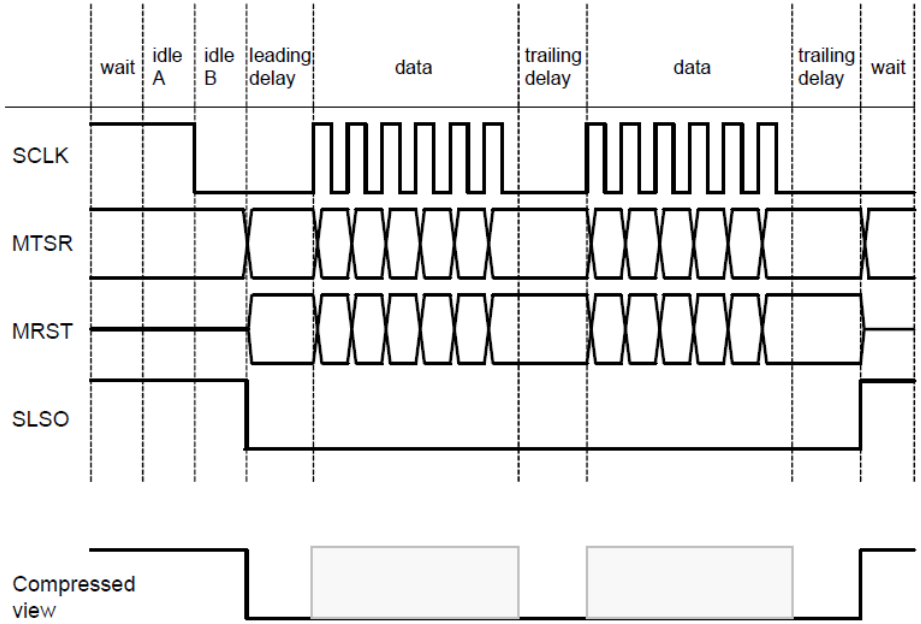
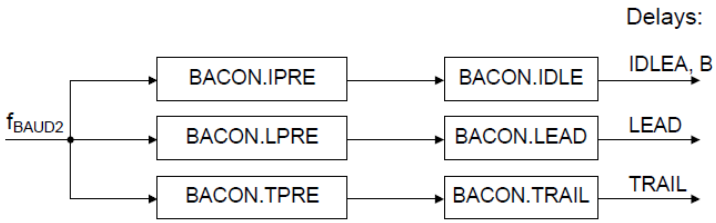
QSPI Frame Shaping

- Shaping of in-frame timing
  - Reg BACON controls the frame shape
  - Frame shaping is available on per channel base





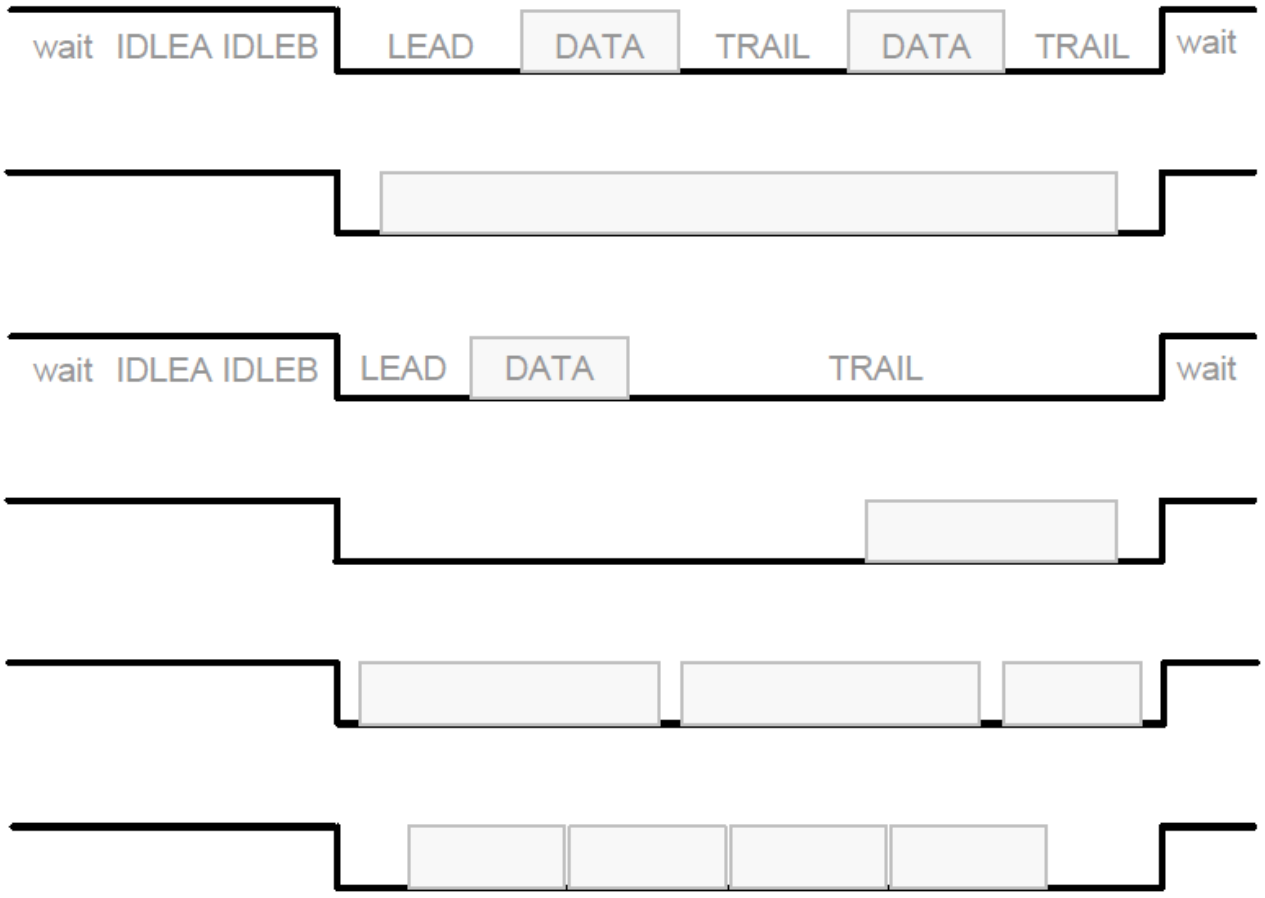
$T_{IDLEA,B} = T_{BAUD2} * 4^{IPRE} * (IDLE+1)$

$T_{LEAD} = T_{BAUD2} * 4^{LPRE} * (LEAD+1)$

$T_{TRAIL} = T_{BAUD2} * 4^{TPRE} * (TRAIL+1)$

QSPI Frame Shaping

- More frame shaping examples



QSPI Frame Shaping

- Frame shaping example 1
  - Reg BACON defines the length of each section below
  - All prescalers take fBAUD2 as input clock
  - IPRE: prescaler for IDLE DELAY, range 1 .. 16384
  - IDLE: defines length of IDLEA and IDLEB, range 1 .. 8
  - LPRE: prescaler for leading delay, range 1 .. 16384
  - LEAD: defines length of leading delay, range 1 .. 8
  - TPRE: prescaler for trailing delay, range 1 .. 16384
  - TRAIL: defines length of trailing delay, range 1 .. 8

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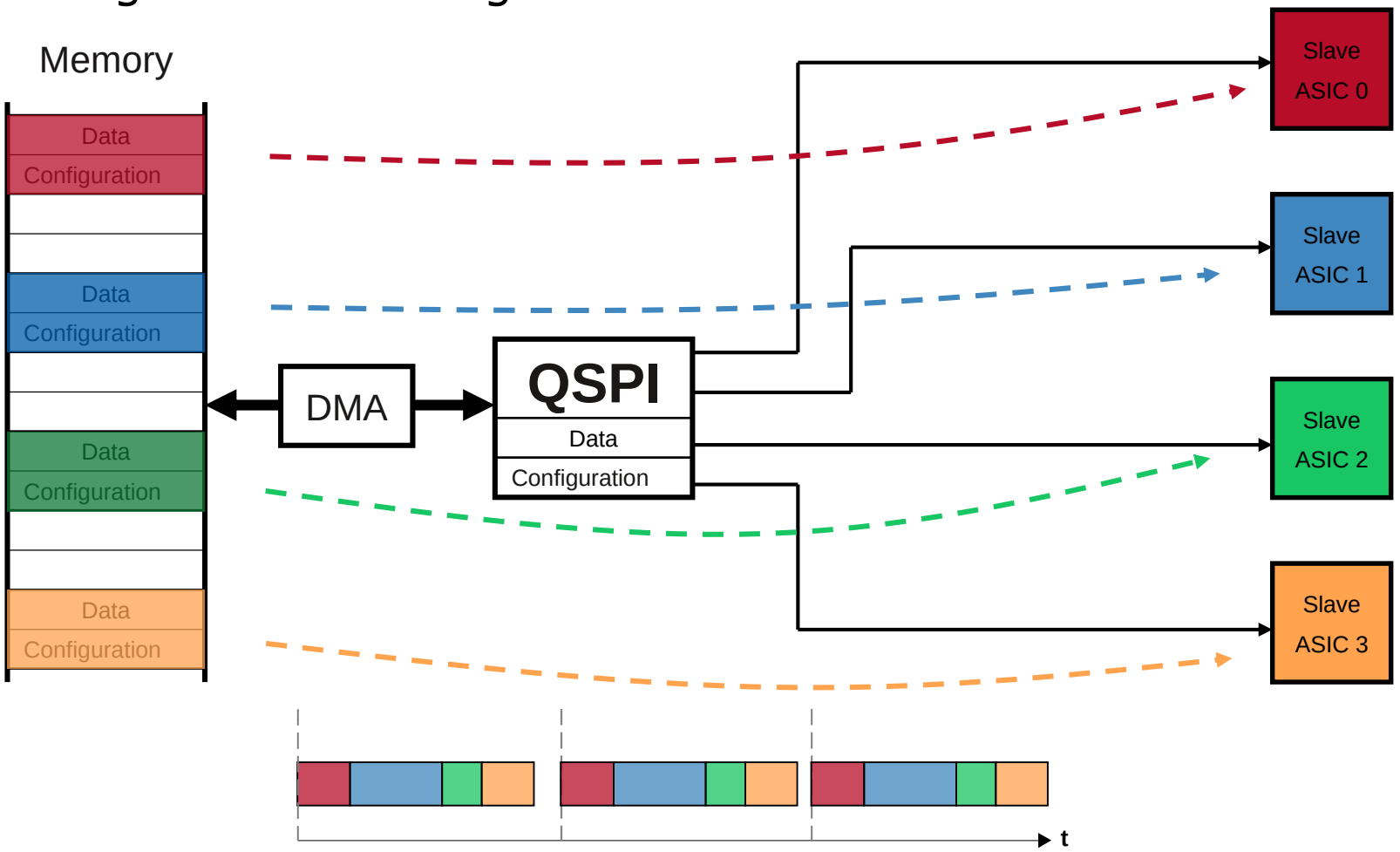
QSPI Concepts

› Configurable and Programmable “Channels”



Data Flow example

QSPI Configuration

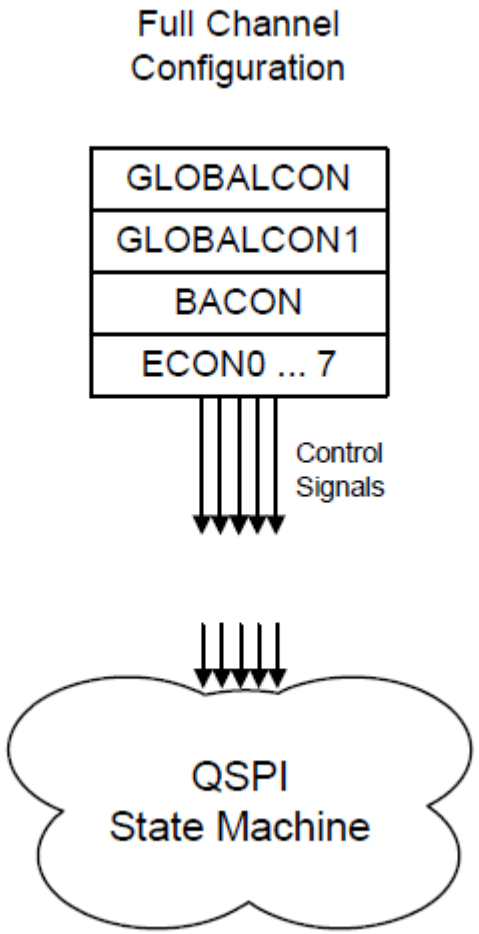
Configuration using registers:

›Fixed configurations:

- GLOBALCON (Global)
  - Master / slave
  - Enable
  - TQ etc.
  - Loop-back (LB)
- GLOBALCON1 (Global)
  - Interrupt configuration
  - FIFO thresholds
- ECON0-ECON7 (Per channel)
  - Q, A,B,C (Baud-rate, shaping)
  - Phase, Polarity, Parity

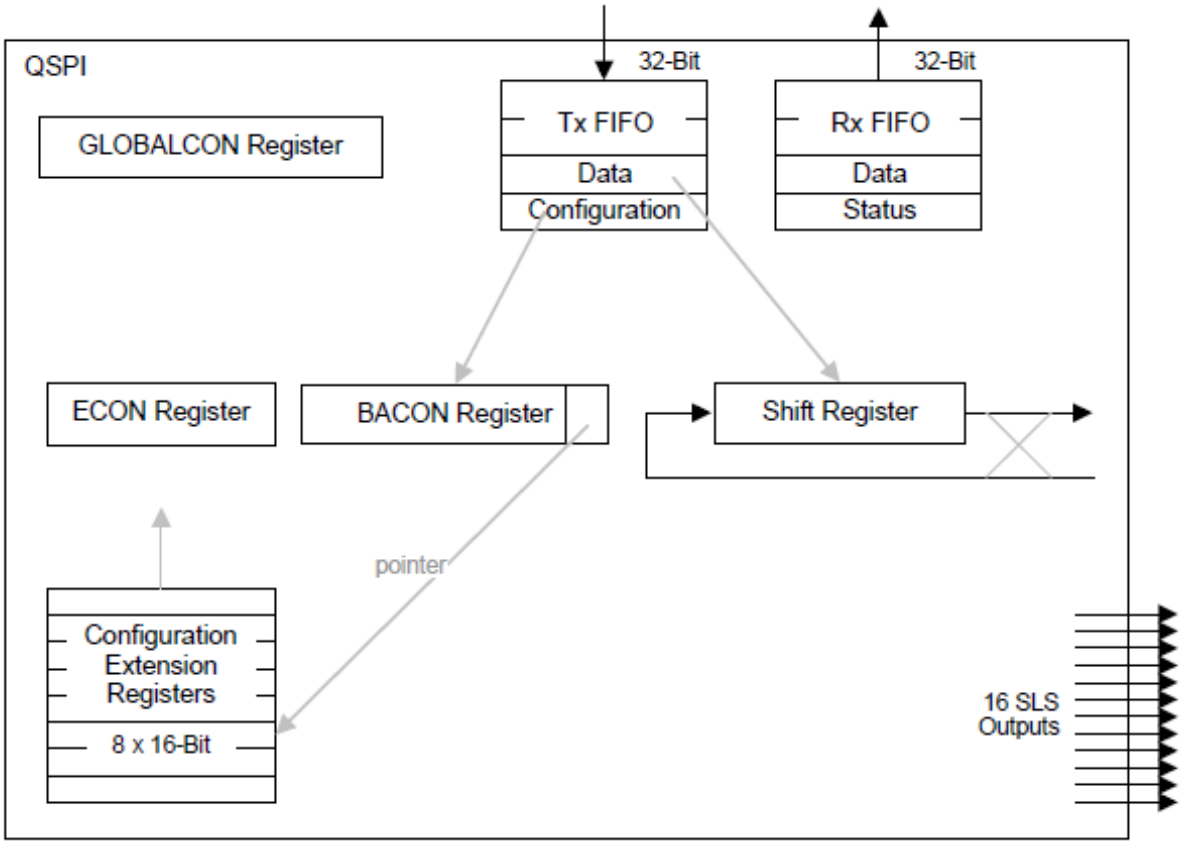
›Dynamic configurations:

- BACON (For each slave)
  - IDLE, LEAD, TRAIL etc.
  - Parity Type
  - Data length
  - Channel select



Queue Support

- Configuration and Data to FIFO
- Dynamic configurations:
  - BACON (For each slave)
    - IDLE, LEAD, TRAIL etc.
    - Parity Type
    - Data length
    - Channel select



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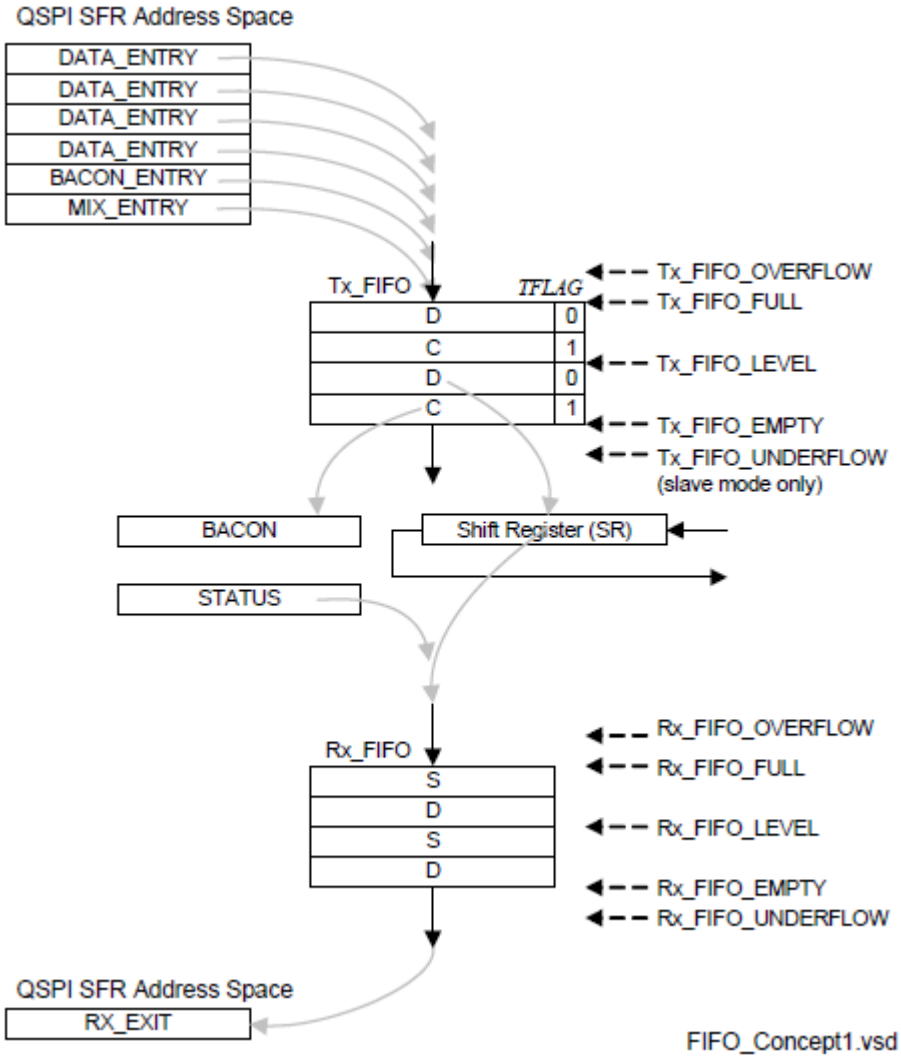
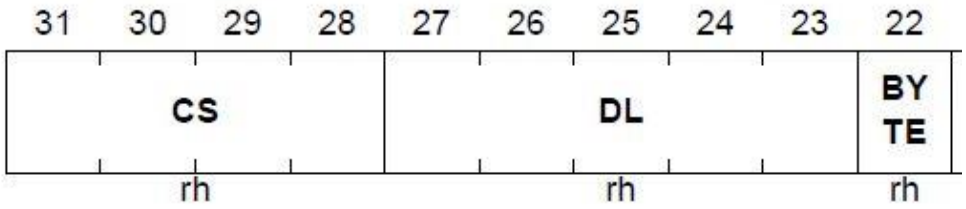
QSPI User Interface

- To transfer data to/from Tx & Rx FIFO.
- Tx FIFO Registers:
  - DATA_ENTRY (8 registers): Interpreted
  - BACON_ENTRY: Interpreted as configur
  - MIX_ENTRY: Configuration or Data
- Rx FIFO Registers:
  - RX_EXIT: Data
    - Or status, if status injection is enabled



QSPI Frame Length

- Frame length programming
  - Frame length can be set dynamically
  - -> individually for each channel
  - -> individually for each frame to be sent
  - BACON.CS defines the channel where the frame will be sent
  - BACON.DL and BACON.BYTE together define the frame length
  - BACON.DL: defines the length of the frame, range 2 .. 32
  - BACON.BYTE: defines whether the value in BACON.DL
    - Defines the length in bytes (long data mode)
    - Or defines the length in bits (short data mode)
  - XXL mode: BACON.DL = 0; BACON.BYTE = 1



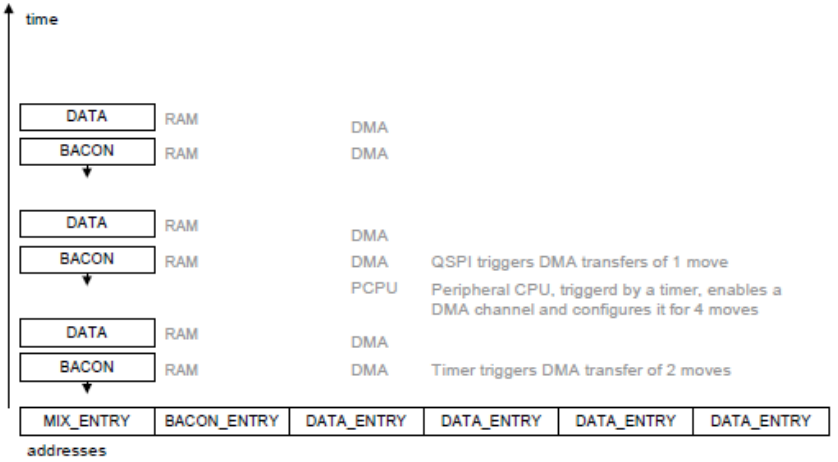
QSPI Short Data Mode

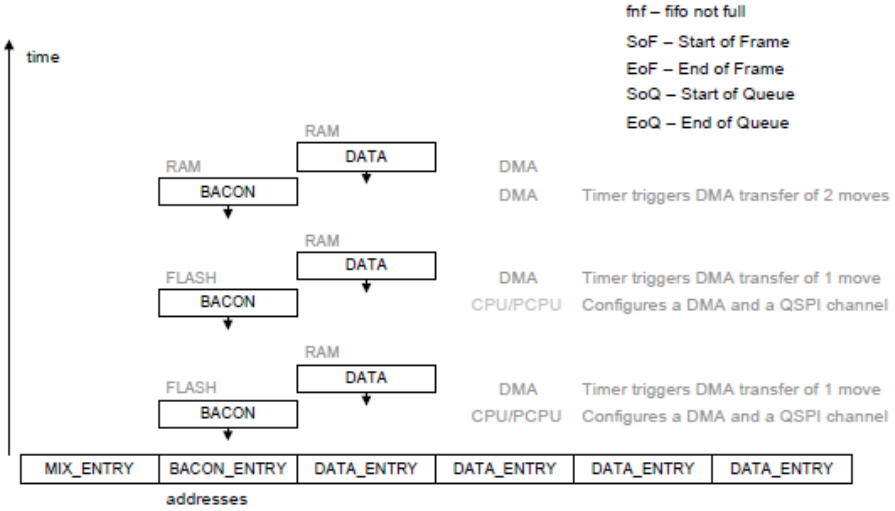
- Single Data
  - 2-32 bits
  - BACON.LAST = 1
  - BACON.BYTE = 0
  - BACON.DL = 2-32 (bits)

- MIX_ENTRY

  OR

- BACON_ENTRY & DATA_ENTRY





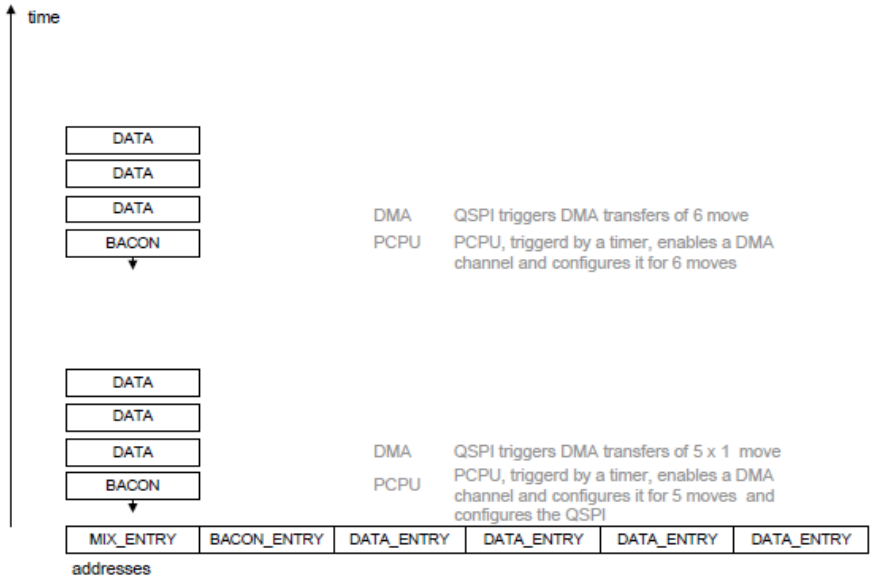
QSPI Long Data Mode

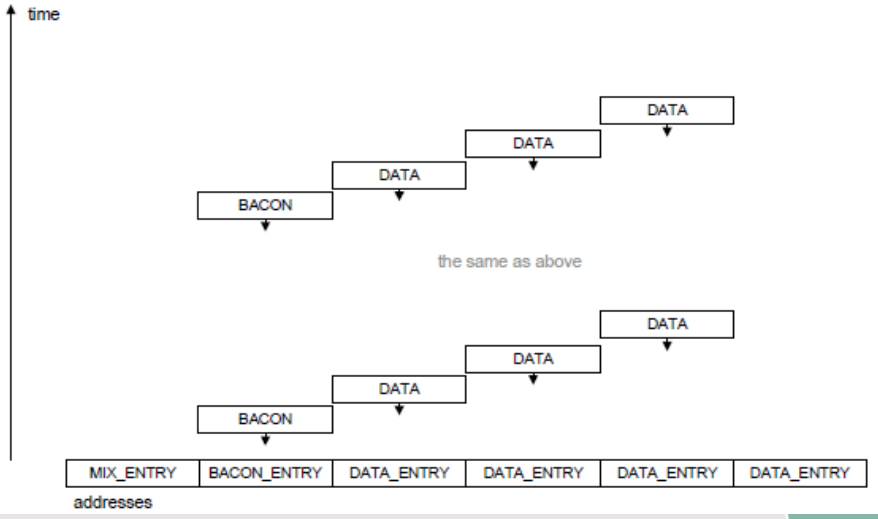
- Up-to 32 bytes in one frame
  - BACON.LAST = 1
  - BACON.BYTE = 1
  - BACON.DL = 2-32 (bytes)

- MIX_ENTRY

  OR

- BACON_ENTRY & DATA_ENTRY





QSPI Continuous Mode

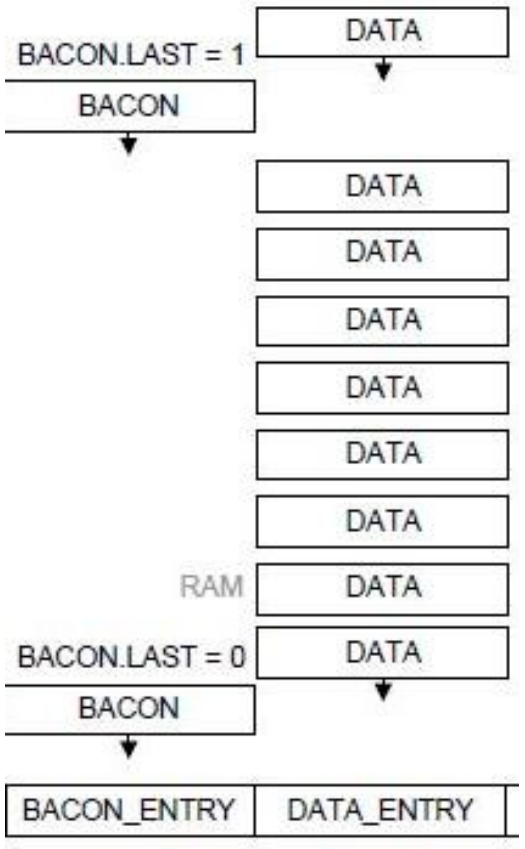
- Transfer of several frames (long or short data)
  - The first frame needs a BACON with BACON.LAST = 0x0
  - The next frames can re-use this BACON
  - The last frame needs a BACON with BACON.LAST = 0x1

  - Short or Long data

LAST	0	rh	**Last Word in a Frame** Defines if the following data word is last in the current frame or not 0_B Not Last 1_B Last

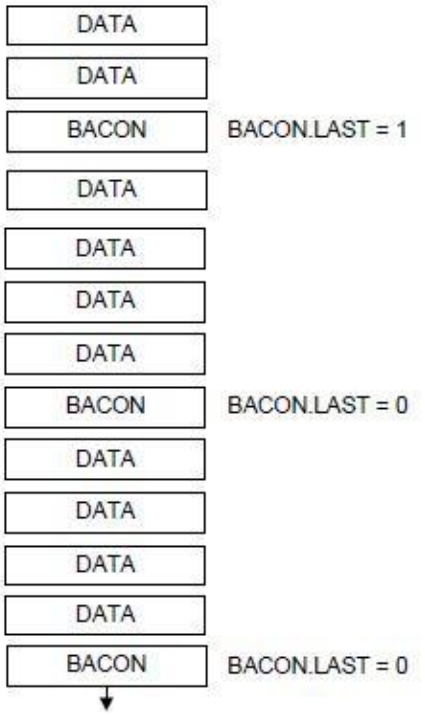
QSPI Continuous Mode (Short data)

- Continuous transfer in Short Data Mode
  - Data fields sized 2 .. 32 bits are written in an “endless” stream
  - The fields are separated by the trailing delay
  - The last field needs the following BACON:
    - BACON.LAST = 0x1
  - If no new BACON is written the former one stays valid



QSPI Continuous Mode (Long data)

- Continuous transfer in Long Data Mode
  - Data fields sized by BACON.DL are written in an "endless" stream
    (up to 32 x 1 byte = 256 bits)
  - The fields are separated by the trailing delay
  - After the complete field a new BACON must be written
  - The last byte block needs the following BACON:
    - BACON.LAST = 0x1



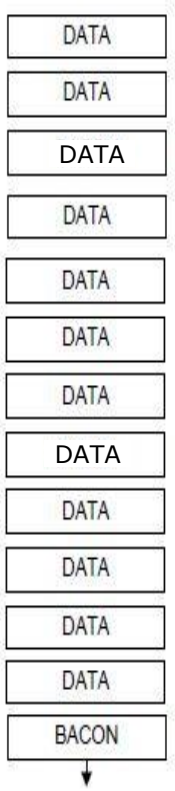
QSPI XXL Frame Modes

- Extension of Long Data Mode
  - Data size 2 upto 65536 Bytes.
  - Data fields sized by BACON.DL are written in an “endless” stream
  - No need for further BACON entries (unlike continuous mode)
- Configuration:
  - BACON.DL = 0; BACON.BYTE = 1.
  - New XXLCON register (Don‘t care unless BACON.DL = 0 & BYTE = 1):
    - XXLCON.XDL defines data length
      - (2-65536 Bytes)
    - XXLCON.BYTECOUNT: Shows remaining bytes to be sent.

XXLCON
Extra Large Data Configuration Register(58_H) **Reset Value: $0000\ 0000_H$**

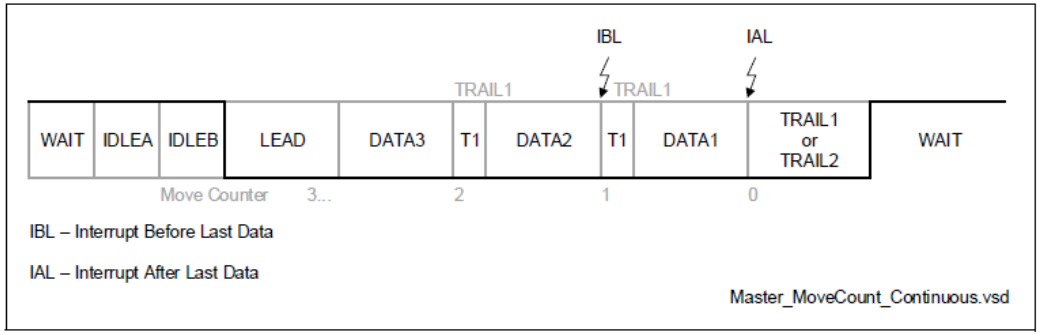
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BYTECOUNT															
r															

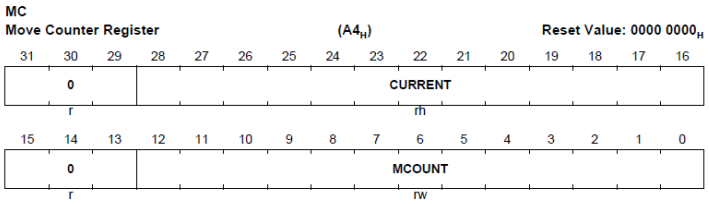
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XDL															
rw															

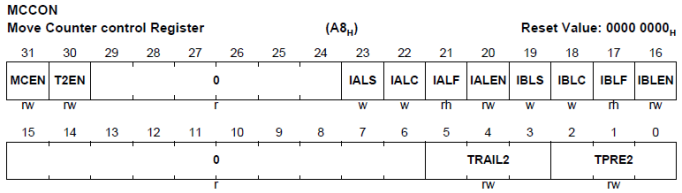


QSPI Move Counter Mode

- Send upto 8192 “short data“ moves in one QSPI frame.
- Enabled by setting MCCON.MCEN = 1.
- Set BACON.BYTE = 0 & BACON.LAST = 0.
- Two interrupts can be triggered:
  - After the move before last has been shifted out (IBL).
  - After the last move has been shifted out (IAL).

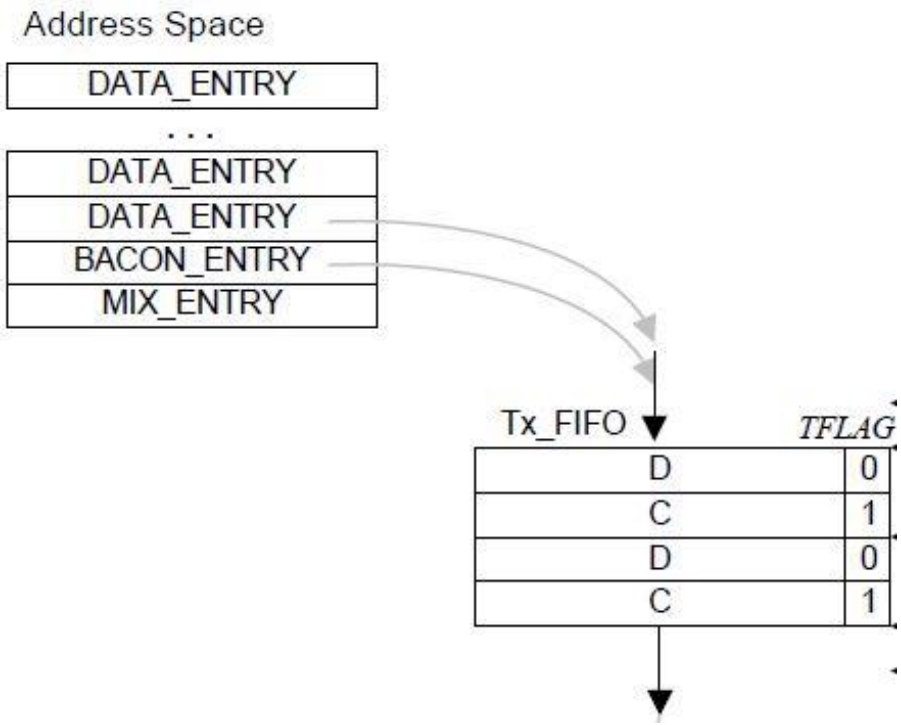






QSPI FIFO Fill Operation

- The QSPI TxFIFO usage
  - The TxFIFO takes data and configuration (BACON)
  - Both have to be written in a defined order
- The written BACON value defines the processing of the following data value
  - Address / offset space:
    - DATA_ENTRY: 0x80
    - …….
    - DATA_ENTRY: 0x64
    - BACON_ENTRY: 0x60
    - MIX_ENTRY: 0x5C
  - The order of the written values is not changed



QSPI FIFO Command Summary

- Each operation consists of the pair BACON / Data
- BACON / Data pairs are written to the TxFIFO
- BACON defines how the following data value will be processed
- BACON defines (for some settings together with reg ECON)
  - Channel number (Slave Select line)
  - Baudrate
  - Frame shape (complete frame and frame fields)
  - Clock duty cycle
  - Data latching
  - Interrupt generation

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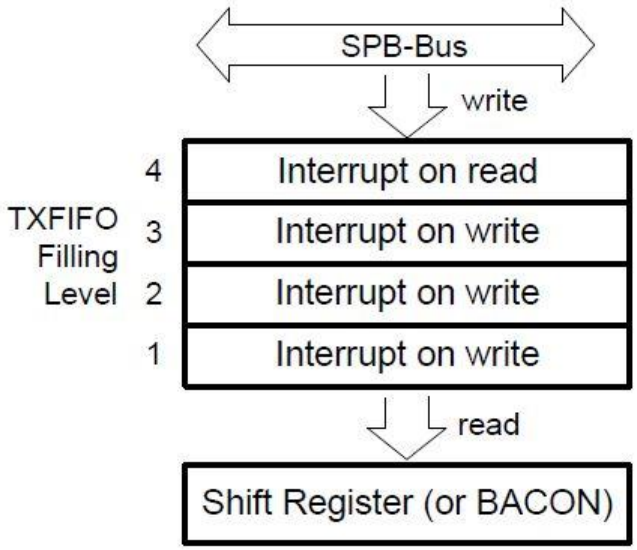
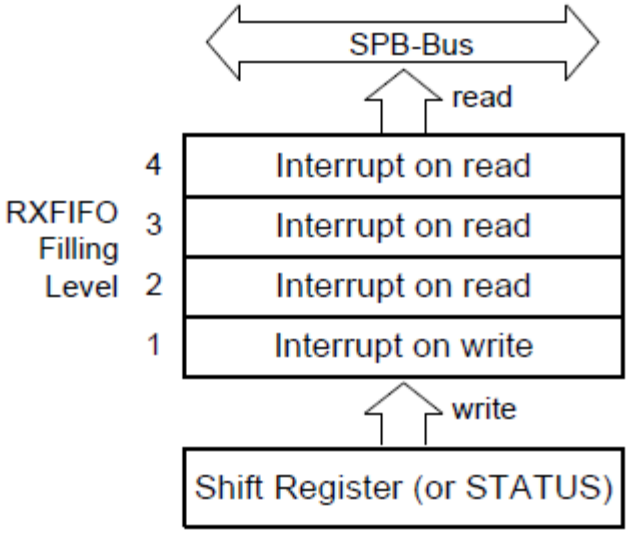
QSPI FIFO Single Move

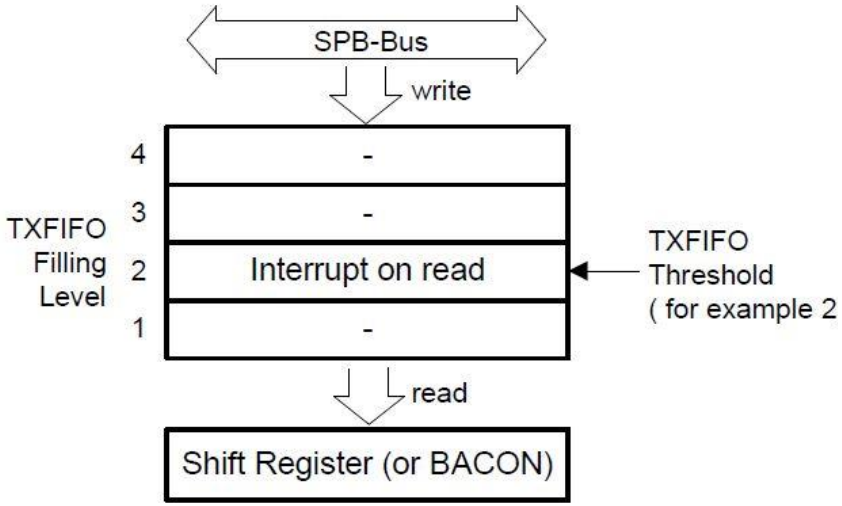
- Keep Tx FIFO full (or Rx FIFO empty)
  - An event happens if the FIFO is not full (or empty for Rx)
  - Eg. Self-Sustaining DMA.
  - GLOBALCON1.TXFM (RXFM) = 0x1.

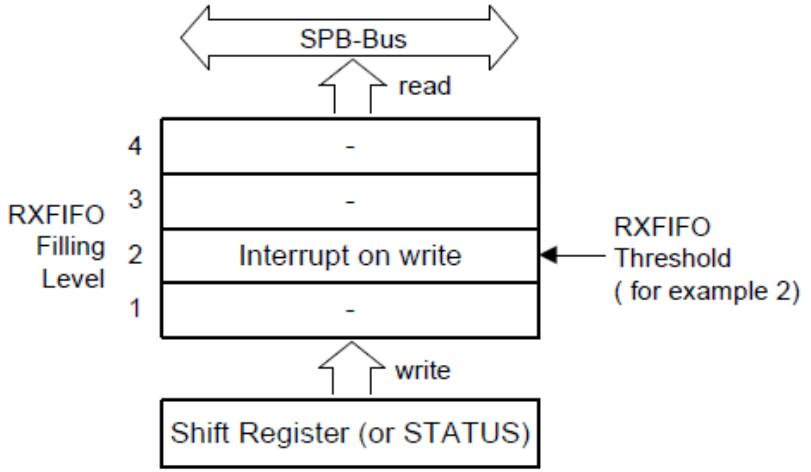




QSPI FIFO Batch Move

- Reduce the no:of Interrupts
  - The FIFO has a configurable watermark (“Threshold”)
  - An event happens if the Tx FIFO fill level falls below watermark
    - (Or above watermark for Rx)
  - GLOBALCON1.TXFM (or RXFM) = 0x2.
  - GLOBALCON1.TXFIFOINT (& RXFIFOINT) => Threshold
  - Eg. Fill using CPU.





QSPI FIFO Combined Move

- Combination of Single and Batch move.
  - The FIFO runs a configurable watermark (“Threshold”)
  - An event happens if the Tx FIFO fill level falls below watermark
    - (Or above watermark for Rx)
  - GLOBALCON1.TXFM (or RXFM) = 0x0.
  - GLOBALCON1.TXFIFOINT (& RXFIFOINT) => Threshold

  - Tx FIFO
    - Fill level is equal or less than GLOBALCON1.TXFIFOINT => Generate Interrupt.
  - Rx FIFO
    - Fill level is equal or greater than GLOBALCON1.RXFIFOINT => Generate Interrupt.

Agenda

1. QSPI Overview
2. QSPI Features
3. QSPI Clocking & Baud rate generation
4. QSPI Frames
5. Concepts of QSPI
6. QSPI User Interface
7. QSPI FIFO Interrupts (and move modes)
8. Conclusion

Conclusion (& Refresh)

- QSPI Clocking
  - f_{SPI} & f_{SPB}
  - Baud rate: GLOBALCON.TQ, ECON.Q, ECON.A, B,C.
  - Duty cycle & sampling point: [A, B+C], B->C.

- Frame timing:
  - BACON.IDLE, LEAD, TRAIL etc.

- Queue concept:
  - Configuration: GLOBALCON, GLOBALCON1, ECON(0-7), BACON
  - BACON_ENTRY, DATA_ENTRY (& MIX_ENTRY)

Conclusion (contd..)

- User Interface (& data length): BACON.BYTE, DL, LAST
  - Short (2-32 bits)
  - Long (2-32 bytes)
  - Continuous
  - XXL mode (up-to 65536 Bytes)

- FIFO Moves
  - Single move (eg. Continuous DMA)
    - Keep Tx FIFO full (or Rx Empty)
  - Batch (eg. CPU)
    - Reduce no: of interrupts.
  - Combined move

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