AURIX 2G Overview

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IFCN ATV SMD GC SAE MC
2018/5/2

Agenda

1. Infineon Microcontroller
2. AURIX TC3xx Overview
3. AURIX TC3xx Features Details
4. AURIX TC3xx Performance
5. AURIX TC3xx Safety Supply
6. AURIX TC3xx SW & Tools
7. AURIX TC3xx Schedule

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Infineon Microcontroller focus areas

Leading in key automotive innovation areas

CHASSIS, SAFETY, ADAS

- Power Steering
- Vehicle Stability Control, Braking
- Chassis/Safety Domain Control
- Airbag
- Suspension
- Sensor Fusion Box
- RADAR, LIDAR
- Vision (2D/3D (TOF)
- Advanced Lighting

ADVANCED CONNECTIVITY

- Connected Gateway
- Full Feature BCM
- V2V / V2X
- eCall
- Online Connectivity Module
- Telematics

POWERTRAIN

- Engine Management (GDI/DDI/MPI)
- Transmission (DCT/ECAT/AMT)
- Hybrid & Electric Vehicle Inverter
- DC/DC Converter
- Battery Management
- Starter-Generator
- 48V

SAFETY: Complete Solution for Safety up to ASIL-D

SECURITY: Integrated hardware security module

Performance

AURIX™ scalable family concept

Automotive Application Roadmap supporting latest trends

Main Market Drivers:

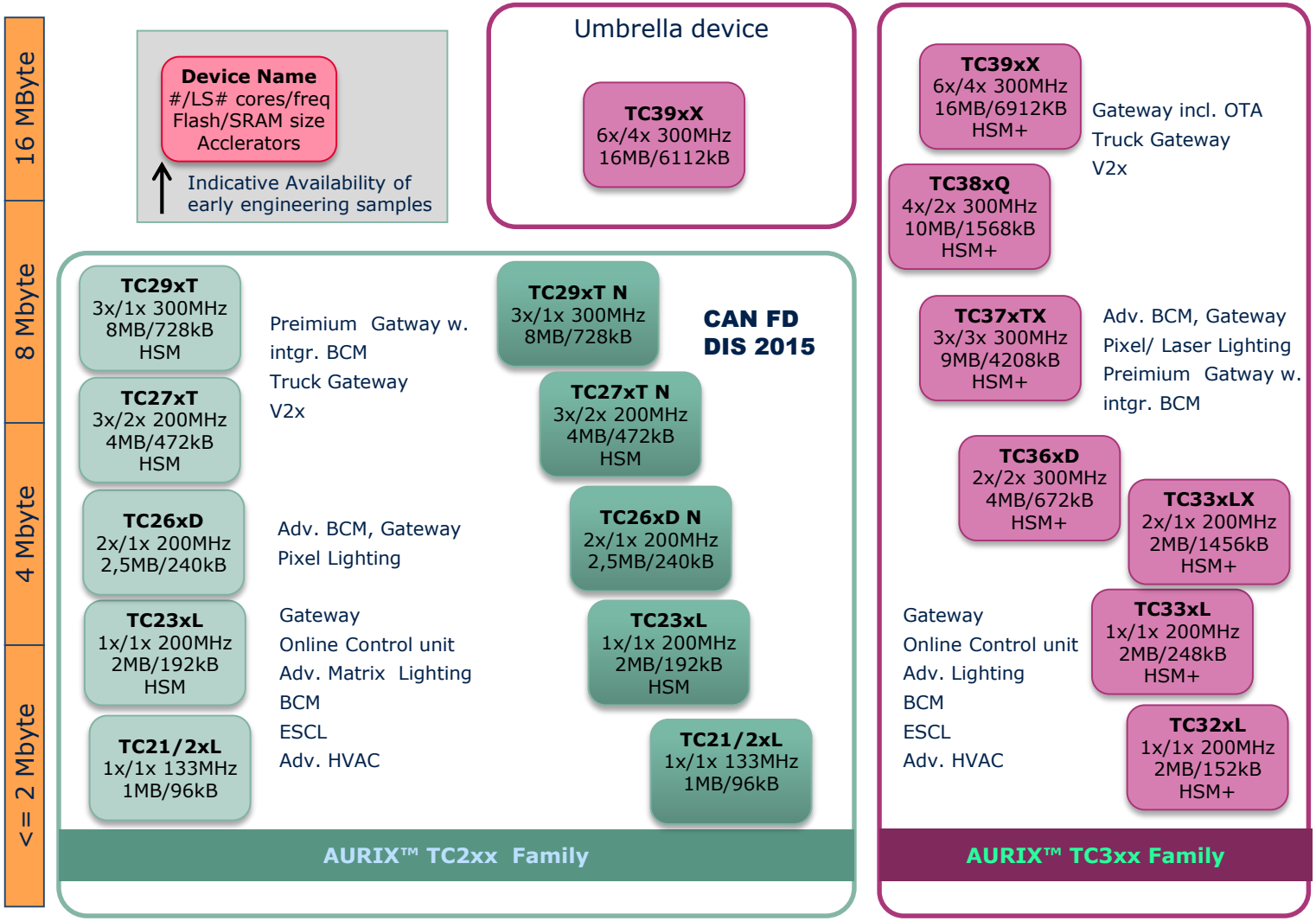
- Fuel Efficiency
- Autonomous Vehicles
- Connected Car

Production	SoP 2015 – 2020+	SoP 2019 – 2024+	SoP 2022 – 2026+
■ 1.5-4MByte ■ Single core	■ 0.5-8MByte ■ 3x Multi-core	■ 1-16MByte ■ 6x Multi-core	■ 2-32MByte ■ Multicore & GHz processing
			Vision 2D/3D
	Gateway/Telematics	Gateway/Telematics	Gateway/Telematics
	Data fusion	Data fusion	Data Fusion
	Radar	Radar	Radar
Domain Control	Steering	Steering	Steering
Hybrid	Braking	Braking	Braking
Transmission	Airbag	Airbag	Airbag
Engine Management	Domain Control	Domain Control	Domain Control
	Hybrid	Hybrid	Hybrid
	Transmission	Transmission	Transmission
	Engine Management	Engine Management	Engine Management

AUDOMAX → AURIX™ TC2xx → AURIX™ TC3xx → AURIX ™ TC4xx

IFX Microcontroller Connectivity Roadmap

future proof roadmap guarantees joint success story



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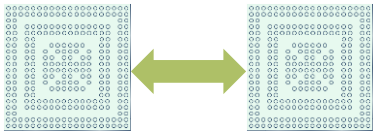
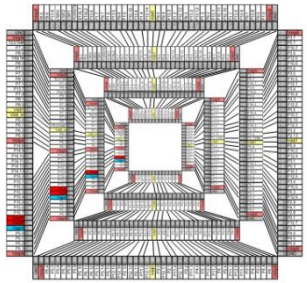
AURIX™ TC2xx to AURIX™ TC3xxx

Easy migration - Scalability & Compatibility

- **Fast conversion** of existing AURIX™ TC2xx designs
  - High AURIX TC3xx compatibility to pinout of existing QFP100/144/176 and BGA packages



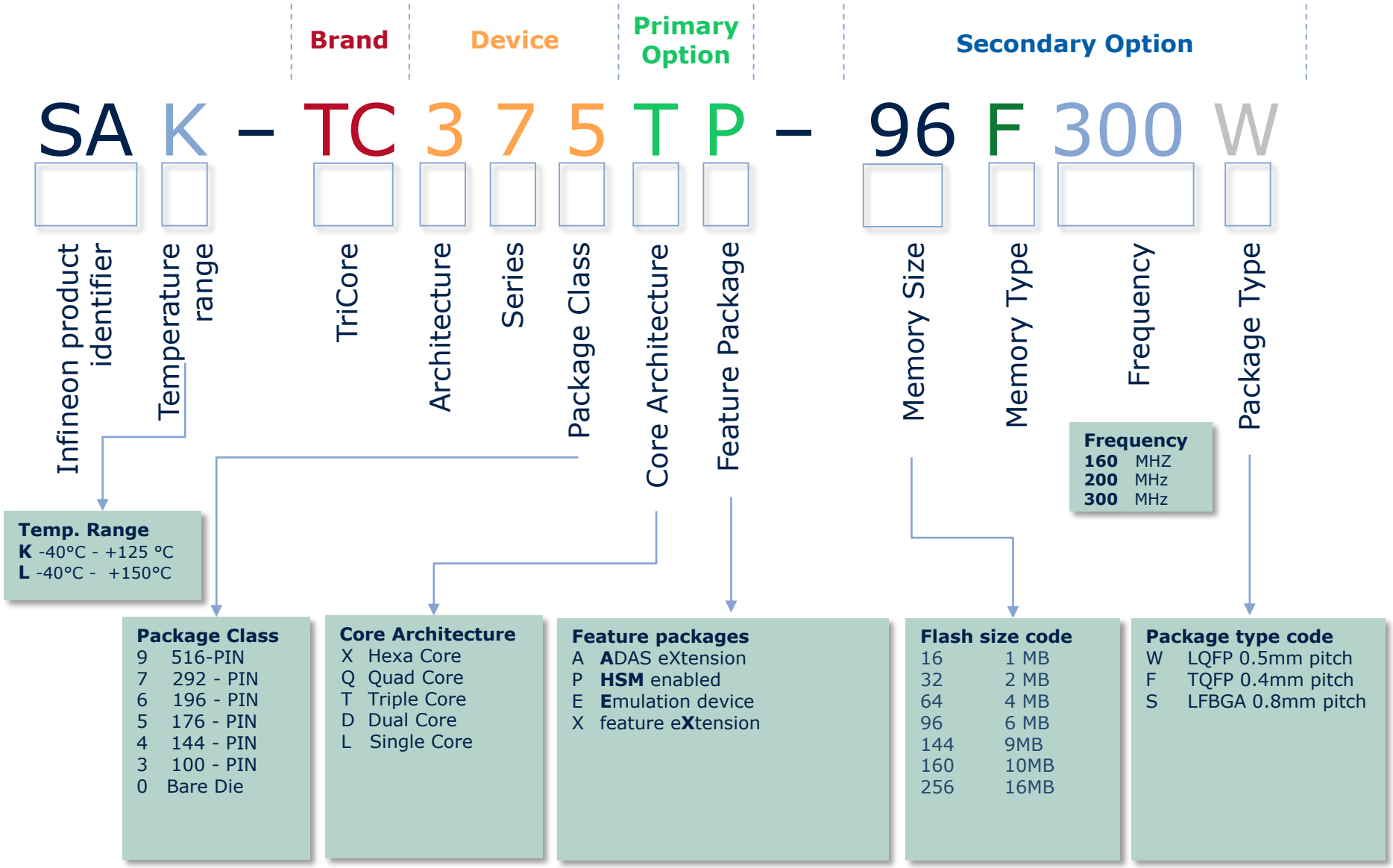
- **Flexibility** - Scalability within the AURIX™ TC3xx family
  - Up-/Downgrade paths for devices in identical packages
  - Compatible pin-out of QFP/BGA package options enabling combi designs



- **Reuse** – Software compatibility across the AURIX™ TC3xx family
  - Binary compatible TC1.6.2 P cores
  - Single set of peripherals across the AURIX™ TC3xx family

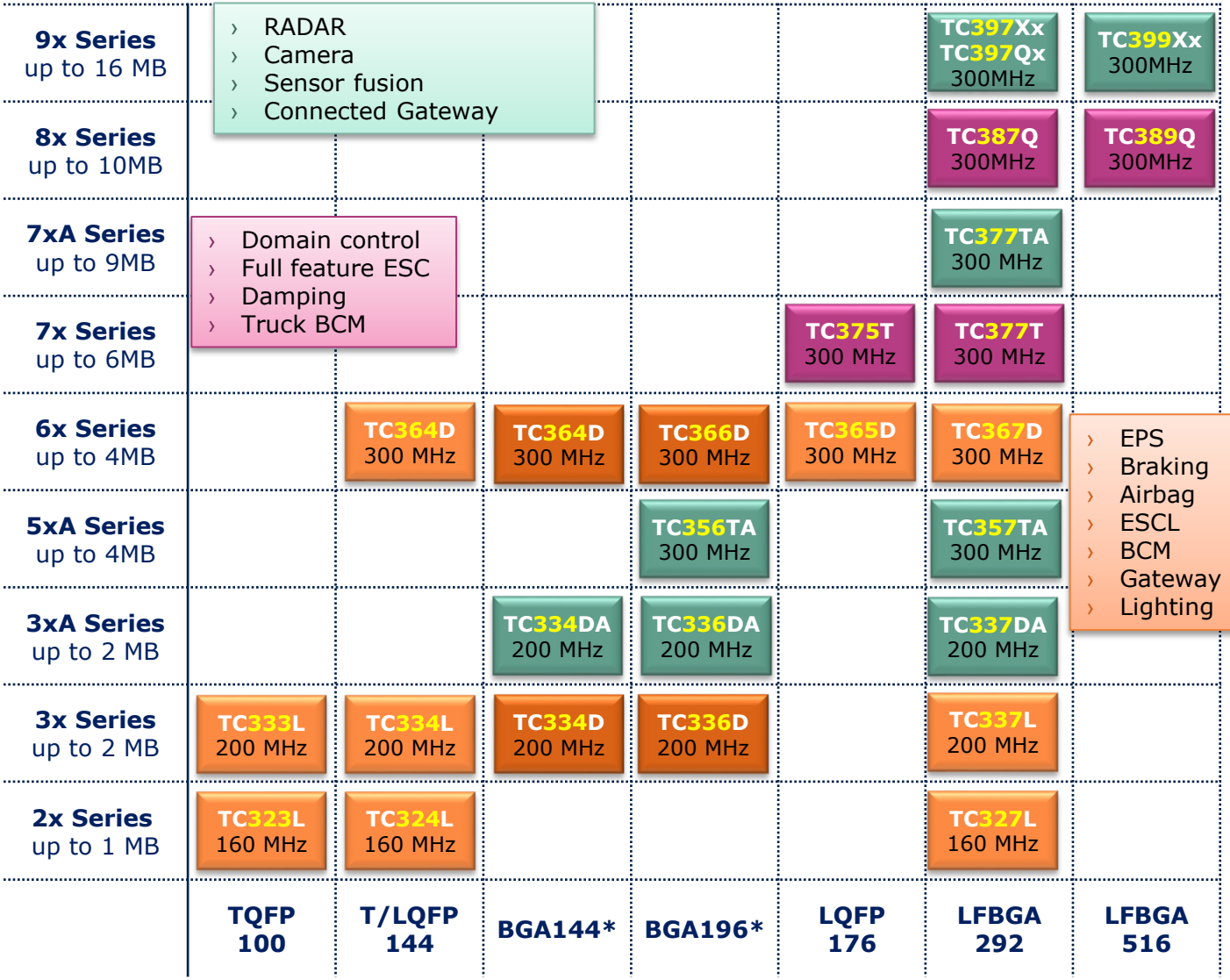
- **Common safety concept** across the family
  - Reuse of safety features from AURIX™ TC2xx
  - Holistic safety concept across the AURIX™ TC3xx family

AURIX 2G Product Naming



AURIX™ TC3xx

From low cost to high performance applications



***in discussion**

MCU Scalability

- Performance & Flash
- Software compatibility
- Pin-compatibility
- Binary compatible cores

Power Consumption

- On-chip SC DC/DC high-efficiency power supply
- Stand-by control unit for lowest quiescent current

Safety/Security Concept

- ISO26262 compliance
- Hardware security support

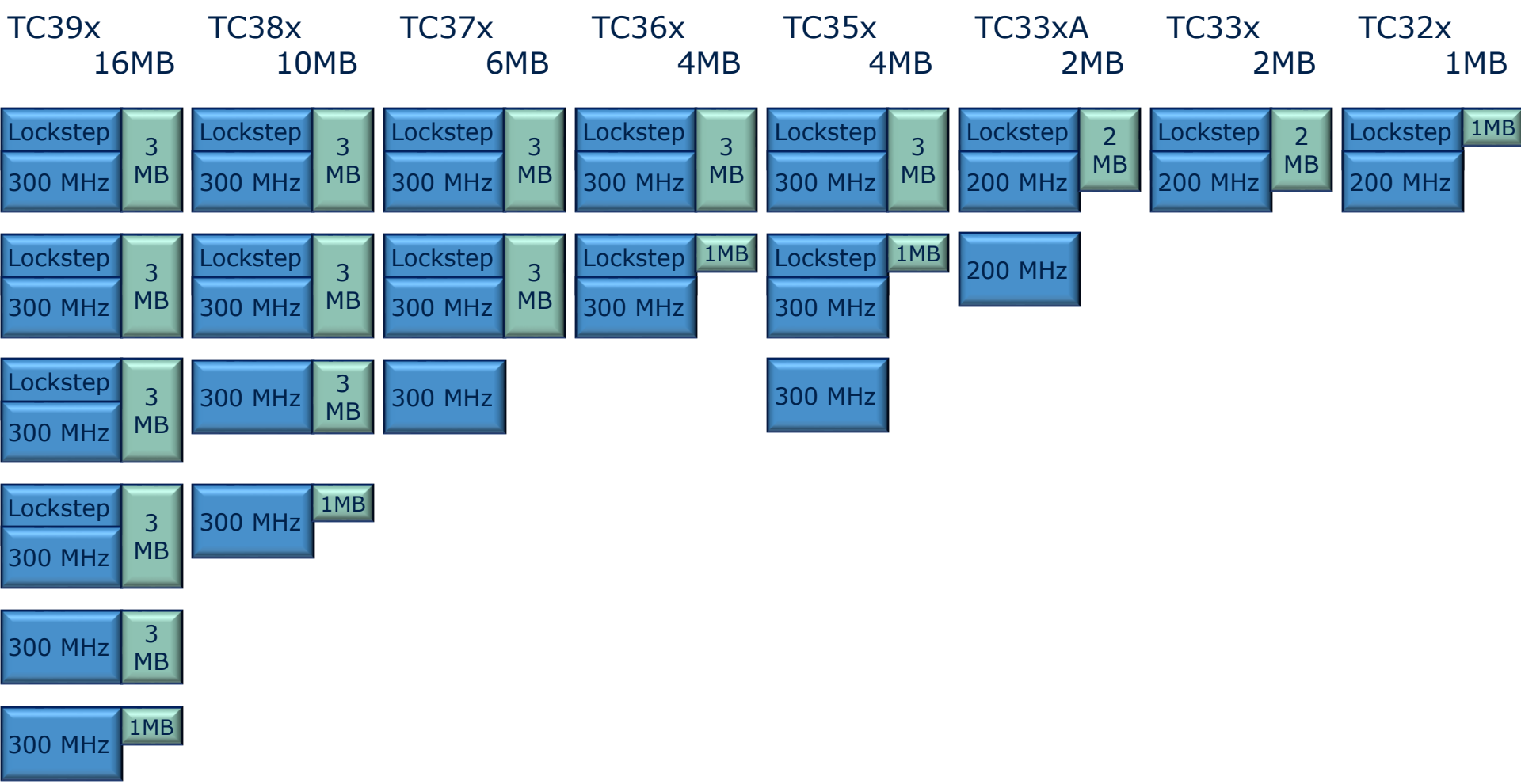
Connectivity

- Ethernet: up to 1GB
- CAN FD: up to 12 channels
- LIN: up to 24 channels
- eMMC IF

L - Single Lockstep Core
D - Dual Core
T - Triple Core
Q - Quadruple Core
X - Sextuple Core

AURIX™ - TC3xx Lockstep Architecture

Scalable CPU And Flash Configuration



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AURIX™ TC3xx Architecture Evolution
(enhancements to AURIX TC2xx)

INNOVATION

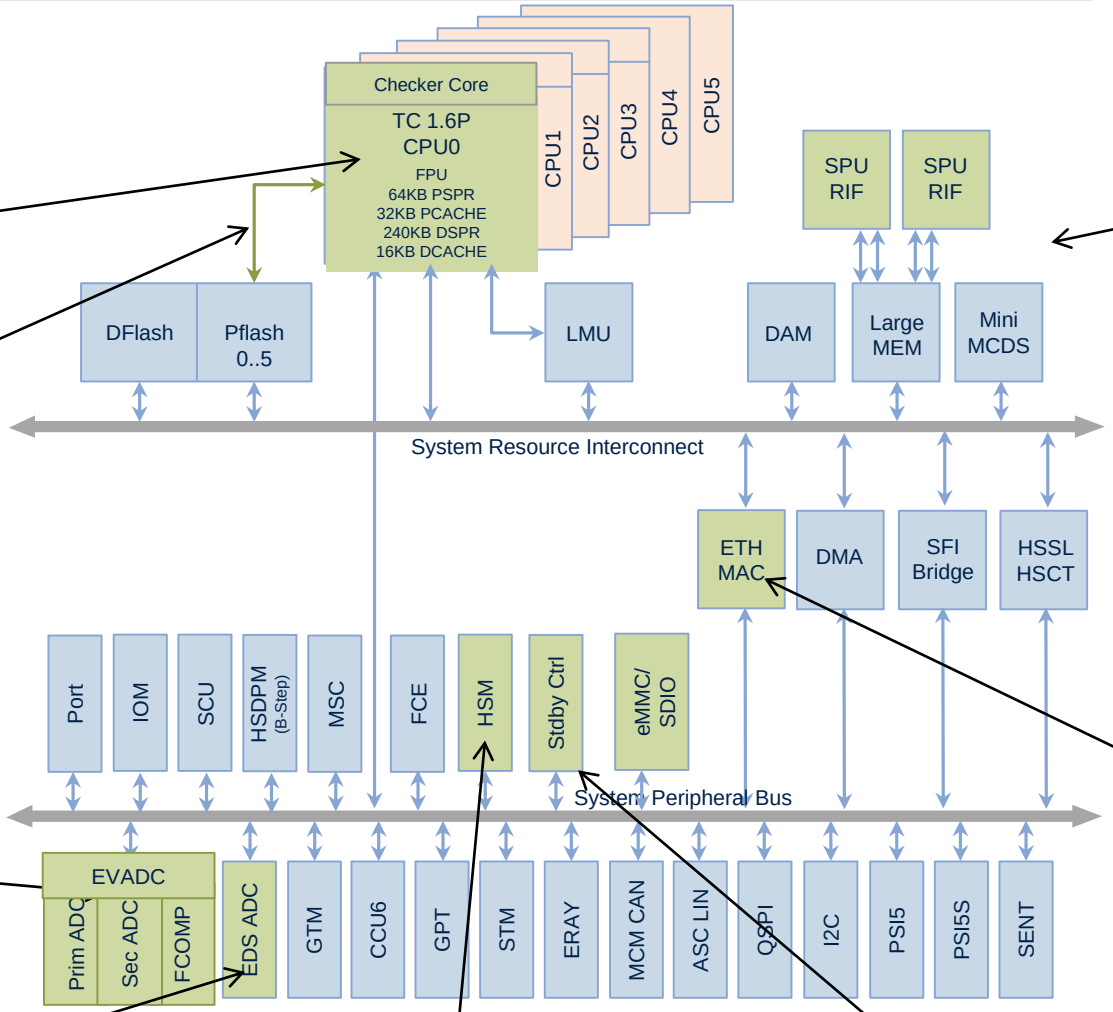
Performance
Multi-core with up to 6 CPUs @300MHz

Direct read path between FLASH and CPU

Memories
more SRAM
linear address space for LMU-SRAMs
enhanced MPU

ADC
proven SAR:
less C-load

Delta-Sigma:
enhanced concept



ADAS
New SPU concept

Safety
Improved Ease of Use

Ethernet
GigE with advanced QoS

IO Pads
all 5V/3.3V

HSM: Full Evita compliance
ECC256 / SHA256

On All Devices

AURIX TC3xx Feature Table

Feature Set		9x Series eXtension (16MB)	8x Series (10MB)	7x Series eXtended (9MB)	7x Series (6MB)	6x Series (4MB)	5x Series (4MB)	3x Series +eXtension (2MB)	3x Series (2MB)	2x Series (1MB)
TriCore 1.6	# Cores / Checker	6/4	4/2	3/3	3/2	2/2	3/2	2/1	1/1	1/1
	Frequency	300MHz	300MHz	300MHz	300MHz	300MHz	300MHz	200MHz	200MHz	160MHZ
Accelerator	Signal processing Unit (SPU)	2xSPU					2xSPU	1xSPU		
Flash	Program Flash	16MB	10MB	9MB	6MB	4MB	4MB	2MB	2MB	1MB
	Data Flash (physical/logical)	1024kB	512kB	256kB	256kB	128kB	128kB	128kB	128kB	96kB
SRAM	Total (DMI , PMI, LMU, AMU)	6912KB	1568kB	4208kB	1136kB	672kB	2837kB	1456kB	248kB	152kB
DMA	Channels	128	128	128	128	64	64	16	16	16
ADC	Modules Primary / Sec / FC / DS	8/4/8/14	8/4/4/10	4/4/2/6	4/4/2/6	4/2/2/4	2/0/0/0	4/2/0/0	2/2/0/0	2/2/0/0
	Channels Primary / Sec / FC /DS	64/64/8/14	64/64/4/10	32/64/2/6	32/64/2/6	32/32/2/4	16/0/0/0	>16/32/0/0	16/32/0/0	16/32/0/0
Timer	GTM TIM / (A)TOM / MCS	94 / 192 / 10	56 / 152 / 7	40 / 88 / 5	40 / 88 / 5	24 / 64 / 3	-	16 / 32 / 0	16 / 32 / 0	16 / 32 / 0
	CCU / GPT modules / bit streaming	2/1/1	2/1/0	2/1/0	2/1/-	2/1/0	2/1/1	2/1/1	2/1/0	2/1/0
Interfaces	FlexRay (#/ch.)	2 /4	2/4	1/2	1/2	1/2	1/2	1/2	1/2	0/0
	CAN-FD / TT	12/1	12/1	8/1	8/1	8/1	6/0	8/0	8/0	6/0
	QSPI / ASCLIN / I2C	6 /12/2	5 /24/2	5/12/1	5/12/1	4/12/1	4/4/0	4/12/0	4/12/0	4/6/0
	SENT / PSI5 / PSI5S	25/4/1	25/4/1	15/2/1	15/2/1	10/2/1	0/0/0	6/0/0	6/0/0	6/0/0
	HSSL / MSC / EBU	1/4/1	1/3/0	1/2/0	1/2/0	1/1/0	0/0/0	0/0/0	0/0/0	0/0/0
	Ethernet 100Mbps/1Gbps	1/1	1/1	1/1	1/1	1/1	1/1	1/1	-/-	-/-
	eMMC/SDIO	1/1		1/1				1/1		
	Radar /ext. ADC IF (RIF)	12x400Mbps LVDS	-	-	-	-	12x400Mbps LVDS	6x100Mbps LVDS	-	-
	Camera IF (CIF)	-	-	1	-	-	-	-	-	-
Security	HSM	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256
Safety	SIL Level	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D
Power	EVR	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)
	Standby Control Unit	yes	yes	yes	yes	yes	yes	yes	yes	yes

AURIX TC3xx to AURIX TC2xx

SRAM Overview

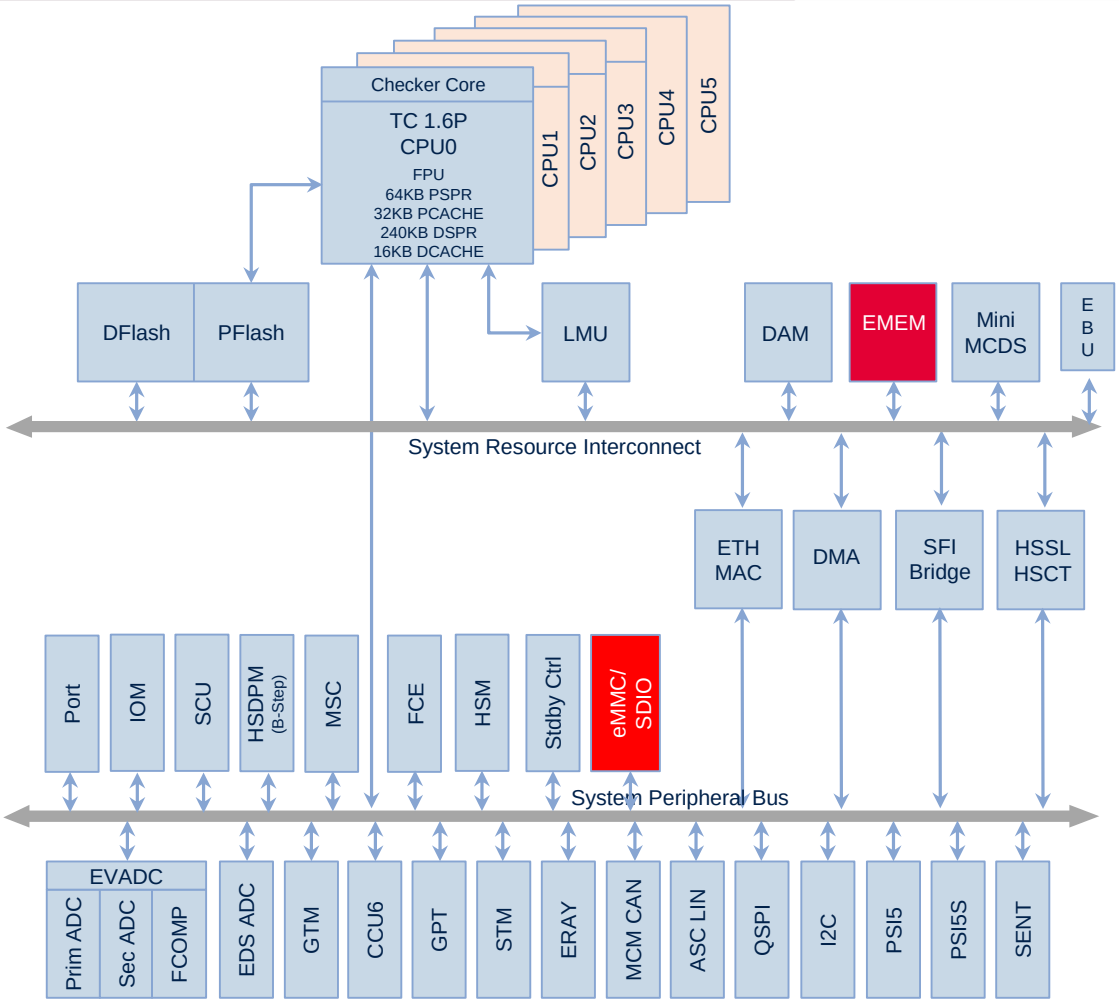
	16MB	16MB	10MB	8MB	9MB	6MB	4MB			2.5MB	2MB			1MB	
	39xXX A-Step	39xXX	38xQ	29xT	37xTX	37xT	27xT	36xD	35xTA	26xD	33xDA	33xL	23xL	32xL	22xL
PMI	6x64	6x64	4x64	32+32+32	3x64	3x64	24+32+32	2x32*	3x64	16+32	2x8*	8*	8	8*	8
Pcache	6x32	6x32	4x32	16+32+32	3x32	3x32	8+16+16	2x32	3x32	8+16	2x32	32	8	32	8
dLMU	6x64	6x64	4x64	-	3x64	3x64	-	2x64	3x64	-	*		-	-	-
DMI CPU 0/1	2x96	2*240	2x240	120+240	2x240	2x240	112+120	2x192*	2x240	72+120	2x96	192*	184	96	88
DMI CPU 2-5	4x96	4x96	2x96	240	96	96	120		1x96						
Dcache	6x16	6x16	4x16	3x8	3x16	3x16	0+8+8	2x16	3x16	0+8	2x16	16	-	16	-
Global LMU	256	768	128	32			32			-			-		-
DAM	128	128	64		32	32	-	0 *		-			-		-
EMEM	4096	4096			4096				2048		1024		-		-
All SRAM w/cache	6112	6912	1568	832	4208	1136	728	672	2837	296	1456	248	200	152	104
All SRAM w/o cache	5824	6624	1376	712	4064	992	576	576	2720	240	1360	200	192	104	96

in discussion

AURIX™– TC39xXX – eXtended feature

6 cores/4 lockstep cores

Feature Set		9x Series (16MB)
TriCore 1.6	# Cores / Checker	6/4
	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	-
Flash	Program Flash	16MB
	Data Flash (physical/logical)	1024/512kB
SRAM	DMI , PMI, LMU, AMU + EMEM	6912kB
DMA	Channels	128
ADC	Converters Primary / Sec / FC / DS	8/4/8/14
	Channels Primary / Sec / FC / DS	64/64/8/14
Timer	GTM TIM / (A)TOM / MCS	94 / 192 / 10
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	2 /4
	CAN-FD / TT	12/1
	QSPI / ASCLIN / I2C	6 /12/2
	SENT / PSI5 / PSI5S	25/4/1
	HSSL / MSC / EBU	1/4/1
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292 **LFBGA 516**

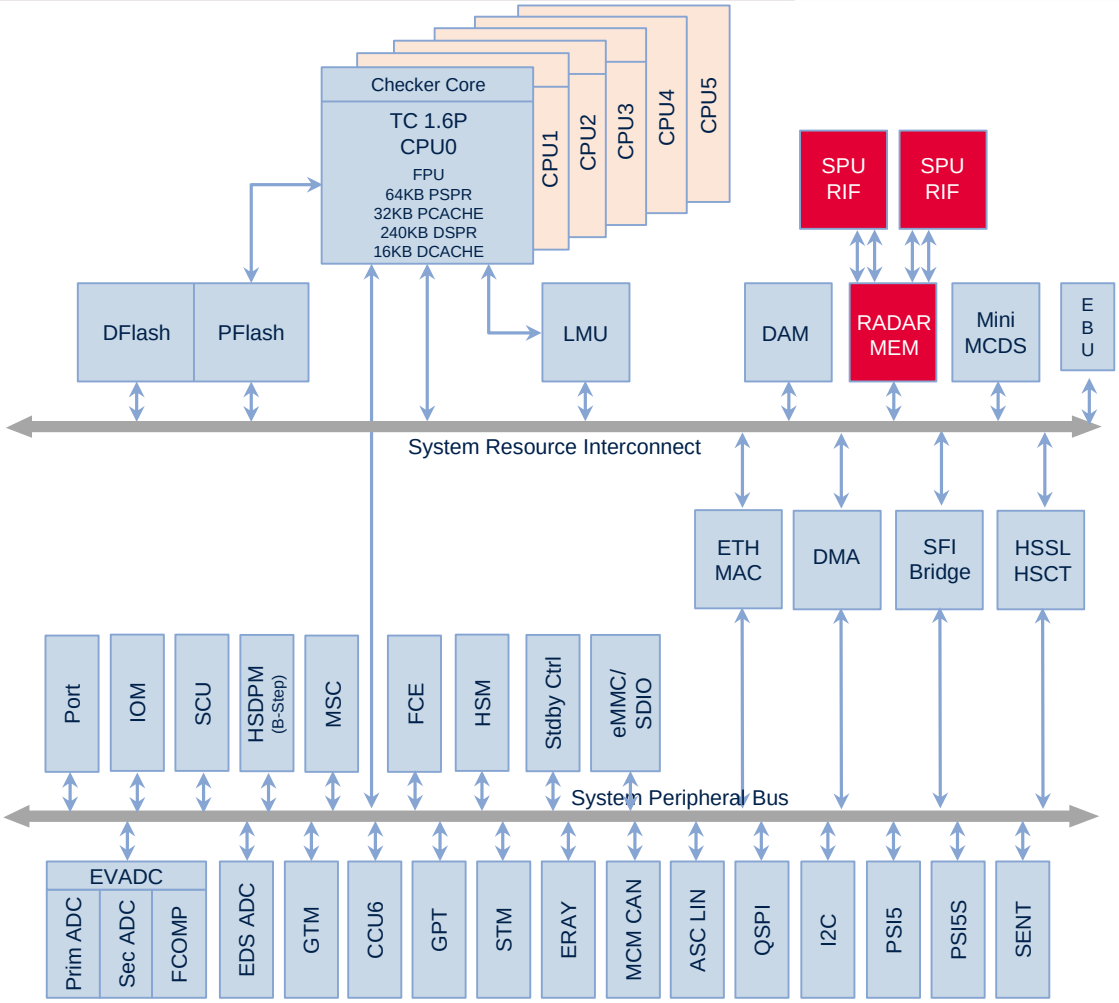
High temperature devices available on request
High performance sign off under evaluation >300MHz
2 Cores with 240kB DSPR + 4 Cores with 96 kB DSPR

preliminary - subject to change

AURIX™– TC39xXA – ADAS feature set

6 cores/4 lockstep cores

Feature Set		9x Series (16MB) + ADAS
TriCore 1.6	# Cores / Checker	6/4
	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	2xSPU
Flash	Program Flash	16MB
	Data Flash (physical/logical)	1024/512kB
SRAM	DMI , PMI, LMU, AMU + RADAR MEM	6912kB
DMA	Channels	128
ADC	Converters Primary / Sec / FC / DS	8/4/8/14
	Channels Primary / Sec / FC / DS	64/64/8/14
Timer	GTM TIM / (A)TOM / MCS	94 / 192 / 10
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	2 /4
	CAN-FD / TT	12/1
	QSPI / ASCLIN / I2C	6 /12/2
	SENT / PSI5 / PSI5S	25/4/1
	HSSL / MSC / EBU	1/4/1
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	12x400MBit LVDS (RIF)
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



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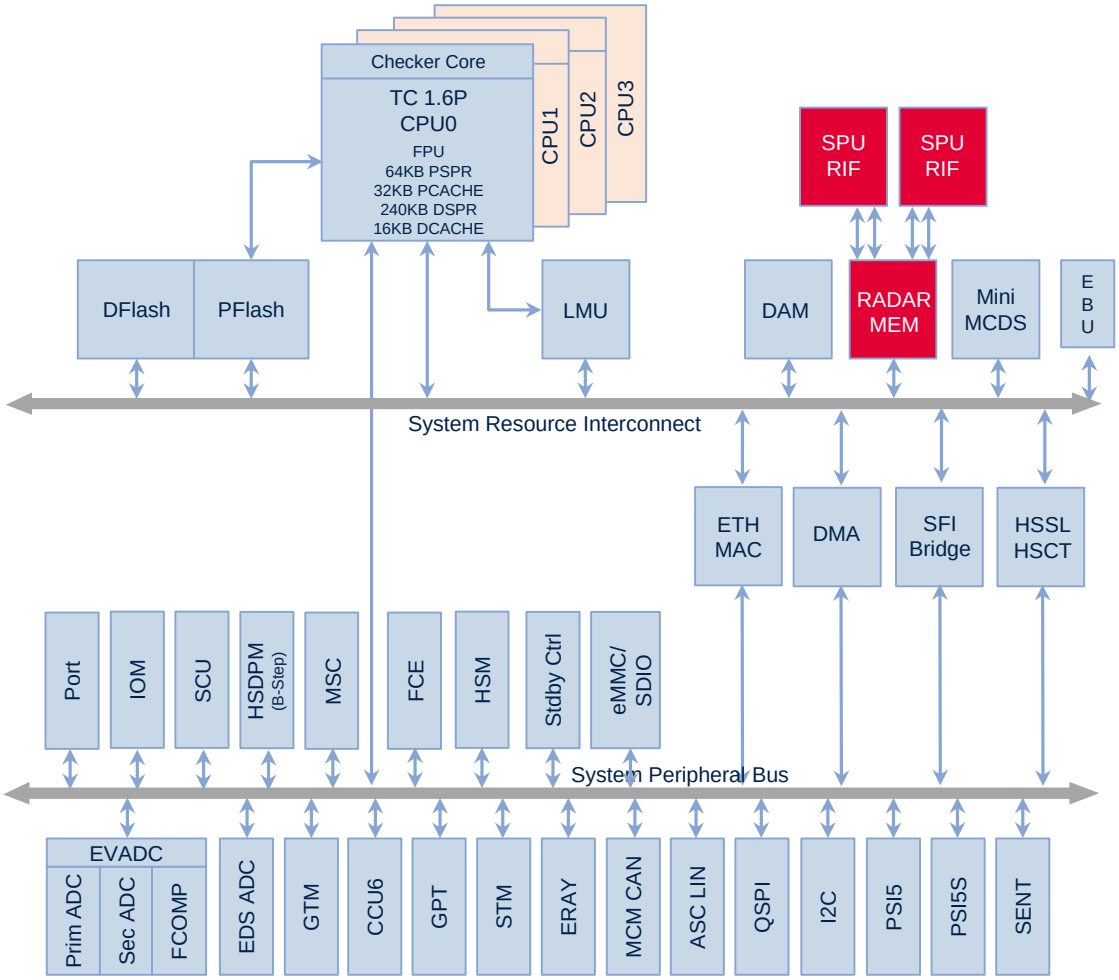
2 Cores with 240kB DSPR + 4 Cores with 96 kB DSPR

preliminary - subject to change

AURIX™– TC39xQA – ADAS feature set

4 cores/3 lockstep cores

Feature Set		9x Series (16MB) + ADAS
TriCore 1.6	# Cores / Checker	4/3
	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	2xSPU
Flash	Program Flash	10MB
	Data Flash (physical/logical)	1024/512kB
SRAM	DMI , PMI, LMU, Cache+ RADAR MEM	6368kB
DMA	Channels	128
ADC	Converters Primary / Sec / FC / DS	8/4/8/14
	Channels Primary / Sec / FC / DS	64/64/8/14
Timer	GTM TIM / (A)TOM / MCS	94 / 192 / 10
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	2 /4
	CAN-FD / TT	12/1
	QSPI / ASCLIN / I2C	6 /12/2
	SENT / PSI5 / PSI5S	25/4/1
	HSSL / MSC / EBU	1/4/1
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	12x400MBit LVDS (RIF)
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292

LFBGA 516

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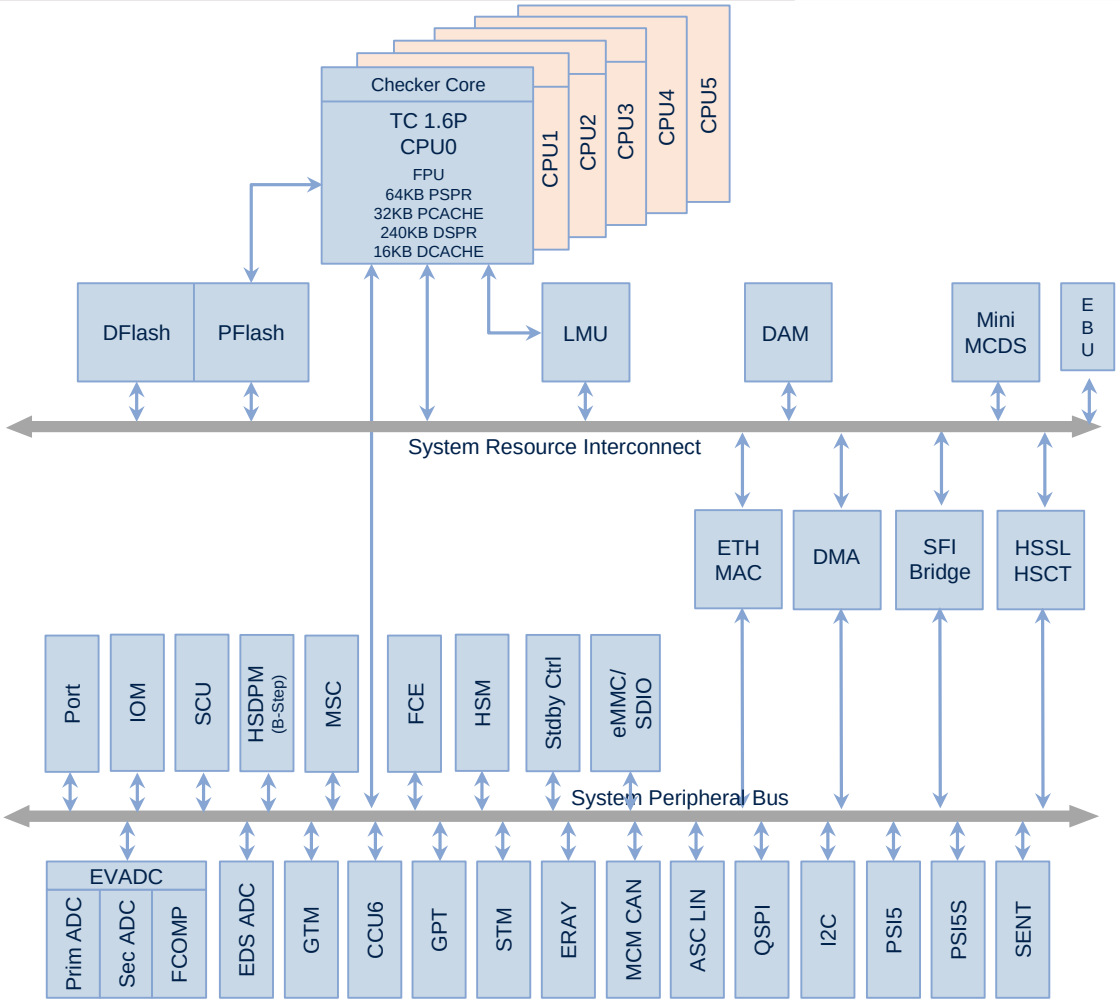
High performance sign off under evaluation >300MHz
2 Cores with 240kB DSPR + 2 Cores with 96 kB DSPR

preliminary - subject to change

AURIX™– TC39xXP

6 cores/4 lockstep cores

Feature Set		9x Series (16MB)
TriCore 1.6	# Cores / Checker	6/4
	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	-
Flash	Program Flash	16MB
	Data Flash (physical/logical)	1024/512kB
SRAM	DMI , PMI, LMU, Cache	2816kB
DMA	Channels	128
ADC	Converters Primary / Sec / FC / DS	8/4/8/14
	Channels Primary / Sec / FC / DS	64/64/8/14
Timer	GTM TIM / (A)TOM / MCS	94 / 192 / 10
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	2 /4
	CAN-FD / TT	12/1
	QSPI / ASCLIN / I2C	6 /12/2
	SENT / PSI5 / PSI5S	25/4/1
	HSSL / MSC / EBU	1/4/1
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292 **LFBGA 516**

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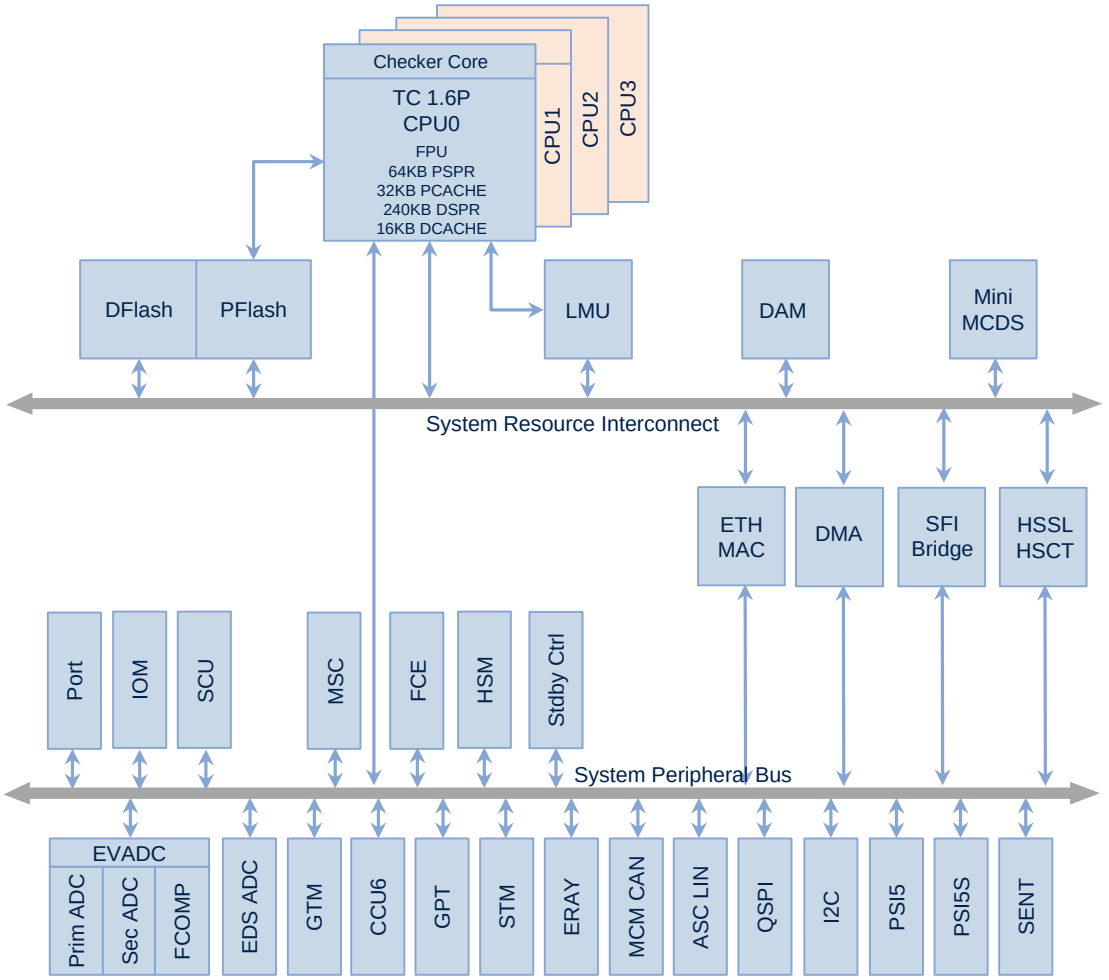
High performance sign off under evaluation >300MHz
2 Cores with 240kB DSPR + 4 Cores with 96 kB

preliminary - subject to change

AURIX™– TC38x series

4 cores/2 lockstep cores

Feature Set		8x Series (10MB)
TriCore	# Cores / Checker	4/2
1.6	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	
Flash	Program Flash	10MB
	Data Flash (single ended)	512kB
SRAM	DMI , PMI, LMU, Cache	1568kB
DMA	Channels	128
ADC	Converters Primary / Sec / FC / DS	8/4/4/10
	Channels Primary / Sec / FC / DS	64/64/4/10
Timer	GTM TIM / (A)TOM / MCS	56 / 152 / 7
	CCU / GPT modules / bit streaming	2/1/0
Interfaces	FlexRay (#/ch.)	2/4
	CAN-FD / TT	12/1
	QSPI / ASCLIN / I2C	5 /12/2
	SENT / PSI5 / PSI5S	25/4/1
	HSSL / MSC / EBU/ eMMc	1/3/0/0
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292 **LFBGA 516**

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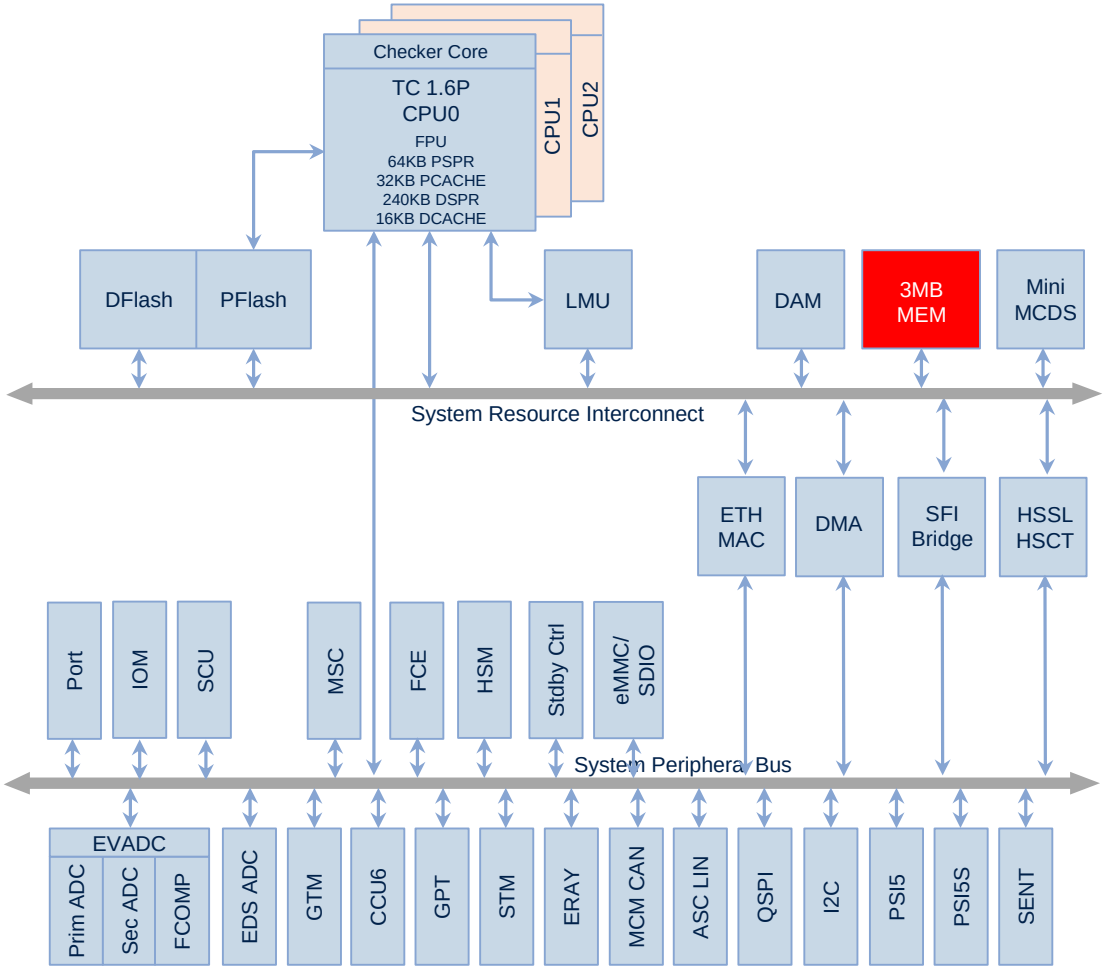
High performance sign off under evaluation >300MHz
2 Cores with 240kB DSPR + 2 Cores with 96 kB DSPR

preliminary - subject to change

AURIX™– TC377TX –feature eXtension

Feature Set		7xX Series
TriCore 1.6	# Cores / Checker	3/3
	Frequency	300MHz
Flash	Program Flash	9MB
	Data Flash (physical/logical)	256/128kB
SRAM	DMI , PMI, LMU, Cahce+ EMEM	4208kB
DMA	Channels	128
ADC	Converters Primary / Sec / FC / DS	4/4/2/6
	Channels Primary / Sec / FC / DS	32/64/2/6
Timer	GTM TIM / (A)TOM / MCS	40 / 88 / 5
	CCU / GPT modules / bit streaming	2/1/0
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	8/1
	QSPI / ASCLIN / I2C	5/12/1
	SENT / PSI5 / PSI5S	15/2/1
	HSSL / MSC / EBU / eMMC	1/2/0 / 1*
	Ethernet 100Mbps/1Gbps	1
	Camera interface (CIF)	1
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292

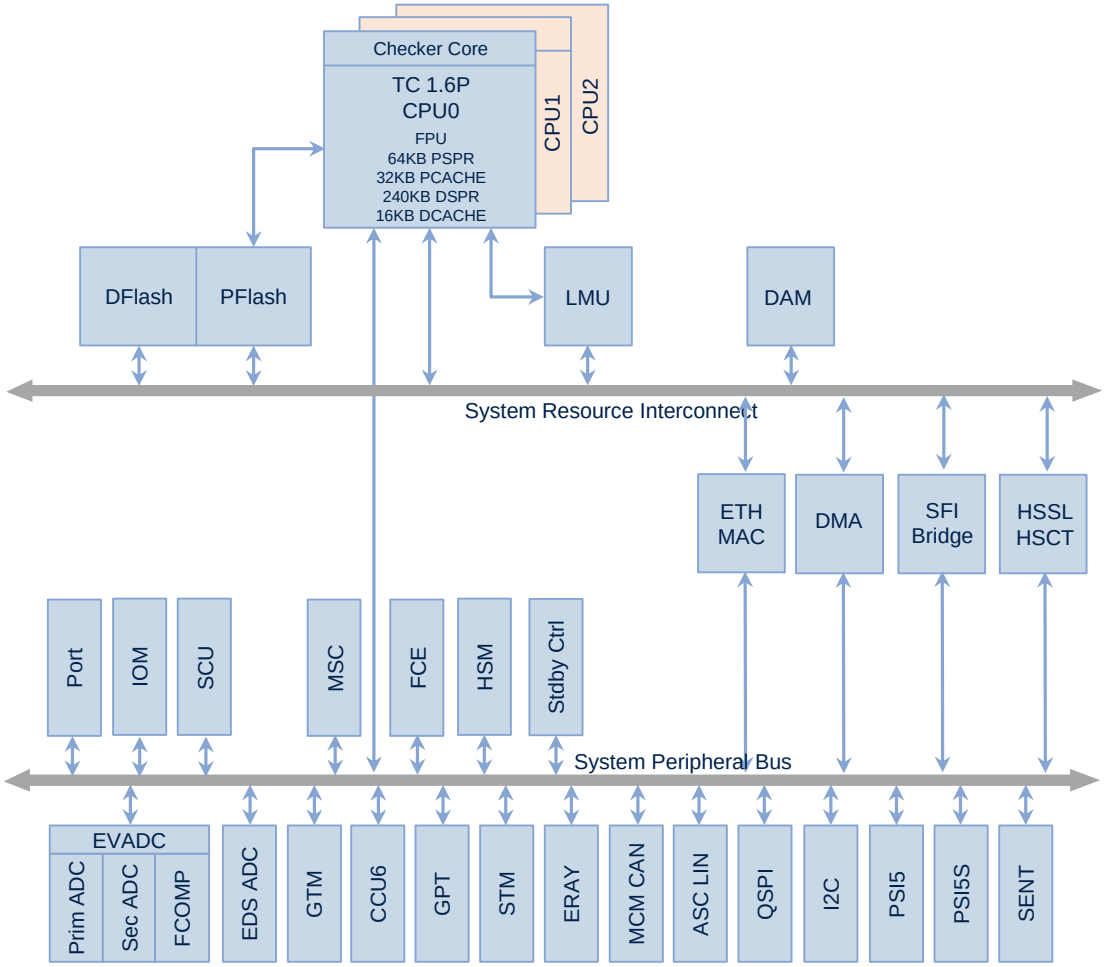
***in discussion**
High performance sign off under evaluation >300MHz
2 Cores with 240kB DSPR + 1 Core with 96 kB DSPR

preliminary - subject to change

AURIX™ - TC37x series

3 cores/2 lockstep cores

Feature Set		7x Series (6MB)
TriCore	# Cores / Checker	3/2
1.6	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	
Flash	Program Flash	6MB
	Data Flash (single ended)	256kB
SRAM	DMI , PMI, LMU, Cache	1136kB
DMA	Channels	128
ADC	Converters Primary / Sec / FC / DS	4/4/2/6
	Channels Primary / Sec / FC / DS	32/64/2/6
Timer	GTM TIM / (A)TOM / MCS	40 / 88 / 5
	CCU / GPT modules / bit streaming	2/1/0
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	8/1
	QSPI / ASCLIN / I2C	5/12/1
	SENT / PSI5 / PSI5S	15/2/1
	HSSL / MSC / EBU	1/2/0
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LQFP 176 **LFBGA 292**

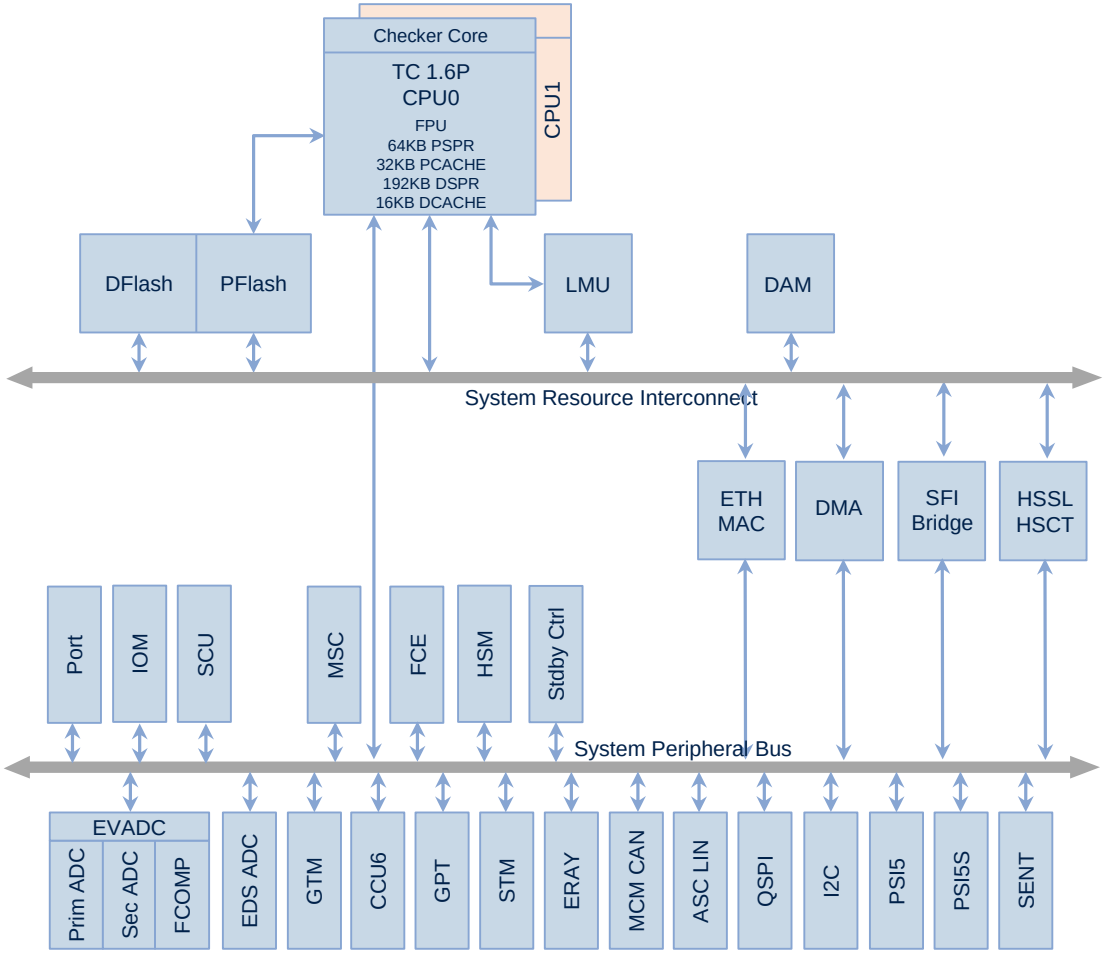
High temperature devices available on request
High performance sign off under evaluation >300MHz
2 Cores with 240kB DSPR + 1 Core with 96 kB

preliminary - subject to change

AURIX™ - TC36x series

2 cores/2 lockstep cores

Feature Set		6x Series (4MB)
TriCore	# Cores / Checker	2/2
1.6	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	
Flash	Program Flash	4MB
	Data Flash (single ended)	128kB
SRAM	DMI , PMI, LMU, Cache	672kB
DMA	Channels	64
ADC	Converters Primary / Sec / FC / DS	4/2/2/4
	Channels Primary / Sec / FC / DS	32/32/2/4
Timer	GTM TIM / (A)TOM / MCS	24 / 64 / 3
	CCU / GPT modules / bit streaming	2/1/0
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	6/1
	QSPI / ASCLIN / I2C	4/12/1
	SENT / PSI5 / PSI5S	10/2/1
	HSSL / MSC / EBU	1/1/0
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

T/LQFP 144 | LQFP 176 | LFBGA 292

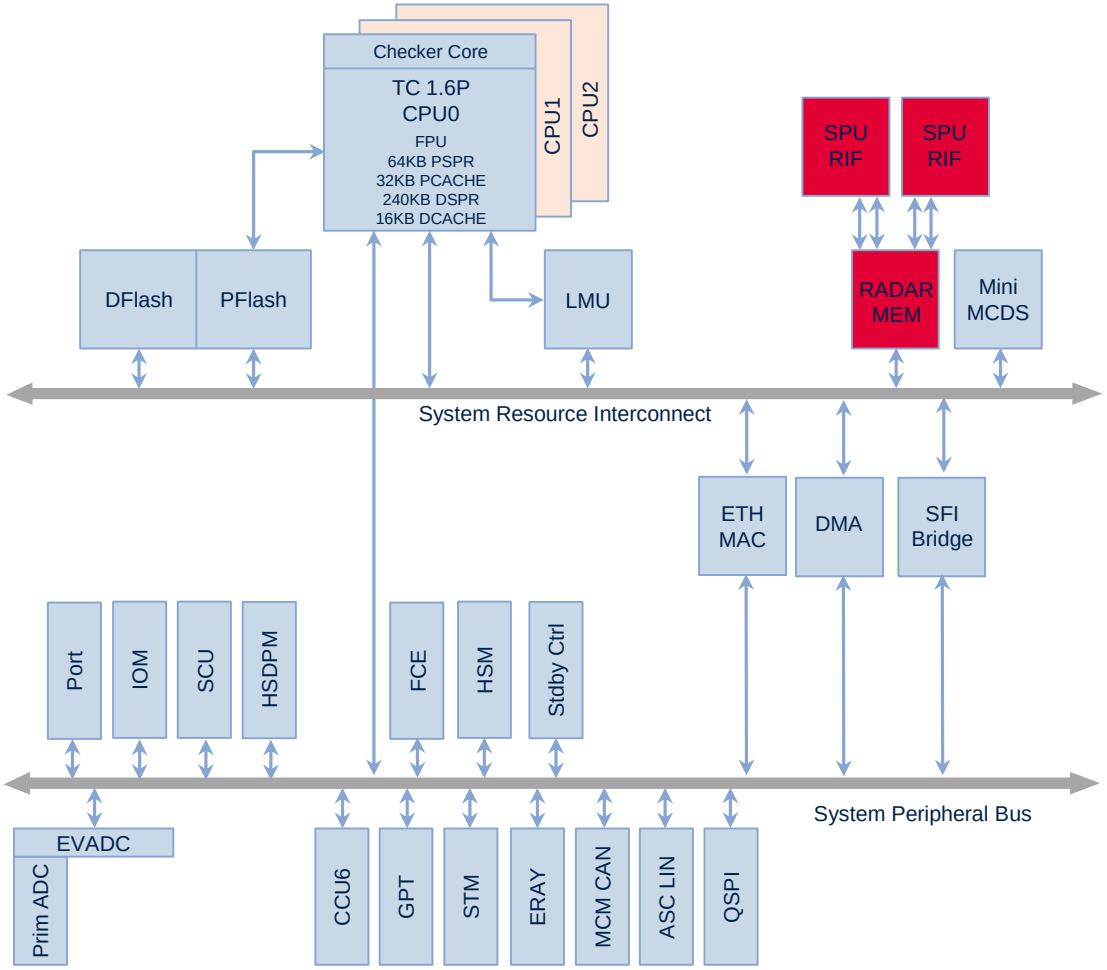
High temperature devices available on request
2 Cores with 196kB DSPR

preliminary - subject to change

AURIX™– TC35xA Series ADAS

3 cores/2 lockstep cores

Feature Set		5x Series ADAS (4MB)
TriCore	# Cores / Checker	3/2
1.6	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	2xSPU
Flash	Program Flash	4MB
	Data Flash (single ended)	128kB
SRAM	DMI , PMI, LMU, Cache + RADAR MEM	2837kB
DMA	Channels	64
ADC	Converters Primary / Sec / FC / DS	2/0/0/0
	Channels Primary / Sec / FC / DS	16/0/0/0
Timer	GTM TIM / (A)TOM / MCS	-
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	6/0
	QSPI / ASCLIN / I2C	4/4/0
	SENT / PSI5 / PSI5S	0/0/0
	HSSL / MSC / EBU	0/0/0
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	12x400Mbps LVDS
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292

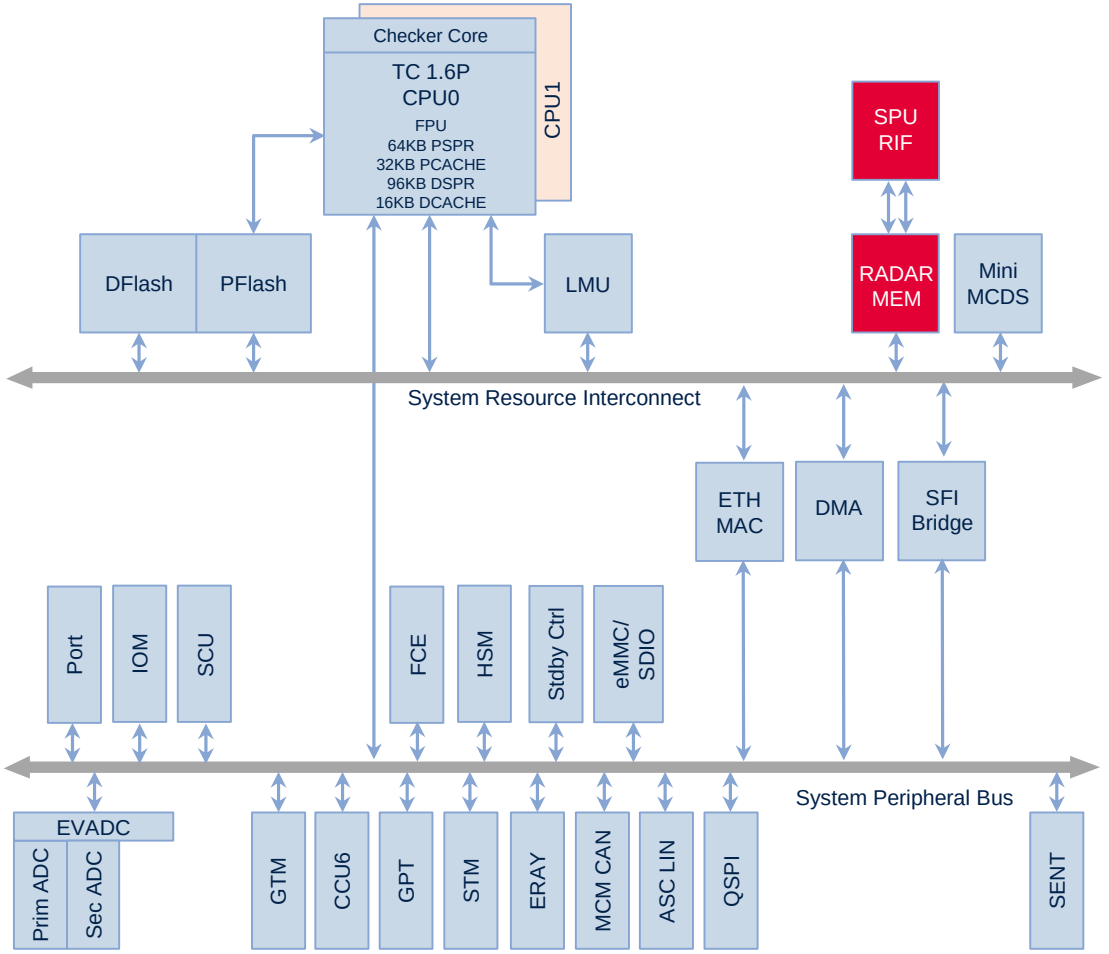
High temperature devices available on request
2 Cores with 240kB DSPR + 1 Core with 96 kB

preliminary - subject to change

AURIX™– TC33xA Series ADAS

2 cores/1 lockstep core

Feature Set		3x Series ADAS (2MB)
TriCore 1.6	# Cores / Checker	2/1
	Frequency	200MHz
Accelerator	Signal processing Unit (SPU)	1xSPU
Flash	Program Flash	2MB
	Data Flash (single ended)	256kB
SRAM	DMI , PMI, LMU, Cache + RADAR MEM	1456kB
DMA	Channels	16
ADC	Converters Primary / Sec / FC / DS	4/2/0/0
	Channels Primary / Sec / FC / DS	>16/32/0/0
Timer	GTM TIM / (A)TOM / MCS	16 / 32 / 0
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	8/0
	QSPI / ASCLIN / I2C	4/12/0
	SENT / PSI5 / PSI5S	6/0/0
	HSSL / MSC / EBU / eMMC	0/0/0/ 1
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	6x100Mbps LVDS
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292

TQFP 144

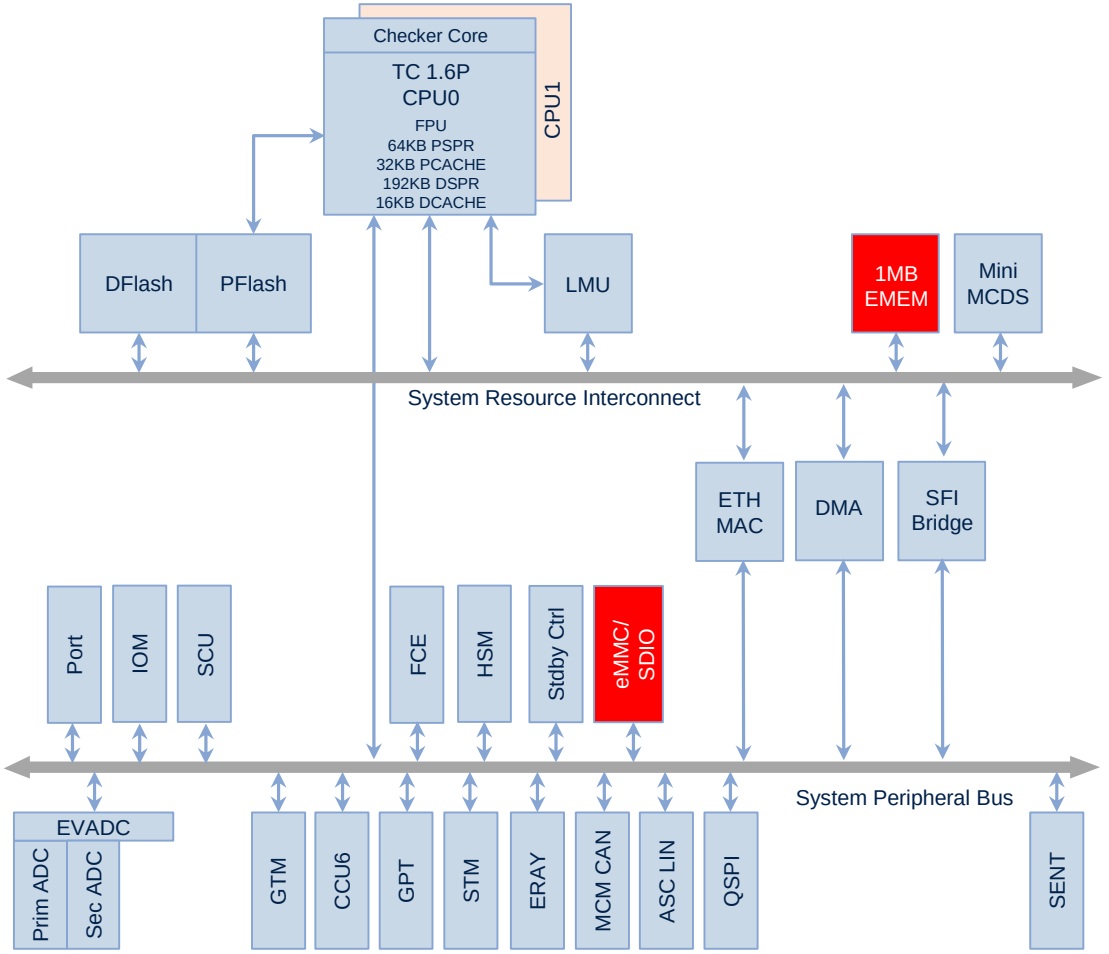
High temperature devices available on request
2 Cores with 96kB DSPR

preliminary - subject to change

AURIX™– TC33x**X** – feature e**Xtension**

2 cores/1 lockstep core

Feature Set		3x Series (2MB)
TriCore 1.6	# Cores / Checker	2/1
	Frequency	200MHz
Accelerator	Signal processing Unit (SPU)	1xSPU
Flash	Program Flash	2MB
	Data Flash (single ended)	256kB
SRAM	DMI , PMI, LMU, Cache + EMEM	1456kB
DMA	Channels	16
ADC	Converters Primary / Sec / FC / DS	4/2/0/0
	Channels Primary / Sec / FC / DS	>16/32/0/0
Timer	GTM TIM / (A)TOM / MCS	16 / 32 / 0
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	8/0
	QSPI / ASCLIN / I2C	4/12/0
	SENT / PSI5 / PSI5S	6/0/0
	HSSL / MSC / EBU / eMMC	0/0/0/ 1
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292

TQFP 144

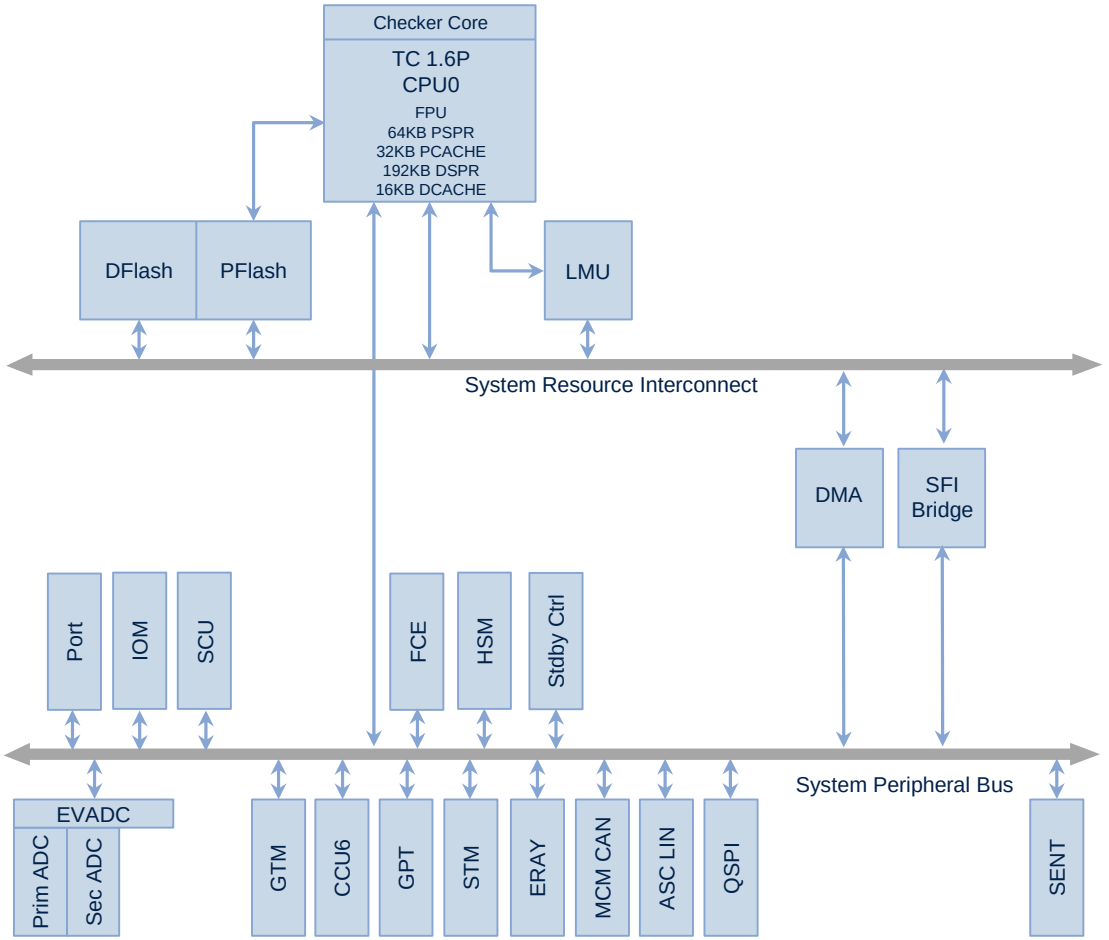
High temperature devices available on request
2 Cores with 196kB DSPR

preliminary - subject to change

AURIX™ - TC33x series

1 core/1 lockstep core

Feature Set		3x Series (2MB)
TriCore	# Cores / Checker	1/1
1.6	Frequency	200MHz
Accelerator	Signal processing Unit (SPU)	
Flash	Program Flash	2MB
	Data Flash (single ended)	128kB
SRAM	DMI , PMI, LMU, Cache	248kB
DMA	Channels	16
ADC	Converters Primary / Sec / FC / DS	2/2/0/0
	Channels Primary / Sec / FC / DS	16/32/0/0
Timer	GTM TIM / (A)TOM / MCS	16 / 32 / 0
	CCU / GPT modules / bit streaming	2/1/0
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	8/0
	QSPI / ASCLIN / I2C	4/12/0
	SENT / PSI5 / PSI5S	6/0/0
	HSSL / MSC / EBU	0/0/0
	Ethernet 100Mbps/1Gbps	-/-
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

TQFP 100 | TQFP 144 | LFBGA 292

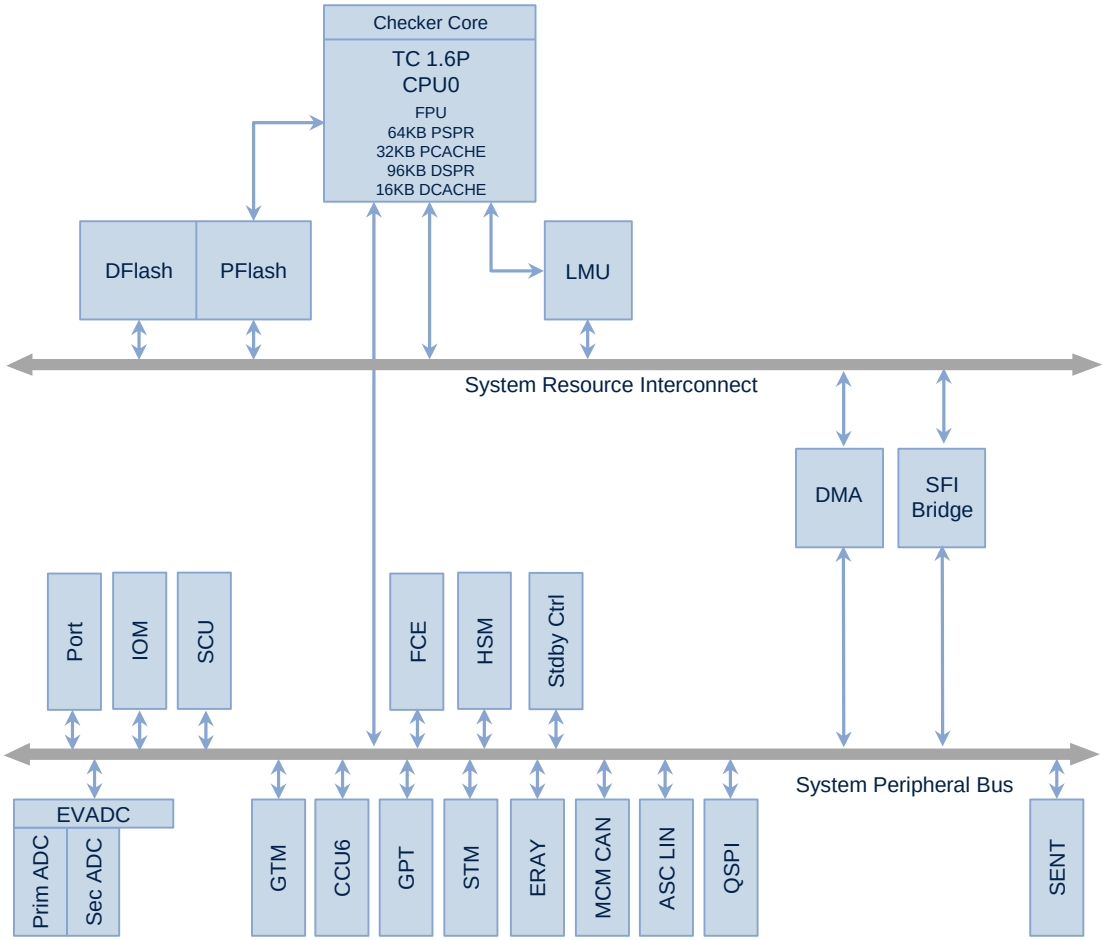
High temperature devices available on request

preliminary - subject to change

AURIX™ - TC32x series

1 core/1 lockstep core

Feature Set		3x Series (2MB)
TriCore	# Cores / Checker	1/1
1.6	Frequency	160MHz
Accelerator	Signal processing Unit (SPU)	
Flash	Program Flash	1MB
	Data Flash (single ended)	96kB
SRAM	DMI , PMI, LMU, Cache	156kB
DMA	Channels	16
ADC	Converters Primary / Sec / FC / DS	2/2/0/0
	Channels Primary / Sec / FC / DS	16/32/0/0
Timer	GTM TIM / (A)TOM / MCS	16 / 32 / 0
	CCU / GPT modules / bit streaming	2/1/0
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	6/0
	QSPI / ASCLIN / I2C	4/12/0
	SENT / PSI5 / PSI5S	6/0/0
	HSSL / MSC / EBU	0/0/0
	Ethernet 100Mbps/1Gbps	-/-
	RADAR /ext. ADC IF (RIF)	-
Security	HSM	optional
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	optional



Package Variants

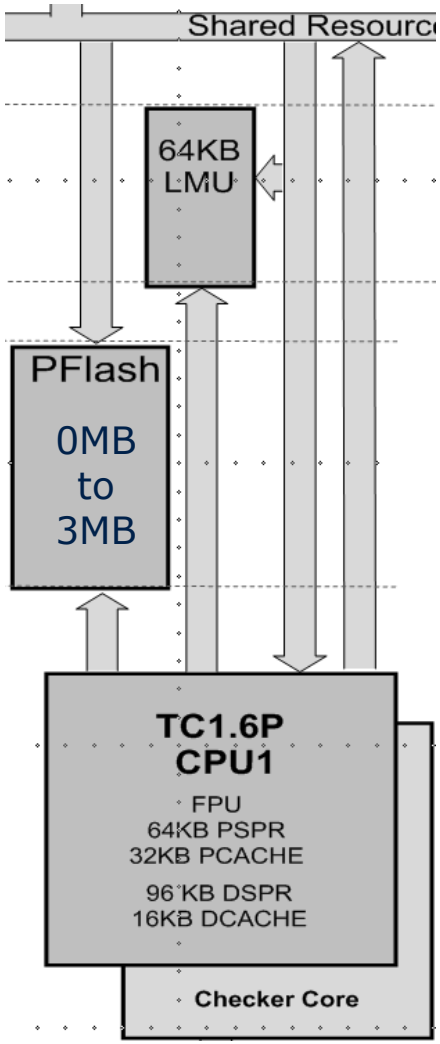
TQFP 100 | TQFP 144 | LFBGA 292

High temperature devices available on request

preliminary - subject to change

Enhanced Local Memory Concept
For Tricore CPUs

- All PFLASH modules are mapped in a continuous address space starting at 8000 0000 / A000 0000
- Local dLMU and global LMU, are mapped in a continuous address space starting at 9000 0000
- All CPUs will provide the same local memory structures
  - 64kB PSPR: 0WS for code fetch
  - 32kB Program Cache
  - 96 to 240kB DSPR: 0WS for data access
  - 16kB Data Cache
  - 64kB local dLMU : 1(2)WS for data read(write)
  - Local path to one PFLASH bank with up to 3MB



AURIX™ TC3xx Memory Concept

Local And Global Memory

- Enhanced protection in AURIX™ - TC3xx
  All memory data and addresses and all accesses to all memories are protected
- Enhanced local and global memory concept
  - Local memories are providing enhanced performance to the specified CPU:
    PSPR, DSPR, dLMU, PFLASH, (Data Cache, Program Cache)
  - All CPUs can access all local memories of other CPUs with "global" performance
  - Global memories have no preferences: global LMU, DAM, EMEM, D-Flash
    All CPUs can access all global memories with "global" performance
- memory access performance

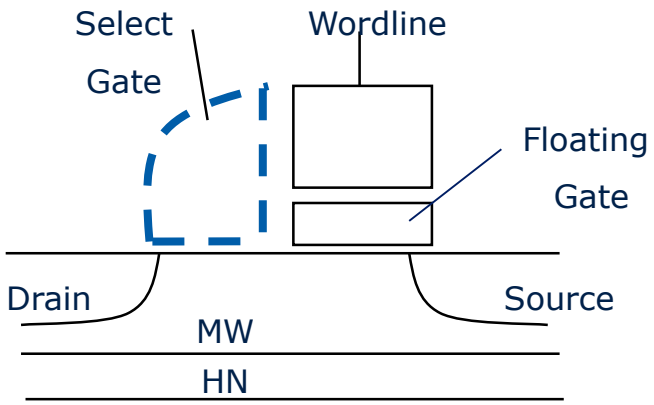
local access wait states

access type	data read	data write	code fetch
local PSPR	6	7	0
local DSPR	0	0	
local dLMU	1	2	7
local PFLASH	3+Flash		2+Flash

global access wait states

access type	data read	data write	code fetch
other PSPR	6	7	6
other DSPR	6	6	6
other local dLMU	7	8	7
other PFLASH	9+Flash		8+Flash
DFLASH	8+Flash		
global LMU, DAM	7	8	7
EMEM	18	10	18

AURIX™ - TC3xx Flash



Aurix Flash Cell

HS3P – Hot Source 3 Poly

Program Flash Parameters

- Programming Granularity: 32 Byte
- Access time: 30ns
- Erase Time (Sector range): ~ 1sec
- Erase Granularity: Sector
- Data Retention: 20y for 1k w/e
- Erase suspend + resume functions
- Erase suspend time <120us
- ECC: 2bit correction, >3bit detection

Data Flash Parameters

- Endurance = 500k or 125k
- Programming Time ~ 75us
- Programming Granularity: 8 Byte
- Access time: 100ns
- Erase Time (Sector range): ~ 1sec
- Erase Granularity: Sector 8kB
- Data Retention 10y
- Erase suspend + resume functions
- Erase suspend time <120us
- ECC: 3bit correction, >4bit detection

Subject to change

AURIX™ - TC3xx Data Flash Options
Single Ended Sensing / Complement Sensing

Two options for operating the Data FLASH: single ended sensing and complement sensing

- configured in user settings - no dynamic change!
- software driver adaptation required (MCAL will support single ended first)

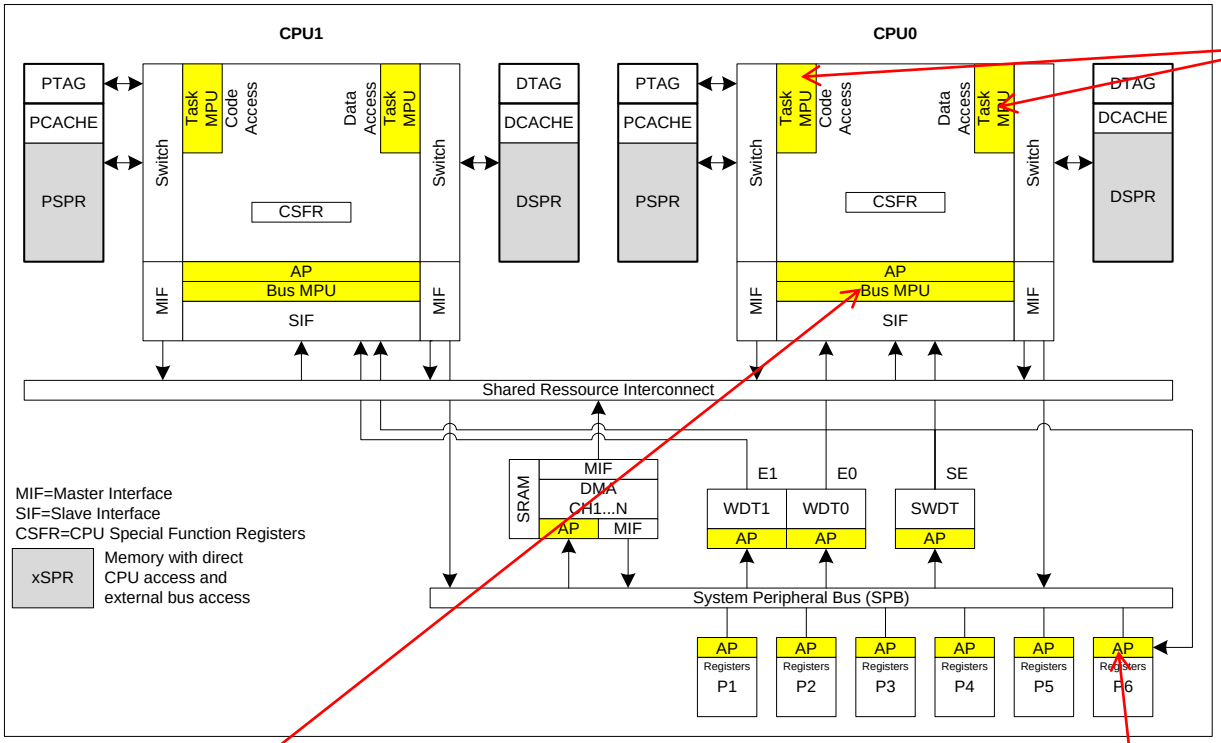
	single ended sensing	**complement sensing**
endurance	125k cycles	500k cycles
Flash cells per bit	1	2

	TC39x (16MB)	**TC38x (10MB)**	**TC37x (6MB)**	**TC36x (4MB)**	**TC35x (4MB)**	**TC33x (2MB)**
Data Flash Single Ended Sensing	1024kB	512kB	256kB	128kB	128kB	128kB
Data Flash Complement Sensing	512kB	256kB	128kB	64kB	64kB	64kB

Subject to change

AURIX™ TC3xx Protection System

Enhanced CPU MPU: 18 data and 10 code Ranges



CPU MPU

- Monitors **direct** access to Local Memories
- Applies to SW Tasks
- **18** data and **10** code ranges; organized in sets; switched via PSW;
- Dynamic re-configuration possible (typically OS)
- Scope: whole address space

Bus MPU

- Monitors SRAM accesses via SRI BUS
- Static or dynamic configuration
- Scope: local SRAM address space

Register Access Protection

- Monitors write accesses to module registers
- Static configuration
- Scope: register address space

AURIX™ - TC3xx

GTM Configurations

AURIX™ - TC3xx (GTM V3.1.2.0 – 2014.12.17)		**TC39x** 16MB	GTM V1.5.5.1	**TC38x** 10MB	GTM V1.5.5.1	**TC37x** 6MB	GTM V1.5.5.1	**TC36x** 4MB	GTM V2.02.1	**TC33x** 2MB
compare with AURIX (65nm) (GTM V1.5.5.1 and V2.02.1)			TC29x 8MB		TC27x 4MB		TC26x 2.5MB		TC23x 2MB	
Timer Inputs	**Total channels**	**64**	48	**56**	32	**40**	24	**24**	8	**16**
TIM	8 channels	**8**	6	**7**	4	**5**	3	3	1	2
Timer Outputs	**Total channels**	**192**	152	**152**	88	**88**	64	**64**	32	**32**
TOM	Standard 16-bit PWM ch.	**6**	5	5	3	3	2	2	2	2
ATOM	Complex 24-bit PWM ch.	**12**	9	9	5	**6**	4	4	0	0
DTM (with 4ch each)	Dead Time Module	**12** (TOM0-5) **12** (ATOM0-5)		**8** (TOM0-3) **12** (ATOM0-5)		**6** (TOM0-2) **10** (ATOM0-4)		**4** (TOM0-1) **8** (ATOM0-3)	**2** (TOM0-1)	**4** (TOM0-1)
SRAM	**Total**	**144.39**	56.75	**104.76**	35.13	**71.13**	26.13	**44.13**	0	0
MCS	Sequencer RAM 1536x32bit	**120**	36	**84**	24	**60**	18	**36**	0	0
PSM	FIFO, 1024x29bit	**3**x 3.63	2x 3.63	2x 3.63	3.63	3.63	3.63	3.63	0	0
DPLL	SRAM	13.5	13.5	13.5	7.5	7.5	4.5	4.5	0	0
Configuration										
Clock Generation	**DPLL**	1	1	1	1	1	1	1	0	0
	CMU	1	1	1	1	1	1	1	1	1
	TBU	3	3	3	3	3	3	3	1	1
Processing	**MCS**	**10**	6	**7**	4	**5**	3	3	0	0
amount 200MHz clusters	max MCS0-MCS4	**5**		**5**		**5**		**3**		
Pattern Evaluation	**SPE**	**6**	4	4	2	2	2	2	0	0
Broadcast Unit1	**BRC**	1	1	1	1	1	1	1	0	0
Safety	**MON**	1	1	1	1	1	1	1	1	1
	CMP	1	1	1	1	1	1	1	1	1

AD Converters In AURIX TC3xx

Proven SAR Architecture

- Four ADC types:
  - Primary SAR: 12 bit
  - Secondary SAR: 12 bit
  - Fast Compare: 10 bit
  - Delta Sigma

- Improvements
  - SAR ADCs: Reduced switched capacitive load on SAR analog inputs 0.5 / 3 pF (with / without buffer option)
  - Delta Sigma: improved modulator, improved analog input with switch cap

Delta Sigma	Primary SAR	Secondary SAR	Fast Compare
up to 40Msamples/s	up to 2.5Msamples/s	up to 1.4Msamples/s	up to ≤ 5Msamples/s

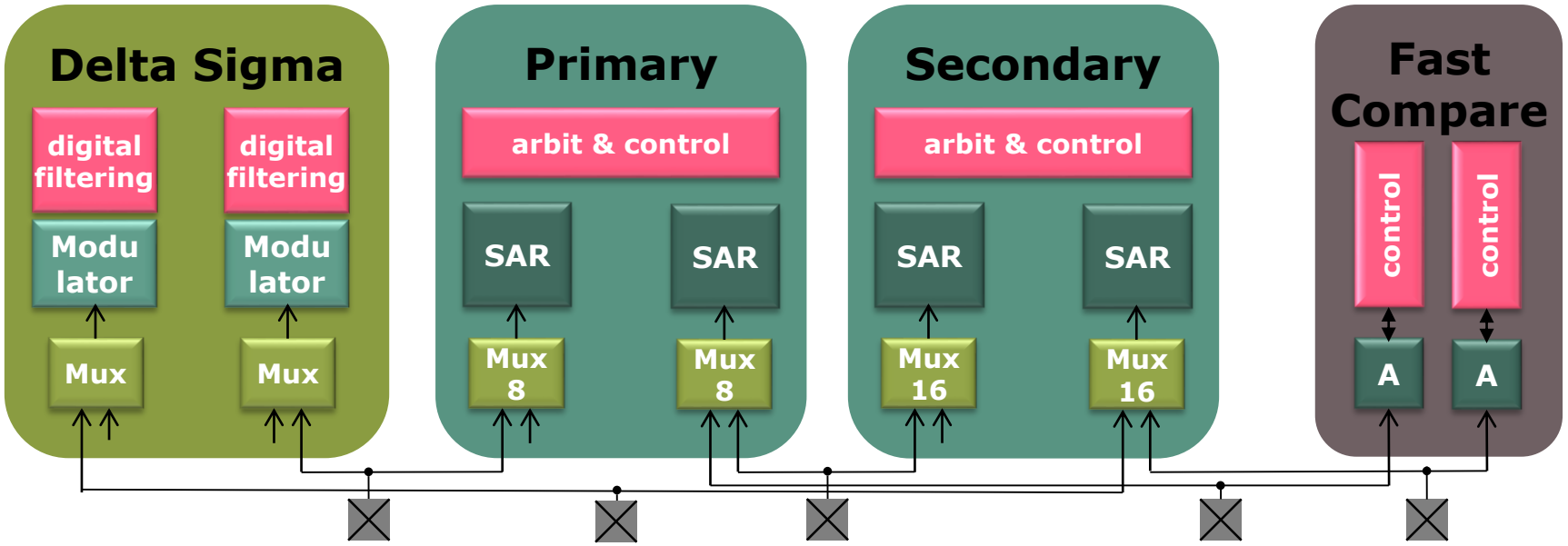
AD Converters in AURIX™ - TC3xx

Proven SAR Architecture

- Four ADC types:
  - **Primary SAR**: 12 bit, ≤ 2.5Msamples/s
  - **Secondary SAR**: 12 bit, ≤ 1.4Msamples/s
  - **Fast Compare**: 10 bit, ≤ 5Msamples/s
  - **Delta Sigma**: 10-13 ENOB ≤ 40Msamples/s
- Two ADCs on every analog input
  improved equidistant and parallel sampling:
  - primary and secondary
  - primary & delta sigma or fast compare
  - secondary & delta sigma or fast compare

ADC Improvements in AURIX™ - TC3xx

- SAR ADCs: Reduced capacitive load on SARs' analog inputs 0.5 / 3 pF (with / without buffer option)
- Delta Sigma ADC:
  - 50% less power consumption (versus AURIX)
  - automatic gain and offset calibration (no CPU load)
    - switched CAP AC replaces analog input amplifier
  - improved switched analog input impedance: 500KΩ (was 100KΩ for Gain=1)
  - improved lower pass-band frequency range for new mode $f_D=f_{PB}*6$ (results in min 4-10kHz PB)



AURIX™ - TC3xx

AD Converter Overview

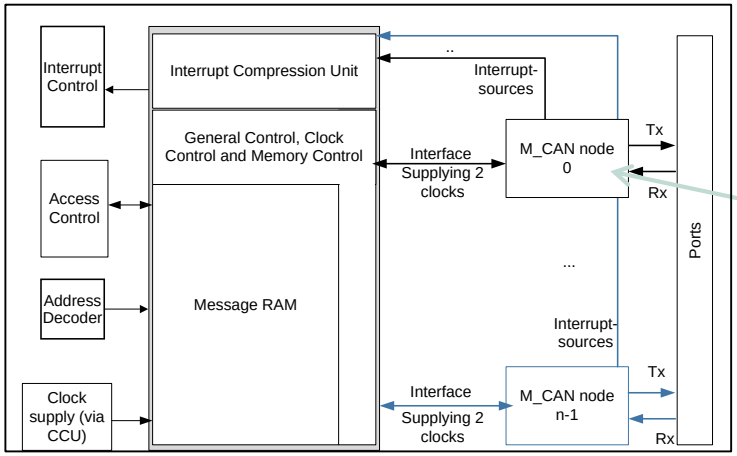
	TC39x (16MB)	TC38x (10MB)	TC37x (6MB)	TC36x (4MB)	TC33x (2MB)
SAR Sampling Stages	12	12	8	6	4
Secondary ADC	4×SAR	4×SAR	4×SAR	2×SAR	2×SAR
Primary -ADC	8×SAR	8×SAR	4×SAR	4×SAR	2×SAR
Fast Compare	8	4	2	2	0
DSADC	14	10	6	4	0
Analog inputs (AURIX TC2xx) In Package Variant	74+28 (=102) (84) BGA516	72+28 (=100) (84) BGA516	48+28 (=76) (60) BGA292	48+12 (=60) (48) QFP176	24+10 (=34) (24) QFP144

- Primary ADC : 8/4/2 SAR AD converters with 8-fold multiplexer , 12-Bit resolution
- Secondary ADC - Background ADC: 4/2 SAR AD converters with 16-fold multiplexer , 12-Bit resolution
- Fast Compare Channels: 4/2/1 fast comparators, no multiplexer, 10-Bit resolution for digital compare register
- ADC clock:
  - generated from non FM modulated Peripheral PLL (f_{PER}) with low jitter
  - synchronization stages in-between f_{SPB} and f_{PER}
- leakage targets for standard analog input pins (non GPIO overlaid) ± 150nA
  leakage targets for overlaid pins (GPIO overlaid) most likely increased to ±600nA

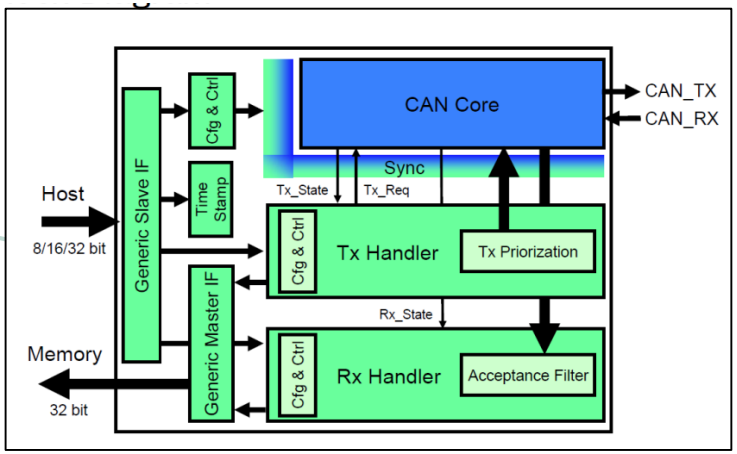
New CAN Module: MCMCAN

- MCMCAN: module name in AURIX™ - TC3xx documentation
- Features
  - CAN-FD
  - M_CAN IP
  - Speed: up to 8Mbit/s
  - TC39x: 12nodes; TC38x/7x: 8nodes; TC36x-2x: 6nodes
  - Debug over CAN
  - Pretended Networking features
  - Module features (a product may have multiple modules)
    - Up to 4 CAN nodes per module; TC39x has 3 modules, all other have 2 modules
    - 16 interrupts per module; configurable trigger source
    - External and internal loop back modes
    - Local FIFO/buffer SRAM with configurable block sizes and full DMA support (example CAN2.0: compares to up to 80MO Rx and 32MO Tx)

Blockdiagram MCMCAN

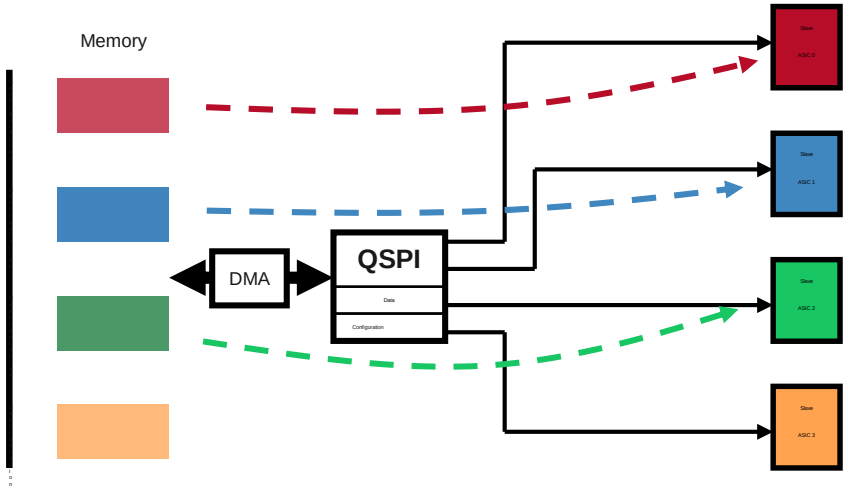


Blockdiagram M_CAN node

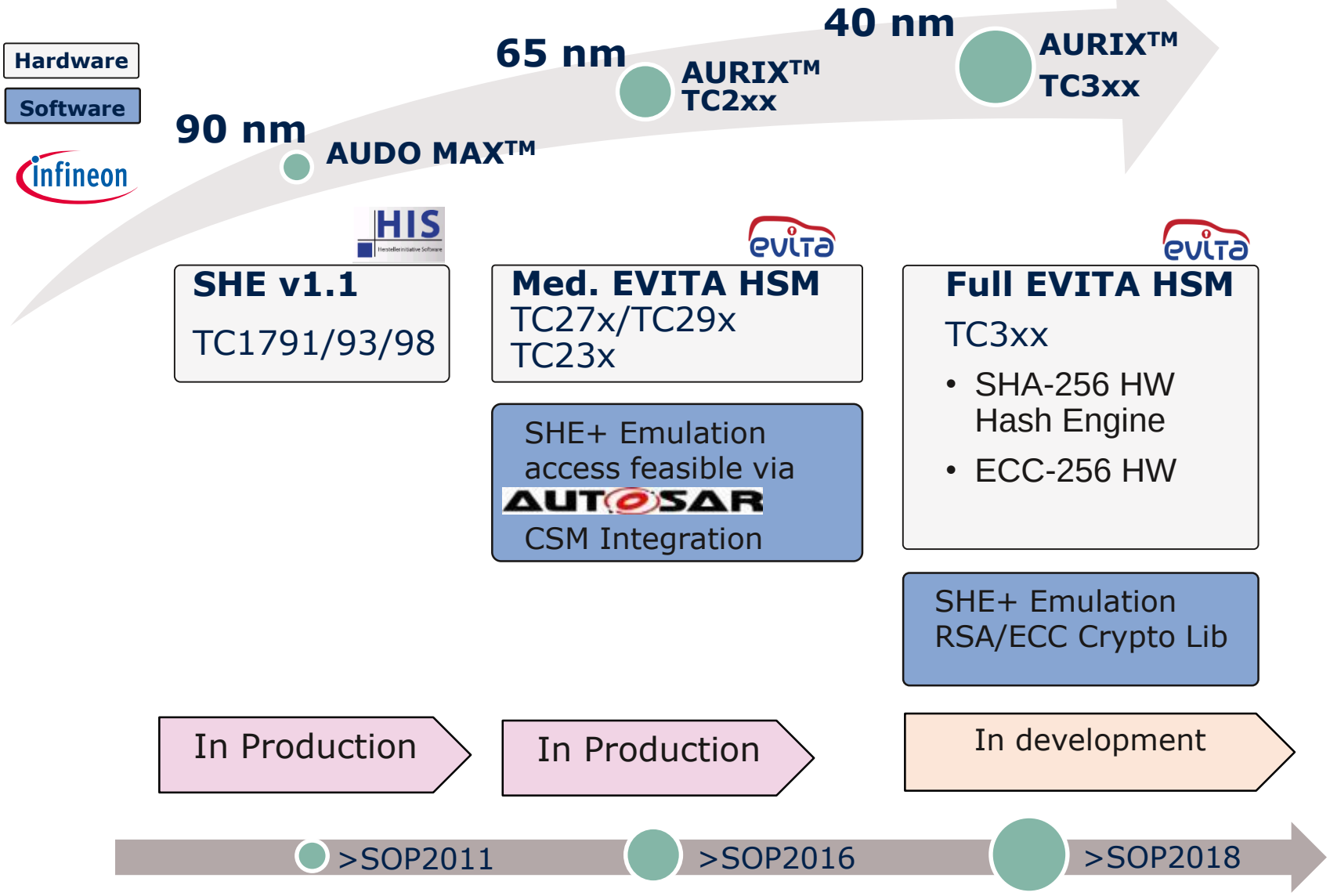


Queued SPI (QSPI)

- Supports widespread & typical multi channel SPI applications
- Up to 16 channels available
- Frame formats from 2 bits to up to 32 bits (plus parity)
- Dynamic channel configuration during operation
- Transmit/receive clock speed up to 50MBaud
- Parity support
- DMA support
- Memory based queues
- PWM over QSPI serialization
- Loop Back Mode
- Module reset
- Functional compatible to TriCore SSC

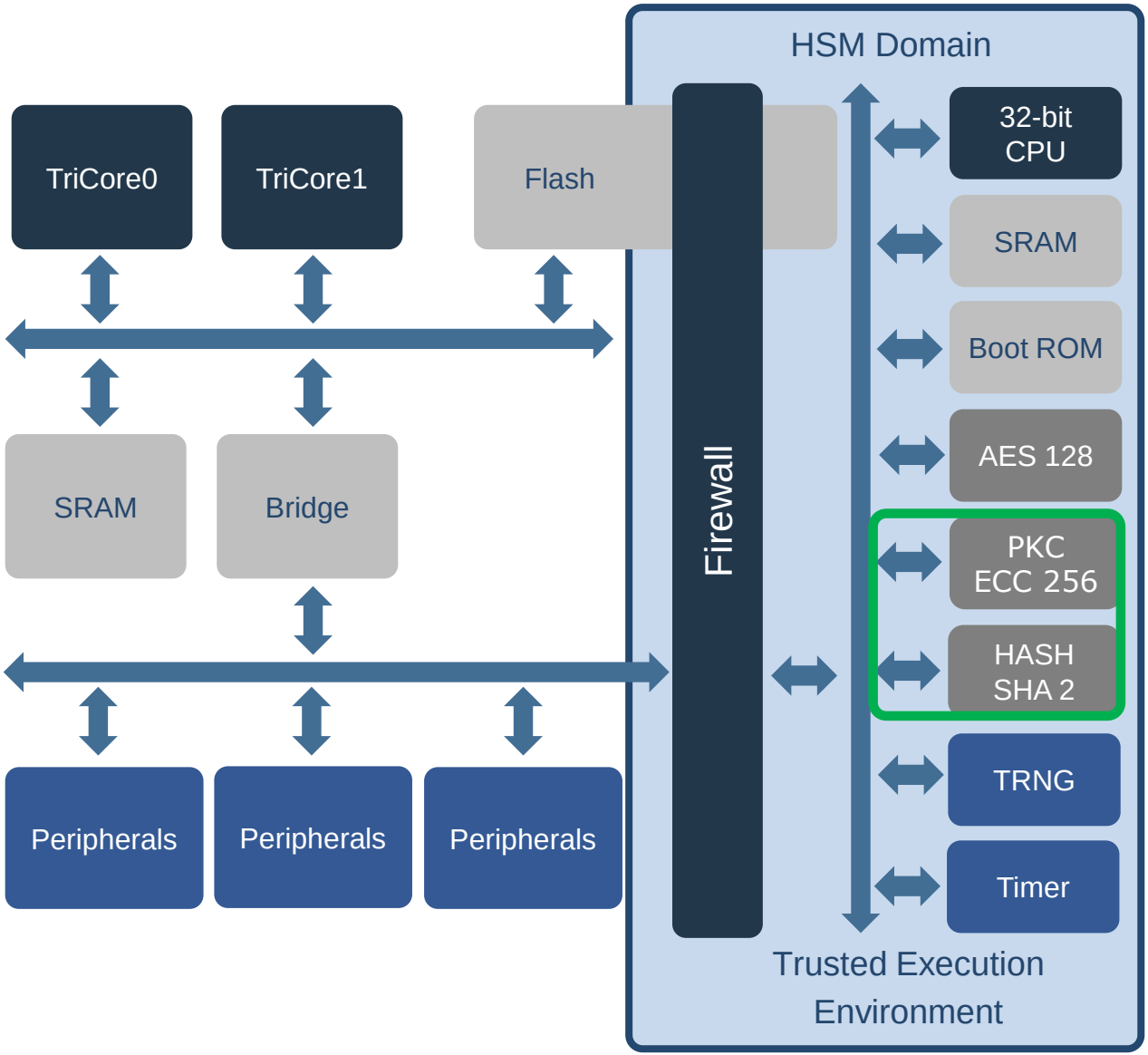


Security Standard Compliance
IFX Microcontroller Security Roadmap



Performance Hardware Security Module (HSM)

AURIX TC3xx: Full EVITA compliant



Performance HSM Features:

- **32-bit processor** with up to 100MHz CPU speed
  - MPU (Memory Protection Unit)
  - 64KB SRAM

  Flash
  - Code storage in 4x64KB+2x16KB reserved HSM PFlash below 2MB
  - Key Storage, Secure Data and Counter in HSM only 2x32kB DFlash
- **AES-128** Hardware Accelerator for symmetric block ciphers (5 contexts)
  - ECB, CBC, CTR, OFB, CFB, GCM & XTS
- **PKC - ECC-256** Hardware Accelerator
- **SHA224/256** Hardware Accelerator
- **T**rue **R**andom **N**umber **G**enerator (**TRNG**) to generate 128-bit random numbers
  - AIS 31 class P2 compliant

Agenda

1. Infineon Microcontroller
2. AURIX TC3xx Overview
3. AURIX TC3xx Features Details
4. AURIX TC3xx Performance
5. AURIX TC3xx Safety Supply
6. AURIX TC3xx SW & Tools
7. AURIX TC3xx Schedule

Performance Increase With AURIX TC3xx

- **Performance increase: code execution from P-Flash:**
  - The crossbar access improves by several clock cycles.
  - Crossbar arbiter with access preference: Access to one PFLASH module behaves like a dedicated path. All other accesses are as in AURIX.
  - A typical code execution (AUTOSAR) will improve by 5-10% depending on cache hit rate and jump location settings.

- **Performance increase TC33x/TC32x: TriCore 1.6P instead of 1.6E;**
  - Performance increase by up to 25% depending on application code
  - Power consumption increase by 30%, 10/20mA (without/with lockstep)

- **Performance increase on peripherals:**
  - CAN-FD: up to 8Mbit/s (was 5Mbit/s)
  - GTM: 200MHz clock option; better granularity on PWM
  - Pads: 5V option on TC33x and TC32x

Performance Increase With AURIX TC3xx

New CRC instruction in TriCore: Fully flexible CRC calculation for handling the many variations of CRCs being used in safety applications

- Programmable polynomial up to CRC16
- Result register is seed register
  - seamless repetition
  - Programmable seed;
- Programmable data length up to 8bit;
  - for more length use seamless repetition
  - no issues with little or big endian
- Single cycle execution within pipeline

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New ADAS -Power-Supply Family TLF3068x

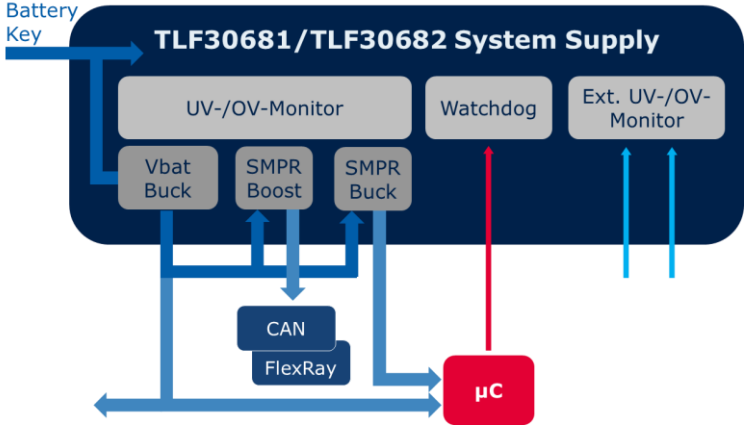
TLF3068x Key Features

- Compatibility: QM- & ISO26262-variants, different currents
- Minimizing size, number and cost of external components: high switching frequency, integrated switches
- High-Efficiency Buck (@ V_{batt}) (3V3 with 3.5A/2.3A-variants)
- Flexible Buck-Post-Regulator (0V9-1V3 with 2A/1A-variants)
- Boost-Post-Regulator (5V with 250mA) for Transceiver
- Integrated Supervisory Features (QM-variants)
  - UV/OV-Monitoring, Flexible Window-Watchdog
- Additional Integrated Safety Features (ISO-variant only)
  - Flexible Functional-Watchdog
  - ERROR-monitoring
  - Safe State Controller with Safety Output
  - BIST
- Small VQFN-48 package (7x7mm²) for Lead Tip Inspection

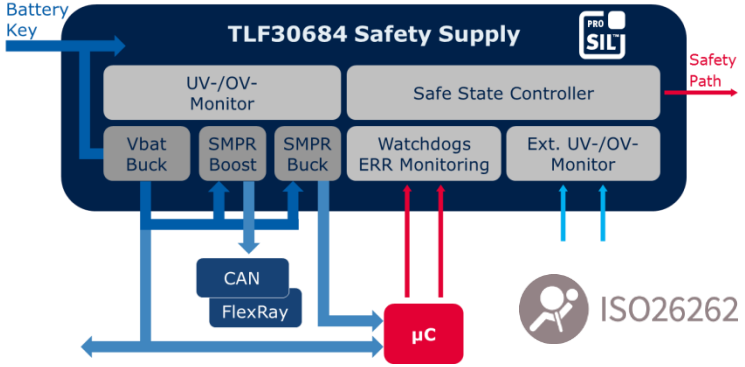
Applications

- 24GHz Radar
- 77/79GHz Radar
- Camera (Multi-Purpose)
- Domain Controller
- Cluster / Center Stack
- Display

QM-variants



ISO26262-variant



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Infineon AURIX Software offering

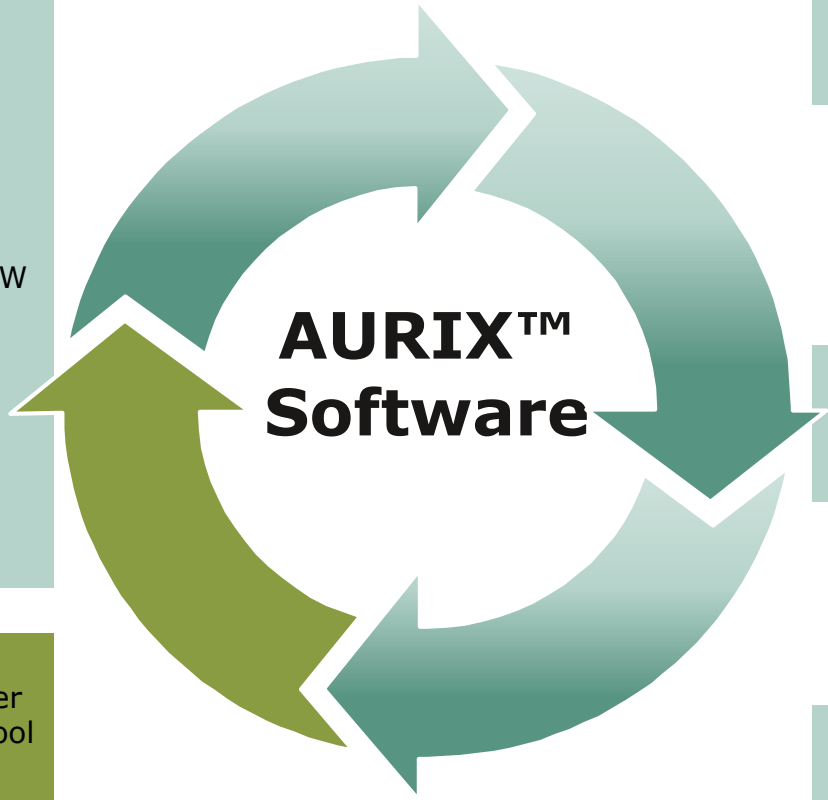
Reduction of customer SW development

Commercial Basic Software

- **AUTOSAR MCAL**:
  - MC-ISAR Basic (Base, MEM, COM Basic)
  - MC-ISAR COM Enhanced
  - MCAL Complex Driver MCD and Demo code
- **Safety driver:** to support HW safety features and external watch dogs

Free tool/ example code

- iLLD: Infineon low level driver
- ACT : AURIX configuration tool
- FreeOSEK
- Free compiler
- Free debugger
- DSP library



Comercial Value Software

- SHE+ security driver:
  - Supporting latest security requirements

Auxiliary Tools and Software

- C Model
- Simulink model (RADAR only)

Software Design Services

- Customer specific driver
- On customer request

MC-ISAR Package Structure
MC-ISAR MicroController – Infineon Software ARchitecture

- MC-ISAR **AURIX** Package Structure
  - MC-ISAR BASE: MCU, WDG, GPT, SPI, PORT, DIO, ICU, PWM, ADC
  - MC-ISAR MEM: FLASH, FEE
  - MC-ISAR COM Basic: CAN, CanTrcv, LIN
  - MC-ISAR COM Enhanced: FlexRay, Ethernet
  - MC-ISAR CD: UART, MSC, DMA, FLSLoader
  - MC-ISAR DEMOCD: HSSL, SENT, I2C, STM, DS-ADC, SMU, IOM for AURIX as demo release/alpha
  - MC-ISAR LIB: BFX, CRC

- MC-ISAR **AURIX TC3xx** Package Structure
  - MC-ISAR BASIC:
    - MCU, WDG, GPT, SPI, PORT, DIO, ICU, PWM, ADC, OCU
    - FLASH, FEE
    - CAN, CanTrcv, LIN
    - BFX, CRC
  - MC-ISAR COM Enhanced: FlexRay, Ethernet
  - MC-ISAR CD: UART, MSC, DMA, FLS Loader
  - MC-ISAR DEMOCD: HSSL, SENT, SMU, further tbd

} Combined into „BASIC“ package

Free TriCore™ Entry Tool Chain

Provider Hightec

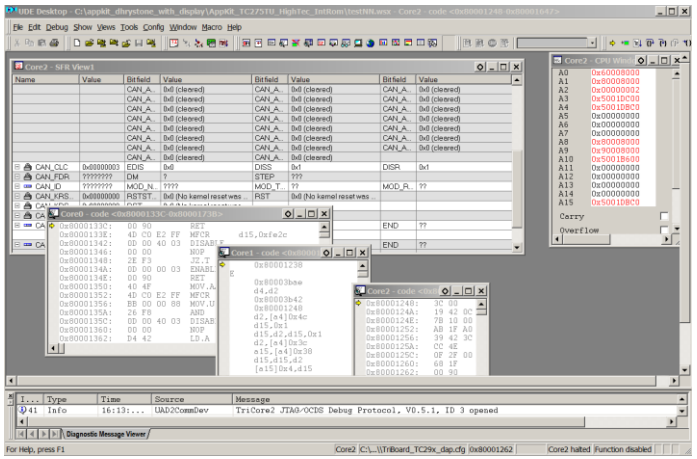
This **free of charge** tooling package provides all requiered features to develop and test software for TriCore™ and AURIX™ .

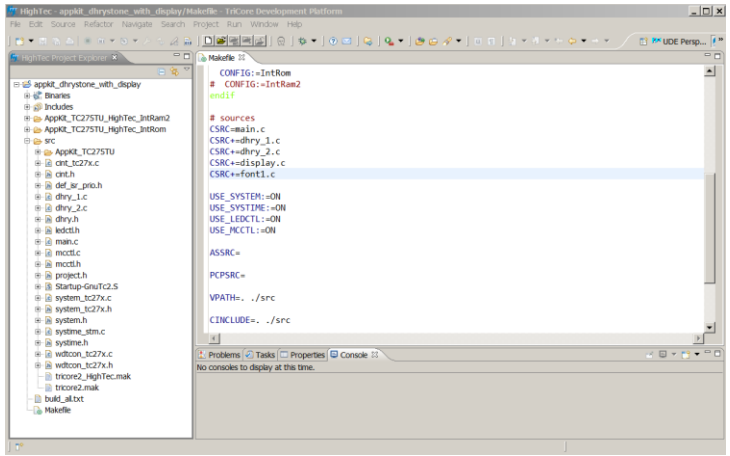
The tool can be used with all available TriCore™ and AURIX™ StarterKits and Application Boards

- Eclipse based IDE
- Project wizzard to easy define the project properties for device and board support
- High performand GNU C compiler
- Integrated source level debugger
- On-chip Flash programming support

Free of charge AURIX2G in development

http://free-entry-toolchain.hightec-rt.com





Free AURIX Configuration
Provider Altium

Free of charge
AURIX2G in development

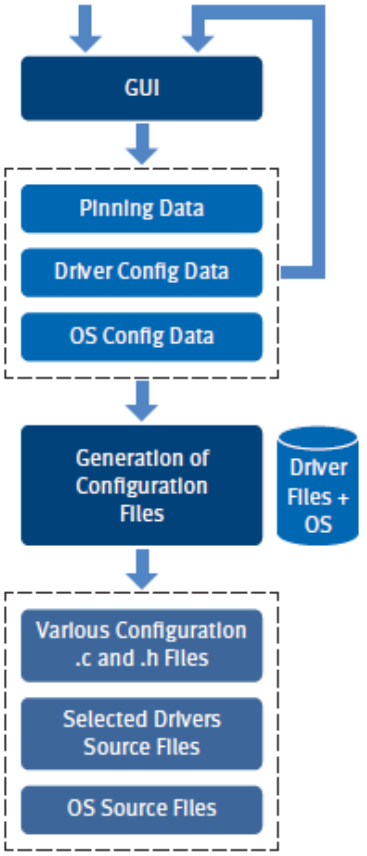
ACT – AURIX Configuration Tool

ACT is a powerful tool that helps engineers to jump start programming of Infineon AURIX microcontrollers

Key Features

- Altium TASKING VX TriCore Lite version including build in
  - AURIX Pin Mapping incl interactive package view
  - AURIX iLLD [Low Level Driver]
  - AURIX OSEK
  - Entry level Compiler and Debugger

http://forms.tasking.com/tricore.html

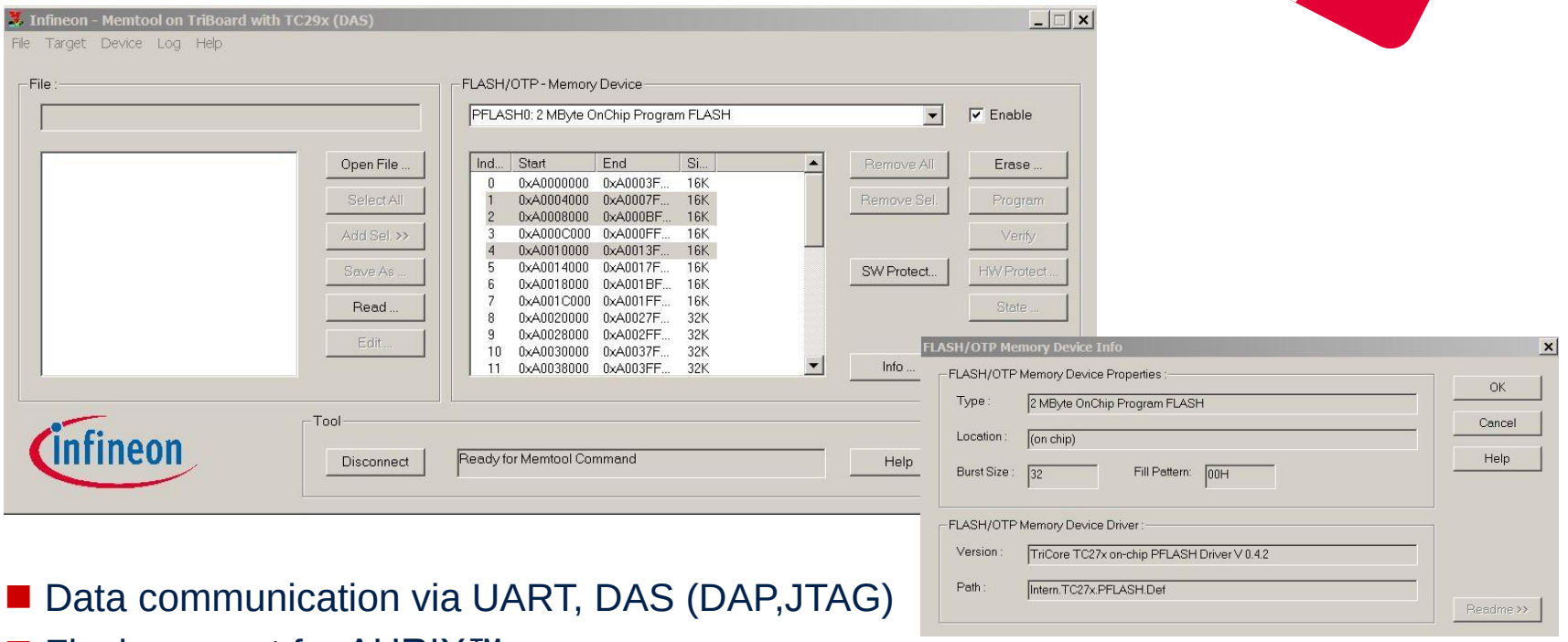


Free AURIX Configuration

Free Flash Loader: Infineon MemTool

Free of charge AURIX2G in development

Infineon provides free Flash Loader SW that supports various interfaces

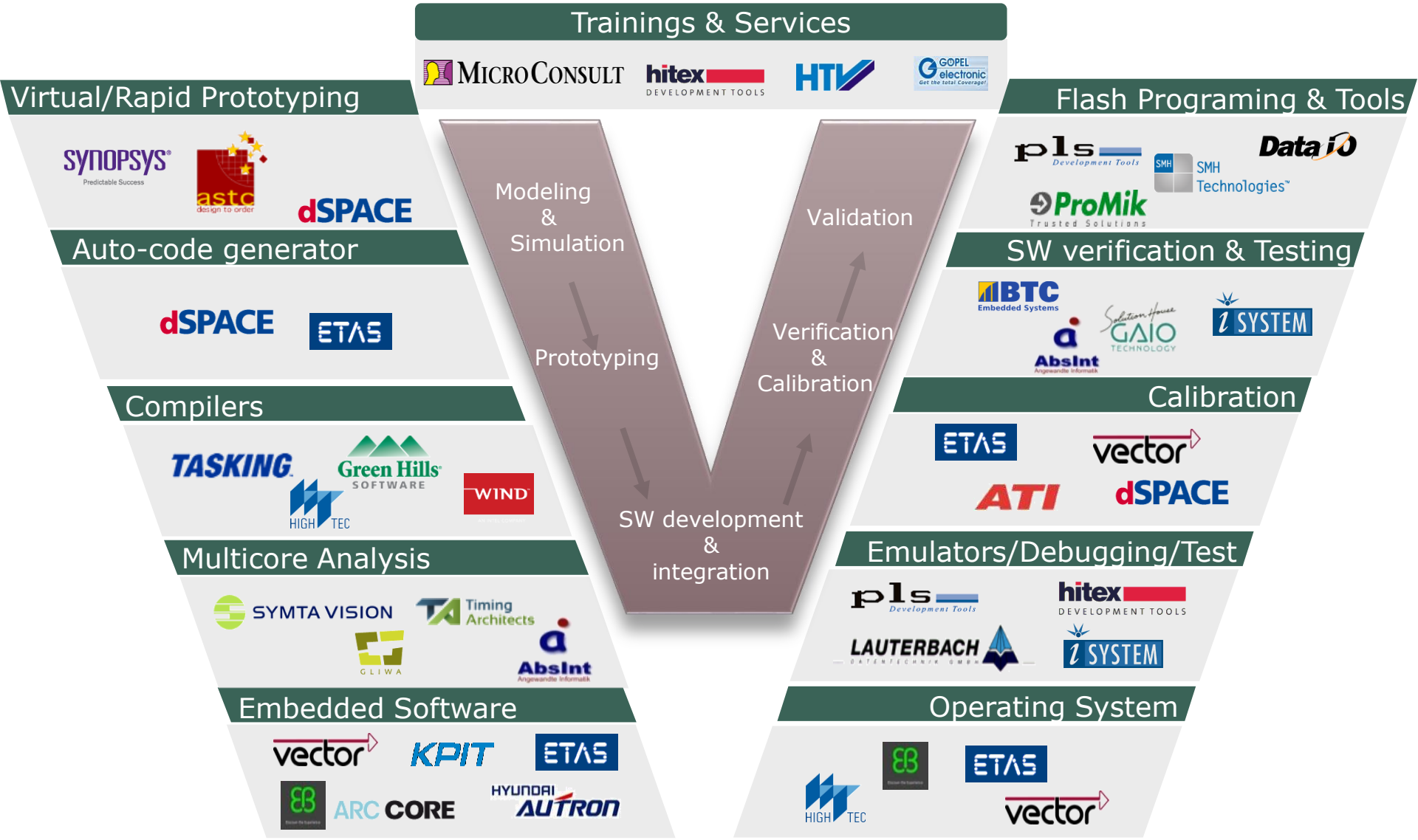


- Data communication via UART, DAS (DAP,JTAG)
- Flash support for AURIX™,
- Batch-Mode functionality
- Automatic COM port detection
- On-chip Flash protection features supported

DOWNLOAD

www.infineon.com/memtool

AURIX Tool Ecosystem will be further improved and Access made easier for customers



Part of your life. Part of tomorrow.

Infineon