AURIX 2G AD Converter Overview

Hansen Chen
IFCN ATV SMD GC SAE MC
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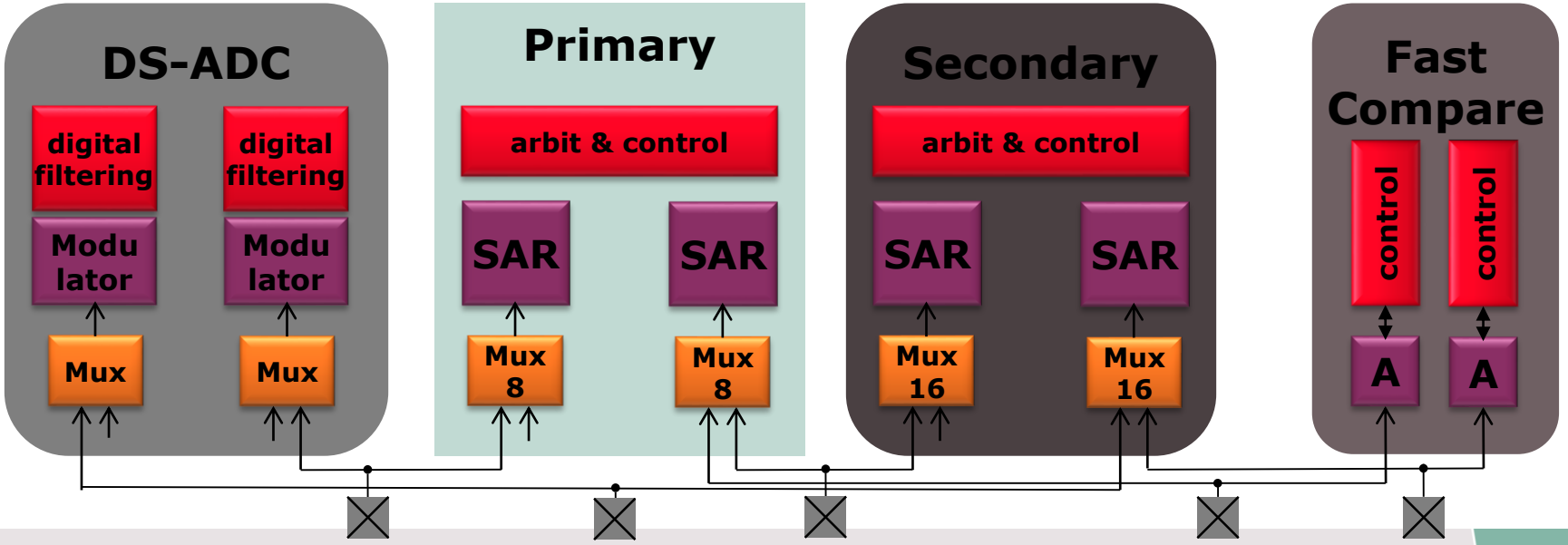
AD Converters in AURIX™ - TC3xx Overview

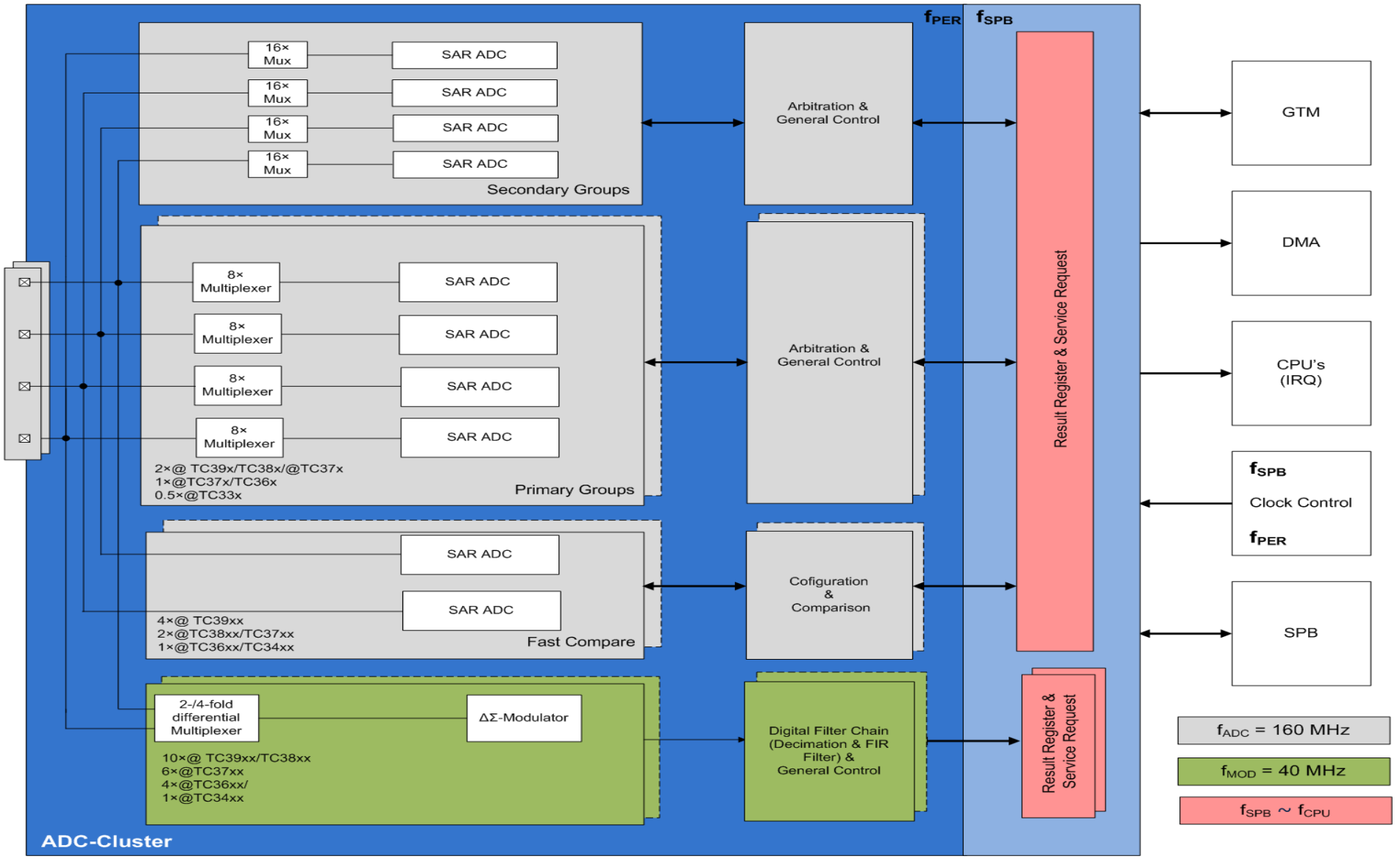
- Four ADC types:
  - **Primary SAR**: 12 bit, ≤ 2.5Msamples/s
  - **Secondary SAR**: 12 bit, ≤ 1.4Msamples/s
  - **Fast Compare**: 10 bit, ≤ 5Msamples/s
  - **DS-ADC**: 13 ENOB, ≤ 200Ksamples/s
- Two ADCs on every analog input
  improved equidistant and parallel sampling:
  - primary and secondary
  - primary & delta sigma or fast compare
  - secondary & delta sigma or fast compare

ADC Improvements in AURIX™ - TC3xx

- SAR ADCs: Reduced capacitive load on SARs' analog inputs 0.3 / 3 pF (with / without buffer option)
- DS-ADC:
  - 50% less power consumption (versus AURIX)
  - automatic gain and offset calibration (no CPU load)
  - improved analog input impedance: 850KΩ (was 100KΩ for Gain=1)
  - increased pass-band frequency range (724Hz – 100KHz)



ADC Cluster Architecture

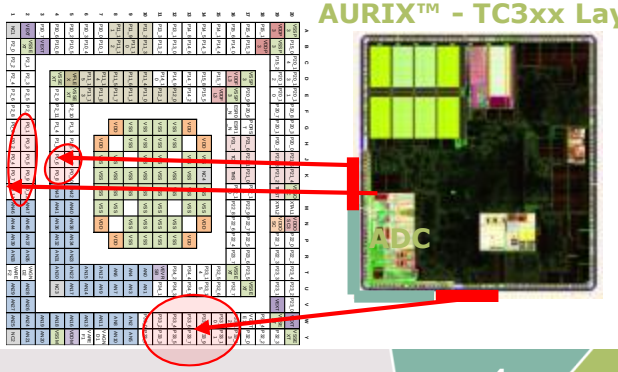


AURIX™ - TC3xx

EVADC/EDSADC – Device Overview and Package Pin Count

	TC39x (16MB)	TC38x (10MB)	TC37x (6MB)	TC36x (4MB)	TC33x (2MB)
Total # of independent Sampling Stages	12	12	8	6	4
Secondary ADC	4×SAR	4×SAR	4×SAR	2×SAR	2×SAR
Primary -ADC sub cluster	8×SAR	8×SAR	4×SAR	4×SAR	2×SAR
# of Fast Compare sub channels	8ch	4ch	2ch	2ch	0ch
# of DSADC	14	10	6	4	0
# of analog inputs (AURIX Comparison) In Package Variant	74+28 (=102) (84) BGA516	72+28 (=100) (84) BGA516	48+28 (=76) (60) BGA292	48+12 (=60) (48) QFP176	24+10 (=34) (24) QFP144

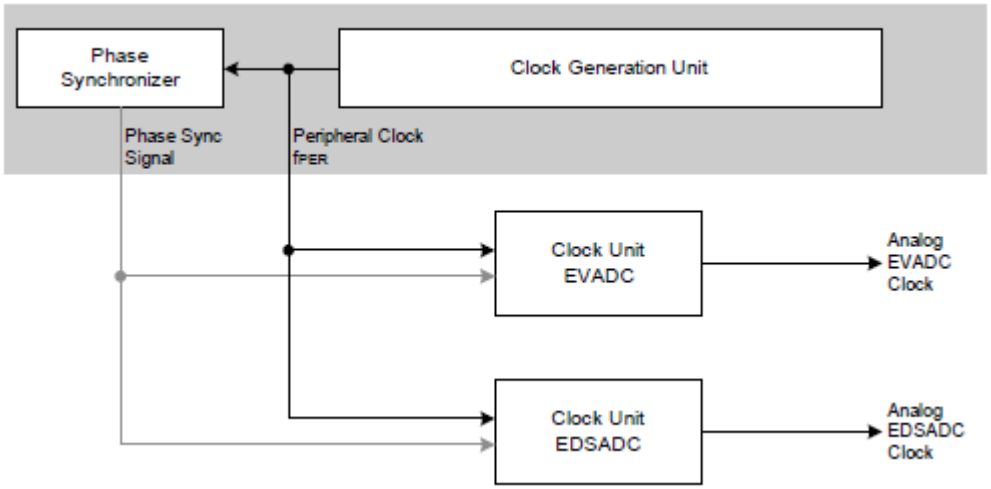
Preliminary
Subject to Change



- Highlights:
  - up to 16 additional overlaid GPIO and analog Pins
    - note that TUE ≤ ±4LSB for GPIO overlaid will increase by ±3LSB
  - leakage for non-overlaid GPIO with max 2 connected Primary/Secondary/fast Compare/DSADC ≤ ±150nA
    - overlaid GPIO leakage strongly dependent on driver class for slow GPIO (e.g.LP) expectation: ±250nA (Tj=150) → ±400nA

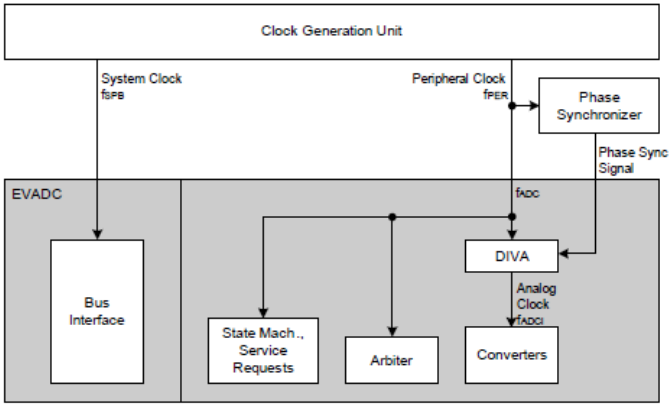
Clock Concept of ADC Cluster: Introducing of Converter Control Module

- Clock and synchronization concept of ADC cluster

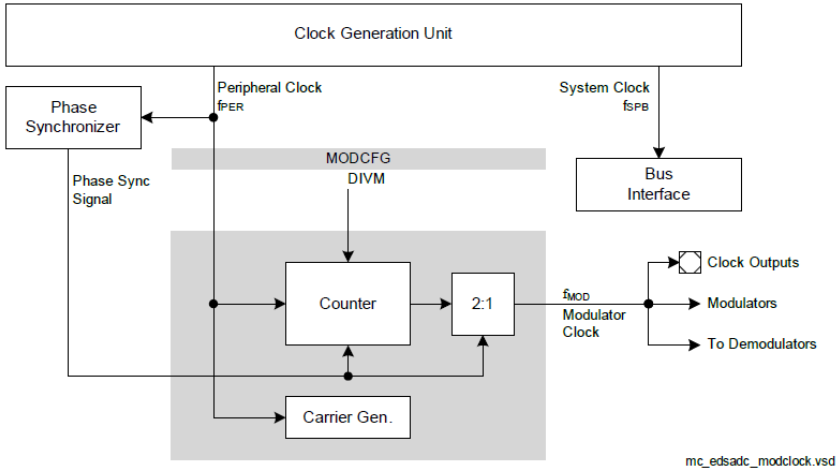


- Synchronization of the different ADC instances will minimize supply, ground and reference related crosstalk
- Phase synchronizer generates a clock enable signal for every ADC instance
- Synchronization signal is derived from the peripheral clock f_{PER} and can be divided by 2/4/6/…/16
- Deterministic phase shift between the ADCs can be configured individually
- Synchronization can be disabled by configuration bit as well

- Clock and synchronization concept of VADC



- Clock and synchronization concept of DS-ADC



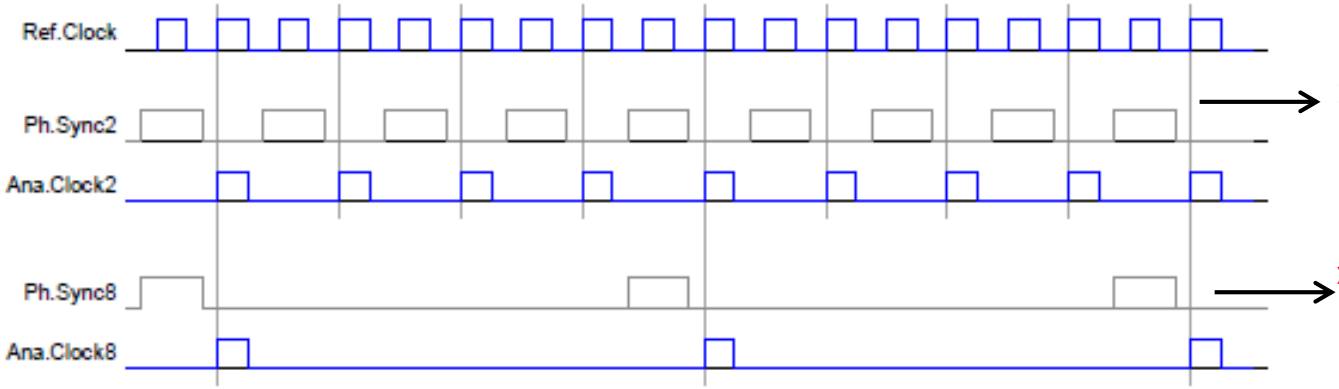
Proposed Converter Clock Configurations

- The frequency (f_{sync}) of the synchronization signal has to be equivalent to the frequency of the DS-modulator (f_{mod})
- The clock of the DS-modulator requires 50% duty cycle
  - Generally DS-modulator frequencies (f_{mod}) of 160MHz/2·n are possible
- The analog clock frequency (f_{ADCI}) of the VADC has to equal or 2·n higher as the DS-modulator frequency (f_{mod})

f_{sync}	f_{mod}	f_{ADCI}
16 MHz (160 MHz/10)	16 MHz (160MHz/10)	16 MHz or 32 MHz (160 MHz/10) or (160 MHz/5)
20 MHz (160 MHz/8)	20 MHz (160 MHz/8)	20 MHz or 40 MHz (160 MHz/8) or (160 MHz/4)
26.67 MHz (160 MHz/6)	26.67 MHz (160 MHz/6)	26.67 MHz or 53.33 MHz (160 MHz/6) or (160 MHz/3)
40 MHz (160 MHz/4)	40 MHz (160 MHz/4)	40 MHz (160 MHz/4)

Converter Synchronization Concept

› Phase Synchronizer Signal



› Phase Sync with 160MHz/2

› Phase Sync with 160MHz/8

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