# AURIX 2G Generic Timer Module(GTM)

Allen
IFCN ATV SMD GC SAE MC
2018/5/2

# Agenda

1. GTM Overview
2. CTBM-Clock & Time Base Management
3. TIM-Timer Input Module
4. ARU-Advanced Routing Unit
5. TOM-Timer Output Module
6. ATOM-ARU connected Timer Output Module
7. DTM-Dead Time Module

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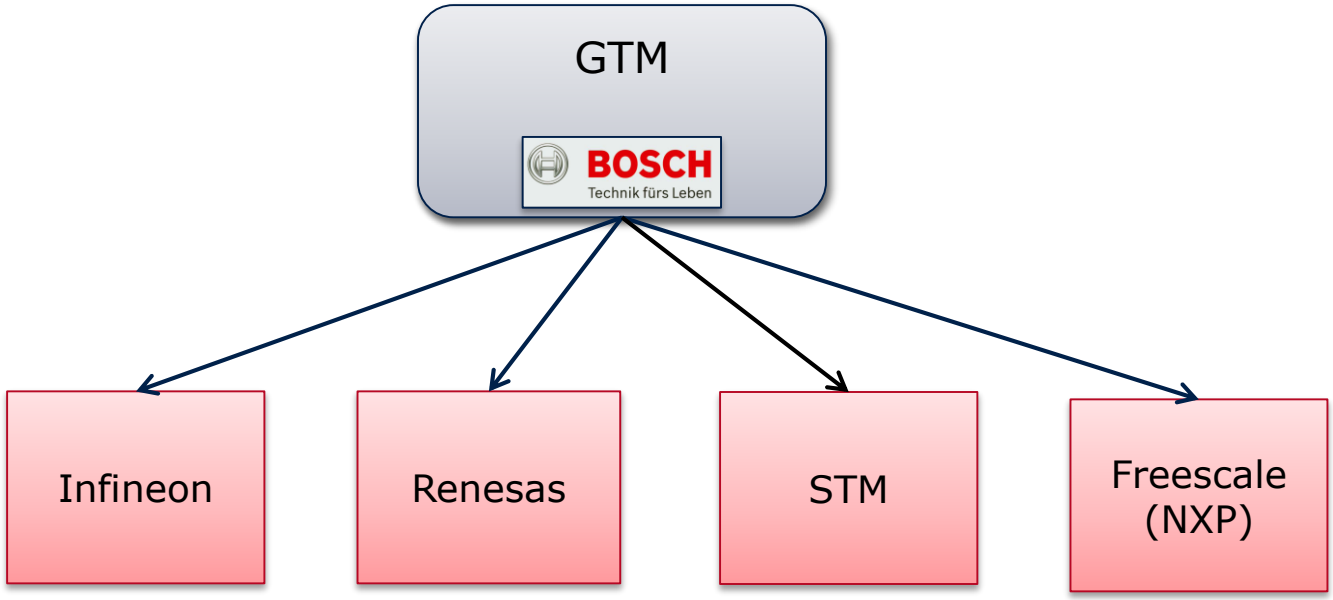
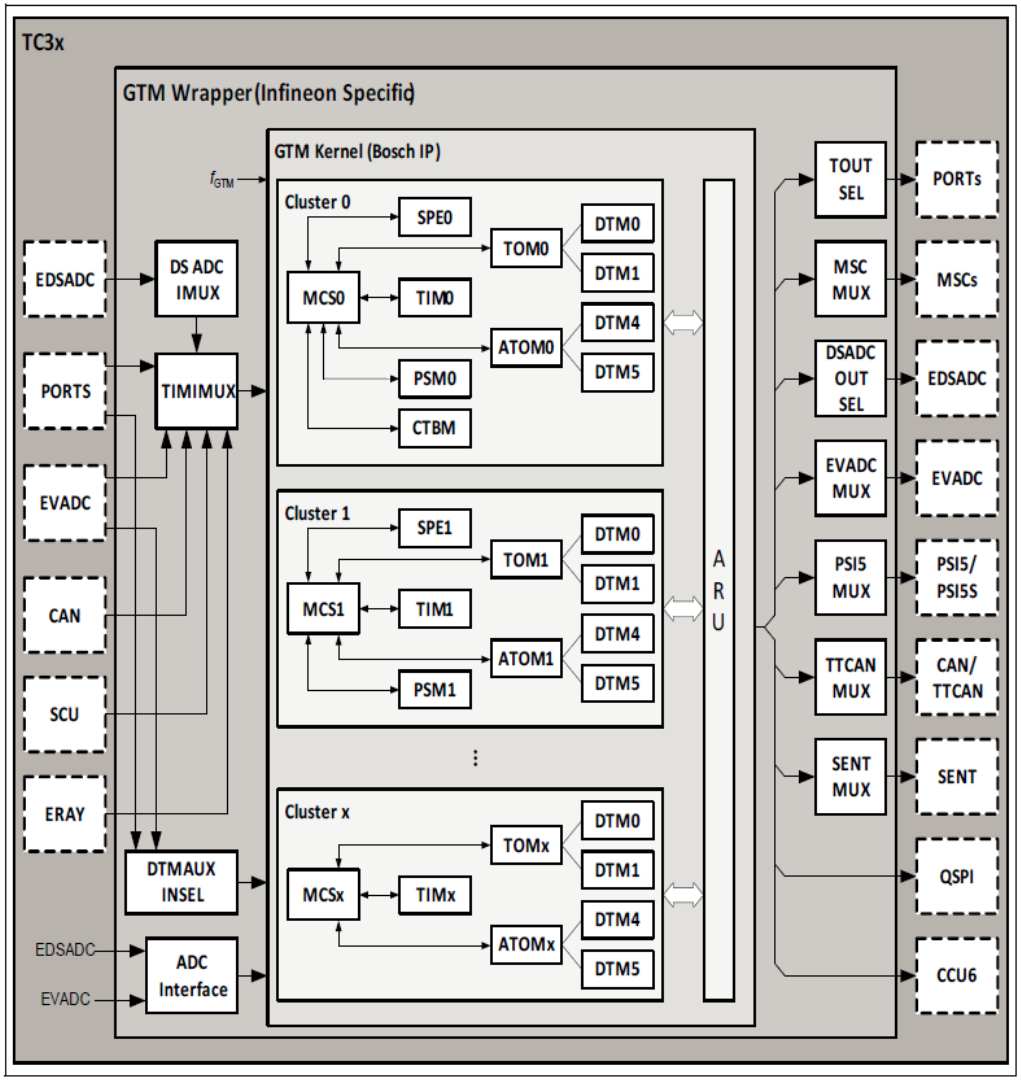
# Generic Timer Module (GTM) from Bosch Standardization




**Customers**

- Unload CPU from critical Tasks
- Simplify Software interface
- Faster Development
- One SW for all Controllers

# AURIX/GTM and GTM Wrapper

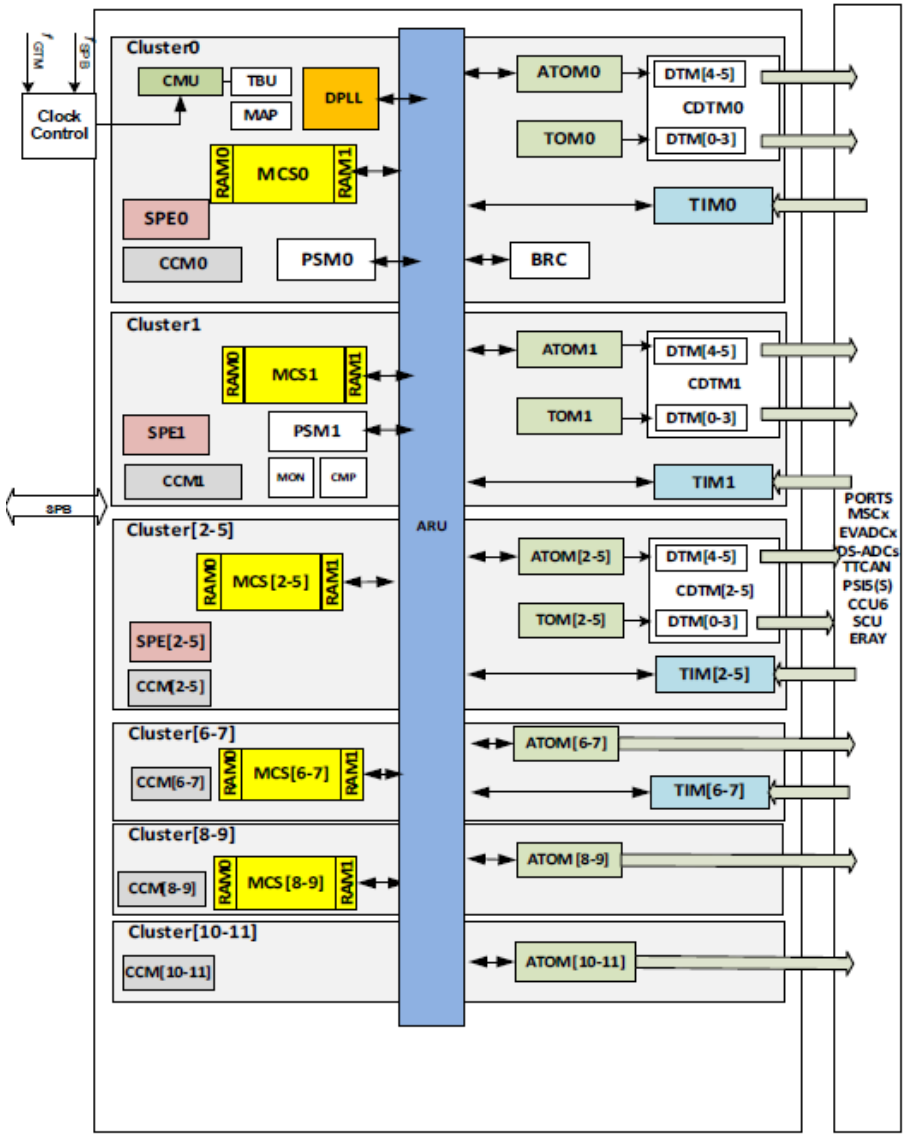



- GTM Implementation (GTM Wrapper) is Infineon Specific
- Control Registers to configure Muxes

Table 1-90 Register Overview - GTM Control Register (continued)s

| Short Name | Description | Offset Addr. | Access Mode | | Reset | Description See |
|---|---|---|---|---|---|---|
| | | | Read | Write | | |
| ACCEN0 | Access Enable Register 0 | 9FE44$_H$ | U, SV | SV, SE | Application | Page 771 |
| OTBU0T | OCDS TBU0 Trigger Register | 9FE14$_H$ | U, SV | SV, P | Debug | Page 973 |
| OTBU1T | OCDS TBU1 Trigger Register | 9FE18$_H$ | U, SV | SV, P | Debug | Page 973 |
| OTBU2T | OCDS TBU2 Trigger Register | 9FE1C$_H$ | U, SV | SV, P | Debug | Page 974 |
| OTBU3T | OCDS TBU3 Trigger Register | 9FFA8$_H$ | U, SV | SV, P | Debug | Page 974 |
| OTSS | OCDS Trigger Set Select Register | 9FE20$_H$ | U, SV | SV, P | Debug | Page 969 |
| OTSC0 | OCDS Trigger Set Control 0 Register | 9FE24$_H$ | U, SV | SV, P | Debug | Page 970 |
| OTSC1 | OCDS Trigger Set Control 1 Register | 9FE28$_H$ | U, SV | SV, P | Debug | Page 971 |
| ODA | OCDS Debug Access Register | 9FE2C$_H$ | U, SV | SV, P | Debug | Page 972 |
| OCS | OCDS Control and Status Register | 9FE30$_H$ | U, SV | SV, P | Debug | Page 770 |
| TIM0INSEL | TIM0 Input Select Register | 9FD10$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TIM1INSEL | TIM1 Input Select Register | 9FD14$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TIM2INSEL | TIM2 Input Select Register | 9FD18$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TIM3INSEL | TIM3 Input Select Register | 9FD1C$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TIM4INSEL | TIM4Input Select Register | 9FD20$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TIM5INSEL | TIM5 Input Select Register | 9FD24$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TIM6INSEL | TIM6 Input Select Register | 9FD28$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TIM7INSEL | TIM7 Input Select Register | 9FD2C$_H$ | U, SV | U, SV, P | Application | Page 813 |
| TOUTSEL0 | Timer Output Select 0 Register | 9FD30$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL1 | Timer Output Select 1 Register | 9FD34$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL2 | Timer Output Select 2 Register | 9FD38$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL3 | Timer Output Select 3 Register | 9FD3C$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL4 | Timer Output Select 4 Register | 9FD40$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL5 | Timer Output Select 5 Register | 9FD44$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL6 | Timer Output Select 6 Register | 9FD48$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL7 | Timer Output Select 7 Register | 9FD4C$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL8 | Timer Output Select 8 Register | 9FD50$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL9 | Timer Output Select 9 Register | 9FD54$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL10 | Timer Output Select 10 Register | 9FD58$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL11 | Timer Output Select 11 Register | 9FD5C$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL12 | Timer Output Select 12 Register | 9FD60$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL13 | Timer Output Select 13 Register | 9FD64$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL14 | Timer Output Select 14 Register | 9FD68$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL15 | Timer Output Select 15 Register | 9FD6C$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL16 | Timer Output Select 16 Register | 9FD70$_H$ | U, SV | U, SV, P | Application | Page 797 |
| TOUTSEL17 | Timer Output Select 17 Register | 9FD74$_H$ | U, SV | U, SV, P | Application | Page 797 |

# GTM (Generic Timer Module)
# AURIX2G - GTM V3.1.x




- GTM is logically divided in Clusters
- The first 5 clusters (0-4), can work up to 200MHz
- The DTM numbering is changed. They are grouped in CDTMx modules (Cluster Dead Time)
- New CCMx Modules (Cluster Configuration)
  - Cluster Clock Frequency
  - Module Clock Gating
  - MCS bus master observation
  - Address Range Protection
  - .....

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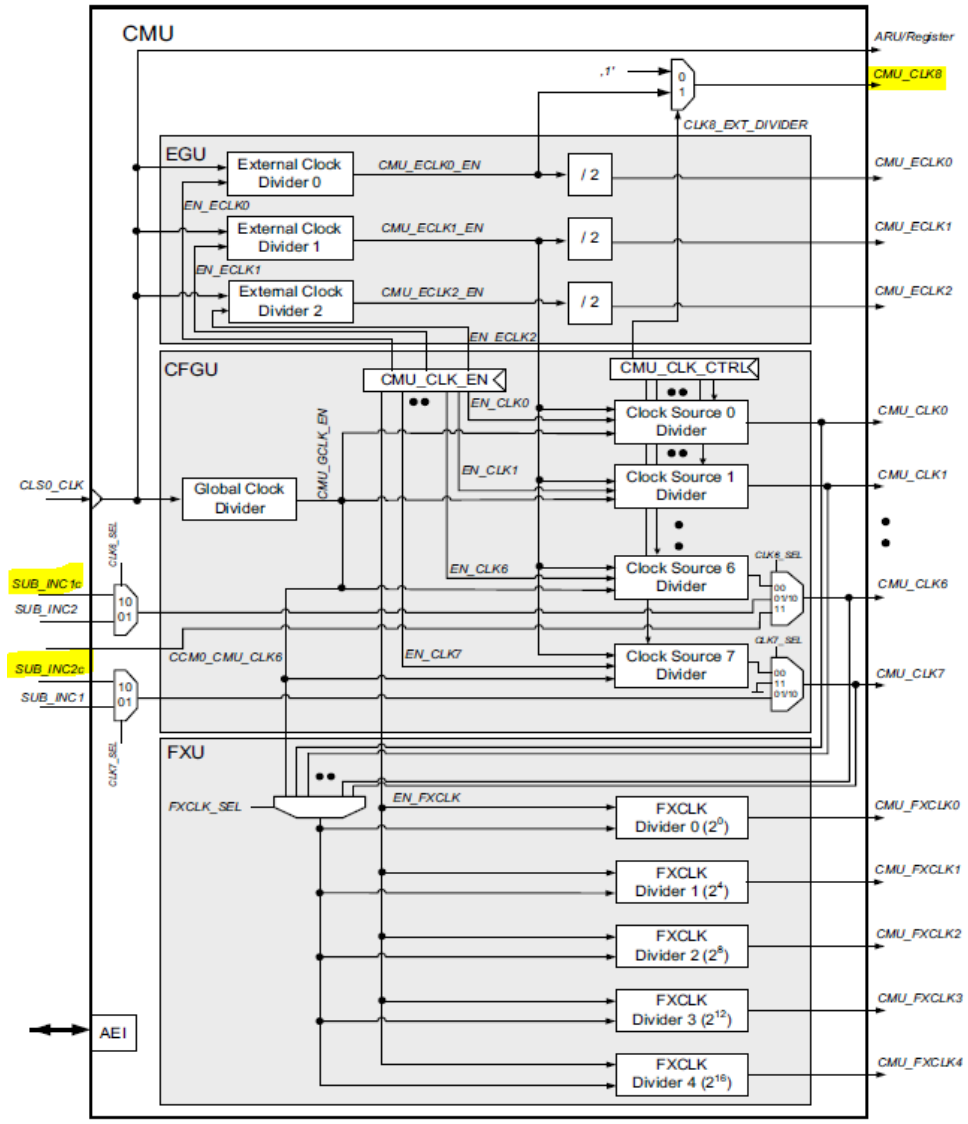
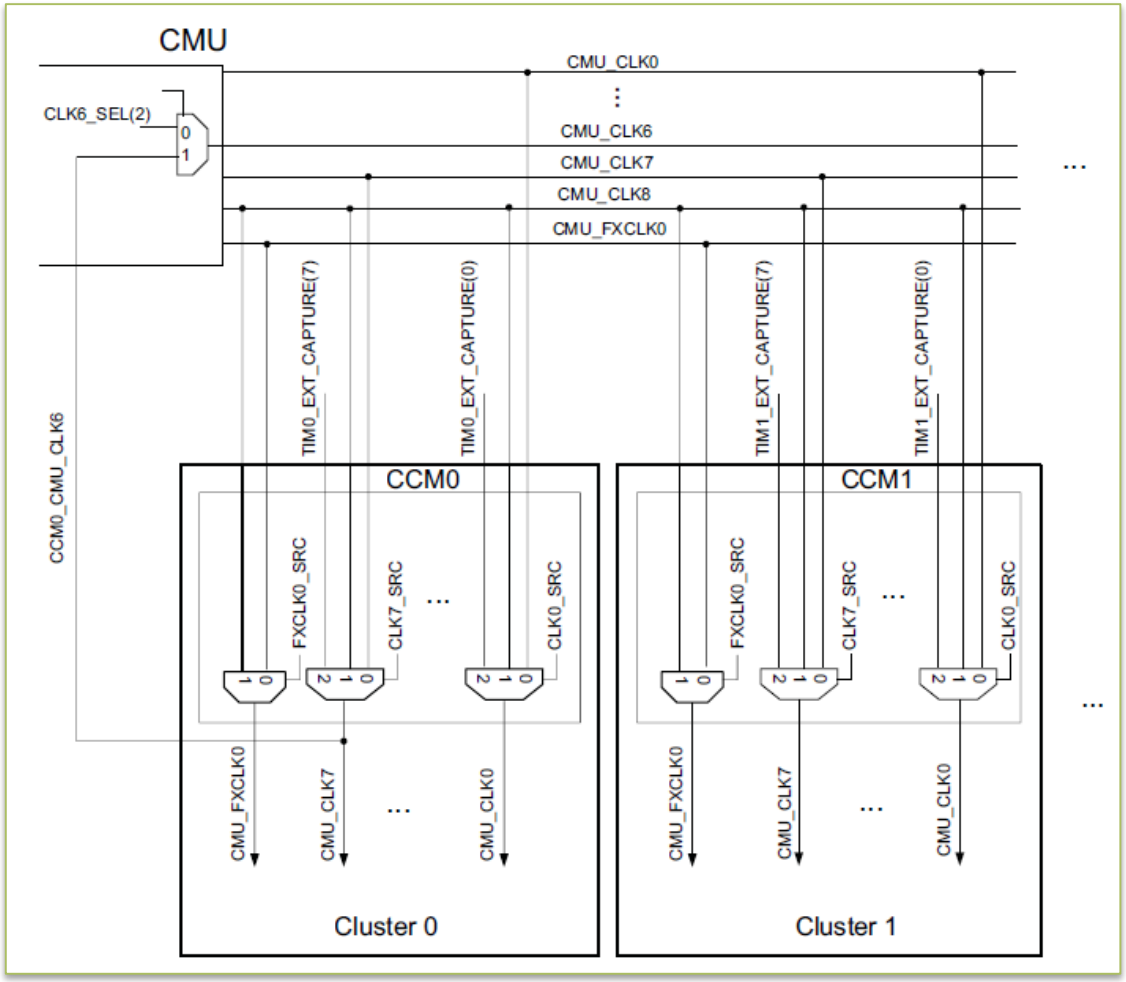
# AURIX2G CTBM




- Input frequency **200MHz**
- Sub_inc1/2**c** (from DPLL) can be used as clock
- CMU_CLK8 is new(for clusters' clock)

# AURIX2G
# CCM – Cluster Configuration Module




- cluster's clock frequency
- module clock gating
- Status observation of the cluster's MCS bus master (AEM),
- address range protection (**MCS**)
- global architecture configuration

# AURIX2G
# CCM – Cluster Configuration Module

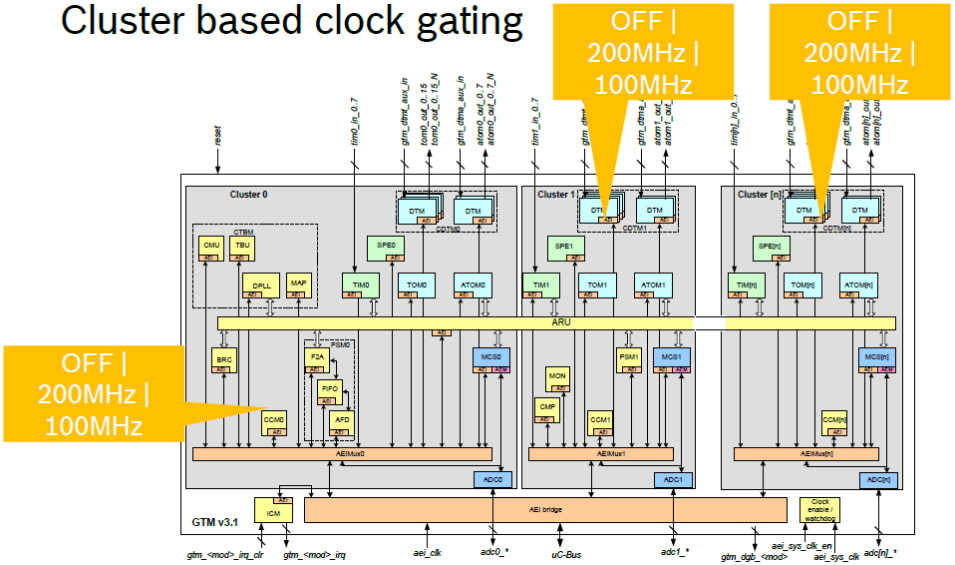
## Dynamic Power reduction

- Cluster based clock gating
- Sub module based clock gating

Introduce new sub module: cluster configuration module CCM

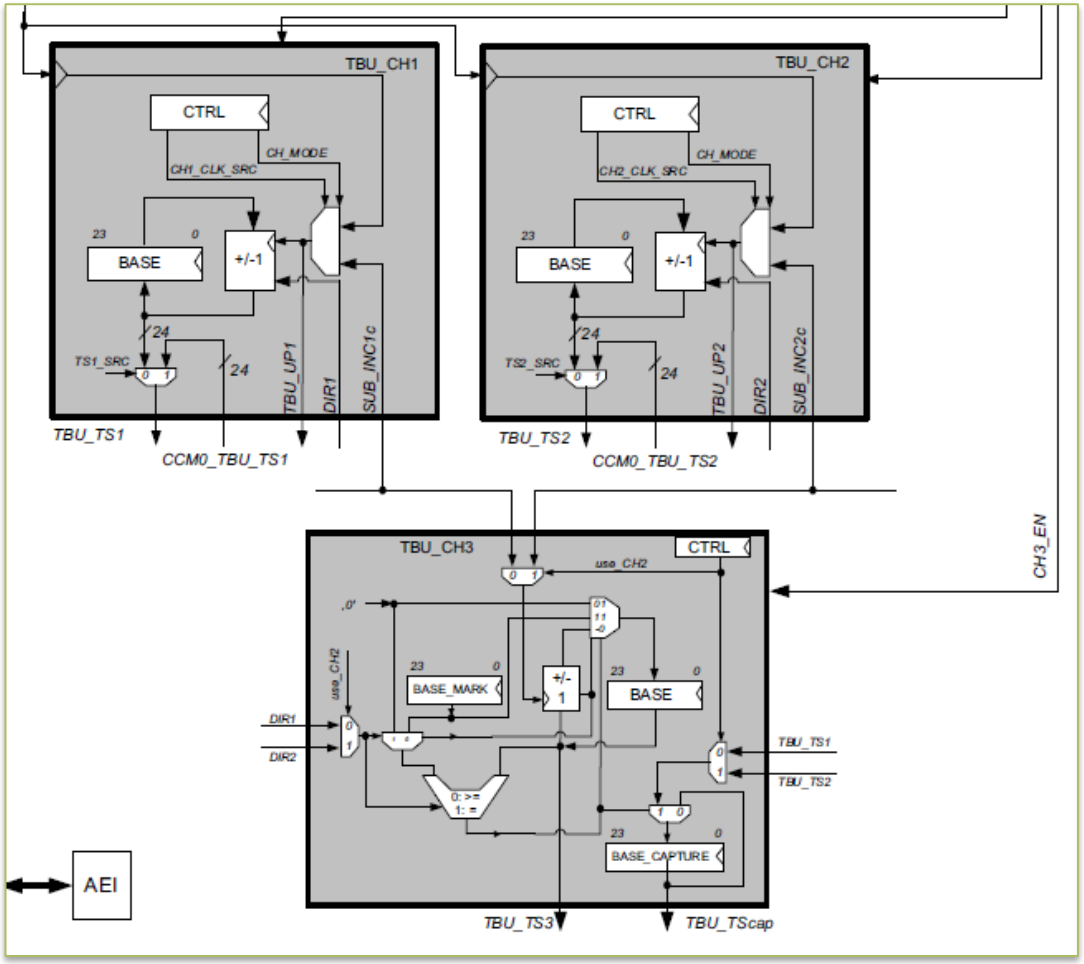
- Introduce control register to disable clock for each sub module
  - Cluster0-n: 1 bit for each TIM, TOM+SPE, ATOM, MCS
  - Cluster0: 1 bit DPLL+MAP , 1 bit BRC
  - Cluster0-n: 1 bit FIFO
  - Cluster1: 1 bit for CMP+MON
- Enabled after reset to ensure compatibility to V1 GTM_IP

Cluster based clock gating

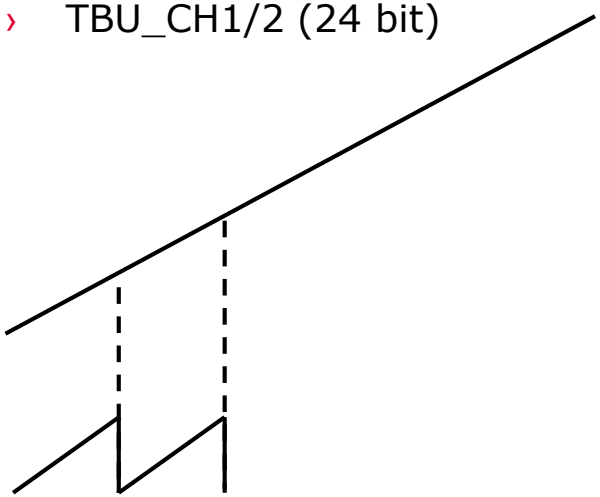



| Register name | Description |
|---|---|
| CCM[i]_PROT | CCMi Protection Register |
| CCM[i]_CFG | CCMi Configuration Register |
| CCM[i]_CMU_CLK_CFG | CCMi CMU Clock Configuration Register |
| CCM[i]_CMU_FXCLK_CFG | CCMi CMU Fixed Clock Configuration Register |
| CCM[i]_AEIM_STA | CCMi MCS Bus Master Status Register |
| CCM[i]_ARP[z]_CTRL | CCMi Address Range Protector z Control Register |
| CCM[i]_ARP[z]_PROT | CCMi Address Range Protector z Protection Register |
| CCM[i]_HW_CONF | CCMi Hardware Configuration Register |
| CCM[i]_TIM_AUX_IN_SRC | CCMi TIM AUX input source Register. |
| CCM[i]_EXT_CAP_EN | CCMi External Capture Enable Register. |
| CCM[i]_TOM_OUT | CCMi TOM Output Register. |
| CCM[i]_ATOM_OUT | CCMi ATOM Output Register. |

# AURIX2G
# TBU_CH3



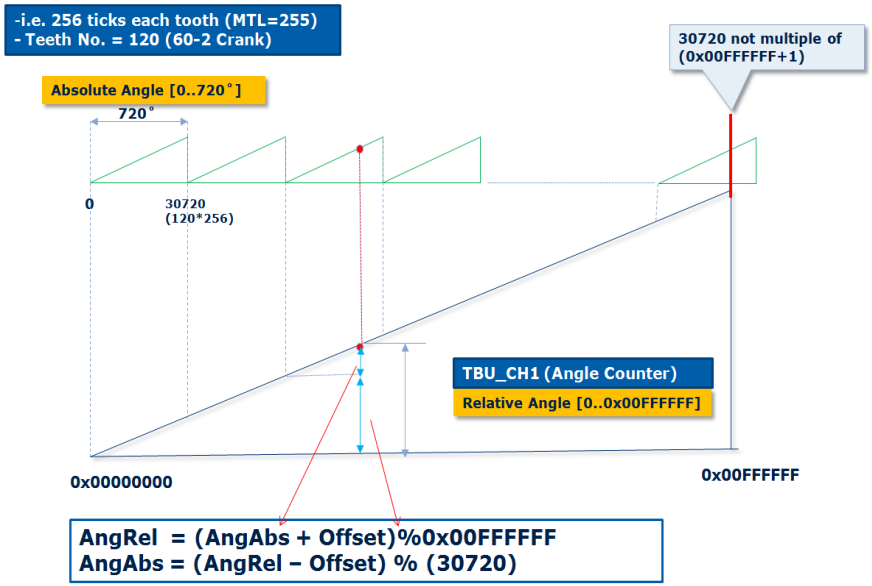

- New TBU3 Counter, (Modulo Counter Mode)
  - TBU_CH1/2 (24 bit)



  - TBU_CH3 (24 bit)

# AURIX2G
# TBU_CH3 Benefits (i.e. Engine Management)

- **AURIX 1G**
- To manage Absolute Vs Relative Angle conversion, the SW (CPU or MCS) needs to store the TBU_CH1 value after every 720 degrees (Offset).




- **AURIX 2G**
- Using the TBU_CH3, the HW stores automatically to TBU_CH1 value (offset) needed for the conversion
- Abs2Rel =>
  - AngRel = (TBU_CH3_BASE_CAPTURE+TBU_CH3_BASE)&0x00FFFFFF
- Rel2Abs =>
  - AngAbs = (AngRel-TBU_CH3_BASE_CAPTURE)%(TBU_CH3_BASE_MARK)

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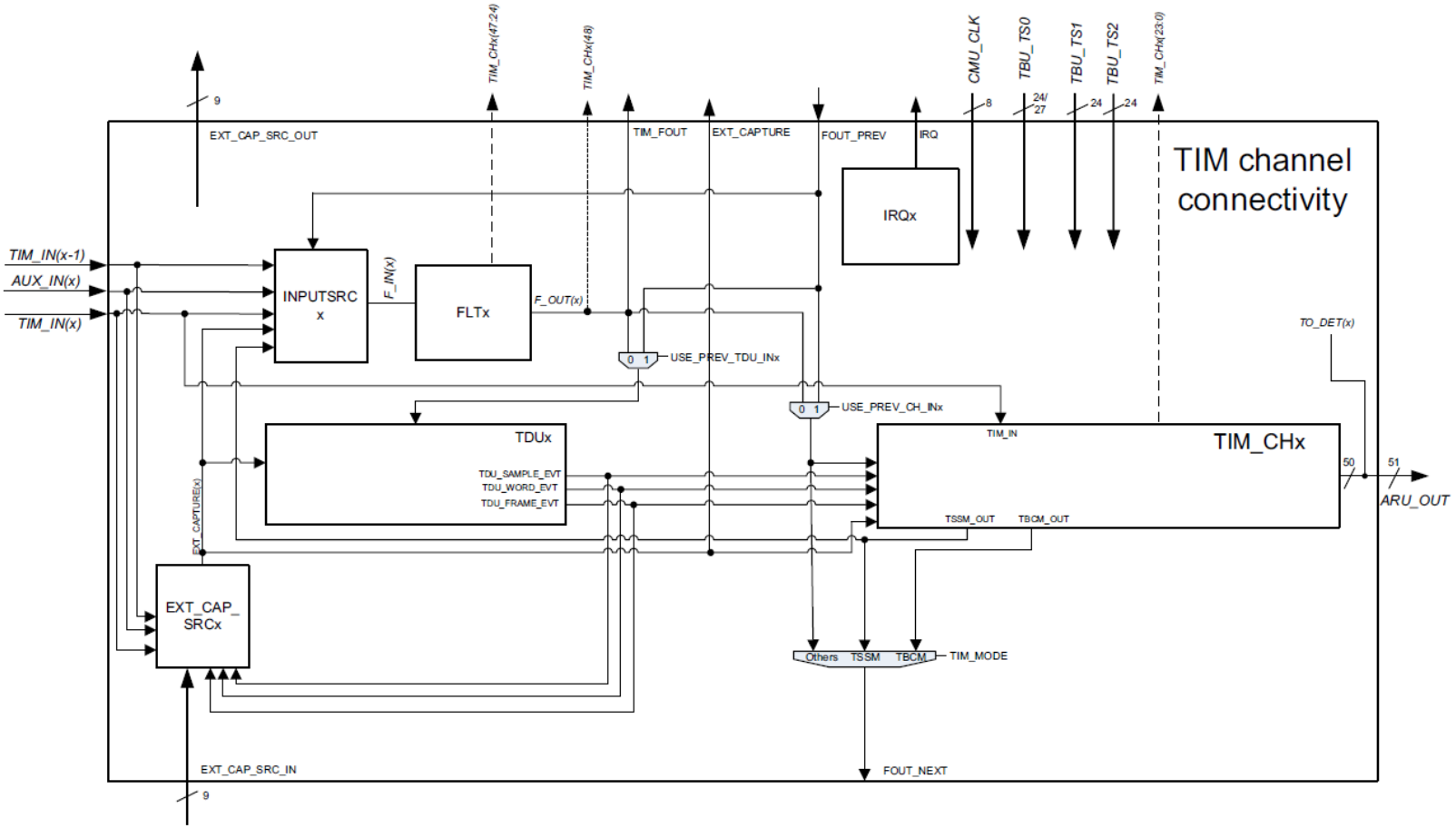
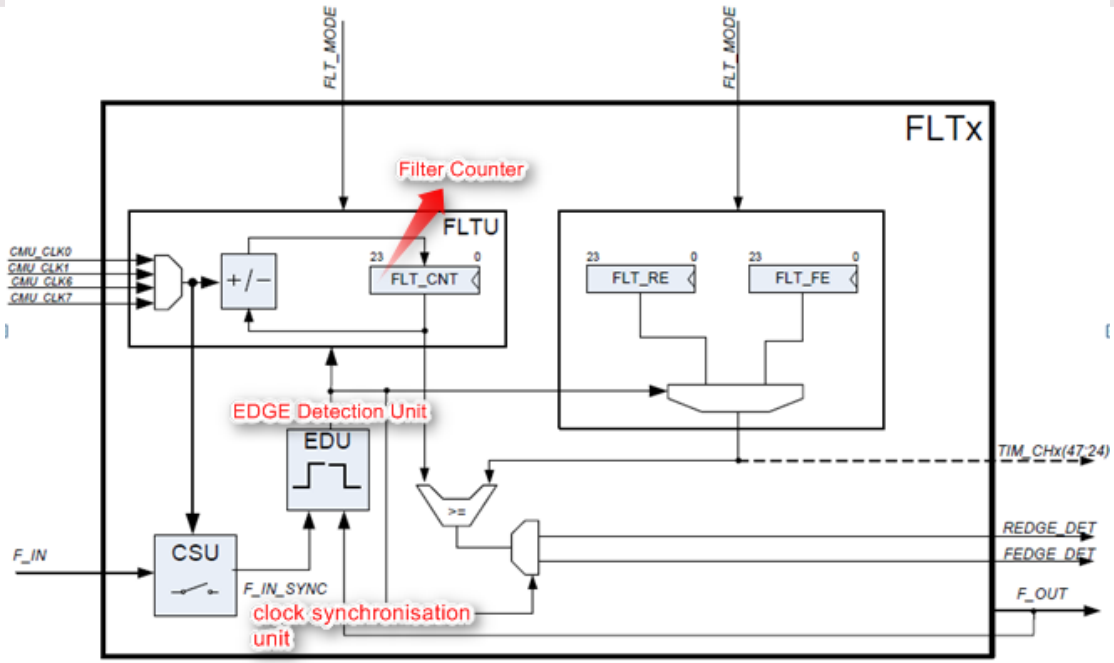
# GTM Architecture Overview
# TIM – Timer Input Module

- TIM is intended **for filtering and capturing** of input signals.
- For **Advanced data processing** the detected input characteristics can be routed through the ARU to GTM processing units (MCS)
- Input characteristics:
  - Time stamp values of detected Edges (RE,FE…)
  - Signal Level
  - Number of Edges received since enabling
  - PWM period and duty measurements
- 7 different operative modes
  - TIM PWM Measurement Mode (**TPWM**)
  - TIM Pulse Integration Mode (**TPIM**)
  - TIM Input Event Mode (**TIEM**)
  - TIM Input Prescaler Mode (**TIPM**)
  - TIM Bit Compression Mode (**TBCM**)
  - TIM Gated Periodic Sampling Mode (**TGPS**)
  - TIM Serial Shift Mode (**TSSM**)

# GTM (Generic Timer Module)
# TIM – Timer Input Module



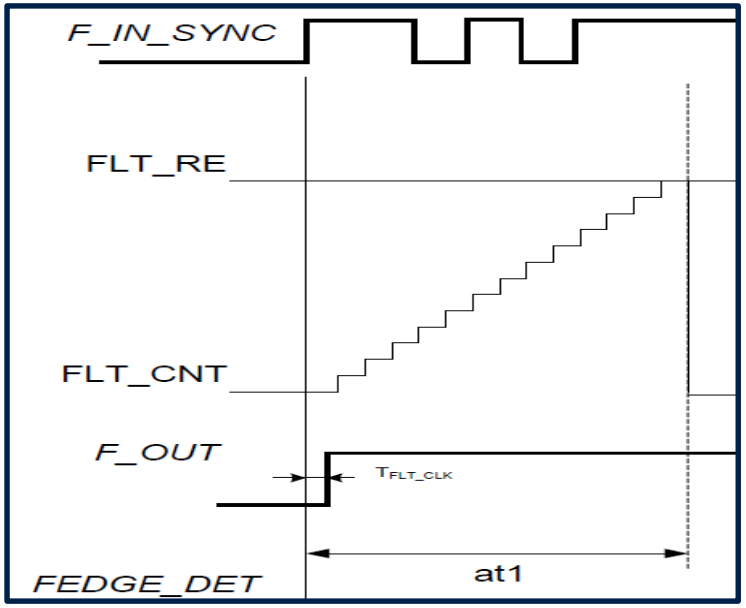
# GTM (Generic Timer Module)
# TIM - FLTx – Filter-Subunit



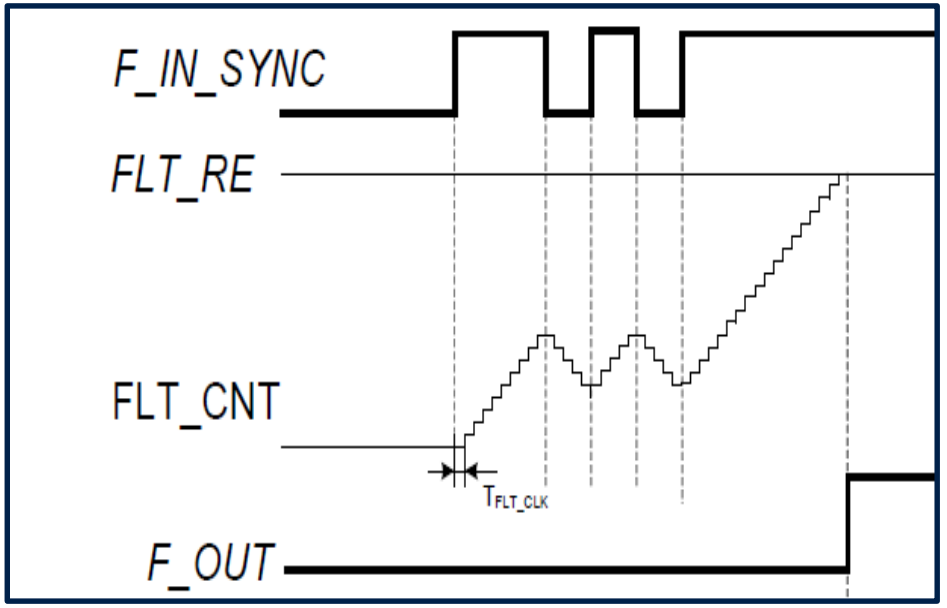

| Filter mode | Meaning of FLT_RE | Meaning of FLT_FE |
|---|---|---|
| Immediate edge propagation | Acceptance time for rising edge | Acceptance time for falling edge |
| Individual de-glitch time (up/down counter) | De-glitch time for rising edge | De-glitch time for falling edge |
| Individual de-glitch time (hold counter) | De-glitch time for rising edge | De-glitch time for falling edge |

# GTM (Generic Timer Module)
# TIM - FLTx – Filter-Subunit

## Immediate Edge Propagation Mode

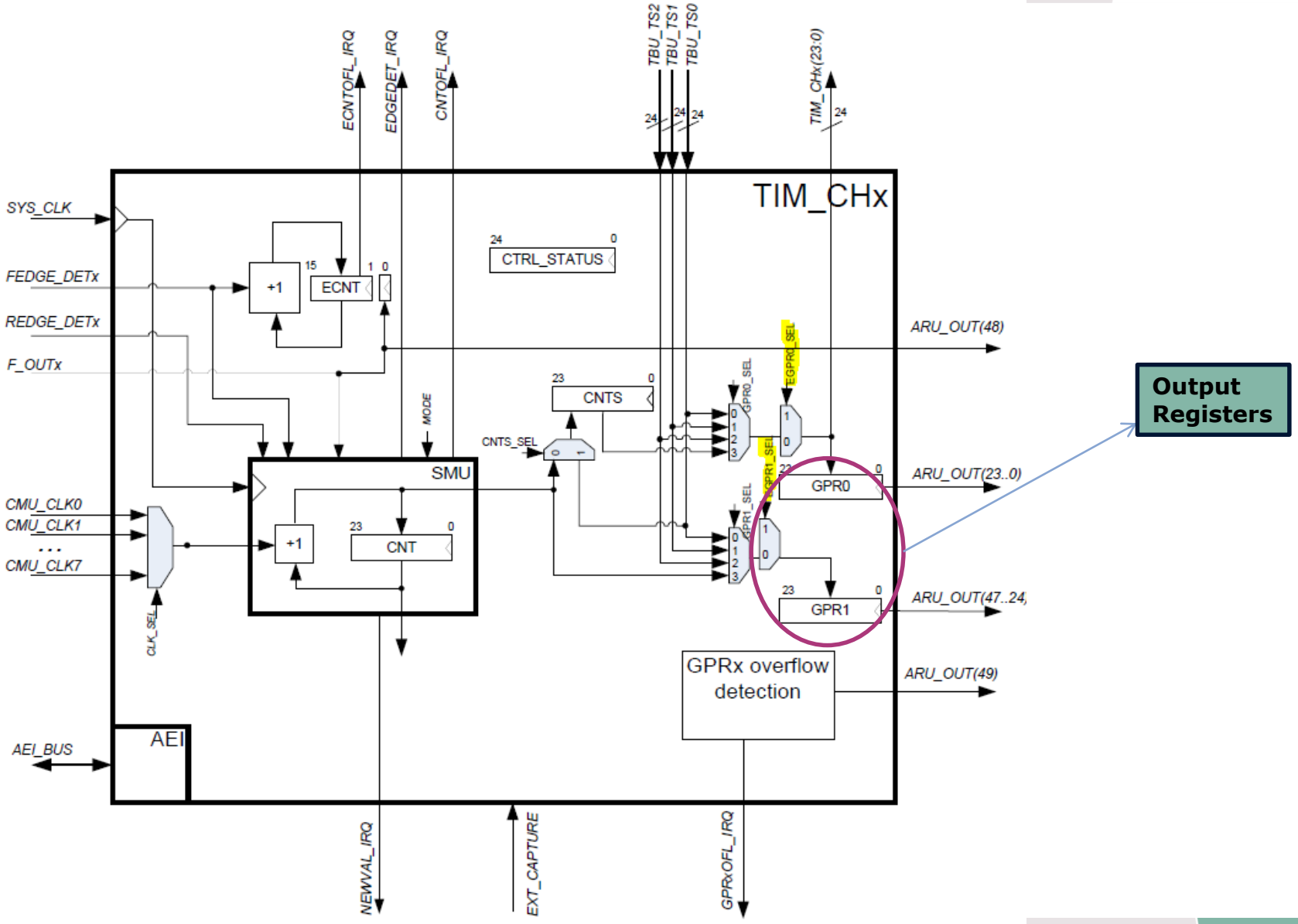



## Individual De-Glitch Time Mode (Hold Cnt)

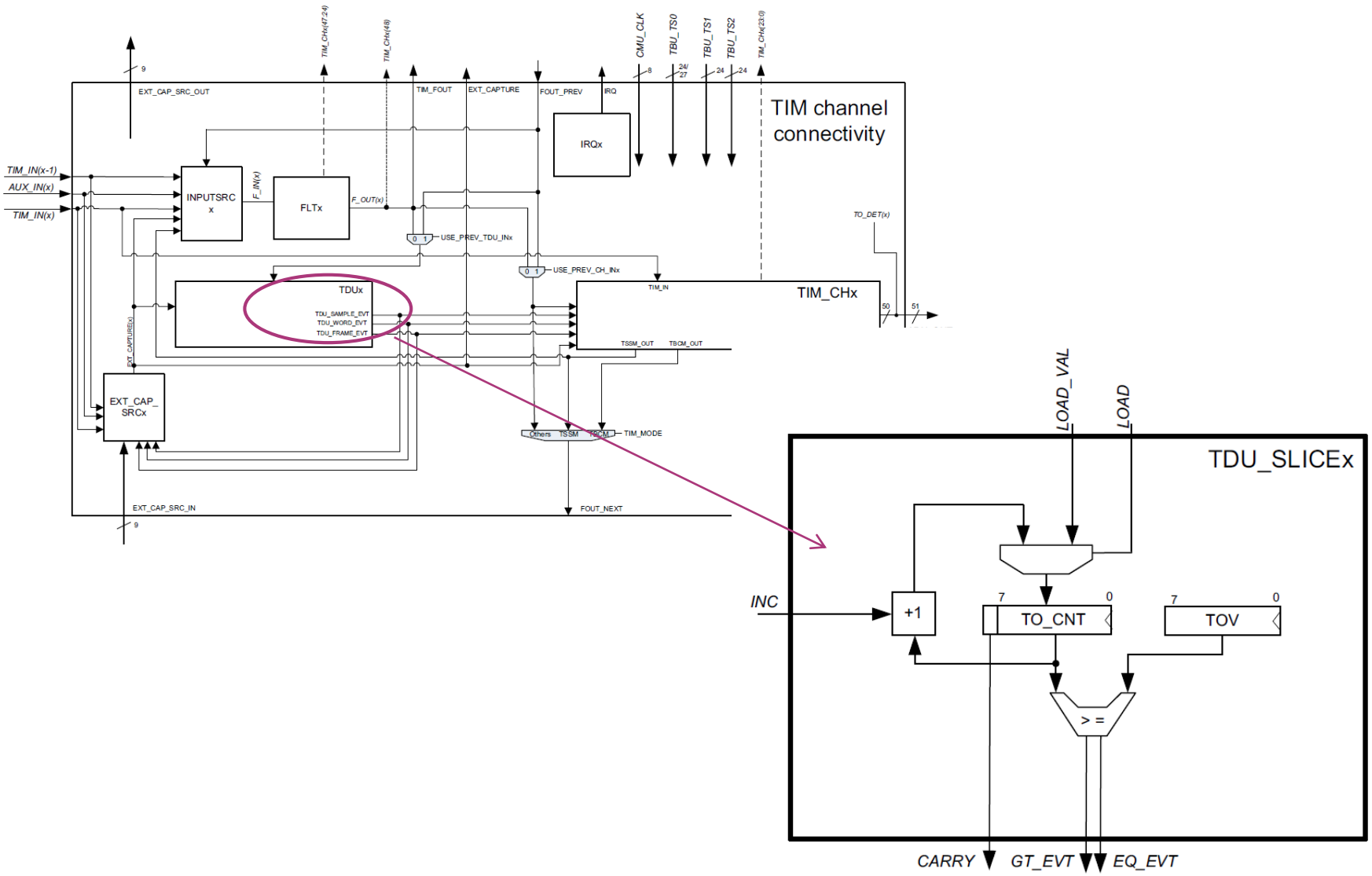



**RE-FE can be conf. with different modes (mixed mode)**

# GTM (Generic Timer Module)
# TIM - TIM_CHx – Timer Channel Architecture

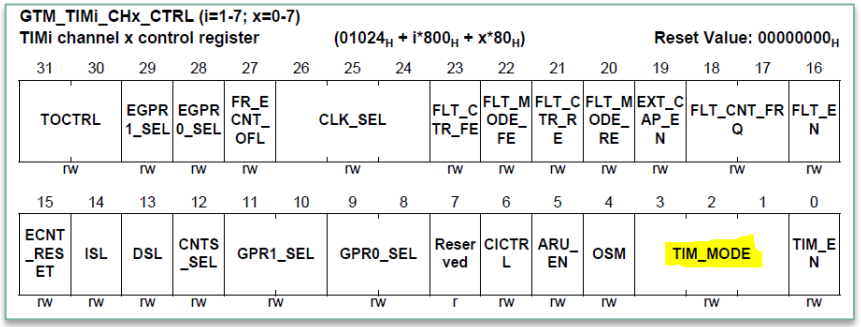


# GTM (Generic Timer Module)
# TIM - TDUx – Timeout Detection Unit



# GTM (Generic Timer Module)
# TIM - TIM_CHx – Channel Modes

- **TIM PWM Measurement Mode** (TPWM)
  - PWM Measuring (Period/Duty)
- **TIM Pulse Integration Mode** (TPIM)
  - Measure a Sum of RE of FE pulses
- **TIM Input Event Mode** (TIEM)
  - Edges Counting (R/F/Both)
- **TIM Input Prescaler Mode** (TIPM)
  - Wait a programmable number of edges before to raise the *TIM[i]_NEWVAL[x]_IRQ*
- **TIM Bit Compression Mode** (TBCM) – ***only on CH0***
  - Combines m-Filtered Input Channels….
- **TIM Gated Periodic Sampling Mode** (TGPS)
  - Periodic Sampling
- **TIM Serial Shift Mode** (TSSM)
  - Serial shifts input signal into register



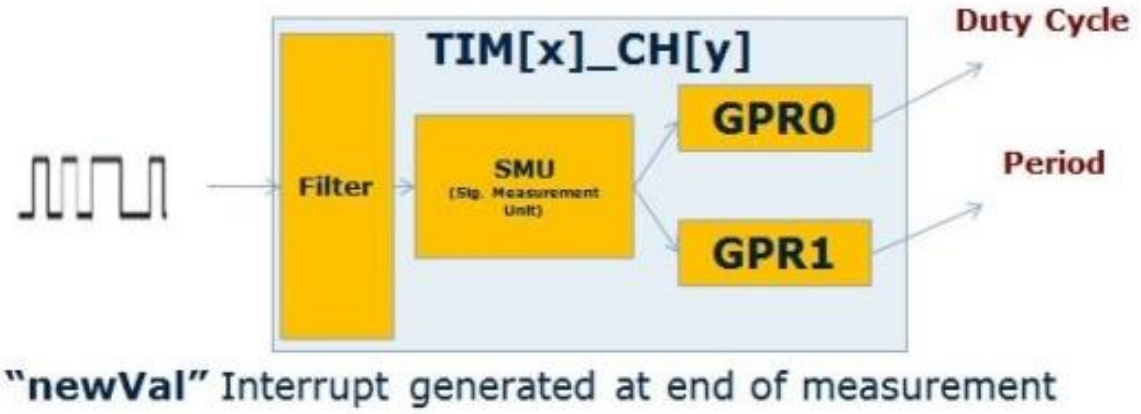
GTM_TIMi_CHx_CTRL (i=1-7; x=0-7)
TIMi channel x control register ($01024_H + i*800_H + x*80_H$) Reset Value: $00000000_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TOCTRL | | EGPR1_SEL | EGPR0_SEL | FR_ECNT_OFL | | CLK_SEL | | FLT_CTR_FE | FLT_MODE_FE | FLT_CTR_RE | FLT_MODE_RE | EXT_CAP_EN | FLT_CNT_FRQ | | FLT_EN |
| rw | | rw | rw | rw | | rw | | rw | rw | rw | rw | rw | rw | | rw |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ECNT_RESET | ISL | DSL | CNTS_SEL | GPR1_SEL | | GPR0_SEL | | Reserved | CICTRL | ARU_EN | OSM | TIM_MODE | | | TIM_EN |
| rw | rw | rw | rw | rw | | rw | | r | rw | rw | rw | rw | | | rw |

# GTM (Generic Timer Module)
# TIM – PWM Measurement Mode (TPWM)

**TIM[x]_CH[y] (TPWM Mode) = TIM PWM Measurement Mode**



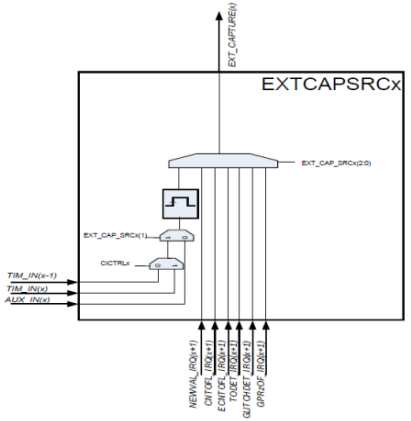

› When **External Capture** feature is enabled, the GPRx update is done on external signal

**GTM_TIMi_CHx_CTRL (i=1-7; x=0-7)**
**TIMi channel x control register** $(01024_H + i*800_H + x*80_H)$ **Reset Value: $00000000_H$**

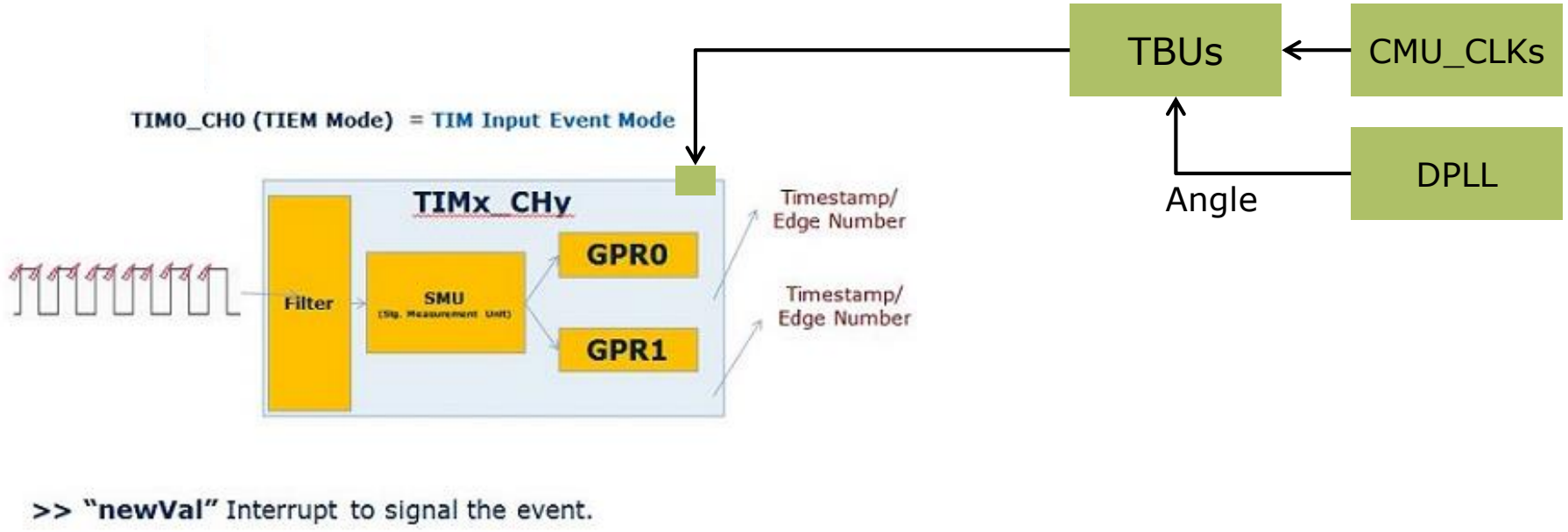
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TOCTRL | | EGPR1_SEL | EGPR0_SEL | FR_ECNT_OFL | CLK_SEL | | | FLT_CTR_FE | FLT_MODE_FE | FLT_CTR_RE | FLT_MODE_RE | EXT_CAP_EN | FLT_CNT_FRQ | | FLT_EN |
| rw | | rw | rw | rw | rw | | | rw | rw | rw | rw | rw | rw | | rw |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ECNT_RESET | ISL | DSL | CNTS_SEL | GPR1_SEL | | GPR0_SEL | | Reserved | CICTRL | ARU_EN | OSM | TIM_MODE | | | TIM_EN |
| rw | rw | rw | rw | rw | | rw | | r | rw | rw | rw | rw | | | rw |

| Input signal F_OUTx | selected CMU Clock | External capture | ISL | DSL | Action description |
|---|---|---|---|---|---|
| 0 | 1 | 0 | - | 0 | CNT++ |
| 1 | 1 | 0 | - | 0 | no |
| rising edge | - | 0 | 0 | 0 | capture CNT value in CNTS |
| falling edge | - | 0 | 0 | 0 | CNT=0 |
| rising edge | - | 0 | 1 | 0 | no |
| falling edge | - | 0 | 1 | 0 | capture CNT value in CNTS; CNT=0 |
| 1 | 1 | 0 | - | 1 | CNT++ |
| 0 | 1 | 0 | - | 1 | no |
| falling edge | - | 0 | 0 | 1 | capture CNT value in CNTS |
| rising edge | - | 0 | 0 | 1 | CNT=0 |
| falling edge | - | 0 | 1 | 1 | no |
| rising edge | - | 0 | 1 | 1 | capture CNT value in CNTS; CNT=0 |
| - | - | rising edge | - | - | do GPRx capture ; issue NEWVAL_IRQ |
| - | 0 | 0 | - | - | no |



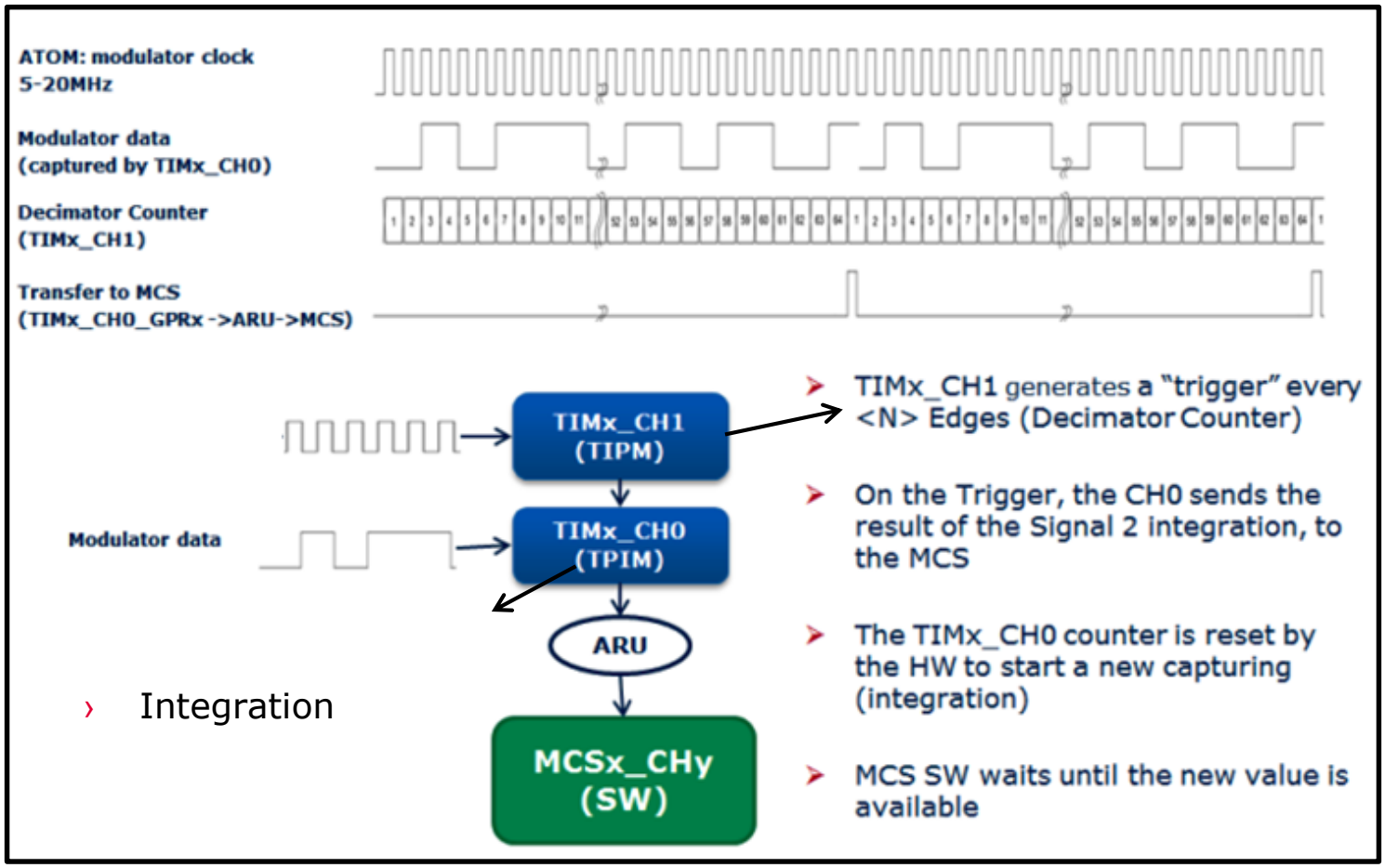
# GTM (Generic Timer Module)
# TIM – Input Event Mode (TIEM)



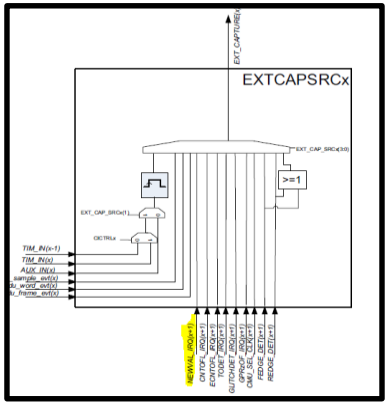

› If the **External Capture** feature is enabled

| Input signal F_OUTx | External capture | ISL | DSL | Action description |
|---|---|---|---|---|
| - | rising edge | 1 | - | do capture; issue NEWVAL_IRQ; CNT++ |
| - | 0 | 1 | - | no |
| 1 | rising edge | 0 | 1 | do capture; issue NEWVAL_IRQ; CNT++ |
| 0 | - | 0 | 1 | no |
| 0 | rising edge | 0 | 0 | do capture; issue NEWVAL_IRQ; CNT++ |
| 1 | - | 0 | 0 | no |

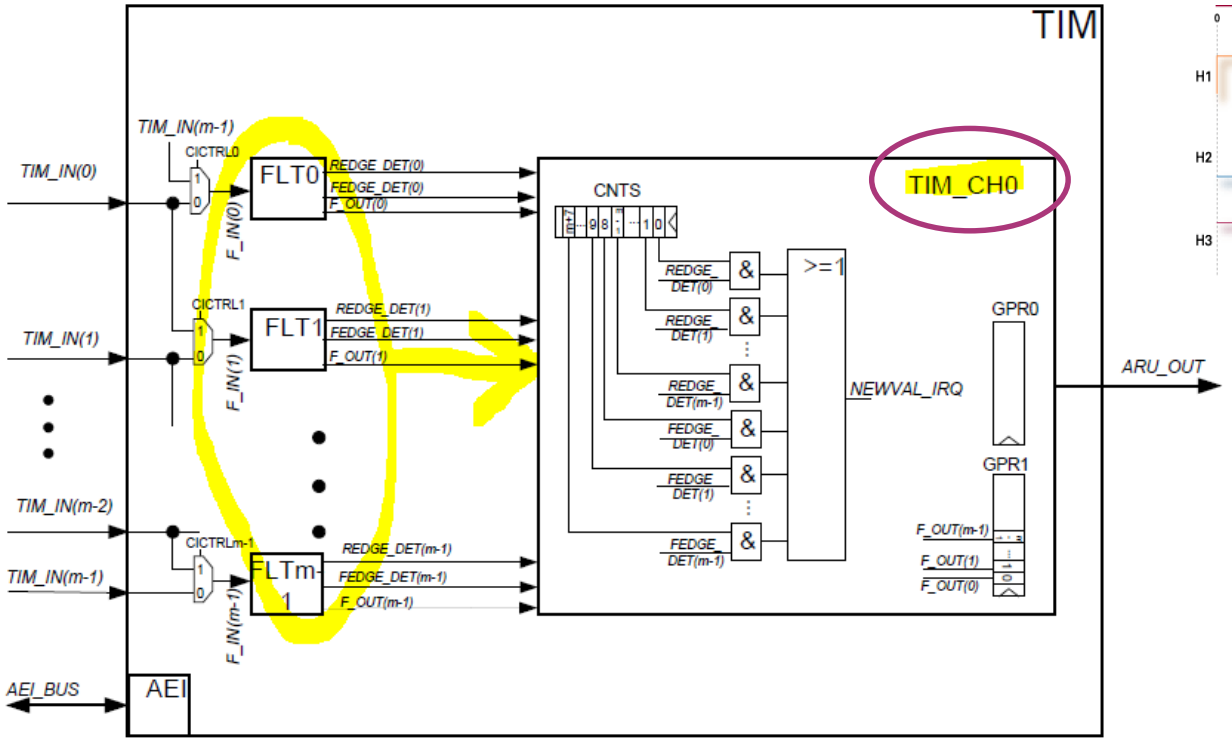
# GTM (Generic Timer Module)
# TIM – TIPM (Prescaler) and TPIM (Integration) Mode

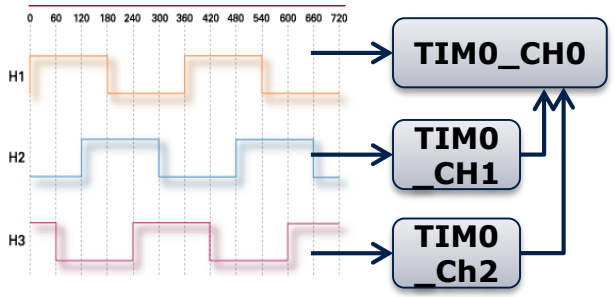



› Integration



# GTM (Generic Timer Module)
# TIM Bit Compression Mode (TBCM)




The register **CNTS** of TIM channel 0 is used to configure the event that releases the *NEWVAL_IRQ* and samples the input signals F_IN(0) to F_IN(*m*-1) in ascending order as a parallel data word in **GPR1**.

The bits 0 to *m-1* of the **CNTS** register are used to select the *REDGE_DET* signals of the TIM filters 0 to *m-1* as a sampling event, and the bits 8 to (7+*m*) are used to select the *FEDGE_DET* signals of the TIM filters 0 to *m-1*, respectively. If multiple events are selected, the events are OR-combined (see also Figure 10.4.2.5.1).

**EGPR0_SEL**,**GPR0_SEL** selects the timestamp value, which is routed through the ARU. **GPR1_SEL** is not applicable in TBCM mode.

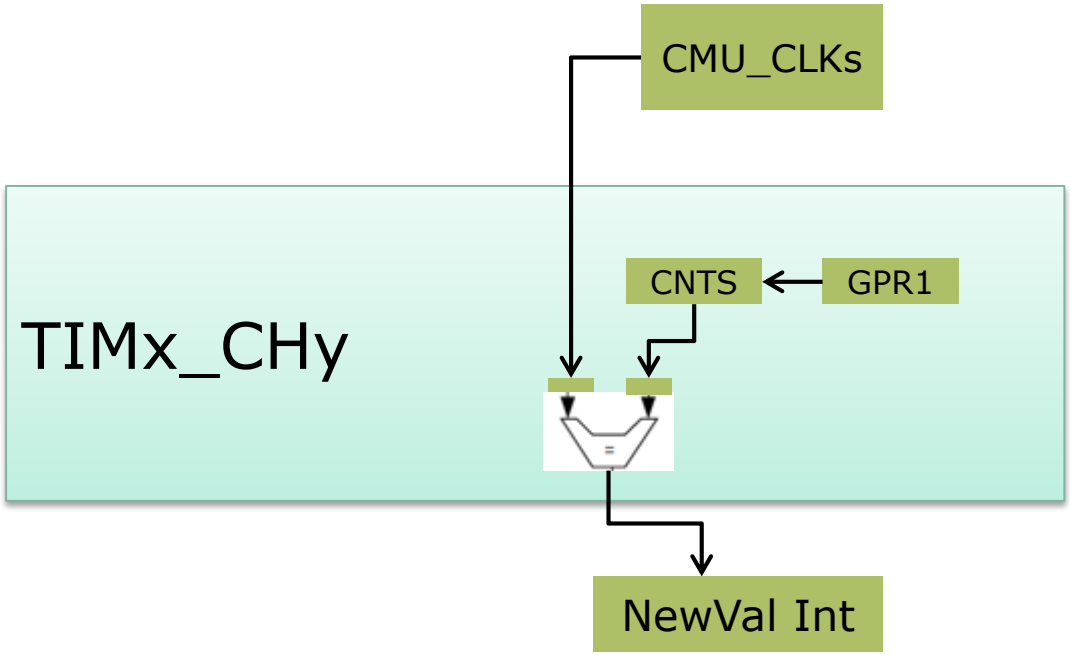
Example:

New Val generated on every new edge detected on 3 channels

```
--- Rising Edge -----
CNTS[0]=1, //CH0
CNTS[1]=1, //CH1
CNTS[2]=1, //CH2
CNTS[3]=0, //CH3
.....
CNTS[7]=0, //CH7
----- Falling Edges ----
CNTS[8]=1, //CH0
CNTS[9]=1, //CH1
CNTS[10]=1,//CH2
CNTS[11]=0,
......
CNTS[14]=0,//CH7
```

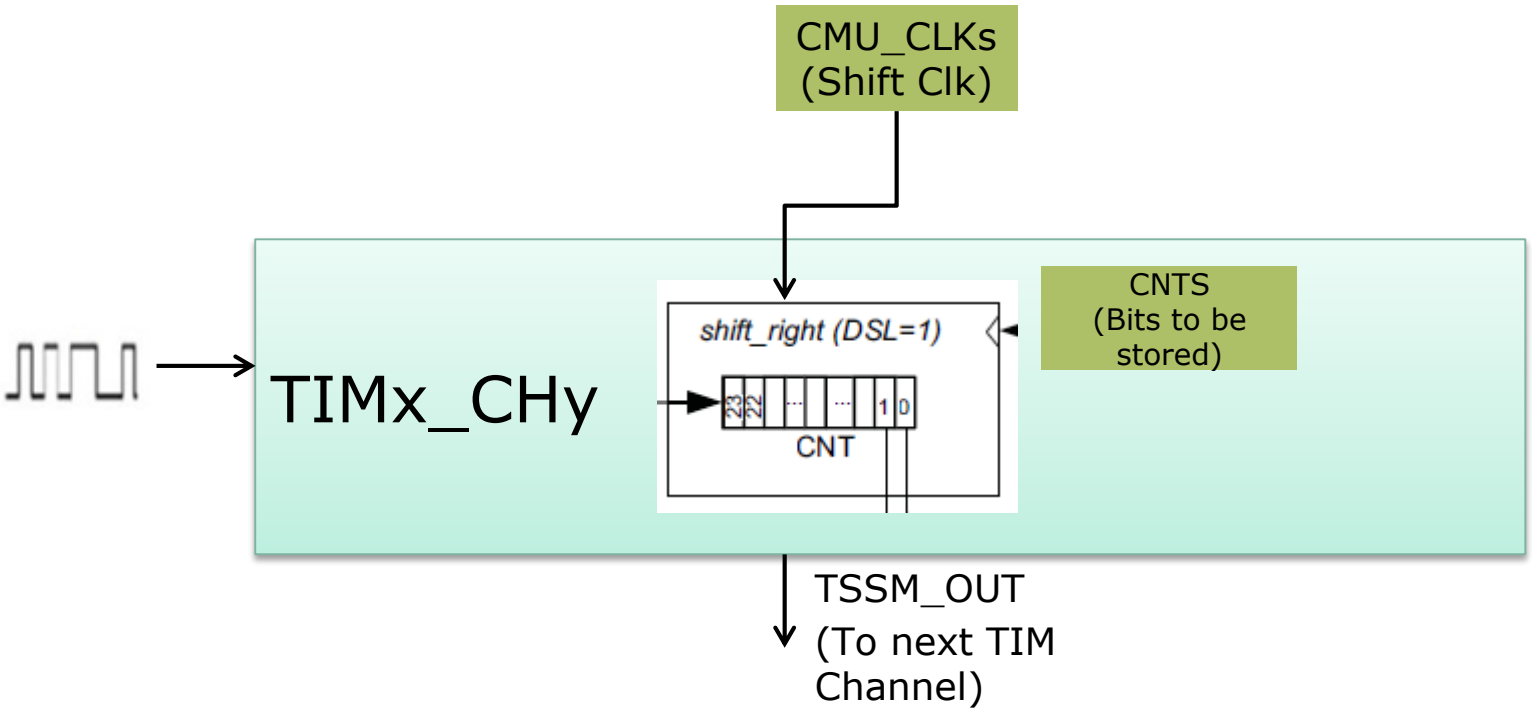
# GTM (Generic Timer Module)
# TIM Gated Periodic Sampling Mode (TGPS)

- To program **Periodic Sampling**
- The number of CMU clock cycles which should elapse before capturing and raising *TIM[i]_NEWVAL[x]_IRQ is programmable.*
- ***CNTS <= how many CMU clock cycles***
- **TIM[i]_CH[x]_GPR1 operates as a shadow register for TIM[i]_CH[x]_CNTS**

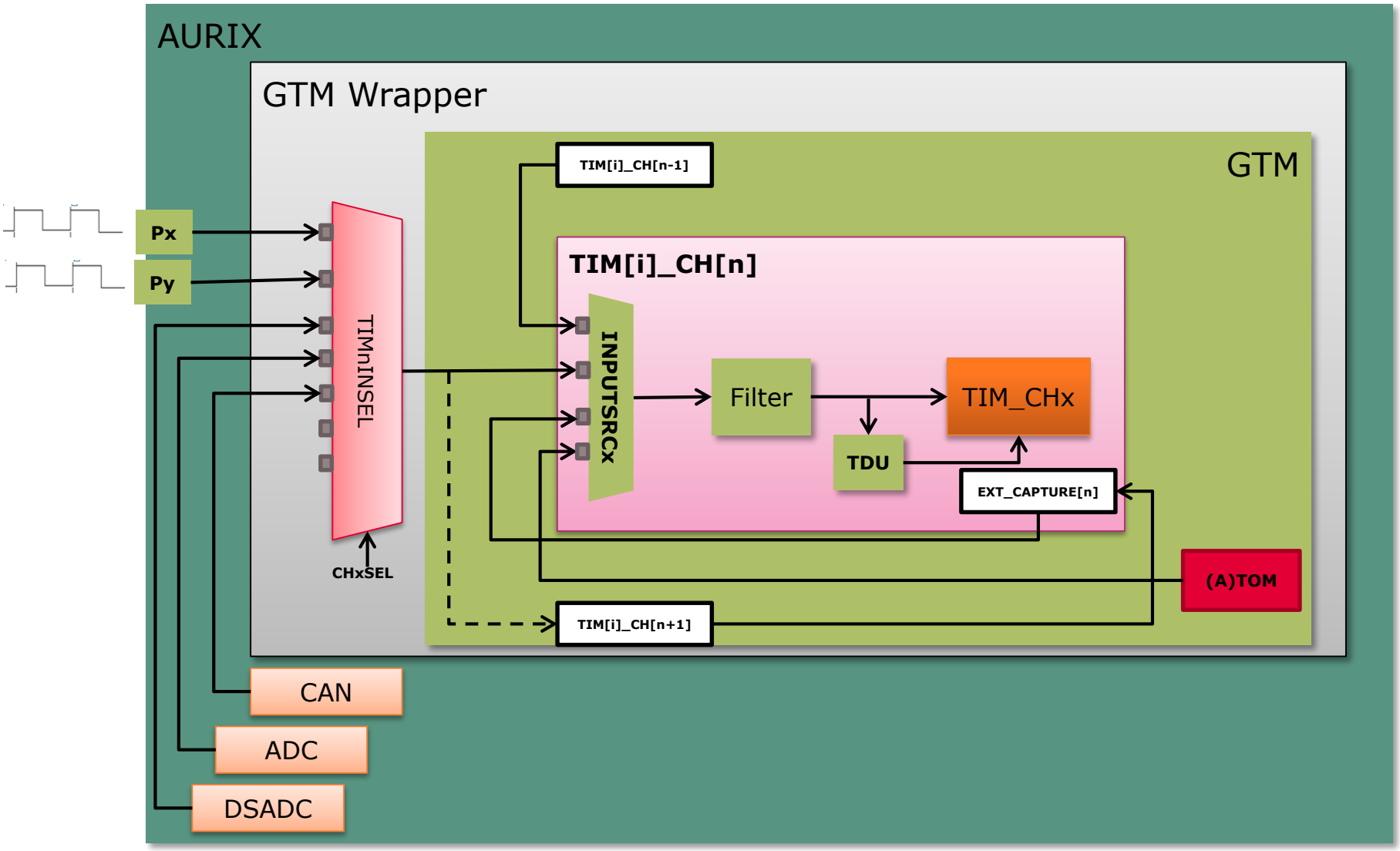


# AURIX2G
# TIM Improvements /TSSM (Serial Shift Mode)

In the TIM Serial Shift Mode on each shift clock event the actual value of the input signal **TSSM_INx** will be registered in dependence of **DSL** n the register **TIM[i]_CH[x]_CNT**.



# General Use Cases
# Signals Measuring and Filtering (Connections)



# Agenda

1. GTM Overview
2. CTBM-Clock & Time Base Management
3. TIM-Timer Input Module
4. ARU-Advanced Routing Unit
5. TOM-Timer Output Module
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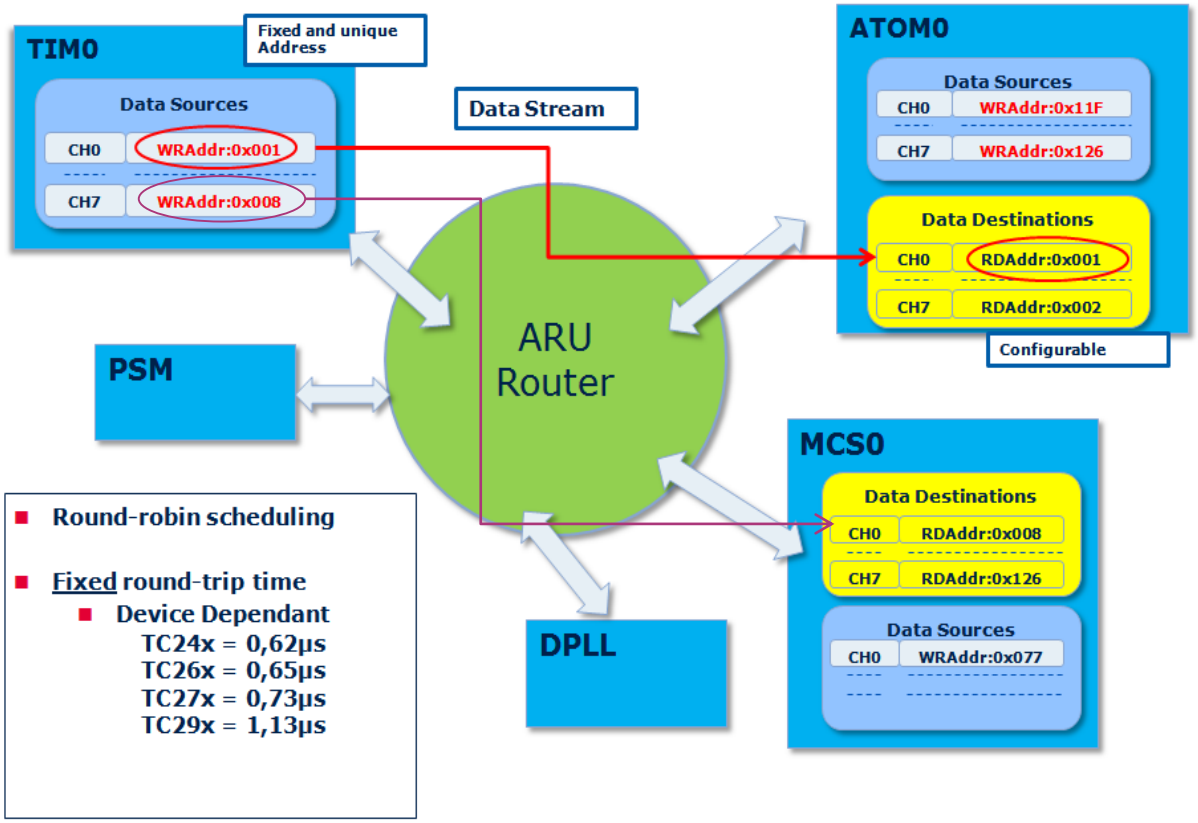
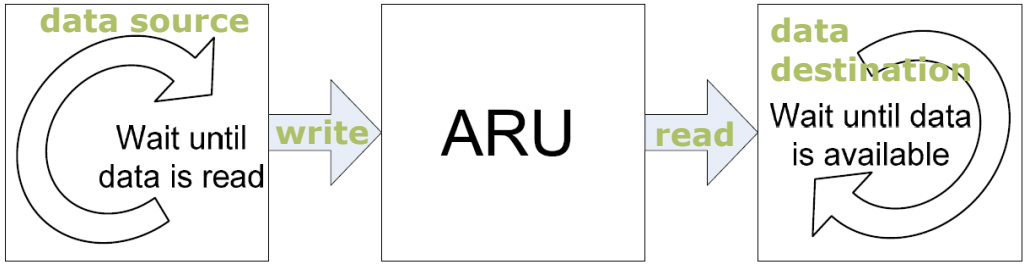
7. DTM-Dead Time Module

# GTM Architecture Overview
# ARU – Advanced Routing Unit

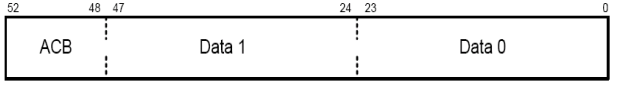



- Round-robin scheduling
- Fixed round-trip time
  - Device Dependant
    - TC24x = 0,62µs
    - TC26x = 0,65µs
    - TC27x = 0,73µs
    - TC29x = 1,13µs



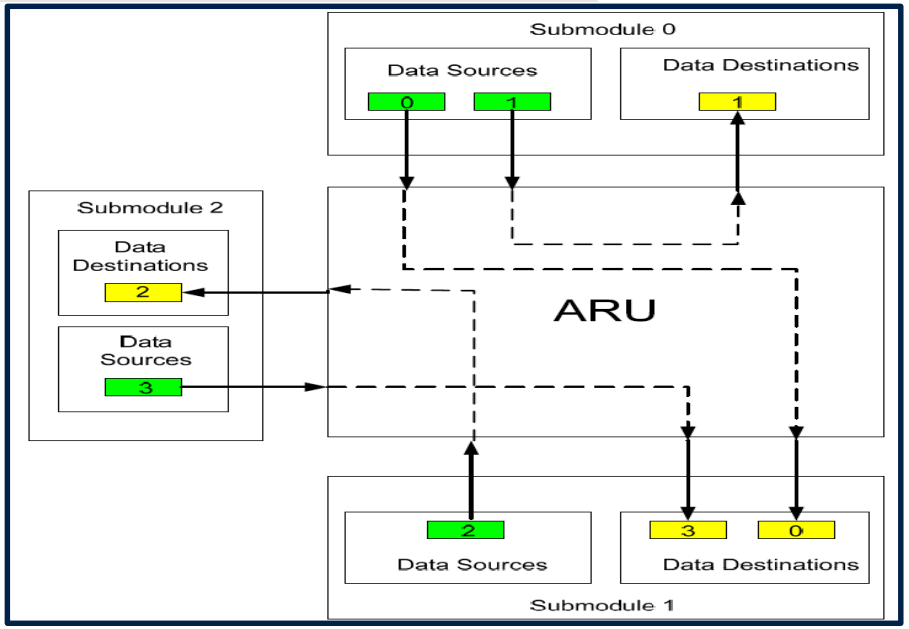

**Basic concept**

- No need of an internal **Interrupt mechanism**.
- Data routing between **source** and **destination** sub modules.
- Deterministic round-robin scheduling
- Worst Case Round Trip Time
  - **113*SYS_CLK** (IP_104)
- The Routed data word size is 53 bits



# GTM (Generic Timer Module)
# ARU – Advanced Routing Unit

- The ARU + Broadcast unit (BRC) and the Parameter Storage Module (PSM) forms the **infrastructural part** of the GTM
  - ARU **write channels** are named **data sources**
    - Each data source has its **fixed and unique source address**
  - ARU **read channels** are named **data destinations**
    - Destination channels have **configurable read addresses** to select a source sub-module channel
  - connection between a data source and a data destination is called **data stream**
  - ARU serves the connected destination sub-module channels in a **round-robin scheduling scheme**
    - Every destination sub-module channel is served regularly in a fixed time scheme
    - Round-Trip time is determined by number of destination sub-module channels connected to ARU




| Submodule | Number of data sources | Number of destinations |
|---|---|---|
| ARU | 1 | 0 |
| DPLL | 24 | 24 |
| TIM 0-3 | 32 | 0 |
| MCS 0-3 | 96 | 32 |
| BRC | 22 | 12 |
| TOM | 0 | 0 |
| ATOM 0-4 | 40 | 40 |
| PSM 0 | 8 | 8 |
| CMP | 0 | 0 |
| MON | 0 | 0 |
| Total | 223 | 116 |

# Agenda

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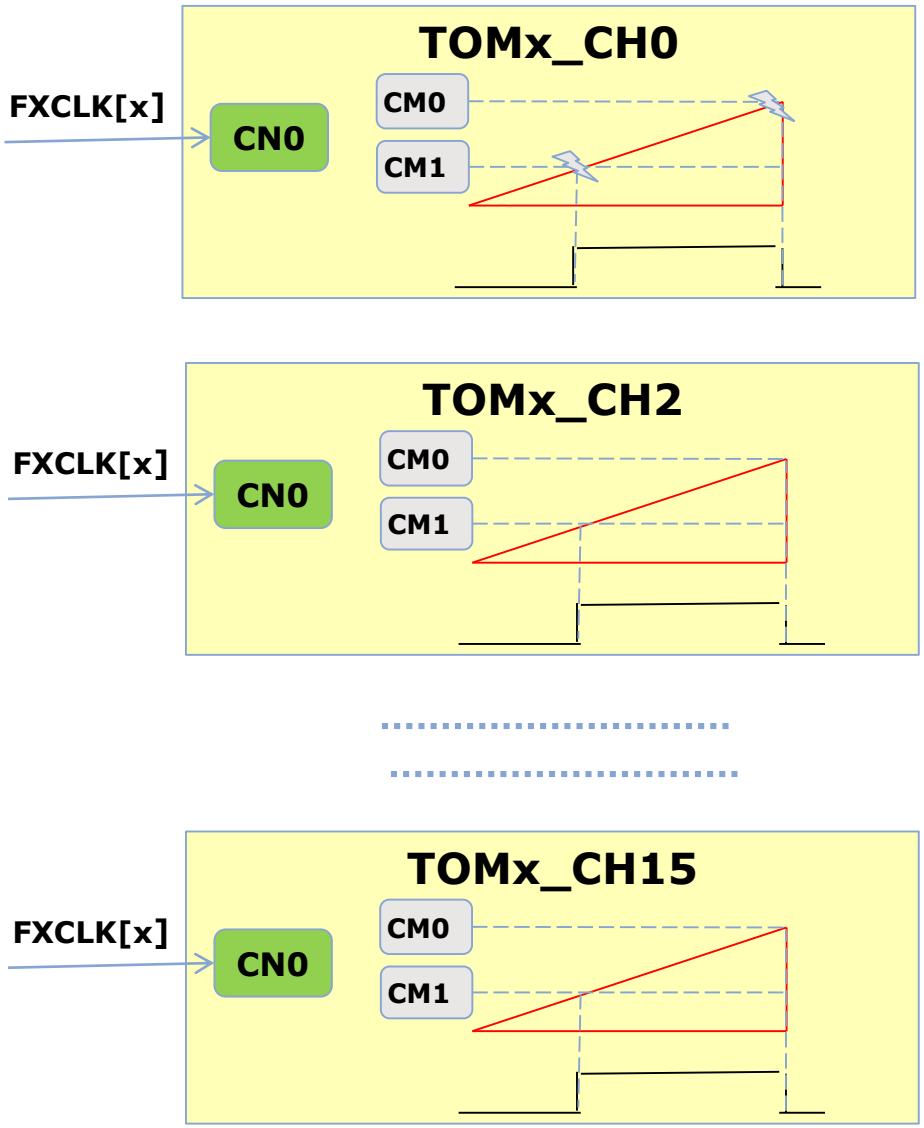
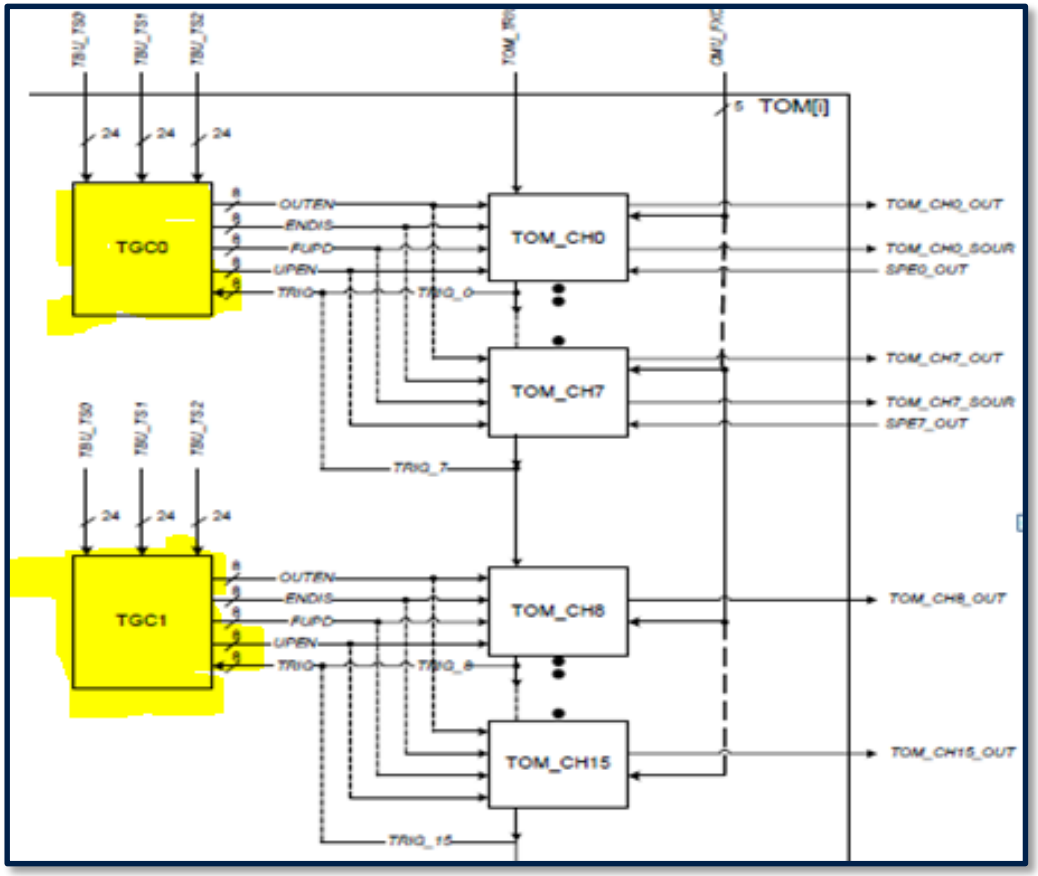
# GTM Architecture Overview
# TOM – Timer Output Module

- **16 independent** channels (**TOM_CH0…15**) for **simple PWM generation**
- A **16-bit Counter (CN0)** for each CHs
- 5 dedicated clocks
  - **FX_CLK (1:1, 1:16, 1:256..)**



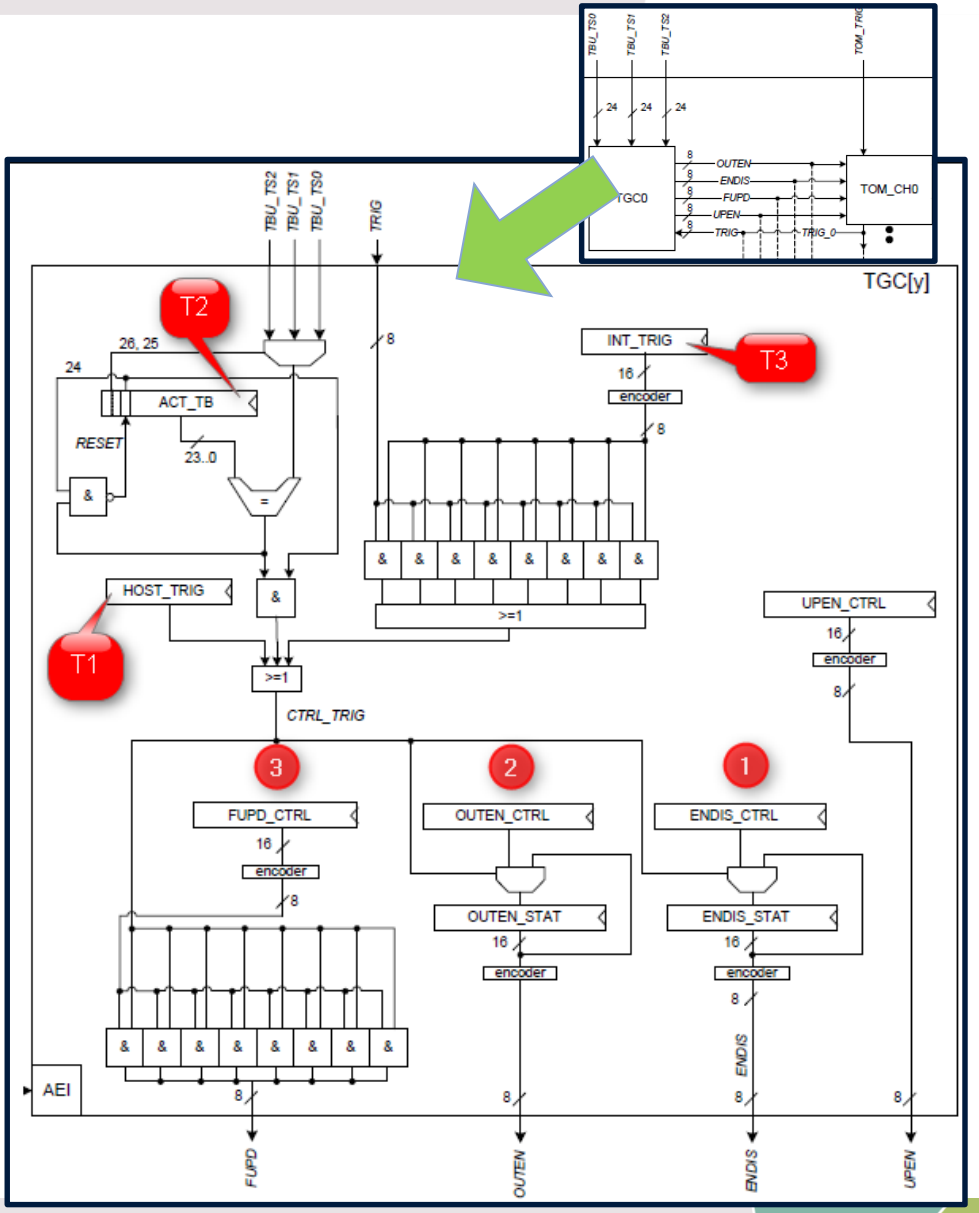
# GTM (Generic Timer Module)
# TOM – Timer Output Module - Overview

- **2 groups of 8 channel**
- **Global channel control**
- **Driver the** channels **synchronously**.
  - Channels enabling/disabling
  - Output Enable/Disable
  - Force update



# GTM (Generic Timer Module)
# TOM – TGCx - Global Channel Control

- 3 **trigger** sources to control the update and enabling of the Channels
  - **T1**: SW (via SFR **HOST_TRG**)
  - **T2**: TBU time stamp based on selected TBU_TSx time base
    - TBU time stamp can be defined by **SFR ACT_TB**
  - **T3**: Internal trigger signal TRIG_x
    - signal TRIG_x coming from channel x within a TOM module can be masked by SFR **INT_TRIG**



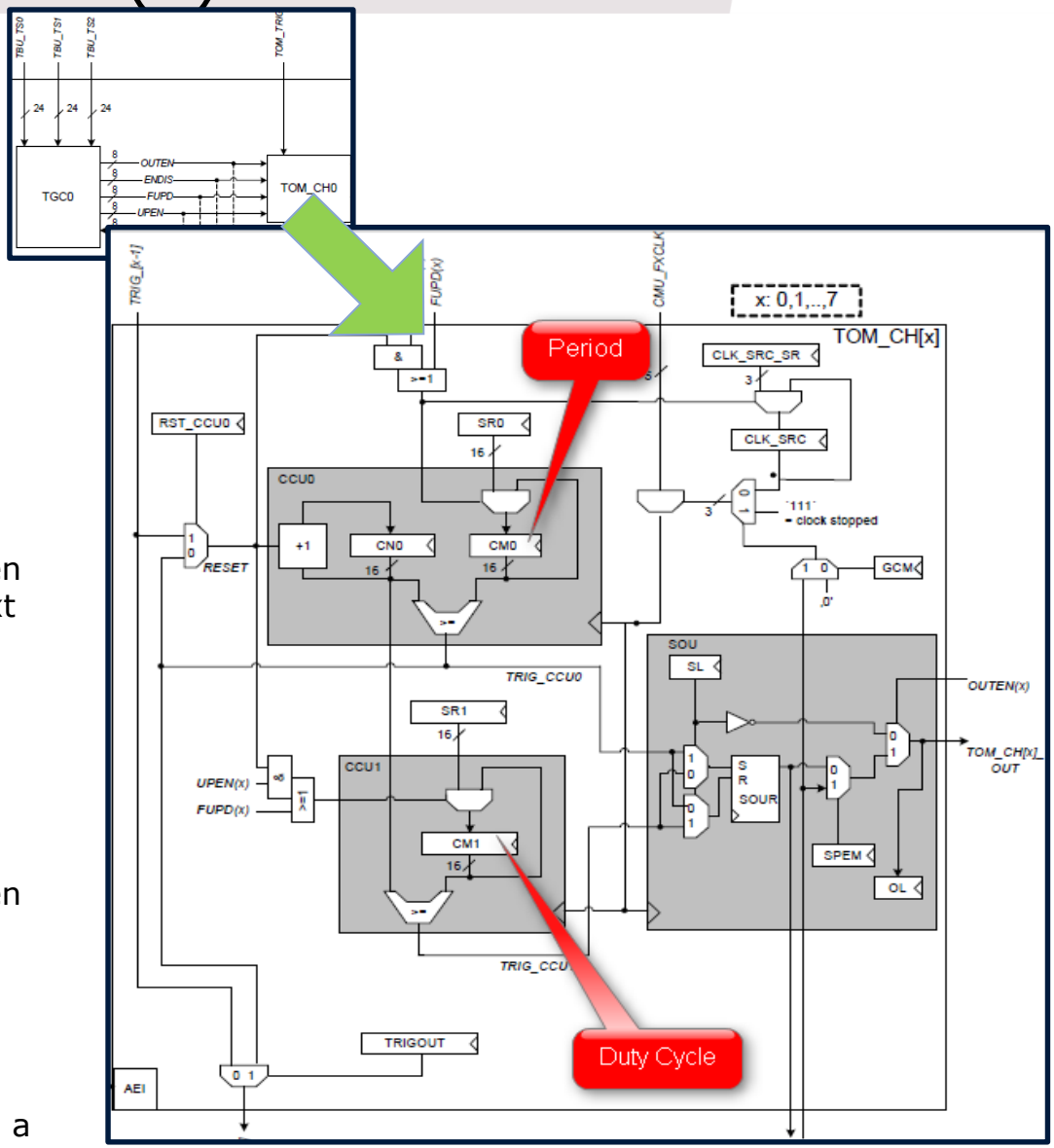
# GTM (Generic Timer Module)
# TOM – TM_CHx – Overview (1)

- Each TOM channel comprises
  - Counter Compare Unit 0 (**CCU0**)
  - Counter Compare Unit 1 (**CCU1**)
  - Signal Output generation Unit (**SOU**)

- **CCU0**
  - 16 bit counter **CN0** can be reset
    - when counter value is equal to 16 bit compare value **CM0** (Period)
    - when signaled by the Trigger signal **TRIG_x-1** (settings **RST_CCU0**)
  - when CN0 is greater or equal than CM0, then CCU0 unit triggers SOU subunit and the next TOM channel (signal **TRIG_CCU0**)

- **CCU1**
  - 16 bit greater equal comparison in-between CN0 and **CM1** (Duty Cycle)
  - when CN0 is greater or equal than CM1, then CCU1 unit triggers **SOU** subunit (signal **TRIG_CCU1**)

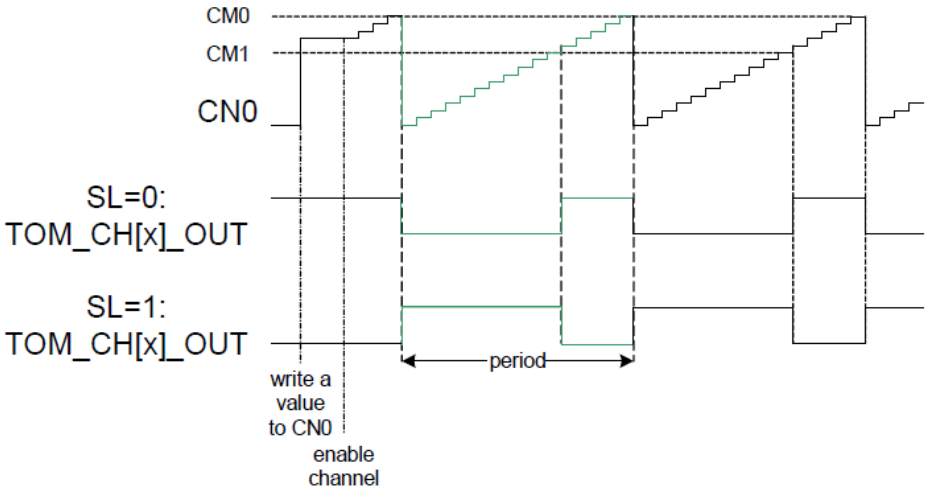
- **SOU**
  - responsible for PWM output generation on trigger signals **TRIG_CCU0** or **TRIG_CCU1** a

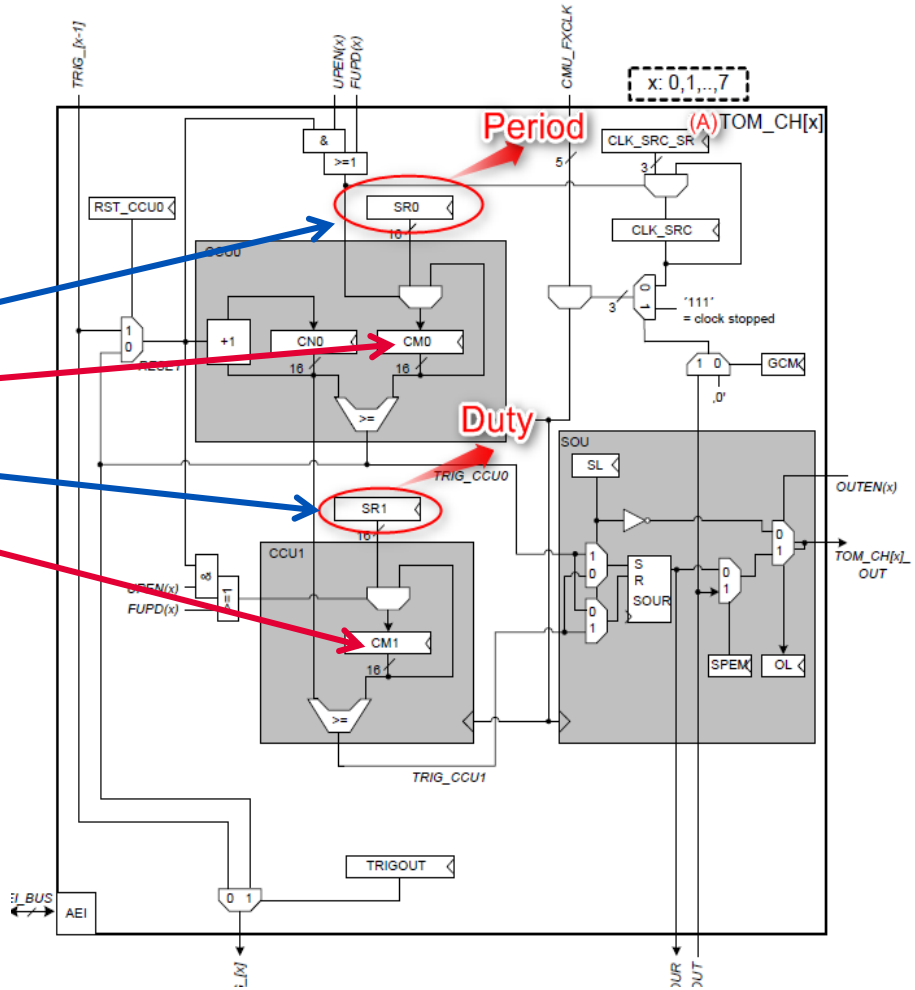


# GTM (Generic Timer Module)
# TOM – PWM Generation (1)

- **TOM and ATOM have similar configuration**
- **Synchronous update**
  - **CPU updates SR0/SR1**
- **Asynchronous update**
  - **CPU updates CM0/CM1**

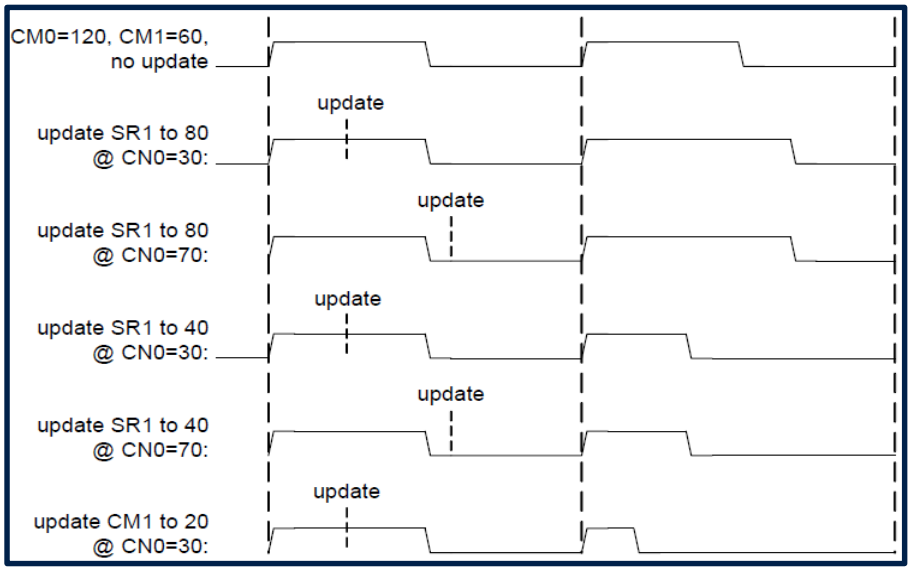
CPU

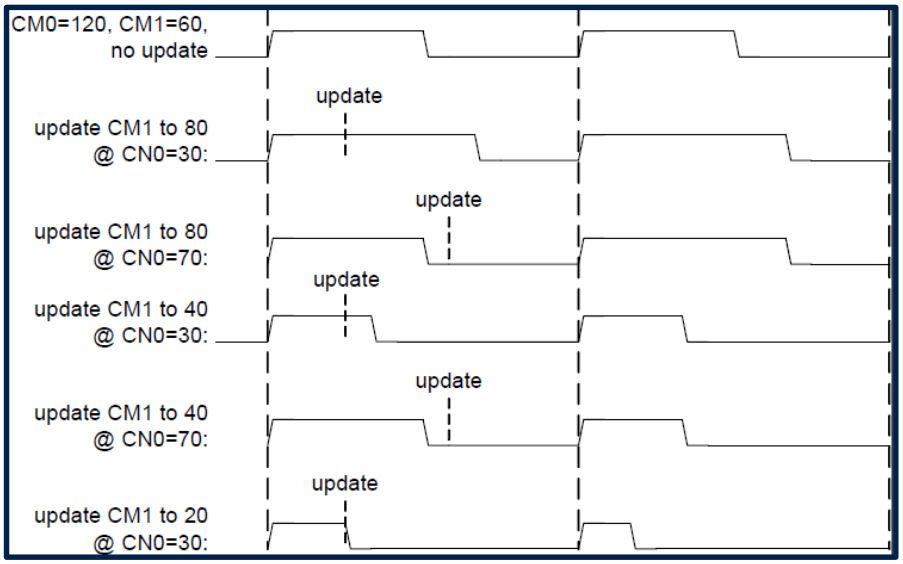



**SL = Signal level for Duty Cycle.**

# GTM (Generic Timer Module)
# TOM – PWM Generation (2)



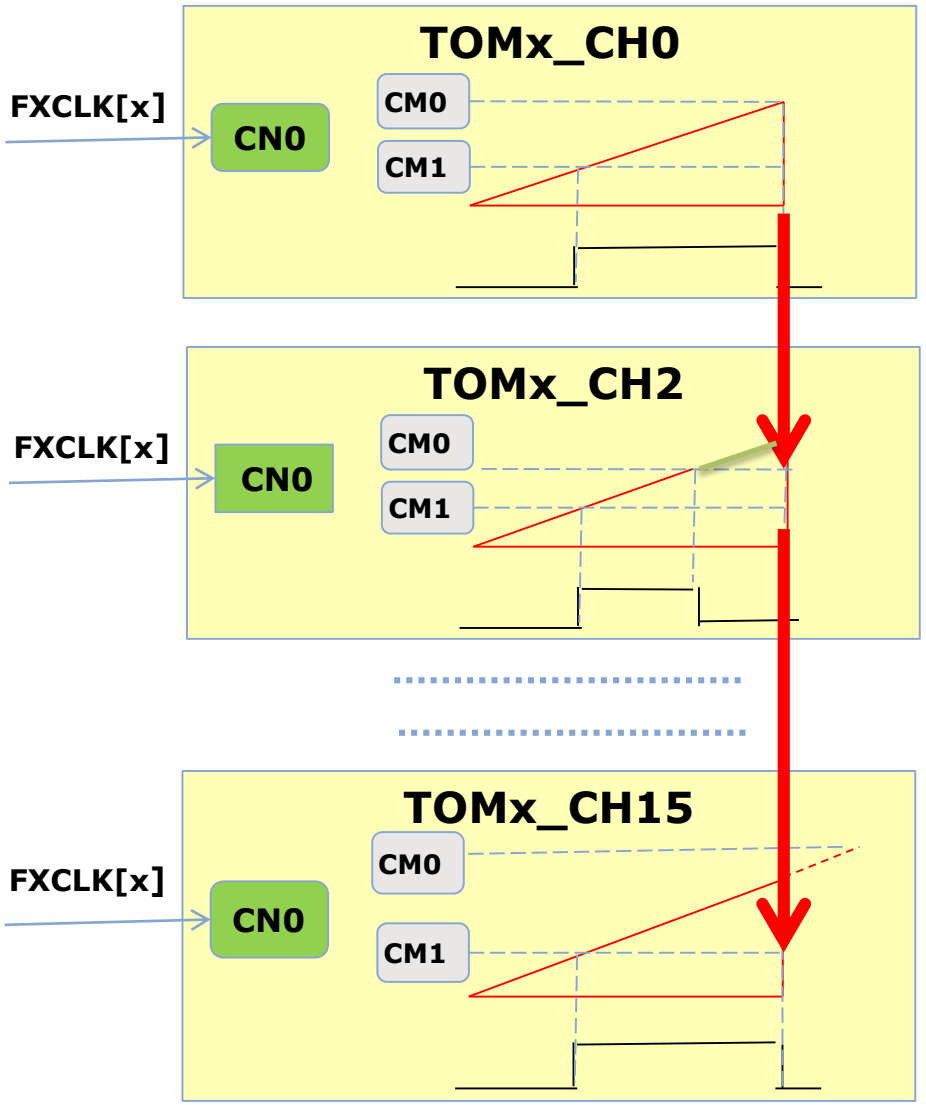

- **Synchronous Update**
- the desired new value can be written directly to register **SR1 (shadow reg.)**
- The new duty cycle is then applied in the period following the period where the update of register SR1 was done

- **Asynchronous Update**
- the desired new value can be written directly to register **CM1**
- Depending on the **point of time** of the update of CM1 in relation to the actual value of CN0 and CM1, **the new duty cycle is applied in the current period or the following period**

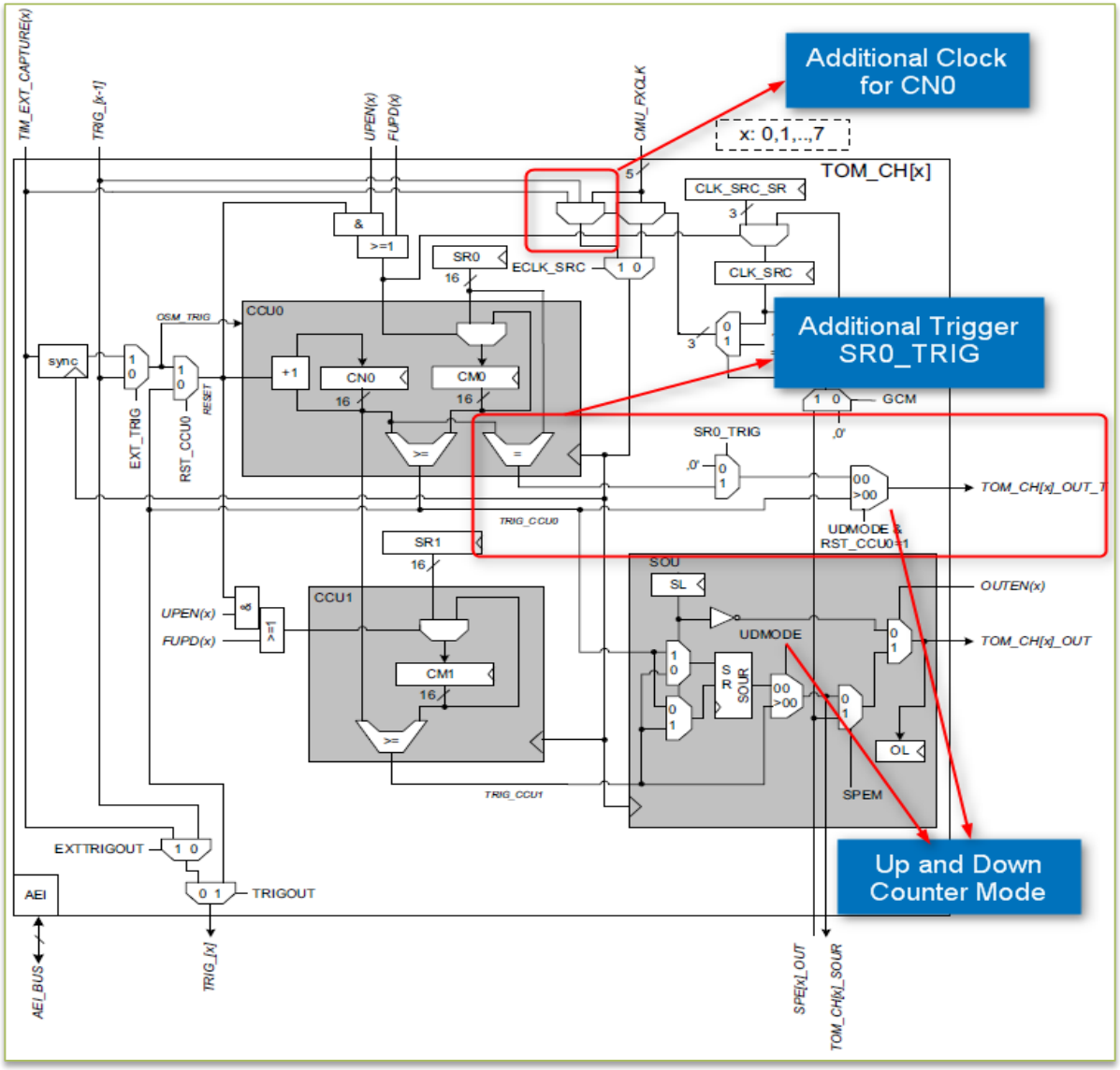
# GTM Architecture Overview
# CN0 Reset by the Previous Channel

- The Counter CN0 can be reset:
  - On CM0 match (period)
  - From the **previous channel**

- **A Trigger can be propagated through all the Channels**



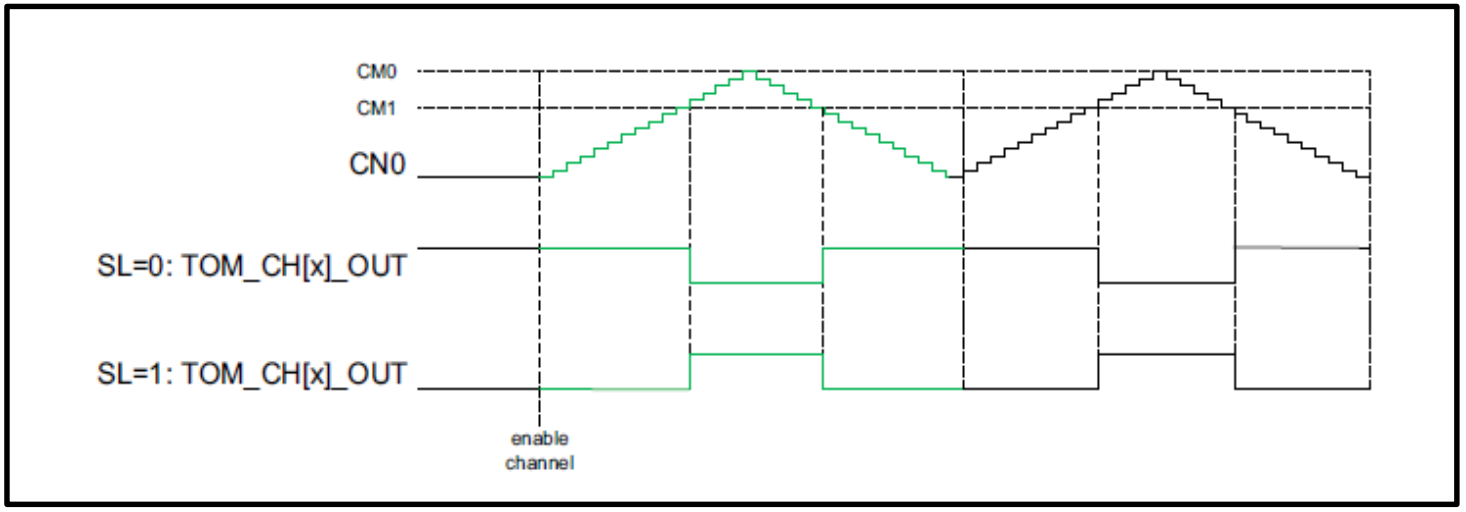
# AURIX2G Improvements (A)TOM



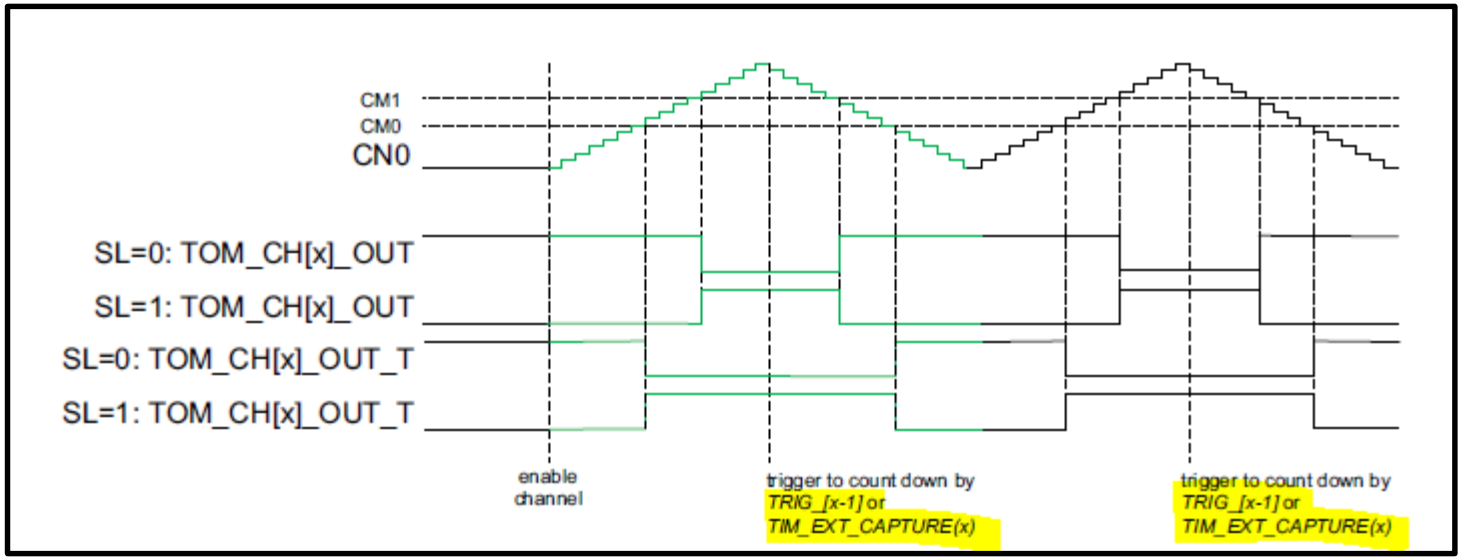

## (A)TOM improvements overview

- (A)TOM trigger pulse generation SR0_TRIG
- (A)TOM up-down counter mode UD_MODE
- (A)TOM extended clock source ECLK_SRC for CN0: *TRIG_[x-1]* and *TIM_EXT_CAPTURE(x)* as clock signa
- (A)TOM freeze mode FREEZE: no change of output *(A)TOM_CH(x)_OUT* if channel is
- ATOM SOMC/SOMB extended update mode EUPD *below)*

# AURIX2G Improvements
# Up-Down counter mode




› In case of Trigger coming from another channel (RST_CC0=1)



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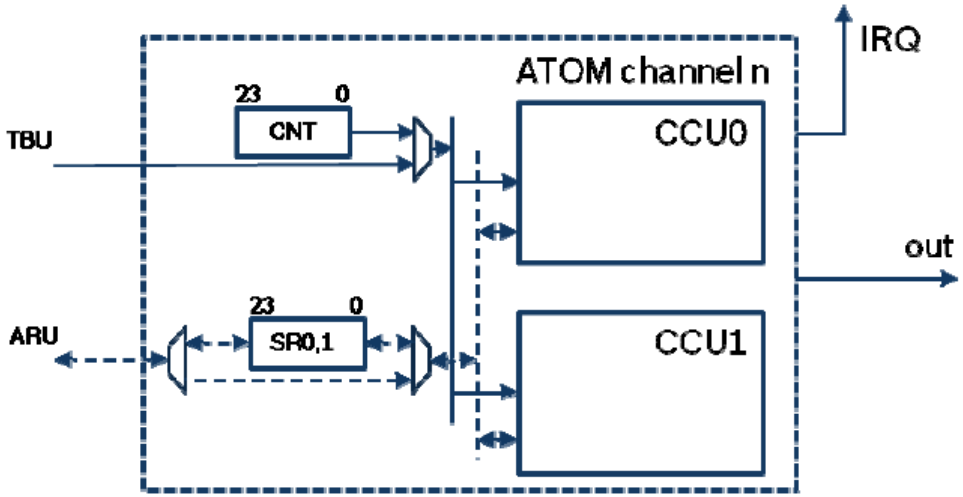
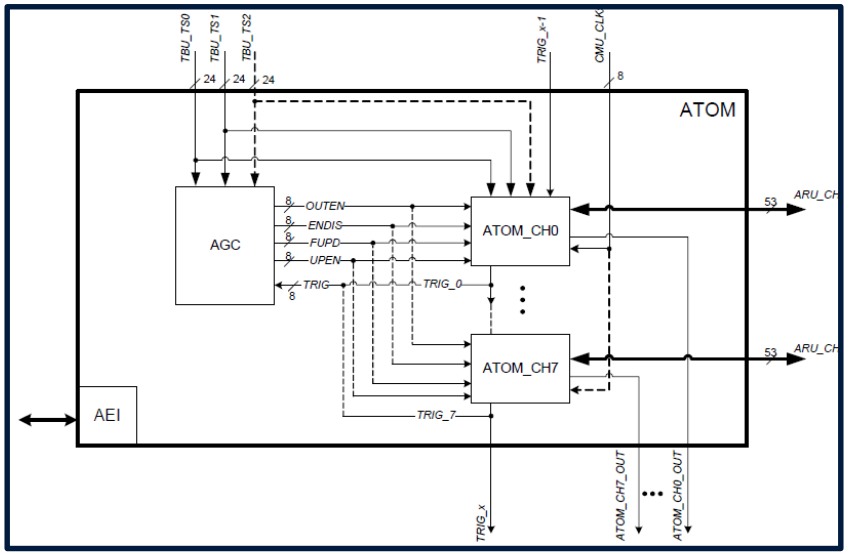
# GTM (Generic Timer Module) ATOM – Channel Architecture

- The most of the concepts are similar to the TOM module



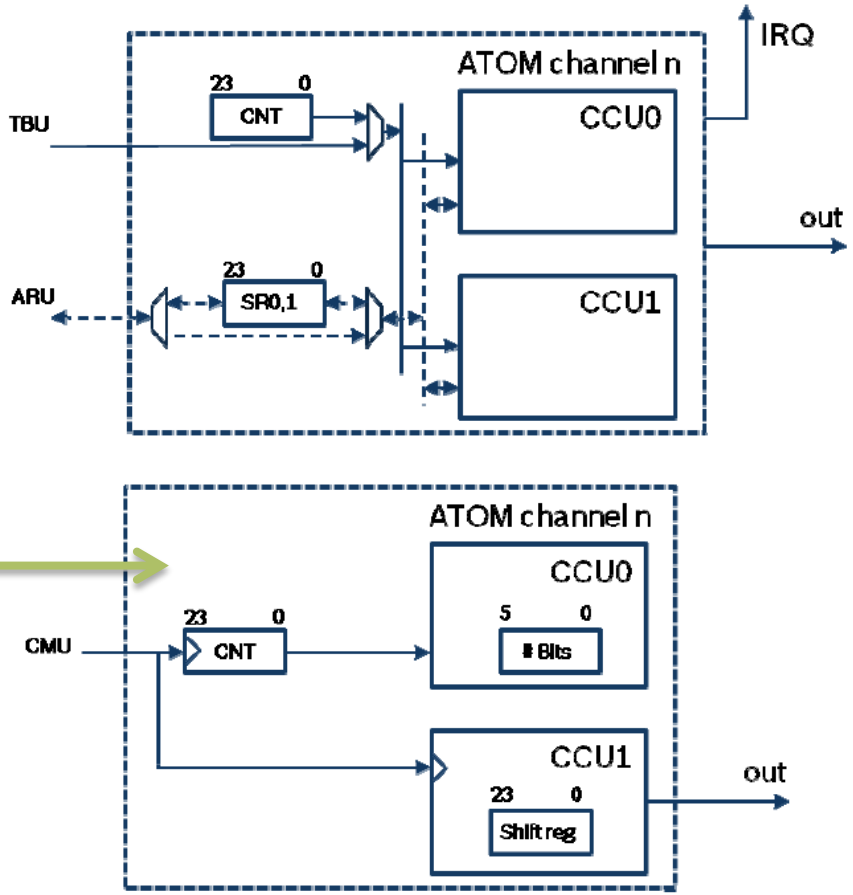

- The main differences are:
  - ATOM uses a different clocks (**CMU_CLK 0…7**)
  - ATOM is connected to other modules with the ARU
  - Compare strategy not only "less and equal" but also "**greater and equal**"
  - Each ATOM sub-module contains **8** channels (not 16)
  - ATOMs can generate **complex PWM** signals.



# GTM (Generic Timer Module)
# ATOM – Channel Architecture

› ATOM supports **4 operative modes**

- Signal Output Mode Compare (**SOMC**)
  - Complex Pulses (Injection/Ignition)
- Signal Output Mode PWM (**SOMP**)
  - PWM Generation
- Signal Output Mode Serial (**SOMS**)
  - Serial Shifter (Left/Right)
- Signal Output Mode Immediate **(SOMI)**

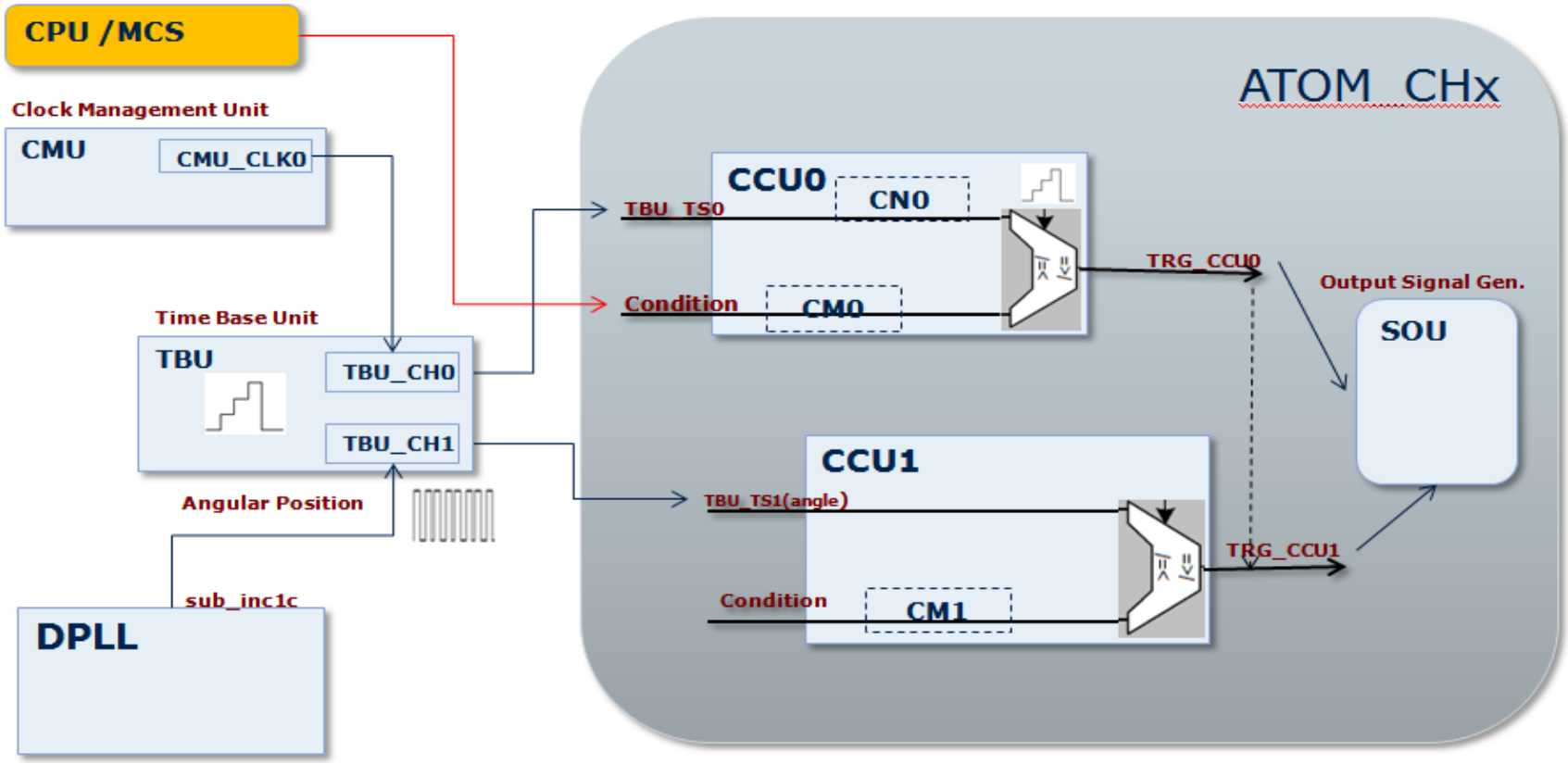



› **** CCU: Counter Compare Unit***

# GTM (Generic Timer Module)
# ATOM – Capture & Compare Strategy (SOMC)

**Controlled by the ARU Control Bits:**

**ACB[4:0]=>**(5 bits ) controls the compare mechanism inside of the CCU0/1.
**ACB[1:0]=>**(2 bits) to define the **output action**: no action, set to '1', set to '0' and toggle.
**ACB[4:2]=>**(3 bits) to define a **compare strategy**: CCU0 only, CCU1 only, compare in both at the same time (serve first/last)



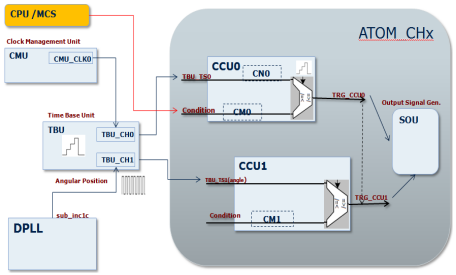
# GTM (Generic Timer Module)
# ATOM – Capture & Compare Strategy (SOMC)

ACB (ARU Control Bit) Description

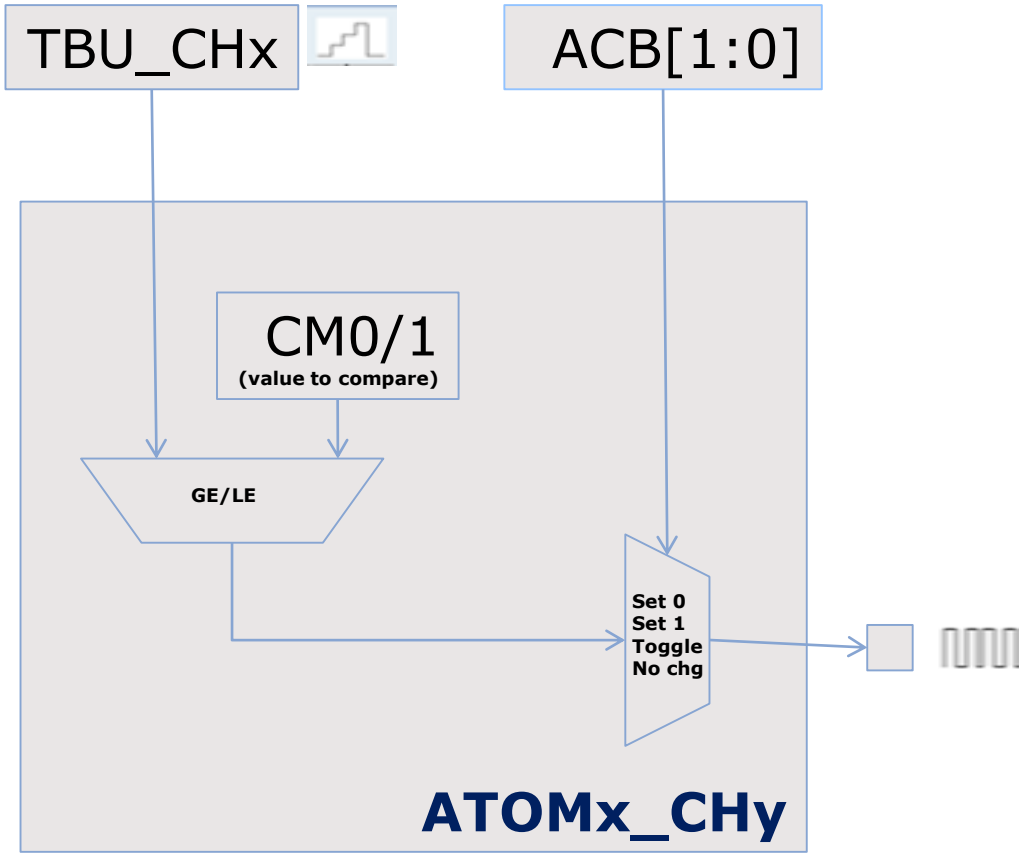
Search : Clear

| HEX | ACB[4] | ACB[3] | ACB[2] | ACB[1] (OUT) | ACB[0] (OUT) | CCU0/1 Comparison Mode | ATOM Output on Match |
|---|---|---|---|---|---|---|---|
| 0x00 | 0 | 0 | 0 | 0 | 0 | Serve First | OUT=No signal Change |
| 0x01 | 0 | 0 | 0 | 0 | 1 | Serve First | OUT=1 (if SL=0)/ OUT= 0 if (SL=1) |
| 0x02 | 0 | 0 | 0 | 1 | 0 | Serve First | OUT=0 (if SL=0)/ OUT= 1 if (SL=1) |
| 0x03 | 0 | 0 | 0 | 1 | 1 | Serve First | OUT=Toggle |
| 0x08 | 0 | 1 | 0 | 0 | 0 | Compare CCU0 only | OUT=No signal Change |
| 0x09 | 0 | 1 | 0 | 0 | 1 | Compare CCU0 only | OUT=1 (if SL=0)/ OUT= 0 if (SL=1) |
| 0x0A | 0 | 1 | 0 | 1 | 0 | Compare CCU0 only | OUT=0 (if SL=0)/ OUT= 1 if (SL=1) |
| 0x0B | 0 | 1 | 0 | 1 | 1 | Compare CCU0 only | OUT=Toggle |
| 0x0C | 0 | 1 | 1 | 0 | 0 | Compare CCU1 only | OUT=No signal Change |
| 0x0D | 0 | 1 | 1 | 0 | 1 | Compare CCU1 only | OUT=1 (if SL=0)/ OUT= 0 if (SL=1) |
| 0x0E | 0 | 1 | 1 | 1 | 0 | Compare CCU1 only | OUT=0 (if SL=0)/ OUT= 1 if (SL=1) |
| 0x0F | 0 | 1 | 1 | 1 | 1 | Compare CCU1 only | OUT=Toggle |
| 0x10 | 1 | 0 | 0 | 0 | 0 | Serve Last | [on CCU0 Match] OUT=No signal Change |
| 0x11 | 1 | 0 | 0 | 0 | 1 | Serve Last | [on CCU0 Match] OUT=1 (if SL=0)/ OUT= 0 if (SL=1) |
| 0x12 | 1 | 0 | 0 | 1 | 0 | Serve Last | [on CCU0 Match] OUT=0 (if SL=0)/ OUT= 1 if (SL=1) |
| 0x13 | 1 | 0 | 0 | 1 | 1 | Serve Last | [on CCU0 Match] OUT=Toggle |
| 0x14 | 1 | 0 | 1 | 0 | 0 | Serve Last | [on CCU0 Match]=>OUT No Change |
| 0x15 | 1 | 0 | 1 | 0 | 1 | Serve Last | [on CCU0 Match] OUT=1 (if SL=0)/ OUT= 0 if (SL=1) |
| 0x16 | 1 | 0 | 1 | 1 | 0 | Serve Last | [on CCU0 Match] OUT=0 (if SL=0)/ OUT= 1 if (SL=1) |
| 0x17 | 1 | 0 | 1 | 1 | 1 | Serve Last | [on CCU0 Match] OUT=Toggle |
| 0x18 | 1 | 1 | 0 | 0 | 0 | Serve Last | [on CCU1 Match] OUT=No signal Change |
| 0x19 | 1 | 1 | 0 | 0 | 1 | Serve Last | [on CCU1 Match] OUT=1 (if SL=0)/ OUT= 0 if (SL=1) |
| 0x1A | 1 | 1 | 0 | 1 | 0 | Serve Last | [on CCU1 Match] OUT=0 (if SL=0)/ OUT= 1 if (SL=1) |
| 0x1B | 1 | 1 | 0 | 1 | 1 | Serve Last | [on CCU1 Match] OUT=Toggle |
| 0x1C | 1 | 1 | 1 | 0 | 0 | Special | Stop ongoing Comparisons |

# GTM (Generic Timer Module)
# ATOM – Capture & Compare Strategy (SOMC)




- TBU_CH => [0, 0x00FFFFFF]
  - Time counter (CH0)
  - Angular counter (CH1/2)



# GTM (Generic Timer Module)
# ATOM – Capture & Compare Strategy (SOMC)

- If the comparison is >= (GE) and the

<CM_value> in **[TBU_CH_curr , (TBU_CH_curr+0x007FFFFF)%(0x00FFFFFF)]**

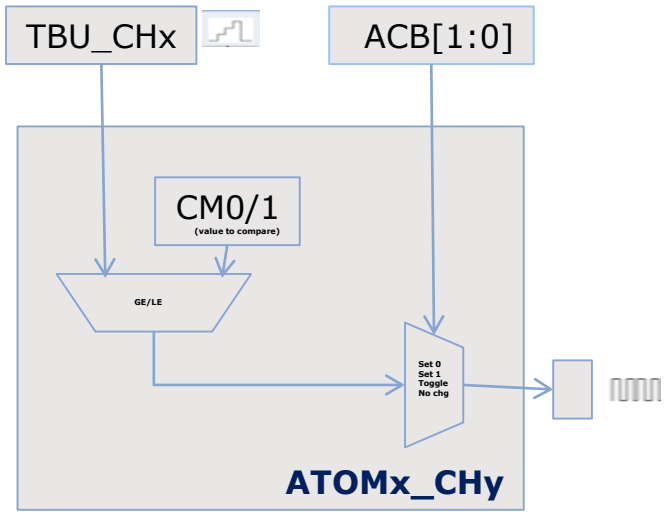
  - The event is considered in the "Future"
  - Otherwise it is consider to be in the past.

For instance:

- TBU_CH_curr=**0x007F00FF**,CM_value = **0x00800020**
- Δ = (0x00800020 - 0x007F00FF)= **0xFF21<0x007FFFFF**
  - The 0x00800020 is in the "future"

- TBU_CH_curr = **0x007F00FF**, CM_value= **0x000000AA**
- Δ = (0x1000000 - 0x007F00FF)+0x000000AA=>
  - D = **0x0080FFAB > 0x007FFFFF**
  - The 0x000000AA value is consider a "past" event

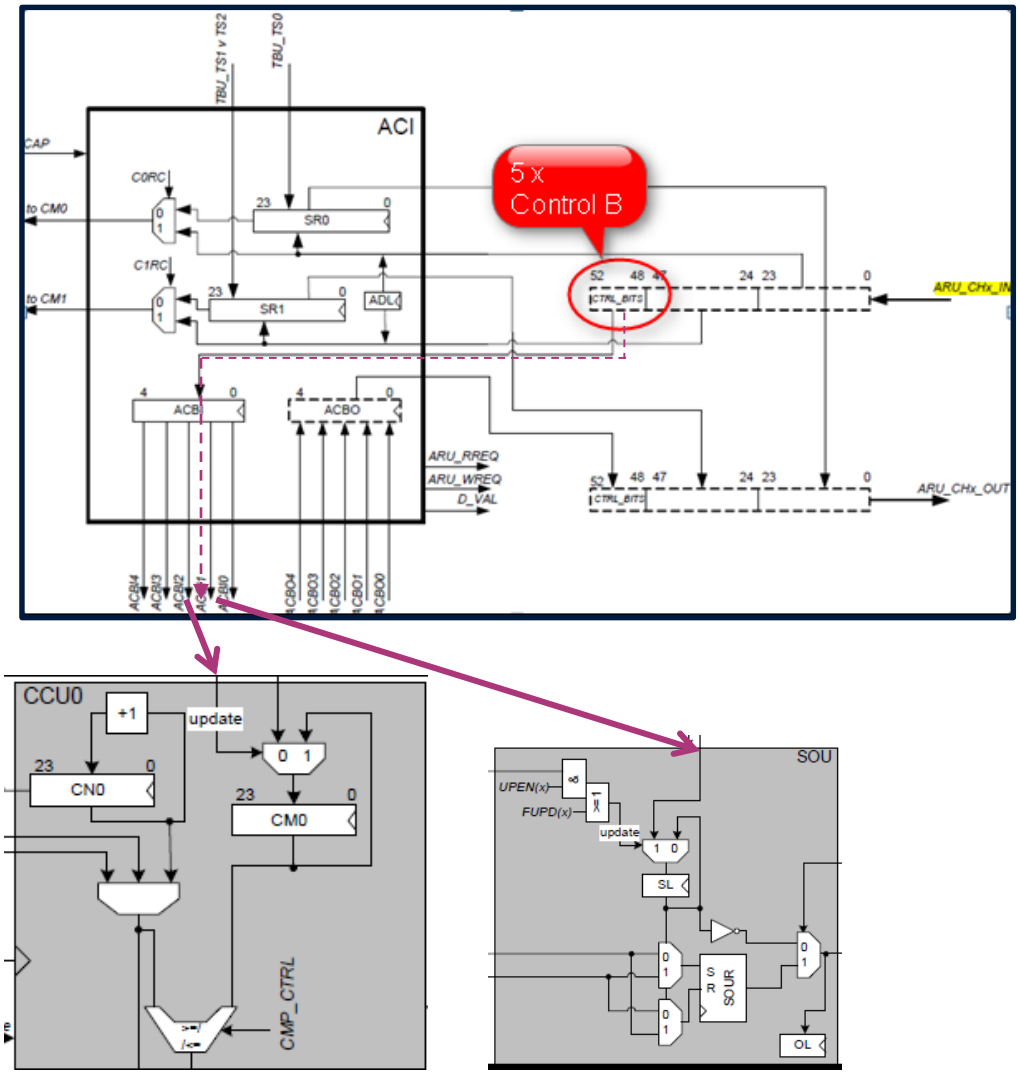
- TBU_CH_curr = **0x00FFAAFF**, CM_value = **0x000000AA**
- Δ = (0x1000000 - 0x00FFAAFF)+0x000000AA=>
  - D = **0x000055AA < 0x007FFFFF => "future Event"**



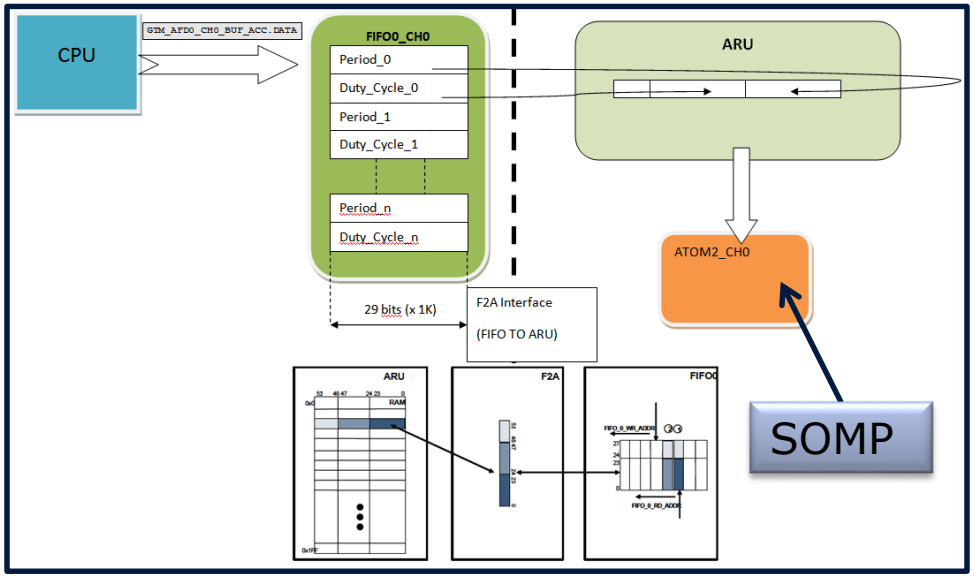
# GTM (Generic Timer Module)
# ATOM – ARU Communication Interface (ACI)

- **responsible for data exchange from/to ARU**
  - **communication is achieved with following SFRs**
    - SR0 & SR1 (24-bit)
    - ACBI & ACBO (5-bit)

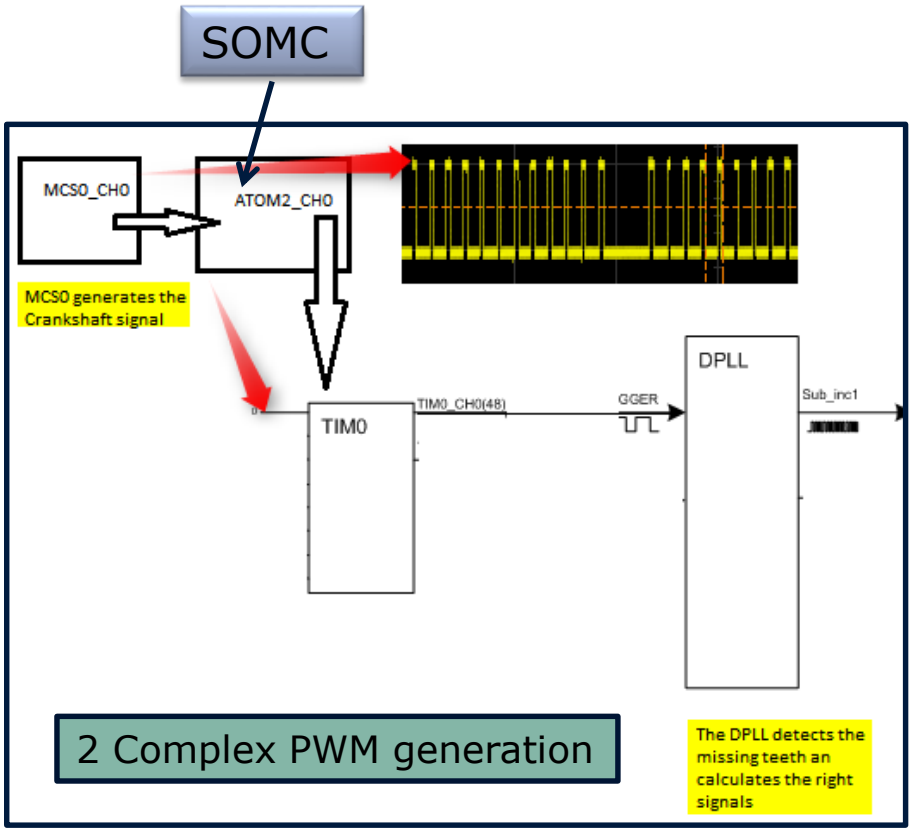
- The meaning of the ARU parameters depends on the ATOM operative mode.
  - In **SOMP** mode **ARU_CHx_IN** contains **duty cycle** an **period.**
  - In **SOMC** mode the ARU_CH_IN contains values to be compared using the ***control strategy (CCU0/CCU1)*** specified by the **CTRL_BITS**
  - Also the output behavior can be controlled with the CTRL_BITS (SOU).



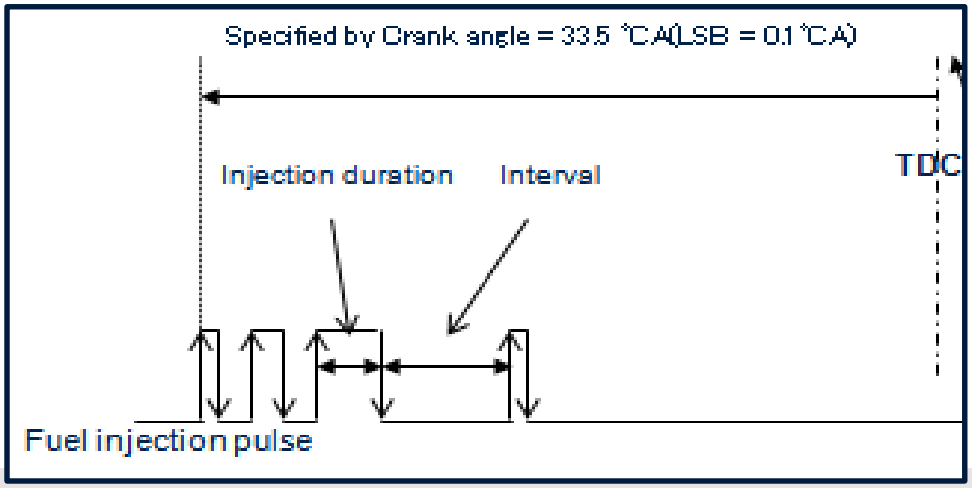
# GTM (Generic Timer Module)
# ATOM – examples




## 1 Flexible PWM Generation




## 3 Ignition/Injection pulses (MCS+DPLL+ATOM)



# AURIX2G
# ATOM Improvements

- (A)TOM trigger pulse generation SR0_TRIG
- (A)TOM up-down counter mode UD_MODE
- (A)TOM extended clock source ECLK_SRC for CN0:
  *TRIG_[x-1]* and *TIM_EXT_CAPTURE(x)* as clock signal for CN0
- (A)TOM freeze mode FREEZE:
  no change of output *(A)TOM_CH(x)_OUT* if channel is enabled/disabled
- ATOM SOMC/SOMB extended update mode EUPD

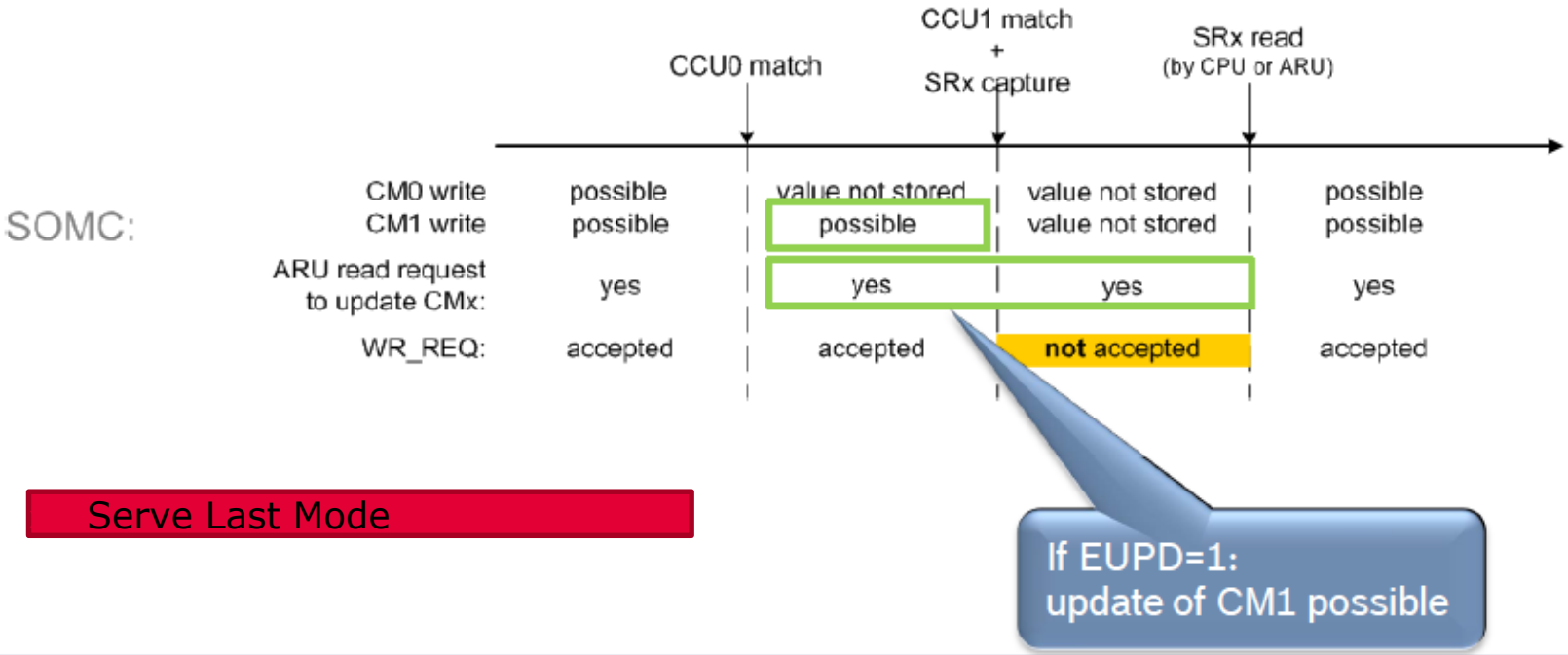
# AURIX2G Improvements (SOMB)

- ATOM Signal Output Mode Buffered Compare
  - Similar to SOMC

In ATOM Signal Output Buffered Compare (**SOMB**), the ATOM channel generates an output signal on behalf of time stamps that located in the ATOM operation registers. These time stamps are compared with the time stamps, the TBU generates. The ATOM is able to receive new compare values either by CPU or via the ARU. The new compare values received via ARU are stored first in the shadow register and only if previous compare match is occurred, the operation register are updated with the content of the shadow register.

# ATOM SOMC/SOMB extended update mode

- ATOM SOMC mode:
  - update of CM1 after CCU0 compare match
  - ARU read request is continued



# Agenda

1. GTM Overview
2. CTBM-Clock & Time Base Management
3. TIM-Timer Input Module
4. ARU-Advanced Routing Unit
5. TOM-Timer Output Module
6. ATOM-ARU connected Timer Output Module
7. DTM-Dead Time Module

# GTM (Generic Timer Module)
# DTM (Dead Time Module)

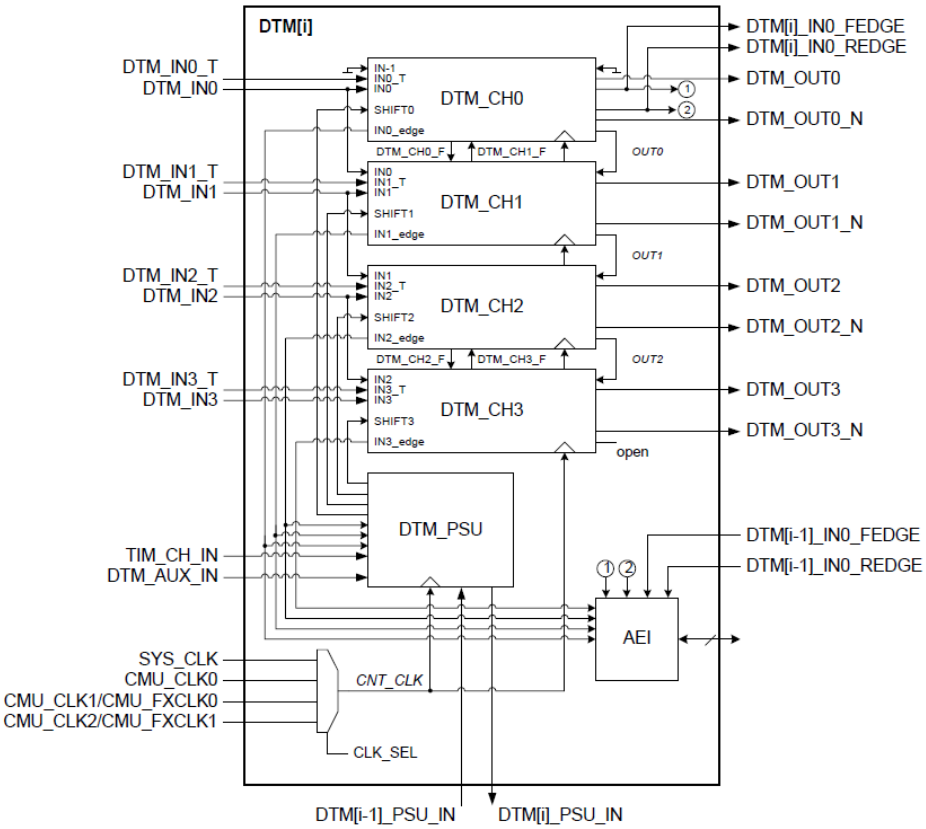
**1. Dead-Time Generation**
Generate the inverted signals with programmable dead-time.

- TOM/ATOM → DTM_IN0 → DTM_OUT0_N
- TOM/ATOM → DTM_IN1 → DTM_OUT1_N
- TOM/ATOM → DTM_IN2 → DTM_OUT2_N
- TOM/ATOM → DTM_IN3 → DTM_OUT3_N

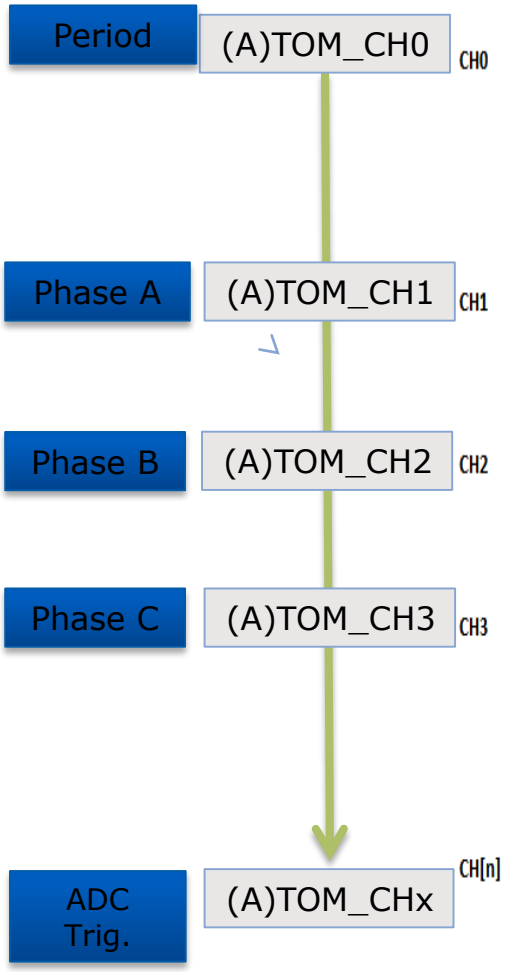
**2. Phase-shift**.
Set the output of one channel to the value of the preceding channel (TIM_CH_IN Trigger or DTM_AUX_IN)

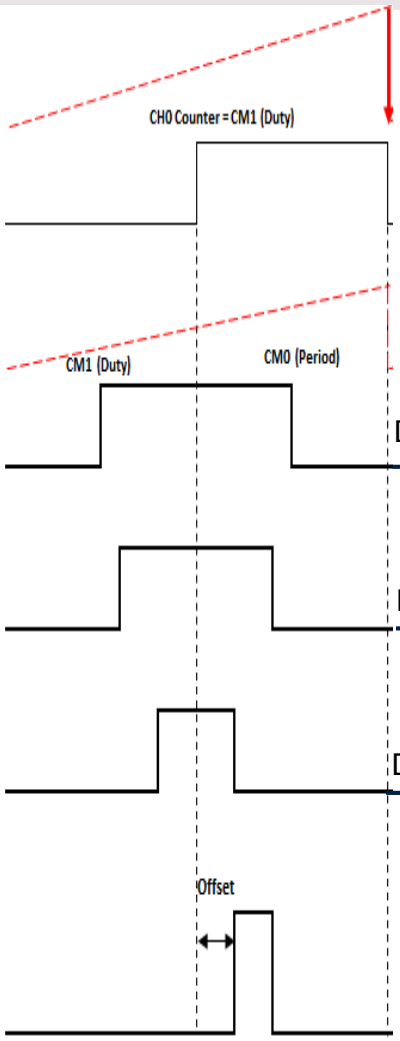
**3. (N)AND/(N)OR/X(N)OR** combine the DTM_IN[x] inputs with TIM_CH_IN or DTM_AUX_IN

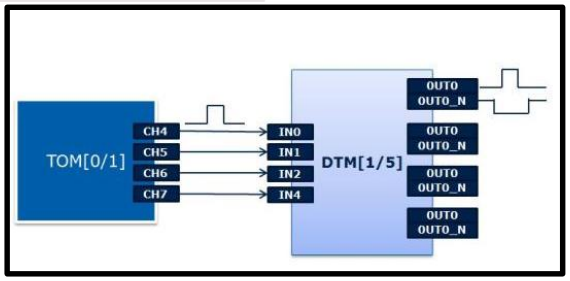
4. **Pulse Generation On Edge**

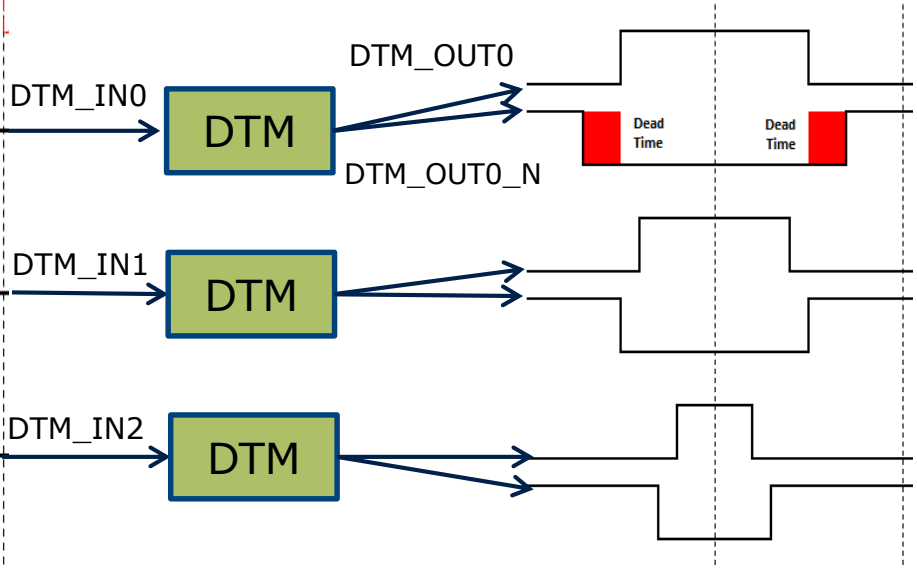


# DTM (Dead Time Module) – TC22x/23x and AURIX2G (3)



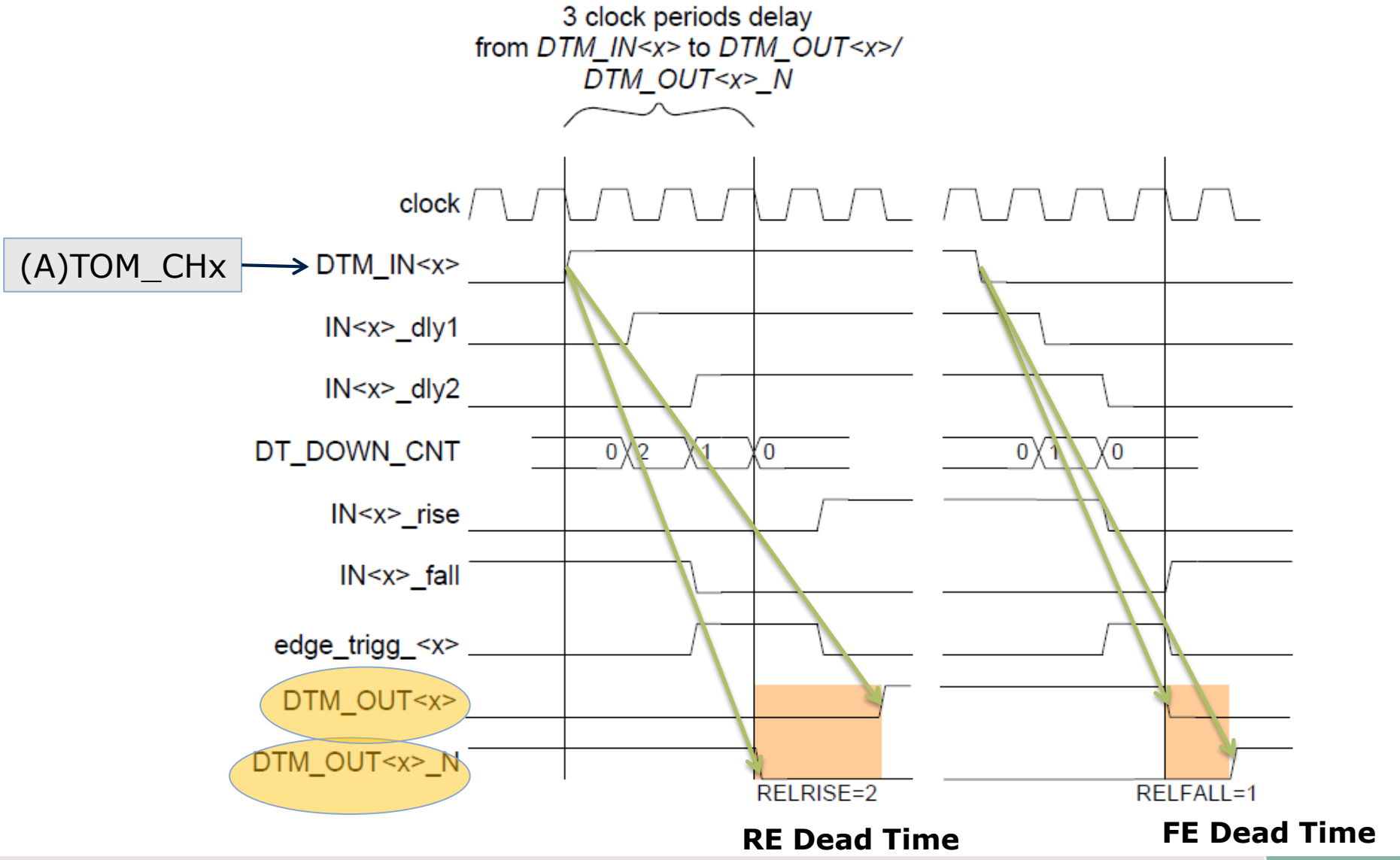



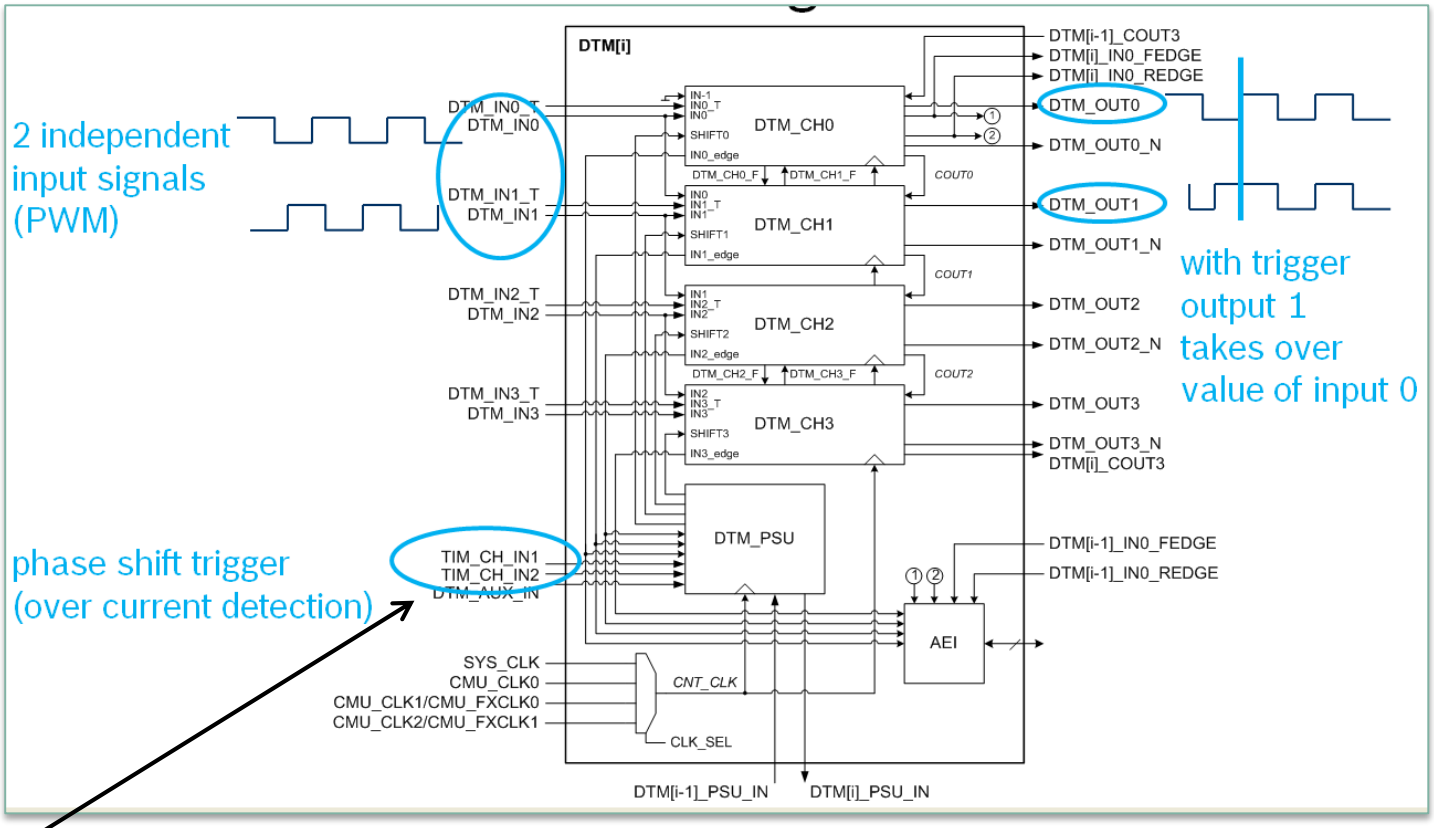




| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| P02.0 | TIN0 | TOUT0 | TIM0_0 | Reserved | TOM0_8 | TOM1_8 | TOM0_4 | TOM1_4 |
| P02.1 | TIN1 | TOUT1 | TIM0_1 | Reserved | TOM0_9 | TOM1_9 | TOM0_4N | TOM1_4N |
| P02.2 | TIN2 | TOUT2 | TIM0_2 | Reserved | TOM0_10 | TOM1_10 | TOM0_5 | TOM1_5 |
| P02.3 | TIN3 | TOUT3 | TIM0_3 | Reserved | TOM0_11 | TOM1_11 | TOM0_5N | TOM1_5N |

# DTM (Dead Time Module)



# DTM (Dead Time Module)
# Phase Shifting

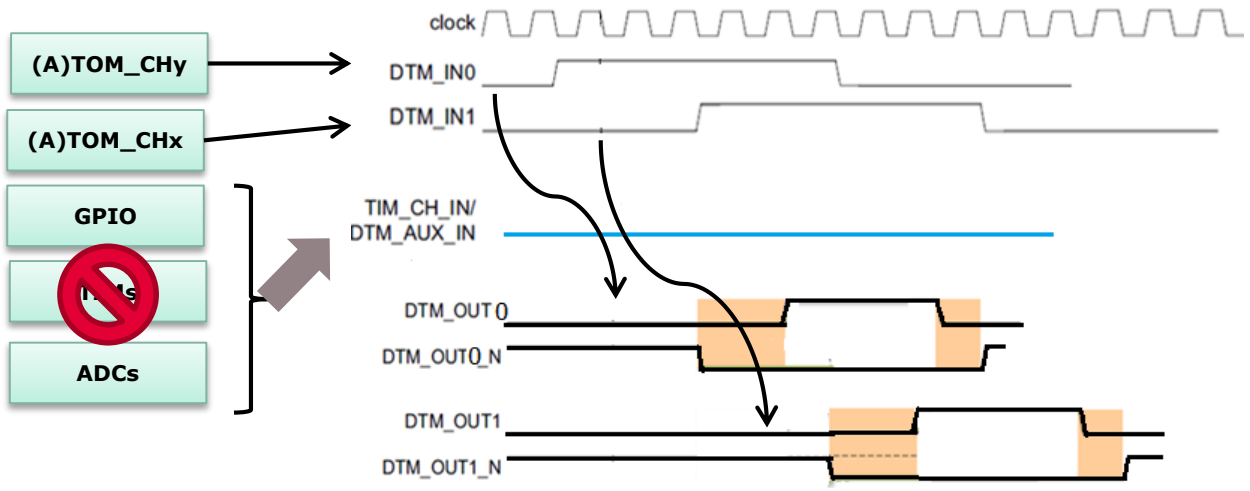



› If No Trigger applied (‘0’):
  – input signal DTM_IN0 is forwarded to output DTM_OUT0
  – input signal DTM_IN1 is forwarded to output DTM_OUT1

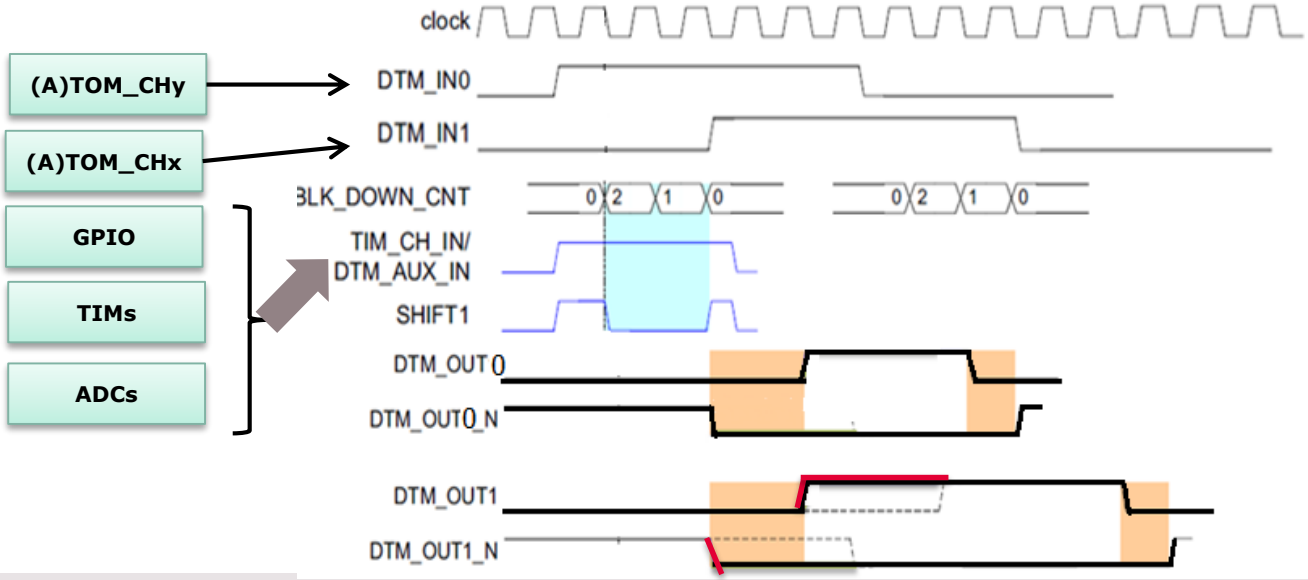
› If phase shift trigger is active (=‘1’),
  – the input signal DTM_IN0 is continued to be forwarded to output DTM_OUT0
  – **the input signal DTM_IN0 is now also forwarded to output DTM_OUT1**.

(The outputs DTM_OUTx_N have no special meaning in this application context)

# DTM (Dead Time Module)
# How DTM Phase Shifting works 2/2




- In case of No triggers, the outputs are generated as expected
- DTM_IN0 => DTM_OUT0/0_N
- DTM_IN1 => DTM0_OUT1/1_N

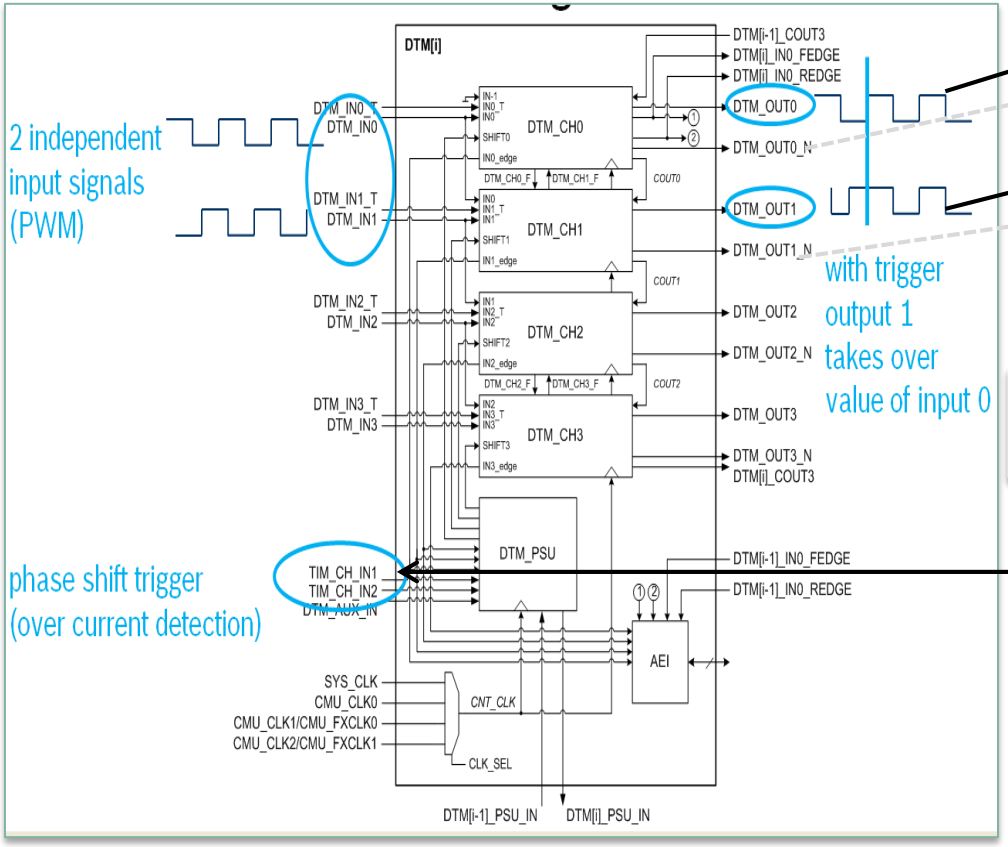


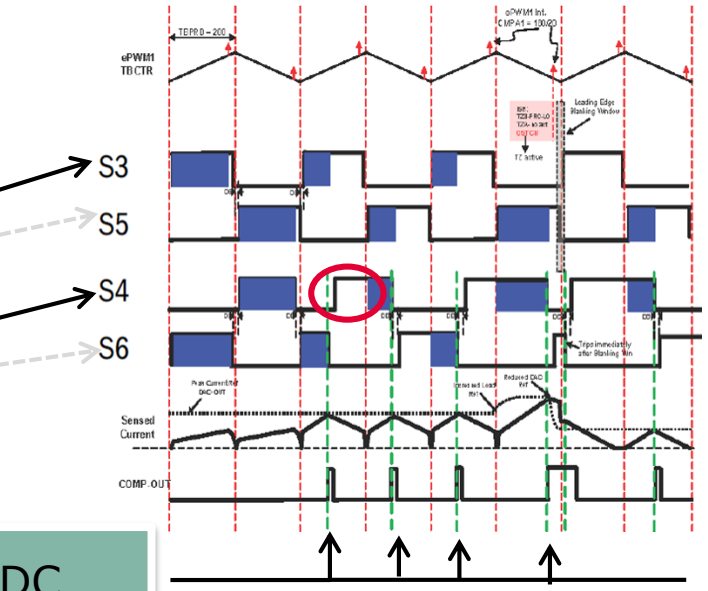

- In case of trigger,

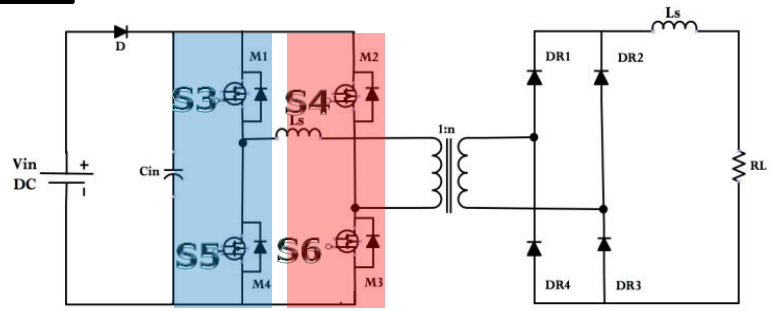
the outputs of DTM_OUT1 will take the DTM_OUT0 value, until the next DTM_IN0 edge

# Controlling Zero Voltage Switched Full Bridge (ZVSFB) Converter – Control Signals

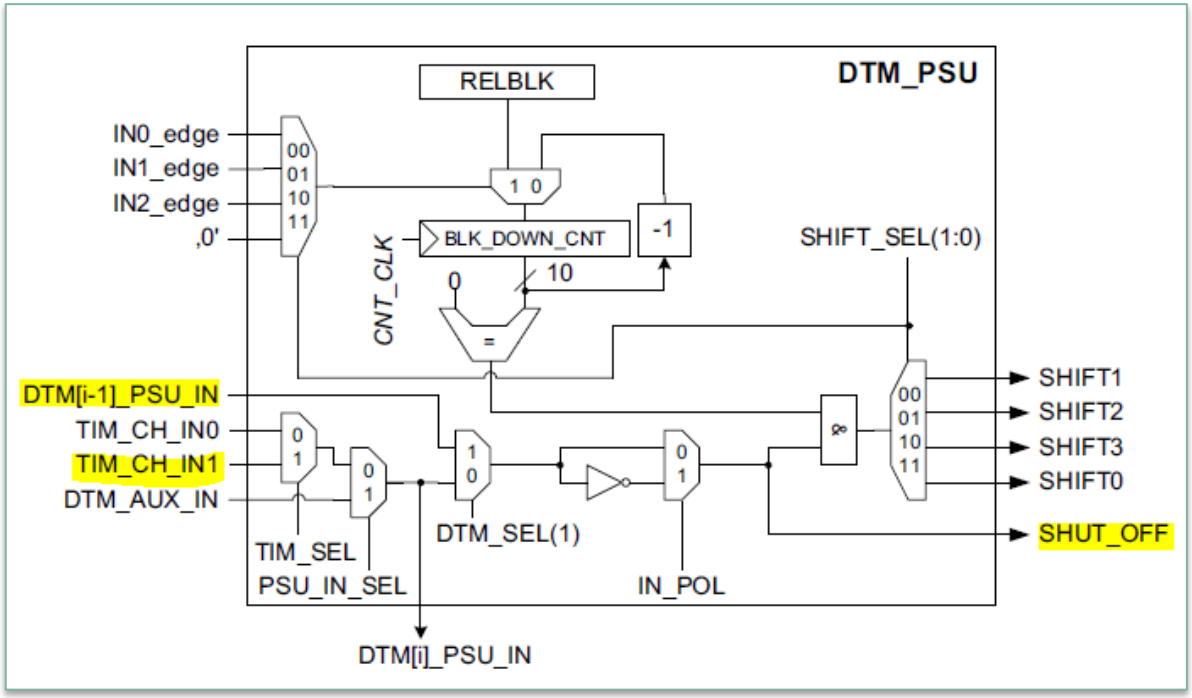
› When the current is above the threshold, the ADC Triggers the DTM to align the S4 phase to S3, until the next S3 edge!



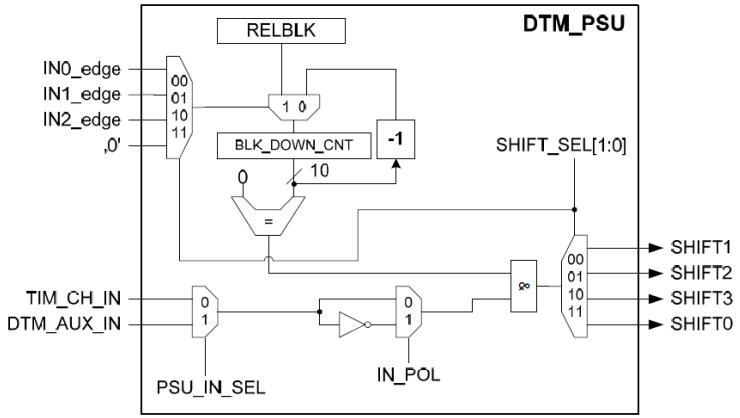



# AURIX2G
# DTM Improvements (Phase Shift Ctrl Unit)




› AURIX1G

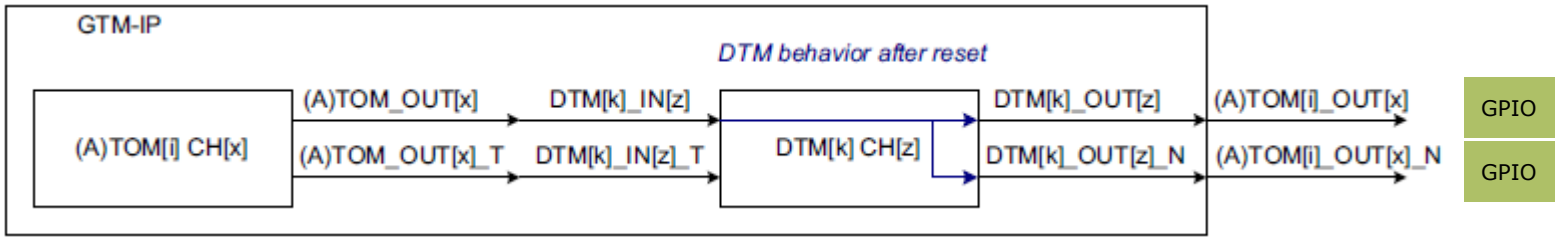


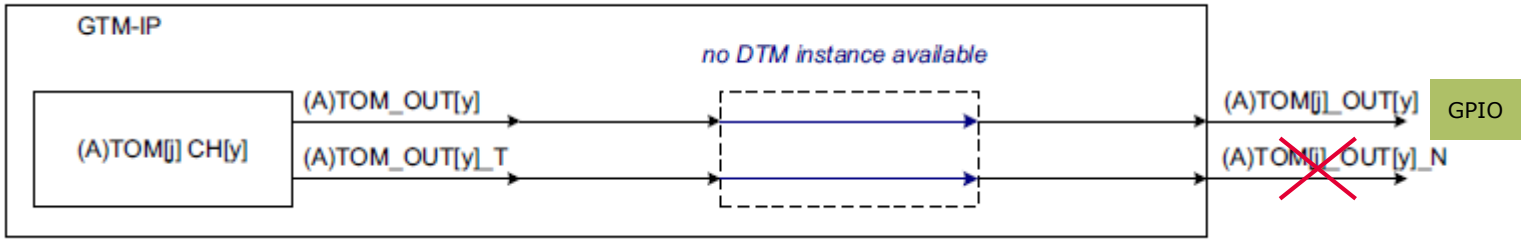
# AURIX2G
# DTM Improvements (Output Shut Off)

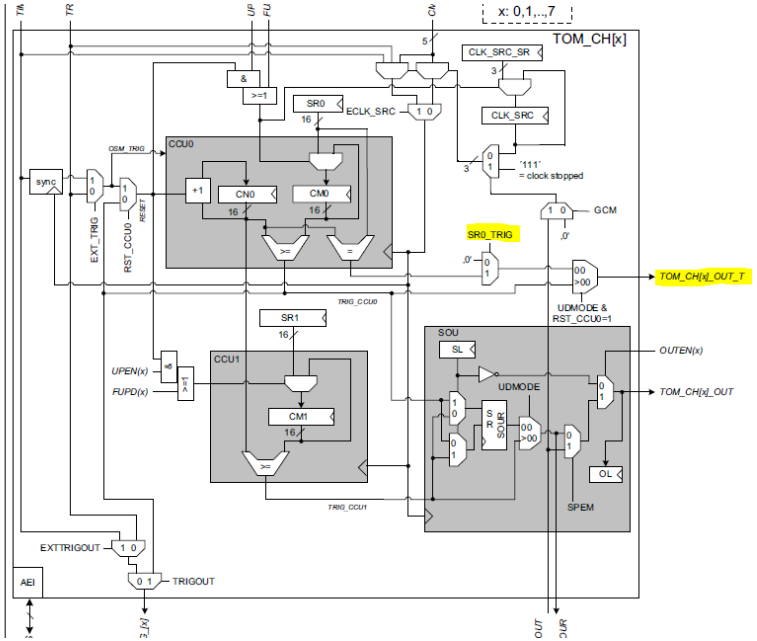
### 1.14.6 DTM output shut off

A fast shut off for the eight outputs of DTM instance i can be triggered by one of the two assigned inputs TIM[n]_CH_IN or DTM[i]_AUX_IN or the two inputs TIM[m]_CH_IN or DTM[i-1]_AUX_IN of the previous DTM instance i-1. The selection of the trigger signal source is done by the bits **PSU_IN_SEL** and **DTM_SEL(1)** (see **Figure 1-95**). The selected trigger signal is named *SHUT_OFF*.

# AURIX2G
# (A)TOM without DTMs



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