AURIX 2G ADAS Peripherals Overview

IFCN ATV SMD GC SAE MC

Agenda

1. AURIX™ - Radar family overview
2. LVDS Interface between MMIC and MCU
3. Radar Signal processing unit: SPU
4. Radar use case example based on SPU concept

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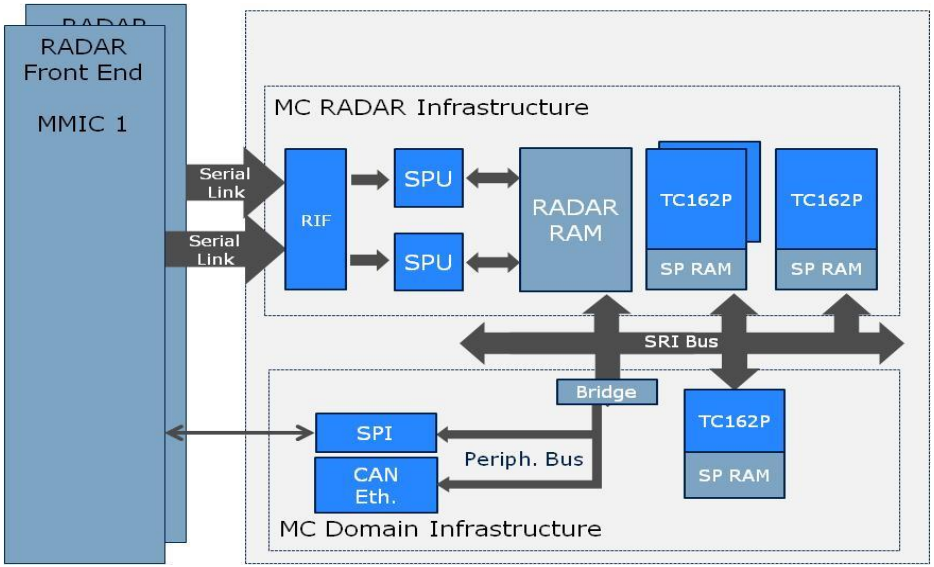
AURIX 2nd Generation

Scalable Radar Controller Family



TC39xX/QA
4x300MHz
10MB/5184kB
2xSPU

- Premium 77/79 GHz long-range RADAR
- Functional safe datafusion controller
- Autonomous vehicles control

TC35xTA
3x300MHz
4MB/2720kB
2xSPU

- Standard 77/79GHz long-range RADAR with up to 8 receive channels
- Standard 77/79GHz medium-range RADAR

TC33xDA
2x200MHz
2MB/1472kB
1xSPU

- Standard 77/79GHz medium-range RADAR with up to 4 receive channels
- Standard 24GHz short-range RADAR

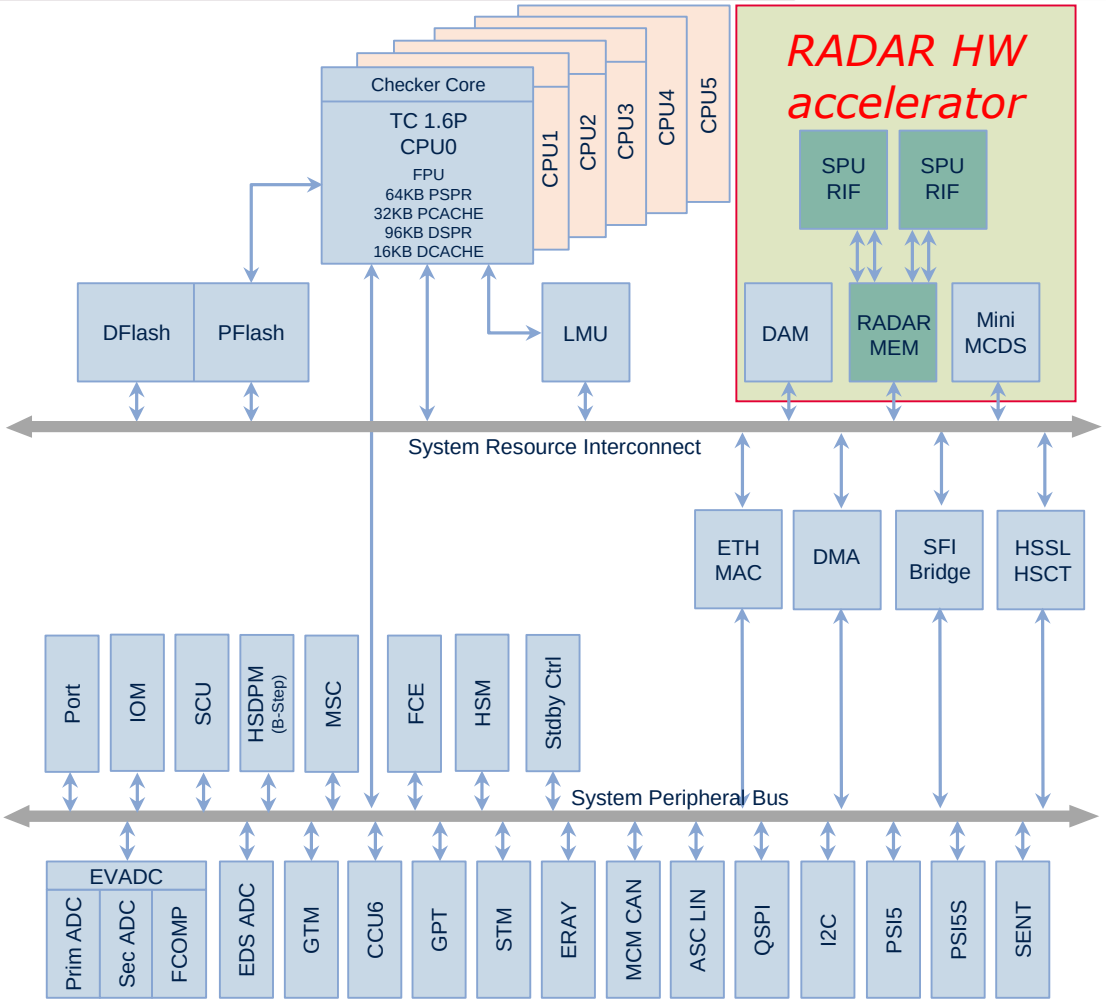
AURIX 2nd Gen. RADAR Controller

- Part of *Infineon 2-chip system solution* for next generation sensors
- *2nd generation* of high-performance multi-core microcontrollers
- *Scalable portfolio* of 3 package-/pin-compatible device classes
- New *RADAR-specific signal processing engine* (SPU)
- 400Mbit/s *fully digital interface* to Infineon RF front-end
- ISO26262 *ASIL-D chipset concept* with aligned safety measure
- Support of latest hardware security standards

AURIX™– TC39xXA - ADAS

6 cores/4 lockstep cores

Feature Set		9x Series (16MB) + ADAS
TriCore 1.6	# Cores / Checker	6/4
	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	2xSPU
Flash	Program Flash	16MB
	Data Flash (physical/logical)	1024/512kB
SRAM	DMI , PMI, LMU, AMU + RADAR MEM	2496kB + 4MB
DMA	Channels	128 + 24 (incl. move engines) ADAS DMAs
ADC	Converters Primary / Sec / FC / DS	8/4/8/14
	Channels Primary / Sec / FC / DS	64/64/8/14
Timer	GTM TIM / (A)TOM / MCS	94 / 192 / 10
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	2 /4
	CAN-FD / TT	12/1
	QSPI / ASCLIN / I2C	6 /8/2
	SENT / PSI5 / PSI5S	25/4/1
	HSSL / MSC / EBU	1/4/1
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	12x400MBit LVDS (RIF)
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292 **LFBGA 516**

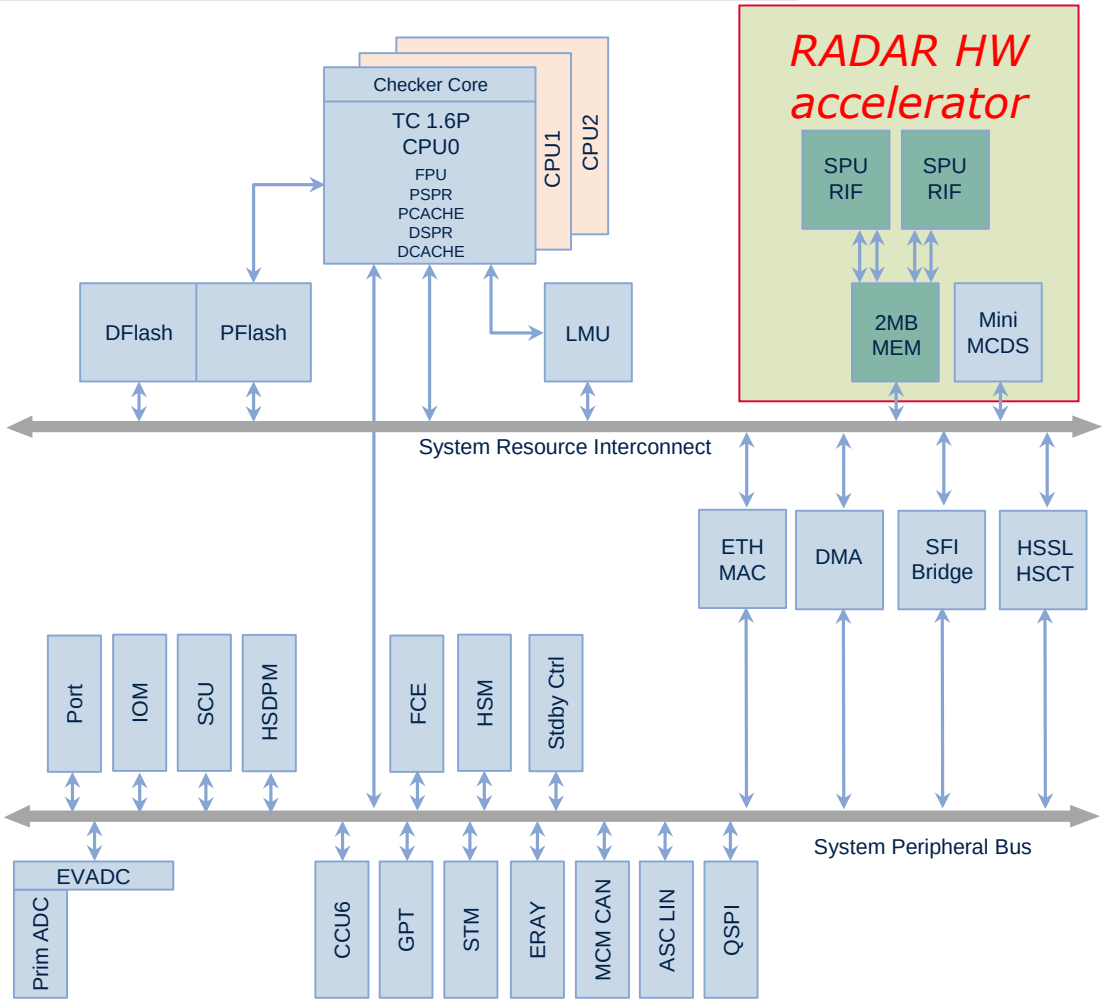
High temperature devices available on request
High performance sign off under evaluation >300MHz

preliminary - subject to change

AURIX™– TC35xTA - Series ADAS

3 cores/2 lockstep cores

Feature Set		5x Series ADAS (4MB)
TriCore	# Cores / Checker	3/2
1.6	Frequency	300MHz
Accelerator	Signal processing Unit (SPU)	2xSPU
Flash	Program Flash	4MB
	Data Flash (single ended)	128kB
SRAM	DMI , PMI, LMU, AMU + RADAR MEM	2720kB
DMA	Channels	64
ADC	Converters Primary / Sec / FC / DS	2/0/0/0
	Channels Primary / Sec / FC / DS	16/0/0/0
Timer	GTM TIM / (A)TOM / MCS	-
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	6/0
	QSPI / ASCLIN / I2C	4/4/0
	SENT / PSI5 / PSI5S	0/0/0
	HSSL / MSC / EBU	0/0/0
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	12x400Mbps LVDS
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292

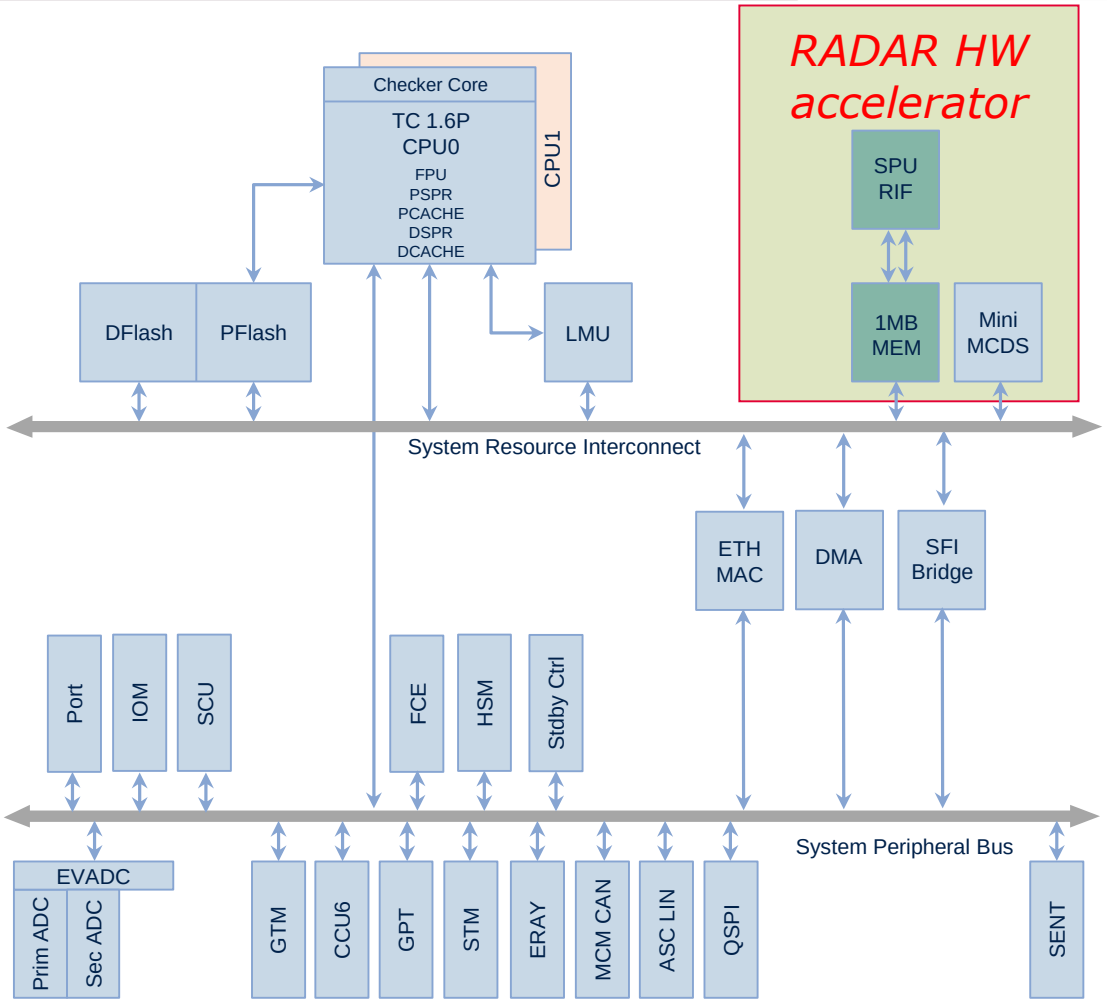
High temperature devices available on request

preliminary - subject to change

AURIX™– TC33xDA - Series ADAS

2 cores/1 lockstep core

Feature Set		3x Series ADAS (2MB)
TriCore 1.6	# Cores / Checker	2/1
	Frequency	200MHz
Accelerator	Signal processing Unit (SPU)	1xSPU
Flash	Program Flash	2MB
	Data Flash (single ended)	256kB
SRAM	DMI , PMI, LMU, AMU + RADAR MEM	1472kB
DMA	Channels	16
ADC	Converters Primary / Sec / FC / DS	4/2/0/0
	Channels Primary / Sec / FC / DS	>16/32/0/0
Timer	GTM TIM / (A)TOM / MCS	16 / 32 / 0
	CCU / GPT modules / bit streaming	2/1/1
Interfaces	FlexRay (#/ch.)	1/2
	CAN-FD / TT	6/0
	QSPI / ASCLIN / I2C	4/6/0
	SENT / PSI5 / PSI5S	6/0/0
	HSSL / MSC / EBU	0/0/0
	Ethernet 100Mbps/1Gbps	1/1
	RADAR /ext. ADC IF (RIF)	6x100Mbps LVDS
Security	HSM	HSM+ECC256
Safety	SIL Level	ASIL D
Power	EVR	Yes (3.3V/5V)
	Standby Control Unit	yes



Package Variants

LFBGA 292

TQFP 144

High temperature devices available on request

preliminary - subject to change

Optimized Chipsets Solution for Next Generation Radar Systems

Scalability, performance, functional safety

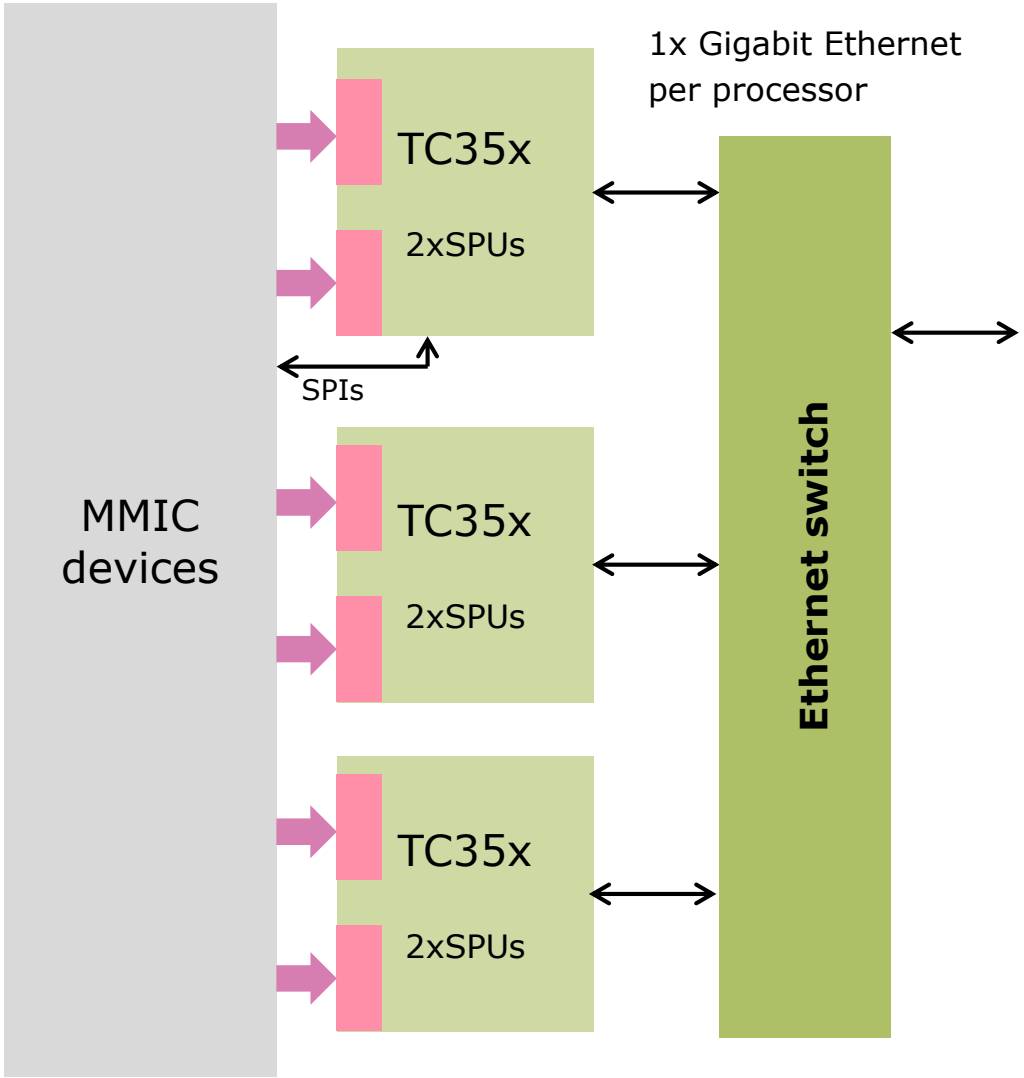
- **Long-Range (ACC)**
  4 TX / 8 RX

- **Mid-Range (AEB)**
  3 TX / 4 RX

- Short-Range (BSD)
  1 TX / 2 RX

High resolution Radar using AURIX-SPU

- 1 processor per 8x Rx channels
- High speed interprocessor com. using Gigabit Ethernet
- Each AURIX-SPU does signal preprocessing and data reduction
- Only FFT peaks are sent over Ethernet
  - Tracking, confirmation, classification is done centrally



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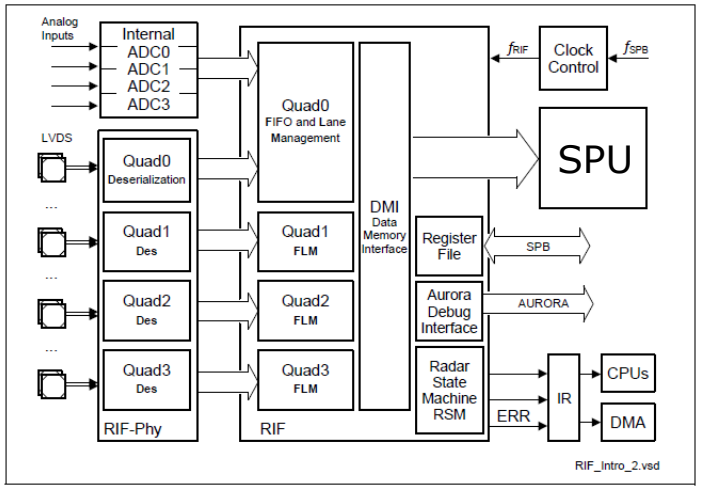
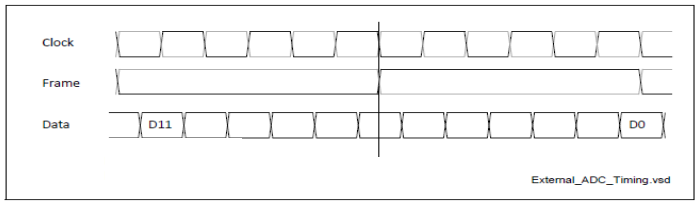
Standardized LVDS Interface proven standard used for RIF IF

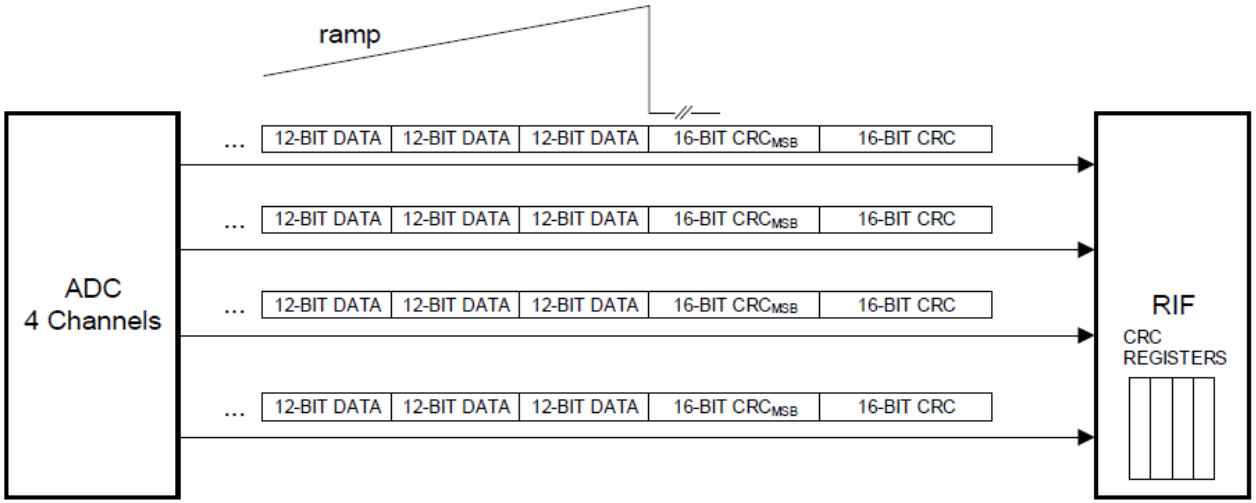
- IEEE 1596-3 General Purpose Link (1996)
- High Speed Standardized Interface
  - Proven standard/protocol for analog frontends
    - Clock Signal
    - Frame Signal
    - 4 x Data lanes
  - Already in use in automotive industry
    - TI ADS5240, AD AD9637
- Very simple protocol:
  - Simpler deserialization as using framing signal
    - 2x smaller logic
  - Simpler bus interface unit as side band information managed by SPI communication
    - 2x smaller interface unit
  - Protected with CRC32
- Scalable: up to 8 Data lanes @400Mbit/s per lane
- Supports on-the-fly ADC Data Deinterleaving





Data Integrity

- On the Fly CRC calculations
  - Calculated using Ethernet 32-Bit CRC 0x04C1 1DB7



- Interrupt triggered on CRC errors
- Communication Robustness
  - 250mV to 400mV (instead of 140 to 270mV) voltage swing
  - 1.2V (instead of 0.2V) voltage offset

  -> Less sensitive to interference

Data Security

- To ensure data transmit quality skew on LVDS channels can be programmed
- In case of Hack, skew parameters will be changed
- To protect the interface, skew calibration parameters can be saved in a secure NVM protected by HSM (Hardware Security Module

Field	Bits	Type	Description
VALUE	[7:0]	rw	**Calibration Word Configuring the Delay Lines** Reset value will be determined by digital simulation. The reset value shall be overwritten by the tester for each quad and remains constant for the life time of the chip. ENDINIT protected.
ACC	8	rw	**Calibration Accuracy** Contains the accuracy of the calibration procedure regarding the target define in the VALUE bit field. 0_B +-1 1_B +-2
CALRESULT	[23:16]	rh	**Calibration Word Resulting from Production Tester Calibration** Contains the result from the latest calibration sequence.
0	[31:24], [15:9]	r	**Reserved** Read as 0; should be written with 0.

Infineon Patent Pending

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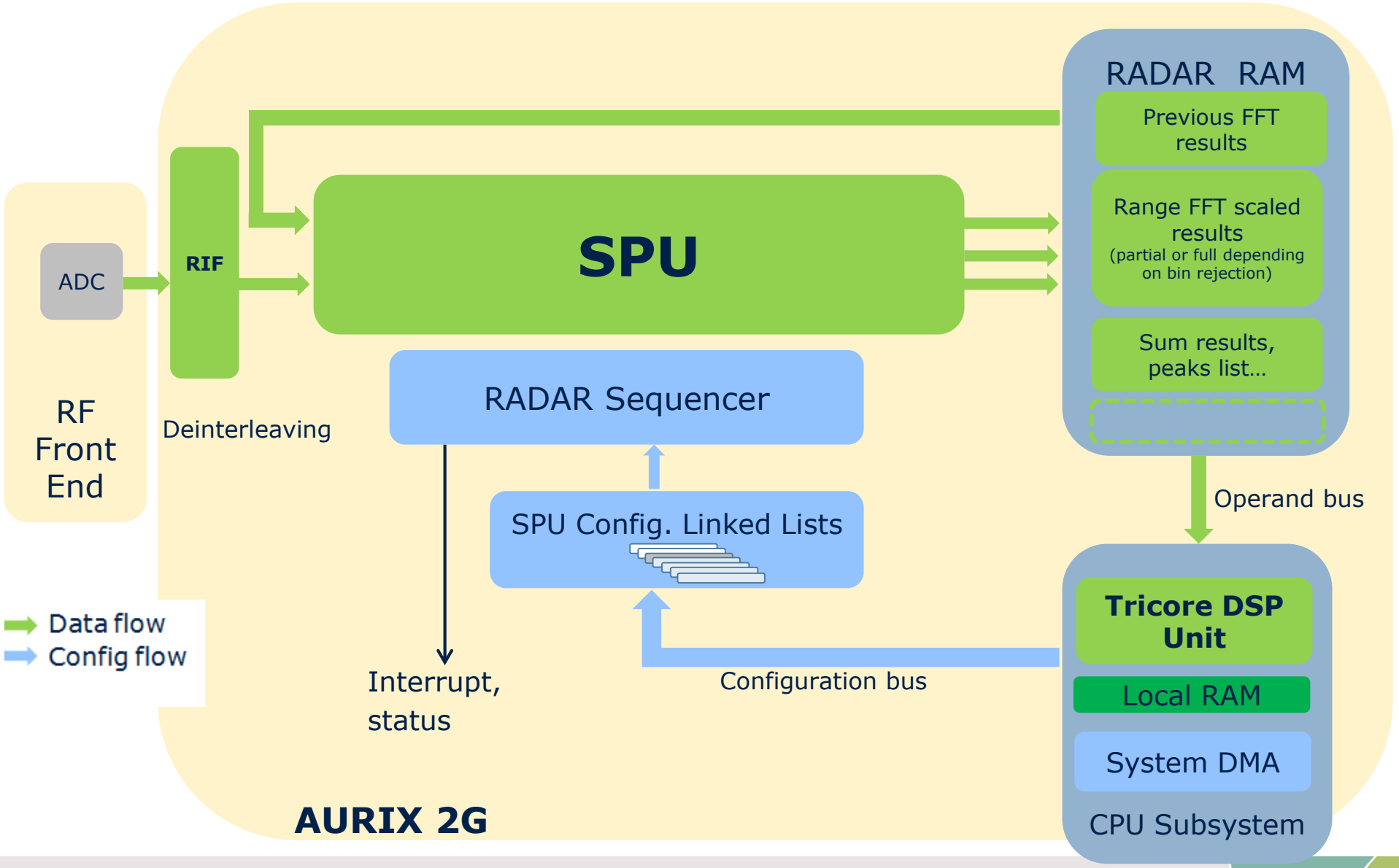
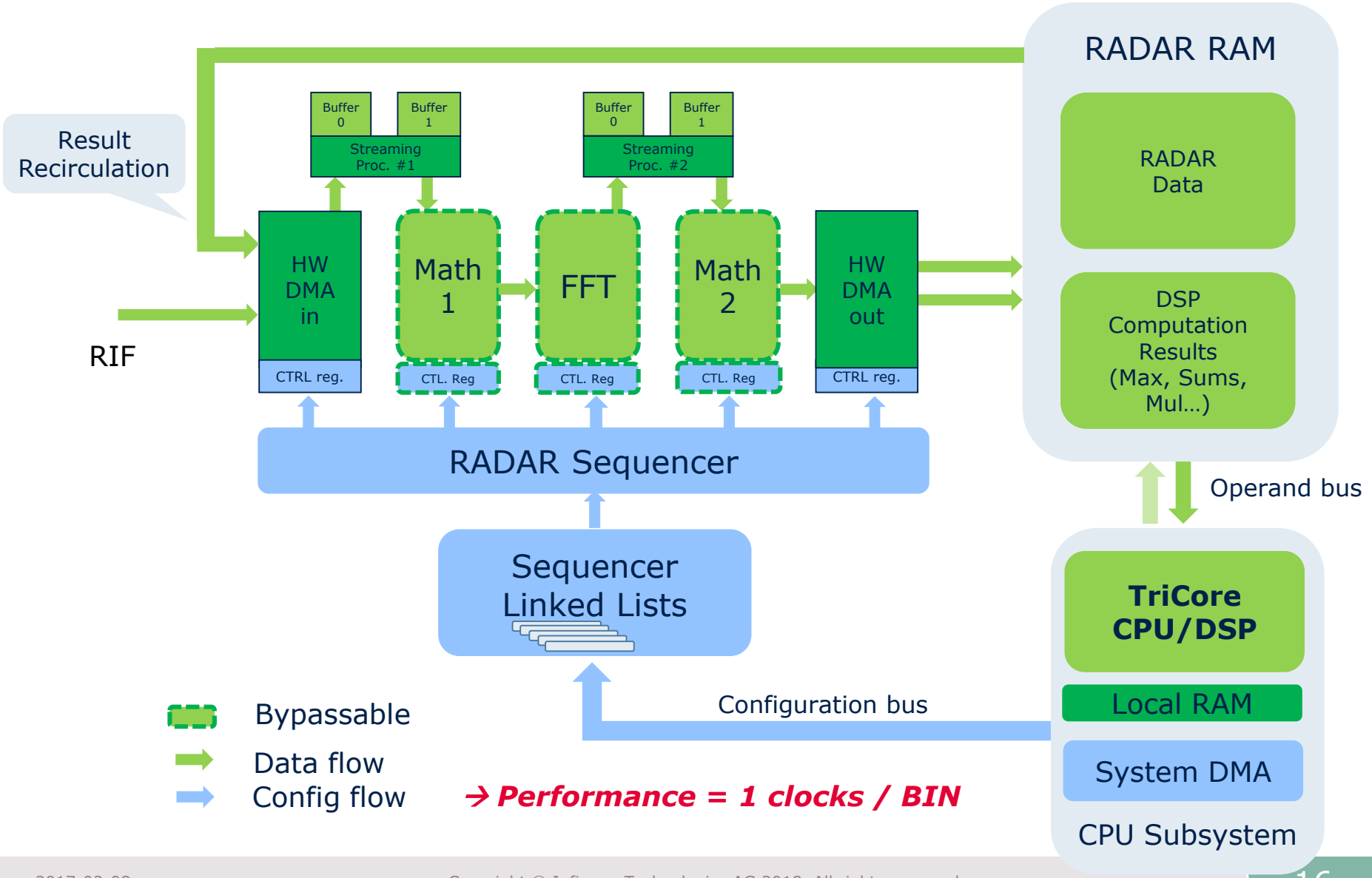
AURIX 2G RADAR family
Configurable RADAR signal processing unit

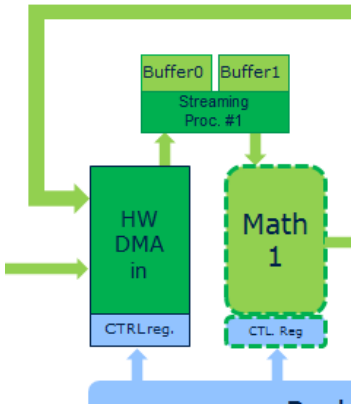


AURIX 2G RADAR family
SPU system overview

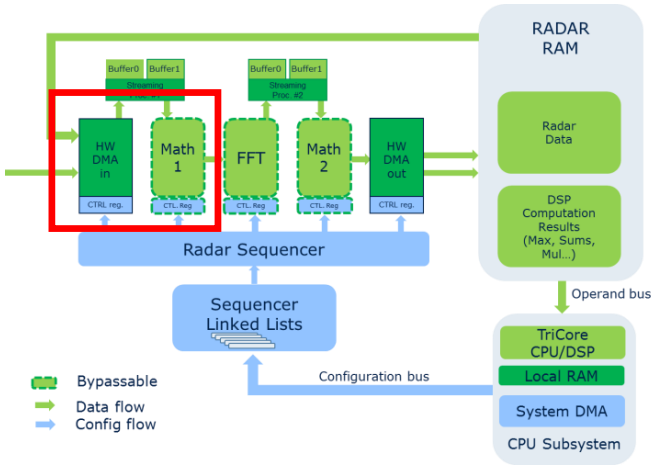


Input HW DMA

- 2 alternative data sources:
  - ADC conversion results
  - Radar RAM



- Implements inner loop, outer loop, sample loop
  - Fully configurable base address, inner loop increment and outer loop increment
  - Configured by Radar sequencer



- 3D DMA
  - Integrated Seamless Transposition
  - MIMO support: seamless multi data cube processing

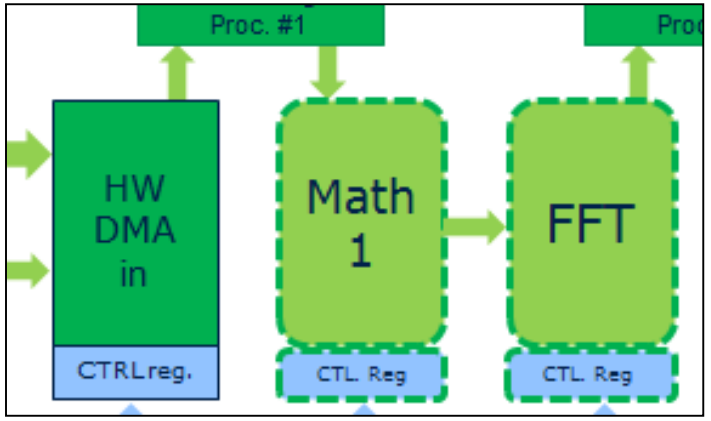
Math1 Unit detailed overview usage on demand

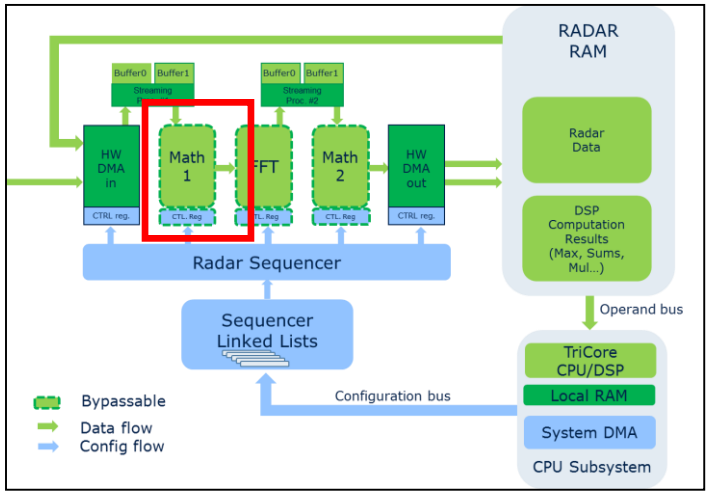
- Bypassable unit/ on demand

- Complex/Real based Math1:
  - Configured by RADAR sequencer
  - Complex vector multiplication
  - Complex windowing
  - Multiple antenna support
  - Support for modulation schemes

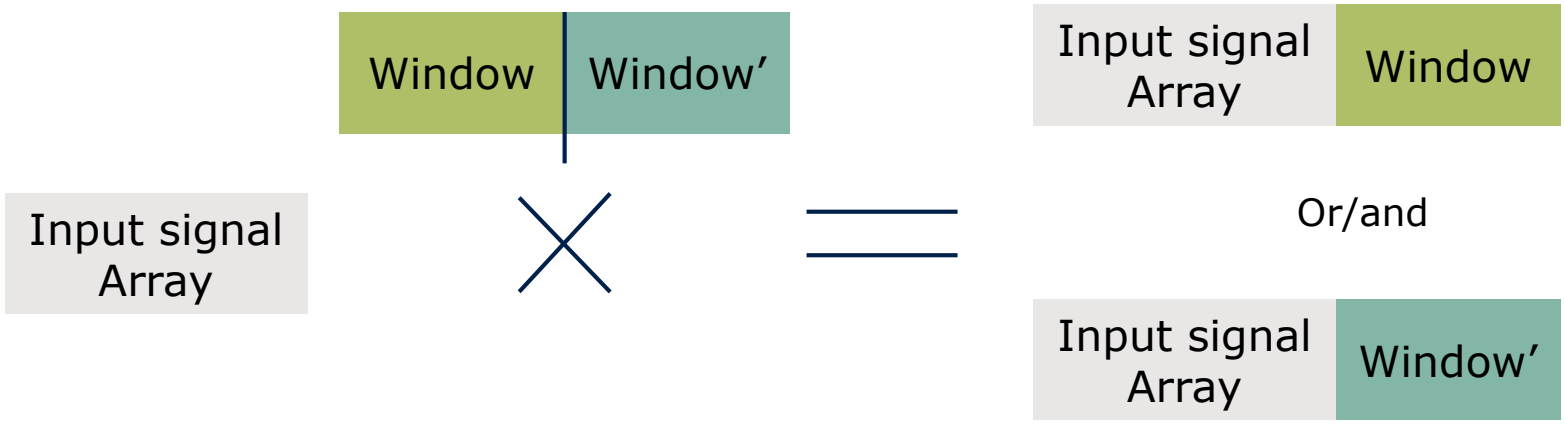
  - Equivalent to 2 complex multiplications followed by complex windowing

→ Performance = 1 clocks / BIN





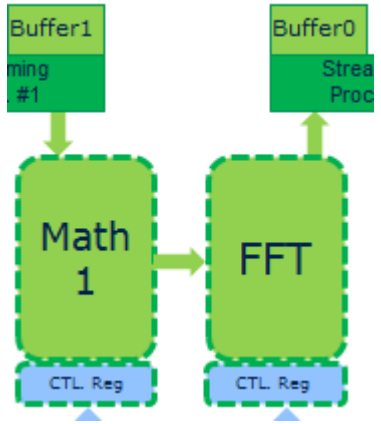
Complex multiplication
RAM based vector multiplication for maximum flexibility

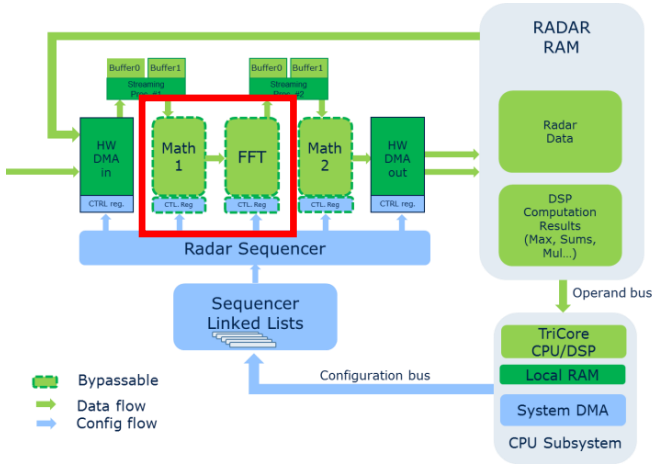


- Vector Complex multiplication:
  - Calculates: $(a_n+ib_n)*(c_n+id_n)=(a_nc_n-b_nd_n)+i(a_nd_n+b_nc_n)$
    - (a+ib) is the input sample, can be real or complex
    - (c+id) is the mul. coeff. ,can be real or complex
  - Sets of coeff. are pre calculated and loaded at run time in a dedicated fast RAM
  - 1 coefficient per bin
  - 1 set of coefficient per FFT
  - 1 weight per Antenna
  - ability to toggle between 2 sets of coefficient
    - each Ramp
    - each FFT

FFT unit

- Bypassable stage
- HW accelerator
  - 1 clocks / BIN
- Configured by Radar sequencer
  - FFT type (Real, Complex)
  - FFT length (4 up to 2048)
  - FFT precision (16bits) or 32bits)
  - In Place FFT support (for second stage FFT)





Performance = 1 clocks / BIN

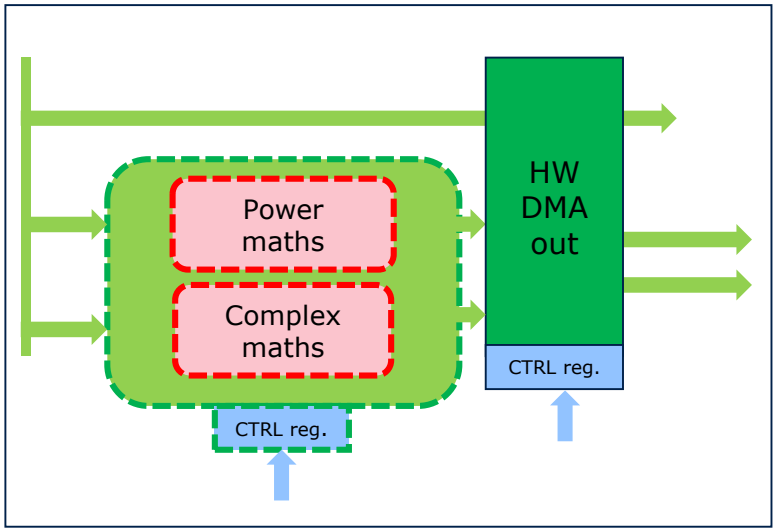
Math2 Unit detailed overview usage on demand

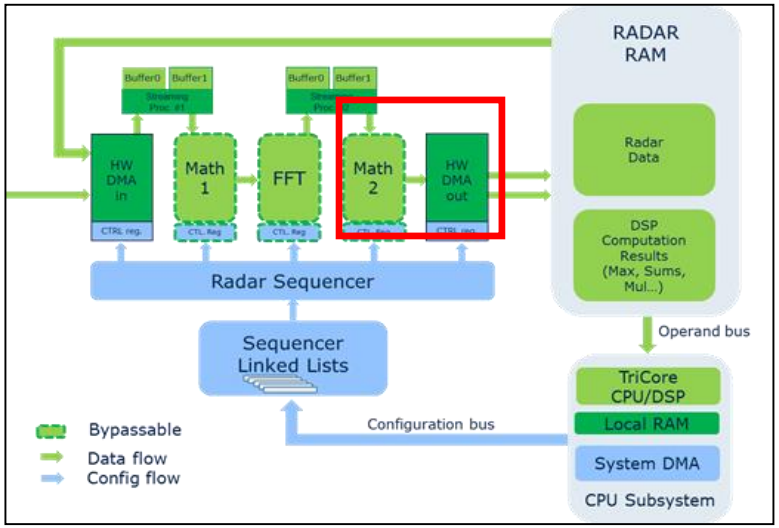
- Bypassable unit/on demand
- 2 main data paths
  - Signal power
    - Linear power (R^2+I^2)
    - Log_2 Power
    - Magnitude Approximation

$$\alpha \times (MAX(ABS(I), ABS(Q))) + \beta \times MIN(ABS(I), ABS(Q)))$$

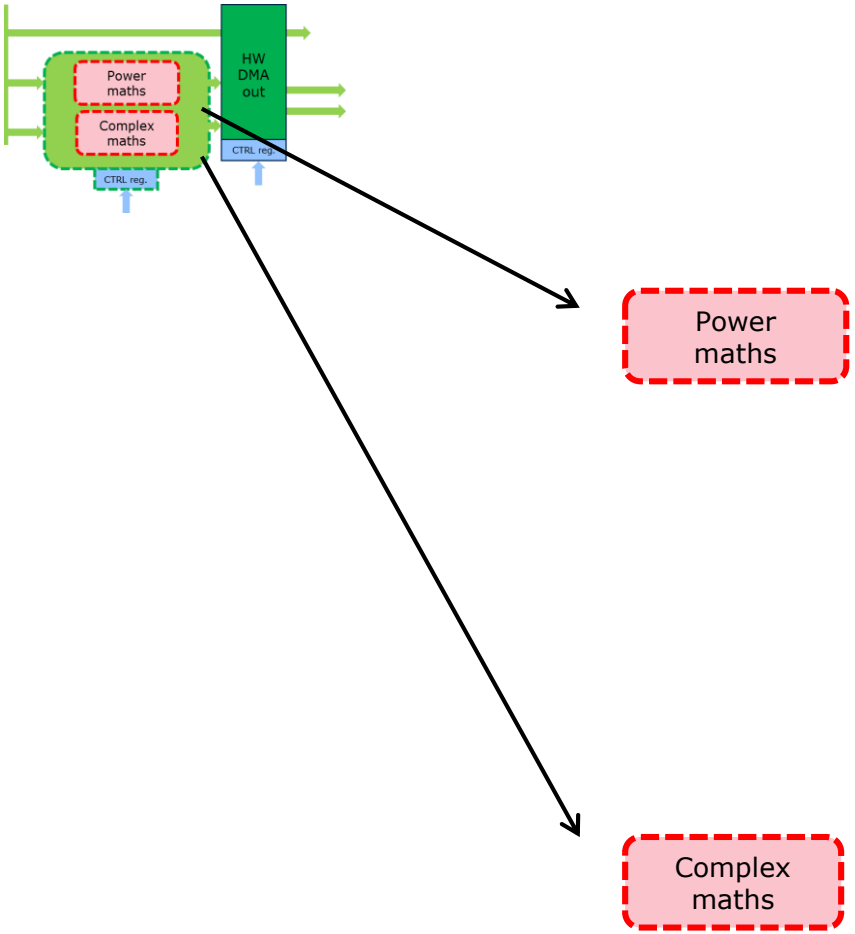
  - Signal (complex or real)
- Each data paths has multiple units running concurrently
- Configured by RADAR sequencer
  - Unit enabling
  - Additional parameters (threshold,…)
  - BIN update rate: 1 or 2 clocks (CFAR) / BINs depending on selected units

→ Performance = 1 to 2 clocks / BIN





Math2 Unit detailed overview
Supported Arithmetics



- Stats
  - Std Deviation
  - Average
  - Histogram
  - Min, Max

  } Concurrent
- Local Max (Out of or Out of 5)
- CA & GO CFAR (concurently)
- Log
- Vector add (NCI)
- Sum Linear Power
- Sum Log2 Power

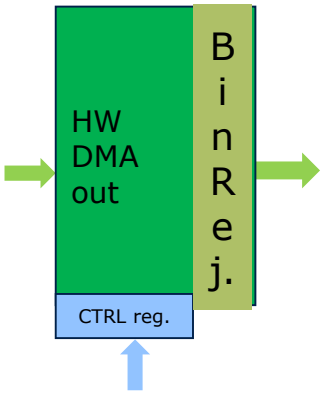
- FFT Data (16 or 32 Bits precision)
- Vector Add (CI)
- Scaling (Up & Down)
- Sum

Bin Rejection Unit

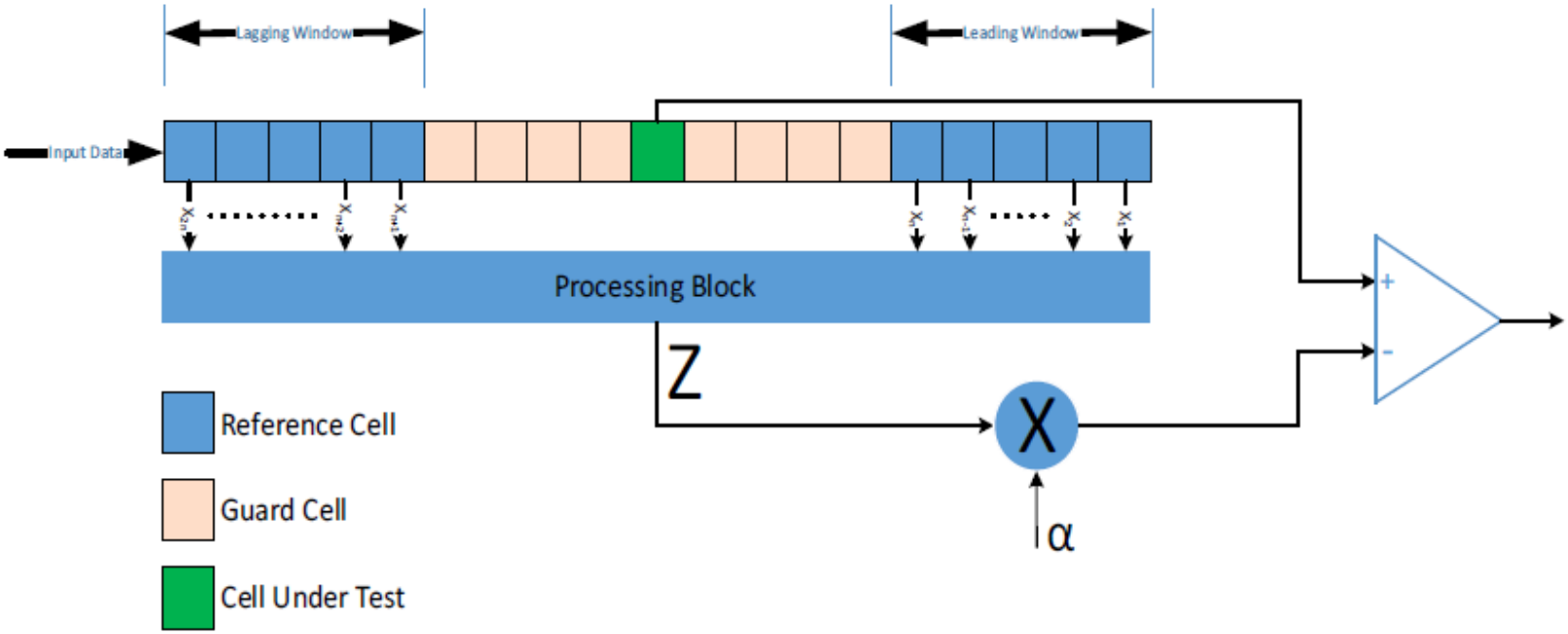
- Embedded in output DMA
- Allows to select which Data are saved to the memory
- Each vector bin has correspond bit defining

if the bin is saved (1) or deleted (0)

- Conditions for bin rejection
  - User defined mask
    - Range Cut Off
    - Real/Complex FFT Symetry
  - Threshold mask (using thresholding unit)
    - If powerof(bin) >threshold, bin is kept
    - If powerof(bin) <threshold, bin is set to 0 or deleted
  - Local Max
    - If powerof(bin) is local max, bin is kept
    - If powerof(bin) is not local max, bin is set to 0 or deleted
  - CFAR defined Mask
    - Same logic



CFAR Engine



- Two configurable CFARs computed concurently:
  - GOS: Ordered Statistics CFARs
    - GOS-CA/GOS-GO/GOS-SO
  - CA: Cell averaging CFARs:
    - CA-CFAR/CAGO-CFAR/CASO-CFAR/CASH-CFAR
  - Spectrum Extension Support
  - Connected to Bin rejection Unit

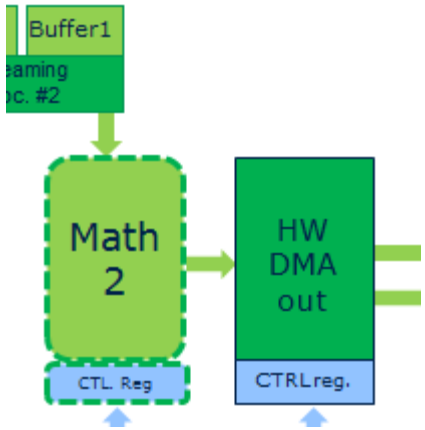
Performance = 2 clocks / BIN

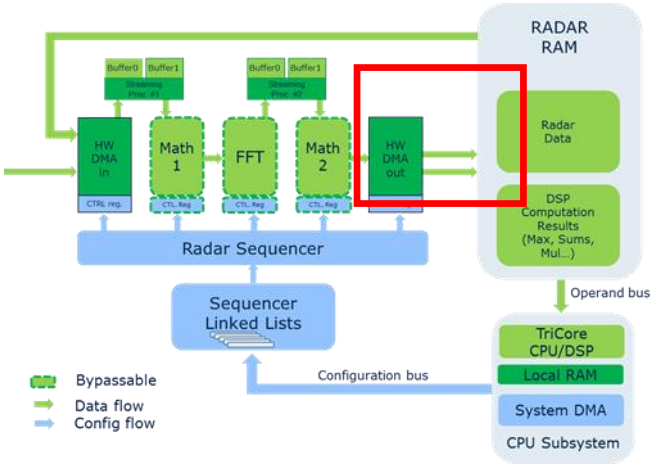
MATH2 Unit Functional Concurrency

	Stats	Local Max	CFAR CA	CFAR GOS	FFT Data	Log Signal Power	Vector Add NCI	Vector Add CI	Sum Linear Pow	Sum	Sum Log2 Pow
Power Domain	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes	No	Yes
Complex Domain	No	No			Yes	No	No	Yes	No	Yes	No
Output Channel (SPU DMA)	Port 3	Port 4		Port 5	Port 1	Port 2	Port 6	Port 7			Port 8
Max Perf	1 clk/Bin	2 clk/bin		2 clk/bin	1 clk/bin	1 clk/bin	2 clk/bin	2 clk/bin	1 clk/bin	1 clk/bin	1 clk/bin

Output HW 3D-DMA

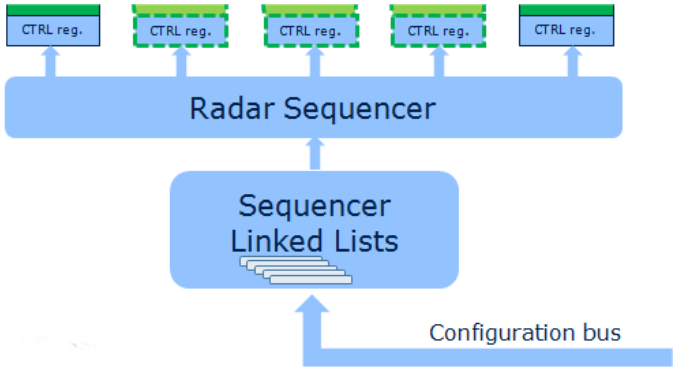
- 1 output FIFO per result source
- Implements inner loop and outer loop for FFT results
  - Fully configurable base address, inner loop increment and outer loop increment
  - Configured by Radar sequencer
  - Ramp/Antenna/Any Offset data Skip
- Implement basic DMA for other results
  - Configurable base address and increment
  - Configured by radar sequencer
- Histograms are stored in a dedicated memory accessible by the CPU.





Radar sequencer

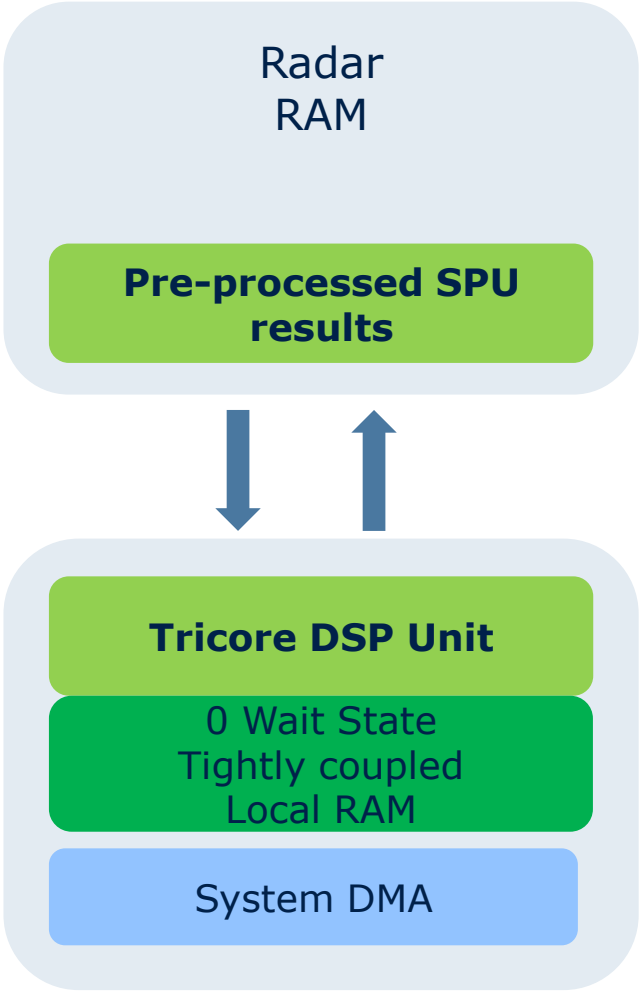
- Back-bone of SPU
  - Managing configuration/reconfiguration of each unit
  - Monitoring of each unit (overflow,..)
  - Configurations stored in RAM shared with TriCore
  - Configuration organised in linked lists



- Reconfiguration
  - Dual buffering (shadow register) in each unit for fast configuration change
    - New configuration prepared during computations
  - Full reconfiguration = new configuration applied after computing pipeline is empty
    - Latency = 2x (nb of BINs) x (2 or 4 clock / BIN)
  - Partial reconfiguration = new configuration applied only on input DMA
    - Latency = 0

High performance DSP Core
Tricore as versatile signal processing RISC Architecture

- 300 MHz Tricore with DSP
  - Tightly coupled 0 wait state RAM
  - Dual MAC
  - Triple Issue:
    - 1 Integer
    - 1 ld/st
    - 1 loop
- Highly optimized DSP library for radar signal processing
  - Linear Algebra
  - BLAS/CBLAS library
- High Speed SRI Interface
  - 64 bit X-Bar Bus
  - 300 MHz
  - Burst support for sustained bandwidth



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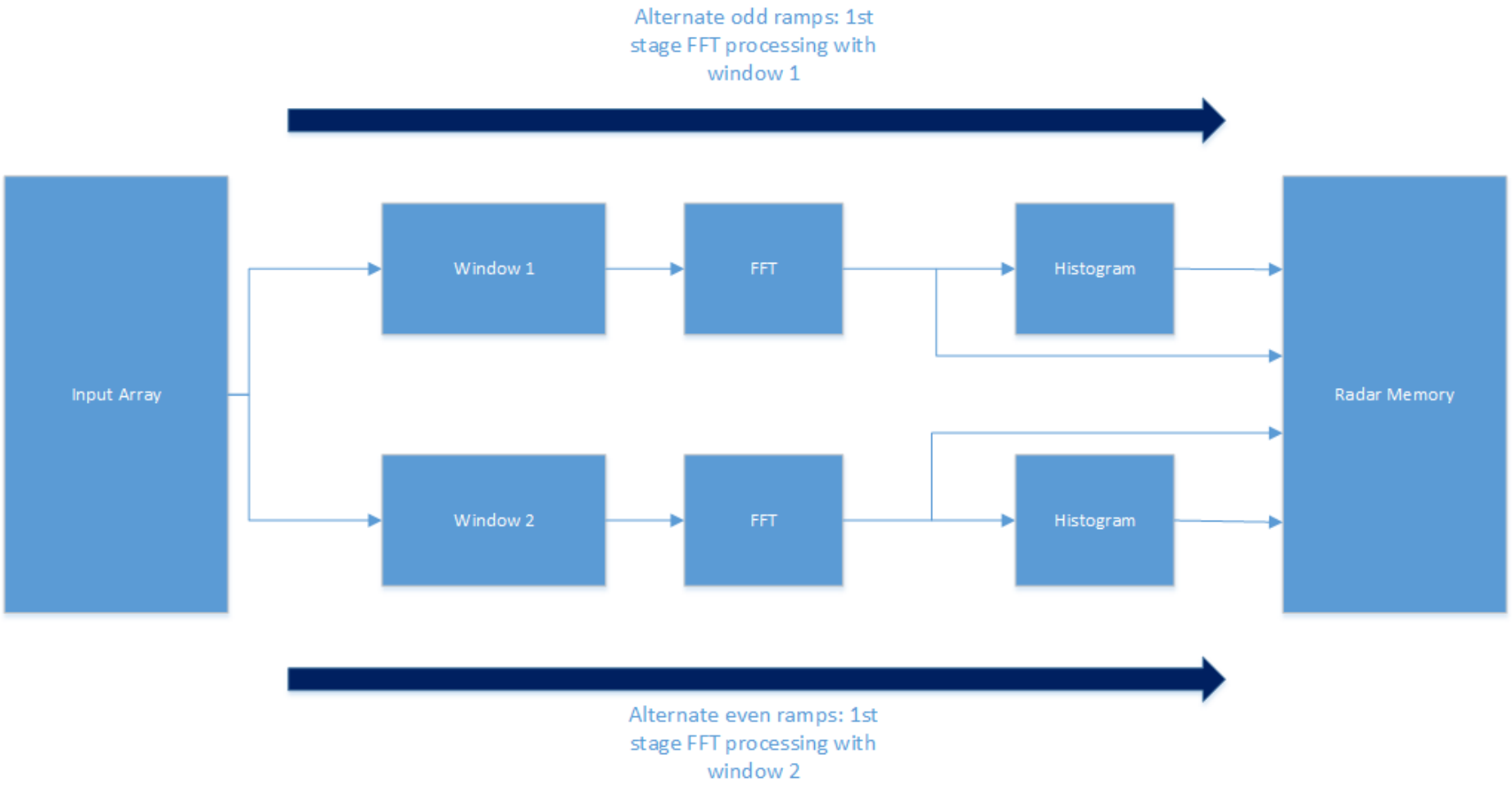
Use Case definition

- First stage FFT
  - Acquisition @33MSPS
  - 128 Ramps
  - 256 Bins/FFT
  - 4 Channels (Rx)
  - Alternate Ramp: Every second ramp with different Window
  - Histogram on data
- Second Stage FFT
- Every FFT processed twice:
  - With DBF
  - Without DBF
- Coherent Integration on DBF FFT Output
- CFAR CA & OS on DBF FFT Power output
- Non Coherent Integration on non-DBF FFT Output
- CFAR CA & OS on non-DBF FFT Power output

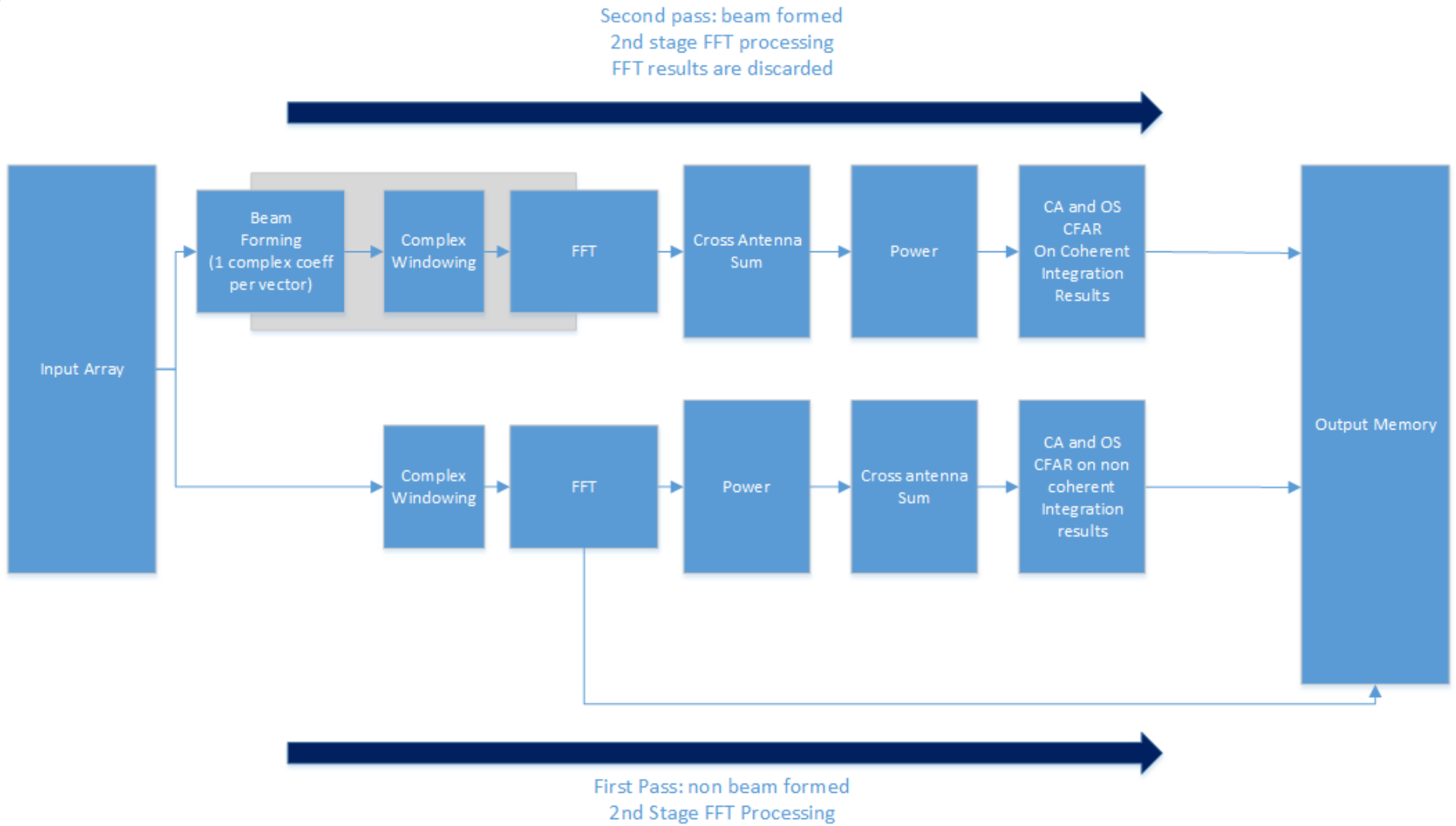
Use case example
First stage FFT processing



- Samples are processed in real time at a rate of 1 clocks/BIN
- Total processing time: 440us (Acquisition time >1ms @33MSPS)

Use Case Example

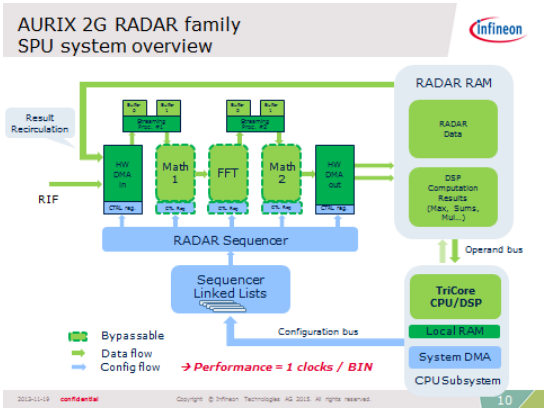
Second Stage FFT processing



- Multipass computations at 1clock/BIN; 2clock/BIN for the step where thresholding is enabled
- 880 us + 2x 111us for final integration

Performance gain

→ ***Performance = 1 clocks / BIN sustained***
→ ***30x more performance than Aurix 1G***



→ ***Acceleration for advanced Radar processing techniques:***
- → ***MIMO Radar***
- → ***Interference detection***
- → ***Digital Beam Forming***
- → ***Coherent & Non-Coherent Integration***
- → ***Thresholding/Min-Max***
- → ***CFAR (CA&OS)***

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