

# AURIX™ TC39x-B

## About this document

### Scope and purpose

The Appendix supplies information specific for the TC39x-B supplementing the family documentation.

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## Introduction

### 1 Introduction

For Introduction, block diagrams and feature set consult the family document.

For Pinning consult the Data Sheet.

## Memory Maps (MEMMAP)

## 2 Memory Maps (MEMMAP)

This is the automatically generated memory map of the TC39x-B.

### 2.1 Overview

The memory map describes the address locations and access possibilities for the units, memories, and reserved areas as “seen” from the different on-chip buses’ point of view.

### 2.2 Functional Description

The bus-specific address maps describe how the different bus master devices react on accesses to on-chip memories and modules, and which address ranges are valid or invalid for the corresponding buses.

The detailed address mapping of e.g. control registers, SRAM blocks or flash banks/sectors within a module is described in the related module chapter.

The SFI is an uni-directional bridge for access from SPB to SRI and therefore not mentioned here as an SRI master in the Address Map. The SFI is fully transparent and does not include an address translation mechanism.

**Note:** *In addition to the here described system address map, each TriCore has a TriCore IP internal access to its PSPR via C000\_0000<sub>H</sub> and an internal access to its DSPR via D000\_0000<sub>H</sub>. This additional/private view to the local scratch pad SRAMs is described in the CPU chapter.*

**Table 1** defines the acronyms and other terms that are used in the address maps.

**Table 1 Definition of Acronyms and Terms**

Term	Description
BE	A bus access is terminated with a bus error.
ok	A bus access is allowed and is executed.
16	A bus access with width 16 and 32 bits is allowed and executed.
32	A bus access with width 32 bits is allowed and executed.
Access	A bus access is allowed and is executed.

#### 2.2.1 Segments

This section summarizes the contents of the segments.

##### Segments 0 and 2

These memory segments are reserved.

##### Segments 1 and 3-7

These memory segments allow access to the CPUs Program and Data Scratch Pad SRAM (PSPR, DSPR), Program and Data Cache SRAMs (PCACHE, DCACHE) as well as TAG SRAMs related to Program and Data Cache (PTAG SRAM<sup>1)</sup> and DTAG SRAM<sup>1)</sup>).

Where DCACHE is supported, DCACHE and DTAG SRAM<sup>1)</sup> can be only accessed if the Data Cache is disabled.

PCACHE and PTAG SRAMs<sup>1)</sup> can be only accessed if the related Program Cache is disabled.

1) TAG SRAMs are not meant to be used as general SRAMs and can be accessed only with single data access and only with 64 bit aligned address.

## Memory Maps (MEMMAP)

The attribute of these segments (cached / non-cached) can be partially configured<sup>1)</sup> for each CPUs data and program side individually (see CPU chapter: Physical Memory Attribute Registers, PMAX).

### Segment 8

This memory segment allows cached access to PFlash and BROM.

### Segment 9

This memory segment allows cached access to LMU and to EMEM.

### Segment 10

This memory segment allows non-cached access to PFlash, DFlash and BROM.

### Segment 11

This memory segment allows non-cached access to LMU and to EMEM.

### Segment 12

This memory segment is reserved.

### Segment 13

This memory segment is reserved.

### Segment 14

This memory segment is reserved.

### Segment 15

The lower 128 Mbyte is SPB address space and the upper 128 Mbyte is SRI address space.

## 2.3 Bus Fabric SRI

This is the merged view of all SRI Bus Segments as used in the TC39x-B.

**Table 2 Address Map as seen by Bus Masters on Bus SRI**

Address Range		Size	Unit	Access Type	
from	to			Read	Write
00000000 <sub>H</sub>	0FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
10000000 <sub>H</sub>	10017FFF <sub>H</sub>	96 Kbyte	Data ScratchPad RAM (CPU5)	ok	ok
10018000 <sub>H</sub>	1001BFFF <sub>H</sub>	16 Kbyte	Data Cache RAM (CPU5)	ok	ok
1001C000 <sub>H</sub>	100BFFFF <sub>H</sub>	-	Reserved	BE	BE
100C0000 <sub>H</sub>	100C17FF <sub>H</sub>	6 Kbyte	Data Cache Tag RAM (CPU5)	ok	ok
100C1800 <sub>H</sub>	100FFFFF <sub>H</sub>	-	Reserved	BE	BE
10100000 <sub>H</sub>	1010FFFF <sub>H</sub>	64 Kbyte	Program ScratchPad RAM (CPU5)	ok	ok
10110000 <sub>H</sub>	10117FFF <sub>H</sub>	32 Kbyte	Program Cache RAM (CPU5)	ok	ok
10118000 <sub>H</sub>	101BFFFF <sub>H</sub>	-	Reserved	BE	BE

1) Mapping of Cache and TAG SRAMs is controlled via the MTU register MTU\_MEMMAP.

**Memory Maps (MEMMAP)****Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
101C0000 <sub>H</sub>	101C2FFF <sub>H</sub>	12 Kbyte	Program Cache TAG RAM (CPU5)	ok	ok
101C3000 <sub>H</sub>	2FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
30000000 <sub>H</sub>	30017FFF <sub>H</sub>	96 Kbyte	Data ScratchPad RAM (CPU4)	ok	ok
30018000 <sub>H</sub>	3001BFFF <sub>H</sub>	16 Kbyte	Data Cache RAM (CPU4)	ok	ok
3001C000 <sub>H</sub>	300BFFFF <sub>H</sub>	-	Reserved	BE	BE
300C0000 <sub>H</sub>	300C17FF <sub>H</sub>	6 Kbyte	Data Cache Tag RAM (CPU4)	ok	ok
300C1800 <sub>H</sub>	300FFFFF <sub>H</sub>	-	Reserved	BE	BE
30100000 <sub>H</sub>	3010FFFF <sub>H</sub>	64 Kbyte	Program ScratchPad RAM (CPU4)	ok	ok
30110000 <sub>H</sub>	30117FFF <sub>H</sub>	32 Kbyte	Program Cache RAM (CPU4)	ok	ok
30118000 <sub>H</sub>	301BFFFF <sub>H</sub>	-	Reserved	BE	BE
301C0000 <sub>H</sub>	301C2FFF <sub>H</sub>	12 Kbyte	Program Cache TAG RAM (CPU4)	ok	ok
301C3000 <sub>H</sub>	3FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
40000000 <sub>H</sub>	40017FFF <sub>H</sub>	96 Kbyte	Data ScratchPad RAM (CPU3)	ok	ok
40018000 <sub>H</sub>	4001BFFF <sub>H</sub>	16 Kbyte	Data Cache RAM (CPU3)	ok	ok
4001C000 <sub>H</sub>	400BFFFF <sub>H</sub>	-	Reserved	BE	BE
400C0000 <sub>H</sub>	400C17FF <sub>H</sub>	6 Kbyte	Data Cache Tag RAM (CPU3)	ok	ok
400C1800 <sub>H</sub>	400FFFFF <sub>H</sub>	-	Reserved	BE	BE
40100000 <sub>H</sub>	4010FFFF <sub>H</sub>	64 Kbyte	Program ScratchPad RAM (CPU3)	ok	ok
40110000 <sub>H</sub>	40117FFF <sub>H</sub>	32 Kbyte	Program Cache RAM (CPU3)	ok	ok
40118000 <sub>H</sub>	401BFFFF <sub>H</sub>	-	Reserved	BE	BE
401C0000 <sub>H</sub>	401C2FFF <sub>H</sub>	12 Kbyte	Program Cache TAG RAM (CPU3)	ok	ok
401C3000 <sub>H</sub>	4FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
50000000 <sub>H</sub>	50017FFF <sub>H</sub>	96 Kbyte	Data ScratchPad RAM (CPU2)	ok	ok
50018000 <sub>H</sub>	5001BFFF <sub>H</sub>	16 Kbyte	Data Cache RAM (CPU2)	ok	ok
5001C000 <sub>H</sub>	500BFFFF <sub>H</sub>	-	Reserved	BE	BE
500C0000 <sub>H</sub>	500C17FF <sub>H</sub>	6 Kbyte	Data Cache Tag RAM (CPU2)	ok	ok
500C1800 <sub>H</sub>	500FFFFF <sub>H</sub>	-	Reserved	BE	BE
50100000 <sub>H</sub>	5010FFFF <sub>H</sub>	64 Kbyte	Program ScratchPad RAM (CPU2)	ok	ok
50110000 <sub>H</sub>	50117FFF <sub>H</sub>	32 Kbyte	Program Cache RAM (CPU2)	ok	ok
50118000 <sub>H</sub>	501BFFFF <sub>H</sub>	-	Reserved	BE	BE
501C0000 <sub>H</sub>	501C2FFF <sub>H</sub>	12 Kbyte	Program Cache TAG RAM (CPU2)	ok	ok
501C3000 <sub>H</sub>	5FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
60000000 <sub>H</sub>	6003BFFF <sub>H</sub>	240 Kbyte	Data ScratchPad RAM (CPU1)	ok	ok
6003C000 <sub>H</sub>	6003FFFF <sub>H</sub>	16 Kbyte	Data Cache RAM (CPU1)	ok	ok
60040000 <sub>H</sub>	600BFFFF <sub>H</sub>	-	Reserved	BE	BE
600C0000 <sub>H</sub>	600C17FF <sub>H</sub>	6 Kbyte	Data Cache Tag RAM (CPU1)	ok	ok
600C1800 <sub>H</sub>	600FFFFF <sub>H</sub>	-	Reserved	BE	BE

**Memory Maps (MEMMAP)****Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
60100000 <sub>H</sub>	6010FFFF <sub>H</sub>	64 Kbyte	Program ScratchPad RAM (CPU1)	ok	ok
60110000 <sub>H</sub>	60117FFF <sub>H</sub>	32 Kbyte	Program Cache RAM (CPU1)	ok	ok
60118000 <sub>H</sub>	601BFFFF <sub>H</sub>	-	Reserved	BE	BE
601C0000 <sub>H</sub>	601C2FFF <sub>H</sub>	12 Kbyte	Program Cache TAG RAM (CPU1)	ok	ok
601C3000 <sub>H</sub>	6FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
70000000 <sub>H</sub>	7003BFFF <sub>H</sub>	240 Kbyte	Data ScratchPad RAM (CPU0)	ok	ok
7003C000 <sub>H</sub>	7003FFFF <sub>H</sub>	16 Kbyte	Data Cache RAM (CPU0)	ok	ok
70040000 <sub>H</sub>	700BFFFF <sub>H</sub>	-	Reserved	BE	BE
700C0000 <sub>H</sub>	700C17FF <sub>H</sub>	6 Kbyte	Data Cache Tag RAM (CPU0)	ok	ok
700C1800 <sub>H</sub>	700FFFFF <sub>H</sub>	-	Reserved	BE	BE
70100000 <sub>H</sub>	7010FFFF <sub>H</sub>	64 Kbyte	Program ScratchPad RAM (CPU0)	ok	ok
70110000 <sub>H</sub>	70117FFF <sub>H</sub>	32 Kbyte	Program Cache RAM (CPU0)	ok	ok
70118000 <sub>H</sub>	701BFFFF <sub>H</sub>	-	Reserved	BE	BE
701C0000 <sub>H</sub>	701C2FFF <sub>H</sub>	12 Kbyte	Program Cache TAG RAM (CPU0)	ok	ok
701C3000 <sub>H</sub>	7FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
80000000 <sub>H</sub>	802FFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI0)	ok	ok
80300000 <sub>H</sub>	805FFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI1)	ok	ok
80600000 <sub>H</sub>	808FFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI2)	ok	ok
80900000 <sub>H</sub>	80BFFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI3)	ok	ok
80C00000 <sub>H</sub>	80EFFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI4)	ok	ok
80F00000 <sub>H</sub>	80FFFFFF <sub>H</sub>	1 Mbyte	Program Flash (PFI5)	ok	ok
81000000 <sub>H</sub>	81FFFFFF <sub>H</sub>	-	Reserved	BE	BE
82000000 <sub>H</sub>	87FFFFFF <sub>H</sub>	96 Mbyte	External Memory Access Port (EBU)	ok	ok
88000000 <sub>H</sub>	8FDFFFFFF <sub>H</sub>	-	Reserved	BE	BE
8FE00000 <sub>H</sub>	8FE7FFFF <sub>H</sub>	512 Kbyte	Online Data Acquisition (OLDA) (DOM0)	BE	ok
8FE80000 <sub>H</sub>	8FFEFFFFFF <sub>H</sub>	-	Reserved	BE	BE
8FFF0000 <sub>H</sub>	8FFFFFFF <sub>H</sub>	64 Kbyte	Boot ROM (BROM) (DMU)	ok	ok
90000000 <sub>H</sub>	9000FFFF <sub>H</sub>	64 Kbyte	DLMU RAM (CPU0)	ok	ok
90010000 <sub>H</sub>	9001FFFF <sub>H</sub>	64 Kbyte	DLMU RAM (CPU1)	ok	ok
90020000 <sub>H</sub>	9002FFFF <sub>H</sub>	64 Kbyte	DLMU RAM (CPU2)	ok	ok
90030000 <sub>H</sub>	9003FFFF <sub>H</sub>	64 Kbyte	DLMU RAM (CPU3)	ok	ok
90040000 <sub>H</sub>	9007FFFF <sub>H</sub>	256 Kbyte	LMU RAM (LMU0)	ok	ok
90080000 <sub>H</sub>	900BFFFF <sub>H</sub>	256 Kbyte	LMU RAM (LMU1)	ok	ok
900C0000 <sub>H</sub>	900FFFFFF <sub>H</sub>	256 Kbyte	LMU RAM (LMU2)	ok	ok
90100000 <sub>H</sub>	9010FFFF <sub>H</sub>	64 Kbyte	DLMU RAM (CPU4)	ok	ok
90110000 <sub>H</sub>	9011FFFF <sub>H</sub>	64 Kbyte	DLMU RAM (CPU5)	ok	ok
90120000 <sub>H</sub>	903FFFFFF <sub>H</sub>	-	Reserved	BE	BE

**Memory Maps (MEMMAP)****Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
90400000 <sub>H</sub>	9040FFFF <sub>H</sub>	64 Kbyte	Access to DAM RAM (uses cached & non-cached DAM address ranges) (DAM0)	ok	ok
90410000 <sub>H</sub>	9041FFFF <sub>H</sub>	64 Kbyte	Access to DAM RAM (uses cached & non-cached DAM address ranges) (DAM1)	ok	ok
90420000 <sub>H</sub>	98FFFFFF <sub>H</sub>	-	Reserved	BE	BE
99000000 <sub>H</sub>	990FFFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 0 (access to EMEM module RAM, cached segment) (EMEMRAM0)	ok	ok
99100000 <sub>H</sub>	991FFFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 1 (access to EMEM module RAM, cached segment) (EMEMRAM1)	ok	ok
99200000 <sub>H</sub>	992FFFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 2 (access to EMEM module RAM, cached segment) (EMEMRAM2)	ok	ok
99300000 <sub>H</sub>	993FFFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 3 (access to EMEM module RAM, cached segment) (EMEMRAM3)	ok	ok
99400000 <sub>H</sub>	9FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
A0000000 <sub>H</sub>	A02FFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI0_NC)	ok	ok
A0300000 <sub>H</sub>	A05FFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI1_NC)	ok	ok
A0600000 <sub>H</sub>	A08FFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI2_NC)	ok	ok
A0900000 <sub>H</sub>	A0BFFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI3_NC)	ok	ok
A0C00000 <sub>H</sub>	A0EFFFFFF <sub>H</sub>	3 Mbyte	Program Flash (PFI4_NC)	ok	ok
A0F00000 <sub>H</sub>	A0FFFFFFF <sub>H</sub>	1 Mbyte	Program Flash (PFI5_NC)	ok	ok
A1000000 <sub>H</sub>	A1FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
A2000000 <sub>H</sub>	A7FFFFFF <sub>H</sub>	96 Mbyte	External Memory Access Port (EBU)	ok	ok
A8000000 <sub>H</sub>	A8003FFF <sub>H</sub>	16 Kbyte	Erase Counter (PFI0)	ok	ok
A8004000 <sub>H</sub>	A807FFFFFF <sub>H</sub>	-	Reserved	BE	BE
A8080000 <sub>H</sub>	A80FFFFFFF <sub>H</sub>	512 Kbyte	Register address space (PFI0)	ok	ok
A8100000 <sub>H</sub>	A82FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
A8300000 <sub>H</sub>	A8303FFF <sub>H</sub>	16 Kbyte	Erase Counter (PFI1)	ok	ok
A8304000 <sub>H</sub>	A837FFFFFF <sub>H</sub>	-	Reserved	BE	BE
A8380000 <sub>H</sub>	A83FFFFFFF <sub>H</sub>	512 Kbyte	Register address space (PFI1)	ok	ok
A8400000 <sub>H</sub>	A85FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
A8600000 <sub>H</sub>	A8603FFF <sub>H</sub>	16 Kbyte	Erase Counter (PFI2)	ok	ok
A8604000 <sub>H</sub>	A867FFFFFF <sub>H</sub>	-	Reserved	BE	BE
A8680000 <sub>H</sub>	A86FFFFFFF <sub>H</sub>	512 Kbyte	Register address space (PFI2)	ok	ok
A8700000 <sub>H</sub>	A88FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
A8900000 <sub>H</sub>	A8903FFF <sub>H</sub>	16 Kbyte	Erase Counter (PFI3)	ok	ok
A8904000 <sub>H</sub>	A897FFFFFF <sub>H</sub>	-	Reserved	BE	BE
A8980000 <sub>H</sub>	A89FFFFFFF <sub>H</sub>	512 Kbyte	Register address space (PFI3)	ok	ok
A8A00000 <sub>H</sub>	A8BFFFFFFF <sub>H</sub>	-	Reserved	BE	BE

## Memory Maps (MEMMAP)

**Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

## Memory Maps (MEMMAP)

**Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

**Memory Maps (MEMMAP)****Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
B9000000 <sub>H</sub>	B90FFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 0 (access to EMEM module RAM, non-cached segment) (EMEMRAM0)	ok	ok
B9100000 <sub>H</sub>	B91FFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 1 (access to EMEM module RAM, non-cached segment) (EMEMRAM1)	ok	ok
B9200000 <sub>H</sub>	B92FFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 2 (access to EMEM module RAM, non-cached segment) (EMEMRAM2)	ok	ok
B9300000 <sub>H</sub>	B93FFFFF <sub>H</sub>	1 Mbyte	SRI slave interface 3 (access to EMEM module RAM, non-cached segment) (EMEMRAM3)	ok	ok
B9400000 <sub>H</sub>	B947FFFF <sub>H</sub>	512 Kbyte	Non-Cached XTM Ram address range (SFIBRIDGE2) Bridge to Bus BBB (SFIBRIDGE2)	ok	ok
B9480000 <sub>H</sub>	F801FFFF <sub>H</sub>	-	Reserved	BE	BE
F8020000 <sub>H</sub>	F8029FFF <sub>H</sub>	40 Kbyte	sri slave interface (FSIRAM)	ok	ok
F802A000 <sub>H</sub>	F802FFFF <sub>H</sub>	-	Reserved	BE	BE
F8030000 <sub>H</sub>	F80300FF <sub>H</sub>	256 byte	sri slave interface (FSI)	ok	ok
F8030100 <sub>H</sub>	F8037FFF <sub>H</sub>	-	Reserved	BE	BE
F8038000 <sub>H</sub>	F803FFFF <sub>H</sub>	32 Kbyte	sri slave interface (PMU)	ok	ok
F8040000 <sub>H</sub>	F807FFFF <sub>H</sub>	256 Kbyte	sri slave interface (DMU)	ok	ok
F8080000 <sub>H</sub>	F80FFFFFF <sub>H</sub>	-	Reserved	BE	BE
F8100000 <sub>H</sub>	F810FFFF <sub>H</sub>	64 Kbyte	Special Function Registers (LMU0)	ok	ok
F8110000 <sub>H</sub>	F811FFFF <sub>H</sub>	64 Kbyte	Special Function Registers (LMU1)	ok	ok
F8120000 <sub>H</sub>	F812FFFF <sub>H</sub>	64 Kbyte	Special Function Registers (LMU2)	ok	ok
F8130000 <sub>H</sub>	F83FFFFFF <sub>H</sub>	-	Reserved	BE	BE
F8400000 <sub>H</sub>	F840FFFF <sub>H</sub>	64 Kbyte	sri slave interface (EBU)	ok	ok
F8410000 <sub>H</sub>	F84FFFFFF <sub>H</sub>	-	Reserved	BE	BE
F8500000 <sub>H</sub>	F8507FFF <sub>H</sub>	32 Kbyte	Special Function Registers (DAM0)	ok	ok
F8508000 <sub>H</sub>	F85080FF <sub>H</sub>	256 byte	sri slave interface (AMU00)	ok	ok
F8508100 <sub>H</sub>	F85081FF <sub>H</sub>	256 byte	sri slave interface (AMU01)	ok	ok
F8508200 <sub>H</sub>	F85083FF <sub>H</sub>	-	Reserved	BE	BE
F8508400 <sub>H</sub>	F85084FF <sub>H</sub>	256 byte	sri slave interface (ADMA0)	ok	ok
F8508500 <sub>H</sub>	F850FFFFFF <sub>H</sub>	-	Reserved	BE	BE
F8510000 <sub>H</sub>	F8517FFF <sub>H</sub>	32 Kbyte	Special Function Registers (DAM1)	ok	ok
F8518000 <sub>H</sub>	F85180FF <sub>H</sub>	256 byte	sri slave interface (AMU10)	ok	ok
F8518100 <sub>H</sub>	F85181FF <sub>H</sub>	256 byte	sri slave interface (AMU11)	ok	ok
F8518200 <sub>H</sub>	F85183FF <sub>H</sub>	-	Reserved	BE	BE
F8518400 <sub>H</sub>	F85184FF <sub>H</sub>	256 byte	sri slave interface (ADMA1)	ok	ok
F8518500 <sub>H</sub>	F86FFFFFF <sub>H</sub>	-	Reserved	BE	BE
F8700000 <sub>H</sub>	F870FFFF <sub>H</sub>	64 Kbyte	sri slave interface (DOM0)	ok	ok
F8710000 <sub>H</sub>	F87FFFFFF <sub>H</sub>	-	Reserved	BE	BE

**Memory Maps (MEMMAP)****Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
F8800000 <sub>H</sub>	F881FFFF <sub>H</sub>	128 Kbyte	Safety Memory Protection Register (CPU0) DLMU Safety Memory Protection registers (CPU0) Safety register protection registers (CPU0) Kernel Reset registers (CPU0) Flash Configuration registers (CPU0) Overlay Block Control registers (CPU0) Memory Integrity Registers (CPU0) Core Special Function Registers (CPU0) General Purpose Registers (CPU0) Memory Protection Registers (CPU0) Temporal Protection System registers (CPU0) Floating point register (CPU0) Core Debug Performance Counter registers (CPU0) Data Memory Interface registers (CPU0) Program Memory Interface registers (CPU0)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok
F8820000 <sub>H</sub>	F883FFFF <sub>H</sub>	128 Kbyte	Safety Memory Protection Register (CPU1) DLMU Safety Memory Protection registers (CPU1) Safety register protection registers (CPU1) Kernel Reset registers (CPU1) Flash Configuration registers (CPU1) Overlay Block Control registers (CPU1) Memory Integrity Registers (CPU1) Core Special Function Registers (CPU1) General Purpose Registers (CPU1) Memory Protection Registers (CPU1) Temporal Protection System registers (CPU1) Floating point register (CPU1) Core Debug Performance Counter registers (CPU1) Data Memory Interface registers (CPU1) Program Memory Interface registers (CPU1)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok
F8840000 <sub>H</sub>	F885FFFF <sub>H</sub>	128 Kbyte	Safety Memory Protection Register (CPU2) DLMU Safety Memory Protection registers (CPU2) Safety register protection registers (CPU2) Kernel Reset registers (CPU2) Flash Configuration registers (CPU2) Overlay Block Control registers (CPU2) Memory Integrity Registers (CPU2) Core Special Function Registers (CPU2) General Purpose Registers (CPU2) Memory Protection Registers (CPU2) Temporal Protection System registers (CPU2) Floating point register (CPU2) Core Debug Performance Counter registers (CPU2) Data Memory Interface registers (CPU2) Program Memory Interface registers (CPU2)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok

**Memory Maps (MEMMAP)****Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
F8860000 <sub>H</sub>	F887FFFF <sub>H</sub>	128 Kbyte	Safety Memory Protection Register (CPU3) DLMU Safety Memory Protection registers (CPU3) Safety register protection registers (CPU3) Kernel Reset registers (CPU3) Flash Configuration registers (CPU3) Overlay Block Control registers (CPU3) Memory Integrity Registers (CPU3) Core Special Function Registers (CPU3) General Purpose Registers (CPU3) Memory Protection Registers (CPU3) Temporal Protection System registers (CPU3) Floating point register (CPU3) Core Debug Performance Counter registers (CPU3) Data Memory Interface registers (CPU3) Program Memory Interface registers (CPU3)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok
F8880000 <sub>H</sub>	F889FFFF <sub>H</sub>	128 Kbyte	Safety Memory Protection Register (CPU4) DLMU Safety Memory Protection registers (CPU4) Safety register protection registers (CPU4) Kernel Reset registers (CPU4) Flash Configuration registers (CPU4) Overlay Block Control registers (CPU4) Memory Integrity Registers (CPU4) Core Special Function Registers (CPU4) General Purpose Registers (CPU4) Memory Protection Registers (CPU4) Temporal Protection System registers (CPU4) Floating point register (CPU4) Core Debug Performance Counter registers (CPU4) Data Memory Interface registers (CPU4) Program Memory Interface registers (CPU4)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok
F88A0000 <sub>H</sub>	F88BFFFF <sub>H</sub>	-	Reserved	BE	BE

**Memory Maps (MEMMAP)****Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
F88C0000 <sub>H</sub>	F88DFFFF <sub>H</sub>	128 Kbyte	Safety Memory Protection Register (CPU5) DLMU Safety Memory Protection registers (CPU5) Safety register protection registers (CPU5) Kernel Reset registers (CPU5) Flash Configuration registers (CPU5) Overlay Block Control registers (CPU5) Memory Integrity Registers (CPU5) Core Special Function Registers (CPU5) General Purpose Registers (CPU5) Memory Protection Registers (CPU5) Temporal Protection System registers (CPU5) Floating point register (CPU5) Core Debug Performance Counter registers (CPU5) Data Memory Interface registers (CPU5) Program Memory Interface registers (CPU5)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok
F88E0000 <sub>H</sub>	F88EFFFF <sub>H</sub>	64 Kbyte	sri slave interface (DOM1)	ok	ok
F88F0000 <sub>H</sub>	F9FFFFFF <sub>H</sub>	-	Reserved	BE	BE
FA000000 <sub>H</sub>	FAFFFFFF <sub>H</sub>	16 Mbyte	Non-Cached XTM Ram address range (SFIBRIDGE2)	ok	ok
FB000000 <sub>H</sub>	FB00FFFF <sub>H</sub>	64 Kbyte	EMEM RAM SRI Interface Control Registers (EMEMMPU0)	ok	ok
FB010000 <sub>H</sub>	FB01FFFF <sub>H</sub>	64 Kbyte	EMEM RAM SRI Interface Control Registers (EMEMMPU1)	ok	ok
FB020000 <sub>H</sub>	FB02FFFF <sub>H</sub>	64 Kbyte	EMEM RAM SRI Interface Control Registers (EMEMMPU2)	ok	ok
FB030000 <sub>H</sub>	FB03FFFF <sub>H</sub>	64 Kbyte	EMEM RAM SRI Interface Control Registers (EMEMMPU3)	ok	ok
FB040000 <sub>H</sub>	FB6FFFFFF <sub>H</sub>	-	Reserved	BE	BE
FB700000 <sub>H</sub>	FB70FFFF <sub>H</sub>	64 Kbyte	sri slave interface (DOM2)	ok	ok
FB710000 <sub>H</sub>	FFBFFFFFF <sub>H</sub>	-	Reserved	BE	BE
FFC00000 <sub>H</sub>	FFC1FFFF <sub>H</sub>	128 Kbyte	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter (DMU)	ok	ok
FFC20000 <sub>H</sub>	FFFFFFF <sub>H</sub>	-	Reserved	BE	BE

**2.4 Bus Instance SPB****Table 3 Address Map as seen by Bus Masters on Bus SPB**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
00000000 <sub>H</sub>	0FFFFFFF <sub>H</sub>	-	Reserved	BE	BE
10000000 <sub>H</sub>	EFFFFFFF <sub>H</sub>	3584 Mbyte	Redirection of SRI ranges (SFIBRIDGE1) Bridge to Bus Segment 00 of SRI (SFIBRIDGE1)	ok	ok

**Memory Maps (MEMMAP)****Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
F0000000 <sub>H</sub>	F00001FF <sub>H</sub>	512 byte	FPI slave interface (FCE)	ok	ok
F0000200 <sub>H</sub>	F00003FF <sub>H</sub>	-	Reserved	BE	BE
F0000400 <sub>H</sub>	F00005FF <sub>H</sub>	512 byte	FPI slave interface (CBS)	ok	ok
F0000600 <sub>H</sub>	F00006FF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN0)	ok	ok
F0000700 <sub>H</sub>	F00007FF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN1)	ok	ok
F0000800 <sub>H</sub>	F00008FF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN2)	ok	ok
F0000900 <sub>H</sub>	F00009FF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN3)	ok	ok
F0000A00 <sub>H</sub>	F0000AFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN4)	ok	ok
F0000B00 <sub>H</sub>	F0000BFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN5)	ok	ok
F0000C00 <sub>H</sub>	F0000CFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN6)	ok	ok
F0000D00 <sub>H</sub>	F0000DFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN7)	ok	ok
F0000E00 <sub>H</sub>	F0000EFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN8)	ok	ok
F0000F00 <sub>H</sub>	F0000FFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN9)	ok	ok
F0001000 <sub>H</sub>	F00010FF <sub>H</sub>	256 byte	FPI slave interface (STM0)	ok	ok
F0001100 <sub>H</sub>	F00011FF <sub>H</sub>	256 byte	FPI slave interface (STM1)	ok	ok
F0001200 <sub>H</sub>	F00012FF <sub>H</sub>	256 byte	FPI slave interface (STM2)	ok	ok
F0001300 <sub>H</sub>	F00013FF <sub>H</sub>	256 byte	FPI slave interface (STM3)	ok	ok
F0001400 <sub>H</sub>	F00014FF <sub>H</sub>	256 byte	FPI slave interface (STM4)	ok	ok
F0001500 <sub>H</sub>	F00015FF <sub>H</sub>	256 byte	FPI slave interface (STM5)	ok	ok
F0001600 <sub>H</sub>	F00017FF <sub>H</sub>	-	Reserved	BE	BE
F0001800 <sub>H</sub>	F00018FF <sub>H</sub>	256 byte	FPI slave interface (GPT120)	ok	ok
F0001900 <sub>H</sub>	F0001BFF <sub>H</sub>	-	Reserved	BE	BE
F0001C00 <sub>H</sub>	F0001CFF <sub>H</sub>	256 byte	Register block QSPI0 (QSPI0)	ok	ok
F0001D00 <sub>H</sub>	F0001DFF <sub>H</sub>	256 byte	Register block QSPI1 (QSPI1)	ok	ok
F0001E00 <sub>H</sub>	F0001EFF <sub>H</sub>	256 byte	Register block QSPI2 (QSPI2)	ok	ok
F0001F00 <sub>H</sub>	F0001FFF <sub>H</sub>	256 byte	Register block QSPI3 (QSPI3)	ok	ok
F0002000 <sub>H</sub>	F00020FF <sub>H</sub>	256 byte	Register block QSPI4 (QSPI4)	ok	ok
F0002100 <sub>H</sub>	F00021FF <sub>H</sub>	256 byte	Register block QSPI5 (QSPI5)	ok	ok
F0002200 <sub>H</sub>	F00025FF <sub>H</sub>	-	Reserved	BE	BE
F0002600 <sub>H</sub>	F00026FF <sub>H</sub>	256 byte	FPI slave interface (MSC0)	ok	ok
F0002700 <sub>H</sub>	F00027FF <sub>H</sub>	256 byte	FPI slave interface (MSC1)	ok	ok
F0002800 <sub>H</sub>	F00028FF <sub>H</sub>	256 byte	FPI slave interface (MSC2)	ok	ok
F0002900 <sub>H</sub>	F00029FF <sub>H</sub>	256 byte	FPI slave interface (MSC3)	ok	ok
F0002A00 <sub>H</sub>	F0002AFF <sub>H</sub>	256 byte	FPI slave interface (CCU60)	ok	ok
F0002B00 <sub>H</sub>	F0002BFF <sub>H</sub>	256 byte	FPI slave interface (CCU61)	ok	ok
F0002C00 <sub>H</sub>	F0002FFF <sub>H</sub>	-	Reserved	BE	BE
F0003000 <sub>H</sub>	F0003AFF <sub>H</sub>	2.7 Kbyte	FPI slave interface (SENT)	ok	ok

**Memory Maps (MEMMAP)****Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
F0003B00 <sub>H</sub>	F0004FFF <sub>H</sub>	-	Reserved	BE	BE
F0005000 <sub>H</sub>	F0005AFF <sub>H</sub>	2.7 Kbyte	FPI slave interface (PSI5) FPI slave interface (PSI5)	ok ok	ok ok
F0005B00 <sub>H</sub>	F0006FFF <sub>H</sub>	-	Reserved	BE	BE
F0007000 <sub>H</sub>	F0007FFF <sub>H</sub>	4 Kbyte	FPI slave interface (PSI5S)	ok	ok
F0008000 <sub>H</sub>	F000FFFF <sub>H</sub>	-	Reserved	BE	BE
F0010000 <sub>H</sub>	F0013FFF <sub>H</sub>	16 Kbyte	FPI slave interface (DMA)	ok	ok
F0014000 <sub>H</sub>	F0016FFF <sub>H</sub>	-	Reserved	BE	BE
F0017000 <sub>H</sub>	F0017FFF <sub>H</sub>	4 Kbyte	FPI slave interface (ERAY1) ERAY RAM (ERAY1)	ok ok	ok ok
F0018000 <sub>H</sub>	F001BFFF <sub>H</sub>	-	Reserved	BE	BE
F001C000 <sub>H</sub>	F001CFFF <sub>H</sub>	4 Kbyte	FPI slave interface (ERAY0) ERAY RAM (ERAY0)	ok ok	ok ok
F001D000 <sub>H</sub>	F001F0FF <sub>H</sub>	8.2 Kbyte	FPI bus interface (GETH) FPI bus interface (GETH)	ok ok	ok ok
F001F100 <sub>H</sub>	F001FFFF <sub>H</sub>	-	Reserved	BE	BE
F0020000 <sub>H</sub>	F0023FFF <sub>H</sub>	16 Kbyte	FPI slave interface (EVADC)	ok	ok
F0024000 <sub>H</sub>	F0024FFF <sub>H</sub>	4 Kbyte	FPI slave interface (EDSADC)	ok	ok
F0025000 <sub>H</sub>	F00250FF <sub>H</sub>	256 byte	FPI slave interface (CONVCTRL)	ok	ok
F0025100 <sub>H</sub>	F002FFFF <sub>H</sub>	-	Reserved	BE	BE
F0030000 <sub>H</sub>	F00300FF <sub>H</sub>	256 byte	BCU Registers (SBCU)	ok	ok
F0030100 <sub>H</sub>	F0034FFF <sub>H</sub>	-	Reserved	BE	BE
F0035000 <sub>H</sub>	F00351FF <sub>H</sub>	512 byte	FPI slave interface (IOM)	ok	ok
F0035200 <sub>H</sub>	F0035FFF <sub>H</sub>	-	Reserved	BE	BE
F0036000 <sub>H</sub>	F00363FF <sub>H</sub>	1 Kbyte	SCU: Connections to FPI/BPI bus (SCU) Clocking System Registers (SCU) Power Management Registers (SCU)	ok ok ok	ok ok ok
F0036400 <sub>H</sub>	F00367FF <sub>H</sub>	-	Reserved	BE	BE
F0036800 <sub>H</sub>	F0036FFF <sub>H</sub>	2 Kbyte	FPI slave interface (SMU)	ok	ok
F0037000 <sub>H</sub>	F0037FFF <sub>H</sub>	4 Kbyte	IR Status and Control Registers (INT)	ok	ok
F0038000 <sub>H</sub>	F0039FFF <sub>H</sub>	8 Kbyte	IR Service Request Control Registers (SRC) (SRC)	ok	ok
F003A000 <sub>H</sub>	F003A0FF <sub>H</sub>	256 byte	SPB bus slave interface (P00)	ok	ok
F003A100 <sub>H</sub>	F003A1FF <sub>H</sub>	256 byte	SPB bus slave interface (P01)	ok	ok
F003A200 <sub>H</sub>	F003A2FF <sub>H</sub>	256 byte	SPB bus slave interface (P02)	ok	ok
F003A300 <sub>H</sub>	F003A9FF <sub>H</sub>	-	Reserved	BE	BE
F003AA00 <sub>H</sub>	F003AAFF <sub>H</sub>	256 byte	SPB bus slave interface (P10)	ok	ok
F003AB00 <sub>H</sub>	F003ABFF <sub>H</sub>	256 byte	SPB bus slave interface (P11)	ok	ok
F003AC00 <sub>H</sub>	F003ACFF <sub>H</sub>	256 byte	SPB bus slave interface (P12)	ok	ok

**Memory Maps (MEMMAP)****Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
F003AD00 <sub>H</sub>	F003ADFF <sub>H</sub>	256 byte	SPB bus slave interface (P13)	ok	ok
F003AE00 <sub>H</sub>	F003AEFF <sub>H</sub>	256 byte	SPB bus slave interface (P14)	ok	ok
F003AF00 <sub>H</sub>	F003AFFF <sub>H</sub>	256 byte	SPB bus slave interface (P15)	ok	ok
F003B000 <sub>H</sub>	F003B3FF <sub>H</sub>	-	Reserved	BE	BE
F003B400 <sub>H</sub>	F003B4FF <sub>H</sub>	256 byte	SPB bus slave interface (P20)	ok	ok
F003B500 <sub>H</sub>	F003B5FF <sub>H</sub>	256 byte	SPB bus slave interface (P21)	ok	ok
F003B600 <sub>H</sub>	F003B6FF <sub>H</sub>	256 byte	SPB bus slave interface (P22)	ok	ok
F003B700 <sub>H</sub>	F003B7FF <sub>H</sub>	256 byte	SPB bus slave interface (P23)	ok	ok
F003B800 <sub>H</sub>	F003B8FF <sub>H</sub>	256 byte	SPB bus slave interface (P24)	ok	ok
F003B900 <sub>H</sub>	F003B9FF <sub>H</sub>	256 byte	SPB bus slave interface (P25)	ok	ok
F003BA00 <sub>H</sub>	F003BAFF <sub>H</sub>	256 byte	SPB bus slave interface (P26)	ok	ok
F003BB00 <sub>H</sub>	F003BDFF <sub>H</sub>	-	Reserved	BE	BE
F003BE00 <sub>H</sub>	F003BEFF <sub>H</sub>	256 byte	SPB bus slave interface (P30)	ok	ok
F003BF00 <sub>H</sub>	F003BFFF <sub>H</sub>	256 byte	SPB bus slave interface (P31)	ok	ok
F003C000 <sub>H</sub>	F003C0FF <sub>H</sub>	256 byte	SPB bus slave interface (P32)	ok	ok
F003C100 <sub>H</sub>	F003C1FF <sub>H</sub>	256 byte	SPB bus slave interface (P33)	ok	ok
F003C200 <sub>H</sub>	F003C2FF <sub>H</sub>	256 byte	SPB bus slave interface (P34)	ok	ok
F003C300 <sub>H</sub>	F003C7FF <sub>H</sub>	-	Reserved	BE	BE
F003C800 <sub>H</sub>	F003C8FF <sub>H</sub>	256 byte	SPB bus slave interface (P40)	ok	ok
F003C900 <sub>H</sub>	F003C9FF <sub>H</sub>	256 byte	SPB bus slave interface (P41)	ok	ok
F003CA00 <sub>H</sub>	F003FFFF <sub>H</sub>	-	Reserved	BE	BE
F0040000 <sub>H</sub>	F005FFFF <sub>H</sub>	128 Kbyte	System Registers (HSM)	32	32
			Debug Registers (HSM)	32	32
			Communication Registers (HSM)	32	32
			HSM Reset (HSM)	32	32
F0060000 <sub>H</sub>	F006FFFF <sub>H</sub>	64 Kbyte	FPI slave interface (MTU) FPI slave interface (MTU)	ok ok	ok ok
F0070000 <sub>H</sub>	F007FFFF <sub>H</sub>	-	Reserved	BE	BE
F0080000 <sub>H</sub>	F00803FF <sub>H</sub>	1 Kbyte	FPI slave interface (HSSL0)	ok	ok
F0080400 <sub>H</sub>	F008FFFF <sub>H</sub>	-	Reserved	BE	BE
F0090000 <sub>H</sub>	F009FFFF <sub>H</sub>	64 Kbyte	FPI slave interface (HSCT0)	ok	ok
F00A0000 <sub>H</sub>	F00A03FF <sub>H</sub>	1 Kbyte	FPI slave interface (HSSL1)	ok	ok
F00A0400 <sub>H</sub>	F00AFFFF <sub>H</sub>	-	Reserved	BE	BE
F00B0000 <sub>H</sub>	F00BFFFF <sub>H</sub>	64 Kbyte	FPI slave interface (HSCT1)	ok	ok
F00C0000 <sub>H</sub>	F00D00FF <sub>H</sub>	64.2 Kbyte	FPI slave interface (I2C0)	ok	ok
			FPI slave interface (I2C0)	ok	ok
F00D0100 <sub>H</sub>	F00DFFFF <sub>H</sub>	-	Reserved	BE	BE

**Memory Maps (MEMMAP)****Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
F00E0000 <sub>H</sub>	F00F00FF <sub>H</sub>	64.2 Kbyte	FPI slave interface (I2C1) FPI slave interface (I2C1)	ok ok	ok ok
F00F0100 <sub>H</sub>	F00FFFFF <sub>H</sub>	-	Reserved	BE	BE
F0100000 <sub>H</sub>	F01FFFFFF <sub>H</sub>	1 Mbyte	FPI slave interface (GTM) FPI slave interface (GTM) Mapped RAMs (GTM) Embedded DPLL RAM 2 (GTM)	ok ok ok ok	ok ok ok ok
F0200000 <sub>H</sub>	F0208FFF <sub>H</sub>	36 Kbyte	RAM Area (CAN0) Register Area (CAN0)	ok ok	ok ok
F0209000 <sub>H</sub>	F020FFFF <sub>H</sub>	-	Reserved	BE	BE
F0210000 <sub>H</sub>	F0218FFF <sub>H</sub>	36 Kbyte	RAM Area (CAN1) Register Area (CAN1)	ok ok	ok ok
F0219000 <sub>H</sub>	F021FFFF <sub>H</sub>	-	Reserved	BE	BE
F0220000 <sub>H</sub>	F0228FFF <sub>H</sub>	36 Kbyte	RAM Area (CAN2) Register Area (CAN2)	ok ok	ok ok
F0229000 <sub>H</sub>	F023FFFF <sub>H</sub>	-	Reserved	BE	BE
F0240000 <sub>H</sub>	F0241FFF <sub>H</sub>	8 Kbyte	Standby Controller XRAM (PMS)	ok	ok
F0242000 <sub>H</sub>	F0247FFF <sub>H</sub>	-	Reserved	BE	BE
F0248000 <sub>H</sub>	F02481FF <sub>H</sub>	512 byte	FPI slave interface (PMS) SMU registers in Standby power domain (PMS)	ok ok	ok ok
F0248200 <sub>H</sub>	F027FFFF <sub>H</sub>	-	Reserved	BE	BE
F0280000 <sub>H</sub>	F0281FFF <sub>H</sub>	8 Kbyte	RAM Area (HSPDM)	ok	ok
F0282000 <sub>H</sub>	F02820FF <sub>H</sub>	256 byte	FPI slave interface for BPI registers access (HSPDM)	ok	ok
F0282100 <sub>H</sub>	F02AFFFF <sub>H</sub>	-	Reserved	BE	BE
F02B0000 <sub>H</sub>	F02B0FFF <sub>H</sub>	4 Kbyte	FPI slave interface (SDMMC0)	ok	ok
F02B1000 <sub>H</sub>	F02C09FF <sub>H</sub>	-	Reserved	BE	BE
F02C0A00 <sub>H</sub>	F02C0AFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN10)	ok	ok
F02C0B00 <sub>H</sub>	F02C0BFF <sub>H</sub>	256 byte	FPI slave interface (ASCLIN11)	ok	ok
F02C0C00 <sub>H</sub>	F7FFFFFF <sub>H</sub>	-	Reserved	BE	BE
F8000000 <sub>H</sub>	FFFFFFFF <sub>H</sub>	128 Mbyte	Redirection of SRI ranges (SFIBRIDGE1)	ok	ok

**2.5 Bus Instance BBB****Table 4 Address Map as seen by Bus Masters on Bus BBB**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
00000000 <sub>H</sub>	98FFFFFF <sub>H</sub>	-	Reserved	BE	BE
99000000 <sub>H</sub>	990FFFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 0 (access to EMEM module RAM, cached segment) (EMEMRAM0)	ok	ok

**Memory Maps (MEMMAP)****Table 4 Address Map as seen by Bus Masters on Bus BBB (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
99100000 <sub>H</sub>	991FFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 1 (access to EMEM module RAM, cached segment) (EMEMRAM1)	ok	ok
99200000 <sub>H</sub>	992FFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 2 (access to EMEM module RAM, cached segment) (EMEMRAM2)	ok	ok
99300000 <sub>H</sub>	993FFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 3 (access to EMEM module RAM, cached segment) (EMEMRAM3)	ok	ok
99400000 <sub>H</sub>	B8FFFFFF <sub>H</sub>	-	Reserved	BE	BE
B9000000 <sub>H</sub>	B90FFFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 0 (access to EMEM module RAM, non-cached segment) (EMEMRAM0)	ok	ok
B9100000 <sub>H</sub>	B91FFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 1 (access to EMEM module RAM, non-cached segment) (EMEMRAM1)	ok	ok
B9200000 <sub>H</sub>	B92FFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 2 (access to EMEM module RAM, non-cached segment) (EMEMRAM2)	ok	ok
B9300000 <sub>H</sub>	B93FFFFF <sub>H</sub>	1 Mbyte	BBB slave interface 3 (access to EMEM module RAM, non-cached segment) (EMEMRAM3)	ok	ok
B9400000 <sub>H</sub>	B947FFFF <sub>H</sub>	512 Kbyte	XTM FPI slave interface (XTM)	ok	ok
B9480000 <sub>H</sub>	EFFFFFFF <sub>H</sub>	-	Reserved	BE	BE
F0000000 <sub>H</sub>	FA0000FF <sub>H</sub>	-	Reserved	BE	BE
FA000100 <sub>H</sub>	FA0001FF <sub>H</sub>	256 byte	BCU Registers (EBCU)	ok	ok
FA000200 <sub>H</sub>	FA000FFF <sub>H</sub>	-	Reserved	BE	BE
FA001000 <sub>H</sub>	FA0010FF <sub>H</sub>	256 byte	FPI slave interface (AGBT)	ok	ok
FA001100 <sub>H</sub>	FA005FFF <sub>H</sub>	-	Reserved	BE	BE
FA006000 <sub>H</sub>	FA0060FF <sub>H</sub>	256 byte	BPI SFF (access to EMEM core registers) (EMEM)	ok	ok
FA006100 <sub>H</sub>	FA00FFFF <sub>H</sub>	-	Reserved	BE	BE
FA010000 <sub>H</sub>	FA01FFFF <sub>H</sub>	64 Kbyte	FPI slave interface (MCDS)	ok	ok
FA020000 <sub>H</sub>	FA03FFFF <sub>H</sub>	-	Reserved	BE	BE
FA040000 <sub>H</sub>	FA0401FF <sub>H</sub>	512 byte	FPI slave interface (RIF0)	ok	ok
FA040200 <sub>H</sub>	FA0403FF <sub>H</sub>	512 byte	FPI slave interface (RIF1)	ok	ok
FA040400 <sub>H</sub>	FA6FFFFFF <sub>H</sub>	-	Reserved	BE	BE
FA700000 <sub>H</sub>	FA7000FF <sub>H</sub>	256 byte	SPU Lockstep Registers (SPULCKSTP)	ok	ok
FA700100 <sub>H</sub>	FA7FFFFFF <sub>H</sub>	-	Reserved	BE	BE
FA800000 <sub>H</sub>	FA8007FF <sub>H</sub>	2 Kbyte	SPU Registers (SPU0)	ok	ok
FA800800 <sub>H</sub>	FA9FFFFFF <sub>H</sub>	-	Reserved	BE	BE
FAA00000 <sub>H</sub>	FAA0FFFF <sub>H</sub>	64 Kbyte	SPU Configuration Memory (SPU0)	32	32
FAA10000 <sub>H</sub>	FABFFFFFF <sub>H</sub>	-	Reserved	BE	BE
FAC00000 <sub>H</sub>	FAC007FF <sub>H</sub>	2 Kbyte	SPU Registers (SPU1)	ok	ok
FAC00800 <sub>H</sub>	FADFFFFFF <sub>H</sub>	-	Reserved	BE	BE

## Memory Maps (MEMMAP)

**Table 4 Address Map as seen by Bus Masters on Bus BBB (cont'd)**

<b>Address Range</b>		<b>Size</b>	<b>Unit</b>	<b>Access Type</b>	
<b>from</b>	<b>to</b>			<b>Read</b>	<b>Write</b>
FAE00000 <sub>H</sub>	FAE0FFFF <sub>H</sub>	64 Kbyte	SPU Configuration Memory (SPU1)	32	32
FAE10000 <sub>H</sub>	FFFFFFF <sub>H</sub>	-	Reserved	BE	BE

**Memory Maps (MEMMAP)****2.6 Revision History****Table 5 Revision History**

Reference	Change to Previous Version	Comment
<b>V0.1.12</b>		
-	Formal change: for some memory ranges (e.g. "PFI0") the name was changed by appending "_NC" (e.g. "PFI0_NC") to ensure that derived tool files contain different symbols for cached and non-cached memory ranges.	-
<a href="#">Page 15</a>	Changed description of range starting at F0240000 from "SCR XRAM (PMS)" to "Standby Controller XRAM (PMS)".	-
<b>V0.1.13</b>		
-	No changes. Only version number changed to keep alignment with family address map.	-
<b>V0.1.14</b>		
-	No changes. Only version number changed to keep alignment with family address map.	-
<b>V0.1.15</b>		
-	No changes. Only version number changed to keep alignment with family address map.	-
<b>V0.1.16</b>		
-	No changes. Only version number changed to keep alignment with family address map.	-
<b>V0.1.17</b>		
-	No changes. Only version number changed to keep alignment with family address map.	-
<b>V0.1.18</b>		
-	No changes. Only version number changed to keep alignment with family address map.	-
<b>V0.1.19</b>		
-	No changes. Only version number changed to keep alignment with family address map.	
<b>V0.1.20</b>		
-	No changes. Only version number changed to keep alignment with family address map.	
<b>V0.1.21</b>		
<a href="#">Page 11</a> , <a href="#">Page 15</a>	In bus instances SPB and BBB several address ranges corrected to "BE".	

**TC39x-B Firmware**

### 3 TC39x-B Firmware

This chapter supplements the family documentation with device specific information for TC39x-B devices.

#### 3.1 Checker Software exit information for ALL CHECKS PASSED

Below the SCU\_STMEM3...SCU\_STMEM6 registers' content corresponding to "ALL CHECKS PASSED" result from Checker Software (CHSW) upon different device reset types is shown.

**Table 6 "ALL CHECKS PASSED" indication by CHSW for TC39x-B**

Reset type	Additional conditions	SCU_STMEM3	SCU_STMEM4	SCU_STMEM5	SCU_STMEM6
Cold power-on <sup>1)</sup>	--	A0F3FB1F <sub>H</sub>	00000001 <sub>H</sub>	A0F3FB1F <sub>H</sub>	A0F3FB1F <sub>H</sub>
Warm power-on	--	A0E3F82F <sub>H</sub>	00000001 <sub>H</sub>	A0E3F82F <sub>H</sub>	A0E3F82F <sub>H</sub>
System reset	--	20E0B84F <sub>H</sub>	00000001 <sub>H</sub>	20E0B84F <sub>H</sub>	20E0B84F <sub>H</sub>
Application reset	CCUCON5.GETHDIV<>0 CCUCON5.ADASDIV<>0	20E0088F <sub>H</sub>	00000001 <sub>H</sub>	20E0088F <sub>H</sub>	20E0088F <sub>H</sub>
	CCUCON5.GETHDIV<>0 CCUCON5.ADASDIV=0	20E0088F <sub>H</sub>	00C00001 <sub>H</sub>	2020088F <sub>H</sub>	20E0088F <sub>H</sub>
	CCUCON5.GETHDIV=0 CCUCON5.ADASDIV<>0	20E0088F <sub>H</sub>	00200001 <sub>H</sub>	20C0088F <sub>H</sub>	20E0088F <sub>H</sub>
	CCUCON5.GETHDIV=0 CCUCON5.ADASDIV=0	20E0088F <sub>H</sub>	00E00001 <sub>H</sub>	2000088F <sub>H</sub>	20E0088F <sub>H</sub>

- 1) Device start-up after LBIST execution is handled by AURIX™ TC3xx Firmware as cold power-on, therefore the SCU\_STMEMx values in this row apply also in such a case (after LBIST).

Note: *The result from some check(s) depends on additional conditions as follows:*

1. *The check for Gigabit Ethernet MAC module(s) calibration will fail after application reset, if the application software has not enabled GETH clock (in SCU\_CCUCON5.GETHDIV register) after the previous power-on/system reset(s) - meaning if the module is not used by application - therefore in such use-case anyway the check for this' module calibration is not relevant.*
2. *The check for RIF module(s) calibration will fail after application reset, if the application software has not enabled ADAS clock (in SCU\_CCUCON5.ADASDIV register) after the previous power-on/system reset(s) - meaning if the module is not used by application - therefore in such use-case anyway the check for this' module calibration is not relevant.*

#### 3.2 Revision History

**Table 7 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.1.0.1.14...V1.1.0.1.16</b>		
	No change	
<b>V1.1.0.1.17</b>		
<b>Table 6</b>	Footnote added, explaining FW handling after LBIST execution (documentation improvement only, no change in implementation)	

## TC39x-B Firmware

Table 7 Revision History

Reference	Change to Previous Version	Comment
<b>V1.1.0.1.18</b>		
-	No functional changes	

## On-Chip System Connectivity {and Bridges}

### 4 On-Chip System Connectivity {and Bridges}

Text with reference to family spec.

#### 4.1 TC39x-B Specific IP Configuration

**Table 8 TC39x-B specific configuration of DOM**

Parameter	DOM0	DOM1	DOM2
<b>Application Reset</b>	Application Reset	Application Reset	Application Reset
<b>Access only when any Endinit (SCU_WDTCPUxCON0.EI = 0 for any CPUx)</b>	ENDINIT	ENDINIT	ENDINIT
<b>Access only when Safety Endinit (SCU_SEICON.EI = 0)</b>	Safety ENDINIT	Safety ENDINIT	Safety ENDINIT
<b>Access only from HSM Master or HSM debug (or FPRO.PROINHSMCFG=0)</b>	HSM Access	HSM Access	HSM Access
<b>Access only when PSW = Supervisor Mode</b>	Supervisor Mode	Supervisor Mode	Supervisor Mode
<b>Access only when PSW = User Mode 0 or 1</b>	User Mode	User Mode	User Mode
<b>Access only when OCDS enabled</b>	Debug Mode	Debug Mode	Debug Mode
<b>Access only from Master x (when MOD_ACCEN0.ENx = 1 or MOD_ACCEN1.ENx = 1)</b>	Valid Master	Valid Master	Valid Master
<b>Access only from Master x (when MOD_ACCEN0.ENx = 1)</b>	Valid Master (0)	Valid Master (0)	Valid Master (0)
<b>Access only from Master x (when MOD_ACCEN1.ENx = 1)</b>	Valid Master (1)	Valid Master (1)	Valid Master (1)
<b>Number of SCI interfaces</b>	16	16	16
<b>sri base address</b>	F8700000 <sub>H</sub>	F88E0000 <sub>H</sub>	FB700000 <sub>H</sub>
<b>sri address range</b>	10000 <sub>H</sub>	10000 <sub>H</sub>	10000 <sub>H</sub>
<b>OLDA base address</b>	8FE00000 <sub>H</sub>		
<b>OLDA range</b>	80000 <sub>H</sub>		
<b>OLDA base address (non-cached)</b>	AFC00000 <sub>H</sub>		
<b>OLDA range (non-cached)</b>	80000 <sub>H</sub>		

## On-Chip System Connectivity {and Bridges}

### 4.2 TC39x-B Specific Register Set

#### Register Address Space Table

**Table 9 Register Address Space - DOM**

Module	Base Address	End Address	Note
(DOM0)	8FE00000 <sub>H</sub>	8FE7FFFF <sub>H</sub>	Online Data Acquisition (OLDA)
	AFE00000 <sub>H</sub>	AFE7FFFF <sub>H</sub>	Online Data Acquisition (OLDA)
DOM0	F8700000 <sub>H</sub>	F870FFFF <sub>H</sub>	sri slave interface
DOM1	F88E0000 <sub>H</sub>	F88EFFFF <sub>H</sub>	sri slave interface
DOM2	FB700000 <sub>H</sub>	FB70FFFF <sub>H</sub>	sri slave interface

#### Register Overview Table

**Table 10 Register Overview - DOM0 (ascending Offset Address)**

Short Name	Description	Offset Address	Access Mode		Page Number
			Read	Write	
DOM0_PECONx (x=0-15)	Protocol Error Control Register x	00000 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM0_PRIORIT Yx (x=0-15)	SCIx Arbiter Priority Register	00008 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM0_ERRADD Rx (x=0-15)	SCI x Error Address Capture Register	00010 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM0_ERRx (x=0-15)	SCI x Error Capture Register	00018 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM0_ID	Identification Register	00408 <sub>H</sub>	32,U,SV	BE	See Family Spec
DOM0_PESTAT	Protocol Error Status Register	00410 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM0_TIDSTAT	Transaction ID Status Register	00418 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM0_TIDEN	Transaction ID Enable Register	00420 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM0_BRCON	Domain 0 Bridge Control Register	00430 <sub>H</sub>	32,U,SV	32,P,SV	5

## On-Chip System Connectivity {and Bridges}

**Table 10 Register Overview - DOM0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
DOM0_ACCENO	Access Enable Register 0	004F0 <sub>H</sub>	32,U,SV	32,SV,SE	See Family Spec
DOM0_ACCEN1	Access Enable Register 1	004F8 <sub>H</sub>	32,U,SV	32,SV,SE	See Family Spec

**Table 11 Register Overview - DOM1 (ascending Offset Address)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
DOM1_PECONx (x=0-15)	Protocol Error Control Register x	00000 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM1_PRIORIT Yx (x=0-15)	SCIx Arbiter Priority Register	00008 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM1_ERRADD Rx (x=0-15)	SCI x Error Address Capture Register	00010 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM1_ERRx (x=0-15)	SCI x Error Capture Register	00018 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM1_ID	Identification Register	00408 <sub>H</sub>	32,U,SV	BE	See Family Spec
DOM1_PESTAT	Protocol Error Status Register	00410 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM1_TIDSTAT	Transaction ID Status Register	00418 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM1_TIDEN	Transaction ID Enable Register	00420 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM1_BRCON	Domain 1 Bridge Control Register	00430 <sub>H</sub>	32,U,SV	32,P,SV	5
DOM1_ACCENO	Access Enable Register 0	004F0 <sub>H</sub>	32,U,SV	32,SV,SE	See Family Spec
DOM1_ACCEN1	Access Enable Register 1	004F8 <sub>H</sub>	32,U,SV	32,SV,SE	See Family Spec

## On-Chip System Connectivity {and Bridges}

**Table 12 Register Overview - DOM2 (ascending Offset Address)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
DOM2_PECONx (x=0-15)	Protocol Error Control Register x	00000 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM2_PRIORIT Yx (x=0-15)	SCIx Arbiter Priority Register	00008 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM2_ERRADD Rx (x=0-15)	SCI x Error Address Capture Register	00010 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM2_ERRx (x=0-15)	SCI x Error Capture Register	00018 <sub>H</sub> + x*20 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM2_ID	Identification Register	00408 <sub>H</sub>	32,U,SV	BE	See Family Spec
DOM2_PESTAT	Protocol Error Status Register	00410 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM2_TIDSTAT	Transaction ID Status Register	00418 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM2_TIDEN	Transaction ID Enable Register	00420 <sub>H</sub>	32,U,SV	32,P,SV	See Family Spec
DOM2_BRCON	Domain 2 Bridge Control Register	00430 <sub>H</sub>	32,U,SV	32,P,SV	<b>6</b>
DOM2_ACCEN0	Access Enable Register 0	004F0 <sub>H</sub>	32,U,SV	32,SV,SE	See Family Spec
DOM2_ACCEN1	Access Enable Register 1	004F8 <sub>H</sub>	32,U,SV	32,SV,SE	See Family Spec

## On-Chip System Connectivity {and Bridges}

### 4.3 TC39x-B Specific Registers

#### 4.3.1 sri slave interface

##### Domain 0 Bridge Control Register

###### DOM0\_BRCON

###### Domain 0 Bridge Control Register

(00430<sub>H</sub>)

Application Reset Value: 0000 0200<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		0		0		1		0		0		0		OLDAE N	
rw		r		rw		rw		r		rw		r		rw	

Field	Bits	Type	Description
OLDAEN	0	rw	<b>Online Data Acquisition Enable</b> This bit is used to control trap generated for write accesses to the OLDA address range associated with this domain. 0 <sub>B</sub> Trap generated on a write access to the OLDA memory range. 1 <sub>B</sub> No trap generated on a write access to the OLDA memory range.
0	5:1, 8:7, 12:11, 31:20	r	<b>Reserved</b> Read as 0; shall be written with 0.
0	6, 10, 19:13	rw	<b>Reserved</b> Read as 0; shall be written with 0.
1	9	rw	<b>Reserved</b> Read as 1; shall be written with 1.

##### Domain 1 Bridge Control Register

###### DOM1\_BRCON

###### Domain 1 Bridge Control Register

(00430<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								0							

## On-Chip System Connectivity {and Bridges}

Field	Bits	Type	Description
0	31:0	r	<b>Reserved</b> Read as 0; shall be written with 0.

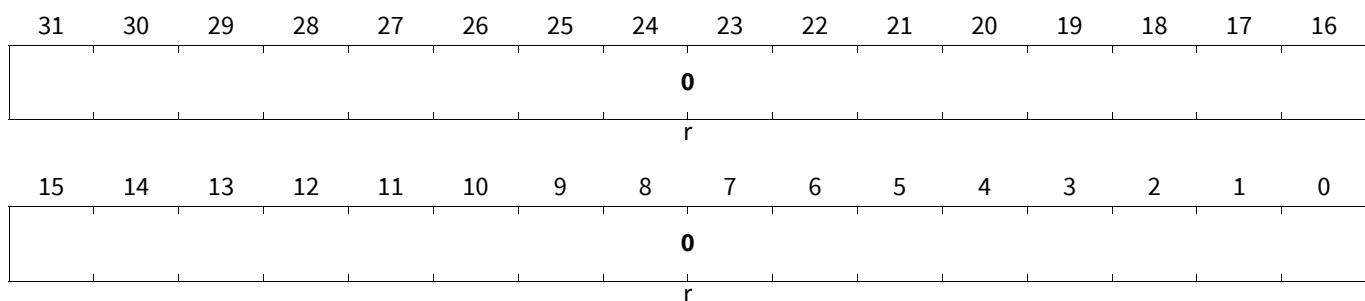
### Domain 2 Bridge Control Register

#### DOM2\_BRCON

##### Domain 2 Bridge Control Register

(00430<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>



Field	Bits	Type	Description
0	31:0	r	<b>Reserved</b> Read as 0; shall be written with 0.

## 4.4 Connectivity

No connections in TC39x-B

## 4.5 Interconnection Matrices

### 4.5.1 Domain 0 Interconnection Matrix

By default the crossbar connects MCIs to SCIs. The following connectivity matrix highlights (in red and yellow) the MCI to SCI interconnects that are non-standard in the TC39x-B. The unimplemented connections are redundant as they would not be useful (illegal or trapping) therefore do not restrict the functionality.

## On-Chip System Connectivity {and Bridges}

	S2S1 D0D2	S2S2 D0D2	LMU0	CPU3S	CPU3P	CPU2S	CPU2P	CPU1P	CPU1S	SCI10	SCI11	SCI12	SCI13	Default Slave
r/w	MCI has read write connectivity to SCI													SC15
r.o	MCI has only read connectivity to SCI													
x	MCI has no connectivity to SCI													
DMA MIFO														r/w
SFI F2S														r/w
CPU0														r/w
CPU1														r/w
CPU2														r/w
CPU3														r/w
S2S0 D1D0														r/w
HSSLO														
	MCI0	r/w	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x
	MCI1	r/w	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x
	MCI2	r/w	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x
	MCI3	r/w	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x
	MCI4	r/w	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x r/w
	MCI5	r/w	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x r/w
	MCI6	x	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x x
	MCI8	r/w	r/w	r/w	r.o	r/w	r.o	r/w	r.o	r/w	r/o	r/w	r/w	x r/w

## **Figure 1 TC39x-B Domain0 Connectivity Matrix**

#### **4.5.2 Domain 1 Interconnection Matrix**

By default the crossbar connects MCIs to SCIs. Following is a list which describes the MCI to SCI interconnects that are NOT implemented in the TC39x-B. The unimplemented connections are redundant as they would not be useful (illegal or trapping) therefore do not restrict the functionality.

## On-Chip System Connectivity {and Bridges}

	LMU2	LMU1	SC11	DAM1					
	SC10	SC11	SC10	SC11					
r/w	MCI has read write connectivity to SCI								
r.o	MCI has only read connectivity to SCI								
x	MCI has no connectivity to SCI								
GETH									
S2S3 D0D1	MCI0	r/w	r/w	r.o	r/w	r.o	r/w	r/w	r/w
CPU4	MCI1	r/w	x	r.o	r/w	r.o	r/w	r/w	r/w
CPU5	MCI2	r/w	r/w	r.o	r/w	r.o	r/w	r/w	r/w
	MCI3	r/w	r/w	r.o	r/w	r.o	r/w	r/w	r/w
HSSL1									
	MC15	r/w	r/w	r.o	r/w	r.o	r/w	r/w	r/w

**Figure 2 TC39x-B Domain1 Connectivity Matrix**

#### **4.5.3 Domain 2 Interconnection Matrix**

By default the crossbar connects MCIs to SCIs. Following is a list which describes the MCI to SCI interconnects that are NOT implemented in the TC39x-B. The unimplemented connections are redundant as they would not be useful (illegal or trapping) therefore do not restrict the functionality.

 r/w	MCI has read write connectivity to SCI													
 r.o	MCI has only read connectivity to SCI													
 x	MCI has no connectivity to SCI													
S2S2 D0D2														
S2S1 D0D2														
S2S4 D1D2														
DMA MIF1														
DMA MIF2														
	MCI0	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	
	MCI1	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	
	MCI2	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	 r/w	
	MCI3	 r/w	 x	 r/w	 x	 r/w	 x	 r/w	 x	 r/w	 x	 r/w	 x	
	MCI4	 r/w	 x	 x	 r/w	 x	 r/w	 x	 r/w	 x	 r/w	 x	 r/w	

**Figure 3 TC39x-B Domain 2 Connectivity Matrix**

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**On-Chip System Connectivity {and Bridges}**

## 4.6 Revision History

**Table 13 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.1.13</b>		
<b>Page 5</b>	Updated BRCON bitfield to show that bit 9 while reserved will read as 1 and should be updated to 1 (The bitfield was incorrectly showing value 0 previously). Restored correct access permission (r/w) for bit fields which are not intended for customer function.	
<b>V1.1.14</b>		
	No change.	
<b>V1.1.15</b>		
	No change.	
<b>V1.1.16</b>		
	No change.	
<b>V1.1.17</b>		
	No change.	

## 4.7 FPI Bus Control Units (SBCU, EBCU)

This chapter supplements the family documentation with device specific information for TC39x-B.

### 4.7.1 TC39x-B Specific IP Configuration

The TC39x-B includes two FPI Bus instances. Each FPI Bus instances has its dedicated Bus Control Unit:

**Table 14 Register Address Space - BCU**

Module	Base Address	End Address	Note
(EBCU)	F0000000 <sub>H</sub>	FFFFFFFFFF <sub>H</sub>	FPI default slave
EBCU	FA000100 <sub>H</sub>	FA0001FF <sub>H</sub>	BCU Registers
(SBCU)	F0000000 <sub>H</sub>	F7FFFFFF <sub>H</sub>	FPI default slave
SBCU	F0030000 <sub>H</sub>	F00300FF <sub>H</sub>	BCU Registers

- System Peripheral Bus (SPB) -> SBCU. The SBCU registers are described in [Chapter 4.7.2](#)
- Back Bone bus (BBB) -> EBCU. The EBCU registers are described in [Chapter 4.7.3](#)

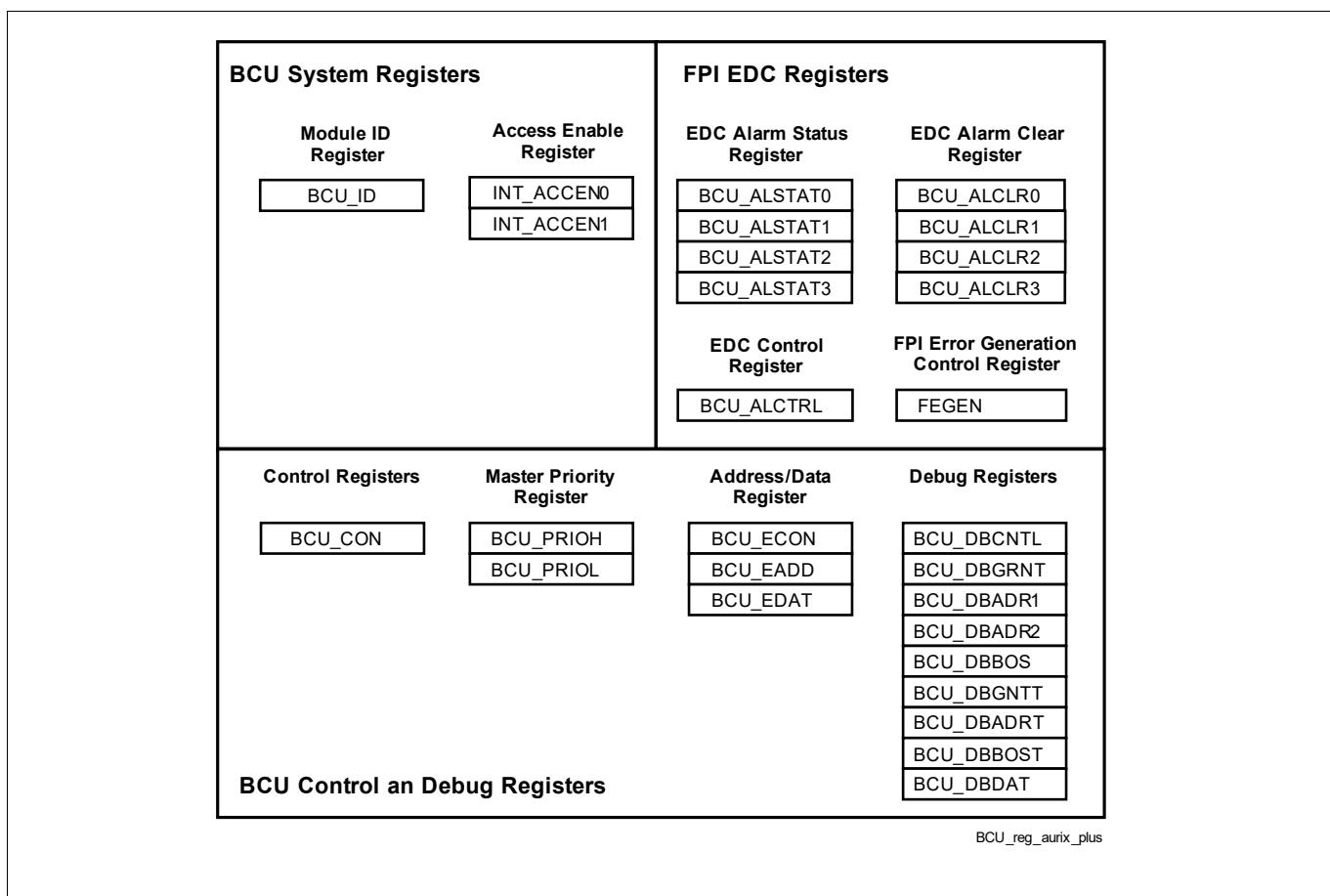
#### 4.7.2 SBCU Control Unit Registers

**Figure 4** and **Table 15** are showing the address maps with all registers of the System Bus Control Unit (SBCU) module.

List of used Reset Class abbreviations:

- Reset Class 1 -> Debug Reset, Power-on Reset (see chapter SCU / Reset Types)
- Reset Class 3 -> Application Reset, System Reset, Power-on Reset (see chapter SCU / Reset Types)

#### SBCU Control Registers Overview



**Figure 4** SBCU Registers

**Table 15** Register Overview - SBCU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SBCU_ID	Module Identification Register	0008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SBCU_CON	BCU Control Register	0010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
SBCU_PRIOH	Arbiter Priority Register High	0014 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>14</b>

**Table 15 Register Overview - SBCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SBCU_PRIOL	Arbiter Priority Register Low	0018 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>15</b>
SBCU_ECON	BCU Error Control Capture Register	0020 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
SBCU_EADD	BCU Error Address Capture Register	0024 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
SBCU_EDAT	BCU Error Data Capture Register	0028 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
SBCU_DBCNTL	BCU Debug Control Register	0030 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBGRNT	SBCU Debug Grant Mask Register	0034 <sub>H</sub>	U,SV	SV,P	Debug Reset	<b>16</b>
SBCU_DBADR1	BCU Debug Address 1 Register	0038 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBADR2	BCU Debug Address 2 Register	003C <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBBOS	BCU Debug Bus Operation Signals Register	0040 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBGNTT	SBCU Debug Trapped Master Register	0044 <sub>H</sub>	U,SV	BE	Debug Reset	<b>18</b>
SBCU_DBADRT	BCU Debug Trapped Address Register	0048 <sub>H</sub>	U,SV	BE	Debug Reset	See Family Spec
SBCU_DBBOST	BCU Debug Trapped Bus Operation Signals Register	004C <sub>H</sub>	U,SV	BE	Debug Reset	See Family Spec
SBCU_DBDAT	BCU Debug Data Status Register	0050 <sub>H</sub>	U,SV	BE	Debug Reset	See Family Spec
SBCU_ALSTATx (x=0-3)	BCU EDC Alarm Status Register x	0060 <sub>H</sub> +x *4	U,SV	SV,P	Application Reset	<b>19</b>
SBCU_ALCLRx (x=0-3)	BCU EDC Alarm Clear Register x	0070 <sub>H</sub> +x *4	U,SV	SV,P	Application Reset	See Family Spec

**Table 15 Register Overview - SBCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SBCU_ALCTRL	BCU EDC Alarm Control Register	0080 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
SBCU_FEGEN	FPI Error Generation Control Register	0084 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
SBCU_ACCEN1	Access Enable Register 1	00F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
SBCU_ACCENO	Access Enable Register 0	00FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

#### 4.7.2.1 SBCU Control Registers Descriptions

Note: For all PRIOH / PRIOL bit fields, a lower number has a higher priority in the arbitration round than a higher one.

##### Arbiter Priority Register High

###### SBCU\_PRIOH

###### Arbiter Priority Register High

(0014<sub>H</sub>)Application Reset Value: FEDC 8888<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>RESERVED</b>				<b>RESERVED</b>				<b>HSMCMI</b>				<b>HSMRMI</b>			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CPU5</b>				<b>CPU4</b>				<b>CPU3</b>				<b>CPU2</b>			
rw				rw				rw				rw			

Field	Bits	Type	Description
<b>CPU2</b>	3:0	rw	<b>CPU2 Priority (Index 8)</b> This bit field defines the priority on the SPB for CPU2 access to the SPB.
<b>CPU3</b>	7:4	rw	<b>CPU3 Priority (Index 9)</b> This bit field defines the priority on the SPB for CPU3 access to the SPB.
<b>CPU4</b>	11:8	rw	<b>CPU4 Priority (Index 10)</b> This bit field defines the priority on the SPB for CPU4 access to the SPB.
<b>CPU5</b>	15:12	rw	<b>CPU5 11 Priority (Index 11)</b> This bit field defines the priority on the SPB for CPU5 access to the SPB.
<b>HSMRMI</b>	19:16	rw	<b>HSMRMI Priority (Index 12)</b> This bit field defines the priority on the SPB for HSMRMI access to the SPB.
<b>HSMCMI</b>	23:20	rw	<b>HSMCMI Priority (Index 13)</b> This bit field defines the priority on the SPB for HSMCMI access to the SPB.
<b>RESERVED</b>	27:24, 31:28	rw	<b>Reserved</b> Read as reset value or last written value; should be written with 0.

## Arbiter Priority Register Low

### SBCU\_PRIOL

**Arbiter Priority Register Low** **(0018<sub>H</sub>)** **Application Reset Value: 8854 3210<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>CPU1</b>				<b>CPU0</b>				<b>RESERVED</b>				<b>HSSL1</b>			
rw					rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>HSSL0</b>				<b>SDMMC</b>				<b>RESERVED</b>				<b>DMA</b>			
rw					rw				rw				rw		

Field	Bits	Type	Description
<b>DMA</b>	3:0	rw	<b>DMA / Cerberus Priority (Index 0)</b> This bit field defines the priority on the SPB for DMA and Cerberus access to the SPB.
<b>RESERVED</b>	7:4, 23:20	rw	<b>Reserved</b> Read as reset value or last written value; should be written with 0.
<b>SDMMC</b>	11:8	rw	<b>SDMMC Priority (Index 2)</b> This bit field defines the priority on the SPB for SDMMC access to the SPB.
<b>HSSL0</b>	15:12	rw	<b>HSSL0 Priority (Index 3)</b> This bit field defines the priority on the SPB for HSSL0 access to the SPB.
<b>HSSL1</b>	19:16	rw	<b>HSSL1 Priority (Index 4)</b> This bit field defines the priority on the SPB for HSSL1 access to the SPB.
<b>CPU0</b>	27:24	rw	<b>CPU0 Priority (Index 6)</b> This bit field defines the priority on the SPB for CPU0 access to the SPB.
<b>CPU1</b>	31:28	rw	<b>CPU1 Priority (Index 7)</b> This bit field defines the priority on the SPB for CPU1 access to the SPB.

#### 4.7.2.2 SBCU OCDS Registers Descriptions

##### SBCU Debug Grant Mask Register

**SBCU\_DBGRNT****SBCU Debug Grant Mask Register**(0034<sub>H</sub>)**Debug Reset Value: 0000 FFFF<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	HSMC MI	HSMR MI	CPU5	CPU4	CPU3	CPU2	CPU1	CPU0	1	HSSL1	HSSL0	SDMMC C	1	DMA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>DMA</b>	0	rw	<b>DMA / Cerberus Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with DMA / Cerberus as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with DMA / Cerberus as bus master are disabled for grant trigger event generation.
<b>SDMMC</b>	2	rw	<b>SDMMC Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with SDMMC as bus master are enabled for grant trigger event generation 1 <sub>B</sub> FPI Bus transactions with SDMMC as bus master are disabled for grant trigger event generation
<b>HSSL0</b>	3	rw	<b>HSSL0 Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with HSSL0 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with HSSL0 as bus master are disabled for grant trigger event generation.
<b>HSSL1</b>	4	rw	<b>HSSL1 Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with HSSL1 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with HSSL1 as bus master are disabled for grant trigger event generation.
<b>CPU0</b>	6	rw	<b>CPU0 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU0 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with CPU as bus master are disabled for grant trigger event generation.
<b>CPU1</b>	7	rw	<b>CPU1 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU1 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with CPU1 as bus master are disabled for grant trigger event generation.

Field	Bits	Type	Description
CPU2	8	rw	<b>CPU2 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU2 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with CPU2 as bus master are disabled for grant trigger event generation.
CPU3	9	rw	<b>CPU3 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU3 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with CPU3 as bus master are disabled for grant trigger event generation.
CPU4	10	rw	<b>CPU4 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU4 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with CPU4 as bus master are disabled for grant trigger event generation.
CPU5	11	rw	<b>CPU5 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU5 as bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions with CPU5 as bus master are disabled for grant trigger event generation.
HSMRMI	12	rw	<b>HSM Register Master Interface Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions requested by the HSM bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions requested by the HSM bus master are disabled for grant trigger event generation.
HSMCMI	13	rw	<b>HSM Cache Master Interface Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions requested by the HSM bus master are enabled for grant trigger event generation. 1 <sub>B</sub> FPI Bus transactions requested by the HSM bus master are disabled for grant trigger event generation.
1	1, 5, 14, 15	rw	<b>Reserved</b> Read as 1 after reset; reading these bits will return the value last written.
0	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## SBCU Debug Trapped Master Register

### SBCU\_DBGNTT

#### SBCU Debug Trapped Master Register

(0044<sub>H</sub>)Debug Reset Value: 0000 FFFF<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
rh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	HSMC MI	HSMR MI	CPU5	CPU4	CPU3	CPU2	CPU1	CPU0	1	HSSL1	HSSL0	SDMM C	1	DMA
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DMA	0	rh	<b>DMA / Cerberus FPI Bus Master Status</b> 0 <sub>B</sub> The DMA or Cerberus was the FPI bus master. 1 <sub>B</sub> Neither DMA nor Cerberus was the FPI Bus master.
SDMMC	2	rh	<b>SDMMC FPI Bus Master Status</b> This bit indicates whether the SDMMC was FPI Bus master when the break trigger event occurred. 0 <sub>B</sub> The SDMMC was the FPI bus master. 1 <sub>B</sub> The SDMMC was not the FPI Bus master.
HSSL0	3	rh	<b>HSSL 0 FPI Bus Master Status</b> This bit indicates whether the HSSL 0 was FPI Bus master when the break trigger event occurred. 0 <sub>B</sub> The HSSL0 was the FPI bus master. 1 <sub>B</sub> The HSSL0 was not the FPI Bus master.
HSSL1	4	rh	<b>HSSL 1 FPI Bus Master Status</b> This bit indicates whether the HSSL 1 was FPI Bus master when the break trigger event occurred. 0 <sub>B</sub> The HSSL1 was the FPI bus master. 1 <sub>B</sub> The HSSL1 was not the FPI Bus master.
CPU0	6	rh	<b>CPU0 FPI Bus Master Status</b> This bit indicates whether the CPU0 was FPI Bus master when the break trigger event occurred. 0 <sub>B</sub> The CPU0 was the FPI Bus master. 1 <sub>B</sub> The CPU0 was not the FPI Bus master.
CPU1	7	rh	<b>CPU1 FPI Bus Master Status</b> This bit indicates whether the CPU1 was FPI Bus master when the break trigger event occurred. 0 <sub>B</sub> The CPU1 was the FPI Bus master. 1 <sub>B</sub> The CPU1 was not the FPI Bus master.

Field	Bits	Type	Description
CPU2	8	rh	<b>CPU2 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU2 as bus master are enabled for grant trigger event generation 1 <sub>B</sub> FPI Bus transactions with CPU2 as bus master are disabled for grant trigger event generation
CPU3	9	rh	<b>CPU3 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU3 as bus master are enabled for grant trigger event generation 1 <sub>B</sub> FPI Bus transactions with CPU3 as bus master are disabled for grant trigger event generation
CPU4	10	rh	<b>CPU4 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU4 as bus master are enabled for grant trigger event generation 1 <sub>B</sub> FPI Bus transactions with CPU4 as bus master are disabled for grant trigger event generation
CPU5	11	rh	<b>CPU5 Grant Trigger Enable</b> 0 <sub>B</sub> FPI Bus transactions with CPU5 as bus master are enabled for grant trigger event generation 1 <sub>B</sub> FPI Bus transactions with CPU5 as bus master are disabled for grant trigger event generation
HSMRMI	12	rh	<b>HSM Register FPI Bus Master Interface Status</b> This bit indicates whether the HSM was FPI Bus master when the break trigger event occurred. 0 <sub>B</sub> HSMRMI was the FPI bus master. 1 <sub>B</sub> HSMRMI was not the FPI Bus master.
HSMCMI	13	rh	<b>HSM Cache FPI Bus Master Interface Status</b> This bit indicates whether the HSM was FPI Bus master when the break trigger event occurred. 0 <sub>B</sub> HSMCMI was the FPI bus master. 1 <sub>B</sub> HSMCMI was not the FPI Bus master.
1	1, 5, 14, 15	rh	<b>Reserved</b> Read as 1 after reset; reading these bits will return the value last written.
0	31:16	rh	<b>Reserved</b> Read as 1 after reset; reading these bits will return the value last written.

### BCU EDC Alarm Status Register x

The BCU provides one Alarm Status Register bit for each implemented FPI master and FPI slave.

Register bits without constant definition are reserved in this product.

**SBCU\_ALSTAT<sub>x</sub> (x=0)****BCU EDC Alarm Status Register x****(0060<sub>H</sub>+x\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>AL31</b>	<b>AL30</b>	<b>AL29</b>	<b>AL28</b>	<b>AL27</b>	<b>AL26</b>	<b>AL25</b>	<b>AL24</b>	<b>AL23</b>	<b>AL22</b>	<b>AL21</b>	<b>AL20</b>	<b>AL19</b>	<b>AL18</b>	<b>AL17</b>	<b>AL16</b>
rh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>AL15</b>	<b>AL14</b>	<b>AL13</b>	<b>AL12</b>	<b>AL11</b>	<b>AL10</b>	<b>AL09</b>	<b>AL08</b>	<b>AL07</b>	<b>AL06</b>	<b>AL05</b>	<b>AL04</b>	<b>AL03</b>	<b>AL02</b>	<b>AL01</b>	<b>AL00</b>
rh															

Field	Bits	Type	Description
<b>ALy (y=00)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>SBCU_S</b> , an EDC error was detected in an active phase of the SBCU Slave Interface.
<b>ALy (y=01)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>DMA_S</b> ,
<b>ALy (y=02)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>IR_S</b> ,
<b>ALy (y=03)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>SFI_F2S_S</b> ,
<b>ALy (y=04)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>SCU_S</b> ,
<b>ALy (y=05)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>SMU_S</b> ,
<b>ALy (y=06)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>PMC_SCR_S</b> ,
<b>ALy (y=07)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>MTU_S</b> ,
<b>ALy (y=08)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>IOM_S</b> ,
<b>ALy (y=09,21)</b>	y	rh	<b>Alarm y</b>
<b>ALy (y=10)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ASCLIN01_S</b> ,
<b>ALy (y=11)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ASCLIN23_S</b> ,
<b>ALy (y=12)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ASCLIN45_S</b> ,
<b>ALy (y=13)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ASCLIN67_S</b> ,
<b>ALy (y=14)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>QSPI0_S</b> ,
<b>ALy (y=15)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>QSPI1_S</b> ,

Field	Bits	Type	Description
ALy (y=16)	y	rh	Alarm y 1_B QSPI2_S,
ALy (y=17)	y	rh	Alarm y 1_B QSPI3_S,
ALy (y=18)	y	rh	Alarm y 1_B QSPI4_S,
ALy (y=19)	y	rh	Alarm y 1_B QSPI5_S,
ALy (y=20)	y	rh	Alarm y 1_B FCEO_S,
ALy (y=22)	y	rh	Alarm y 1_B STM0_S,
ALy (y=23)	y	rh	Alarm y 1_B STM1_S,
ALy (y=24)	y	rh	Alarm y 1_B STM2_S,
ALy (y=25)	y	rh	Alarm y 1_B STM3_S,
ALy (y=26)	y	rh	Alarm y 1_B STM4_S,
ALy (y=27)	y	rh	Alarm y 1_B STM5_S,
ALy (y=28)	y	rh	Alarm y 1_B PSI5_S,
ALy (y=29)	y	rh	Alarm y 1_B PSI5S_S,
ALy (y=30)	y	rh	Alarm y 1_B ERAY0_S,
ALy (y=31)	y	rh	Alarm y 1_B ERAY1_S,

**SBCU\_ALSTATx (x=1)****BCU EDC Alarm Status Register x****(0060<sub>H</sub>+x\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>AL31</b>	<b>AL30</b>	<b>AL29</b>	<b>AL28</b>	<b>AL27</b>	<b>AL26</b>	<b>AL25</b>	<b>AL24</b>	<b>AL23</b>	<b>AL22</b>	<b>AL21</b>	<b>AL20</b>	<b>AL19</b>	<b>AL18</b>	<b>AL17</b>	<b>AL16</b>
rh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>AL15</b>	<b>AL14</b>	<b>AL13</b>	<b>AL12</b>	<b>AL11</b>	<b>AL10</b>	<b>AL09</b>	<b>AL08</b>	<b>AL07</b>	<b>AL06</b>	<b>AL05</b>	<b>AL04</b>	<b>AL03</b>	<b>AL02</b>	<b>AL01</b>	<b>AL00</b>
rh															

Field	Bits	Type	Description
<b>ALy (y=00)</b>	y	rh	<b>Alarm y</b> 1_B <b>GPT12_S</b> , an EDC error was detected in an active phase of the GPT12 Slave Interface.
<b>ALy (y=01)</b>	y	rh	<b>Alarm y</b> 1_B <b>CCU6_S</b> ,
<b>ALy (y=02)</b>	y	rh	<b>Alarm y</b> 1_B <b>GTM_S</b> ,
<b>ALy (y=03)</b>	y	rh	<b>Alarm y</b> 1_B <b>MSC0_S</b> ,
<b>ALy (y=04)</b>	y	rh	<b>Alarm y</b> 1_B <b>MSC1_S</b> ,
<b>ALy (y=05)</b>	y	rh	<b>Alarm y</b> 1_B <b>MSC2_S</b> ,
<b>ALy (y=06)</b>	y	rh	<b>Alarm y</b> 1_B <b>MSC3_S</b> ,
<b>ALy (y=07)</b>	y	rh	<b>Alarm y</b> 1_B <b>SENT_S</b> ,
<b>ALy (y=08)</b>	y	rh	<b>Alarm y</b> 1_B <b>ETH_S</b> ,
<b>ALy (y=09)</b>	y	rh	<b>Alarm y</b> 1_B <b>EVADC_S</b> ,
<b>ALy (y=10)</b>	y	rh	<b>Alarm y</b> 1_B <b>EDSADC_S</b> ,
<b>ALy (y=11)</b>	y	rh	<b>Alarm y</b> 1_B <b>HSM_S</b> ,
<b>ALy (y=12)</b>	y	rh	<b>Alarm y</b> 1_B <b>HSSL0_S</b> ,
<b>ALy (y=13)</b>	y	rh	<b>Alarm y</b> 1_B <b>CAN0_S</b> ,
<b>ALy (y=14)</b>	y	rh	<b>Alarm y</b> 1_B <b>CAN1_S</b> ,
<b>ALy (y=15)</b>	y	rh	<b>Alarm y</b> 1_B <b>CAN2_S</b> ,
<b>ALy (y=16)</b>	y	rh	<b>Alarm y</b> 1_B <b>I2C0_S</b> ,
<b>ALy (y=17)</b>	y	rh	<b>Alarm y</b> 1_B <b>I2C1_S</b> ,
<b>ALy (y=18)</b>	y	rh	<b>Alarm y</b> 1_B <b>HSSL1_S</b> ,
<b>ALy (y=19)</b>	y	rh	<b>Alarm y</b> 1_B <b>CONVCTRL_S</b> ,

Field	Bits	Type	Description
ALy (y=20)	y	rh	Alarm y 1 <sub>B</sub> ASCLIN89_S,
ALy (y=21)	y	rh	Alarm y 1 <sub>B</sub> ASCLIN1011_S,
ALy (y=22-27)	y	rh	Alarm y
ALy (y=28)	y	rh	Alarm y 1 <sub>B</sub> HSPDM_SRAM_S,
ALy (y=29)	y	rh	Alarm y 1 <sub>B</sub> HSPDM_SFR_S,
ALy (y=30)	y	rh	Alarm y 1 <sub>B</sub> SDMMC_S,
ALy (y=31)	y	rh	Alarm y 1 <sub>B</sub> CERBERUS_S,

**SBCU\_ALSTATx (x=2)****BCU EDC Alarm Status Register x****(0060<sub>H</sub>+x\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	AL30	AL29	AL28	AL27	AL26	AL25	AL24	AL23	AL22	AL21	AL20	AL19	AL18	AL17	AL16
rh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	AL14	AL13	AL12	AL11	AL10	AL09	AL08	AL07	AL06	AL05	AL04	AL03	AL02	AL01	AL00
rh															

Field	Bits	Type	Description
ALy (y=00)	y	rh	Alarm y 1 <sub>B</sub> P00_S, an EDC error was detected in an active phase of the Port 00 Slave Interface.
ALy (y=01)	y	rh	Alarm y 1 <sub>B</sub> P01_S,
ALy (y=02)	y	rh	Alarm y 1 <sub>B</sub> P02_S,
ALy (y=03,10,18,24)	y	rh	Alarm y
ALy (y=04)	y	rh	Alarm y 1 <sub>B</sub> P10_S,
ALy (y=05)	y	rh	Alarm y 1 <sub>B</sub> P11_S,
ALy (y=06)	y	rh	Alarm y 1 <sub>B</sub> P12_S,

Field	Bits	Type	Description
<b>ALy (y=07)</b>	y	rh	<b>Alarm y</b> 1_B P13_S,
<b>ALy (y=08)</b>	y	rh	<b>Alarm y</b> 1_B P14_S,
<b>ALy (y=09)</b>	y	rh	<b>Alarm y</b> 1_B P15_S,
<b>ALy (y=11)</b>	y	rh	<b>Alarm y</b> 1_B P20_S,
<b>ALy (y=12)</b>	y	rh	<b>Alarm y</b> 1_B P21_S,
<b>ALy (y=13)</b>	y	rh	<b>Alarm y</b> 1_B P22_S,
<b>ALy (y=14)</b>	y	rh	<b>Alarm y</b> 1_B P23_S,
<b>ALy (y=15)</b>	y	rh	<b>Alarm y</b> 1_B P24_S,
<b>ALy (y=16)</b>	y	rh	<b>Alarm y</b> 1_B P25_S,
<b>ALy (y=17)</b>	y	rh	<b>Alarm y</b> 1_B P26_S,
<b>ALy (y=19)</b>	y	rh	<b>Alarm y</b> 1_B P30_S,
<b>ALy (y=20)</b>	y	rh	<b>Alarm y</b> 1_B P31_S,
<b>ALy (y=21)</b>	y	rh	<b>Alarm y</b> 1_B P32_S,
<b>ALy (y=22)</b>	y	rh	<b>Alarm y</b> 1_B P33_S,
<b>ALy (y=23)</b>	y	rh	<b>Alarm y</b> 1_B P34_S,
<b>ALy (y=25)</b>	y	rh	<b>Alarm y</b> 1_B P40_S,
<b>ALy (y=26)</b>	y	rh	<b>Alarm y</b> 1_B P41_S,
<b>ALy (y=27)</b>	y	rh	<b>Alarm y</b> 1_B P50_S,
<b>ALy (y=28)</b>	y	rh	<b>Alarm y</b> 1_B P51_S,
<b>ALy (y=29)</b>	y	rh	<b>Alarm y</b> 1_B HSCT0_S,
<b>ALy (y=30)</b>	y	rh	<b>Alarm y</b> 1_B HSCT1_S,

Field	Bits	Type	Description
ALy (y=31)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>SBCU_M</b> , an EDC error was detected in an active phase of the SBCU Master Interface.

**SBCU\_ALSTATx (x=3)****BCU EDC Alarm Status Register x****(0060<sub>H</sub>+x\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>AL31</b>	<b>AL30</b>	<b>AL29</b>	<b>AL28</b>	<b>AL27</b>	<b>AL26</b>	<b>AL25</b>	<b>AL24</b>	<b>AL23</b>	<b>AL22</b>	<b>AL21</b>	<b>AL20</b>	<b>AL19</b>	<b>AL18</b>	<b>AL17</b>	<b>AL16</b>
rh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>AL15</b>	<b>AL14</b>	<b>AL13</b>	<b>AL12</b>	<b>AL11</b>	<b>AL10</b>	<b>AL09</b>	<b>AL08</b>	<b>AL07</b>	<b>AL06</b>	<b>AL05</b>	<b>AL04</b>	<b>AL03</b>	<b>AL02</b>	<b>AL01</b>	<b>AL00</b>
rh															

Field	Bits	Type	Description
ALy (y=00)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>A_EN</b> , multiple output enables active: A_EN_N (Master)
ALy (y=01)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ABORT_EN</b> , multiple output enables active: ABORT_EN_N (Master)
ALy (y=02)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ACK_EN</b> , multiple output enables active: ACK_EN_N (Default Master and Slave)
ALy (y=03)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>D_EN</b> , multiple output enables active: D_EN_N (Master and Slave)
ALy (y=04-15,17,21,30-31)	y	rh	<b>Alarm y</b>
ALy (y=16)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>DMA_M</b> , an EDC error was detected in an active phase of the DMA / Cerberus Master Interface.
ALy (y=18)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>SDMMC_M</b> ,
ALy (y=19)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>HSSL0_M</b> ,
ALy (y=20)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>HSSL1_M</b> ,
ALy (y=22)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>CPU0_M</b> ,
ALy (y=23)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>CPU1_M</b> ,
ALy (y=24)	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>CPU2_M</b> ,

Field	Bits	Type	Description
ALy (y=25)	y	rh	<b>Alarm y</b> 1_B CPU3_M,
ALy (y=26)	y	rh	<b>Alarm y</b> 1_B CPU4_M,
ALy (y=27)	y	rh	<b>Alarm y</b> 1_B CPU5_M,
ALy (y=28)	y	rh	<b>Alarm y</b> 1_B HSMRMI_M,
ALy (y=29)	y	rh	<b>Alarm y</b> 1_B HSMCMI_M,

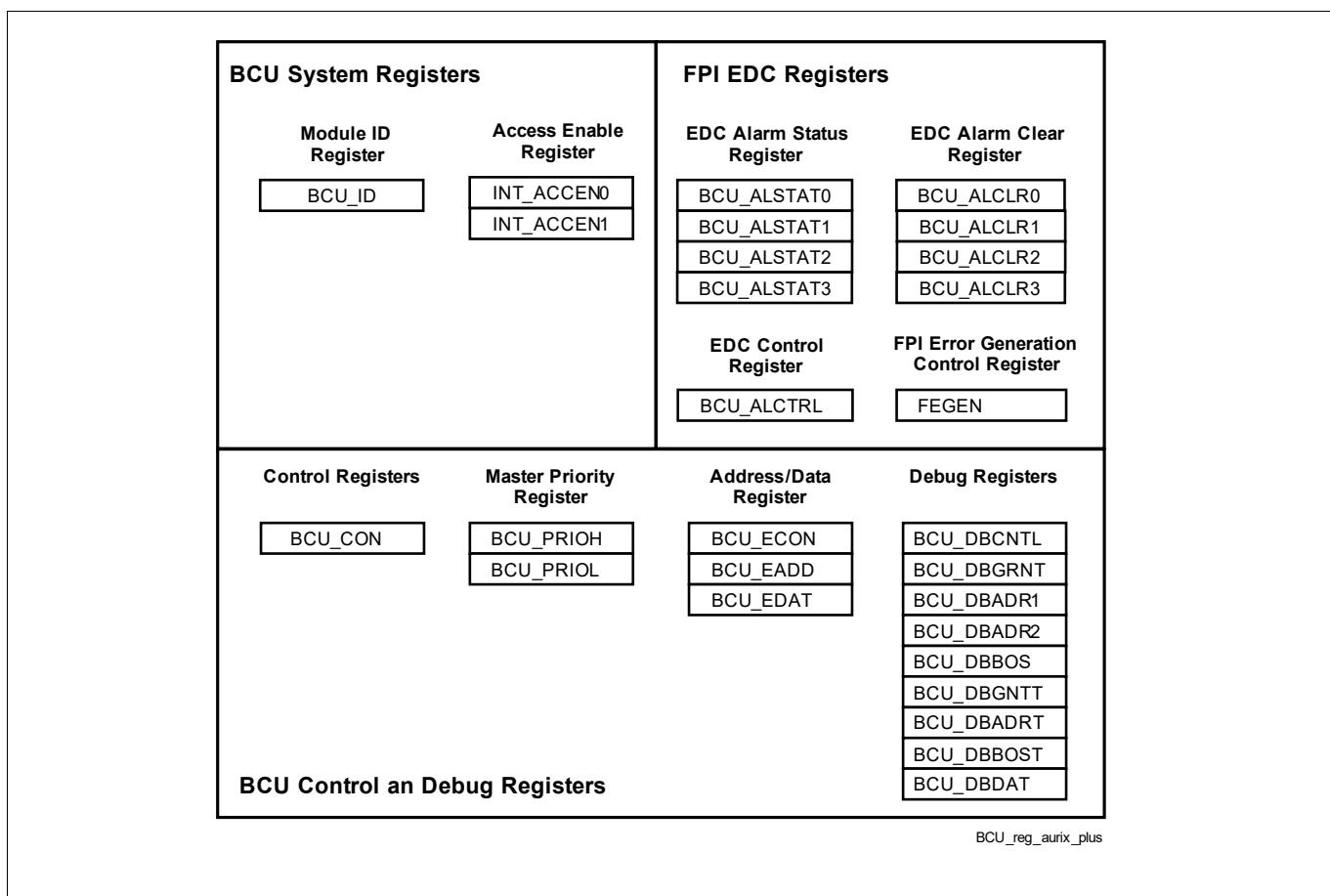
#### 4.7.3 EBCU Control Unit Registers

**Figure 5** and **Table 16** are showing the address maps with all registers of the Back Bone Bus (BBB) Bus Control Unit (EBCU) module.

List of used Reset Class abbreviations:

- Reset Class 1 -> Debug Reset, Power-on Reset (see chapter SCU / Reset Types)
- Reset Class 3 -> Application Reset, System Reset, Power-on Reset (see chapter SCU / Reset Types)

#### EBCU Control Registers Overview



**Figure 5** EBCU Registers

**Table 16** Register Overview - EBCU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
EBCU_ID	Module Identification Register	0008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
EBCU_CON	BCU Control Register	0010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
EBCU_PRIOH	Arbiter Priority Register High	0014 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>30</b>

**Table 16 Register Overview - EBCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EBCU_PRIOL	Arbiter Priority Register Low	0018 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>30</b>
EBCU_ECON	BCU Error Control Capture Register	0020 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
EBCU_EADD	BCU Error Address Capture Register	0024 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
EBCU_EDAT	BCU Error Data Capture Register	0028 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
EBCU_DBCNTL	BCU Debug Control Register	0030 <sub>H</sub>	U,SV	SV,P	Debug Reset	<b>32</b>
EBCU_DBGRNT	EBCU Debug Grant Mask Register	0034 <sub>H</sub>	U,SV	SV,P	Debug Reset	<b>34</b>
EBCU_DBADR1	BCU Debug Address 1 Register	0038 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
EBCU_DBADR2	BCU Debug Address 2 Register	003C <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
EBCU_DBBOS	BCU Debug Bus Operation Signals Register	0040 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
EBCU_DBGNTT	EBCU Debug Trapped Master Register	0044 <sub>H</sub>	U,SV	BE	Debug Reset	<b>35</b>
EBCU_DBADRT	BCU Debug Trapped Address Register	0048 <sub>H</sub>	U,SV	BE	Debug Reset	See Family Spec
EBCU_DBHOST	BCU Debug Trapped Bus Operation Signals Register	004C <sub>H</sub>	U,SV	BE	Debug Reset	See Family Spec
EBCU_DBDDAT	BCU Debug Data Status Register	0050 <sub>H</sub>	U,SV	BE	Debug Reset	See Family Spec
EBCU_ALSTATx (x=0-3)	BCU EDC Alarm Status Register x	0060 <sub>H</sub> +x *4	U,SV	SV,P	Application Reset	<b>36</b>
EBCU_ALCLRx (x=0-3)	BCU EDC Alarm Clear Register x	0070 <sub>H</sub> +x *4	U,SV	SV,P	Application Reset	See Family Spec
EBCU_ALCTRL	BCU EDC Alarm Control Register	0080 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec

**Table 16 Register Overview - EBCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EBCU_FEGEN	FPI Error Generation Control Register	0084 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
EBCU_ACCEN1	Access Enable Register 1	00F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
EBCU_ACCEN0	Access Enable Register 0	00FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

#### 4.7.3.1 EBCU Control Registers Descriptions

Note: For all PRIOH / PRIOL bit fields, a lower number has a higher priority in the arbitration round than a higher one.

##### Arbiter Priority Register High

###### EBCU\_PRIOH

###### Arbiter Priority Register High

(0014<sub>H</sub>)Application Reset Value: FEDC BA98<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				RESERVED				RESERVED			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
rw				rw				rw				rw			

Field	Bits	Type	Description
RESERVED (i=8-15)	4*i-29:4*i-32	rw	<b>Reserved</b> Read as reset value or last written value; should be written with 0.

##### Arbiter Priority Register Low

###### EBCU\_PRIOL

###### Arbiter Priority Register Low

(0018<sub>H</sub>)Application Reset Value: 7658 8210<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SFI_S2F				RESERVED				RESERVED			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOC32E				RESERVED				RESERVED				IOC32P			
rw				rw				rw				rw			

Field	Bits	Type	Description
IOC32P	3:0	rw	<b>IOC32P Priority (Index 0)</b> This bit field defines the priority on the BBB for IOC32P access to the BBB.
RESERVED	7:4, 11:8, 19:16, 23:20, 31:28	rw	<b>Reserved</b> Read as reset value or last written value; should be written with 0.
IOC32E	15:12	rw	<b>IOC32E Priority (Index 3)</b> This bit field defines the priority on the BBB for IOC32E access to the BBB.

Field	Bits	Type	Description
SFI_S2F	27:24	rw	<b>SFI Bridge SRI2FPI Priority (Index 6)</b> This bit field defines the priority on the BPB for SFI_S2F access to the BBB.

#### 4.7.3.2 EBCU OCDS Registers Descriptions

##### BCU Debug Control Register

EBCU\_DBCNTL

BCU Debug Control Register (0030<sub>H</sub>) Debug Reset Value: 0000 7003<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ONBO S3	ONBO S2	ONBO S1	ONBO S0	0	ONA2	0	ONA1	0						ONG	
rw	rw	rw	rw	r	rw	r	rw	r	rw	r	rw	r	r	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CONC OM2	CONC OM1	CONC OM0	0	0	0	0	0	0	RA	0	OA	EO		
r	rw	rw	rw	r	r	r	r	r	r	w	r	rh	r		

Field	Bits	Type	Description
EO	0	r	<b>Status of BCU Debug Support Enable</b> This bit is controlled by the Cerberus and enables the BCU debug support. 0 <sub>B</sub> BCU debug support is disabled 1 <sub>B</sub> BCU debug support is enabled (default after reset)
OA	1	rh	<b>Status of BCU Breakpoint Logic</b> The OA bit is set by writing a 1 to bit RA. When OA is set, registers DBGNTT, DBADRT and DBDAT are reset. Also DBBOST is reset with the exception of the bit field FPIIRST. 0 <sub>B</sub> The BCU breakpoint logic is disarmed. Any further breakpoint activation is discarded 1 <sub>B</sub> The BCU breakpoint logic is armed
RA	4	w	<b>Rearm BCU Breakpoint Logic</b> Writing a 1 to this bit rearms BCU breakpoint logic and sets bit OA = 1. RA is always reads as 0.
CONCOM0	12	rw	<b>Grant and Address Trigger Relation</b> 0 <sub>B</sub> The grant phase trigger condition and the address trigger condition (see CONCOM1) are combined with a logical OR for further control 1 <sub>B</sub> The grant phase trigger condition and the address trigger condition (see CONCOM1) are combined with a logical AND for further control.

Field	Bits	Type	Description
<b>CONCOM1</b>	13	rw	<p><b>Address 1 and Address 2 Trigger Relation</b></p> <p><b>0<sub>B</sub></b> Address 1 trigger condition and address 2 trigger condition are combined with a logical OR to the address trigger condition for further control</p> <p><b>1<sub>B</sub></b> Address 1 trigger condition and address 2 trigger condition are combined with a logical AND to the address trigger condition for further control</p>
<b>CONCOM2</b>	14	rw	<p><b>Address and Signal Trigger Relation</b></p> <p><b>0<sub>B</sub></b> Address trigger condition (see CONCOM1) and signal status trigger conditions are combined with a logical OR for further control</p> <p><b>1<sub>B</sub></b> Address phase trigger condition (see CONCOM1) and the signal status trigger conditions are combined with a logical AND for further control</p>
<b>ONG</b>	16	rw	<p><b>Grant Trigger Enable</b></p> <p><b>0<sub>B</sub></b> No grant debug event trigger is generated</p> <p><b>1<sub>B</sub></b> The grant debug event trigger is enabled and generated according the settings of register DBGRNT</p>
<b>ONA1</b>	21:20	rw	<p><b>Address 1 Trigger Control</b></p> <p><b>00<sub>B</sub></b> No address 1 trigger is generated</p> <p><b>01<sub>B</sub></b> An address 1 trigger event is generated if the FPI Bus address is equal to DBADR1</p> <p><b>10<sub>B</sub></b> An address 1 trigger event is generated if FPI Bus address is greater or equal to DBADR1</p> <p><b>11<sub>B</sub></b> same as 00<sub>B</sub></p>
<b>ONA2</b>	25:24	rw	<p><b>Address 2 Trigger Control</b></p> <p><b>00<sub>B</sub></b> No address 2 trigger is generated.</p> <p><b>01<sub>B</sub></b> An address 2 trigger event is generated if the FPI Bus address is equal to DBADR2</p> <p><b>10<sub>B</sub></b> An address 2 trigger event is generated if FPI Bus address is less or equal to DBADR2</p> <p><b>11<sub>B</sub></b> same as 00<sub>B</sub></p>
<b>ONBOS0</b>	28	rw	<p><b>Op code Signal Status Trigger Condition</b></p> <p><b>0<sub>B</sub></b> A signal status trigger is generated for all FPI Bus op-codes except a “no operation” op-code</p> <p><b>1<sub>B</sub></b> A signal status trigger is generated if the FPI Bus op-code matches the op-code as defined in DBBOS.OPC</p>
<b>ONBOS1</b>	29	rw	<p><b>Supervisor Mode Signal Trigger Condition</b></p> <p><b>0<sub>B</sub></b> The signal status trigger generation for the FPI Bus Supervisor Mode signal is disabled.</p> <p><b>1<sub>B</sub></b> A signal status trigger is generated if the FPI Bus Supervisor Mode signal state is equal to the value of DBBOS.SVM</p>

Field	Bits	Type	Description
<b>ONBOS2</b>	30	rw	<b>Write Signal Trigger Condition</b>  $0_B$ The signal status trigger generation for the FPI Bus write signal is disabled. $1_B$ A signal status trigger is generated if the FPI Bus write signal state is equal to the value of DBBOS.WR
<b>ONBOS3</b>	31	rw	<b>Read Signal Trigger Condition</b>  $0_B$ The signal status trigger generation for the FPI Bus read signal is disabled. $1_B$ A signal status trigger is generated if the FPI Bus read signal state is equal to the value of DBBOS.RD
<b>0</b>	3:2, 6:5, 7, 11:8, 15, 19:17, 23:22, 27:26	r	<b>Reserved</b> Read as 0; should be written with 0.

### EBCU Debug Grant Mask Register

#### EBCU\_DBGRNT

##### EBCU Debug Grant Mask Register

(0034<sub>H</sub>)

Debug Reset Value: 0000 FFFF<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>1</b>	<b>SFI_S2_F</b>	<b>1</b>	<b>1</b>	<b>IOC32_E</b>	<b>1</b>	<b>1</b>	<b>IOC32_P</b>								
rw	rw	rw	rw	rw	rw	rw									

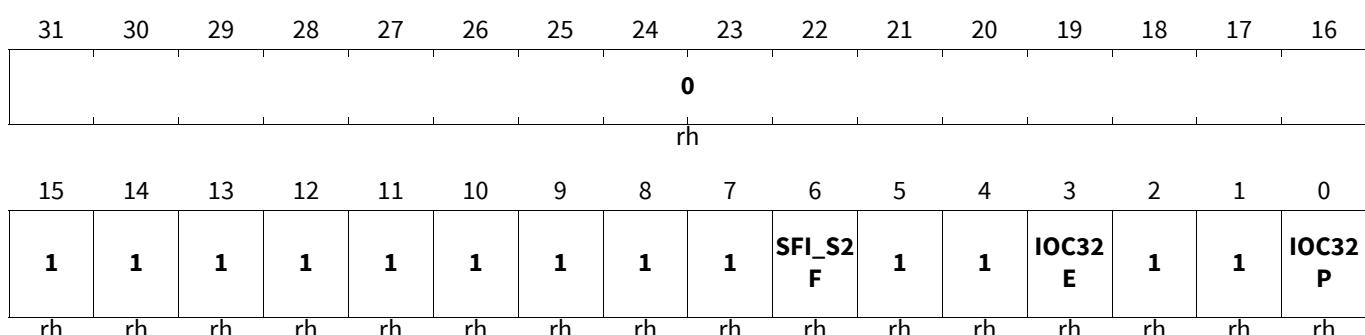
Field	Bits	Type	Description
<b>IOC32P</b>	0	rw	<b>IOC32P Trigger Enable</b>  $0_B$ FPI Bus transactions with IOC32P as bus master are enabled for grant trigger event generation $1_B$ FPI Bus transactions with IOC32P as bus master are disabled for grant trigger event generation

Field	Bits	Type	Description
<b>IOC32E</b>	3	rw	<b>IOC32E Grant Trigger Enable</b> $0_B$ FPI Bus transactions with IOC32E as bus master are enabled for grant trigger event generation $1_B$ FPI Bus transactions with IOC32E as bus master are disabled for grant trigger event generation
<b>SFI_S2F</b>	6	rw	<b>SFI_S2F Grant Trigger Enable</b> $0_B$ FPI Bus transactions with SFI_S2F as bus master are enabled for grant trigger event generation $1_B$ FPI Bus transactions with SFI_S2F as bus master are disabled for grant trigger event generation
<b>1</b>	1, 2, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15	rw	<b>Reserved</b> Read as 1 after reset; reading these bits will return the value last written.
<b>0</b>	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

### EBCU Debug Trapped Master Register

#### EBCU\_DBGNTT

#### EBCU Debug Trapped Master Register

(0044<sub>H</sub>)Debug Reset Value: 0000 FFFF<sub>H</sub>

Field	Bits	Type	Description
<b>IOC32P</b>	0	rh	<b>IOC32P FPI Bus Master Status</b> This bit indicates whether the IOC32P was FPI Bus master when the break trigger event occurred. $0_B$ The IOC32P was the FPI bus master. $1_B$ The IOC32P was not the FPI Bus master.

Field	Bits	Type	Description
<b>IOC32E</b>	3	rh	<b>IOC32E FPI Bus Master Status</b> This bit indicates whether the IOC32E was FPI Bus master when the break trigger event occurred. $0_B$ The IOC32E was the FPI bus master. $1_B$ The IOC32E was not the FPI Bus master.
<b>SFI_S2F</b>	6	rh	<b>SFI_S2F FPI Bus Master Status</b> This bit indicates whether the SFI_S2F with a medium priority request was FPI Bus master when the break trigger event occurred. $0_B$ The medium-priority SFI_S2F was the FPI bus master. $1_B$ The medium-priority SFI_S2F was not the FPI Bus master.
<b>1</b>	1, 2, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15	rh	<b>Reserved</b> Read as 1 after reset; reading these bits will return the value last written.
<b>0</b>	31:16	rh	<b>Reserved</b> Read as 1 after reset; reading these bits will return the value last written.

**EBCU\_ALSTATx (x=0)****BCU EDC Alarm Status Register x**(0060<sub>H</sub>+x\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>AL31</b>	<b>AL30</b>	<b>AL29</b>	<b>AL28</b>	<b>AL27</b>	<b>AL26</b>	<b>AL25</b>	<b>AL24</b>	<b>AL23</b>	<b>AL22</b>	<b>AL21</b>	<b>AL20</b>	<b>AL19</b>	<b>AL18</b>	<b>AL17</b>	<b>AL16</b>
rh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>AL15</b>	<b>AL14</b>	<b>AL13</b>	<b>AL12</b>	<b>AL11</b>	<b>AL10</b>	<b>AL09</b>	<b>AL08</b>	<b>AL07</b>	<b>AL06</b>	<b>AL05</b>	<b>AL04</b>	<b>AL03</b>	<b>AL02</b>	<b>AL01</b>	<b>AL00</b>
rh															

Field	Bits	Type	Description
<b>ALy (y=00)</b>	y	rh	<b>Alarm y</b> $1_B$ <b>EBCU_S</b> ,
<b>ALy (y=01)</b>	y	rh	<b>Alarm y</b> $1_B$ <b>MCDS_S</b> ,
<b>ALy (y=02)</b>	y	rh	<b>Alarm y</b> $1_B$ <b>AGBT_S</b> ,

Field	Bits	Type	Description
ALy (y=03-05,12-15,23-31)	y	rh	<b>Alarm y</b>
ALy (y=06)	y	rh	<b>Alarm y</b> 1_B EMEM_XTMRAM_S,
ALy (y=07)	y	rh	<b>Alarm y</b> 1_B EMEM_CTRL_S,
ALy (y=08)	y	rh	<b>Alarm y</b> 1_B EMEM0_S,
ALy (y=09)	y	rh	<b>Alarm y</b> 1_B EMEM1_S,
ALy (y=10)	y	rh	<b>Alarm y</b> 1_B EMEM2_S,
ALy (y=11)	y	rh	<b>Alarm y</b> 1_B EMEM3_S,
ALy (y=16)	y	rh	<b>Alarm y</b> 1_B RIFO_S,
ALy (y=17)	y	rh	<b>Alarm y</b> 1_B RIF1_S,
ALy (y=18)	y	rh	<b>Alarm y</b> 1_B SPU0_S,
ALy (y=19)	y	rh	<b>Alarm y</b> 1_B SPU_CFG0_S,
ALy (y=20)	y	rh	<b>Alarm y</b> 1_B SPU1_S,
ALy (y=21)	y	rh	<b>Alarm y</b> 1_B SPU_CFG1_S,
ALy (y=22)	y	rh	<b>Alarm y</b> 1_B SPU_LS_SFR_S,

**EBCU\_ALSTATx (x=1)**

BCU EDC Alarm Status Register x

(0060<sub>H</sub>+x\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	AL30	AL29	AL28	AL27	AL26	AL25	AL24	AL23	AL22	AL21	AL20	AL19	AL18	AL17	AL16
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	AL14	AL13	AL12	AL11	AL10	AL09	AL08	AL07	AL06	AL05	AL04	AL03	AL02	AL01	AL00
rh															

Field	Bits	Type	Description
ALy (y=00-31)	y	rh	<b>Alarm y</b>

**EBCU\_ALSTATx (x=2)****BCU EDC Alarm Status Register x**(0060<sub>H</sub>+x\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>AL31</b>	<b>AL30</b>	<b>AL29</b>	<b>AL28</b>	<b>AL27</b>	<b>AL26</b>	<b>AL25</b>	<b>AL24</b>	<b>AL23</b>	<b>AL22</b>	<b>AL21</b>	<b>AL20</b>	<b>AL19</b>	<b>AL18</b>	<b>AL17</b>	<b>AL16</b>
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>AL15</b>	<b>AL14</b>	<b>AL13</b>	<b>AL12</b>	<b>AL11</b>	<b>AL10</b>	<b>AL09</b>	<b>AL08</b>	<b>AL07</b>	<b>AL06</b>	<b>AL05</b>	<b>AL04</b>	<b>AL03</b>	<b>AL02</b>	<b>AL01</b>	<b>AL00</b>
rh															

Field	Bits	Type	Description
<b>ALy (y=00-30)</b>	y	rh	<b>Alarm y</b>
<b>ALy (y=31)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>EBCU_M</b> , an EDC error was detected in an active phase of the EBCU Master Interface.

**EBCU\_ALSTATx (x=3)****BCU EDC Alarm Status Register x**(0060<sub>H</sub>+x\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>AL31</b>	<b>AL30</b>	<b>AL29</b>	<b>AL28</b>	<b>AL27</b>	<b>AL26</b>	<b>AL25</b>	<b>AL24</b>	<b>AL23</b>	<b>AL22</b>	<b>AL21</b>	<b>AL20</b>	<b>AL19</b>	<b>AL18</b>	<b>AL17</b>	<b>AL16</b>
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>AL15</b>	<b>AL14</b>	<b>AL13</b>	<b>AL12</b>	<b>AL11</b>	<b>AL10</b>	<b>AL09</b>	<b>AL08</b>	<b>AL07</b>	<b>AL06</b>	<b>AL05</b>	<b>AL04</b>	<b>AL03</b>	<b>AL02</b>	<b>AL01</b>	<b>AL00</b>
rh															

Field	Bits	Type	Description
<b>ALy (y=00)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>A_EN</b> , multiple output enables active: A_EN_N (Master)
<b>ALy (y=01)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ABORT_EN</b> , multiple output enables active: ABORT_EN_N (Master)
<b>ALy (y=02)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>ACK_EN</b> , multiple output enables active: ACK_EN_N (Default Master and Slave)
<b>ALy (y=03)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>D_EN</b> , multiple output enables active: D_EN_N (Master and Slave)
<b>ALy (y=04-15,17-18,20-31)</b>	y	rh	<b>Alarm y</b>
<b>ALy (y=16)</b>	y	rh	<b>Alarm y</b> 1 <sub>B</sub> <b>IOC32P_M</b> ,

Field	Bits	Type	Description
ALy (y=19)	y	rh	Alarm y 1_B IOC32E_M,

## 4.7.4 Connectivity

### 4.7.4.1 SBCU Connectivity

Table 17 Connections of SBCU

Interface Signals	connects		Description
SBCU:INT	to	INT:sbcu_INT	Bus Control Unit SPB Service Request

### 4.7.4.2 EBCU Connectivity

Table 18 Connections of EBCU

Interface Signals	connects		Description
EBCU:INT	to	INT:bbbcu_INT	Bus Control Unit BBB Service Request

## 4.7.5 Revision History

Table 19 Revision History

Reference	Change to Previous Version	Comment
V1.2.7	No functional change.	
V1.2.8	No functional changes.	-
V1.2.9		
Page 30, Page 34, Page 35	Wrongly mentioned CIF removed	

**CPU Subsystem (CPU)****5 CPU Subsystem (CPU)**

This chapter describes the CPU subsystem module of the TC39x-B.

**5.1 TC39x-B Specific Configuration**

No product specific configuration for CPU

**5.2 TC39x-B Specific Register Set****Register Address Space Table****Table 20 Register Address Space - CPU**

<b>Module</b>	<b>Base Address</b>	<b>End Address</b>	<b>Note</b>
(CPU0)	70000000 <sub>H</sub>	7003BFFF <sub>H</sub>	Data ScratchPad RAM interface
	7003C000 <sub>H</sub>	7003FFFF <sub>H</sub>	Data Cache RAM interface
	700C0000 <sub>H</sub>	700C17FF <sub>H</sub>	Data Cache Tag RAM interface
	70100000 <sub>H</sub>	7010FFFF <sub>H</sub>	Program ScratchPad RAM interface
	70110000 <sub>H</sub>	70117FFF <sub>H</sub>	Program Cache RAM interface
	701C0000 <sub>H</sub>	701C2FFF <sub>H</sub>	Program Cache TAG RAM interface
	90000000 <sub>H</sub>	9000FFFF <sub>H</sub>	DLMU RAM interface (cached)
	B0000000 <sub>H</sub>	B000FFFF <sub>H</sub>	DLMU RAM interface (non-cached)
CPU0	F8800000 <sub>H</sub>	F881FFFF <sub>H</sub>	SRI slave interface for SFR+CSFR
(CPU1)	60000000 <sub>H</sub>	6003BFFF <sub>H</sub>	Data ScratchPad RAM interface
	6003C000 <sub>H</sub>	6003FFFF <sub>H</sub>	Data Cache RAM interface
	600C0000 <sub>H</sub>	600C17FF <sub>H</sub>	Data Cache Tag RAM interface
	60100000 <sub>H</sub>	6010FFFF <sub>H</sub>	Program ScratchPad RAM interface
	60110000 <sub>H</sub>	60117FFF <sub>H</sub>	Program Cache RAM interface
	601C0000 <sub>H</sub>	601C2FFF <sub>H</sub>	Program Cache TAG RAM interface
	90010000 <sub>H</sub>	9001FFFF <sub>H</sub>	DLMU RAM interface (cached)
	B0010000 <sub>H</sub>	B001FFFF <sub>H</sub>	DLMU RAM interface (non-cached)
CPU1	F8820000 <sub>H</sub>	F883FFFF <sub>H</sub>	SRI slave interface for SFR+CSFR
(CPU2)	50000000 <sub>H</sub>	50017FFF <sub>H</sub>	Data ScratchPad RAM interface
	50018000 <sub>H</sub>	5001BFFF <sub>H</sub>	Data Cache RAM interface
	500C0000 <sub>H</sub>	500C17FF <sub>H</sub>	Data Cache Tag RAM interface
	50100000 <sub>H</sub>	5010FFFF <sub>H</sub>	Program ScratchPad RAM interface
	50110000 <sub>H</sub>	50117FFF <sub>H</sub>	Program Cache RAM interface
	501C0000 <sub>H</sub>	501C2FFF <sub>H</sub>	Program Cache TAG RAM interface
	90020000 <sub>H</sub>	9002FFFF <sub>H</sub>	DLMU RAM interface (cached)
	B0020000 <sub>H</sub>	B002FFFF <sub>H</sub>	DLMU RAM interface (non-cached)
CPU2	F8840000 <sub>H</sub>	F885FFFF <sub>H</sub>	SRI slave interface for SFR+CSFR

**CPU Subsystem (CPU)****Table 20 Register Address Space - CPU (cont'd)**

<b>Module</b>	<b>Base Address</b>	<b>End Address</b>	<b>Note</b>
(CPU3)	40000000 <sub>H</sub>	40017FFF <sub>H</sub>	Data ScratchPad RAM interface
	40018000 <sub>H</sub>	4001BFFF <sub>H</sub>	Data Cache RAM interface
	400C0000 <sub>H</sub>	400C17FF <sub>H</sub>	Data Cache Tag RAM interface
	40100000 <sub>H</sub>	4010FFFF <sub>H</sub>	Program ScratchPad RAM interface
	40110000 <sub>H</sub>	40117FFF <sub>H</sub>	Program Cache RAM interface
	401C0000 <sub>H</sub>	401C2FFF <sub>H</sub>	Program Cache TAG RAM interface
	90030000 <sub>H</sub>	9003FFFF <sub>H</sub>	DLMU RAM interface (cached)
	B0030000 <sub>H</sub>	B003FFFF <sub>H</sub>	DLMU RAM interface (non-cached)
CPU3	F8860000 <sub>H</sub>	F887FFFF <sub>H</sub>	SRI slave interface for SFR+CSFR
(CPU4)	30000000 <sub>H</sub>	30017FFF <sub>H</sub>	Data ScratchPad RAM interface
	30018000 <sub>H</sub>	3001BFFF <sub>H</sub>	Data Cache RAM interface
	300C0000 <sub>H</sub>	300C17FF <sub>H</sub>	Data Cache Tag RAM interface
	30100000 <sub>H</sub>	3010FFFF <sub>H</sub>	Program ScratchPad RAM interface
	30110000 <sub>H</sub>	30117FFF <sub>H</sub>	Program Cache RAM interface
	301C0000 <sub>H</sub>	301C2FFF <sub>H</sub>	Program Cache TAG RAM interface
	90100000 <sub>H</sub>	9010FFFF <sub>H</sub>	DLMU RAM interface (cached)
	B0100000 <sub>H</sub>	B010FFFF <sub>H</sub>	DLMU RAM interface (non-cached)
CPU4	F8880000 <sub>H</sub>	F889FFFF <sub>H</sub>	SRI slave interface for SFR+CSFR
(CPU5)	10000000 <sub>H</sub>	10017FFF <sub>H</sub>	Data ScratchPad RAM interface
	10018000 <sub>H</sub>	1001BFFF <sub>H</sub>	Data Cache RAM interface
	100C0000 <sub>H</sub>	100C17FF <sub>H</sub>	Data Cache Tag RAM interface
	10100000 <sub>H</sub>	1010FFFF <sub>H</sub>	Program ScratchPad RAM interface
	10110000 <sub>H</sub>	10117FFF <sub>H</sub>	Program Cache RAM interface
	101C0000 <sub>H</sub>	101C2FFF <sub>H</sub>	Program Cache TAG RAM interface
	90110000 <sub>H</sub>	9011FFFF <sub>H</sub>	DLMU RAM interface (cached)
	B0110000 <sub>H</sub>	B011FFFF <sub>H</sub>	DLMU RAM interface (non-cached)
CPU5	F88C0000 <sub>H</sub>	F88DFFFF <sub>H</sub>	SRI slave interface for SFR+CSFR

**Register Overview Table****Register Overview Tables of CPU****Table 21 Register Overview - CPU0 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_FLASHCON0	CPUx Flash Configuration Register 0	01100 <sub>H</sub>	48
CPU0_FLASHCON1	CPUx Flash Configuration Register 1	01104 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_FLASHCON2	CPUx Flash Configuration Register 2	01108 <sub>H</sub>	See Family Spec
CPU0_FLASHCON3	CPUx Flash Configuration Register 3	0110C <sub>H</sub>	See Family Spec
CPU0_FLASHCON4	CPUx Flash Configuration Register 4	01110 <sub>H</sub>	See Family Spec
CPU0_KRST0	CPUx Reset Register 0	0D000 <sub>H</sub>	See Family Spec
CPU0_KRST1	CPUx Reset Register 1	0D004 <sub>H</sub>	See Family Spec
CPU0_KRSTCLR	CPUx Reset Clear Register	0D008 <sub>H</sub>	See Family Spec
CPU0_SPR_SPROT_R GNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_SPR_SPROT_R GNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_SPR_SPROT_R GNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_SPR_SPROT_R GNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_SPR_SPROT_R GNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_SPR_SPROT_R GNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_SFR_SPROT_A CCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 <sub>H</sub>	See Family Spec
CPU0_SFR_SPROT_A CCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_LPБ_SPROT_A CCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 <sub>H</sub>	See Family Spec
CPU0_LPБ_SPROT_A CCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 <sub>H</sub>	See Family Spec
CPU0_DLMU_SPROT _RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_DLMU_SPROT _RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_DLMU_SPROT _RGNACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_DLMU_SPROT _RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_DLMU_SPROT _RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_DLMU_SPROT _RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU0_OSEL	CPUx Overlay Range Select Register	0FB00 <sub>H</sub>	See Family Spec
CPU0_RABRI (i=0-31)	CPUx Redirected Address Base Register i	0FB10 <sub>H</sub> +i*12	See Family Spec
CPU0_OTARI (i=0-31)	CPUx Overlay Target Address Register i	0FB14 <sub>H</sub> +i*12	See Family Spec
CPU0_OMASKi (i=0-31)	CPUx Overlay Mask Register i	0FB18 <sub>H</sub> +i*12	See Family Spec
CPU0_SEGEN	CPUx SRI Error Generation Register	11030 <sub>H</sub>	See Family Spec
CPU0_TASK_ASİ	CPUx Task Address Space Identifier Register	18004 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_PMA0	CPUx Data Access CacheabilityRegister	18100 <sub>H</sub>	See Family Spec
CPU0_PMA1	CPUx Code Access CacheabilityRegister	18104 <sub>H</sub>	See Family Spec
CPU0_PMA2	CPUx Peripheral Space Identifier register	18108 <sub>H</sub>	See Family Spec
CPU0_DCON2	CPUx Data Control Register 2	19000 <sub>H</sub>	See Family Spec
CPU0_SMACON	CPUx SIST Mode Access Control Register	1900C <sub>H</sub>	See Family Spec
CPU0_DSTR	CPUx Data Synchronous Trap Register	19010 <sub>H</sub>	See Family Spec
CPU0_DATR	CPUx Data Asynchronous Trap Register	19018 <sub>H</sub>	See Family Spec
CPU0_DEADD	CPUx Data Error Address Register	1901C <sub>H</sub>	See Family Spec
CPU0_DIEAR	CPUx Data Integrity Error Address Register	19020 <sub>H</sub>	See Family Spec
CPU0_DIETR	CPUx Data Integrity Error Trap Register	19024 <sub>H</sub>	See Family Spec
CPU0_DCON0	CPUx Data Memory Control Register	19040 <sub>H</sub>	See Family Spec
CPU0_PSTR	CPUx Program Synchronous Trap Register	19200 <sub>H</sub>	See Family Spec
CPU0_PCON1	CPUx Program Control 1	19204 <sub>H</sub>	See Family Spec
CPU0_PCON2	CPUx Program Control 2	19208 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_PCON0	CPUx Program Control 0	1920C <sub>H</sub>	See Family Spec
CPU0_PIEAR	CPUx Program Integrity Error Address Register	19210 <sub>H</sub>	See Family Spec
CPU0_PIETR	CPUx Program Integrity Error Trap Register	19214 <sub>H</sub>	See Family Spec
CPU0_COMPAT	CPUx Compatibility Control Register	19400 <sub>H</sub>	See Family Spec
CPU0_FPU_TRAP_CO_N	CPUx Trap Control Register	1A000 <sub>H</sub>	See Family Spec
CPU0_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 <sub>H</sub>	See Family Spec
CPU0_FPU_TRAP_OP_C	CPUx Trapping Instruction Opcode Register	1A008 <sub>H</sub>	See Family Spec
CPU0_FPU_TRAP_SR_C1	CPUx Trapping Instruction Operand Register	1A010 <sub>H</sub>	See Family Spec
CPU0_FPU_TRAP_SR_C2	CPUx Trapping Instruction Operand Register	1A014 <sub>H</sub>	See Family Spec
CPU0_FPU_TRAP_SR_C3	CPUx Trapping Instruction Operand Register	1A018 <sub>H</sub>	See Family Spec
CPU0_DPRy_L (y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 <sub>H</sub> +y*8	See Family Spec
CPU0_DPRy_U (y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 <sub>H</sub> +y*8	See Family Spec
CPU0_CPRy_L (y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 <sub>H</sub> +y*8	See Family Spec
CPU0_CPRy_U (y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 <sub>H</sub> +y*8	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_CPxExE_y (y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 <sub>H</sub> +y*4	See Family Spec
CPU0_DPxRE_y (y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 <sub>H</sub> +y*4	See Family Spec
CPU0_DPxWE_y (y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 <sub>H</sub> +y*4	See Family Spec
CPU0_CPxExE_y (y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 <sub>H</sub> +(y-4)*4	See Family Spec
CPU0_DPxRE_y (y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 <sub>H</sub> +(y-4)*4	See Family Spec
CPU0_DPxWE_y (y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 <sub>H</sub> +(y-4)*4	See Family Spec
CPU0_TPS_CON	CPUx Temporal Protection System Control Register	1E400 <sub>H</sub>	See Family Spec
CPU0_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 <sub>H</sub> +y*4	See Family Spec
CPU0_TPS_EXTIM_E_NTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 <sub>H</sub>	See Family Spec
CPU0_TPS_EXTIM_E_NTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 <sub>H</sub>	See Family Spec
CPU0_TPS_EXTIM_E_XIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 <sub>H</sub>	See Family Spec
CPU0_TPS_EXTIM_E_XIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C <sub>H</sub>	See Family Spec
CPU0_TPS_EXTIM_C_LASS_EN	CPUx Exception Timer Class Enable Register	1E450 <sub>H</sub>	See Family Spec
CPU0_TPS_EXTIM_S_TAT	CPUx Exception Timer Status Register	1E454 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_TPS_EXTIM_FCX	CPUx Exception Timer FCX Register	1E458 <sub>H</sub>	See Family Spec
CPU0_TRIEVT (i=0-7)	CPUx Trigger Event i	1F000 <sub>H</sub> +i*8	See Family Spec
CPU0_TRIADR (i=0-7)	CPUx Trigger Address i	1F004 <sub>H</sub> +i*8	See Family Spec
CPU0_CCTRL	CPUx Counter Control	1FC00 <sub>H</sub>	See Family Spec
CPU0_CCNT	CPUx CPU Clock Cycle Count	1FC04 <sub>H</sub>	See Family Spec
CPU0_ICNT	CPUx Instruction Count	1FC08 <sub>H</sub>	See Family Spec
CPU0_M1CNT	CPUx Multi-Count Register 1	1FC0C <sub>H</sub>	See Family Spec
CPU0_M2CNT	CPUx Multi-Count Register 2	1FC10 <sub>H</sub>	See Family Spec
CPU0_M3CNT	CPUx Multi-Count Register 3	1FC14 <sub>H</sub>	See Family Spec
CPU0_DBGSR	CPUx Debug Status Register	1FD00 <sub>H</sub>	See Family Spec
CPU0_EXEVT	CPUx External Event Register	1FD08 <sub>H</sub>	See Family Spec
CPU0_CREVT	CPUx Core Register Access Event	1FD0C <sub>H</sub>	See Family Spec
CPU0_SWEVT	CPUx Software Debug Event	1FD10 <sub>H</sub>	See Family Spec
CPU0_TRIG_ACC	CPUx TriggerAddressx	1FD30 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_DMS	CPUx Debug Monitor Start Address	1FD40 <sub>H</sub>	See Family Spec
CPU0_DCX	CPUx Debug Context Save Area Pointer	1FD44 <sub>H</sub>	See Family Spec
CPU0_DBGTCR	CPUx Debug Trap Control Register	1FD48 <sub>H</sub>	See Family Spec
CPU0_PCXI	CPUx Previous Context Information Register	1FE00 <sub>H</sub>	See Family Spec
CPU0_PSW	CPUx Program Status Word	1FE04 <sub>H</sub>	See Family Spec
CPU0_PC	CPUx Program Counter	1FE08 <sub>H</sub>	See Family Spec
CPU0_SYSCON	CPUx System Configuration Register	1FE14 <sub>H</sub>	See Family Spec
CPU0_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 <sub>H</sub>	See Family Spec
CPU0_CORE_ID	CPUx Core Identification Register	1FE1C <sub>H</sub>	See Family Spec
CPU0_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 <sub>H</sub>	See Family Spec
CPU0_BTV	CPUx Base Trap Vector Table Pointer	1FE24 <sub>H</sub>	See Family Spec
CPU0_ISP	CPUx Interrupt Stack Pointer	1FE28 <sub>H</sub>	See Family Spec
CPU0_ICR	CPUx Interrupt Control Register	1FE2C <sub>H</sub>	See Family Spec
CPU0_FCX	CPUx Free CSA List Head Pointer	1FE38 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 21 Register Overview - CPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU0_LCX	CPUx Free CSA List Limit Pointer	1FE3C <sub>H</sub>	See Family Spec
CPU0_CUS_ID	CPUx Customer ID register	1FE50 <sub>H</sub>	See Family Spec
CPU0_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 <sub>H</sub> +y*4	See Family Spec
CPU0_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 <sub>H</sub> +y*4	See Family Spec

**Table 22 Register Overview - CPU1 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_FLASHCON0	CPUx Flash Configuration Register 0	01100 <sub>H</sub>	<b>48</b>
CPU1_FLASHCON1	CPUx Flash Configuration Register 1	01104 <sub>H</sub>	See Family Spec
CPU1_FLASHCON2	CPUx Flash Configuration Register 2	01108 <sub>H</sub>	See Family Spec
CPU1_FLASHCON3	CPUx Flash Configuration Register 3	0110C <sub>H</sub>	See Family Spec
CPU1_FLASHCON4	CPUx Flash Configuration Register 4	01110 <sub>H</sub>	See Family Spec
CPU1_KRST0	CPUx Reset Register 0	0D000 <sub>H</sub>	See Family Spec
CPU1_KRST1	CPUx Reset Register 1	0D004 <sub>H</sub>	See Family Spec
CPU1_KRSTCLR	CPUx Reset Clear Register	0D008 <sub>H</sub>	See Family Spec
CPU1_SPR_SPROT_R GNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 22 Register Overview - CPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_SPR_SPROT_R GNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_SPR_SPROT_R GNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_SPR_SPROT_R GNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_SPR_SPROT_R GNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_SPR_SPROT_R GNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_SFR_SPROT_A CCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 <sub>H</sub>	See Family Spec
CPU1_SFR_SPROT_A CCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 <sub>H</sub>	See Family Spec
CPU1_LPB_SPROT_A CCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 <sub>H</sub>	See Family Spec
CPU1_LPB_SPROT_A CCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 <sub>H</sub>	See Family Spec
CPU1_DLMU_SPROT _RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_DLMU_SPROT _RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_DLMU_SPROT _RGNACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_DLMU_SPROT _RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_DLMU_SPROT _RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 22 Register Overview - CPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_DLMU_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU1_OSEL	CPUx Overlay Range Select Register	0FB00 <sub>H</sub>	See Family Spec
CPU1_RABRi (i=0-31)	CPUx Redirected Address Base Register i	0FB10 <sub>H</sub> +i*12	See Family Spec
CPU1_OTARI (i=0-31)	CPUx Overlay Target Address Register i	0FB14 <sub>H</sub> +i*12	See Family Spec
CPU1_OMASKi (i=0-31)	CPUx Overlay Mask Register i	0FB18 <sub>H</sub> +i*12	See Family Spec
CPU1_SEGEN	CPUx SRI Error Generation Register	11030 <sub>H</sub>	See Family Spec
CPU1_TASK_ASI	CPUx Task Address Space Identifier Register	18004 <sub>H</sub>	See Family Spec
CPU1_PMA0	CPUx Data Access CacheabilityRegister	18100 <sub>H</sub>	See Family Spec
CPU1_PMA1	CPUx Code Access CacheabilityRegister	18104 <sub>H</sub>	See Family Spec
CPU1_PMA2	CPUx Peripheral Space Identifier register	18108 <sub>H</sub>	See Family Spec
CPU1_DCON2	CPUx Data Control Register 2	19000 <sub>H</sub>	See Family Spec
CPU1_SMACON	CPUx SIST Mode Access Control Register	1900C <sub>H</sub>	See Family Spec
CPU1_DSTR	CPUx Data Synchronous Trap Register	19010 <sub>H</sub>	See Family Spec
CPU1_DATR	CPUx Data Asynchronous Trap Register	19018 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 22 Register Overview - CPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_DEADD	CPUx Data Error Address Register	1901C <sub>H</sub>	See Family Spec
CPU1_DIEAR	CPUx Data Integrity Error Address Register	19020 <sub>H</sub>	See Family Spec
CPU1_DIETR	CPUx Data Integrity Error Trap Register	19024 <sub>H</sub>	See Family Spec
CPU1_DCON0	CPUx Data Memory Control Register	19040 <sub>H</sub>	See Family Spec
CPU1_PSTR	CPUx Program Synchronous Trap Register	19200 <sub>H</sub>	See Family Spec
CPU1_PCON1	CPUx Program Control 1	19204 <sub>H</sub>	See Family Spec
CPU1_PCON2	CPUx Program Control 2	19208 <sub>H</sub>	See Family Spec
CPU1_PCON0	CPUx Program Control 0	1920C <sub>H</sub>	See Family Spec
CPU1_PIEAR	CPUx Program Integrity Error Address Register	19210 <sub>H</sub>	See Family Spec
CPU1_PIETR	CPUx Program Integrity Error Trap Register	19214 <sub>H</sub>	See Family Spec
CPU1_COMPAT	CPUx Compatibility Control Register	19400 <sub>H</sub>	See Family Spec
CPU1_FPU_TRAP_CO_N	CPUx Trap Control Register	1A000 <sub>H</sub>	See Family Spec
CPU1_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 <sub>H</sub>	See Family Spec
CPU1_FPU_TRAP_OP_C	CPUx Trapping Instruction Opcode Register	1A008 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 22 Register Overview - CPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_FPU_TRAP_SR_C1	CPUx Trapping Instruction Operand Register	1A010 <sub>H</sub>	See Family Spec
CPU1_FPU_TRAP_SR_C2	CPUx Trapping Instruction Operand Register	1A014 <sub>H</sub>	See Family Spec
CPU1_FPU_TRAP_SR_C3	CPUx Trapping Instruction Operand Register	1A018 <sub>H</sub>	See Family Spec
CPU1_DPRy_L(y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 <sub>H</sub> +y*8	See Family Spec
CPU1_DPRy_U(y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 <sub>H</sub> +y*8	See Family Spec
CPU1_CPRy_L(y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 <sub>H</sub> +y*8	See Family Spec
CPU1_CPRy_U(y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 <sub>H</sub> +y*8	See Family Spec
CPU1_CPXE_y(y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 <sub>H</sub> +y*4	See Family Spec
CPU1_DPREG_y(y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 <sub>H</sub> +y*4	See Family Spec
CPU1_DPWE_y(y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 <sub>H</sub> +y*4	See Family Spec
CPU1_CPXE_y(y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 <sub>H</sub> +(y-4)*4	See Family Spec
CPU1_DPREG_y(y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 <sub>H</sub> +(y-4)*4	See Family Spec
CPU1_DPWE_y(y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 <sub>H</sub> +(y-4)*4	See Family Spec
CPU1_TPS_CON	CPUx Temporal Protection System Control Register	1E400 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 22 Register Overview - CPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 <sub>H</sub> +y*4	See Family Spec
CPU1_TPS_EXTIM_E_NTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 <sub>H</sub>	See Family Spec
CPU1_TPS_EXTIM_E_NTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 <sub>H</sub>	See Family Spec
CPU1_TPS_EXTIM_E_XIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 <sub>H</sub>	See Family Spec
CPU1_TPS_EXTIM_E_XIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C <sub>H</sub>	See Family Spec
CPU1_TPS_EXTIM_C_LASS_EN	CPUx Exception Timer Class Enable Register	1E450 <sub>H</sub>	See Family Spec
CPU1_TPS_EXTIM_S_TAT	CPUx Exception Timer Status Register	1E454 <sub>H</sub>	See Family Spec
CPU1_TPS_EXTIM_F_CX	CPUx Exception Timer FCX Register	1E458 <sub>H</sub>	See Family Spec
CPU1_TRIEVT (i=0-7)	CPUx Trigger Event i	1F000 <sub>H</sub> +i*8	See Family Spec
CPU1_TRIADR (i=0-7)	CPUx Trigger Address i	1F004 <sub>H</sub> +i*8	See Family Spec
CPU1_CCTRL	CPUx Counter Control	1FC00 <sub>H</sub>	See Family Spec
CPU1_CCNT	CPUx CPU Clock Cycle Count	1FC04 <sub>H</sub>	See Family Spec
CPU1_ICNT	CPUx Instruction Count	1FC08 <sub>H</sub>	See Family Spec
CPU1_M1CNT	CPUx Multi-Count Register 1	1FC0C <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 22 Register Overview - CPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_M2CNT	CPUx Multi-Count Register 2	1FC10 <sub>H</sub>	See Family Spec
CPU1_M3CNT	CPUx Multi-Count Register 3	1FC14 <sub>H</sub>	See Family Spec
CPU1_DBGSR	CPUx Debug Status Register	1FD00 <sub>H</sub>	See Family Spec
CPU1_EXEVT	CPUx External Event Register	1FD08 <sub>H</sub>	See Family Spec
CPU1_CREVT	CPUx Core Register Access Event	1FD0C <sub>H</sub>	See Family Spec
CPU1_SWEVT	CPUx Software Debug Event	1FD10 <sub>H</sub>	See Family Spec
CPU1_TRIG_ACC	CPUx TriggerAddressx	1FD30 <sub>H</sub>	See Family Spec
CPU1_DMS	CPUx Debug Monitor Start Address	1FD40 <sub>H</sub>	See Family Spec
CPU1_DCX	CPUx Debug Context Save Area Pointer	1FD44 <sub>H</sub>	See Family Spec
CPU1_DBGTCR	CPUx Debug Trap Control Register	1FD48 <sub>H</sub>	See Family Spec
CPU1_PCXI	CPUx Previous Context Information Register	1FE00 <sub>H</sub>	See Family Spec
CPU1_PSW	CPUx Program Status Word	1FE04 <sub>H</sub>	See Family Spec
CPU1_PC	CPUx Program Counter	1FE08 <sub>H</sub>	See Family Spec
CPU1_SYSCON	CPUx System Configuration Register	1FE14 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 22 Register Overview - CPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU1_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 <sub>H</sub>	See Family Spec
CPU1_CORE_ID	CPUx Core Identification Register	1FE1C <sub>H</sub>	See Family Spec
CPU1_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 <sub>H</sub>	See Family Spec
CPU1_BTV	CPUx Base Trap Vector Table Pointer	1FE24 <sub>H</sub>	See Family Spec
CPU1_ISP	CPUx Interrupt Stack Pointer	1FE28 <sub>H</sub>	See Family Spec
CPU1_ICR	CPUx Interrupt Control Register	1FE2C <sub>H</sub>	See Family Spec
CPU1_FCX	CPUx Free CSA List Head Pointer	1FE38 <sub>H</sub>	See Family Spec
CPU1_LCX	CPUx Free CSA List Limit Pointer	1FE3C <sub>H</sub>	See Family Spec
CPU1_CUS_ID	CPUx Customer ID register	1FE50 <sub>H</sub>	See Family Spec
CPU1_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 <sub>H</sub> +y*4	See Family Spec
CPU1_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 <sub>H</sub> +y*4	See Family Spec

**Table 23 Register Overview - CPU2 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_FLASHCON0	CPUx Flash Configuration Register 0	01100 <sub>H</sub>	<b>48</b>
CPU2_FLASHCON1	CPUx Flash Configuration Register 1	01104 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_FLASHCON2	CPUx Flash Configuration Register 2	01108 <sub>H</sub>	See Family Spec
CPU2_FLASHCON3	CPUx Flash Configuration Register 3	0110C <sub>H</sub>	See Family Spec
CPU2_FLASHCON4	CPUx Flash Configuration Register 4	01110 <sub>H</sub>	See Family Spec
CPU2_KRST0	CPUx Reset Register 0	0D000 <sub>H</sub>	See Family Spec
CPU2_KRST1	CPUx Reset Register 1	0D004 <sub>H</sub>	See Family Spec
CPU2_KRSTCLR	CPUx Reset Clear Register	0D008 <sub>H</sub>	See Family Spec
CPU2_SPR_SPROT_R GNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_SPR_SPROT_R GNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_SPR_SPROT_R GNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_SPR_SPROT_R GNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_SPR_SPROT_R GNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_SPR_SPROT_R GNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_SFR_SPROT_A CCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 <sub>H</sub>	See Family Spec
CPU2_SFR_SPROT_A CCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_LPБ_SPROT_A CCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 <sub>H</sub>	See Family Spec
CPU2_LPБ_SPROT_A CCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 <sub>H</sub>	See Family Spec
CPU2_DLMU_SPROT _RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_DLMU_SPROT _RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_DLMU_SPROT _RGNACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_DLMU_SPROT _RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_DLMU_SPROT _RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_DLMU_SPROT _RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU2_OSEL	CPUx Overlay Range Select Register	0FB00 <sub>H</sub>	See Family Spec
CPU2_RABRI (i=0-31)	CPUx Redirected Address Base Register i	0FB10 <sub>H</sub> +i*12	See Family Spec
CPU2_OTARI (i=0-31)	CPUx Overlay Target Address Register i	0FB14 <sub>H</sub> +i*12	See Family Spec
CPU2_OMASKi (i=0-31)	CPUx Overlay Mask Register i	0FB18 <sub>H</sub> +i*12	See Family Spec
CPU2_SEGEN	CPUx SRI Error Generation Register	11030 <sub>H</sub>	See Family Spec
CPU2_TASK_ASİ	CPUx Task Address Space Identifier Register	18004 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_PMA0	CPUx Data Access CacheabilityRegister	18100 <sub>H</sub>	See Family Spec
CPU2_PMA1	CPUx Code Access CacheabilityRegister	18104 <sub>H</sub>	See Family Spec
CPU2_PMA2	CPUx Peripheral Space Identifier register	18108 <sub>H</sub>	See Family Spec
CPU2_DCON2	CPUx Data Control Register 2	19000 <sub>H</sub>	See Family Spec
CPU2_SMACON	CPUx SIST Mode Access Control Register	1900C <sub>H</sub>	See Family Spec
CPU2_DSTR	CPUx Data Synchronous Trap Register	19010 <sub>H</sub>	See Family Spec
CPU2_DATR	CPUx Data Asynchronous Trap Register	19018 <sub>H</sub>	See Family Spec
CPU2_DEADD	CPUx Data Error Address Register	1901C <sub>H</sub>	See Family Spec
CPU2_DIEAR	CPUx Data Integrity Error Address Register	19020 <sub>H</sub>	See Family Spec
CPU2_DIETR	CPUx Data Integrity Error Trap Register	19024 <sub>H</sub>	See Family Spec
CPU2_DCON0	CPUx Data Memory Control Register	19040 <sub>H</sub>	See Family Spec
CPU2_PSTR	CPUx Program Synchronous Trap Register	19200 <sub>H</sub>	See Family Spec
CPU2_PCON1	CPUx Program Control 1	19204 <sub>H</sub>	See Family Spec
CPU2_PCON2	CPUx Program Control 2	19208 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_PCON0	CPUx Program Control 0	1920C <sub>H</sub>	See Family Spec
CPU2_PIEAR	CPUx Program Integrity Error Address Register	19210 <sub>H</sub>	See Family Spec
CPU2_PIETR	CPUx Program Integrity Error Trap Register	19214 <sub>H</sub>	See Family Spec
CPU2_COMPAT	CPUx Compatibility Control Register	19400 <sub>H</sub>	See Family Spec
CPU2_FPU_TRAP_CO_N	CPUx Trap Control Register	1A000 <sub>H</sub>	See Family Spec
CPU2_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 <sub>H</sub>	See Family Spec
CPU2_FPU_TRAP_OP_C	CPUx Trapping Instruction Opcode Register	1A008 <sub>H</sub>	See Family Spec
CPU2_FPU_TRAP_SR_C1	CPUx Trapping Instruction Operand Register	1A010 <sub>H</sub>	See Family Spec
CPU2_FPU_TRAP_SR_C2	CPUx Trapping Instruction Operand Register	1A014 <sub>H</sub>	See Family Spec
CPU2_FPU_TRAP_SR_C3	CPUx Trapping Instruction Operand Register	1A018 <sub>H</sub>	See Family Spec
CPU2_DPRy_L (y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 <sub>H</sub> +y*8	See Family Spec
CPU2_DPRy_U (y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 <sub>H</sub> +y*8	See Family Spec
CPU2_CPRy_L (y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 <sub>H</sub> +y*8	See Family Spec
CPU2_CPRy_U (y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 <sub>H</sub> +y*8	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_CPxExE_y (y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 <sub>H</sub> +y*4	See Family Spec
CPU2_DPxRE_y (y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 <sub>H</sub> +y*4	See Family Spec
CPU2_DPxWE_y (y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 <sub>H</sub> +y*4	See Family Spec
CPU2_CPxExE_y (y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 <sub>H</sub> +(y-4)*4	See Family Spec
CPU2_DPxRE_y (y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 <sub>H</sub> +(y-4)*4	See Family Spec
CPU2_DPxWE_y (y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 <sub>H</sub> +(y-4)*4	See Family Spec
CPU2_TPS_CON	CPUx Temporal Protection System Control Register	1E400 <sub>H</sub>	See Family Spec
CPU2_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 <sub>H</sub> +y*4	See Family Spec
CPU2_TPS_EXTIM_E_NTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 <sub>H</sub>	See Family Spec
CPU2_TPS_EXTIM_E_NTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 <sub>H</sub>	See Family Spec
CPU2_TPS_EXTIM_E_XIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 <sub>H</sub>	See Family Spec
CPU2_TPS_EXTIM_E_XIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C <sub>H</sub>	See Family Spec
CPU2_TPS_EXTIM_C_LASS_EN	CPUx Exception Timer Class Enable Register	1E450 <sub>H</sub>	See Family Spec
CPU2_TPS_EXTIM_S_TAT	CPUx Exception Timer Status Register	1E454 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_TPS_EXTIM_FCX	CPUx Exception Timer FCX Register	1E458 <sub>H</sub>	See Family Spec
CPU2_TRIEVT (i=0-7)	CPUx Trigger Event i	1F000 <sub>H</sub> +i*8	See Family Spec
CPU2_TRIADR (i=0-7)	CPUx Trigger Address i	1F004 <sub>H</sub> +i*8	See Family Spec
CPU2_CCTRL	CPUx Counter Control	1FC00 <sub>H</sub>	See Family Spec
CPU2_CCNT	CPUx CPU Clock Cycle Count	1FC04 <sub>H</sub>	See Family Spec
CPU2_ICNT	CPUx Instruction Count	1FC08 <sub>H</sub>	See Family Spec
CPU2_M1CNT	CPUx Multi-Count Register 1	1FC0C <sub>H</sub>	See Family Spec
CPU2_M2CNT	CPUx Multi-Count Register 2	1FC10 <sub>H</sub>	See Family Spec
CPU2_M3CNT	CPUx Multi-Count Register 3	1FC14 <sub>H</sub>	See Family Spec
CPU2_DBGSR	CPUx Debug Status Register	1FD00 <sub>H</sub>	See Family Spec
CPU2_EXEVT	CPUx External Event Register	1FD08 <sub>H</sub>	See Family Spec
CPU2_CREVT	CPUx Core Register Access Event	1FD0C <sub>H</sub>	See Family Spec
CPU2_SWEVT	CPUx Software Debug Event	1FD10 <sub>H</sub>	See Family Spec
CPU2_TRIG_ACC	CPUx TriggerAddressx	1FD30 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_DMS	CPUx Debug Monitor Start Address	1FD40 <sub>H</sub>	See Family Spec
CPU2_DCX	CPUx Debug Context Save Area Pointer	1FD44 <sub>H</sub>	See Family Spec
CPU2_DBGTCR	CPUx Debug Trap Control Register	1FD48 <sub>H</sub>	See Family Spec
CPU2_PCXI	CPUx Previous Context Information Register	1FE00 <sub>H</sub>	See Family Spec
CPU2_PSW	CPUx Program Status Word	1FE04 <sub>H</sub>	See Family Spec
CPU2_PC	CPUx Program Counter	1FE08 <sub>H</sub>	See Family Spec
CPU2_SYSCON	CPUx System Configuration Register	1FE14 <sub>H</sub>	See Family Spec
CPU2_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 <sub>H</sub>	See Family Spec
CPU2_CORE_ID	CPUx Core Identification Register	1FE1C <sub>H</sub>	See Family Spec
CPU2_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 <sub>H</sub>	See Family Spec
CPU2_BTV	CPUx Base Trap Vector Table Pointer	1FE24 <sub>H</sub>	See Family Spec
CPU2_ISP	CPUx Interrupt Stack Pointer	1FE28 <sub>H</sub>	See Family Spec
CPU2_ICR	CPUx Interrupt Control Register	1FE2C <sub>H</sub>	See Family Spec
CPU2_FCX	CPUx Free CSA List Head Pointer	1FE38 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 23 Register Overview - CPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU2_LCX	CPUx Free CSA List Limit Pointer	1FE3C <sub>H</sub>	See Family Spec
CPU2_CUS_ID	CPUx Customer ID register	1FE50 <sub>H</sub>	See Family Spec
CPU2_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 <sub>H</sub> +y*4	See Family Spec
CPU2_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 <sub>H</sub> +y*4	See Family Spec

**Table 24 Register Overview - CPU3 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_FLASHCON0	CPUx Flash Configuration Register 0	01100 <sub>H</sub>	<b>48</b>
CPU3_FLASHCON1	CPUx Flash Configuration Register 1	01104 <sub>H</sub>	See Family Spec
CPU3_FLASHCON2	CPUx Flash Configuration Register 2	01108 <sub>H</sub>	See Family Spec
CPU3_FLASHCON3	CPUx Flash Configuration Register 3	0110C <sub>H</sub>	See Family Spec
CPU3_FLASHCON4	CPUx Flash Configuration Register 4	01110 <sub>H</sub>	See Family Spec
CPU3_KRST0	CPUx Reset Register 0	0D000 <sub>H</sub>	See Family Spec
CPU3_KRST1	CPUx Reset Register 1	0D004 <sub>H</sub>	See Family Spec
CPU3_KRSTCLR	CPUx Reset Clear Register	0D008 <sub>H</sub>	See Family Spec
CPU3_SPR_SPROT_R GNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 24 Register Overview - CPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_SPR_SPROT_R GNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_SPR_SPROT_R GNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_SPR_SPROT_R GNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_SPR_SPROT_R GNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_SPR_SPROT_R GNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_SFR_SPROT_A CCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 <sub>H</sub>	See Family Spec
CPU3_SFR_SPROT_A CCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 <sub>H</sub>	See Family Spec
CPU3_LPB_SPROT_A CCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 <sub>H</sub>	See Family Spec
CPU3_LPB_SPROT_A CCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 <sub>H</sub>	See Family Spec
CPU3_DLMU_SPROT _RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_DLMU_SPROT _RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_DLMU_SPROT _RGNAACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_DLMU_SPROT _RGNAACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_DLMU_SPROT _RGNAACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 24 Register Overview - CPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_DLMU_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU3_OSEL	CPUx Overlay Range Select Register	0FB00 <sub>H</sub>	See Family Spec
CPU3_RABRi (i=0-31)	CPUx Redirected Address Base Register i	0FB10 <sub>H</sub> +i*12	See Family Spec
CPU3_OTARI (i=0-31)	CPUx Overlay Target Address Register i	0FB14 <sub>H</sub> +i*12	See Family Spec
CPU3_OMASKi (i=0-31)	CPUx Overlay Mask Register i	0FB18 <sub>H</sub> +i*12	See Family Spec
CPU3_SEGEN	CPUx SRI Error Generation Register	11030 <sub>H</sub>	See Family Spec
CPU3_TASK_ASI	CPUx Task Address Space Identifier Register	18004 <sub>H</sub>	See Family Spec
CPU3_PMA0	CPUx Data Access CacheabilityRegister	18100 <sub>H</sub>	See Family Spec
CPU3_PMA1	CPUx Code Access CacheabilityRegister	18104 <sub>H</sub>	See Family Spec
CPU3_PMA2	CPUx Peripheral Space Identifier register	18108 <sub>H</sub>	See Family Spec
CPU3_DCON2	CPUx Data Control Register 2	19000 <sub>H</sub>	See Family Spec
CPU3_SMACON	CPUx SIST Mode Access Control Register	1900C <sub>H</sub>	See Family Spec
CPU3_DSTR	CPUx Data Synchronous Trap Register	19010 <sub>H</sub>	See Family Spec
CPU3_DATR	CPUx Data Asynchronous Trap Register	19018 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 24 Register Overview - CPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_DEADD	CPUx Data Error Address Register	1901C <sub>H</sub>	See Family Spec
CPU3_DIEAR	CPUx Data Integrity Error Address Register	19020 <sub>H</sub>	See Family Spec
CPU3_DIETR	CPUx Data Integrity Error Trap Register	19024 <sub>H</sub>	See Family Spec
CPU3_DCON0	CPUx Data Memory Control Register	19040 <sub>H</sub>	See Family Spec
CPU3_PSTR	CPUx Program Synchronous Trap Register	19200 <sub>H</sub>	See Family Spec
CPU3_PCON1	CPUx Program Control 1	19204 <sub>H</sub>	See Family Spec
CPU3_PCON2	CPUx Program Control 2	19208 <sub>H</sub>	See Family Spec
CPU3_PCON0	CPUx Program Control 0	1920C <sub>H</sub>	See Family Spec
CPU3_PIEAR	CPUx Program Integrity Error Address Register	19210 <sub>H</sub>	See Family Spec
CPU3_PIETR	CPUx Program Integrity Error Trap Register	19214 <sub>H</sub>	See Family Spec
CPU3_COMPAT	CPUx Compatibility Control Register	19400 <sub>H</sub>	See Family Spec
CPU3_FPU_TRAP_CO_N	CPUx Trap Control Register	1A000 <sub>H</sub>	See Family Spec
CPU3_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 <sub>H</sub>	See Family Spec
CPU3_FPU_TRAP_OP_C	CPUx Trapping Instruction Opcode Register	1A008 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 24 Register Overview - CPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_FPU_TRAP_SR_C1	CPUx Trapping Instruction Operand Register	1A010 <sub>H</sub>	See Family Spec
CPU3_FPU_TRAP_SR_C2	CPUx Trapping Instruction Operand Register	1A014 <sub>H</sub>	See Family Spec
CPU3_FPU_TRAP_SR_C3	CPUx Trapping Instruction Operand Register	1A018 <sub>H</sub>	See Family Spec
CPU3_DPRy_L(y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 <sub>H</sub> +y*8	See Family Spec
CPU3_DPRy_U(y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 <sub>H</sub> +y*8	See Family Spec
CPU3_CPRy_L(y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 <sub>H</sub> +y*8	See Family Spec
CPU3_CPRy_U(y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 <sub>H</sub> +y*8	See Family Spec
CPU3_CPXE_y(y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 <sub>H</sub> +y*4	See Family Spec
CPU3_DPREG_y(y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 <sub>H</sub> +y*4	See Family Spec
CPU3_DPWE_y(y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 <sub>H</sub> +y*4	See Family Spec
CPU3_CPXE_y(y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 <sub>H</sub> +(y-4)*4	See Family Spec
CPU3_DPREG_y(y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 <sub>H</sub> +(y-4)*4	See Family Spec
CPU3_DPWE_y(y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 <sub>H</sub> +(y-4)*4	See Family Spec
CPU3_TPS_CON	CPUx Temporal Protection System Control Register	1E400 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 24 Register Overview - CPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 <sub>H</sub> +y*4	See Family Spec
CPU3_TPS_EXTIM_E_NTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 <sub>H</sub>	See Family Spec
CPU3_TPS_EXTIM_E_NTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 <sub>H</sub>	See Family Spec
CPU3_TPS_EXTIM_E_XIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 <sub>H</sub>	See Family Spec
CPU3_TPS_EXTIM_E_XIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C <sub>H</sub>	See Family Spec
CPU3_TPS_EXTIM_C_LASS_EN	CPUx Exception Timer Class Enable Register	1E450 <sub>H</sub>	See Family Spec
CPU3_TPS_EXTIM_S_TAT	CPUx Exception Timer Status Register	1E454 <sub>H</sub>	See Family Spec
CPU3_TPS_EXTIM_F_CX	CPUx Exception Timer FCX Register	1E458 <sub>H</sub>	See Family Spec
CPU3_TRIEVT (i=0-7)	CPUx Trigger Event i	1F000 <sub>H</sub> +i*8	See Family Spec
CPU3_TRIADR (i=0-7)	CPUx Trigger Address i	1F004 <sub>H</sub> +i*8	See Family Spec
CPU3_CCTRL	CPUx Counter Control	1FC00 <sub>H</sub>	See Family Spec
CPU3_CCNT	CPUx CPU Clock Cycle Count	1FC04 <sub>H</sub>	See Family Spec
CPU3_ICNT	CPUx Instruction Count	1FC08 <sub>H</sub>	See Family Spec
CPU3_M1CNT	CPUx Multi-Count Register 1	1FC0C <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 24 Register Overview - CPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_M2CNT	CPUx Multi-Count Register 2	1FC10 <sub>H</sub>	See Family Spec
CPU3_M3CNT	CPUx Multi-Count Register 3	1FC14 <sub>H</sub>	See Family Spec
CPU3_DBGSR	CPUx Debug Status Register	1FD00 <sub>H</sub>	See Family Spec
CPU3_EXEVT	CPUx External Event Register	1FD08 <sub>H</sub>	See Family Spec
CPU3_CREVT	CPUx Core Register Access Event	1FD0C <sub>H</sub>	See Family Spec
CPU3_SWEVT	CPUx Software Debug Event	1FD10 <sub>H</sub>	See Family Spec
CPU3_TRIG_ACC	CPUx TriggerAddressx	1FD30 <sub>H</sub>	See Family Spec
CPU3_DMS	CPUx Debug Monitor Start Address	1FD40 <sub>H</sub>	See Family Spec
CPU3_DCX	CPUx Debug Context Save Area Pointer	1FD44 <sub>H</sub>	See Family Spec
CPU3_DBGTCR	CPUx Debug Trap Control Register	1FD48 <sub>H</sub>	See Family Spec
CPU3_PCXI	CPUx Previous Context Information Register	1FE00 <sub>H</sub>	See Family Spec
CPU3_PSW	CPUx Program Status Word	1FE04 <sub>H</sub>	See Family Spec
CPU3_PC	CPUx Program Counter	1FE08 <sub>H</sub>	See Family Spec
CPU3_SYSCON	CPUx System Configuration Register	1FE14 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 24 Register Overview - CPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU3_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 <sub>H</sub>	See Family Spec
CPU3_CORE_ID	CPUx Core Identification Register	1FE1C <sub>H</sub>	See Family Spec
CPU3_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 <sub>H</sub>	See Family Spec
CPU3_BTV	CPUx Base Trap Vector Table Pointer	1FE24 <sub>H</sub>	See Family Spec
CPU3_ISP	CPUx Interrupt Stack Pointer	1FE28 <sub>H</sub>	See Family Spec
CPU3_ICR	CPUx Interrupt Control Register	1FE2C <sub>H</sub>	See Family Spec
CPU3_FCX	CPUx Free CSA List Head Pointer	1FE38 <sub>H</sub>	See Family Spec
CPU3_LCX	CPUx Free CSA List Limit Pointer	1FE3C <sub>H</sub>	See Family Spec
CPU3_CUS_ID	CPUx Customer ID register	1FE50 <sub>H</sub>	See Family Spec
CPU3_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 <sub>H</sub> +y*4	See Family Spec
CPU3_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 <sub>H</sub> +y*4	See Family Spec

**Table 25 Register Overview - CPU4 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_FLASHCON0	CPUx Flash Configuration Register 0	01100 <sub>H</sub>	<b>48</b>
CPU4_FLASHCON1	CPUx Flash Configuration Register 1	01104 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_FLASHCON2	CPUx Flash Configuration Register 2	01108 <sub>H</sub>	See Family Spec
CPU4_FLASHCON3	CPUx Flash Configuration Register 3	0110C <sub>H</sub>	See Family Spec
CPU4_FLASHCON4	CPUx Flash Configuration Register 4	01110 <sub>H</sub>	See Family Spec
CPU4_KRST0	CPUx Reset Register 0	0D000 <sub>H</sub>	See Family Spec
CPU4_KRST1	CPUx Reset Register 1	0D004 <sub>H</sub>	See Family Spec
CPU4_KRSTCLR	CPUx Reset Clear Register	0D008 <sub>H</sub>	See Family Spec
CPU4_SPR_SPROT_R GNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_SPR_SPROT_R GNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_SPR_SPROT_R GNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_SPR_SPROT_R GNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_SPR_SPROT_R GNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_SPR_SPROT_R GNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_SFR_SPROT_A CCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 <sub>H</sub>	See Family Spec
CPU4_SFR_SPROT_A CCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_LPБ_SPROT_A CCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 <sub>H</sub>	See Family Spec
CPU4_LPБ_SPROT_A CCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 <sub>H</sub>	See Family Spec
CPU4_DLMU_SPROT _RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_DLMU_SPROT _RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_DLMU_SPROT _RGNACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_DLMU_SPROT _RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_DLMU_SPROT _RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_DLMU_SPROT _RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU4_OSEL	CPUx Overlay Range Select Register	0FB00 <sub>H</sub>	See Family Spec
CPU4_RABRi (i=0-31)	CPUx Redirected Address Base Register i	0FB10 <sub>H</sub> +i*12	See Family Spec
CPU4_OTARI (i=0-31)	CPUx Overlay Target Address Register i	0FB14 <sub>H</sub> +i*12	See Family Spec
CPU4_OMASKi (i=0-31)	CPUx Overlay Mask Register i	0FB18 <sub>H</sub> +i*12	See Family Spec
CPU4_SEGEN	CPUx SRI Error Generation Register	11030 <sub>H</sub>	See Family Spec
CPU4_TASK_ASİ	CPUx Task Address Space Identifier Register	18004 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_PMA0	CPUx Data Access CacheabilityRegister	18100 <sub>H</sub>	See Family Spec
CPU4_PMA1	CPUx Code Access CacheabilityRegister	18104 <sub>H</sub>	See Family Spec
CPU4_PMA2	CPUx Peripheral Space Identifier register	18108 <sub>H</sub>	See Family Spec
CPU4_DCON2	CPUx Data Control Register 2	19000 <sub>H</sub>	See Family Spec
CPU4_SMACON	CPUx SIST Mode Access Control Register	1900C <sub>H</sub>	See Family Spec
CPU4_DSTR	CPUx Data Synchronous Trap Register	19010 <sub>H</sub>	See Family Spec
CPU4_DATR	CPUx Data Asynchronous Trap Register	19018 <sub>H</sub>	See Family Spec
CPU4_DEADD	CPUx Data Error Address Register	1901C <sub>H</sub>	See Family Spec
CPU4_DIEAR	CPUx Data Integrity Error Address Register	19020 <sub>H</sub>	See Family Spec
CPU4_DIETR	CPUx Data Integrity Error Trap Register	19024 <sub>H</sub>	See Family Spec
CPU4_DCON0	CPUx Data Memory Control Register	19040 <sub>H</sub>	See Family Spec
CPU4_PSTR	CPUx Program Synchronous Trap Register	19200 <sub>H</sub>	See Family Spec
CPU4_PCON1	CPUx Program Control 1	19204 <sub>H</sub>	See Family Spec
CPU4_PCON2	CPUx Program Control 2	19208 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_PCON0	CPUx Program Control 0	1920C <sub>H</sub>	See Family Spec
CPU4_PIEAR	CPUx Program Integrity Error Address Register	19210 <sub>H</sub>	See Family Spec
CPU4_PIETR	CPUx Program Integrity Error Trap Register	19214 <sub>H</sub>	See Family Spec
CPU4_COMPAT	CPUx Compatibility Control Register	19400 <sub>H</sub>	See Family Spec
CPU4_FPU_TRAP_CO_N	CPUx Trap Control Register	1A000 <sub>H</sub>	See Family Spec
CPU4_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 <sub>H</sub>	See Family Spec
CPU4_FPU_TRAP_OP_C	CPUx Trapping Instruction Opcode Register	1A008 <sub>H</sub>	See Family Spec
CPU4_FPU_TRAP_SR_C1	CPUx Trapping Instruction Operand Register	1A010 <sub>H</sub>	See Family Spec
CPU4_FPU_TRAP_SR_C2	CPUx Trapping Instruction Operand Register	1A014 <sub>H</sub>	See Family Spec
CPU4_FPU_TRAP_SR_C3	CPUx Trapping Instruction Operand Register	1A018 <sub>H</sub>	See Family Spec
CPU4_DPRy_L (y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 <sub>H</sub> +y*8	See Family Spec
CPU4_DPRy_U (y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 <sub>H</sub> +y*8	See Family Spec
CPU4_CPRy_L (y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 <sub>H</sub> +y*8	See Family Spec
CPU4_CPRy_U (y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 <sub>H</sub> +y*8	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_CPxExE_y (y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 <sub>H</sub> +y*4	See Family Spec
CPU4_DPxRE_y (y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 <sub>H</sub> +y*4	See Family Spec
CPU4_DPxWE_y (y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 <sub>H</sub> +y*4	See Family Spec
CPU4_CPxExE_y (y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 <sub>H</sub> +(y-4)*4	See Family Spec
CPU4_DPxRE_y (y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 <sub>H</sub> +(y-4)*4	See Family Spec
CPU4_DPxWE_y (y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 <sub>H</sub> +(y-4)*4	See Family Spec
CPU4_TPS_CON	CPUx Temporal Protection System Control Register	1E400 <sub>H</sub>	See Family Spec
CPU4_TPS_TIMERY (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 <sub>H</sub> +y*4	See Family Spec
CPU4_TPS_EXTIM_E NTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 <sub>H</sub>	See Family Spec
CPU4_TPS_EXTIM_E NTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 <sub>H</sub>	See Family Spec
CPU4_TPS_EXTIM_E XIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 <sub>H</sub>	See Family Spec
CPU4_TPS_EXTIM_E XIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C <sub>H</sub>	See Family Spec
CPU4_TPS_EXTIM_C LASS_EN	CPUx Exception Timer Class Enable Register	1E450 <sub>H</sub>	See Family Spec
CPU4_TPS_EXTIM_S TAT	CPUx Exception Timer Status Register	1E454 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_TPS_EXTIM_FCX	CPUx Exception Timer FCX Register	1E458 <sub>H</sub>	See Family Spec
CPU4_TRIEVT (i=0-7)	CPUx Trigger Event i	1F000 <sub>H</sub> +i*8	See Family Spec
CPU4_TRIADR (i=0-7)	CPUx Trigger Address i	1F004 <sub>H</sub> +i*8	See Family Spec
CPU4_CCTRL	CPUx Counter Control	1FC00 <sub>H</sub>	See Family Spec
CPU4_CCNT	CPUx CPU Clock Cycle Count	1FC04 <sub>H</sub>	See Family Spec
CPU4_ICNT	CPUx Instruction Count	1FC08 <sub>H</sub>	See Family Spec
CPU4_M1CNT	CPUx Multi-Count Register 1	1FC0C <sub>H</sub>	See Family Spec
CPU4_M2CNT	CPUx Multi-Count Register 2	1FC10 <sub>H</sub>	See Family Spec
CPU4_M3CNT	CPUx Multi-Count Register 3	1FC14 <sub>H</sub>	See Family Spec
CPU4_DBGSR	CPUx Debug Status Register	1FD00 <sub>H</sub>	See Family Spec
CPU4_EXEVT	CPUx External Event Register	1FD08 <sub>H</sub>	See Family Spec
CPU4_CREVT	CPUx Core Register Access Event	1FD0C <sub>H</sub>	See Family Spec
CPU4_SWEVT	CPUx Software Debug Event	1FD10 <sub>H</sub>	See Family Spec
CPU4_TRIG_ACC	CPUx TriggerAddressx	1FD30 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_DMS	CPUx Debug Monitor Start Address	1FD40 <sub>H</sub>	See Family Spec
CPU4_DCX	CPUx Debug Context Save Area Pointer	1FD44 <sub>H</sub>	See Family Spec
CPU4_DBGTCR	CPUx Debug Trap Control Register	1FD48 <sub>H</sub>	See Family Spec
CPU4_PCXI	CPUx Previous Context Information Register	1FE00 <sub>H</sub>	See Family Spec
CPU4_PSW	CPUx Program Status Word	1FE04 <sub>H</sub>	See Family Spec
CPU4_PC	CPUx Program Counter	1FE08 <sub>H</sub>	See Family Spec
CPU4_SYSCON	CPUx System Configuration Register	1FE14 <sub>H</sub>	See Family Spec
CPU4_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 <sub>H</sub>	See Family Spec
CPU4_CORE_ID	CPUx Core Identification Register	1FE1C <sub>H</sub>	See Family Spec
CPU4_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 <sub>H</sub>	See Family Spec
CPU4_BTV	CPUx Base Trap Vector Table Pointer	1FE24 <sub>H</sub>	See Family Spec
CPU4_ISP	CPUx Interrupt Stack Pointer	1FE28 <sub>H</sub>	See Family Spec
CPU4_ICR	CPUx Interrupt Control Register	1FE2C <sub>H</sub>	See Family Spec
CPU4_FCX	CPUx Free CSA List Head Pointer	1FE38 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 25 Register Overview - CPU4 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU4_LCX	CPUx Free CSA List Limit Pointer	1FE3C <sub>H</sub>	See Family Spec
CPU4_CUS_ID	CPUx Customer ID register	1FE50 <sub>H</sub>	See Family Spec
CPU4_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 <sub>H</sub> +y*4	See Family Spec
CPU4_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 <sub>H</sub> +y*4	See Family Spec

**Table 26 Register Overview - CPU5 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_FLASHCON0	CPUx Flash Configuration Register 0	01100 <sub>H</sub>	<b>48</b>
CPU5_FLASHCON1	CPUx Flash Configuration Register 1	01104 <sub>H</sub>	See Family Spec
CPU5_FLASHCON2	CPUx Flash Configuration Register 2	01108 <sub>H</sub>	See Family Spec
CPU5_FLASHCON3	CPUx Flash Configuration Register 3	0110C <sub>H</sub>	See Family Spec
CPU5_FLASHCON4	CPUx Flash Configuration Register 4	01110 <sub>H</sub>	See Family Spec
CPU5_KRST0	CPUx Reset Register 0	0D000 <sub>H</sub>	See Family Spec
CPU5_KRST1	CPUx Reset Register 1	0D004 <sub>H</sub>	See Family Spec
CPU5_KRSTCLR	CPUx Reset Clear Register	0D008 <sub>H</sub>	See Family Spec
CPU5_SPR_SPROT_R GNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 26 Register Overview - CPU5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_SPR_SPROT_R GNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_SPR_SPROT_R GNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_SPR_SPROT_R GNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_SPR_SPROT_R GNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_SPR_SPROT_R GNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_SFR_SPROT_A CCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 <sub>H</sub>	See Family Spec
CPU5_SFR_SPROT_A CCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 <sub>H</sub>	See Family Spec
CPU5_LPB_SPROT_A CCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 <sub>H</sub>	See Family Spec
CPU5_LPB_SPROT_A CCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 <sub>H</sub>	See Family Spec
CPU5_DLMU_SPROT _RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_DLMU_SPROT _RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_DLMU_SPROT _RGNACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_DLMU_SPROT _RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_DLMU_SPROT _RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 26 Register Overview - CPU5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_DLMU_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C <sub>H</sub> +i*10 <sub>H</sub>	See Family Spec
CPU5_OSEL	CPUx Overlay Range Select Register	0FB00 <sub>H</sub>	See Family Spec
CPU5_RABRi (i=0-31)	CPUx Redirected Address Base Register i	0FB10 <sub>H</sub> +i*12	See Family Spec
CPU5_OTARI (i=0-31)	CPUx Overlay Target Address Register i	0FB14 <sub>H</sub> +i*12	See Family Spec
CPU5_OMASKi (i=0-31)	CPUx Overlay Mask Register i	0FB18 <sub>H</sub> +i*12	See Family Spec
CPU5_SEGEN	CPUx SRI Error Generation Register	11030 <sub>H</sub>	See Family Spec
CPU5_TASK_ASI	CPUx Task Address Space Identifier Register	18004 <sub>H</sub>	See Family Spec
CPU5_PMA0	CPUx Data Access CacheabilityRegister	18100 <sub>H</sub>	See Family Spec
CPU5_PMA1	CPUx Code Access CacheabilityRegister	18104 <sub>H</sub>	See Family Spec
CPU5_PMA2	CPUx Peripheral Space Identifier register	18108 <sub>H</sub>	See Family Spec
CPU5_DCON2	CPUx Data Control Register 2	19000 <sub>H</sub>	See Family Spec
CPU5_SMACON	CPUx SIST Mode Access Control Register	1900C <sub>H</sub>	See Family Spec
CPU5_DSTR	CPUx Data Synchronous Trap Register	19010 <sub>H</sub>	See Family Spec
CPU5_DATR	CPUx Data Asynchronous Trap Register	19018 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 26 Register Overview - CPU5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_DEADD	CPUx Data Error Address Register	1901C <sub>H</sub>	See Family Spec
CPU5_DIEAR	CPUx Data Integrity Error Address Register	19020 <sub>H</sub>	See Family Spec
CPU5_DIETR	CPUx Data Integrity Error Trap Register	19024 <sub>H</sub>	See Family Spec
CPU5_DCON0	CPUx Data Memory Control Register	19040 <sub>H</sub>	See Family Spec
CPU5_PSTR	CPUx Program Synchronous Trap Register	19200 <sub>H</sub>	See Family Spec
CPU5_PCON1	CPUx Program Control 1	19204 <sub>H</sub>	See Family Spec
CPU5_PCON2	CPUx Program Control 2	19208 <sub>H</sub>	See Family Spec
CPU5_PCON0	CPUx Program Control 0	1920C <sub>H</sub>	See Family Spec
CPU5_PIEAR	CPUx Program Integrity Error Address Register	19210 <sub>H</sub>	See Family Spec
CPU5_PIETR	CPUx Program Integrity Error Trap Register	19214 <sub>H</sub>	See Family Spec
CPU5_COMPAT	CPUx Compatibility Control Register	19400 <sub>H</sub>	See Family Spec
CPU5_FPU_TRAP_CO_N	CPUx Trap Control Register	1A000 <sub>H</sub>	See Family Spec
CPU5_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 <sub>H</sub>	See Family Spec
CPU5_FPU_TRAP_OP_C	CPUx Trapping Instruction Opcode Register	1A008 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 26 Register Overview - CPU5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_FPU_TRAP_SR_C1	CPUx Trapping Instruction Operand Register	1A010 <sub>H</sub>	See Family Spec
CPU5_FPU_TRAP_SR_C2	CPUx Trapping Instruction Operand Register	1A014 <sub>H</sub>	See Family Spec
CPU5_FPU_TRAP_SR_C3	CPUx Trapping Instruction Operand Register	1A018 <sub>H</sub>	See Family Spec
CPU5_DPRy_L(y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 <sub>H</sub> +y*8	See Family Spec
CPU5_DPRy_U(y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 <sub>H</sub> +y*8	See Family Spec
CPU5_CPRy_L(y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 <sub>H</sub> +y*8	See Family Spec
CPU5_CPRy_U(y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 <sub>H</sub> +y*8	See Family Spec
CPU5_CPXE_y(y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 <sub>H</sub> +y*4	See Family Spec
CPU5_DPREG_y(y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 <sub>H</sub> +y*4	See Family Spec
CPU5_DPWE_y(y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 <sub>H</sub> +y*4	See Family Spec
CPU5_CPXE_y(y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 <sub>H</sub> +(y-4)*4	See Family Spec
CPU5_DPREG_y(y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 <sub>H</sub> +(y-4)*4	See Family Spec
CPU5_DPWE_y(y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 <sub>H</sub> +(y-4)*4	See Family Spec
CPU5_TPS_CON	CPUx Temporal Protection System Control Register	1E400 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 26 Register Overview - CPU5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 <sub>H</sub> +y*4	See Family Spec
CPU5_TPS_EXTIM_E_NTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 <sub>H</sub>	See Family Spec
CPU5_TPS_EXTIM_E_NTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 <sub>H</sub>	See Family Spec
CPU5_TPS_EXTIM_E_XIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 <sub>H</sub>	See Family Spec
CPU5_TPS_EXTIM_E_XIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C <sub>H</sub>	See Family Spec
CPU5_TPS_EXTIM_C_LASS_EN	CPUx Exception Timer Class Enable Register	1E450 <sub>H</sub>	See Family Spec
CPU5_TPS_EXTIM_S_TAT	CPUx Exception Timer Status Register	1E454 <sub>H</sub>	See Family Spec
CPU5_TPS_EXTIM_F_CX	CPUx Exception Timer FCX Register	1E458 <sub>H</sub>	See Family Spec
CPU5_TRIEVT (i=0-7)	CPUx Trigger Event i	1F000 <sub>H</sub> +i*8	See Family Spec
CPU5_TRIADR (i=0-7)	CPUx Trigger Address i	1F004 <sub>H</sub> +i*8	See Family Spec
CPU5_CCTRL	CPUx Counter Control	1FC00 <sub>H</sub>	See Family Spec
CPU5_CCNT	CPUx CPU Clock Cycle Count	1FC04 <sub>H</sub>	See Family Spec
CPU5_ICNT	CPUx Instruction Count	1FC08 <sub>H</sub>	See Family Spec
CPU5_M1CNT	CPUx Multi-Count Register 1	1FC0C <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 26 Register Overview - CPU5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_M2CNT	CPUx Multi-Count Register 2	1FC10 <sub>H</sub>	See Family Spec
CPU5_M3CNT	CPUx Multi-Count Register 3	1FC14 <sub>H</sub>	See Family Spec
CPU5_DBGSR	CPUx Debug Status Register	1FD00 <sub>H</sub>	See Family Spec
CPU5_EXEVT	CPUx External Event Register	1FD08 <sub>H</sub>	See Family Spec
CPU5_CREVT	CPUx Core Register Access Event	1FD0C <sub>H</sub>	See Family Spec
CPU5_SWEVT	CPUx Software Debug Event	1FD10 <sub>H</sub>	See Family Spec
CPU5_TRIG_ACC	CPUx TriggerAddressx	1FD30 <sub>H</sub>	See Family Spec
CPU5_DMS	CPUx Debug Monitor Start Address	1FD40 <sub>H</sub>	See Family Spec
CPU5_DCX	CPUx Debug Context Save Area Pointer	1FD44 <sub>H</sub>	See Family Spec
CPU5_DBGTCR	CPUx Debug Trap Control Register	1FD48 <sub>H</sub>	See Family Spec
CPU5_PCXI	CPUx Previous Context Information Register	1FE00 <sub>H</sub>	See Family Spec
CPU5_PSW	CPUx Program Status Word	1FE04 <sub>H</sub>	See Family Spec
CPU5_PC	CPUx Program Counter	1FE08 <sub>H</sub>	See Family Spec
CPU5_SYSCON	CPUx System Configuration Register	1FE14 <sub>H</sub>	See Family Spec

**CPU Subsystem (CPU)****Table 26 Register Overview - CPU5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CPU5_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 <sub>H</sub>	See Family Spec
CPU5_CORE_ID	CPUx Core Identification Register	1FE1C <sub>H</sub>	See Family Spec
CPU5_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 <sub>H</sub>	See Family Spec
CPU5_BTV	CPUx Base Trap Vector Table Pointer	1FE24 <sub>H</sub>	See Family Spec
CPU5_ISP	CPUx Interrupt Stack Pointer	1FE28 <sub>H</sub>	See Family Spec
CPU5_ICR	CPUx Interrupt Control Register	1FE2C <sub>H</sub>	See Family Spec
CPU5_FCX	CPUx Free CSA List Head Pointer	1FE38 <sub>H</sub>	See Family Spec
CPU5_LCX	CPUx Free CSA List Limit Pointer	1FE3C <sub>H</sub>	See Family Spec
CPU5_CUS_ID	CPUx Customer ID register	1FE50 <sub>H</sub>	See Family Spec
CPU5_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 <sub>H</sub> +y*4	See Family Spec
CPU5_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 <sub>H</sub> +y*4	See Family Spec

**CPU Subsystem (CPU)****5.3 TC39x-B Specific Registers****5.3.1 SRI slave interface for SFR+CSFR****CPUx Flash Configuration Register 0**

Software may program a Flash Prefetch Buffer with a master tag identifier stored in Flash Configuration Register 0.

If a CPU instance does not have a local PFlash bank then the FLASHCON0 register associated with that instance will have no functionality.

**CPU0\_FLASHCON0**

**CPUx Flash Configuration Register 0** **(01100<sub>H</sub>)** **Reset Value:** [Table 27](#)

**CPU1\_FLASHCON0**

**CPUx Flash Configuration Register 0** **(01100<sub>H</sub>)** **Reset Value:** [Table 28](#)

**CPU2\_FLASHCON0**

**CPUx Flash Configuration Register 0** **(01100<sub>H</sub>)** **Reset Value:** [Table 29](#)

**CPU3\_FLASHCON0**

**CPUx Flash Configuration Register 0** **(01100<sub>H</sub>)** **Reset Value:** [Table 30](#)

**CPU4\_FLASHCON0**

**CPUx Flash Configuration Register 0** **(01100<sub>H</sub>)** **Reset Value:** [Table 31](#)

**CPU5\_FLASHCON0**

**CPUx Flash Configuration Register 0** **(01100<sub>H</sub>)** **Reset Value:** [Table 32](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>RES</b>	<b>TAG4</b>				<b>RES</b>	<b>TAG3</b>				<b>RES</b>	<b>TAG2</b>				<b>RES</b>
r	rw				r	rw				r	rw				r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>	<b>TAG1</b>				<b>RES</b>	<b>TAG1</b>				<b>RES</b>	<b>TAG1</b>				<b>RES</b>
r	rw				r	rw				r	rw				r

Field	Bits	Type	Description
<b>TAG1</b>	5:0	rw	<b>Flash Prefetch Buffer 1 Configuration</b> FPB is assigned to on chip bus master with master tag id equal to TAG1.
<b>RES</b>	7:6, 15:14, 23:22, 31:30	r	<b>Reserved</b> Always read as 0; should be written with 0.
<b>TAG2</b>	13:8	rw	<b>Flash Prefetch Buffer 2 Configuration</b> FPB is assigned to on chip bus master with master tag id equal to TAG2.
<b>TAG3</b>	21:16	rw	<b>Flash Prefetch Buffer 3 Configuration</b> FPB is assigned to on chip bus master with master tag id equal to TAG3.
<b>TAG4</b>	29:24	rw	<b>Flash Prefetch Buffer 4 Configuration</b> FPB is assigned to on chip bus master with master tag id equal to TAG4.

**CPU Subsystem (CPU)****Table 27 Reset Values of CPU0\_FLASHCON0**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	3F3F 3F3F <sub>H</sub>	
CFS Value	2322 2120 <sub>H</sub>	

**Table 28 Reset Values of CPU1\_FLASHCON0**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	3F3F 3F3F <sub>H</sub>	
CFS Value	2322 2021 <sub>H</sub>	

**Table 29 Reset Values of CPU2\_FLASHCON0**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	3F3F 3F3F <sub>H</sub>	
CFS Value	2321 2022 <sub>H</sub>	

**Table 30 Reset Values of CPU3\_FLASHCON0**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	3F3F 3F3F <sub>H</sub>	
CFS Value	2221 2023 <sub>H</sub>	

**Table 31 Reset Values of CPU4\_FLASHCON0**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	3F3F 3F3F <sub>H</sub>	
CFS Value	2221 2024 <sub>H</sub>	

**Table 32 Reset Values of CPU5\_FLASHCON0**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	3F3F 3F3F <sub>H</sub>	
CFS Value	2221 2025 <sub>H</sub>	

## 5.4 Connectivity

No connections in TC39x-B

## 5.5 Revision History

**Table 33 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
<b>V1.1.16</b>	No change	
<b>V1.1.17</b>		

**CPU Subsystem (CPU)****Table 33 Revision History (cont'd)**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
	No change	
<b>V1.1.18</b>		
	No change	
<b>V1.1.19</b>		
	No change	
<b>V1.1.20</b>		
<a href="#">Page 2, 10</a> , <a href="#">17, 25, 32</a> , <a href="#">40</a>	Change index variable from 'x' to intended 'i' for registers SPR_SPROT_RGNACCENAi_R and SPR_SPROT_RGNACCENBi_R to remove confusion with CPU instance variable.	
<a href="#">Page 2, 10</a> , <a href="#">17, 25, 32</a> , <a href="#">40</a>	Change index variable from 'x' to intended 'i' for registers all DLMU_SPROT registers to remove confusion with CPU instance variable.	
<b>V1.1.21</b>		
	No change	

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## Non Volatile Memory (NVM) Subsystem

# 6 Non Volatile Memory (NVM) Subsystem

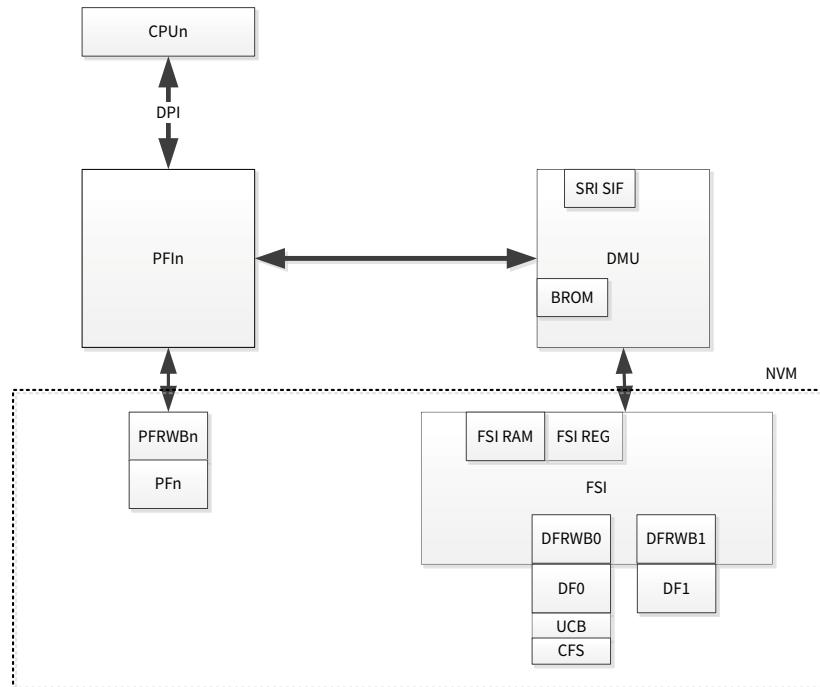
## 6.1 Overview

The Non Volatile Memory (NVM) Subsystem comprises of the Data Memory Unit (DMU), Program Flash Interface (PFI), and Non Volatile Memory module (comprising of the Flash Standard Interface (FSI), Program and Data Flash memories and Program Flash Read Write buffer (PFRWB)).

- Data Memory Unit (DMU): Controls command sequences executed on all program and data flash memories.
- Flash Standard Interface (FSI): Executes erase, program and verify operations on all flash memories.
- Program Flash (PFLASH): Divided into one or more banks each connected to a CPU. It is used by the application to store program code and data constants. Compute performance is optimized by using a point-to-point interface to minimize latency and maximize bandwidth. Each PFLASH is connected to a PFlash Read Write Buffer (PFRWB) that performs the ECC correction and detection and provides the read data to the system.
- Program Flash Interface (PFI): Each PFLASH bank has a unique point-to-point fast connection to a CPU provided by a PFI. The PFI interfaces between the CPU and the PFRWB and contains the Prefetch Buffers for storing speculative data.
- Data Flash (DFLASH): The Data Flash Module is used to emulate EEPROM and store data and divided into two banks. DFLASH read accesses are relatively slow compared to PFLASH accesses. The DFlash Read Write Buffer (DFRWB) in the FSI interfaces to the DFLASH to provide the read data. Data Flash Module also contains regions to store configuration data - User Configuration Blocks (UCBs), and Configuration Sector (CFS) which is not accessible by user.
- Boot ROM (BROM): Connected to the system via the DMU SRI port.
  - Tuning protection (commonly called the “Secure Watchdog”) to protect user software and data from malfunctions.

**Attention:** *The ‘Non Volatile Memory Subsystem’ chapter is the AURIX PMU chapter re-structured for closer alignment to AURIXTC3XX product architecture. It comprises of the DMU, PFI, NVM and UCB Chapters. Please note that the application accessible registers located in the FSI, and the PFLASH read status and control registers are described in the NVM chapter.*

## Non Volatile Memory (NVM) Subsystem



**Figure 6 Non Volatile Memory (NVM) Subsystem**

The purpose of the PFLASH NVM is:

- One or more PFLASH banks stores program code and data constants.
- Implementation of Erase Counters.

The purpose of the DFLASH NVM is:

- Emulation of Electrically Erasable Programmable Read Only Memory (EEPROM):
  - CPU-EEPROM used by the user application.
  - HSM-EEPROM used by the security application.
- Multiple User Configuration Blocks (UCB) used for:
  - Password based read protection combined with write protection.
  - Read-only UCB configured by IFX with unique chip identifier and trimming data.
- Configuration Sector (CFS) stores system set-up data not accessible by the user.

Data stored in the NVM is protected by ECC checksum.

- An ECC decoder at the output of the NVM corrects and detects faults in the NVM array.
- The NVM is fault tolerant and supports system operation in the presence of a number of NVM bit errors.
- For Program Flash the calculation of the ECC checksum is extended across the address to provide read protection against addressing faults.

If the Flash is not operating in the application then the NVM may be programmed and erased by command sequences executed by the FSI micro controller. All read accesses to Flash are memory mapped reads. Margin read levels may be used to check how completely a cell is programmed or erased.

The Non Volatile Memory interface micro architecture includes a security layer and a safety layer.

### Security Layer (provided by DMU and PFI)

- Read protection is enabled/disabled with a Flash Module (Bank) granularity.

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## Non Volatile Memory (NVM) Subsystem

- Write protection is enabled/disabled with a Flash Module sector based granularity.

### Safety Layer

- Master specific read access protection to each Flash Module (Bank).
- Master specific read and write access control to individual Special Function Registers (SFRs).
- Integrity of data stored in the NVM is ensured by an ECC checksum
- Integrity of PFlash read path is ensured by monitoring of read parameters in the FSI (MISR, redundant Flip Flops etc.), PFI partial lockstep mechanism, protection of PFlash wait cycles with ECC checksum, protection of data from PFI to CPU by ECC checksum and an additional safety mechanism to ensure that the local PFlash is not being programmed/erased when not expected by PFI.

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**Non Volatile Memory (NVM) Subsystem****6.2 Revision History****Table 34 Revision History**

Reference	Change to Previous Version	Comment
V2.0.3	Created to form a concise introduction chapter for the appendices	
V2.0.4	No Changes.	
V2.0.5	No Changes.	
V2.0.6	No Changes.	
V2.0.7	No Changes.	

## 6.3 Data Memory Unit (DMU)

This chapter supplements the family documentation with the device specific information for TC39x-B.

### 6.3.1 TC39x-B Specific Register Set

#### Register Address Space Table

**Table 35 Register Address Space - PMU**

Module	Base Address	End Address	Note
PMU	F8038000 <sub>H</sub>	F803FFFF <sub>H</sub>	sri slave interface

**Table 36 Register Address Space - DMU**

Module	Base Address	End Address	Note
(DMU)	8FFF0000 <sub>H</sub>	8FFFFFFF <sub>H</sub>	Boot ROM (BROM)
	AF000000 <sub>H</sub>	AF0FFFFF <sub>H</sub>	Data Flash 0 EEPROM (DF0) and Host Command Sequence Interpreter
	AFC00000 <sub>H</sub>	AFC1FFFF <sub>H</sub>	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter
	AFFF0000 <sub>H</sub>	AFFFFFFF <sub>H</sub>	Boot ROM (BROM)
DMU	F8040000 <sub>H</sub>	F807FFFF <sub>H</sub>	SRI slave interface - Register Address Space
(DMU)	FFC00000 <sub>H</sub>	FFC1FFFF <sub>H</sub>	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter

#### Register Overview Table

**Table 37 Register Overview - PMU (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMU_ID	Module Identification Register	0508 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec

**Table 38 Register Overview - DMU (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HF_ID	Module Identification Register	0000008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMU_HF_STATUS	Flash Status Register	0000010 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONTROL	Flash Control Register	0000014 <sub>H</sub>	U,SV	P,SV,E	Application Reset	See Family Spec

**Table 38 Register Overview - DMU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMU_HF_OPERATION	Flash Operation Register	0000018H	U,SV	BE	System Reset	See Family Spec
DMU_HF_PROTECT	Flash Protection Status Register	000001CH	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONFIRM0	Flash Confirm Status Register 0	0000020H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONFIRM1	Flash Confirm Status Register 1	0000024H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONFIRM2	Flash Confirm Status Register 2	0000028H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_EER	Enable Error Interrupt Control Register	0000030H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_ERRSR	Error Status Register	0000034H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CLRE	Clear Error Register	0000038H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_ECCR	DF0 ECC Read Register	0000040H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_ECCS	DF0 ECC Status Register	0000044H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_ECCC	DF0 ECC Control Register	0000048H	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_ECCW	DF0 ECC Write Register	000004CH	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_CCONTROL	Cranking Control Register	0000050H	U,SV	P,SV	System Reset	See Family Spec
DMU_HF_PSTATUS	Power Status Register	0000060H	U,SV	BE	Application Reset	See Family Spec

**Table 38 Register Overview - DMU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMU_HF_PCONT ROL	Power Control Register	0000064 <sub>H</sub>	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_PWAIT	PFLASH Wait Cycle Register	0000068 <sub>H</sub>	U,SV	P,SV,E	System Reset	See Family Spec
DMU_HF_DWAIT	DFLASH Wait Cycle Register	000006C <sub>H</sub>	U,SV	P,SV,E	System Reset	See Family Spec
DMU_HF_PROCO NUSR	DF0 User Mode Control	0000074 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NPF	PFLASH Protection Configuration	0000080 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NTP	Tuning Protection Configuration	0000084 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NDF	DFLASH Protection Configuration	0000088 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NRAM	RAM Configuration	000008C <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NDBG	Debug Interface Protection Configuration	0000090 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_SUSPE ND	Suspend Control Register	00000F0 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec
DMU_HF_MARGI N	Margin Control Register	00000F4 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec
DMU_HF_ACCEN 1	Access Enable Register 1	00000F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
DMU_HF_ACCEN 0	Access Enable Register 0	00000FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
DMU_HP_PROCO NPi0 (i=0-5)	PFLASH Bank i Protection Configuration 0	0010000 <sub>H+i*100H</sub>	U,SV	BE	See Family Spec	See Family Spec

**Table 38 Register Overview - DMU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMU_HP_PROCO_NPi1 (i=0-5)	PFLASH Bank i Protection Configuration 1	0010004 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NPi2 (i=0-5)	PFLASH Bank i Protection Configuration 2	0010008 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NPi3 (i=0-5)	PFLASH Bank i Protection Configuration 3	001000C <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NPi4 (i=0-5)	PFLASH Bank i Protection Configuration 4	0010010 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NPi5 (i=0-5)	PFLASH Bank i Protection Configuration 5	0010014 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NOTPi0 (i=0-5)	PFLASH Bank i OTP Protection Configuration 0	0010040 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NOTPi1 (i=0-5)	PFLASH Bank i OTP Protection Configuration 1	0010044 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NOTPi2 (i=0-5)	PFLASH Bank i OTP Protection Configuration 2	0010048 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NOTPi3 (i=0-5)	PFLASH Bank i OTP Protection Configuration 3	001004C <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NOTPi4 (i=0-5)	PFLASH Bank i OTP Protection Configuration 4	0010050 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NOTPi5 (i=0-5)	PFLASH Bank i OTP Protection Configuration 5	0010054 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NWOPi0 (i=0-5)	PFLASH Bank i WOP Configuration 0	0010080 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NWOPi1 (i=0-5)	PFLASH Bank i WOP Configuration 1	0010084 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NWOPi2 (i=0-5)	PFLASH Bank i WOP Configuration 2	0010088 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec

**Table 38 Register Overview - DMU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMU_HP_PROCO_NWOPi3 (i=0-5)	PFLASH Bank i WOP Configuration 3	001008C <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NWOPi4 (i=0-5)	PFLASH Bank i WOP Configuration 4	0010090 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO_NWOPi5 (i=0-5)	PFLASH Bank i WOP Configuration 5	0010094 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI_Oi0 (i=0-5)	PFLASH Bank i Erase Counter Priority configuration 0	00100A0 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI_Oi1 (i=0-5)	PFLASH Bank i Erase Counter Priority Configuration 1	00100A4 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI_Oi2 (i=0-5)	PFLASH Bank i Erase Counter Priority Configuration 2	00100A8 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI_Oi3 (i=0-5)	PFLASH Bank i Erase Counter Priority Configuration 3	00100AC <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI_Oi4 (i=0-5)	PFLASH Bank i Erase Counter Priority Configuration 4	00100B0 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI_Oi5 (i=0-5)	PFLASH Bank i Erase Counter Priority Configuration 5	00100B4 <sub>H</sub> +i*100 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
DMU_SF_STATUSES	HSM Flash Status Register	0020010 <sub>H</sub>	H	BE	Application Reset	See Family Spec
DMU_SF_CONTROL	HSM Flash Configuration Register	0020014 <sub>H</sub>	H	H	Application Reset	See Family Spec
DMU_SF_OPERATION	HSM Flash Operation Register	0020018 <sub>H</sub>	H	BE	System Reset	See Family Spec
DMU_SF_EER	HSM Enable Error Interrupt Control Register	0020030 <sub>H</sub>	H	H	Application Reset	See Family Spec
DMU_SF_ERRSR	HSM Error Status Register	0020034 <sub>H</sub>	H	BE	Application Reset	See Family Spec

**Table 38 Register Overview - DMU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMU_SF_CLRE	HSM Clear Error Register	0020038 H	H	H	Application Reset	See Family Spec
DMU_SF_ECCR	HSM DF1 ECC Read Register	0020040 H	H	BE	Application Reset	See Family Spec
DMU_SF_ECCS	HSM DF1 ECC Status Register	0020044 H	H	BE	Application Reset	See Family Spec
DMU_SF_ECCC	HSM DF1 ECC Control Register	0020048 H	H	H	Application Reset	See Family Spec
DMU_SF_ECCW	HSM DF1 ECC Write Register	002004C H	H	H	Application Reset	See Family Spec
DMU_SF_PROCO_NUSR	HSM DF1 User Mode Control	0020074 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SF_SUSPEND	HSM Suspend Control Register	00200E8 H	H	H	Application Reset	See Family Spec
DMU_SF_MARGIN	HSM DF1 Margin Control Register	00200EC H	H	H	Application Reset	See Family Spec
DMU_SP_PROCO_NHSMCFG	HSM Protection Configuration	0030000 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCO_NHSMCBS	HSM Code Boot Sector	0030004 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCO_NHSMCX0	HSM Code Exclusive Protection Configuration	0030008 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCO_NHSMCX1	HSM Code Exclusive Protection Configuration	003000C H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCO_NHSMCOTP0	HSM Code OTP Protection Configuration	0030010 H	U,SV	BE	See Family Spec	See Family Spec

**Table 38 Register Overview - DMU (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_SP_PROCO_NHSMCOTP1	HSM Code OTP Protection Configuration	0030014H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCO_NHSM	HSM Interface Protection Configuration	0030040H	U,SV	BE	See Family Spec	See Family Spec

### 6.3.2 TC39x-B Specific Registers

No deviations from the Family Spec.

### 6.3.3 Connectivity

**Table 39 Connections of DMU**

Interface Signals	connects		Description
DMU:irq_dmu_HOST_INT	to	INT:dmu.HOST_INT	PMU Host Service Request
DMU:irq_dmu_FSI_INT	to	INT:dmu.FSI_INT	PMU FSI Service Request

### 6.3.4 Revision History

**Table 40 Revision History**

Reference	Change to Previous Version	Comment
V2.0.9	No document changes - version update to remain aligned with family document.	
V2.0.10	No document changes - version update to remain aligned with family document.	
V2.0.11	No functional changes.	
V2.0.12	No functional changes.	

## 6.4 Non Volatile Memory (NVM)

This chapter supplements the family documentation with the device specific information for TC39xB.

### 6.4.1 TC39x-B Specific Register Set

#### Register Address Space Table

**Table 41 Register Address Space - FSI**

Module	Base Address	End Address	Note
FSI	F8030000 <sub>H</sub>	F80300FF <sub>H</sub>	sri slave interface

**Table 42 Register Address Space - PFI**

Module	Base Address	End Address	Note
(PFI0)	80000000 <sub>H</sub>	802FFFFF <sub>H</sub>	Program Flash cached address space
	A0000000 <sub>H</sub>	A02FFFFF <sub>H</sub>	Program Flash non-cached address space
	A8000000 <sub>H</sub>	A8003FFF <sub>H</sub>	Erase Counter address space
PFI0	A8080000 <sub>H</sub>	A80FFFFFF <sub>H</sub>	Register address space
(PFI1)	80300000 <sub>H</sub>	805FFFFFF <sub>H</sub>	Program Flash cached address space
	A0300000 <sub>H</sub>	A05FFFFFF <sub>H</sub>	Program Flash non-cached address space
	A8300000 <sub>H</sub>	A8303FFF <sub>H</sub>	Erase Counter address space
PFI1	A8380000 <sub>H</sub>	A83FFFFFF <sub>H</sub>	Register address space
(PFI2)	80600000 <sub>H</sub>	808FFFFFF <sub>H</sub>	Program Flash cached address space
	A0600000 <sub>H</sub>	A08FFFFFF <sub>H</sub>	Program Flash non-cached address space
	A8600000 <sub>H</sub>	A8603FFF <sub>H</sub>	Erase Counter address space
PFI2	A8680000 <sub>H</sub>	A86FFFFFF <sub>H</sub>	Register address space
(PFI3)	80900000 <sub>H</sub>	80BFFFFFF <sub>H</sub>	Program Flash cached address space
	A0900000 <sub>H</sub>	A0BFFFFFF <sub>H</sub>	Program Flash non-cached address space
	A8900000 <sub>H</sub>	A8903FFF <sub>H</sub>	Erase Counter address space
PFI3	A8980000 <sub>H</sub>	A89FFFFFF <sub>H</sub>	Register address space
(PFI4)	80C00000 <sub>H</sub>	80EFFFFFF <sub>H</sub>	Program Flash cached address space
	A0C00000 <sub>H</sub>	A0EFFFFFF <sub>H</sub>	Program Flash non-cached address space
	A8C00000 <sub>H</sub>	A8C03FFF <sub>H</sub>	Erase Counter address space
PFI4	A8C80000 <sub>H</sub>	A8CFFFFFF <sub>H</sub>	Register address space
(PFI5)	80F00000 <sub>H</sub>	80FFFFFFF <sub>H</sub>	Program Flash cached address space
	A0F00000 <sub>H</sub>	A0FFFFFFF <sub>H</sub>	Program Flash non-cached address space
	A8F00000 <sub>H</sub>	A8F03FFF <sub>H</sub>	Erase Counter address space
PFI5	A8F80000 <sub>H</sub>	A8FFFFFFF <sub>H</sub>	Register address space

#### Register Overview Table

**Table 43 Register Overview - FSI (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FSI_COMM_1	Communication Register 1	0004 <sub>H</sub>	U,SV	U,SV	System Reset	See Family Spec
FSI_COMM_2	Communication Register 2	0005 <sub>H</sub>	U,SV	U,SV	System Reset	See Family Spec
FSI_HSMCOMM_1	HSM Communication Register 1	0006 <sub>H</sub>	H	H	System Reset	See Family Spec
FSI_HSMCOMM_2	HSM Communication Register 2	0007 <sub>H</sub>	H	H	System Reset	See Family Spec

**Table 44 Register Overview - PFI (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
PFI0_ECCR	ECC Read Register	000000 <sub>H</sub>	See Family Spec
PFI1_ECCR	ECC Read Register	000000 <sub>H</sub>	See Family Spec
PFI2_ECCR	ECC Read Register	000000 <sub>H</sub>	See Family Spec
PFI3_ECCR	ECC Read Register	000000 <sub>H</sub>	See Family Spec
PFI4_ECCR	ECC Read Register	000000 <sub>H</sub>	See Family Spec
PFI5_ECCR	ECC Read Register	000000 <sub>H</sub>	See Family Spec
PFI0_ECCS	ECC Status Register	000020 <sub>H</sub>	See Family Spec
PFI1_ECCS	ECC Status Register	000020 <sub>H</sub>	See Family Spec

**Table 44 Register Overview - PFI (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
PFI2_ECCS	ECC Status Register	000020 <sub>H</sub>	See Family Spec
PFI3_ECCS	ECC Status Register	000020 <sub>H</sub>	See Family Spec
PFI4_ECCS	ECC Status Register	000020 <sub>H</sub>	See Family Spec
PFI5_ECCS	ECC Status Register	000020 <sub>H</sub>	See Family Spec
PFI0_SBABRECORDx (x=0-16)	SBAB Record x	002000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI1_SBABRECORDx (x=0-16)	SBAB Record x	002000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI2_SBABRECORDx (x=0-16)	SBAB Record x	002000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI3_SBABRECORDx (x=0-16)	SBAB Record x	002000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI4_SBABRECORDx (x=0-16)	SBAB Record x	002000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI5_SBABRECORDx (x=0-16)	SBAB Record x	002000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI0_DBABRECORDx (x=0-1)	DBAB Record x	004000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI1_DBABRECORDx (x=0-1)	DBAB Record x	004000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI2_DBABRECORDx (x=0-1)	DBAB Record x	004000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI3_DBABRECORDx (x=0-1)	DBAB Record x	004000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec

**Table 44 Register Overview - PFI (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
PFI4_DBABRECORDx (x=0-1)	DBAB Record x	004000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI5_DBABRECORDx (x=0-1)	DBAB Record x	004000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI0_MBABRECORDx (x=0)	MBAB Record 0	008000 <sub>H</sub>	See Family Spec
PFI1_MBABRECORDx (x=0)	MBAB Record 0	008000 <sub>H</sub>	See Family Spec
PFI2_MBABRECORDx (x=0)	MBAB Record 0	008000 <sub>H</sub>	See Family Spec
PFI3_MBABRECORDx (x=0)	MBAB Record 0	008000 <sub>H</sub>	See Family Spec
PFI4_MBABRECORDx (x=0)	MBAB Record 0	008000 <sub>H</sub>	See Family Spec
PFI5_MBABRECORDx (x=0)	MBAB Record 0	008000 <sub>H</sub>	See Family Spec
PFI0_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI1_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI2_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI3_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI4_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec
PFI5_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 <sub>H</sub> +x*20 <sub>H</sub>	See Family Spec

## 6.4.2 Connectivity

No connections in device.

## 6.4.3 Revision History

**Table 45 Revision History**

Reference	Change to Previous Version	Comment
V2.0.4	No document changes - version update to remain aligned with family document.	
V2.0.5	No document changes - version update to remain aligned with family document.	
V2.0.6	No functional changes.	

**Local Memory Unit (LMU)****7 Local Memory Unit (LMU)**

This is a description of the TC39x-B specific features of the LMU of the AURIX™ TC3XX product family.

**7.1 TC39x-B Specific IP Configuration**

Each of the LMU instances in the TC39x-B provides 256 KiB of SRAM.

**7.2 TC39x-B Specific Register Set****Table 46 Register Address Space - LMU**

<b>Module</b>	<b>Base Address</b>	<b>End Address</b>	<b>Note</b>
(LMU0)	90040000 <sub>H</sub>	9007FFFF <sub>H</sub>	sri slave interface (RAM Address Range cached)
	B0040000 <sub>H</sub>	B007FFFF <sub>H</sub>	sri slave interface (RAM Address Range non-cached)
LMU0	F8100000 <sub>H</sub>	F810FFFF <sub>H</sub>	sri slave interface
(LMU1)	90080000 <sub>H</sub>	900BFFFF <sub>H</sub>	sri slave interface (RAM Address Range cached)
	B0080000 <sub>H</sub>	B00BFFFF <sub>H</sub>	sri slave interface (RAM Address Range non-cached)
LMU1	F8110000 <sub>H</sub>	F811FFFF <sub>H</sub>	sri slave interface
(LMU2)	900C0000 <sub>H</sub>	900FFFFFF <sub>H</sub>	sri slave interface (RAM Address Range cached)
	B00C0000 <sub>H</sub>	B00FFFFFF <sub>H</sub>	sri slave interface (RAM Address Range non-cached)
LMU2	F8120000 <sub>H</sub>	F812FFFF <sub>H</sub>	sri slave interface

**Register Overview Tables of LMU****Table 47 Register Overview - LMU0 (ascending Offset Address)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
LMU0_CLC	LMU Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	See Family Spec
LMU0_MODID	LMU Module ID Register	00008 <sub>H</sub>	SV	BE	See Family Spec
LMU0_ACCENO	LMU Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	See Family Spec
LMU0_ACCEN1	LMU Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	See Family Spec
LMU0_MEMCON	LMU Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	See Family Spec
LMU0_SCTRL	LMU Safety Control Register	00024 <sub>H</sub>	SV	SV,SE,P	See Family Spec

**Local Memory Unit (LMU)****Table 47 Register Overview - LMU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
LMU0_RGNLAX <sub>(x=0-15)</sub>	LMU Region Lower Address Register	00050 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU0_RGNUAX <sub>(x=0-15)</sub>	LMU Region Upper Address Register	00054 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU0_RGNACC ENWAx (x=0-15)	LMU Region Write Access Enable Register A	00058 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU0_RGNACC ENWBx (x=0-15)	LMU Region Write Access Enable Register B	0005C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU0_RGNACC ENRAx (x=0-15)	LMU Region Read Access Enable Register A	00158 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU0_RGNACC ENRBx (x=0-15)	LMU Region Read Access Enable Register B	0015C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec

**Table 48 Register Overview - LMU1 (ascending Offset Address)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
LMU1_CLC	LMU Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	See Family Spec
LMU1_MODID	LMU Module ID Register	00008 <sub>H</sub>	SV	BE	See Family Spec
LMU1_ACCENO	LMU Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	See Family Spec
LMU1_ACCEN1	LMU Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	See Family Spec
LMU1_MEMCON	LMU Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	See Family Spec
LMU1_SCTRL	LMU Safety Control Register	00024 <sub>H</sub>	SV	SV,SE,P	See Family Spec

**Local Memory Unit (LMU)****Table 48 Register Overview - LMU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
LMU1_RGNLAX <sup>(x=0-15)</sup>	LMU Region Lower Address Register	00050 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU1_RGNUAX <sup>(x=0-15)</sup>	LMU Region Upper Address Register	00054 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU1_RGNACC ENWAx <sup>(x=0-15)</sup>	LMU Region Write Access Enable Register A	00058 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU1_RGNACC ENWBx <sup>(x=0-15)</sup>	LMU Region Write Access Enable Register B	0005C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU1_RGNACC ENRAx <sup>(x=0-15)</sup>	LMU Region Read Access Enable Register A	00158 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU1_RGNACC ENRBx <sup>(x=0-15)</sup>	LMU Region Read Access Enable Register B	0015C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec

**Table 49 Register Overview - LMU2 (ascending Offset Address)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
LMU2_CLC	LMU Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	See Family Spec
LMU2_MODID	LMU Module ID Register	00008 <sub>H</sub>	SV	BE	See Family Spec
LMU2_ACCEN0	LMU Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	See Family Spec
LMU2_ACCEN1	LMU Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	See Family Spec
LMU2_MEMCON	LMU Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	See Family Spec
LMU2_SCTRL	LMU Safety Control Register	00024 <sub>H</sub>	SV	SV,SE,P	See Family Spec

## Local Memory Unit (LMU)

**Table 49 Register Overview - LMU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
LMU2_RGNL <sub>A</sub> x (x=0-15)	LMU Region Lower Address Register	00050 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU2_RGNU <sub>A</sub> x (x=0-15)	LMU Region Upper Address Register	00054 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU2_RGNACC ENWA <sub>x</sub> (x=0-15)	LMU Region Write Access Enable Register A	00058 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU2_RGNACC ENWB <sub>x</sub> (x=0-15)	LMU Region Write Access Enable Register B	0005C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU2_RGNACC ENRA <sub>x</sub> (x=0-15)	LMU Region Read Access Enable Register A	00158 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec
LMU2_RGNACC ENRB <sub>x</sub> (x=0-15)	LMU Region Read Access Enable Register B	0015C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	See Family Spec

## 7.3 TC39x-B Specific Registers

There are no TC39x-B specific registers in the LMU

## 7.4 Connectivity

No connections in TC39x-B

## 7.5 Revision History

**Table 50 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
<b>V3.1.15</b>		
All	Revision history update, no functional changes.	
<b>V3.1.16</b>		
-	No functional change.	

## Default Application Memory (DAM)

# 8 Default Application Memory (DAM)

This appendix covers product specific information for the DAM module used in the AURIX™ TC3XX product family.

## 8.1 TC39x-B Specific IP Configuration

RAM size for the TC39x-B is 64 KiB per instance

## 8.2 TC39x-B Specific Register Set

**Table 51 Register Address Space - DAM**

Module	Base Address	End Address	Note
(DAM0)	90400000 <sub>H</sub>	9040FFFF <sub>H</sub>	DAM RAM Access cached address space
	B0400000 <sub>H</sub>	B040FFFF <sub>H</sub>	DAM RAM Access non-cached address space
DAM0	F8500000 <sub>H</sub>	F8507FFF <sub>H</sub>	Special Function Register Address Space
(DAM1)	90410000 <sub>H</sub>	9041FFFF <sub>H</sub>	DAM RAM Access cached address space
	B0410000 <sub>H</sub>	B041FFFF <sub>H</sub>	DAM RAM Access non-cached address space
DAM1	F8510000 <sub>H</sub>	F8517FFF <sub>H</sub>	Special Function Register Address Space

## Register Overview Tables of DAM

**Table 52 Register Overview - DAM0 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DAM0_CLC	DAM Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
DAM0_MODID	DAM Module ID Register	00008 <sub>H</sub>	SV	BE	Application Reset	See Family Spec
DAM0_ACCENO	DAM Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
DAM0_ACCEN1	DAM Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
DAM0_MEMCON	DAM Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
DAM0_RGNL <sub>A</sub> x (x=0-7)	DAM Region Lower Address Register	00050 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Default Application Memory (DAM)****Table 52 Register Overview - DAM0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DAM0_RGNUAx (x=0-7)	DAM Region Upper Address Register	00054 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM0_RGNACCE NWAx (x=0-7)	DAM Region Write Enable Register A	00058 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM0_RGNACCE NWBx (x=0-7)	DAM Region Write Enable Register B	0005C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM0_RGNACCE NRAx (x=0-7)	DAM Region Read Enable Register A	000D8 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM0_RGNACCE NRBx (x=0-7)	DAM Region Read Enable Register B	000DC <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Table 53 Register Overview - DAM1 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DAM1_CLC	DAM Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
DAM1_MODID	DAM Module ID Register	00008 <sub>H</sub>	SV	BE	Application Reset	See Family Spec
DAM1_ACCENO	DAM Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
DAM1_ACCEN1	DAM Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
DAM1_MEMCON	DAM Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
DAM1_RGNLAX (x=0-7)	DAM Region Lower Address Register	00050 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM1_RGNUAx (x=0-7)	DAM Region Upper Address Register	00054 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

## Default Application Memory (DAM)

**Table 53 Register Overview - DAM1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DAM1_RGNACCE_NWAx(x=0-7)	DAM Region Write Enable Register A	00058 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM1_RGNACCE_NWBx(x=0-7)	DAM Region Write Enable Register B	0005C <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM1_RGNACCE_NRAX(x=0-7)	DAM Region Read Enable Register A	000D8 <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
DAM1_RGNACCE_NRBx(x=0-7)	DAM Region Read Enable Register B	000DC <sub>H</sub> + x*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

## 8.3 TC39x-B Specific Registers

There are no device specific registers

## 8.4 Connectivity

**Table 54 Connections of DAM0**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
DAM0:LI0_INT	to	INT:damu0.LI0_INT	DAM0 Limit 0 Service Request
DAM0:RI0_INT	to	INT:damu0.RI0_INT	DAM0 Ready 0 Service Request
DAM0:LI1_INT	to	INT:damu0.LI1_INT	DAM0 Limit 1 Service Request
DAM0:RI1_INT	to	INT:damu0.RI1_INT	DAM0 Ready 1 Service Request
DAM0:DR_INT	to	INT:damu0.DR_INT	DAM0 DMA Ready Service Request
DAM0:ERR_INT	to	INT:damu0.ERR_INT	DAM0 Error Service Request

**Table 55 Connections of DAM1**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
DAM1:LI0_INT	to	INT:damu1.LI0_INT	DAM0 Limit 0 Service Request
DAM1:RI0_INT	to	INT:damu1.RI0_INT	DAM0 Ready 0 Service Request
DAM1:LI1_INT	to	INT:damu1.LI1_INT	DAM0 Limit 1 Service Request
DAM1:RI1_INT	to	INT:damu1.RI1_INT	DAM0 Ready 1 Service Request
DAM1:DR_INT	to	INT:damu1.DR_INT	DAM0 DMA Ready Service Request
DAM1:ERR_INT	to	INT:damu1.ERR_INT	DAM0 Error Service Request

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**Default Application Memory (DAM)**

## 8.5 Revision History

**Table 56 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.3.10</b>		
<a href="#">Page 3</a>	Connection tables update, no functional changes.	-
<a href="#">Page 4</a>	Revision history clean up.	-
<b>V1.3.11</b>		
-	Regeneration of document to align with new version of User Manual Chapter. No functional changes.	
<b>V1.3.12</b>		
-	No functional changes.	

## System Control Unit (SCU)

# 9 System Control Unit (SCU)

This chapter describes the System Control Unit (short SCU) Module of the TC39x-B.

## 9.1 TC39x-B Specific IP Configuration

**Table 57 TC39x-B specific configuration of SCU**

Parameter	SCU
<b>Number of WDT linked to the number of CPU</b>	6
<b>Name of the ssw value</b>	After SSW execution
<b>CFS value for DTSCBGOCTRL register</b>	40 <sub>H</sub>
<b>CFS value for DTSCCON register</b>	200 <sub>H</sub>

The following sections describe several differences that are device specific at the SCU level.

### 9.1.1 LBIST considerations for TC39x-B

The LBIST function can be controlled via four registers available at SCU level: LBISTCTRL0, LBISTCTRL1, LBISTCTRL2 and LBISTCTRL3 (for a complete description of these register, please address the family specification).

The LBISTCTRL3 register contains the MISR signature value that can be read back via software, after the LBIST execution (and the execution is valid).

#### 9.1.1.1 TC39x BA/BB/BC

##### LBIST Configuration A

LBISTCTRL0.PATTERNS = 0x80;

LBISTCTRL2.LENGTH = 0x86;

With LBISTCTRL1.BODY = 0:

- LBISTCTRL1 = 0x54000007
- LBISTCTRL3 = 0x01432DEB

With LBISTCTRL1.BODY = 1:

- LBISTCTRL1 = 0x5C000007
- LBISTCTRL3 = 0xF8097B38

#### 9.1.1.2 TC39x BD

##### LBIST Configuration A

LBISTCTRL0.PATTERNS = 0x80;

LBISTCTRL2.LENGTH = 0x86;

With LBISTCTRL1.BODY = 0:

- LBISTCTRL1 = 0x54000007
- LBISTCTRL3 = 0x95F1EC84

With LBISTCTRL1.BODY = 1:

- LBISTCTRL1 = 0x5C000007

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**System Control Unit (SCU)**

- LBISTCTRL3 = 0x6CBBBA57

**System Control Unit (SCU)****9.2 TC39x-B Specific Register Set**

The address space for the module registers is defined in [Register Address Space - SCU](#).

**Table 58 Register Address Space - SCU**

Module	Base Address	End Address	Note
SCU	F0036000 <sub>H</sub>	F00363FF <sub>H</sub>	SCU: Connections to FPI/BPI bus

**Table 59 Register Overview - SCU (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_ID	Reserved (0010 <sub>H</sub> Byte)	0000 <sub>H</sub>	BE	BE	System Reset	See Family Spec
	Identification Register	0008 <sub>H</sub>	U,SV	BE		
SCU_OSCCON	Reserved (0010 <sub>H</sub> Byte)	000C <sub>H</sub>	BE	BE	See Family Spec	See Family Spec
	OSC Control Register	0010 <sub>H</sub>	U,SV	SV,SE,P0		
SCU_SYSPLLSTA T	System PLL Status Register	0014 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
SCU_SYSPLLCON 0	System PLL Configuration 0 Register	0018 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_SYSPLLCON 1	System PLL Configuration 1 Register	001C <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_SYSPLLCON 2	System PLL Configuration 2 Register	0020 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_PERPLLSTA T	Peripheral PLL Status Register	0024 <sub>H</sub>	U,SV	BE	System Reset	See Family Spec
SCU_PERPLLCO N0	Peripheral PLL Configuration 0 Register	0028 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_PERPLLCO N1	Peripheral PLL Configuration 1 Register	002C <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCONO	CCU Clock Control Register 0	0030 <sub>H</sub>	U,SV	SV,SE,P0	See Family Spec	See Family Spec

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SCU_CCUCON1	CCU Clock Control Register 1	0034 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_FDR	Fractional Divider Register	0038 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_EXTCON	External Clock Control Register	003C <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON2	CCU Clock Control Register 2	0040 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON3	CCU Clock Control Register 3	0044 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON4	CCU Clock Control Register 4	0048 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON5	CCU Clock Control Register 5	004C <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_RSTSTAT	Reset Status Register	0050 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
	Reserved (0004 <sub>H</sub> Byte)	0054 <sub>H</sub>	BE	BE		
SCU_RSTCON	Reset Configuration Register	0058 <sub>H</sub>	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_ARSTDIS	Application Reset Disable Register	005C <sub>H</sub>	U,SV	SV,E,P0	PowerOn Reset	See Family Spec
SCU_SWRSTCON	Software Reset Configuration Register	0060 <sub>H</sub>	U,SV	SV,E,P0	See Family Spec	See Family Spec
SCU_RSTCON2	Additional Reset Control Register	0064 <sub>H</sub>	U,SV	SV,E,P0	See Family Spec	See Family Spec
SCU_RSTCON3	Reset Configuration Register 3	0068 <sub>H</sub>	U,SV	SV,E,P0	See Family Spec	See Family Spec
	Reserved (0004 <sub>H</sub> Byte)	006C <sub>H</sub>	BE	BE		

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SCU_ESRCFGx (x=0-1)	ESRx Input Configuration Register	0070 <sub>H</sub> +x *4	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_ESROCFG	ESR Output Configuration Register	0078 <sub>H</sub>	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_SYSCON	System Control Register	007C <sub>H</sub>	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_CCUCON6	CCU Clock Control Register 6	0080 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON7	CCU Clock Control Register 7	0084 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON8	CCU Clock Control Register 8	0088 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON9	CCU Clock Control Register 9	008C <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON10	CCU Clock Control Register 10	0090 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON11	CCU Clock Control Register 11	0094 <sub>H</sub>	U,SV	SV,SE,P0	System Reset	See Family Spec
	Reserved (0004 <sub>H</sub> Byte)	0098 <sub>H</sub>	BE	BE		
SCU_PDR	ESR Pad Driver Mode Register	009C <sub>H</sub>	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_IOCR	Input/Output Control Register	00A0 <sub>H</sub>	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_OUT	ESR Output Register	00A4 <sub>H</sub>	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_OMR	ESR Output Modification Register	00A8 <sub>H</sub>	U,SV	U,SV,P0	System Reset	See Family Spec

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SCU_IN	ESR Input Register	00AC <sub>H</sub>	U,SV	BE	System Reset	See Family Spec
	Reserved (0004 <sub>H</sub> Byte)	00BC <sub>H</sub>	BE	BE		
SCU_STSTAT	Start-up Status Register	00C0 <sub>H</sub>	U,SV	BE	PowerOn Reset	See Family Spec
SCU_STCON	Start-up Configuration Register	00C4 <sub>H</sub>	U,SV	ST,P0	Application Reset	See Family Spec
SCU_PMCSR0	Power Management Control and Status Register	00C8 <sub>H</sub>	U,SV	SE,CE0,SV, P0	Application Reset	See Family Spec
SCU_PMCSR1	Power Management Control and Status Register	00CC <sub>H</sub>	U,SV	SE,CE1,SV, P0	Application Reset	See Family Spec
SCU_PMCSR2	Power Management Control and Status Register	00D0 <sub>H</sub>	U,SV	SE,CE2,SV, P0	Application Reset	See Family Spec
SCU_PMCSR3	Power Management Control and Status Register	00D4 <sub>H</sub>	U,SV	SE,CE3,SV, P0	Application Reset	See Family Spec
SCU_PMCSR4	Power Management Control and Status Register	00D8 <sub>H</sub>	U,SV	SE,CE4,SV, P0	Application Reset	See Family Spec
SCU_PMCSR5	Power Management Control and Status Register	00DC <sub>H</sub>	U,SV	SE,CE5,SV, P0	Application Reset	See Family Spec
SCU_PMSTAT0	Power Management Status Register 0	00E4 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SCU_PMSWCR1	Standby and Wake-up Control Register 1	00E8 <sub>H</sub>	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
	Reserved (0020 <sub>H</sub> Byte)	00F0 <sub>H</sub>	BE	BE		
SCU_EMSR	Emergency Stop Register	00FC <sub>H</sub>	U,SV	SV,SE,P0	Application Reset	See Family Spec
SCU_EMSSW	Emergency Stop Software set and clear register	0100 <sub>H</sub>	U,SV	U,SV,P0	Application Reset	See Family Spec

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SCU_DTSCSTAT	Core Die Temperature Sensor Status Register	0104 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SCU_DTSCLIM	Core Die Temperature Sensor Limit Register	0108 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
	Reserved (0060 <sub>H</sub> Byte)	0114 <sub>H</sub>	BE	BE		
SCU_TRAPDIS1	Trap Disable Register 1	0120 <sub>H</sub>	U,SV	SV,E,P0	Application Reset	See Family Spec
SCU_TRAPSTAT	Trap Status Register	0124 <sub>H</sub>	U,SV	BE	System Reset	See Family Spec
SCU_TRAPSET	Trap Set Register	0128 <sub>H</sub>	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_TRAPCLR	Trap Clear Register	012C <sub>H</sub>	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_TRAPDIS0	Trap Disable Register 0	0130 <sub>H</sub>	U,SV	SV,E,P0	Application Reset	See Family Spec
SCU_LCLCON0	LCL CPU0 and CPU2 Control Register	0134 <sub>H</sub>	U,SV	SV,SE,ST,P0	See Family Spec	See Family Spec
SCU_LCLCON1	LCL CPU1 and CPU3 Control Register	0138 <sub>H</sub>	U,SV	SV,SE,ST,P0	See Family Spec	See Family Spec
SCU_LCLTEST	LCL Test Register	013C <sub>H</sub>	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_CHIPID	Chip Identification Register	0140 <sub>H</sub>	U,SV	ST,P0	See Family Spec	See Family Spec
SCU_MANID	Manufacturer Identification Register	0144 <sub>H</sub>	U,SV	BE	System Reset	See Family Spec
SCU_SWAPCTRL	Address Map Control Register	014C <sub>H</sub>	U,SV	ST,P0	System Reset	See Family Spec
	Reserved (0060 <sub>H</sub> Byte)	0158 <sub>H</sub>	BE	BE		
	Reserved (0060 <sub>H</sub> Byte)	015C <sub>H</sub>	BE	BE		

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
	Reserved (0060 <sub>H</sub> Byte)	0160 <sub>H</sub>	BE	BE		
SCU_LBISTCTRL0	Logic BIST Control 0 Register	0164 <sub>H</sub>	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_LBISTCTRL1	Logic BIST Control 1 Register	0168 <sub>H</sub>	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_LBISTCTRL2	Logic BIST Control 2 Register	016C <sub>H</sub>	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_LBISTCTRL3	Logic BIST Control 3 Register	0170 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
	Reserved (0020 <sub>H</sub> Byte)	0178 <sub>H</sub>	BE	BE		
SCU_STMEM1	Start-up Memory Register 1	0184 <sub>H</sub>	U,SV	ST,P0	PowerOn Reset	See Family Spec
SCU_STMEM2	Start-up Memory Register 2	0188 <sub>H</sub>	U,SV	ST,P0	System Reset	See Family Spec
SCU_PDISC	Pad Disable Control Register	018C <sub>H</sub>	U,SV	SV,E,P0	System Reset	See Family Spec
	Reserved (0020 <sub>H</sub> Byte)	0194 <sub>H</sub>	BE	BE		
SCU_PMTRCSR0	Power Management Transition Control and Status Register 0	0198 <sub>H</sub>	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR1	Power Management Transition Control and Status Register 1	019C <sub>H</sub>	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR2	Power Management Transition Control and Status Register 2	01A0 <sub>H</sub>	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR3	Power Management Transition Control and Status Register 3	01A4 <sub>H</sub>	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_STMEM3	Start-up Memory Register 3	01C0 <sub>H</sub>	U,SV	ST,P0	Application Reset	See Family Spec
SCU_STMEM4	Start-up Memory Register 4	01C4 <sub>H</sub>	U,SV	ST,P0	Cold PowerOn Reset	See Family Spec

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SCU_STMEM5	Start-up Memory Register 5	01C8 <sub>H</sub>	U,SV	ST,P0	PowerOn Reset	See Family Spec
SCU_STMEM6	Start-up Memory Register 6	01CC <sub>H</sub>	U,SV	ST,P0	System Reset	See Family Spec
SCU_OVCENABLE	Overlay Enable Register	01E0 <sub>H</sub>	U,SV	SV,SE,P0	Application Reset	See Family Spec
SCU_OVCCON	Overlay Control Register	01E4 <sub>H</sub>	U,SV	SV,P0	Application Reset	See Family Spec
SCU_EIFILT	External Input Filter Register	020C <sub>H</sub>	U,SV	SE,SV,P0	Application Reset	See Family Spec
SCU_EICR <sub>i</sub> (i=0-3)	External Input Channel Register i	0210 <sub>H</sub> +i*4	U,SV	SE,SV,P0	Application Reset	See Family Spec
SCU_EIFR	External Input Flag Register	0220 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SCU_FMR	Flag Modification Register	0224 <sub>H</sub>	U,SV	U,SV,P0	Application Reset	See Family Spec
SCU_PDERR	Pattern Detection Result Register	0228 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SCU_IGCR <sub>j</sub> (j=0-3)	Flag Gating Register j	022C <sub>H</sub> +j*4	U,SV	SE,SV,P0	Application Reset	See Family Spec
	Reserved (0030 <sub>H</sub> Byte)	023C <sub>H</sub>	BE	BE		
SCU_WDTCPUyCON0 (y=0) (y=1) (y=2) (y=3) (y=4) (y=5)	CPUy WDT Control Register 0	024C <sub>H</sub> +y*12	U,SV	U,SV,32,CP Uy (y=CPU number)	Application Reset	See Family Spec

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SCU_WDTCPUyC ON1 (y=0) (y=1) (y=2) (y=3) (y=4) (y=5)	CPUy WDT Control Register 1	0250 <sub>H</sub> +y *12	U,SV	SV,CEy,P0	Application Reset	See Family Spec
SCU_WDTCPUyS R (y=0) (y=1) (y=2) (y=3) (y=4) (y=5)	CPUy WDT Status Register	0254 <sub>H</sub> +y *12	U,SV	BE	Application Reset	See Family Spec
SCU_EICON0	ENDINIT Global Control Register 0	029C <sub>H</sub>	U,SV	U,SV,32,P0	Application Reset	See Family Spec
SCU_EICON1	ENDINIT Global Control Register 1	02A0 <sub>H</sub>	U,SV	SV,E,P0	Application Reset	See Family Spec
SCU_EISR	ENDINIT Timeout Counter Status Register	02A4 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SCU_WDTSCON0	Safety WDT Control Register 0	02A8 <sub>H</sub>	U,SV	U,SV,32,P1	Application Reset	See Family Spec
SCU_WDTSCON1	Safety WDT Control Register 1	02AC <sub>H</sub>	U,SV	SV,SE,P1	Application Reset	See Family Spec
SCU_WDTSSR	Safety WDT Status Register	02B0 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SCU_SEICON0	Safety ENDINIT Control Register 0	02B4 <sub>H</sub>	U,SV	U,SV,32,P1	Application Reset	See Family Spec
SCU_SEICON1	Safety ENDINIT Control Register 1	02B8 <sub>H</sub>	U,SV	SV,SE,P1	Application Reset	See Family Spec
SCU_SEISR	Safety ENDINIT Timeout Status Register	02BC <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec

**System Control Unit (SCU)****Table 59 Register Overview - SCU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
	Reserved (0440 <sub>H</sub> Byte)	02DC <sub>H</sub>	BE	BE		
SCU_ACCEN11	Access Enable Register 11	03F0 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN10	Access Enable Register 10	03F4 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN01	Access Enable Register 01	03F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN00	Access Enable Register 00	03FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
	Reserved (0440 <sub>H</sub> Byte)	0400 <sub>H</sub>	BE	BE		

**9.3 TC39x-B Specific Registers**

No deviations from the Family Spec

**9.4 Connectivity****Table 60 Connections of SCU**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
SCU:CBS_ENDINIT_DIS	from	CBS:ocds_oc(3)	Watchdog ENDINIT disable from Cerberus
SCU:CBS_WDT_SUSP	from	CBS:ocds_wdtsus	Watchdog suspend from Cerberus
SCU:EMGSTOP_PORT_A	from	SMU:FSPSCU	Emergency stop Port Pin A input request
SCU:EMGSTOP_PORT_B	from	P21.2:IN	Emergency stop Port Pin B input request
SCU:ESR0_PORT_IN	from	TC39x-B:ESR0	ESR0 Port Pin input - can be used to trigger a reset or an NMI
SCU:ESR1_PORT_IN	from	TC39x-B:ESR1	ESR1 Port Pin input - can be used to trigger a reset or an NMI
SCU:E_IOUT(0)	to	RIF0:RAMP1C EVADC:G0REQTRH EVADC:G8REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(1)	to	RIF1:RAMP1C EVADC:G1REQTRH EVADC:G9REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(2)	to	EVADC:G2REQTRH EVADC:G10REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)

**System Control Unit (SCU)****Table 60 Connections of SCU (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
SCU:E_IOUT(3:2)	to	CAN0:ECTT(4:3)	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(3)	to	EVADC:G3REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
		EVADC:G11REQTRH	
SCU:E_IOUT(4)	to	CAN0:TTCPT_TRIG(4)	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
		EVADC:G4REQTRH	
SCU:E_IOUT(5)	to	EVADC:G5REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(6)	to	EVADC:G6REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(7)	to	EVADC:G7REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_PDOUT(0)	to	CCU60:CTRAPPD	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		CCU60:T12HRH	
		EDSADC:ITR0G	
		EDSADC:ITR8G	
		EVADC:G0REQGTM	
		EVADC:G8REQGTM	
		GTM:TIM0_IN0(12)	
SCU:E_PDOUT(1)	to	CCU61:CTRAPPD	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		CCU61:T12HRH	
		EDSADC:ITR1G	
		EDSADC:ITR9G	
		EVADC:G1REQGTM	
		EVADC:G9REQGTM	
		GTM:TIM0_IN1(12)	
SCU:E_PDOUT(2)	to	EDSADC:ITR2G	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EDSADC:ITR10G	
		EVADC:G2REQGTM	
		EVADC:G10REQGTM	
		GTM:TIM0_IN2(12)	
SCU:E_PDOUT(3:0)	to	ERAY0:STPWT(3:0)	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
SCU:E_PDOUT(3:0)	to	ERAY1:STPWT(3:0)	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)

**System Control Unit (SCU)****Table 60 Connections of SCU (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
SCU:E_PDOUT(3)	to	EDSADC:ITR3G	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EDSADC:ITR11G	
		EVADC:G3REQGTM	
		EVADC:G11REQGTM	
		GTM:TIM0_IN3(12)	
SCU:E_PDOUT(4)	to	CCU60:CC62IND	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EDSADC:ITR4G	
		EDSADC:ITR12G	
		EVADC:G4REQGTM	
		GPT120:T3INC	
		GTM:TIM0_IN4(12)	
SCU:E_PDOUT(5)	to	CCU61:CC62IND	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EDSADC:ITR5G	
		EDSADC:ITR13G	
		EVADC:G5REQGTM	
		GTM:TIM0_IN5(12)	
SCU:E_PDOUT(6)	to	EDSADC:ITR6G	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EVADC:G6REQGTM	
		GPT120:CAPINB	
		GTM:TIM0_IN6(12)	
SCU:E_PDOUT(7)	to	EDSADC:ITR7G	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EVADC:G7REQGTM	
		GTM:TIM0_IN7(12)	
SCU:E_REQ0(0)	from	P15.4:IN	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(1)	from	CCU60:COUT60	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(2)	from	P10.7:IN	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(3)	from	MSC0:FCLP	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(4)	from	STM5:STMIR(0)	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(0)	from	P14.3:IN	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(1)	from	CCU61:COUT60	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(2)	from	P10.8:IN	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.

**System Control Unit (SCU)****Table 60 Connections of SCU (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
SCU:E_REQ1(3)	from	STM0:STMIR(0)	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(0)	from	P10.2:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(1)	from	P02.1:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(2)	from	P00.4:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(3)	from	ERAY0:MT	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(0)	from	P10.3:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(1)	from	P14.1:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(2)	from	P02.0:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(3)	from	STM1:STMIR(0)	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(0)	from	P33.7:IN	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(1)	from	GTM:SCU_TRIG(0)	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(2)	from	GPT120:T3OUT	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(3)	from	P15.5:IN	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(0)	from	P15.8:IN	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(1)	from	GTM:SCU_TRIG(1)	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(2)	from	GPT120:T6OUT	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(3)	from	STM2:STMIR(0)	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(0)	from	P20.0:IN	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(1)	from	TC39x-B:ESR0	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(3)	from	P11.10:IN	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(4)	from	STM3:STMIR(0)	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.

## System Control Unit (SCU)

**Table 60 Connections of SCU (cont'd)**

Interface Signals	connects	Description
SCU:E_REQ6(5)	from GTM:SCU_TRIG(2)	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(0)	from P20.9:IN	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(1)	from TC39x-B:ESR1	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(2)	from P15.1:IN	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(3)	from ERAY1:MT	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(4)	from STM4:STMIR(0)	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(5)	from GTM:SCU_TRIG(3)	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:RST_REQ_STM(10)	from HSM:SYSRST	Reset request from STMn (MSB is STM5 and LSB is STM0)
SCU:RST_REQ_STM(11)	from HSM:APPRST	Reset request from STMn (MSB is STM5 and LSB is STM0)
SCU:SMU_EMGSTP_REQ	from SMU:EMERGENCYSTOPR_EQ	Emergency stop request from SMU
SCU:SMU_TRAP_REQ	from SMU:NMIREQ	TRAP request from the SMU
SCU:TRAP_CPU(0)	to cpu_pfi_pfrwb_0:tc162p_nmi_trap	TRAP output to CPU <sub>n</sub> (MSB is CPU5 and LSB is CPU0)
SCU:TRAP_CPU(1)	to cpu_pfi_pfrwb_1:tc162p_nmi_trap	TRAP output to CPU <sub>n</sub> (MSB is CPU5 and LSB is CPU0)
SCU:TRAP_CPU(2)	to cpu_pfi_pfrwb_2:tc162p_nmi_trap	TRAP output to CPU <sub>n</sub> (MSB is CPU5 and LSB is CPU0)
SCU:TRAP_CPU(3)	to cpu_pfi_pfrwb_3:tc162p_nmi_trap	TRAP output to CPU <sub>n</sub> (MSB is CPU5 and LSB is CPU0)
SCU:TRAP_CPU(4)	to cpu_pfi_pfrwb_4:tc162p_nmi_trap	TRAP output to CPU <sub>n</sub> (MSB is CPU5 and LSB is CPU0)
SCU:TRAP_CPU(5)	to cpu_pfi_pfrwb_5:tc162p_nmi_trap	TRAP output to CPU <sub>n</sub> (MSB is CPU5 and LSB is CPU0)
SCU:ERU_INT(3:0)	to INT:scu.ERU_INT(3:0)	SCU ERU Service Request x

## 9.5 Revision History

The following table contains the revision history of the SCU that is relevant for the TC39x-B device. For a complete revision history please address the family user manual.

This section only includes entries, respective to the Clock System, that are related to register updates. For a complete Clock System revision history please address the family user manual.

**System Control Unit (SCU)****Table 61 Revision History**

Reference	Change to Previous Version	Comment
<b>V2.1.21</b>		
	Revision History entries up to V2.1.20 removed.	
<a href="#">Page 3</a>	Note referring to TESTMODE pin has been removed from documentation.	
<a href="#">Page 11</a>	Connectivity information updated.	
<b>V2.1.22</b>		
	Revision History entries up to V2.1.22 removed.	
	No functional changes.	
<b>V2.1.23</b>		
	Revision History entries up to V2.1.21 removed.	
<a href="#">Page 11</a>	Connectivity table updated due to update of Connexion DB.	
<a href="#">Page 1</a>	LBISTCTRL register configuration corrected.	
<b>V2.1.24</b>		
	No functional changes.	
<b>V2.1.25</b>		
	No functional changes.	
<b>V2.1.26</b>		
	No functional changes.	
<b>V2.1.27</b>		
	No functional changes.	

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## Clocking System

### 10 Clocking System

Device specific information about the clocking system is contained in the SCU chapter as both modules share a common bus interface.

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**Power Management System (PMS)**

## 11 Power Management System (PMS)

This chapter describes the Power Management System (PMS) Module of the TC39x-B.

### 11.1 TC39x-B Specific IP Configuration

**Table 62 TC39x-B specific configuration of PMS**

Parameter	PMS
CFS value for the PMSWCR4 register	02000020 <sub>H</sub>

**Power Management System (PMS)****11.2 TC39x-B Specific Register Set**

The PMS related SCU registers are specified in the SCU section of this appendix.

**Table 63 Register Address Space - PMS**

<b>Module</b>	<b>Base Address</b>	<b>End Address</b>	<b>Note</b>
(PMS)	F0240000 <sub>H</sub>	F0241FFF <sub>H</sub>	
PMS	F0248000 <sub>H</sub>	F02481FF <sub>H</sub>	FPI slave interface

**Table 64 Register Overview - PMS (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
PMS_ID	Identification Register	0008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
PMS_EVRSTAT	EVR Status Register	002C <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRADCSTA T	EVR Primary ADC Status Register	0034 <sub>H</sub>	U,SV	BE	LVD Reset	See Family Spec
PMS_EVRRSTCO N	EVR Reset Control Register	003C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRRSTSTA T	EVR Reset Status Register	0044 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRTRIM	EVR Trim Control Register	004C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRTRIMSTA T	EVR Trim Status Register	0050 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONSTA T1	EVR Secondary ADC Status Register 1	0060 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONSTA T2	EVR Secondary ADC Status Register 2	0064 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONCTR L	EVR Secondary Monitor Control Register	0068 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRMONFILT	EVR Secondary Monitor Filter Register	0070 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec

**Power Management System (PMS)****Table 64 Register Overview - PMS (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
PMS_PMSIEN	PMS Interrupt Enable Register	0074 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRUVMON	EVR Secondary Under-voltage Monitor Register	0078 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROVMON	EVR Secondary Over-voltage Monitor Register	007C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRUVMON2	EVR Secondary Under-voltage Monitor Register 2	0080 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROVMON2	EVR Secondary Over-voltage Monitor Register 2	0084 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_HSMUVMON	EVR Primary HSM Under-voltage Monitor Register	0088 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_HSMOVMON	EVR Primary HSM Over-voltage Monitor Register	008C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVR33CON	EVR33 Control Register	0090 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROSCCTRLL	EVR Oscillator Control Register	00A0 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_PMSWCR0	Standby and Wake-up Control Register 0	00B4 <sub>H</sub>	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR2	Standby and Wake-up Control Register 2	00B8 <sub>H</sub>	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR3	Standby and Wake-up Control Register 3	00C0 <sub>H</sub>	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR4	Standby and Wake-up Control Register 4	00C4 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_PMSWCR5	Standby and Wake-up Control Register 5	00C8 <sub>H</sub>	U,SV	SV,SE,P	LVD Reset	See Family Spec

## Power Management System (PMS)

**Table 64 Register Overview - PMS (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
PMS_PMSWSTAT	Standby and Wake-up Status Register	00D4 <sub>H</sub>	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWSTAT2	Standby and Wake-up Status Register 2	00D8 <sub>H</sub>	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWUTCNT	Standby WUT Counter Register	00DC <sub>H</sub>	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWSTATCLR	Standby and Wake-up Status Clear Register	00E8 <sub>H</sub>	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_EVRSDSTAT0	EVR SD Status Register 0	00FC <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRSDCTRL0	EVRC SD Control Register 0	0108 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL1	EVRC SD Control Register 1	010C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL2	EVRC SD Control Register 2	0110 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL3	EVRC SD Control Register 3	0114 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL4	EVRC SD Control Register 4	0118 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL5	EVRC SD Control Register 5	011C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL6	EVRC SD Control Register 6	0120 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL7	EVRC SD Control Register 7	0124 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL8	EVRC SD Control Register 8	0128 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec

**Power Management System (PMS)****Table 64 Register Overview - PMS (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
PMS_EVRSDCTRL 9	EVRC SD Control Register 9	012C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 10	EVRC SD Control Register 10	0130 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 11	EVRC SD Control Register 11	0134 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF0	EVRC SD Coefficient Register 0	0148 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF1	EVRC SD Coefficient Register 1	014C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF2	EVRC SD Coefficient Register 2	0150 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF3	EVRC SD Coefficient Register 3	0154 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF4	EVRC SD Coefficient Register 4	0158 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF5	EVRC SD Coefficient Register 5	015C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF6	EVRC SD Coefficient Register 6	0160 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF7	EVRC SD Coefficient Register 7	0164 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF8	EVRC SD Coefficient Register 8	0168 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF9	EVRC SD Coefficient Register 9	016C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_AG2i_STDB Y (i=0-1)	Alarm Status Register	0188 <sub>H</sub> +i* 4	U,SV	SV,SE,P	LVD Reset	See Family Spec

## Power Management System (PMS)

**Table 64 Register Overview - PMS (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
PMS_MONBISTS_TAT	SMU_stdby BIST Status Register	0190 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_MONBISTC_TRL	SMU_stdby BIST Control Register	0198 <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_CMD_STDB_Y	SMU_stdby Command Register	019C <sub>H</sub>	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_AG2iFSP_STDBY(i=0-1)	SMU_stdby FSP Configuration Register	01A4 <sub>H</sub> +i*4	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_DTSSTAT	Die Temperature Sensor Status Register	01C0 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
PMS_DTSLIM	Die Temperature Sensor Limit Register	01C8 <sub>H</sub>	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSS	OCDS Trigger Set Select Register	01E0 <sub>H</sub>	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSC0	OCDS Trigger Set Control 0 Register	01E4 <sub>H</sub>	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSC1	OCDS Trigger Set Control 1 Register	01E8 <sub>H</sub>	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_ACCEN1	Access Enable Register 1	01F8 <sub>H</sub>	U,SV	SV,SE,32	Application Reset	See Family Spec
PMS_ACCEN0	Access Enable Register 0	01FC <sub>H</sub>	U,SV	SV,SE,32	Application Reset	See Family Spec

### 11.3 TC39x-B Specific Registers

No deviations from the Family Spec

## Power Management System (PMS)

### 11.4 Connectivity

**Table 65 Connections of PMS**

Interface Signals	connects		Description
PMS:DCDCSYNCO	to	P32.4:HWOUT(0)	DC-DC synchronization output
		P32.2:ALT(6)	
		P32.4:ALT(2)	
PMS:ESR0PORST	to	TC39x-B:ESR0	ESR0 control output during PORST activation
PMS:ESR0WKP	from	TC39x-B:ESR0	ESR0 pin input
PMS:ESR1WKP	from	TC39x-B:ESR1	ESR1 pin input
PMS:HWCFG1IN	from	TC39x-B:P14.5	HWCFG1 pin input
PMS:HWCFG2IN	from	TC39x-B:P14.2	HWCFG2 pin input
PMS:HWCFG4IN	from	TC39x-B:P10.5	HWCFG4 pin input
PMS:HWCFG5IN	from	TC39x-B:P10.6	HWCFG5 pin input
PMS:HWCFG6IN	from	TC39x-B:P14.4	HWCFG6 pin input
PMS:PINAWKP	from	TC39x-B:P14.1	PINA (P14.1) pin input
PMS:PINBWKP	from	TC39x-B:P33.12	PINB (P33.12) pin input
PMS:PORSTIN	from	TC39x-B:PORST	PORST pin input
PMS:PORSTOUT	to	TC39x-B:PORST	PORST pin output
PMS:TESTMODEIN	from	TC39x-B:P20.2	TESTMODE pin input
PMS:VDDMLVL	to	converter_0:converter_low_supp	VDDM monitor signal to Converter
PMS:VGATE1N	to	TC39x-B:CTRL1V3N	DCDC N ch. MOSFET gate driver output
		TC39x-B:CTRL1V3N	
PMS:VGATE1P	to	TC39x-B:CTRL1V3P	DCDC P ch. MOSFET gate driver output
		TC39x-B:CTRL1V3P	

### 11.5 Revision History

**Table 66 Revision History**

Reference	Change to Previous Version	Comment
V2.2.28	No changes.	
V2.2.29	- No functional changes.	
V2.2.30	<b>Page 2</b> Register “PMS_EVR33CON” now visible to the customer.	
V2.2.31	- No functional changes.	
V2.2.32	- No functional changes.	

**Power Management System (PMS)****Table 66 Revision History (cont'd)**

Reference	Change to Previous Version	Comment
<b>V2.2.33</b>		
-	No functional changes.	
<b>V2.2.34</b>		
-	No functional changes.	

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**Power Management System for Low-End (PMSLE)****12 Power Management System for Low-End (PMSLE)**

This device doesn't contain a PMSLE module.

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## Memory Test Unit (MTU)

### 13 Memory Test Unit (MTU)

For the generic description of the Memory Test Unit (MTU) and the SRAM Support Hardware (SSH), please refer to the platform chapter.

#### 13.1 TC39x-B Specific IP Configuration

There is no device specific IP configuration. MTU+SSH is generic across all derivates in the platforms. Only the SSH instances vary.

##### 13.1.1 Handling of Large DSPR SRAMs

On this device, the CPU0 and CPU1 have large DSPR SRAMs. Therefore, there are two SSHs to support these SRAMs. These are named as CPUxDMEM and CPUxDMEM1 (x=0,1).

Logically, these 2 SSHs behave as separate SSHs, with their own MEMTEST\_EN bits, Alarms to the SMU, error status flags etc. However special handling is required to enter test mode for these SSHs.

When running a Non-Destructive-test, only one of the DMEM SSHs shall be enabled at a time. This is because the ECC encoder and decoder are shared between the two SSHs.

However, as long as destructive tests or SSH register accesses are to be performed, then both SSHs can be enabled together.

Please note that when one of the DMEM SSH is enabled, the complete DSPR+DCACHE is unavailable for functional access. This is due to internal interleaving of the logical address space.

Although the DCACHE is also split equally between the two SRAMs, the entire cache has to be mapped at once to the system address map. Hence only a single bit is provided in the MTU\_MEMMAP register for the entire DMEM.

The partial-erase (i.e. erasing the Cache area; refer the family spec) is triggered separately when each MEMTEST\_EN bit is set.

The MEMMAP bit triggers the partial erase in both SSHs at the same time.

If both the SSHs are enabled / disabled at the same time, the software should check either the bits in the MTU\_MEMSTAT register, or ensure that the EN bits for both the SSHs are set / cleared in the MEMTEST registers to ensure that the partial-erase has completed.

##### 13.1.2 SRAMs with Address ECC

On this device, in the EMEM0-3 SRAMs, the ECC is calculated over the data as well as the address. This means, that for the same data word at different addresses, the corresponding ECC value will be different.

For these SRAMs/SSHs, initializing the SRAM with ECC correct data using MCONTROL.DINIT is not supported. The SRAMs can be still completely initialized via the MCONTROL.SRAM\_CLR bit (Refer platform specification chapter on Filling a Memory with Defined Contents).

**Memory Test Unit (MTU)****13.2 TC39x-B Specific Register Set****Register Address Space Table****Table 67 Register Address Space - MTU**

Module	Base Address	End Address	Note
MTU	F0060000 <sub>H</sub>	F006FFFF <sub>H</sub>	FPI slave interface

**Register Overview Table****Table 68 Register Overview - MTU (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
MTU_CLC	Clock Control Register	0000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
MTU_ID	Identification Register	0008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
MTU_MEMTESTi (i=0-2)	Memory MBIST Enable Register i	0010 <sub>H</sub> +i*4	U,SV	SV,SE,P	Application Reset	<a href="#">3</a>
MTU_MEMMAP	Memory Mapping Enable Register	001C <sub>H</sub>	U,SV	SV,SE,P	Application Reset	<a href="#">12</a>
MTU_MEMSTATi (i=0-2)	Memory Status Register i	0038 <sub>H</sub> +i*4	U,SV	BE	Application Reset	<a href="#">16</a>
MTU_MEMDONEi (i=0-2)	Memory Test Done Status Register i	0050 <sub>H</sub> +i*4	U,SV	BE	Application Reset	<a href="#">21</a>
MTU_MEMFDAi (i=0-2)	Memory Test FDA Status Register i	0060 <sub>H</sub> +i*4	U,SV	BE	Application Reset	<a href="#">29</a>
MTU_ACCEN1	Access Enable Register 1	00F8 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
MTU_ACCENO	Access Enable Register 0	00FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
MTU_MCI_CONFi G0 (i=0-95)	Configuration Registers	1000 <sub>H</sub> +i*100 <sub>H</sub>	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCI_CONFi G1 (i=0-95)	Configuration Register 1	1002 <sub>H</sub> +i*100 <sub>H</sub>	U,SV,16	U,SV,P,16	Application Reset	See Family Spec

**Memory Test Unit (MTU)****Table 68 Register Overview - MTU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
MTU_MCi_MCON TROL (i=0-95)	MBIST Control Register	$1004_H+i^*$ $100_H$	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_MSTA TUS (i=0-95)	Status Register	$1006_H+i^*$ $100_H$	U,SV,16	BE	Application Reset	See Family Spec
MTU_MCi_RANG E (i=0-95)	Range Register, single address mode	$1008_H+i^*$ $100_H$	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_REVID (i=0-95)	Revision ID Register	$100C_H+i^*$ $100_H$	U,SV,16	BE	Application Reset	See Family Spec
MTU_MCi_ECCS (i=0-95)	ECC Safety Register	$100E_H+i^*$ $100_H$	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_ECCD (i=0-95)	Memory ECC Detection Register	$1010_H+i^*$ $100_H$	U,SV,16	SV,P,16	See Family Spec	See Family Spec
MTU_MCi_ETRRx (i=0-95;x=0-4)	Error Tracking Register x	$1012_H+i^*$ $100_H+x^*$ 2	U,SV,16	BE	PowerOn Reset	See Family Spec
MTU_MCi_RDBFL y (i=0-95;y=0-66)	Read Data and Bit Flip Register y	$1060_H+i^*$ $100_H+y^*$ 2	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_ALMS RCS (i=0-95)	Alarm Sources Configuration Register	$10EE_H+i^*$ $100_H$	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_FAULT STS (i=0-95)	SSH Safety Faults Status Register	$10F0_H+i^*$ $100_H$	U,SV,16	SV,SE,P,16	PowerOn Reset	See Family Spec
MTU_MCi_ERRIN FOx (i=0-95;x=0-4)	Error Information Register x	$10F2_H+i^*$ $100_H+x^*$ 2	U,SV,16	BE	PowerOn Reset	See Family Spec

**13.3 TC39x-B Specific Registers****13.3.1 MEMTEST Implementation****Memory MBIST Enable Register i**

The memory test register MEMTEST holds CPU configurable select bits for the various SSH instances. See the product specific appendix for mapping of memory controller numbers.

## Memory Test Unit (MTU)

MTU\_MEMTESTi (i=0)

Memory MBIST Enable Register i

(0010<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LMU1_0_EN	LMU0_0_EN	CPU5_DLMU_EN	CPU5_PTAG_EN	CPU5_PMEM_EN	CPU5_DTAG_EN	CPU5_DMEM_EN	CPU4_DLMU_EN	CPU4_PTAG_EN	CPU4_PMEM_EN	CPU4_DTAG_EN	CPU4_DMEM_EN	CPU3_DLMU_EN	CPU3_PTAG_EN	CPU3_PMEM_EN	CPU3_DTAG_EN
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU3_DMEM_EN	CPU2_DLMU_EN	CPU2_PTAG_EN	CPU2_PMEM_EN	CPU2_DTAG_EN	CPU2_DMEM_EN	CPU1_DLMU_STBY_EN	CPU1_PTAG_EN	CPU1_PMEM_EN	CPU1_DTAG_EN	CPU1_DMEM_EN	CPU0_DLMU_STBY_EN	CPU0_PTAG_EN	CPU0_PMEM_EN	CPU0_DTAG_EN	CPU0_DMEM_EN
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CPU0_DMEM_EN	0	rwh	<b>CPU0 DMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU0_DTAG_EN	1	rwh	<b>CPU0 DTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU0_PMEM_EN	2	rwh	<b>CPU0 PMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU0_PTAG_EN	3	rwh	<b>CPU0 PTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU0_DLMU_STBY_EN	4	rwh	<b>CPU0 STANDBY DLMU SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU1_DMEM_EN	5	rwh	<b>CPU1 DMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU1_DTAG_EN	6	rwh	<b>CPU1 DTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU1_PMEM_EN	7	rwh	<b>CPU1 PMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU1_PTAG_EN	8	rwh	<b>CPU1 PTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU1_DLMU_STBY_EN	9	rwh	<b>CPU1 STANDBY DLMU SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU2_DMEM_EN</b>	10	rwh	<b>CPU2 DMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU2_DTAG_EN</b>	11	rwh	<b>CPU2 DTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU2_PMEM_EN</b>	12	rwh	<b>CPU2 PMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU2_PTAG_EN</b>	13	rwh	<b>CPU2 PTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU2_DLMU_EN</b>	14	rwh	<b>CPU2 DLMU memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU3_DMEM_EN</b>	15	rwh	<b>CPU3 DMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU3_DTAG_EN</b>	16	rwh	<b>CPU3 DTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU3_PMEM_EN</b>	17	rwh	<b>CPU3 PMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU3_PTAG_EN</b>	18	rwh	<b>CPU3 PTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU3_DLMU_EN</b>	19	rwh	<b>CPU3 DLMU memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU4_DMEM_EN</b>	20	rwh	<b>CPU4 DMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU4_DTAG_EN</b>	21	rwh	<b>CPU4 DTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU4_PMEM_EN</b>	22	rwh	<b>CPU4 PMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU4_PTAG_EN</b>	23	rwh	<b>CPU4 PTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>CPU4_DLMU_EN</b>	24	rwh	<b>CPU4 DLMU memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled

**Memory Test Unit (MTU)**

Field	Bits	Type	Description
CPU5_DMEM_EN	25	rwh	<b>CPU5 DMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU5_DTAG_EN	26	rwh	<b>CPU5 DTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU5_PMEM_EN	27	rwh	<b>CPU5 PMEM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU5_PTAG_EN	28	rwh	<b>CPU5 PTAG SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
CPU5_DLNU_EN	29	rwh	<b>CPU5 DLNU memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
LMU00_EN	30	rwh	<b>LMU00 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
LMU10_EN	31	rwh	<b>LMU10 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled

**MTU\_MEMTESTi (i=1)****Memory MBIST Enable Register i**(0010<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCAN_20_EN	MCAN_10_EN	RES29	GTM_DPLL2_EN	GTM_DPLL1_BC_EN	GTM_DPLL1_A_EN	GTM_MCS1F_AST_E_N	GTM_MCS1_SLOW	GTM_MCS0F_AST_E_N	GTM_MCS0_SLOW	GTM_FIFO_EN	SPU_C1_EN	SPU_C0_EN	SPU_B1_EN	SPU_B0_EN	EMEM_XTM_EN
rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMEM_3_EN	EMEM_2_EN	EMEM_1_EN	EMEM_0_EN	MCDS_EN	RES10	SADM_A_EN	R8	DAM1_EN	DAM0_EN	RES5	RES4	CPU1_DMEM1_EN	CPU0_DMEM1_EN	RES1	LMU2_0_EN
rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	r	r	rwh	rwh	r	rwh

Field	Bits	Type	Description
LMU20_EN	0	rwh	<b>LMU20 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
RESx (x=1,4-5,10,29)	x	r	<b>Reserved</b> Reserved. Shall be written with zero.

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU0_DMEM1_EN</b>	2	rwh	<b>CPU0 DMEM1 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled <sup>1)</sup> .
<b>CPU1_DMEM1_EN</b>	3	rwh	<b>CPU1 DMEM1 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled <sup>2)</sup> .
<b>DAM0_EN</b>	6	rwh	<b>DAM0 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>DAM1_EN</b>	7	rwh	<b>DAM1 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>R8</b>	8	rwh	<b>Reserved - Res</b> Reserved. Not used in this product. Shall be written with zero.
<b>SADMA_EN</b>	9	rwh	<b>Safety DMA SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>MCDS_EN</b>	11	rwh	<b>MCDS memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>EMEM0_EN</b>	12	rwh	<b>EMEM0 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>EMEM1_EN</b>	13	rwh	<b>EMEM1 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>EMEM2_EN</b>	14	rwh	<b>EMEM2 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>EMEM3_EN</b>	15	rwh	<b>EMEM3 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>EMEM_XTM_EN</b>	16	rwh	<b>EMEM XTM memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>SPU_BUFFER0_EN</b>	17	rwh	<b>SPU BUFFER0 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>SPU_BUFFER1_EN</b>	18	rwh	<b>SPU BUFFER1 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>SPU_CONFIG0_EN</b>	19	rwh	<b>SPU CONFIG0 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>SPU_CONFIG1_EN</b>	20	rwh	<b>SPU CONFIG1 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_FIFO_EN</b>	21	rwh	<b>GTM FIFO memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_MCS0SL OW_EN</b>	22	rwh	<b>GTM MCS0 SLOW memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_MCS0FA ST_EN</b>	23	rwh	<b>GTM MCS0 FAST memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_MCS1SL OW_EN</b>	24	rwh	<b>GTM MCS1 SLOW memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_MCS1FA ST_EN</b>	25	rwh	<b>GTM MCS1 FAST memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_DPLL1A_EN</b>	26	rwh	<b>GTM DPLL1A memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_DPLL1B_C_EN</b>	27	rwh	<b>GTM DPLL1BC memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>GTM_DPLL2_EN</b>	28	rwh	<b>GTM DPLL2 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>MCAN10_EN</b>	30	rwh	<b>MCAN10 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>MCAN20_EN</b>	31	rwh	<b>MCAN20 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled

1) Please refer to separate section related to handling of the large DMEM on this device.

2) Please refer to separate section related to handling of the large DMEM on this device.

## Memory Test Unit (MTU)

MTU\_MEMTESTi (i=2)

Memory MBIST Enable Register i

(0010<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPU_F	SPU_F	SPU_F	SPU_F	SPU_F	SPU_F	SPU_F	SPU_F	RES23	RES22	HSPD_M_RA_M_EN	SDMM_C_EN	GIGET_H_TX_EN	GIGET_H_RX_EN	RES17	EMEM5_EN
FT31_	FT30_	FT21_	FT20_	FT11_	FT10_	FT01_	FT00_			rwh	rwh	rwh	rwh	r	rwh
RAM_EN	RAM_EN	RAM_EN	RAM_EN	RAM_EN	RAM_EN	RAM_EN	RAM_EN			rwh	rwh	rwh	rwh	r	rwh
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	r	rwh	rwh	rwh	rwh	r	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMEM4_EN	SCR_RAMINT_EN	SCR_XRAM_EN	R12	R11	R10	R9	R8	ERAY_MBFI_EN	ERAY_MBFO_EN	ERAY_TBF1_E_N	ERAY_TBF1_E_N	ERAY_OBF1_EN	ERAY_OBF0_EN	PSI5_EN	MCAN21_EN
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
MCAN21_EN	0	rwh	<b>MCAN21 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
RESx (x=17,22-23)	x	r	<b>Reserved</b> Reserved. Shall be written with zero.
PSI5_EN	1	rwh	<b>PSI5 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
ERAY_OBF0_E_N	2	rwh	<b>ERAY OBF0 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
ERAY_OBF1_E_N	3	rwh	<b>ERAY OBF1 SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
ERAY_TBF_IB_F0_EN	4	rwh	<b>ERAY TBF IBF0 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
ERAY_TBF_IB_F1_EN	5	rwh	<b>ERAY TBF IBF1 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
ERAY_MBFO_E_N	6	rwh	<b>ERAY MBF0 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
ERAY_MBFI_E_N	7	rwh	<b>ERAY MBF1 memory SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
R8	8	rwh	<b>Reserved - Res</b> Reserved. Not used in this product. Shall be written with zero.

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>R9</b>	9	rwh	<b>Reserved - Res</b> Reserved. Not used in this product. Shall be written with zero.
<b>R10</b>	10	rwh	<b>Reserved - Res</b> Reserved. Not used in this product. Shall be written with zero.
<b>R11</b>	11	rwh	<b>Reserved - Res</b> Reserved. Not used in this product. Shall be written with zero.
<b>R12</b>	12	rwh	<b>Reserved - Res</b> Reserved. Not used in this product. Shall be written with zero.
<b>SCR_XRAM_E_N</b>	13	rwh	<b>SCR XRAM SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled
<b>SCR_RAMINT_EN</b>	14	rwh	<b>SCR Internal RAM SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled
<b>EMEM4_EN</b>	15	rwh	<b>EMEM4 SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled
<b>EMEM5_EN</b>	16	rwh	<b>EMEM5 SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled
<b>GIGETH_RX_EN</b>	18	rwh	<b>Gigabit Ethernet RX SSH instance Enable</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>GIGETH_TX_EN</b>	19	rwh	<b>Gigabit Ethernet TX SSH instance Enable</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>SDMMC_EN</b>	20	rwh	<b>SDMMC memory SSH instance Enable</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>HSPDM_RAM_EN</b>	21	rwh	<b>HDSPDM RAM SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled
<b>SPU_FFT00_RAM_EN</b>	24	rwh	<b>SPU FFT00 RAM SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled
<b>SPU_FFT01_RAM_EN</b>	25	rwh	<b>SPU FFT01 RAM SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled
<b>SPU_FFT10_RAM_EN</b>	26	rwh	<b>SPU FFT10 RAM SSH instance Enable</b> $0_B$ SSH instance is disabled $1_B$ SSH instance is enabled

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>SPU_FFT11_R</b>	27	rwh	<b>SPU FFT11 RAM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>AM_EN</b>			
<b>SPU_FFT20_R</b>	28	rwh	<b>SPU FFT20 RAM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>AM_EN</b>			
<b>SPU_FFT21_R</b>	29	rwh	<b>SPU FFT21 RAM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>AM_EN</b>			
<b>SPU_FFT30_R</b>	30	rwh	<b>SPU FFT30 RAM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>AM_EN</b>			
<b>SPU_FFT31_R</b>	31	rwh	<b>SPU FFT31 RAM SSH instance Enable</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled
<b>AM_EN</b>			

## Memory Test Unit (MTU)

### 13.3.2 MEMMAP Implementation

The Memory Mapping Enable register MEMMAP has configurable control bits to select memory-mapped test mode for each CPU memory.

Cache and Scratchpad memories are physically implemented as a single RAM, but this register function assumes two separate logical RAM partitions. In this register additional bits CPUxDCMAP and CPUxPCMAP are defined. These control the Cache partitions of the RAMs for Data Side and Program side respectively. Since cache content and tags of a cache must be simultaneously switched from memory mapped to cache functional mode, the control bits are mirrored and only one bit is writeable for each cache. The bits corresponding to the tag memories of the same cache will always take the same value as that written to the main Cache Memory control bit. This linkage is product specific.

Please note that the MEMMAP register is used only to map the Cache/Tag memories to system address space. These bits have no effect on testing these memories itself. For system address range into which the memories will be mapped, please refer to the memory map chapter.

#### Memory Mapping Enable Register

The Memory Mapping Enable register MEMMAP has configurable control bits to select memory-mapped test mode. See the Integration Section for mapping of memory controller numbers.

#### MTU\_MEMMAP

**Memory Mapping Enable Register (001C<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		R29	CPU5_PTMA_P	CPU5_PCMA_P	CPU5_DTMA_P	CPU5_DCMA_P	R24	CPU4_PTMA_P	CPU4_PCMA_P	CPU4_DTMA_P	CPU4_DCMA_P	R19	CPU3_PTMA_P	CPU3_PCMA_P	CPU3_DTMA_P
r		rh	rwh	rh	rwh	r	rh	rwh	rh	rwh	rh	r	rh	rwh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU3_DCMA_P	R14	CPU2_PTMA_P	CPU2_PCMA_P	CPU2_DTMA_P	CPU2_DCMA_P	R9	CPU1_PTMA_P	CPU1_PCMA_P	CPU1_DTMA_P	CPU1_DCMA_P	R4	CPU0_PTMA_P	CPU0_PCMA_P	CPU0_DTMA_P	CPU0_DCMA_P
rwh	r	rh	rwh	rh	rwh	r	rh	rwh	rh	rwh	r	rh	rwh	rh	rwh

Field	Bits	Type	Description
CPU0_DCMAP	0	rwh	<b>CPU0 DCACHE Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
CPU0_DTMAP	1	rh	<b>CPU0 DTAG Mapping</b> Read only. Mirrors the state of CPU0_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
CPU0_PCMAP	2	rwh	<b>CPU0 PCACHE Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU0_PTMAP</b>	3	rh	<b>CPU0 PTAG Mapping</b> Read only. Mirrors the state of CPU0_PCMAP. CPU P-cache memories may only be mapped simultaneously. $0_B$ Normal cache function $1_B$ Memory-mapped
<b>R4</b>	4	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU1_DCMAP</b>	5	rwh	<b>CPU1 DCache Mapping</b> $0_B$ Normal cache function $1_B$ Memory-mapped
<b>CPU1_DTMAP</b>	6	rh	<b>CPU1 DTAG Mapping</b> Read only. Mirrors the state of CPU1_DCMAP. CPU D-cache memories may only be mapped simultaneously. $0_B$ Normal cache function $1_B$ Memory-mapped
<b>CPU1_PCMAP</b>	7	rwh	<b>CPU1 PCACHE Mapping</b> $0_B$ Normal cache function $1_B$ Memory-mapped
<b>CPU1_PTMAP</b>	8	rh	<b>CPU1 PTAG Mapping</b> Read only. Mirrors the state of CPU1_PCMAP. CPU P-cache memories may only be mapped simultaneously. $0_B$ Normal cache function $1_B$ Memory-mapped
<b>R9</b>	9	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU2_DCMAP</b>	10	rwh	<b>CPU2 DCache Mapping</b> $0_B$ Normal cache function $1_B$ Memory-mapped
<b>CPU2_DTMAP</b>	11	rh	<b>CPU2 DTAG Mapping</b> Read only. Mirrors the state of CPU2_DCMAP. CPU D-cache memories may only be mapped simultaneously. $0_B$ Normal cache function $1_B$ Memory-mapped
<b>CPU2_PCMAP</b>	12	rwh	<b>CPU2 PCACHE Mapping</b> $0_B$ Normal cache function $1_B$ Memory-mapped
<b>CPU2_PTMAP</b>	13	rh	<b>CPU2 PTAG Mapping</b> Read only. Mirrors the state of CPU2_PCMAP. CPU P-cache memories may only be mapped simultaneously. $0_B$ Normal cache function $1_B$ Memory-mapped
<b>R14</b>	14	r	<b>Reserved - Res</b> Reserved. Not used in this product.

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU3_DCMAP</b>	15	rwh	<b>CPU3 DCache Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU3_DTMAP</b>	16	rh	<b>CPU3 DTAG Mapping</b> Read only. Mirrors the state of CPU3_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU3_PCMAP</b>	17	rwh	<b>CPU3 PCACHE Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU3_PTMAP</b>	18	rh	<b>CPU3 PTAG Mapping</b> Read only. Mirrors the state of CPU3_PCMAP. CPU P-cache memories may only be mapped simultaneously. 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>R19</b>	19	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU4_DCMAP</b>	20	rwh	<b>CPU4 DCache Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU4_DTMAP</b>	21	rh	<b>CPU4 DTAG Mapping</b> Read only. Mirrors the state of CPU4_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU4_PCMAP</b>	22	rwh	<b>CPU4 PCACHE Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU4_PTMAP</b>	23	rh	<b>CPU4 PTAG Mapping</b> Read only. Mirrors the state of CPU4_PCMAP. CPU P-cache memories may only be mapped simultaneously. 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>R24</b>	24	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU5_DCMAP</b>	25	rwh	<b>CPU5 DCache Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU5_DTMAP</b>	26	rh	<b>CPU5 DTAG Mapping</b> Read only. Mirrors the state of CPU5_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU5_PCMAP</b>	27	rwh	<b>CPU5 PCACHE Mapping</b> 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>CPU5_PTMAP</b>	28	rh	<b>CPU5 PTAG Mapping</b> Read only. Mirrors the state of CPU5_PCMAP. CPU P-cache memories may only be mapped simultaneously. 0 <sub>B</sub> Normal cache function 1 <sub>B</sub> Memory-mapped
<b>R29</b>	31:29	r	<b>Reserved - Res</b> Reserved. Not used in this product.

## Memory Test Unit (MTU)

### 13.3.3 MEMSTAT Implementation

The Memory Status Registers MEMSTAT<sub>x</sub> have an implemented bit for each security relevant RAM.

The Data- and Program- Cache and Scratchpad memories are physically implemented as a single RAM with a single MBIST. Hence CPU<sub>x</sub>\_DMEM\_AIU and CPU<sub>x</sub>\_PMEM\_AIU give the status of the partial initialization of the cache partitions for the Data and Program memories respectively.

#### Memory Status Register i

The memory status register MEMSTAT shows whether each SSH instance is currently executing an automatic initialization sequence.

##### MTU\_MEMSTAT<sub>i</sub> (i=0)

**Memory Status Register i** (0038<sub>H</sub>+i\*4) **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		R29	CPU5_PTAG_AIU	CPU5_PMEM_AIU	CPU5_DTAG_AIU	CPU5_DMEM_AIU	R24	CPU4_PTAG_AIU	CPU4_PMEM_AIU	CPU4_DTAG_AIU	CPU4_DMEM_AIU	R19	CPU3_PTAG_AIU	CPU3_PMEM_AIU	CPU3_DTAG_AIU
r			rh	rh	rh	rh	r	rh	rh	rh	rh	r	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU3_DMEM_AIU	R14	CPU2_PTAG_AIU	CPU2_PMEM_AIU	CPU2_DTAG_AIU	CPU2_DMEM_AIU	R9	CPU1_PTAG_AIU	CPU1_PMEM_AIU	CPU1_DTAG_AIU	CPU1_DMEM_AIU	R4	CPU0_PTAG_AIU	CPU0_PMEM_AIU	CPU0_DTAG_AIU	CPU0_DMEM_AIU
rh	r	rh	rh	rh	rh	r	rh	rh	rh	rh	r	rh	rh	rh	rh

Field	Bits	Type	Description
CPU0_DMEM_AIU	0	rh	<b>CPU0 DMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
CPU0_DTAG_AIU	1	rh	<b>CPU0 DTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
CPU0_PMEM_AIU	2	rh	<b>CPU0 PMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize

**Memory Test Unit (MTU)**

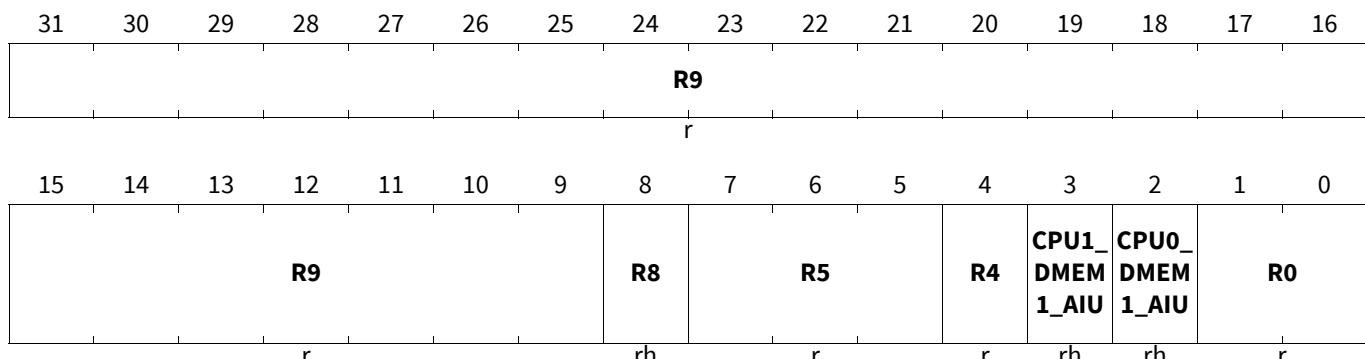
<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU0_PTAG_AIU</b>	3	rh	<b>CPU0 PTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>R4</b>	4	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU1_DMEM_AIU</b>	5	rh	<b>CPU1 DMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU1_DTAG_AIU</b>	6	rh	<b>CPU1 DTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU1_PMEM_AIU</b>	7	rh	<b>CPU1 PMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU1_PTAG_AIU</b>	8	rh	<b>CPU1 PTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>R9</b>	9	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU2_DMEM_AIU</b>	10	rh	<b>CPU2 DMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU2_DTAG_AIU</b>	11	rh	<b>CPU2 DTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU2_PMEM_AIU</b>	12	rh	<b>CPU2 PMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU2_PTAG_AIU</b>	13	rh	<b>CPU2 PTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>R14</b>	14	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU3_DMEM_AIU</b>	15	rh	<b>CPU3 DMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU3_DTAG_AIU</b>	16	rh	<b>CPU3 DTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU3_PMEM_AIU</b>	17	rh	<b>CPU3 PMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU3_PTAG_AIU</b>	18	rh	<b>CPU3 PTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>R19</b>	19	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU4_DMEM_AIU</b>	20	rh	<b>CPU4 DMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize

**Memory Test Unit (MTU)**

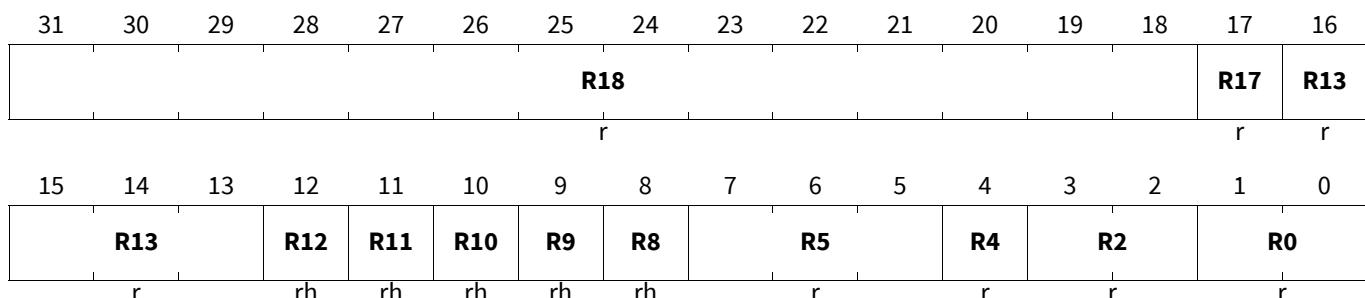
<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU4_DTAG_AIU</b>	21	rh	<b>CPU4 DTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU4_PMEM_AIU</b>	22	rh	<b>CPU4 PMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU4_PTAG_AIU</b>	23	rh	<b>CPU4 PTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>R24</b>	24	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU5_DMEM_AIU</b>	25	rh	<b>CPU5 DMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU5_DTAG_AIU</b>	26	rh	<b>CPU5 DTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU5_PMEM_AIU</b>	27	rh	<b>CPU5 PMEM Partial AutoInitialize of Cache Partition Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>CPU5_PTAG_AIU</b>	28	rh	<b>CPU5 PTAG MBIST AutoInitialize Underway</b> This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0 <sub>B</sub> MBIST not running autoinitialize 1 <sub>B</sub> MBIST running autoinitialize
<b>R29</b>	31:29	r	<b>Reserved - Res</b> Reserved. Not used in this product.

**Memory Test Unit (MTU)****MTU\_MEMSTATi (i=1)****Memory Status Register i****(0038<sub>H</sub>+i\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
<b>R0</b>	1:0	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>CPU0_DMEM1_AIU</b>	2	rh	<b>CPU0 DMEM1 Partial AutoInitialize of Cache Partition Underway</b>  0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled <sup>1)</sup> .
<b>CPU1_DMEM1_AIU</b>	3	rh	<b>CPU1 DMEM1 Partial AutoInitialize of Cache Partition Underway</b>  0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled <sup>2)</sup> .
<b>R4</b>	4	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R5</b>	7:5	r	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R8</b>	8	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R9</b>	31:9	r	<b>Reserved - Res</b> Reserved. Not used in this product.

1) Please refer to separate section related to handling of the large DMEM on this device.

2) Please refer to separate section related to handling of the large DMEM on this device.

**MTU\_MEMSTATi (i=2)****Memory Status Register i****(0038<sub>H</sub>+i\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

**Memory Test Unit (MTU)**

Field	Bits	Type	Description
R0	1:0	r	<b>Reserved - Res</b> Reserved. Not used in this product.
R2	3:2	r	<b>Reserved - Res</b> Reserved. Not used in this product.
R4	4	r	<b>Reserved - Res</b> Reserved. Not used in this product.
R5	7:5	r	<b>Reserved - Res</b> Reserved. Not used in this product.
R8	8	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
R9	9	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
R10	10	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
R11	11	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
R12	12	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
R13	16:13	r	<b>Reserved - Res</b> Reserved. Not used in this product.
R17	17	r	<b>Reserved - Res</b> Reserved. Not used in this product.
R18	31:18	r	<b>Reserved - Res</b> Reserved. Not used in this product.

**13.3.4 MEMDONE Implementation****Memory Test Done Status Register i**

Each bit in one of the memory test done status registers MEMDONEx reflects the status of the MSTATUS.DONE bit in the corresponding SSH. See the implementation section for the implemented register bits.

## Memory Test Unit (MTU)

MTU\_MEMDONEi (i=0)

Memory Test Done Status Register i

(0050<sub>H</sub>+i\*4)Application Reset Value: FFFF FFFF<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LMU1_0_DONE	LMU0_0_DONE	CPU5_DLMU_DON_E	CPU5_PTAG_DONE	CPU5_PMEM_DONE	CPU5_DTAG_DONE	CPU5_DMEM_DONE	CPU4_DLMU_DONE	CPU4_PTAG_DONE	CPU4_PMEM_DONE	CPU4_DTAG_DONE	CPU4_DMEM_DONE	CPU3_DLMU_DONE	CPU3_PTAG_DONE	CPU3_PMEM_DONE	CPU3_DTAG_DONE
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU3_DMEM_DONE	CPU2_DLMU_DONE	CPU2_PTAG_DONE	CPU2_PMEM_DONE	CPU2_DTAG_DONE	CPU2_DMEM_DONE	CPU1_DLMU_STBY_DONE	CPU1_PTAG_DONE	CPU1_PMEM_DONE	CPU1_DTAG_DONE	CPU1_DMEM_DONE	CPU0_DLMU_STBY_DONE	CPU0_PTAG_DONE	CPU0_PMEM_DONE	CPU0_DTAG_DONE	CPU0_DMEM_DONE
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CPU0_DMEM_DONE	0	rh	<b>CPU0 DMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU0_DTAG_DONE	1	rh	<b>CPU0 DTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU0_PMEM_DONE	2	rh	<b>CPU0 PMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU0_PTAG_DONE	3	rh	<b>CPU0 PTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU0_DLMU_STBY_DONE	4	rh	<b>CPU0 STANDBY DLMU Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU1_DMEM_DONE	5	rh	<b>CPU1 DMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU1_DTAG_DONE	6	rh	<b>CPU1 DTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU1_PMEM_DONE	7	rh	<b>CPU1 PMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU1_PTAG_DONE	8	rh	<b>CPU1 PTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1

**Memory Test Unit (MTU)**

Field	Bits	Type	Description
CPU1_DLMU_STBY_DONE	9	rh	<b>CPU1 STANDBY DLMU Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU2_DMEM_DONE	10	rh	<b>CPU2 DMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU2_DTAG_DONE	11	rh	<b>CPU2 DTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU2_PMEM_DONE	12	rh	<b>CPU2 PMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU2_PTAG_DONE	13	rh	<b>CPU2 PTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU2_DLMU_DONE	14	rh	<b>CPU2 DLMU memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU3_DMEM_DONE	15	rh	<b>CPU3 DMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU3_DTAG_DONE	16	rh	<b>CPU3 DTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU3_PMEM_DONE	17	rh	<b>CPU3 PMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU3_PTAG_DONE	18	rh	<b>CPU3 PTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU3_DLMU_DONE	19	rh	<b>CPU3 DLMU memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU4_DMEM_DONE	20	rh	<b>CPU4 DMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU4_DTAG_DONE	21	rh	<b>CPU4 DTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU4_PMEM_DONE	22	rh	<b>CPU4 PMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU4_PTAG_DONE	23	rh	<b>CPU4 PTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1

**Memory Test Unit (MTU)**

Field	Bits	Type	Description
CPU4_DLMU_DONE	24	rh	<b>CPU4 DLMU memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU5_DMEM_DONE	25	rh	<b>CPU5 DMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU5_DTAG_DONE	26	rh	<b>CPU5 DTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU5_PMEM_DONE	27	rh	<b>CPU5 PMEM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU5_PTAG_DONE	28	rh	<b>CPU5 PTAG Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
CPU5_DLMU_DONE	29	rh	<b>CPU5 DLMU memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
LMU00_DONE	30	rh	<b>LMU00 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
LMU10_DONE	31	rh	<b>LMU10 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1

**MTU\_MEMDONE*i* (i=1)****Memory Test Done Status Register i****(0050<sub>H</sub>+i\*4)****Application Reset Value: FFFF FFFF<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCAN_20_DO_NE	MCAN_10_DO_NE	RES29	GTM_DPLL2_E	GTM_DPLL1_BC_D	GTM_DPLL1_A_DO_NE	GTM_MCS1F	GTM_MCS1_SLOW	GTM_MCS0F	GTM_MCS0_SLOW	GTM_FIFO_D_ONE	SPU_C_1_DO_NE	SPU_C_0_DO_NE	SPU_B_1_DO_NE	SPU_B_0_DO_NE	EMEM_XTM_DONE
rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMEM_3_DO_NE	EMEM_2_DO_NE	EMEM_1_DO_NE	EMEM_0_DO_NE	MCDS_DONE	RES10	SADM_A_DO_NE	R8	DAM1_DONE	DAM0_DONE	RES5	RES4	CPU1_DMEM_1_DO_NE	CPU0_DMEM_1_DO_NE	RES1	LMU20_DONE
rh	rh	rh	rh	rh	r	rh	rh	rh	rh	r	r	rh	rh	r	rh

Field	Bits	Type	Description
LMU20_DONE	0	rh	<b>LMU20 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>RESz (z=1,4-5,10,29)</b>	z	r	<b>Reserved</b> Reserved. Not used in this product.
<b>CPU0_DMEM1_DONE</b>	2	rh	<b>CPU0 DMEM1 Test Done Status</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled <sup>1)</sup> .
<b>CPU1_DMEM1_DONE</b>	3	rh	<b>CPU1 DMEM1 Test Done Status</b> 0 <sub>B</sub> SSH instance is disabled 1 <sub>B</sub> SSH instance is enabled <sup>2)</sup> .
<b>DAM0_DONE</b>	6	rh	<b>DAM0 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>DAM1_DONE</b>	7	rh	<b>DAM1 Test Done Status - DAM1_DONE</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>R8</b>	8	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>SADMA_DONE</b>	9	rh	<b>Safety DMA Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>MCDS_DONE</b>	11	rh	<b>MCDS memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>EMEM0_DONE</b>	12	rh	<b>EMEM0 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>EMEM1_DONE</b>	13	rh	<b>EMEM1 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>EMEM2_DONE</b>	14	rh	<b>EMEM2 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>EMEM3_DONE</b>	15	rh	<b>EMEM3 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>EMEM_XTM_DONE</b>	16	rh	<b>EMEM XTM memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>SPU_BUFFER0_DONE</b>	17	rh	<b>SPU BUFFER0 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>SPU_BUFFER1_DONE</b>	18	rh	<b>SPU BUFFER1 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1

**Memory Test Unit (MTU)**

Field	Bits	Type	Description
<b>SPU_CONFIG0_DONE</b>	19	rh	<b>SPU CONFIG0 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>SPU_CONFIG1_DONE</b>	20	rh	<b>SPU CONFIG1 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_FIFO_DONE</b>	21	rh	<b>GTM FIFO memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_MCS0LOW_DONE</b>	22	rh	<b>GTM MCS0 SLOW memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_MCS0FAST_ST_DONE</b>	23	rh	<b>GTM MCS0 FAST memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_MCS1LOW_DONE</b>	24	rh	<b>GTM MCS1 SLOW memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_MCS1FAST_ST_DONE</b>	25	rh	<b>GTM MCS1 FAST memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_DPLL1ADONE</b>	26	rh	<b>GTM DPLL1A memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_DPLL1BC_DONE</b>	27	rh	<b>GTM DPLL1BC memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GTM_DPLL2_DONE</b>	28	rh	<b>GTM DPLL2 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>MCAN10_DONE</b>	30	rh	<b>MCAN10 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>MCAN20_DONE</b>	31	rh	<b>MCAN20 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1

1) Please refer to separate section related to handling of the large DMEM on this device.

2) Please refer to separate section related to handling of the large DMEM on this device.

## Memory Test Unit (MTU)

## MTU\_MEMDONEi (i=2)

## Memory Test Done Status Register i

(0050<sub>H</sub>+i\*4)Application Reset Value: FFFF FFFF<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPU_F FT31_ RAM_ DONE	SPU_F FT30_ RAM_ DONE	SPU_F FT21_ RAM_ DONE	SPU_F FT20_ RAM_ DONE	SPU_F FT11_ RAM_ DONE	SPU_F FT10_ RAM_ DONE	SPU_F FT01_ RAM_ DONE	SPU_F FT00_ RAM_ DONE	RES23	RES22	HSPD_M_RA_M_DO_NE	SDMM_C_DO_NE	GIGET_H_TX_DONE	GIGET_H_RX_DONE	RES17	EMEM5_DO_NE
rh	rh	rh	rh	rh	rh	rh	rh	r	r	rh	rh	rh	rh	r	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMEM4_DONE NE	SCR_RAMINT_DON_E	SCR_XRAM_DONE	R12	R11	R10	R9	R8	ERAY_MBFI_DONE	ERAY_MBFO_DONE	ERAY_TBF1_DONE	ERAY_TBF_I_DONE	ERAY_OBF1_DONE	ERAY_OBF0_DONE	PSI5_DONE	MCAN21_DONE
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
MCAN21_DONE	0	rh	<b>MCAN21 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
RESz (z=17,22-23)	z	r	<b>Reserved</b> Reserved. Not used in this product.
PSI5_DONE	1	rh	<b>PSI5 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
ERAY_OBF0 DONE	2	rh	<b>ERAY OBF0 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
ERAY_OBF1 DONE	3	rh	<b>ERAY OBF1 Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
ERAY_TBF_IBF0 DONE	4	rh	<b>ERAY TBF IBF0 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
ERAY_TBF_IBF1 DONE	5	rh	<b>ERAY TBF IBF1 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
ERAY_MBFI DONE	6	rh	<b>ERAY MBF0 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
ERAY_MBFO DONE	7	rh	<b>ERAY MBF1 memory Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
R8	8	rh	<b>Reserved - Res</b> Reserved. Not used in this product.

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>R9</b>	9	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R10</b>	10	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R11</b>	11	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R12</b>	12	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>SCR_XRAM_D ONE</b>	13	rh	<b>SCR XRAM Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>SCR_RAMINT_ DONE</b>	14	rh	<b>SCR Internal RAM Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>EMEM4_DONE</b>	15	rh	<b>EMEM4 Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>EMEM5_DONE</b>	16	rh	<b>EMEM5 Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>GIGETH_RX_D ONE</b>	18	rh	<b>Gigabit Ethernet RX memoryTest Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>GIGETH_TX_D ONE</b>	19	rh	<b>Gigabit Ethernet TX memoryTest Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>SDMMC_DON E</b>	20	rh	<b>SDMMC memoryTest Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>HSPDM_RAM_ DONE</b>	21	rh	<b>HDS PDM RAM Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>SPU_FFT00_R AM_DONE</b>	24	rh	<b>SPU FFT00 RAM Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>SPU_FFT01_R AM_DONE</b>	25	rh	<b>SPU FFT01 RAM Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>SPU_FFT10_R AM_DONE</b>	26	rh	<b>SPU FFT10 RAM Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1
<b>SPU_FFT11_R AM_DONE</b>	27	rh	<b>SPU FFT11 RAM Test Done Status</b> $0_B$ SSH MSTATUS.DONE = 0 $1_B$ SSH MSTATUS.DONE = 1

**Memory Test Unit (MTU)**

Field	Bits	Type	Description
<b>SPU_FFT20_R_AM_DONE</b>	28	rh	<b>SPU FFT20 RAM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>SPU_FFT21_R_AM_DONE</b>	29	rh	<b>SPU FFT21 RAM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>SPU_FFT30_R_AM_DONE</b>	30	rh	<b>SPU FFT30 RAM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>SPU_FFT31_R_AM_DONE</b>	31	rh	<b>SPU FFT31 RAM Test Done Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1

**13.3.5 MEMFDA Implementation****Memory Test FDA Status Register i**

Each bit in one of the memory test done status registers MEMFDAx reflects the status of the MSTATUS.FDA bit in the corresponding SSH. See the implementation section for the implemented register bits.

**MTU\_MEMFDAi (i=0)****Memory Test FDA Status Register i**(0060<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LMU1_0_FDA	LMU0_0_FDA	CPU5_DLMU_FDA	CPU5_PTAG_FDA	CPU5_PMEM_FDA	CPU5_DTAG_FDA	CPU5_DMEM_FDA	CPU4_DLMU_FDA	CPU4_PTAG_FDA	CPU4_PMEM_FDA	CPU4_DTAG_FDA	CPU4_DMEM_FDA	CPU3_DLMU_FDA	CPU3_PTAG_FDA	CPU3_PMEM_FDA	CPU3_DTAG_FDA
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU3_DMEM_FDA	CPU2_DLMU_FDA	CPU2_PTAG_FDA	CPU2_PMEM_FDA	CPU2_DTAG_FDA	CPU2_DMEM_FDA	CPU1_DLMU_STBY_FDA	CPU1_PTAG_FDA	CPU1_PMEM_FDA	CPU1_DTAG_FDA	CPU1_DMEM_FDA	CPU0_DLMU_STBY_FDA	CPU0_PTAG_FDA	CPU0_PMEM_FDA	CPU0_DTAG_FDA	CPU0_DMEM_FDA
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
<b>CPU0_DMEM_FDA</b>	0	rh	<b>CPU0 DMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU0_DTAG_FDA</b>	1	rh	<b>CPU0 DTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU0_PMEM_FDA</b>	2	rh	<b>CPU0 PMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU0_PTAG_FDA</b>	3	rh	<b>CPU0 PTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU0_DLMU_STBY_FDA</b>	4	rh	<b>CPU0 STANDBY DLMU Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU1_DMEM_FDA</b>	5	rh	<b>CPU1 DMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU1_DTAG_FDA</b>	6	rh	<b>CPU1 DTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU1_PMEM_FDA</b>	7	rh	<b>CPU1 PMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU1_PTAG_FDA</b>	8	rh	<b>CPU1 PTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU1_DLMU_STBY_FDA</b>	9	rh	<b>CPU1 STANDBY DLMU Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU2_DMEM_FDA</b>	10	rh	<b>CPU2 DMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU2_DTAG_FDA</b>	11	rh	<b>CPU2 DTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU2_PMEM_FDA</b>	12	rh	<b>CPU2 PMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU2_PTAG_FDA</b>	13	rh	<b>CPU2 PTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU2_DLMU_FDA</b>	14	rh	<b>CPU2 DLMU memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU3_DMEM_FDA</b>	15	rh	<b>CPU3 DMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU3_DTAG_FDA</b>	16	rh	<b>CPU3 DTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU3_PMEM_FDA</b>	17	rh	<b>CPU3 PMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CPU3_PTAG_FDA</b>	18	rh	<b>CPU3 PTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU3_DLMU_FDA</b>	19	rh	<b>CPU3 DLMU memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU4_DMEM_FDA</b>	20	rh	<b>CPU4 DMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU4_DTAG_FDA</b>	21	rh	<b>CPU4 DTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU4_PMEM_FDA</b>	22	rh	<b>CPU4 PMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU4_PTAG_FDA</b>	23	rh	<b>CPU4 PTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU4_DLMU_FDA</b>	24	rh	<b>CPU4 DLMU memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU5_DMEM_FDA</b>	25	rh	<b>CPU5 DMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU5_DTAG_FDA</b>	26	rh	<b>CPU5 DTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU5_PMEM_FDA</b>	27	rh	<b>CPU5 PMEM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU5_PTAG_FDA</b>	28	rh	<b>CPU5 PTAG Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>CPU5_DLMU_FDA</b>	29	rh	<b>CPU5 DLMU memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>LMU00_FDA</b>	30	rh	<b>LMU00 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>LMU10_FDA</b>	31	rh	<b>LMU10 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

## Memory Test Unit (MTU)

## MTU\_MEMFDAi (i=1)

## Memory Test FDA Status Register i

(0060<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCAN 20_FDA A	MCAN 10_FDA A	RES29	GTM_ DPLL2 _FDA	GTM_ DPLL1 BC_FD A	GTM_ DPLL1 AST_F DA	GTM_ MCS1F SLOW	GTM_ MCS1 _FDA	GTM_ MCS0F SLOW	GTM_ MCS0 _FDA	GTM_F IFO_F DA	SPU_C ONFIG 1_FDA	SPU_C ONFIG 0_FDA	SPU_B UFFER 1_FDA	SPU_B UFFER 0_FDA	EMEM XTM_ FDA
rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMEM 3_FDA	EMEM 2_FDA	EMEM 1_FDA	EMEM 0_FDA	MCDS _FDA	RES10	SADM A_FDA	R8	DAM1 _FDA	DAM0 _FDA	RES5	RES4	CPU1 DMEM 1_FDA	CPU0 DMEM 1_FDA	RES1	LMU2 0_FDA
rh	rh	rh	rh	rh	r	rh	rh	rh	rh	r	r	rh	rh	r	rh

Field	Bits	Type	Description
LMU20_FDA	0	rh	<b>LMU20 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
RESz (z=1,4-5,10,29)	z	r	<b>Reserved</b> Reserved. Not used in this product.
CPU0_DMEM1_FDA	2	rh	<b>CPU0 DMEM1 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
CPU1_DMEM1_FDA	3	rh	<b>CPU1 DMEM1 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
DAM0_FDA	6	rh	<b>DAM0 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
DAM1_FDA	7	rh	<b>DAM1 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
R8	8	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
SADMA_FDA	9	rh	<b>Safety DMA Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
MCDS_FDA	11	rh	<b>MCDS memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
EMEM0_FDA	12	rh	<b>EMEM0 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>EMEM1_FDA</b>	13	rh	<b>EMEM1 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>EMEM2_FDA</b>	14	rh	<b>EMEM2 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>EMEM3_FDA</b>	15	rh	<b>EMEM3 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>EMEM_XTM_FDA</b>	16	rh	<b>EMEM XTM memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>SPU_BUFFER0_FDA</b>	17	rh	<b>SPU BUFFER0 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>SPU_BUFFER1_FDA</b>	18	rh	<b>SPU BUFFER1 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>SPU_CONFIG0_FDA</b>	19	rh	<b>SPU CONFIG0 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>SPU_CONFIG1_FDA</b>	20	rh	<b>SPU CONFIG1 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GTM_FIFO_FA</b>	21	rh	<b>GTM FIFO memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GTM_MCS0SLOW_FDA</b>	22	rh	<b>GTM MCS0 SLOW memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GTM_MCS0FAST_FDA</b>	23	rh	<b>GTM MCS0 FAST memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GTM_MCS1SLOW_FDA</b>	24	rh	<b>GTM MCS1 SLOW memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GTM_MCS1FAST_FDA</b>	25	rh	<b>GTM MCS1 FAST memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GTM_DPLL1AFDA</b>	26	rh	<b>GTM DPLL1A memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GTM_DPLL1BCFDA</b>	27	rh	<b>GTM DPLL1BC memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

**Memory Test Unit (MTU)**

Field	Bits	Type	Description
<b>GTM_DPLL2_FDA</b>	28	rh	<b>GTM DPLL2 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>MCAN10_FDA</b>	30	rh	<b>MCAN10 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>MCAN20_FDA</b>	31	rh	<b>MCAN20 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

**MTU\_MEMFDAi (i=2)****Memory Test FDA Status Register i**(0060<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SPU_FFT31_DA</b>	<b>SPU_FFT30_DA</b>	<b>SPU_FFT21_DA</b>	<b>SPU_FFT20_DA</b>	<b>SPU_FFT11_DA</b>	<b>SPU_FFT10_DA</b>	<b>SPU_FFT01_DA</b>	<b>SPU_FFT00_DA</b>	<b>RES23</b>	<b>RES22</b>	<b>HSPD_M_RAM_FD_A</b>	<b>SDMM_C_FDA</b>	<b>GIGETH_RX_FDA</b>	<b>GIGETH_RX_FDA</b>	<b>RES17</b>	<b>EMEM5_FDA</b>
rh	rh	rh	rh	rh	rh	rh	rh	r	r	rh	rh	rh	rh	r	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>EMEM4_FDA</b>	<b>SCR_RAMINT_FDA</b>	<b>SCR_XRAM_FDA</b>	<b>R12</b>	<b>R11</b>	<b>R10</b>	<b>R9</b>	<b>R8</b>	<b>ERAYMBF1_FDA</b>	<b>ERAYMBF0_FDA</b>	<b>ERAYTBF1_FDA</b>	<b>ERAYTBF0_FDA</b>	<b>ERAYOBF1_FDA</b>	<b>ERAYOBFO_FDA</b>	<b>PSI5_FDA</b>	<b>MCAN21_FDA</b>
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
<b>MCAN21_FDA</b>	0	rh	<b>MCAN20 memory Test FDA Status - MCAN20_FDA</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>RESz (z=17,22-23)</b>	z	r	<b>Reserved</b> Reserved. Not used in this product.
<b>PSI5_FDA</b>	1	rh	<b>PSI5 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>ERAY_OBF0_FDA</b>	2	rh	<b>ERAY OBF0 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>ERAY_OBF1_FDA</b>	3	rh	<b>ERAY OBF1 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>ERAY_TBF_IB_F0_FDA</b>	4	rh	<b>ERAY TBF IBF0 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>ERAY_TBF_IB_F1_FDA</b>	5	rh	<b>ERAY TBF IBF1 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>ERAY_MBF0_FDA</b>	6	rh	<b>ERAY MBF0 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>ERAY_MBF1_FDA</b>	7	rh	<b>ERAY MBF1 memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>R8</b>	8	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R9</b>	9	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R10</b>	10	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R11</b>	11	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>R12</b>	12	rh	<b>Reserved - Res</b> Reserved. Not used in this product.
<b>SCR_XRAM_FDA</b>	13	rh	<b>SCR XRAM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>SCR_RAMINT_FDA</b>	14	rh	<b>SCR Internal RAM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>EMEM4_FDA</b>	15	rh	<b>EMEM4 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>EMEM5_FDA</b>	16	rh	<b>EMEM5 Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1
<b>GIGETH_RX_FDA</b>	18	rh	<b>Gigabit Ethernet RX memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>GIGETH_TX_FDA</b>	19	rh	<b>Gigabit Ethernet TX SSH memory Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>SDMMC_FDA</b>	20	rh	<b>SDMMC memory SSH Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.DONE = 0 1 <sub>B</sub> SSH MSTATUS.DONE = 1
<b>HSPDM_RAM_FDA</b>	21	rh	<b>HDSPDM RAM Test FDA Status</b> 0 <sub>B</sub> SSH MSTATUS.FDA = 0 1 <sub>B</sub> SSH MSTATUS.FDA = 1

**Memory Test Unit (MTU)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>SPU_FFT00_R AM_FDA</b>	24	rh	<b>SPU FFT00 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1
<b>SPU_FFT01_R AM_FDA</b>	25	rh	<b>SPU FFT01 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1
<b>SPU_FFT10_R AM_FDA</b>	26	rh	<b>SPU FFT10 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1
<b>SPU_FFT11_R AM_FDA</b>	27	rh	<b>SPU FFT11 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1
<b>SPU_FFT20_R AM_FDA</b>	28	rh	<b>SPU FFT20 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1
<b>SPU_FFT21_R AM_FDA</b>	29	rh	<b>SPU FFT21 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1
<b>SPU_FFT30_R AM_FDA</b>	30	rh	<b>SPU FFT30 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1
<b>SPU_FFT31_R AM_FDA</b>	31	rh	<b>SPU FFT31 RAM Test FDA Status</b> $0_B$ SSH MSTATUS.FDA = 0 $1_B$ SSH MSTATUS.FDA = 1

## Memory Test Unit (MTU)

### 13.4 SSH Instances

The system SRAMs do not all have the same configuration. [Table 69 “SSH instances” on Page 37](#) shows the instance-specific configurations of the SRAM Support Hardware.

The ECC values for all SRAMs are computed only out of the data information\*.

The base address of an SSH instance MC<sub>x</sub> can be calculated from the MC\_BASE (defined in the platform chapter) as: Base Address of SSH instance x (MC<sub>x</sub>) = MC\_BASE + x\*0x100

**Table 69 SSH instances**

(MC <sub>x</sub> ) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
0	CPU0_DMEM	5	SECDED	2	16
1	CPU0_DTAG	5	SECDED	2	4
2	CPU0_PMEM	5	SECDED	2	8
3	CPU0_PTAG	5	DED	2	4
4	CPU0_DLMU_STBY	5	SECDED	2	8
5	CPU1_DMEM	5	SECDED	2	16
6	CPU1_DTAG	5	SECDED	2	4
7	CPU1_PMEM	5	SECDED	2	8
8	CPU1_PTAG	5	DED	2	4
9	CPU1_DLMU_STBY	5	SECDED	2	8
10	CPU2_DMEM	5	SECDED	2	16
11	CPU2_DTAG	5	SECDED	2	4
12	CPU2_PMEM	5	SECDED	2	8
13	CPU2_PTAG	5	DED	2	4
14	CPU2_DLMU	5	SECDED	2	8
15	CPU3_DMEM	5	SECDED	2	16
16	CPU3_DTAG	5	SECDED	2	4
17	CPU3_PMEM	5	SECDED	2	8
18	CPU3_PTAG	5	DED	2	4
19	CPU3_DLMU	5	SECDED	2	8
20	CPU4_DMEM	5	SECDED	2	16
21	CPU4_DTAG	5	SECDED	2	4
22	CPU4_PMEM	5	SECDED	2	8
23	CPU4_PTAG	5	DED	2	4
24	CPU4_DLMU	5	SECDED	2	8
25	CPU5_DMEM	5	SECDED	2	16
26	CPU5_DTAG	5	SECDED	2	4
27	CPU5_PMEM	5	SECDED	2	8
28	CPU5_PTAG	5	DED	2	4
29	CPU5_DLMU	5	SECDED	2	8

**Memory Test Unit (MTU)****Table 69 SSH instances (cont'd)**

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
30	LMU00	5	SECDED	2	8
31	LMU10	5	SECDED	2	8
32	LMU20	5	SECDED	2	8
33	Reserved				
34	CPU0_DMEM1	5	SECDED	2	16
35	CPU1_DMEM1	5	SECDED	2	16
36-37	Reserved				
38	DAM0	5	SECDED	1	8
39	DAM1	5	SECDED	1	8
41	SADMA	5	SECDED	1	4
42	Reserved				
43	MCDS	5	DED	1	4
44	EMEM0	5	SECDED	1	8
45	EMEM1	5	SECDED	1	8
46	EMEM2	5	SECDED	1	8
47	EMEM3	5	SECDED	1	8
48	EMEM_XTM	5	SECDED	1	4
49	SPU_BUFFER0	5	SECDED	1	4
50	SPU_BUFFER1	5	SECDED	1	4
51	SPU_CONFIG0	5	SECDED	2	8
52	SPU_CONFIG1	5	SECDED	2	8
53	GTM_FIFO	5	SECDED	1	4
54	GTM_MCS0SLOW	5	SECDED	1	4
55	GTM_MCS0FAST	5	SECDED	1	4
56	GTM_MCS1SLOW	5	SECDED	1	4
57	GTM_MCS1FAST	5	SECDED	1	4
58	GTM_DPLL1A	5	SECDED	1	4
59	GTM_DPLL1BC	5	SECDED	1	4
60	GTM_DPLL2	5	SECDED	1	8
61	<b>Reserved</b>				
62	M_CAN10	5	SECDED	1	16
63	M_CAN20	5	SECDED	1	16
64	M_CAN21	5	SECDED	1	16
65	PSI5	5	SECDED	1	4
66	ERAY_OBF0	5	SECDED	1	4
67	ERAY_OBF1	5	SECDED	1	4
68	ERAY_TBF_IBF0	5	SECDED	1	4

**Memory Test Unit (MTU)****Table 69 SSH instances (cont'd)**

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
69	ERAY_TBF_IBF1	5	SECDED	1	4
70	ERAY_MBFO	5	SECDED	1	4
71	ERAY_MBFI	5	SECDED	1	4
77	SCR_XRAM	5	SECDED	2	8
78	SCR_RAMINT	5	SECDED	1	4
79	Reserved				
80	Reserved				
81	Reserved				
82	GIGETH_RX_RAM	5	SECDED	1	4
83	GIGETH_TX_RAM	5	SECDED	1	4
84	SDMMC_RAM	5	SECDED	1	4
85	HSPDM_RAM	5	SECDED	1	8
86- 87	Reserved				
88	SPU_FFT00	5	SECDED	1	4
89	SPU_FFT01	5	SECDED	1	4
90	SPU_FFT10	5	SECDED	1	4
91	SPU_FFT11	5	SECDED	1	4
92	SPU_FFT20	5	SECDED	1	4
93	SPU_FFT21	5	SECDED	1	4
94	SPU_FFT30	5	SECDED	1	4
95	SPU_FFT31	5	SECDED	1	4

**Memory Test Unit (MTU)****13.4.1 Ganging for SRAM test and initialization**

Whenever an MBIST test or SRAM initialization is started via the MTU/SSH, there is a certain jump in the current consumption, due to the parallel accesses to the SRAM cells during the test or initialization. This current jump is different for the different SRAMs in the product, and depends on the size of the SRAM, the clock frequency e.t.c. If too many SRAMs are tested or initialized in parallel, it may result in a significant current jump, which may put the device outside of the specified operating conditions. On the other hand, in order to reduce the overall test and/or initialization time, it may be imperative for the application to perform the test or initialization of many SRAMs in parallel.

In order to achieve this trade-off between current jump and test/initialization time - it is advised to partition the available SRAMs into different “Gangs”. This is referred to as Ganging. The SRAMs in each Gang are all initialized/tested in parallel - while the Gangs themselves are executed in sequence, one after the other. This ensures that the current jump never exceeds the allowed limits, while at the same time the overall test time is minimized.

Gangs 0-16 are defined for the platform. Depending on the device and the number of implemented SRAMs, the number of gangs needed may be less. The numbering of the gangs is not important and does not signify any order.

In the below ganging tables, a ganging configuration for this product is shown. This assumes a 4-march element (4N) non-destructive test (r,w\*,r\*,w) on a zero-data background (i.e. the SRAM is cleared with ECC-correct zero data). The same gangs may be used for SRAM initialization.

The provided ganging example is ensured to satisfy the specified limitations in current jumps of this device, while at the same time optimizing the overall test time. All implemented SRAMs are considered here. If certain SRAMs are not of interest to a particular application, then the gangs may be modified appropriately.

**Table 70 GANG-0**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
44	EMEM0
62	M_CAN10

**Table 71 GANG-1**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
45	EMEM1
63	M_CAN20
64	M_CAN21
70	ERAY_MBF0

**Table 72 GANG-2**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
46	EMEM2
71	ERAY_MBF1

**Table 73 GANG-3**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
47	EMEM3

**Memory Test Unit (MTU)****Table 74 GANG-4**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
34	CPU0_DMEM1
35	CPU1_DMEM1
60	GTM_DPLL2
78	SCR_RAMINT

**Table 75 GANG-5**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
00	CPU0_DMEM
05	CPU1_DMEM
77	SCR_XRAM
85	HSPDM_RAM

**Table 76 GANG-6**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
04	CPU0_DLMU_STBY
30	LMU00
31	LMU10
53	GTM_FIFO

**Table 77 GANG-7**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
10	CPU2_DMEM
32	LMU20
54	GTM_MCS0SLOW
82	GIGETH_RX_RAM
84	SDMMC_RAM

**Table 78 GANG-8**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
15	CPU3_DMEM
20	CPU4_DMEM

**Table 79 GANG-9**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
25	CPU5_DMEM
51	SPU_CONFIG0

**Memory Test Unit (MTU)****Table 79 GANG-9**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
52	SPU_CONFIG1
56	GTM_MCS1SLOW

**Table 80 GANG-10**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
19	CPU3_DLMU
24	CPU4_DLMU
29	CPU5_DLMU
38	DAM0
39	DAM1
83	GIGETH_TX_RAM

**Table 81 GANG-11**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
02	CPU0_PMEM
09	CPU1_DLMU_STBY
14	CPU2_DLMU
55	GTM_MCS0FAST
57	GTM_MCS1FAST
65	PSI5

**Table 82 GANG-12**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
07	CPU1_PMEM
12	CPU2_PMEM
17	CPU3_PMEM

**Table 83 GANG-13**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
03	CPU0_PTAG
22	CPU4_PMEM
27	CPU5_PMEM
43	MCDS
48	EMEM_XTM

**Memory Test Unit (MTU)****Table 84 GANG-14**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
08	CPU1_PTAG
13	CPU2_PTAG
18	CPU3_PTAG
23	CPU4_PTAG
28	CPU5_PTAG
49	SPU_BUFFER0
50	SPU_BUFFER1
59	GTM_DPLL1BC

**Table 85 GANG-15**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
01	CPU0_DTAG
06	CPU1_DTAG
11	CPU2_DTAG
16	CPU3_DTAG
21	CPU4_DTAG
26	CPU5_DTAG
41	SADMA
58	GTM_DPLL1A
66	ERAY_OBF0
67	ERAY_OBF1
68	ERAY_TBF_IBF0
69	ERAY_TBF_IBF1
88-93	SPU_FFT00, 01, 10, 11, 20, 21

**Table 86 GANG-16**

<b>MCx(x=)</b>	<b>Module / SRAM</b>
94	SPU_FFT30
95	SPU_FFT31

**13.5 Connectivity**

**Memory Test Unit (MTU)****Table 87 Connections of MTU**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
MTU:CPU0DCMAP	to	cpu_pfi_pfrwb_0:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU1DCMAP	to	cpu_pfi_pfrwb_1:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU2DCMAP	to	cpu_pfi_pfrwb_2:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU3DCMAP	to	cpu_pfi_pfrwb_3:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU4DCMAP	to	cpu_pfi_pfrwb_4:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU5DCMAP	to	cpu_pfi_pfrwb_5:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU0PCMAP	to	cpu_pfi_pfrwb_0:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:CPU1PCMAP	to	cpu_pfi_pfrwb_1:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:CPU2PCMAP	to	cpu_pfi_pfrwb_2:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:CPU3PCMAP	to	cpu_pfi_pfrwb_3:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:CPU4PCMAP	to	cpu_pfi_pfrwb_4:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:CPU5PCMAP	to	cpu_pfi_pfrwb_5:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:dmu_no_ram_init	from	DMU:MTU_NO_RAMIN	Disable RAM auto-initialization
MTU:scu_hsm_dbg	from	SCU:scu_hsm_dbg	HSM debug enable from SCU
MTU:sleep_n	from	SCU:scu_syst_sleep_n	Sleep request
MTU:DONE_INT	to	INT:mtu.DONE_INT	MTU Done Service Request
MTU:tcu_hsm_dbg_analysis_en	from	TCU:hsm_debug_mode	HSM debug request from TCU

**Memory Test Unit (MTU)****13.6 Revision History****Table 88 Revision History**

Reference	Change to Previous Version	Comment
<b>V7.4.7</b>		
<a href="#">Page 45</a>	Revision History entries up to V7.4.6 removed.	
<a href="#">Page 40</a>	Ganging information updated.	
<a href="#">Page 43</a>	Connectivity information updated.	
<b>V7.4.8</b>		
<a href="#">Page 45</a>	Revision History entries up to V7.4.7 removed.	
<a href="#">Page 12</a>	MEMMAP Reserved (not implemented) bits changed to "read".	
<a href="#">Page 3</a> , <a href="#">Page 21</a> , <a href="#">Page 29</a>	"SADMA" changed to "Safety DMA" in short description of MEMTEST1/9, MEMDONE1/9 and MEMFDA1/9 bit fields.	
<b>V7.4.9</b>		
-	No functional changes.	
<a href="#">Page 40</a>	Corrected typo CPU1_PTAG to CPU1_DTAG in Ganging Information for Gang 15, SSH 06.	
<a href="#">Page 43</a>	Formal update of connectivity table, noch functional change.	
<b>V7.4.10</b>		
-	No functional changes.	
<b>V7.4.11</b>		
-	No functional changes.	
<b>V7.4.12</b>		
-	No functional changes.	
<b>V7.4.13</b>		
-	No functional changes.	

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**

## 14 General Purpose I/O Ports and Peripheral I/O Lines (Ports)

This chapter supplements the family documentation with device specific information for TC39x-B.

### 14.1 TC39x-B Specific IP Configuration

The Ports configuration (which Port modules are implemented, their width and functionality) is represented by the device specific register set shown in this chapter.

### 14.2 TC39x-B Specific Register Set

**Table 89 Register Address Space - Pn**

Module	Base Address	End Address	Note
P00	F003A000 <sub>H</sub>	F003A0FF <sub>H</sub>	SPB bus slave interface
P01	F003A100 <sub>H</sub>	F003A1FF <sub>H</sub>	SPB bus slave interface
P02	F003A200 <sub>H</sub>	F003A2FF <sub>H</sub>	SPB bus slave interface
P10	F003AA00 <sub>H</sub>	F003AAFF <sub>H</sub>	SPB bus slave interface
P11	F003AB00 <sub>H</sub>	F003ABFF <sub>H</sub>	SPB bus slave interface
P12	F003AC00 <sub>H</sub>	F003ACFF <sub>H</sub>	SPB bus slave interface
P13	F003AD00 <sub>H</sub>	F003ADFF <sub>H</sub>	SPB bus slave interface
P14	F003AE00 <sub>H</sub>	F003AEFF <sub>H</sub>	SPB bus slave interface
P15	F003AF00 <sub>H</sub>	F003AFFF <sub>H</sub>	SPB bus slave interface
P20	F003B400 <sub>H</sub>	F003B4FF <sub>H</sub>	SPB bus slave interface
P21	F003B500 <sub>H</sub>	F003B5FF <sub>H</sub>	SPB bus slave interface
P22	F003B600 <sub>H</sub>	F003B6FF <sub>H</sub>	SPB bus slave interface
P23	F003B700 <sub>H</sub>	F003B7FF <sub>H</sub>	SPB bus slave interface
P24	F003B800 <sub>H</sub>	F003B8FF <sub>H</sub>	SPB bus slave interface
P25	F003B900 <sub>H</sub>	F003B9FF <sub>H</sub>	SPB bus slave interface
P26	F003BA00 <sub>H</sub>	F003BAFF <sub>H</sub>	SPB bus slave interface
P30	F003BE00 <sub>H</sub>	F003BEFF <sub>H</sub>	SPB bus slave interface
P31	F003BF00 <sub>H</sub>	F003BFFF <sub>H</sub>	SPB bus slave interface
P32	F003C000 <sub>H</sub>	F003C0FF <sub>H</sub>	SPB bus slave interface
P33	F003C100 <sub>H</sub>	F003C1FF <sub>H</sub>	SPB bus slave interface
P34	F003C200 <sub>H</sub>	F003C2FF <sub>H</sub>	SPB bus slave interface
P40	F003C800 <sub>H</sub>	F003C8FF <sub>H</sub>	SPB bus slave interface
P41	F003C900 <sub>H</sub>	F003C9FF <sub>H</sub>	SPB bus slave interface

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### Register Overview Tables of Pn

**Table 90 Register Overview - P00 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P00_OUT	Port 00 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">39</a>
P00_OMR	Port 00 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">44</a>
P00_ID	Port 00 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">49</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P00_IOCR0	Port 00 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">52</a>	<a href="#">52</a>
P00_IOCR4	Port 00 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">58</a>	<a href="#">58</a>
P00_IOCR8	Port 00 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">63</a>	<a href="#">63</a>
P00_IOCR12	Port 00 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">67</a>	<a href="#">67</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P00_IN	Port 00 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">71</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x*4	BE	BE		
P00_PDR0	Port 00 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">75</a>	<a href="#">75</a>
P00_PDR1	Port 00 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">82</a>	<a href="#">82</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x*4	BE	BE		
P00_ESR	Port 00 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<a href="#">87</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x*4	BE	BE		
P00_PDISC	Port 00 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">94</a>	<a href="#">94</a>
P00_PCSR	Port 00 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">102</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x*4	BE	BE		
P00_OMSR0	Port 00 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">110</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 90 Register Overview - P00 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P00_OMSR4	Port 00 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">114</a>
P00_OMSR8	Port 00 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">118</a>
P00_OMSR12	Port 00 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">120</a>
P00_OMCR0	Port 00 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">123</a>
P00_OMCR4	Port 00 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">127</a>
P00_OMCR8	Port 00 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">130</a>
P00_OMCR12	Port 00 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">133</a>
P00_OMSR	Port 00 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">136</a>
P00_OMCR	Port 00 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P00_ACCEN1	Port 00 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">154</a>
P00_ACCENO	Port 00 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">158</a>

**Table 91 Register Overview - P01 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P01_OUT	Port 01 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">39</a>
P01_OMR	Port 01 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">44</a>
P01_ID	Port 01 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">49</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P01_IOCRO	Port 01 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">52</a>	<a href="#">52</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 91 Register Overview - P01 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P01_IOCR4	Port 01 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page 58	58
P01_IOCR8	Port 01 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page 63	63
P01_IOCR12	Port 01 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page 67	67
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P01_IN	Port 01 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	71
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x*4	BE	BE		
P01_PDR0	Port 01 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page 75	75
P01_PDR1	Port 01 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page 82	82
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x*4	BE	BE		
P01_ESR	Port 01 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	87
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x*4	BE	BE		
P01_PDISC	Port 01 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page 94	94
P01_PCSR	Port 01 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	103
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x*4	BE	BE		
P01_OMSR0	Port 01 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	110
P01_OMSR4	Port 01 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	114
P01_OMSR8	Port 01 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	118
P01_OMSR12	Port 01 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	120
P01_OMCR0	Port 01 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	123
P01_OMCR4	Port 01 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	127
P01_OMCR8	Port 01 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	130

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 91 Register Overview - P01 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P01_OMCR12	Port 01 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">133</a>
P01_OMSR	Port 01 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">136</a>
P01_OMCR	Port 01 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P01_ACCEN1	Port 01 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">154</a>
P01_ACCENO	Port 01 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">158</a>

**Table 92 Register Overview - P02 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P02_OUT	Port 02 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">39</a>
P02_OMR	Port 02 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">44</a>
P02_ID	Port 02 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">49</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P02_IOCR0	Port 02 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">52</a>	<a href="#">52</a>
P02_IOCR4	Port 02 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">58</a>	<a href="#">58</a>
P02_IOCR8	Port 02 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">63</a>	<a href="#">63</a>
P02_IOCR12	Port 02 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">67</a>	<a href="#">67</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P02_IN	Port 02 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">71</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P02_PDR0	Port 02 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">75</a>	<a href="#">75</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 92 Register Overview - P02 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P02_PDR1	Port 02 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page 82	<b>82</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P02_ESR	Port 02 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>87</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P02_PDISC	Port 02 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page 94	<b>94</b>
P02_PCSR	Port 02 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>103</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P02_OMSR0	Port 02 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>110</b>
P02_OMSR4	Port 02 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>114</b>
P02_OMSR8	Port 02 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>118</b>
P02_OMSR12	Port 02 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>120</b>
P02_OMCR0	Port 02 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>123</b>
P02_OMCR4	Port 02 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>127</b>
P02_OMCR8	Port 02 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>130</b>
P02_OMCR12	Port 02 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>133</b>
P02_OMSR	Port 02 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>136</b>
P02_OMCR	Port 02 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>140</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 92 Register Overview - P02 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P02_ACCEN1	Port 02 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>154</b>
P02_ACCENO	Port 02 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>158</b>

**Table 93 Register Overview - P10 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P10_OUT	Port 10 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>39</b>
P10_OMR	Port 10 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>44</b>
P10_ID	Port 10 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>49</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P10_IOCR0	Port 10 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>52</b>	<b>52</b>
P10_IOCR4	Port 10 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>58</b>	<b>58</b>
P10_IOCR8	Port 10 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>63</b>	<b>63</b>
P10_IOCR12	Port 10 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <b>67</b>	<b>67</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P10_IN	Port 10 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>71</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x*4	BE	BE		
P10_PDR0	Port 10 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>75</b>	<b>75</b>
P10_PDR1	Port 10 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>82</b>	<b>82</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x*4	BE	BE		
P10_ESR	Port 10 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>87</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x*4	BE	BE		
P10_PDISC	Port 10 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>94</b>	<b>94</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 93 Register Overview - P10 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P10_PCSR	Port 10 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">103</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P10_OMSR0	Port 10 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">110</a>
P10_OMSR4	Port 10 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">114</a>
P10_OMSR8	Port 10 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">118</a>
P10_OMSR12	Port 10 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">120</a>
P10_OMCR0	Port 10 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">123</a>
P10_OMCR4	Port 10 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">127</a>
P10_OMCR8	Port 10 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">130</a>
P10_OMCR12	Port 10 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">133</a>
P10_OMSR	Port 10 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">136</a>
P10_OMCR	Port 10 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P10_ACCEN1	Port 10 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">154</a>
P10_ACCENO	Port 10 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">158</a>

**Table 94 Register Overview - P11 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P11_OUT	Port 11 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">39</a>
P11_OMR	Port 11 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">44</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 94 Register Overview - P11 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P11_ID	Port 11 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>49</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P11_IOCR0	Port 11 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>52</b>	<b>52</b>
P11_IOCR4	Port 11 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>58</b>	<b>58</b>
P11_IOCR8	Port 11 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>63</b>	<b>63</b>
P11_IOCR12	Port 11 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <b>67</b>	<b>67</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P11_IN	Port 11 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>71</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x*4	BE	BE		
P11_PDR0	Port 11 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>75</b>	<b>75</b>
P11_PDR1	Port 11 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>82</b>	<b>82</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x*4	BE	BE		
P11_ESR	Port 11 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>87</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x*4	BE	BE		
P11_PDISC	Port 11 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>94</b>	<b>94</b>
P11_PCSR	Port 11 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>105</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x*4	BE	BE		
P11_OMSR0	Port 11 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>110</b>
P11_OMSR4	Port 11 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>114</b>
P11_OMSR8	Port 11 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>118</b>
P11_OMSR12	Port 11 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>120</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 94 Register Overview - P11 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P11_OMCR0	Port 11 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">123</a>
P11_OMCR4	Port 11 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">127</a>
P11_OMCR8	Port 11 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">130</a>
P11_OMCR12	Port 11 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">133</a>
P11_OMSR	Port 11 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">136</a>
P11_OMCR	Port 11 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P11_ACCEN1	Port 11 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">154</a>
P11_ACCENO	Port 11 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">158</a>

**Table 95 Register Overview - P12 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P12_OUT	Port 12 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">41</a>
P12_OMR	Port 12 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">46</a>
P12_ID	Port 12 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">49</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P12_IOCR0	Port 12 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">52</a>	<a href="#">52</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P12_IN	Port 12 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">73</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P12_PDR0	Port 12 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">80</a>	<a href="#">80</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 95 Register Overview - P12 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P12_ESR	Port 12 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>90</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P12_PDISC	Port 12 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>98</b>	<b>98</b>
P12_PCSR	Port 12 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>106</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P12_OMSR0	Port 12 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>110</b>
P12_OMCR0	Port 12 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>123</b>
P12_OMSR	Port 12 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>138</b>
P12_OMCR	Port 12 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>143</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P12_ACCEN1	Port 12 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>154</b>
P12_ACCENO	Port 12 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>158</b>

**Table 96 Register Overview - P13 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P13_OUT	Port 13 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>39</b>
P13_OMR	Port 13 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>44</b>
P13_ID	Port 13 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>49</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 96 Register Overview - P13 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P13_IOCR0	Port 13 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page 52	52
P13_IOCR4	Port 13 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page 58	58
P13_IOCR8	Port 13 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page 63	63
P13_IOCR12	Port 13 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page 67	67
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P13_IN	Port 13 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	71
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x*4	BE	BE		
P13_PDR0	Port 13 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page 75	75
P13_PDR1	Port 13 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page 82	82
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x*4	BE	BE		
P13_ESR	Port 13 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	87
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x*4	BE	BE		
P13_PDISC	Port 13 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page 94	94
P13_PCSR	Port 13 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	103
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x*4	BE	BE		
P13_OMSR0	Port 13 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	110
P13_OMSR4	Port 13 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	114
P13_OMSR8	Port 13 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	118
P13_OMSR12	Port 13 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	120
P13_OMCR0	Port 13 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	123
P13_OMCR4	Port 13 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	127

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 96 Register Overview - P13 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P13_OMCR8	Port 13 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>130</b>
P13_OMCR12	Port 13 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>133</b>
P13_OMSR	Port 13 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>136</b>
P13_OMCR	Port 13 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>140</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
P13_LPCR <sub>x</sub>	Port 13 LVDS Pad Control Register x	0A0 <sub>H</sub> +x* 4	U,SV	SV,E,P	See page <b>145</b>	<b>145</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P13_ACCEN1	Port 13 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>154</b>
P13_ACCEN0	Port 13 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>158</b>

**Table 97 Register Overview - P14 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P14_OUT	Port 14 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>39</b>
P14_OMR	Port 14 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>44</b>
P14_ID	Port 14 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>49</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P14_IOCR0	Port 14 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>52</b>	<b>52</b>
P14_IOCR4	Port 14 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>58</b>	<b>58</b>
P14_IOCR8	Port 14 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>63</b>	<b>63</b>
P14_IOCR12	Port 14 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <b>67</b>	<b>67</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P14_IN	Port 14 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>71</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 97 Register Overview - P14 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P14_PDR0	Port 14 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page 75	75
P14_PDR1	Port 14 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page 82	82
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P14_ESR	Port 14 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	87
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P14_PDISC	Port 14 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page 94	94
P14_PCSR	Port 14 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	103
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P14_OMSR0	Port 14 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	110
P14_OMSR4	Port 14 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	114
P14_OMSR8	Port 14 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	118
P14_OMSR12	Port 14 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	120
P14_OMCR0	Port 14 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	123
P14_OMCR4	Port 14 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	127
P14_OMCR8	Port 14 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	130
P14_OMCR12	Port 14 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	133
P14_OMSR	Port 14 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	136
P14_OMCR	Port 14 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	140
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 97 Register Overview - P14 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P14_LPCR <sub>x</sub>	Port 14 LVDS Pad Control Register x	0A0 <sub>H</sub> +x* 4	U,SV	SV,E,P	See page 148	148
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P14_ACCEN1	Port 14 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	154
P14_ACCEN0	Port 14 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	158

**Table 98 Register Overview - P15 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P15_OUT	Port 15 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	39
P15_OMR	Port 15 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	44
P15_ID	Port 15 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	49
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P15_IOCR0	Port 15 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page 52	52
P15_IOCR4	Port 15 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page 58	58
P15_IOCR8	Port 15 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page 63	63
P15_IOCR12	Port 15 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page 67	67
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P15_IN	Port 15 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	71
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P15_PDR0	Port 15 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page 75	75
P15_PDR1	Port 15 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page 82	82
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P15_ESR	Port 15 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	87

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 98 Register Overview - P15 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P15_PDISC	Port 15 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page 94	94
P15_PCSR	Port 15 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	103
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P15_OMSR0	Port 15 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	110
P15_OMSR4	Port 15 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	114
P15_OMSR8	Port 15 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	118
P15_OMSR12	Port 15 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	120
P15_OMCR0	Port 15 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	123
P15_OMCR4	Port 15 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	127
P15_OMCR8	Port 15 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	130
P15_OMCR12	Port 15 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	133
P15_OMSR	Port 15 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	136
P15_OMCR	Port 15 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	140
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
P15_LPCR <sub>x</sub>	Port 15 LVDS Pad Control Register x	0A0 <sub>H</sub> +x* 4	U,SV	SV,E,P	See page 145	145
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P15_ACCEN1	Port 15 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	154
P15_ACCENO	Port 15 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	158

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 99 Register Overview - P20 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P20_OUT	Port 20 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>39</b>
P20_OMR	Port 20 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>44</b>
P20_ID	Port 20 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>49</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P20_IOCR0	Port 20 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>52</b>	<b>52</b>
P20_IOCR4	Port 20 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>58</b>	<b>58</b>
P20_IOCR8	Port 20 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>63</b>	<b>63</b>
P20_IOCR12	Port 20 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <b>67</b>	<b>67</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P20_IN	Port 20 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>71</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P20_PDR0	Port 20 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>75</b>	<b>75</b>
P20_PDR1	Port 20 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>82</b>	<b>82</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P20_ESR	Port 20 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>87</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P20_PDISC	Port 20 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>94</b>	<b>94</b>
P20_PCSR	Port 20 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>103</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P20_OMSR0	Port 20 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>110</b>
P20_OMSR4	Port 20 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>114</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 99 Register Overview - P20 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P20_OMSR8	Port 20 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">118</a>
P20_OMSR12	Port 20 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">120</a>
P20_OMCR0	Port 20 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">123</a>
P20_OMCR4	Port 20 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">127</a>
P20_OMCR8	Port 20 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">130</a>
P20_OMCR12	Port 20 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">133</a>
P20_OMSR	Port 20 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">136</a>
P20_OMCR	Port 20 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P20_ACCEN1	Port 20 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">154</a>
P20_ACCEN0	Port 20 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">158</a>

**Table 100 Register Overview - P21 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P21_OUT	Port 21 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">42</a>
P21_OMR	Port 21 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">47</a>
P21_ID	Port 21 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">51</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P21_IOCR0	Port 21 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">56</a>	<a href="#">56</a>
P21_IOCR4	Port 21 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">58</a>	<a href="#">58</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 100 Register Overview - P21 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P21_IN	Port 21 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">74</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P21_PDR0	Port 21 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">75</a>	<a href="#">75</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P21_ESR	Port 21 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<a href="#">91</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P21_PDISC	Port 21 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">99</a>	<a href="#">99</a>
P21_PCSR	Port 21 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">106</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P21_OMSR0	Port 21 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">112</a>
P21_OMSR4	Port 21 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">114</a>
P21_OMCR0	Port 21 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">125</a>
P21_OMCR4	Port 21 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">127</a>
P21_OMSR	Port 21 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">139</a>
P21_OMCR	Port 21 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">144</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
P21_LPCR <sub>x</sub>	Port 21 LVDS Pad Control Register x	0A0 <sub>H</sub> +x* 4	U,SV	SV,E,P	See page <a href="#">149</a>	<a href="#">149</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P21_ACCEN1	Port 21 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">156</a>
P21_ACCEN0	Port 21 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">160</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 101 Register Overview - P22 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P22_OUT	Port 22 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>43</b>
P22_OMR	Port 22 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>48</b>
P22_ID	Port 22 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>51</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P22_IOCR0	Port 22 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>56</b>	<b>56</b>
P22_IOCR4	Port 22 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>61</b>	<b>61</b>
P22_IOCR8	Port 22 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>63</b>	<b>63</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P22_IN	Port 22 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>74</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P22_PDR0	Port 22 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>78</b>	<b>78</b>
P22_PDR1	Port 22 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>85</b>	<b>85</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P22_ESR	Port 22 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>91</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P22_PDISC	Port 22 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>100</b>	<b>100</b>
P22_PCSR	Port 22 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>107</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P22_OMSR0	Port 22 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>112</b>
P22_OMSR4	Port 22 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>116</b>
P22_OMSR8	Port 22 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>118</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 101 Register Overview - P22 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P22_OMCR0	Port 22 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">125</a>
P22_OMCR4	Port 22 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">129</a>
P22_OMCR8	Port 22 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">130</a>
P22_OMSR	Port 22 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
P22_OMCR	Port 22 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">145</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
P22_LPCR <sub>x</sub>	Port 22 LVDS Pad Control Register x	0A0 <sub>H</sub> +x* 4	U,SV	SV,E,P	See page <a href="#">145</a>	<a href="#">145</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P22_ACCEN1	Port 22 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">156</a>
P22_ACCEN0	Port 22 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">160</a>

**Table 102 Register Overview - P23 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P23_OUT	Port 23 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">42</a>
P23_OMR	Port 23 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">47</a>
P23_ID	Port 23 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">51</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P23_IOCR0	Port 23 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">56</a>	<a href="#">56</a>
P23_IOCR4	Port 23 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">61</a>	<a href="#">61</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P23_IN	Port 23 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">74</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 102 Register Overview - P23 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P23_PDR0	Port 23 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page 78	<b>78</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P23_ESR	Port 23 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>92</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P23_PDISC	Port 23 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page 99	<b>99</b>
P23_PCSR	Port 23 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>106</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P23_OMSR0	Port 23 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>112</b>
P23_OMSR4	Port 23 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>116</b>
P23_OMCR0	Port 23 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>125</b>
P23_OMCR4	Port 23 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>129</b>
P23_OMSR	Port 23 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>139</b>
P23_OMCR	Port 23 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>144</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P23_ACCEN1	Port 23 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>156</b>
P23_ACCENO	Port 23 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>160</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 103 Register Overview - P24 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P24_OUT	Port 24 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>39</b>
P24_OMR	Port 24 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>44</b>
P24_ID	Port 24 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>51</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P24_IOCR0	Port 24 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>56</b>	<b>56</b>
P24_IOCR4	Port 24 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>61</b>	<b>61</b>
P24_IOCR8	Port 24 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>66</b>	<b>66</b>
P24_IOCR12	Port 24 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <b>67</b>	<b>67</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P24_IN	Port 24 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>71</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P24_PDR0	Port 24 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>78</b>	<b>78</b>
P24_PDR1	Port 24 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>82</b>	<b>82</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P24_ESR	Port 24 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>87</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P24_PDISC	Port 24 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>94</b>	<b>94</b>
P24_PCSR	Port 24 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>103</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P24_OMSR0	Port 24 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>112</b>
P24_OMSR4	Port 24 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>116</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 103 Register Overview - P24 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P24_OMSR8	Port 24 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">119</a>
P24_OMSR12	Port 24 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">120</a>
P24_OMCR0	Port 24 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">125</a>
P24_OMCR4	Port 24 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">129</a>
P24_OMCR8	Port 24 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">132</a>
P24_OMCR12	Port 24 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">133</a>
P24_OMSR	Port 24 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">136</a>
P24_OMCR	Port 24 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P24_ACCEN1	Port 24 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">156</a>
P24_ACCEN0	Port 24 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">160</a>

**Table 104 Register Overview - P25 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P25_OUT	Port 25 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">40</a>
P25_OMR	Port 25 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">45</a>
P25_ID	Port 25 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">51</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P25_IOCR0	Port 25 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">56</a>	<a href="#">56</a>
P25_IOCR4	Port 25 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">61</a>	<a href="#">61</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 104 Register Overview - P25 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P25_IOCR8	Port 25 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">66</a>	<a href="#">66</a>
P25_IOCR12	Port 25 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">70</a>	<a href="#">70</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P25_IN	Port 25 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">73</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P25_PDR0	Port 25 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">78</a>	<a href="#">78</a>
P25_PDR1	Port 25 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">84</a>	<a href="#">84</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P25_ESR	Port 25 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<a href="#">89</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P25_PDISC	Port 25 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">97</a>	<a href="#">97</a>
P25_PCSR	Port 25 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">103</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P25_OMSR0	Port 25 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">112</a>
P25_OMSR4	Port 25 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">116</a>
P25_OMSR8	Port 25 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">119</a>
P25_OMSR12	Port 25 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">122</a>
P25_OMCR0	Port 25 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">125</a>
P25_OMCR4	Port 25 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">129</a>
P25_OMCR8	Port 25 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">132</a>
P25_OMCR12	Port 25 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">135</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 104 Register Overview - P25 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P25_OMSR	Port 25 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>137</b>
P25_OMCR	Port 25 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>142</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P25_ACCEN1	Port 25 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>156</b>
P25_ACCEN0	Port 25 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>160</b>

**Table 105 Register Overview - P26 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P26_OUT	Port 26 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>41</b>
P26_OMR	Port 26 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>46</b>
P26_ID	Port 26 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>51</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P26_IOCR0	Port 26 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>56</b>	<b>56</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P26_IN	Port 26 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>73</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P26_PDR0	Port 26 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>80</b>	<b>80</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P26_ESR	Port 26 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>90</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P26_PDISC	Port 26 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>98</b>	<b>98</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 105 Register Overview - P26 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P26_PCSR	Port 26 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">106</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P26_OMSR0	Port 26 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">112</a>
P26_OMCR0	Port 26 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">125</a>
P26_OMSR	Port 26 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">138</a>
P26_OMCR	Port 26 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">143</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P26_ACCEN1	Port 26 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">156</a>
P26_ACCEN0	Port 26 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">160</a>

**Table 106 Register Overview - P30 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P30_OUT	Port 30 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">40</a>
P30_OMR	Port 30 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">45</a>
P30_ID	Port 30 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">51</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P30_IOCR0	Port 30 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">56</a>	<a href="#">56</a>
P30_IOCR4	Port 30 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">61</a>	<a href="#">61</a>
P30_IOCR8	Port 30 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">66</a>	<a href="#">66</a>
P30_IOCR12	Port 30 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">70</a>	<a href="#">70</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 106 Register Overview - P30 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P30_IN	Port 30 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">73</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P30_PDR0	Port 30 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">78</a>	<a href="#">78</a>
P30_PDR1	Port 30 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">84</a>	<a href="#">84</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P30_ESR	Port 30 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<a href="#">89</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P30_PDISC	Port 30 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">97</a>	<a href="#">97</a>
P30_PCSR	Port 30 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">103</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P30_OMSR0	Port 30 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">112</a>
P30_OMSR4	Port 30 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">116</a>
P30_OMSR8	Port 30 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">119</a>
P30_OMSR12	Port 30 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">122</a>
P30_OMCR0	Port 30 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">125</a>
P30_OMCR4	Port 30 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">129</a>
P30_OMCR8	Port 30 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">132</a>
P30_OMCR12	Port 30 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">135</a>
P30_OMSR	Port 30 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">137</a>
P30_OMCR	Port 30 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">142</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 106 Register Overview - P30 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P30_ACCEN1	Port 30 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">156</a>
P30_ACCENO	Port 30 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">160</a>

**Table 107 Register Overview - P31 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P31_OUT	Port 31 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">40</a>
P31_OMR	Port 31 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">45</a>
P31_ID	Port 31 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">51</a>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P31_IOCR0	Port 31 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">56</a>	<a href="#">56</a>
P31_IOCR4	Port 31 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">61</a>	<a href="#">61</a>
P31_IOCR8	Port 31 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">66</a>	<a href="#">66</a>
P31_IOCR12	Port 31 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <a href="#">70</a>	<a href="#">70</a>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P31_IN	Port 31 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<a href="#">73</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P31_PDR0	Port 31 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">78</a>	<a href="#">78</a>
P31_PDR1	Port 31 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">84</a>	<a href="#">84</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P31_ESR	Port 31 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<a href="#">89</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 107 Register Overview - P31 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P31_PDISC	Port 31 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page 97	<b>97</b>
P31_PCSR	Port 31 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>104</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P31_OMSR0	Port 31 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>112</b>
P31_OMSR4	Port 31 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>116</b>
P31_OMSR8	Port 31 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>119</b>
P31_OMSR12	Port 31 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>122</b>
P31_OMCR0	Port 31 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>125</b>
P31_OMCR4	Port 31 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>129</b>
P31_OMCR8	Port 31 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>132</b>
P31_OMCR12	Port 31 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>135</b>
P31_OMSR	Port 31 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>137</b>
P31_OMCR	Port 31 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>142</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P31_ACCEN1	Port 31 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>156</b>
P31_ACCENO	Port 31 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>160</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 108 Register Overview - P32 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P32_OUT	Port 32 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>42</b>
P32_OMR	Port 32 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>47</b>
P32_ID	Port 32 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>51</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P32_IOCR0	Port 32 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>56</b>	<b>56</b>
P32_IOCR4	Port 32 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>61</b>	<b>61</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P32_IN	Port 32 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>74</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P32_PDR0	Port 32 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>78</b>	<b>78</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P32_ESR	Port 32 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>92</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P32_PDISC	Port 32 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>99</b>	<b>99</b>
P32_PCSR	Port 32 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>106</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P32_OMSR0	Port 32 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>112</b>
P32_OMSR4	Port 32 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>116</b>
P32_OMCR0	Port 32 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>125</b>
P32_OMCR4	Port 32 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>129</b>
P32_OMSR	Port 32 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>139</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 108 Register Overview - P32 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P32_OMCR	Port 32 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>144</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P32_ACCEN1	Port 32 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>156</b>
P32_ACCEN0	Port 32 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>160</b>

**Table 109 Register Overview - P33 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P33_OUT	Port 33 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>40</b>
P33_OMR	Port 33 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>45</b>
P33_ID	Port 33 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>51</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P33_IOCR0	Port 33 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>56</b>	<b>56</b>
P33_IOCR4	Port 33 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>61</b>	<b>61</b>
P33_IOCR8	Port 33 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>66</b>	<b>66</b>
P33_IOCR12	Port 33 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <b>70</b>	<b>70</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P33_IN	Port 33 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>73</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P33_PDR0	Port 33 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>78</b>	<b>78</b>
P33_PDR1	Port 33 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>84</b>	<b>84</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 109 Register Overview - P33 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P33_ESR	Port 33 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<a href="#">93</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P33_PDISC	Port 33 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">97</a>	<a href="#">97</a>
P33_PCSR	Port 33 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">108</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P33_OMSR0	Port 33 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">112</a>
P33_OMSR4	Port 33 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">116</a>
P33_OMSR8	Port 33 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">119</a>
P33_OMSR12	Port 33 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">122</a>
P33_OMCR0	Port 33 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">125</a>
P33_OMCR4	Port 33 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">129</a>
P33_OMCR8	Port 33 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">132</a>
P33_OMCR12	Port 33 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">135</a>
P33_OMSR	Port 33 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">137</a>
P33_OMCR	Port 33 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">142</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P33_ACCEN1	Port 33 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">156</a>
P33_ACCENO	Port 33 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">160</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 110 Register Overview - P34 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P34_OUT	Port 34 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>42</b>
P34_OMR	Port 34 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>47</b>
P34_ID	Port 34 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>52</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P34_IOCR0	Port 34 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>57</b>	<b>57</b>
P34_IOCR4	Port 34 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>61</b>	<b>61</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P34_IN	Port 34 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>74</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P34_PDR0	Port 34 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>78</b>	<b>78</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P34_ESR	Port 34 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>92</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P34_PDISC	Port 34 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>99</b>	<b>99</b>
P34_PCSR	Port 34 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>109</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P34_OMSR0	Port 34 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>113</b>
P34_OMSR4	Port 34 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>116</b>
P34_OMCR0	Port 34 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>126</b>
P34_OMCR4	Port 34 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>129</b>
P34_OMSR	Port 34 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>139</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 110 Register Overview - P34 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P34_OMCR	Port 34 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>144</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x*4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x*4	BE	BE		
P34_ACCEN1	Port 34 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>157</b>
P34_ACCEN0	Port 34 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>161</b>

**Table 111 Register Overview - P40 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P40_OUT	Port 40 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>40</b>
P40_OMR	Port 40 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>45</b>
P40_ID	Port 40 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>52</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P40_IOCR0	Port 40 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>57</b>	<b>57</b>
P40_IOCR4	Port 40 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>61</b>	<b>61</b>
P40_IOCR8	Port 40 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>66</b>	<b>66</b>
P40_IOCR12	Port 40 Input/Output Control Register 12	01C <sub>H</sub>	U,SV	U,SV,P	See page <b>70</b>	<b>70</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P40_IN	Port 40 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>73</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x*4	BE	BE		
P40_PDR0	Port 40 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>78</b>	<b>78</b>
P40_PDR1	Port 40 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>84</b>	<b>84</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x*4	BE	BE		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 111 Register Overview - P40 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P40_ESR	Port 40 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<a href="#">94</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P40_PDISC	Port 40 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <a href="#">97</a>	<a href="#">97</a>
P40_PCSR	Port 40 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">110</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P40_OMSR0	Port 40 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">113</a>
P40_OMSR4	Port 40 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">116</a>
P40_OMSR8	Port 40 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">119</a>
P40_OMSR12	Port 40 Output Modification Set Register 12	07C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">122</a>
P40_OMCR0	Port 40 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">126</a>
P40_OMCR4	Port 40 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">129</a>
P40_OMCR8	Port 40 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">132</a>
P40_OMCR12	Port 40 Output Modification Clear Register 12	08C <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">135</a>
P40_OMSR	Port 40 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">137</a>
P40_OMCR	Port 40 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">142</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P40_ACCEN1	Port 40 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">157</a>
P40_ACCENO	Port 40 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">161</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 112 Register Overview - P41 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P41_OUT	Port 41 Output Register	000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>43</b>
P41_OMR	Port 41 Output Modification Register	004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>48</b>
P41_ID	Port 41 Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	<b>52</b>
	Reserved (004 <sub>H</sub> Byte)	00C <sub>H</sub>	BE	BE		
P41_IOCR0	Port 41 Input/Output Control Register 0	010 <sub>H</sub>	U,SV	U,SV,P	See page <b>57</b>	<b>57</b>
P41_IOCR4	Port 41 Input/Output Control Register 4	014 <sub>H</sub>	U,SV	U,SV,P	See page <b>62</b>	<b>62</b>
P41_IOCR8	Port 41 Input/Output Control Register 8	018 <sub>H</sub>	U,SV	U,SV,P	See page <b>66</b>	<b>66</b>
	Reserved (004 <sub>H</sub> Byte)	020 <sub>H</sub>	BE	BE		
P41_IN	Port 41 Input Register	024 <sub>H</sub>	U,SV	BE	Application Reset	<b>74</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-5)	028 <sub>H</sub> +x* 4	BE	BE		
P41_PDR0	Port 41 Pad Driver Mode Register 0	040 <sub>H</sub>	U,SV	SV,E,P	See page <b>80</b>	<b>80</b>
P41_PDR1	Port 41 Pad Driver Mode Register 1	044 <sub>H</sub>	U,SV	SV,E,P	See page <b>86</b>	<b>86</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	048 <sub>H</sub> +x* 4	BE	BE		
P41_ESR	Port 41 Emergency Stop Register	050 <sub>H</sub>	U,SV	SV,E,P	Application Reset	<b>94</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-2)	054 <sub>H</sub> +x* 4	BE	BE		
P41_PDISC	Port 41 Pin Function Decision Control Register	060 <sub>H</sub>	U,SV	SV,E,P	See page <b>101</b>	<b>101</b>
P41_PCSR	Port 41 Pin Controller Select Register	064 <sub>H</sub>	U,SV	SV,SE	Application Reset	<b>107</b>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	068 <sub>H</sub> +x* 4	BE	BE		
P41_OMSR0	Port 41 Output Modification Set Register 0	070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>113</b>
P41_OMSR4	Port 41 Output Modification Set Register 4	074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>117</b>
P41_OMSR8	Port 41 Output Modification Set Register 8	078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<b>119</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 112 Register Overview - P41 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
P41_OMCR0	Port 41 Output Modification Clear Register 0	080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">126</a>
P41_OMCR4	Port 41 Output Modification Clear Register 4	084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">130</a>
P41_OMCR8	Port 41 Output Modification Clear Register 8	088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">132</a>
P41_OMSR	Port 41 Output Modification Set Register	090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">140</a>
P41_OMCR	Port 41 Output Modification Clear Register	094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">145</a>
	Reserved (004 <sub>H</sub> Byte) (x=0-1)	098 <sub>H</sub> +x* 4	BE	BE		
	Reserved (004 <sub>H</sub> Byte) (x=0-13)	0C0 <sub>H</sub> +x* 4	BE	BE		
P41_ACCEN1	Port 41 Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">157</a>
P41_ACCENO	Port 41 Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	<a href="#">161</a>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### 14.3 Pn Registers

#### 14.3.1 SPB bus slave interface

##### Port 00 Output Register

The port output register determines the value of a GPIO pin when it is selected by Pn\_IOCRx as output. Writing a 0 to a Pn\_OUT.Px (x = 0-15) bit position delivers a low level at the corresponding output pin. A high level is output when the corresponding bit is written with a 1. Note that the bits of Pn\_OUT.Px can be individually set or cleared by writing appropriate values into the port output modification set register Pn\_OMSR or port output modification clear register Pn\_OMCR, respectively. The Pn\_OUT.Px bits can also be set, cleared or toggled with register Pn\_OMR within the same write operation.

##### P00\_OUT

**Port 00 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P01\_OUT

**Port 01 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P02\_OUT

**Port 02 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P10\_OUT

**Port 10 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P11\_OUT

**Port 11 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P13\_OUT

**Port 13 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P14\_OUT

**Port 14 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P15\_OUT

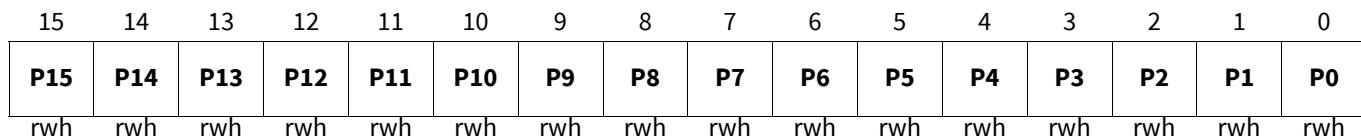
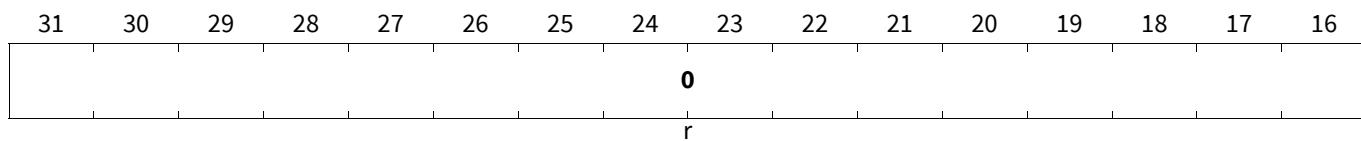
**Port 15 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P20\_OUT

**Port 20 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

##### P24\_OUT

**Port 24 Output Register** (000<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
Px (x=0-15)	x	rwh	<p><b>Output Bit x</b></p> <p>This bit determines the level at the output pin Pn.x if the output is selected as GPIO output.</p> <p>Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers.</p> <p>0<sub>B</sub> The output level of Pn.x is 0.</p> <p>1<sub>B</sub> The output level of Pn.x is 1.</p>
0	31:16	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

**Table 113 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OUT](#)

Applies to [P01\\_OUT](#)

Applies to [P02\\_OUT](#)

Applies to [P10\\_OUT](#)

Applies to [P11\\_OUT](#)

Applies to [P13\\_OUT](#)

Applies to [P14\\_OUT](#)

Applies to [P15\\_OUT](#)

Applies to [P20\\_OUT](#)

Applies to [P24\\_OUT](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-15)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-15)	

### P25\_OUT

**Port 25 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OUT

**Port 30 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OUT

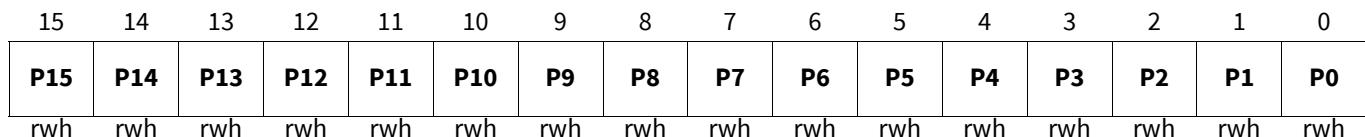
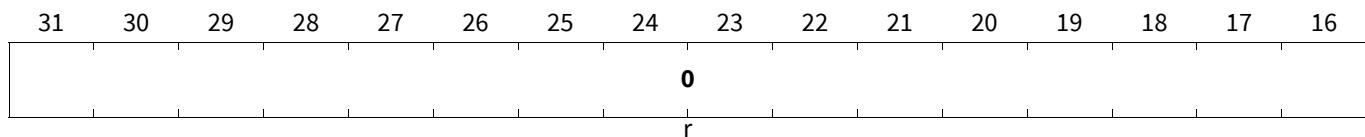
**Port 31 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OUT

**Port 33 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OUT

**Port 40 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
Px (x=0-15)	x	rwh	<p><b>Output Bit x</b></p> <p>This bit determines the level at the output pin Pn.x if the output is selected as GPIO output.</p> <p>Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers.</p> <p>0<sub>B</sub> The output level of Pn.x is 0. 1<sub>B</sub> The output level of Pn.x is 1.</p>
0	31:16	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

**Table 114 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_OUT](#)

Applies to [P30\\_OUT](#)

Applies to [P31\\_OUT](#)

Applies to [P33\\_OUT](#)

Applies to [P40\\_OUT](#)

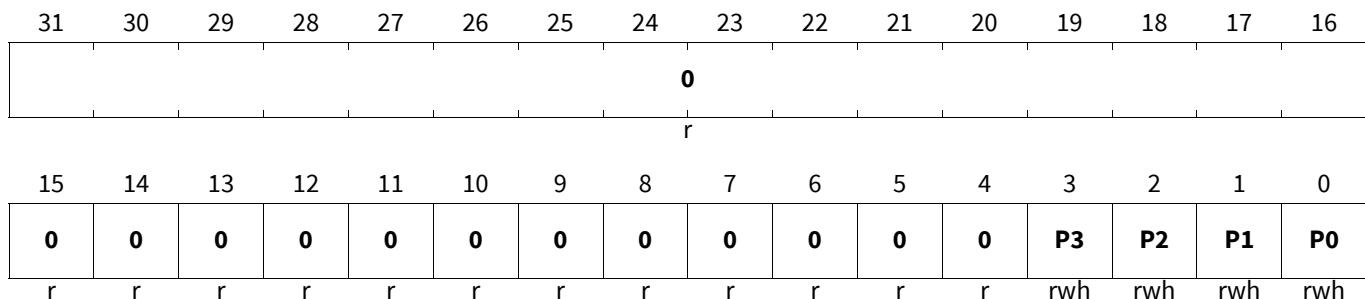
Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-15)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-15)	

### P12\_OUT

**Port 12 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P26\_OUT

**Port 26 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
Px (x=0-3)	x	rwh	<p><b>Output Bit x</b></p> <p>This bit determines the level at the output pin Pn.x if the output is selected as GPIO output.</p> <p>Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers.</p> <p>0<sub>B</sub> The output level of Pn.x is 0. 1<sub>B</sub> The output level of Pn.x is 1.</p>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 115 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_OUT](#)

Applies to [P26\\_OUT](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	rwh	Px (x=0-3)
Otherwise (default)	rh	Px (x=0-3)

### P21\_OUT

**Port 21 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_OUT

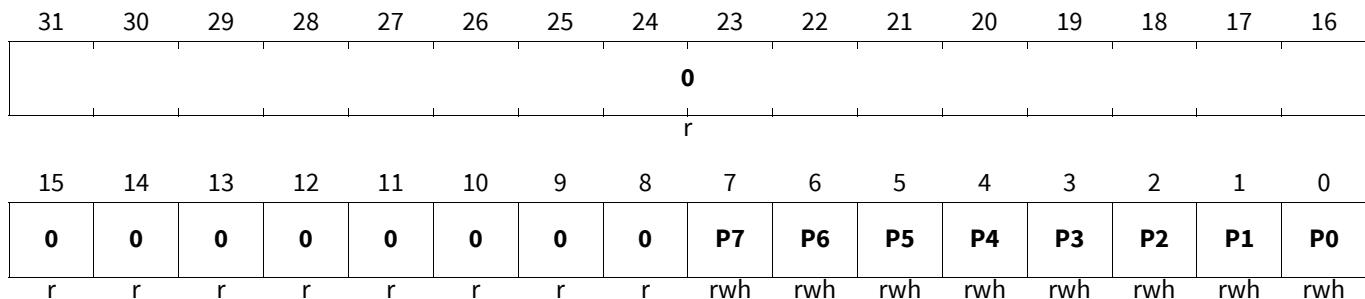
**Port 23 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_OUT

**Port 32 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P34\_OUT

**Port 34 Output Register** (000<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
Px (x=0-7)	x	rwh	<b>Output Bit x</b> This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0 <sub>B</sub> The output level of Pn.x is 0. 1 <sub>B</sub> The output level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 116 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_OUT](#)

Applies to [P23\\_OUT](#)

Applies to [P32\\_OUT](#)

Applies to [P34\\_OUT](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-7)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-7)	

### P22\_OUT

**Port 22 Output Register** (000<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

### P41\_OUT

**Port 41 Output Register** (000<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
r	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-11)	x	rwh	<b>Output Bit x</b> This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0 <sub>B</sub> The output level of Pn.x is 0. 1 <sub>B</sub> The output level of Pn.x is 1.
0	15, 14, 13, 12, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 117 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_OUT](#)

Applies to [P41\\_OUT](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-11)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-11)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### Port 00 Output Modification Register

The port output modification register contains control bits that make it possible to individually set, clear or toggle the logic state of a single port line by manipulating the output register.

#### P00\_OMR

<b>Port 00 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P01_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 01 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P02_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 02 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P10_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 10 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P11_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 11 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P13_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 13 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P14_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 14 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P15_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 15 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P20_OMR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 20 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P24_OMR</b>		
<b>Port 24 Output Modification Register</b>	(004 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>PCL15</b>	<b>PCL14</b>	<b>PCL13</b>	<b>PCL12</b>	<b>PCL11</b>	<b>PCL10</b>	<b>PCL9</b>	<b>PCL8</b>	<b>PCL7</b>	<b>PCL6</b>	<b>PCL5</b>	<b>PCL4</b>	<b>PCL3</b>	<b>PCL2</b>	<b>PCL1</b>	<b>PCL0</b>
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PS15</b>	<b>PS14</b>	<b>PS13</b>	<b>PS12</b>	<b>PS11</b>	<b>PS10</b>	<b>PS9</b>	<b>PS8</b>	<b>PS7</b>	<b>PS6</b>	<b>PS5</b>	<b>PS4</b>	<b>PS3</b>	<b>PS2</b>	<b>PS1</b>	<b>PS0</b>
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
<b>PSx (x=0-15)</b>	x	w0	<p><b>Set Bit x</b>            Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Sets or toggles Pn_OUT.Px.</p>
<b>PCLx (x=0-15)</b>	x+16	w0	<p><b>Clear Bit x</b>            Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Clears or toggles Pn_OUT.Px.</p>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 118 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMR](#)

Applies to [P01\\_OMR](#)

Applies to [P02\\_OMR](#)

Applies to [P10\\_OMR](#)

Applies to [P11\\_OMR](#)

Applies to [P13\\_OMR](#)

Applies to [P14\\_OMR](#)

Applies to [P15\\_OMR](#)

Applies to [P20\\_OMR](#)

Applies to [P24\\_OMR](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	w0	PCLx (x=0-15), PSx (x=0-15) write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15), PSx (x=0-15)

Note: Register  $Pn\_OMR$  is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

**Table 119 Function of the Bits PCLx and PSx**

PCLx	PSx	Function
0	0	Bit $Pn\_OUT.Px$ is not changed.
0	1	Bit $Pn\_OUT.Px$ is set.
1	0	Bit $Pn\_OUT.Px$ is reset.
1	1	Bit $Pn\_OUT.Px$ is toggled.

### P25\_OMR

**Port 25 Output Modification Register** [\*\*\(004<sub>H</sub>\)\*\*](#) **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMR

**Port 30 Output Modification Register** [\*\*\(004<sub>H</sub>\)\*\*](#) **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMR

**Port 31 Output Modification Register** [\*\*\(004<sub>H</sub>\)\*\*](#) **Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMR

**Port 33 Output Modification Register** [\*\*\(004<sub>H</sub>\)\*\*](#) **Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMR

**Port 40 Output Modification Register** [\*\*\(004<sub>H</sub>\)\*\*](#) **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>PCL15</b>	<b>PCL14</b>	<b>PCL13</b>	<b>PCL12</b>	<b>PCL11</b>	<b>PCL10</b>	<b>PCL9</b>	<b>PCL8</b>	<b>PCL7</b>	<b>PCL6</b>	<b>PCL5</b>	<b>PCL4</b>	<b>PCL3</b>	<b>PCL2</b>	<b>PCL1</b>	<b>PCL0</b>
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PS15</b>	<b>PS14</b>	<b>PS13</b>	<b>PS12</b>	<b>PS11</b>	<b>PS10</b>	<b>PS9</b>	<b>PS8</b>	<b>PS7</b>	<b>PS6</b>	<b>PS5</b>	<b>PS4</b>	<b>PS3</b>	<b>PS2</b>	<b>PS1</b>	<b>PS0</b>
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PSx (x=0-15)</b>	x	w0	<p><b>Set Bit x</b>            Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Sets or toggles Pn_OUT.Px.</p>
<b>PCLx (x=0-15)</b>	x+16	w0	<p><b>Clear Bit x</b>            Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Clears or toggles Pn_OUT.Px.</p>

**Table 120 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_OMR](#)

Applies to [P30\\_OMR](#)

Applies to [P31\\_OMR](#)

Applies to [P33\\_OMR](#)

Applies to [P40\\_OMR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-15), PSx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15), PSx (x=0-15)	

### P12\_OMR

**Port 12 Output Modification Register** (004<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P26\_OMR

**Port 26 Output Modification Register** (004<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	PCL3	PCL2	PCL1	PCL0
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PS3	PS2	PS1	PS0
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PSx (x=0-3)</b>	x	w0	<p><b>Set Bit x</b>            Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <b>Table 119</b>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Sets or toggles Pn_OUT.Px.</p>
<b>PCLx (x=0-3)</b>	x+16	w0	<p><b>Clear Bit x</b>            Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <b>Table 119</b>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Clears or toggles Pn_OUT.Px.</p>
<b>0</b>	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

**Table 121 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_OMR](#)

Applies to [P26\\_OMR](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	w0	PCLx (x=0-3), PSx (x=0-3) write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3), PSx (x=0-3)

### P21\_OMR

**Port 21 Output Modification Register** (004<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_OMR

**Port 23 Output Modification Register** (004<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_OMR

**Port 32 Output Modification Register** (004<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P34\_OMR

**Port 34 Output Modification Register** (004<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PSx (x=0-7)</b>	x	w0	<p><b>Set Bit x</b>            Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Sets or toggles Pn_OUT.Px.</p>
<b>PCLx (x=0-7)</b>	x+16	w0	<p><b>Clear Bit x</b>            Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p>0<sub>B</sub> No operation            1<sub>B</sub> Clears or toggles Pn_OUT.Px.</p>
<b>0</b>	15, 14, 13, 12, 11, 10, 9, 8, 31, 30, 29, 28, 27, 26, 25, 24	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

**Table 122 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_OMR](#)

Applies to [P23\\_OMR](#)

Applies to [P32\\_OMR](#)

Applies to [P34\\_OMR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-7), PSx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-7), PSx (x=0-7)	

### P22\_OMR

**Port 22 Output Modification Register** **Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_OMR

**Port 41 Output Modification Register** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>PCL11</b>	<b>PCL10</b>	<b>PCL9</b>	<b>PCL8</b>	<b>PCL7</b>	<b>PCL6</b>	<b>PCL5</b>	<b>PCL4</b>	<b>PCL3</b>	<b>PCL2</b>	<b>PCL1</b>	<b>PCL0</b>
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>PS11</b>	<b>PS10</b>	<b>PS9</b>	<b>PS8</b>	<b>PS7</b>	<b>PS6</b>	<b>PS5</b>	<b>PS4</b>	<b>PS3</b>	<b>PS2</b>	<b>PS1</b>	<b>PS0</b>
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PSx (x=0-11)</b>	x	w0	<p><b>Set Bit x</b>            Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p><math>0_B</math> No operation  <math>1_B</math> Sets or toggles Pn_OUT.Px.</p>
<b>PCLx (x=0-11)</b>	x+16	w0	<p><b>Clear Bit x</b>            Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in <a href="#">Table 119</a>.</p> <p><math>0_B</math> No operation  <math>1_B</math> Clears or toggles Pn_OUT.Px.</p>
<b>0</b>	15, 14, 13, 12, 31, 30, 29, 28	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

**Table 123 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_OMR](#)

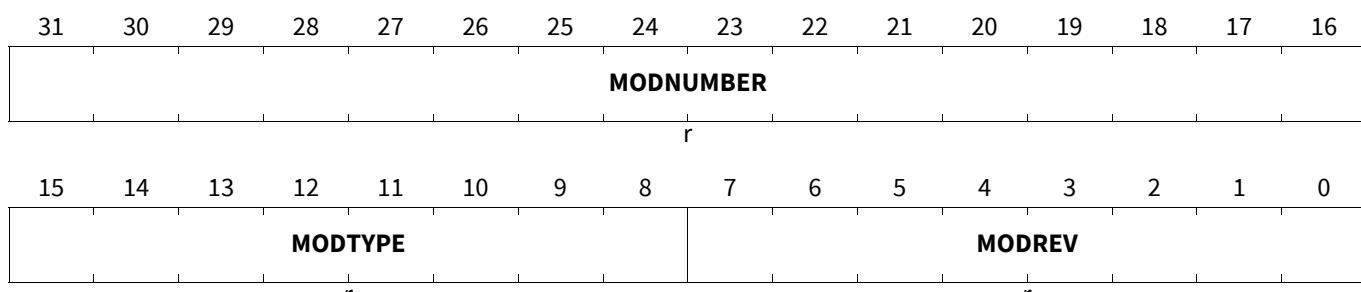
Applies to [P41\\_OMR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-11), PSx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-11), PSx (x=0-11)	

### Port 00 Identification Register

The module Identification Register ID contains read-only information about the module version.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**P00\_ID**
**Port 00 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P01\_ID**
**Port 01 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P02\_ID**
**Port 02 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P10\_ID**
**Port 10 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P11\_ID**
**Port 11 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P12\_ID**
**Port 12 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P13\_ID**
**Port 13 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P14\_ID**
**Port 14 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P15\_ID**
**Port 15 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**
**P20\_ID**
**Port 20 Identification Register** (008<sub>H</sub>) **Application Reset Value: 00C8 C0XX<sub>H</sub>**


Field	Bits	Type	Description
<b>MODREV</b>	7:0	r	<b>Module Revision Number</b> This bit field indicates the revision number of the TC39x-B module (01 <sub>H</sub> = first revision).
<b>MODTYPE</b>	15:8	r	<b>Module Type</b> This bit field is C0 <sub>H</sub> . It defines a 32-bit module
<b>MODNUMBER</b>	31:16	r	<b>Module Number</b> This bit field defines the module identification number. The value for the Ports module is 00C8 <sub>H</sub>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P21\_ID

**Port 21 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P22\_ID

**Port 22 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P23\_ID

**Port 23 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P24\_ID

**Port 24 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P25\_ID

**Port 25 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P26\_ID

**Port 26 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P30\_ID

**Port 30 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P31\_ID

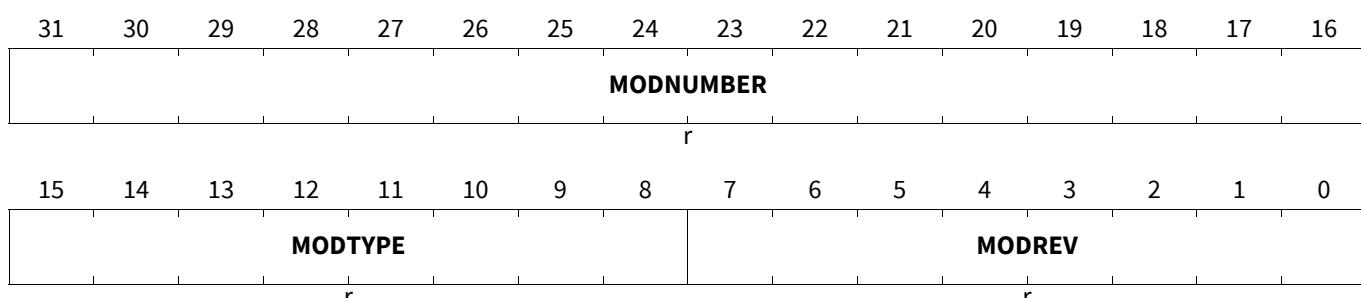
**Port 31 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P32\_ID

**Port 32 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>

### P33\_ID

**Port 33 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 COXX<sub>H</sub>



Field	Bits	Type	Description
<b>MODREV</b>	7:0	r	<b>Module Revision Number</b> This bit field indicates the revision number of the TC39x-B module (01 <sub>H</sub> = first revision).
<b>MODTYPE</b>	15:8	r	<b>Module Type</b> This bit field is C0 <sub>H</sub> . It defines a 32-bit module
<b>MODNUMBER</b>	31:16	r	<b>Module Number</b> This bit field defines the module identification number. The value for the Ports module is 00C8 <sub>H</sub>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P34\_ID

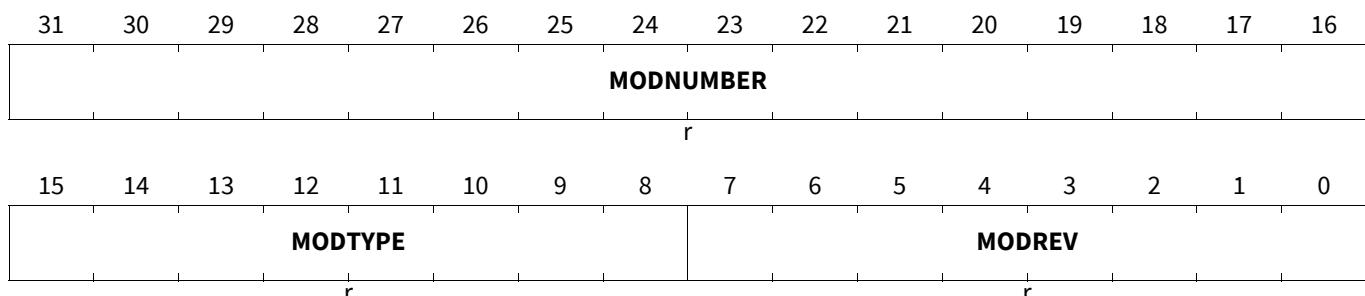
**Port 34 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 C0XX<sub>H</sub>

### P40\_ID

**Port 40 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 C0XX<sub>H</sub>

### P41\_ID

**Port 41 Identification Register** (008<sub>H</sub>) **Application Reset Value:** 00C8 C0XX<sub>H</sub>



Field	Bits	Type	Description
<b>MODREV</b>	7:0	r	<b>Module Revision Number</b> This bit field indicates the revision number of the TC39x-B module (01 <sub>H</sub> = first revision).
<b>MODTYPE</b>	15:8	r	<b>Module Type</b> This bit field is C0 <sub>H</sub> . It defines a 32-bit module
<b>MODNUMBER</b>	31:16	r	<b>Module Number</b> This bit field defines the module identification number. The value for the Ports module is 00C8 <sub>H</sub>

### Port 00 Input/Output Control Register 0

The port input/output control registers select the digital output and input driver functionality and characteristics of a GPIO port pin. Port direction (input or output), pull-up, pull-down, or no pull devices for inputs, and push-pull or open-drain functionality for outputs can be selected by the corresponding bit fields PCx (x = 0-15). Each 32-bit wide port input/output control register controls four GPIO port lines:

Register Pn\_IOCR0 controls the Pn.[3:0] port lines

Register Pn\_IOCR4 controls the Pn.[7:4] port lines

Register Pn\_IOCR8 controls the Pn.[11:8] port lines

Register Pn\_IOCR12 controls the Pn.[15:12] port lines

The structure with one control bit field for each port pin located in different register bytes offers the possibility to configure the port pin functionality of a single pin with byte-oriented accesses without accessing the other PCx bit fields.

The reset values of 1010 1010<sub>H</sub> and 0000 0000<sub>H</sub> for Pn\_IOCRx registers represents input pull-up and no input pull device (tri-state mode) being activated, respectively. The switching of the intended mode of the device is controlled by HWCFG6. When a cold reset is activated and HWCFG6=1, the port pins except P33.8, P40 and P41 are set to input pull-up mode, P33.8, P40 and P41 are in tri-state mode as long as PORST is activated. If HWCFG6=0, the pins have the default state of tri-state mode. The pad state can also be configured by software through PMSWCR5.TRISTREQ bit. In the event of a warm reset or wake-up from standby mode, PMSWCR5.TRISTREQ is not affected by reset, hence Pn\_IOCRx registers have the reset values configured as per the last state of the TRISTREQ bit.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Note: In LVDS (RX and TX) operation the IOCR register of both pins of the LVDS pair must be configured as output, i.e.  $1xxxx_B$ . This ensures that the pull devices are disconnected and don't interfere with LVDS operation.

Register Pn\_IOCR0 controls the Pn.[3:0] port lines

### P00\_IOCRO

**Port 00 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P01\_IOCRO

**Port 01 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P02\_IOCRO

**Port 02 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P10\_IOCRO

**Port 10 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P11\_IOCRO

**Port 11 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P12\_IOCRO

**Port 12 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P13\_IOCRO

**Port 13 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P14\_IOCRO

**Port 14 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P15\_IOCRO

**Port 15 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

### P20\_IOCRO

**Port 20 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 125](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC3				0				PC2				0			
rw				r				rw				r			
15				14				13				12			
PC1				0				7				PC0			
rw				r				rw				r			

Field	Bits	Type	Description
PCx (x=0-3)	8*x+7:8*x+3	rw	<b>Port Control for Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 124 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_IOCRO](#)

Applies to [P01\\_IOCRO](#)

Applies to [P02\\_IOCRO](#)

Applies to [P10\\_IOCRO](#)

Applies to [P11\\_IOCRO](#)

Applies to [P12\\_IOCRO](#)

Applies to [P13\\_IOCRO](#)

Applies to [P14\\_IOCRO](#)

Applies to [P15\\_IOCRO](#)

Applies to [P20\\_IOCRO](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PCx (x=0-3)	

**Table 125 Reset Values**

Applies to [P00\\_IOCRO](#)

Applies to [P01\\_IOCRO](#)

Applies to [P02\\_IOCRO](#)

Applies to [P10\\_IOCRO](#)

Applies to [P11\\_IOCRO](#)

Applies to [P12\\_IOCRO](#)

Applies to [P13\\_IOCRO](#)

Applies to [P14\\_IOCRO](#)

Applies to [P15\\_IOCRO](#)

Applies to [P20\\_IOCRO](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

### Port Control Coding

[Table 126](#) describes the coding of the PCx bit fields that determine the port line functionality.

**Table 126 PCx Coding**

PCx[4:0]	I/O	Characteristics	Selected Pull-up / Pull-down / Selected Output Function
0XX00 <sub>B</sub>	Input	-	No input pull device connected, tri-state mode
0XX01 <sub>B</sub>			Input pull-down device connected
0XX10 <sub>B</sub>			Input pull-up device connected <sup>1)</sup>
0XX11 <sub>B</sub>			No input pull device connected, tri-state mode

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 126 PCx Coding (cont'd)**

PCx[4:0]	I/O	Characteristics	Selected Pull-up / Pull-down / Selected Output Function
10000 <sub>B</sub>	Output	Push-pull	General-purpose output
10001 <sub>B</sub>			Alternate output function 1
10010 <sub>B</sub>			Alternate output function 2
10011 <sub>B</sub>			Alternate output function 3
10100 <sub>B</sub>			Alternate output function 4
10101 <sub>B</sub>			Alternate output function 5
10110 <sub>B</sub>			Alternate output function 6
10111 <sub>B</sub>			Alternate output function 7
11000 <sub>B</sub>	Open-drain	Open-drain	General-purpose output
11001 <sub>B</sub>			Alternate output function 1
11010 <sub>B</sub>			Alternate output function 2
11011 <sub>B</sub>			Alternate output function 3
11100 <sub>B</sub>			Alternate output function 4
11101 <sub>B</sub>			Alternate output function 5
11110 <sub>B</sub>			Alternate output function 6
11111 <sub>B</sub>			Alternate output function 7

1) This is the default pull device setting after reset for powertrain applications.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P21\_IOCR0

**Port 21 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P22\_IOCR0

**Port 22 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P23\_IOCR0

**Port 23 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P24\_IOCR0

**Port 24 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P25\_IOCR0

**Port 25 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P26\_IOCR0

**Port 26 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P30\_IOCR0

**Port 30 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P31\_IOCR0

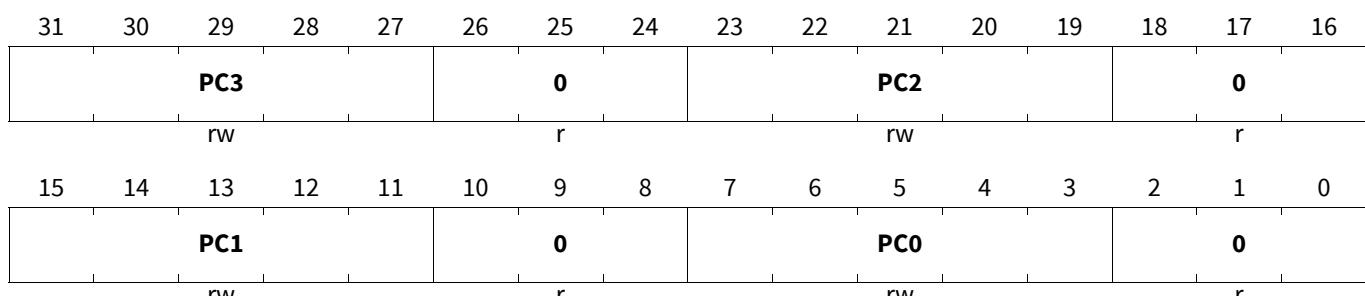
**Port 31 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P32\_IOCR0

**Port 32 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)

### P33\_IOCR0

**Port 33 Input/Output Control Register 0** (010<sub>H</sub>) **Reset Value:** [Table 128](#)



Field	Bits	Type	Description
PCx (x=0-3)	8*x+7:8*x+3	rw	<b>Port Control for Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 127 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_IOCRO](#)

Applies to [P22\\_IOCRO](#)

Applies to [P23\\_IOCRO](#)

Applies to [P24\\_IOCRO](#)

Applies to [P25\\_IOCRO](#)

Applies to [P26\\_IOCRO](#)

Applies to [P30\\_IOCRO](#)

Applies to [P31\\_IOCRO](#)

Applies to [P32\\_IOCRO](#)

Applies to [P33\\_IOCRO](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PCx (x=0-3)	

**Table 128 Reset Values**

Applies to [P21\\_IOCRO](#)

Applies to [P22\\_IOCRO](#)

Applies to [P23\\_IOCRO](#)

Applies to [P24\\_IOCRO](#)

Applies to [P25\\_IOCRO](#)

Applies to [P26\\_IOCRO](#)

Applies to [P30\\_IOCRO](#)

Applies to [P31\\_IOCRO](#)

Applies to [P32\\_IOCRO](#)

Applies to [P33\\_IOCRO](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

### P34\_IOCRO

**Port 34 Input/Output Control Register 0** (010<sub>H</sub>) Reset Value: [Table 130](#)

### P40\_IOCRO

**Port 40 Input/Output Control Register 0** (010<sub>H</sub>) Reset Value: [Table 131](#)

### P41\_IOCRO

**Port 41 Input/Output Control Register 0** (010<sub>H</sub>) Reset Value: [Table 131](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		PC3			0				PC2			0			
		rw			r				rw			r			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		PC1			0				PC0			0			
		rw			r				rw			r			

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCx (x=0-3)	8*x+7:8*x+3	rw	<b>Port Control for Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 129 Access Mode Restrictions sorted by descending priority**

Applies to [P34\\_IOCRO](#)

Applies to [P40\\_IOCRO](#)

Applies to [P41\\_IOCRO](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PCx (x=0-3)	

**Table 130 Reset Values of P34\_IOCRO**

Reset Type	Reset Value	Note
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

**Table 131 Reset Values variant 2**

Applies to [P40\\_IOCRO](#)

Applies to [P41\\_IOCRO](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

### Port 00 Input/Output Control Register 4

Register Pn\_IOCR4 controls the Pn.[7:4] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_IOC4

**Port 00 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P01\_IOC4

**Port 01 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P02\_IOC4

**Port 02 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P10\_IOC4

**Port 10 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P11\_IOC4

**Port 11 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P13\_IOC4

**Port 13 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P14\_IOC4

**Port 14 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P15\_IOC4

**Port 15 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P20\_IOC4

**Port 20 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

### P21\_IOC4

**Port 21 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 133](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		PC7			0			PC6				0			
rw				r				rw				r			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PC5				0			PC4				0			
rw				r				rw				r			

Field	Bits	Type	Description
PCx (x=4-7)	8*x-25:8*x-29	rw	<b>Port Control for Port 00 Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 132 Access Mode Restrictions sorted by descending priority**Applies to [P00\\_IOC4](#)Applies to [P01\\_IOC4](#)Applies to [P02\\_IOC4](#)Applies to [P10\\_IOC4](#)Applies to [P11\\_IOC4](#)Applies to [P13\\_IOC4](#)Applies to [P14\\_IOC4](#)Applies to [P15\\_IOC4](#)Applies to [P20\\_IOC4](#)Applies to [P21\\_IOC4](#)

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Master enabled in ACCEN	rw	PCx (x=4-7)	write access for enabled masters
Otherwise (default)	r	PCx (x=4-7)	

**Table 133 Reset Values**Applies to [P00\\_IOC4](#)Applies to [P01\\_IOC4](#)Applies to [P02\\_IOC4](#)Applies to [P10\\_IOC4](#)Applies to [P11\\_IOC4](#)Applies to [P13\\_IOC4](#)Applies to [P14\\_IOC4](#)Applies to [P15\\_IOC4](#)Applies to [P20\\_IOC4](#)Applies to [P21\\_IOC4](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P22\_IOCR4

**Port 22 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P23\_IOCR4

**Port 23 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P24\_IOCR4

**Port 24 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P25\_IOCR4

**Port 25 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P30\_IOCR4

**Port 30 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P31\_IOCR4

**Port 31 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P32\_IOCR4

**Port 32 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P33\_IOCR4

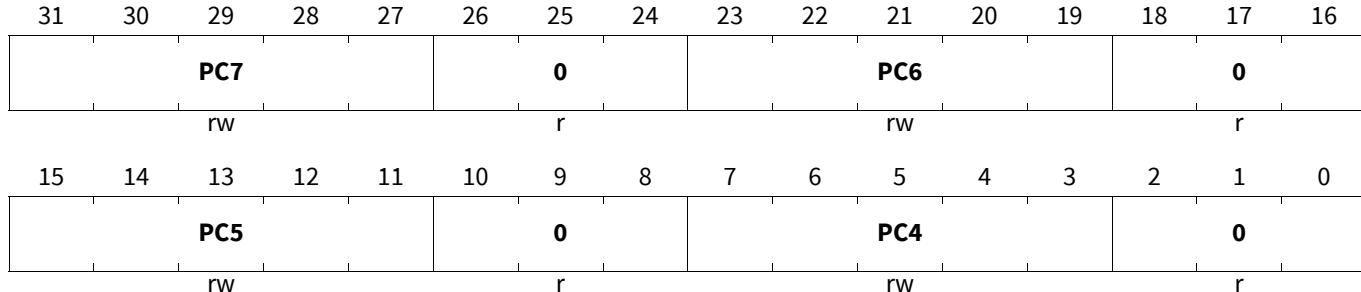
**Port 33 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P34\_IOCR4

**Port 34 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 135](#)

### P40\_IOCR4

**Port 40 Input/Output Control Register 4** (014<sub>H</sub>) **Reset Value:** [Table 136](#)



Field	Bits	Type	Description
<b>PCx (x=4-7)</b>	8*x-25:8*x-29	rw	<b>Port Control for Port 22 Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
<b>0</b>	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 134 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_IOC4](#)

Applies to [P23\\_IOC4](#)

Applies to [P24\\_IOC4](#)

Applies to [P25\\_IOC4](#)

Applies to [P30\\_IOC4](#)

Applies to [P31\\_IOC4](#)

Applies to [P32\\_IOC4](#)

Applies to [P33\\_IOC4](#)

Applies to [P34\\_IOC4](#)

Applies to [P40\\_IOC4](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	rw	PCx (x=4-7) write access for enabled masters
Otherwise (default)	r	PCx (x=4-7)

**Table 135 Reset Values variant 1**

Applies to [P22\\_IOC4](#)

Applies to [P23\\_IOC4](#)

Applies to [P24\\_IOC4](#)

Applies to [P25\\_IOC4](#)

Applies to [P30\\_IOC4](#)

Applies to [P31\\_IOC4](#)

Applies to [P32\\_IOC4](#)

Applies to [P33\\_IOC4](#)

Applies to [P34\\_IOC4](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

**Table 136 Reset Values of P40\_IOC4**

Reset Type	Reset Value	Note
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

### P41\_IOC4

#### Port 41 Input/Output Control Register 4

(014<sub>H</sub>)

Reset Value: [Table 138](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC7				0		PC6				0		r		r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC5				0		PC4				0		r		r	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCx (x=4-7)	8*x-25:8*x-29	rw	<b>Port Control for Port 41 Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 137 Access Mode Restrictions of P41\_IOCR4 sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=4-7)	write access for enabled masters
Otherwise (default)	r	PCx (x=4-7)	

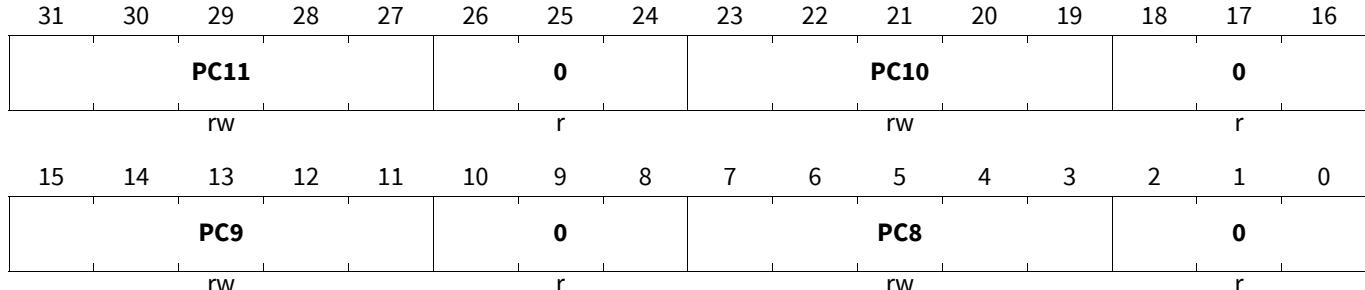
**Table 138 Reset Values of P41\_IOCR4**

Reset Type	Reset Value	Note
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0001 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

### Port 00 Input/Output Control Register 8

Register Pn\_IOCR8 controls the Pn.[11:8] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**P00\_IOC8**
**Port 00 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P01\_IOC8**
**Port 01 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P02\_IOC8**
**Port 02 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P10\_IOC8**
**Port 10 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P11\_IOC8**
**Port 11 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P13\_IOC8**
**Port 13 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P14\_IOC8**
**Port 14 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P15\_IOC8**
**Port 15 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P20\_IOC8**
**Port 20 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)
**P22\_IOC8**
**Port 22 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 140](#)


Field	Bits	Type	Description
<b>PCx (x=8-11)</b>	8*x-57:8*x-61	rw	<b>Port Control for Port 00 Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 139 Access Mode Restrictions sorted by descending priority**Applies to [P00\\_IOC8](#)Applies to [P01\\_IOC8](#)Applies to [P02\\_IOC8](#)Applies to [P10\\_IOC8](#)Applies to [P11\\_IOC8](#)Applies to [P13\\_IOC8](#)Applies to [P14\\_IOC8](#)Applies to [P15\\_IOC8](#)Applies to [P20\\_IOC8](#)Applies to [P22\\_IOC8](#)

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Master enabled in ACCEN	rw	PCx (x=8-11)	write access for enabled masters
Otherwise (default)	r	PCx (x=8-11)	

**Table 140 Reset Values**Applies to [P00\\_IOC8](#)Applies to [P01\\_IOC8](#)Applies to [P02\\_IOC8](#)Applies to [P10\\_IOC8](#)Applies to [P11\\_IOC8](#)Applies to [P13\\_IOC8](#)Applies to [P14\\_IOC8](#)Applies to [P15\\_IOC8](#)Applies to [P20\\_IOC8](#)Applies to [P22\\_IOC8](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P24\_IOCR8

**Port 24 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 142](#)

### P25\_IOCR8

**Port 25 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 142](#)

### P30\_IOCR8

**Port 30 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 142](#)

### P31\_IOCR8

**Port 31 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 142](#)

### P33\_IOCR8

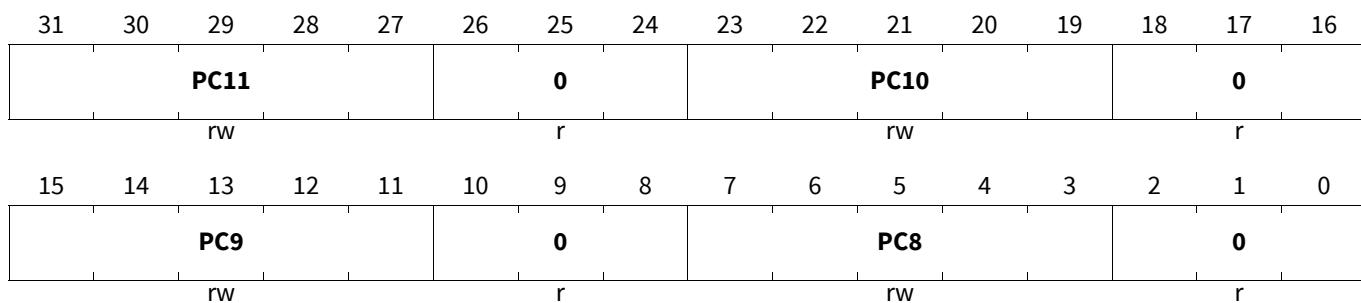
**Port 33 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 143](#)

### P40\_IOCR8

**Port 40 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 144](#)

### P41\_IOCR8

**Port 41 Input/Output Control Register 8** (018<sub>H</sub>) **Reset Value:** [Table 144](#)



Field	Bits	Type	Description
<b>PCx (x=8-11)</b>	8*x-57:8*x-61	rw	<b>Port Control for Port 24 Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 141 Access Mode Restrictions sorted by descending priority**

Applies to [P24\\_IOCR8](#)

Applies to [P25\\_IOCR8](#)

Applies to [P30\\_IOCR8](#)

Applies to [P31\\_IOCR8](#)

Applies to [P33\\_IOCR8](#)

Applies to [P40\\_IOCR8](#)

Applies to [P41\\_IOCR8](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=8-11)	write access for enabled masters
Otherwise (default)	r	PCx (x=8-11)	

---

**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 142 Reset Values variant 1**Applies to [P24\\_IOCR8](#)Applies to [P25\\_IOCR8](#)Applies to [P30\\_IOCR8](#)Applies to [P31\\_IOCR8](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

**Table 143 Reset Values of P33\_IOCR8**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1000 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

**Table 144 Reset Values variant 3**Applies to [P40\\_IOCR8](#)Applies to [P41\\_IOCR8](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

**Port 00 Input/Output Control Register 12**

Register Pn\_IOCR12 controls the Pn.[15:12] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_IOC12

**Port 00 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P01\_IOC12

**Port 01 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P02\_IOC12

**Port 02 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P10\_IOC12

**Port 10 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P11\_IOC12

**Port 11 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P13\_IOC12

**Port 13 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P14\_IOC12

**Port 14 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P15\_IOC12

**Port 15 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P20\_IOC12

**Port 20 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

### P24\_IOC12

**Port 24 Input/Output Control Register 12** (01C<sub>H</sub>) **Reset Value:** [Table 146](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>PC15</b>				0		<b>PC14</b>				0		0			
							r								r
rw				r		rw				rw		r			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PC13</b>				0		<b>PC12</b>				0		0			
							r								r
rw				r		rw				r		r			

Field	Bits	Type	Description
<b>PCx (x=12-15)</b>	8*x-89:8*x-93	rw	<b>Port Control for Port 00 Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

---

**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 145 Access Mode Restrictions sorted by descending priority**Applies to [P00\\_IOC12](#)Applies to [P01\\_IOC12](#)Applies to [P02\\_IOC12](#)Applies to [P10\\_IOC12](#)Applies to [P11\\_IOC12](#)Applies to [P13\\_IOC12](#)Applies to [P14\\_IOC12](#)Applies to [P15\\_IOC12](#)Applies to [P20\\_IOC12](#)Applies to [P24\\_IOC12](#)

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Master enabled in ACCEN	rw	PCx (x=12-15)	write access for enabled masters
Otherwise (default)	r	PCx (x=12-15)	

**Table 146 Reset Values**Applies to [P00\\_IOC12](#)Applies to [P01\\_IOC12](#)Applies to [P02\\_IOC12](#)Applies to [P10\\_IOC12](#)Applies to [P11\\_IOC12](#)Applies to [P13\\_IOC12](#)Applies to [P14\\_IOC12](#)Applies to [P15\\_IOC12](#)Applies to [P20\\_IOC12](#)Applies to [P24\\_IOC12](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P25\_IOCR12

**Port 25 Input/Output Control Register 12** (01C<sub>H</sub>)

Reset Value: [Table 148](#)

### P30\_IOCR12

**Port 30 Input/Output Control Register 12** (01C<sub>H</sub>)

Reset Value: [Table 148](#)

### P31\_IOCR12

**Port 31 Input/Output Control Register 12** (01C<sub>H</sub>)

Reset Value: [Table 148](#)

### P33\_IOCR12

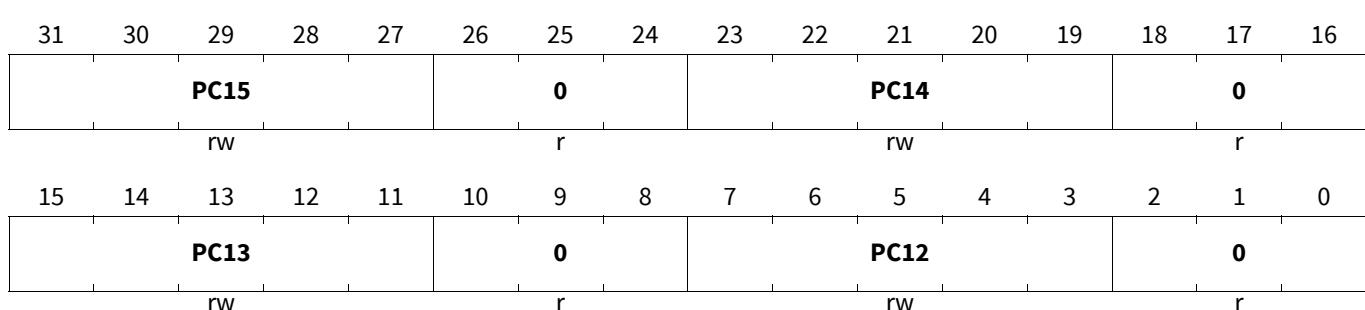
**Port 33 Input/Output Control Register 12** (01C<sub>H</sub>)

Reset Value: [Table 148](#)

### P40\_IOCR12

**Port 40 Input/Output Control Register 12** (01C<sub>H</sub>)

Reset Value: [Table 149](#)



Field	Bits	Type	Description
<b>PCx (x=12-15)</b>	8*x-89:8*x-93	rw	<b>Port Control for Port 25 Pin x</b> This bit field defines the Port n line x functionality according to <a href="#">Table 126</a> .
0	26:24, 18:16, 10:8, 2:0	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 147 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_IOCR12](#)

Applies to [P30\\_IOCR12](#)

Applies to [P31\\_IOCR12](#)

Applies to [P33\\_IOCR12](#)

Applies to [P40\\_IOCR12](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=12-15)	write access for enabled masters
Otherwise (default)	r	PCx (x=12-15)	

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**


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**Table 148 Reset Values variant 1**Applies to [P25\\_IOCR12](#)Applies to [P30\\_IOCR12](#)Applies to [P31\\_IOCR12](#)Applies to [P33\\_IOCR12](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

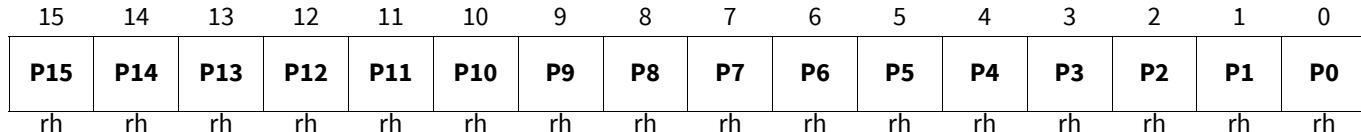
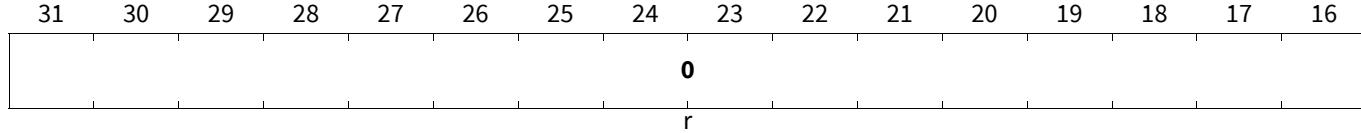
**Table 149 Reset Values of P40\_IOCR12**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0000 <sub>H</sub>	HWCFG6 is 1 (input pull-up mode)

**Port 00 Input Register**

The logic level of a GPIO pin can be read via the read-only port input register Pn\_IN. Reading the Pn\_IN register always returns the current logical value at the GPIO pin independently whether the pin is selected as input or output.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**P00\_IN**
**Port 00 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P01\_IN**
**Port 01 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P02\_IN**
**Port 02 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P10\_IN**
**Port 10 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P11\_IN**
**Port 11 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P13\_IN**
**Port 13 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P14\_IN**
**Port 14 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P15\_IN**
**Port 15 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P20\_IN**
**Port 20 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**
**P24\_IN**
**Port 24 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**


Field	Bits	Type	Description
<b>Px (x=0-15)</b>	x	rh	<b>Input Bit x</b> This bit indicates the level at the input pin Pn.x. 0 <sub>B</sub> The input level of Pn.x is 0. 1 <sub>B</sub> The input level of Pn.x is 1.
<b>0</b>	31:16	r	<b>Reserved</b> Read as 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P25\_IN

**Port 25 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**

### P30\_IN

**Port 30 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**

### P31\_IN

**Port 31 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**

### P33\_IN

**Port 33 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**

### P40\_IN

**Port 40 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 XXXX<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>P15</b>	<b>P14</b>	<b>P13</b>	<b>P12</b>	<b>P11</b>	<b>P10</b>	<b>P9</b>	<b>P8</b>	<b>P7</b>	<b>P6</b>	<b>P5</b>	<b>P4</b>	<b>P3</b>	<b>P2</b>	<b>P1</b>	<b>P0</b>
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
<b>Px (x=0-15)</b>	x	rh	<b>Input Bit x</b> This bit indicates the level at the input pin Pn.x. $0_B$ The input level of Pn.x is 0. $1_B$ The input level of Pn.x is 1.
<b>0</b>	31:16	r	<b>Reserved</b> Read as 0.

### P12\_IN

**Port 12 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 000X<sub>H</sub>**

### P26\_IN

**Port 26 Input Register** (024<sub>H</sub>) **Application Reset Value: 0000 000X<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>P3</b>	<b>P2</b>	<b>P1</b>	<b>P0</b>
r	r	r	r	r	r	r	r	r	r	r	r	rh	rh	rh	rh

Field	Bits	Type	Description
<b>Px (x=0-3)</b>	x	rh	<b>Input Bit x</b> This bit indicates the level at the input pin Pn.x. $0_B$ The input level of Pn.x is 0. $1_B$ The input level of Pn.x is 1.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

### P21\_IN

**Port 21 Input Register** (024<sub>H</sub>) Application Reset Value: 0000 00XX<sub>H</sub>

### P23\_IN

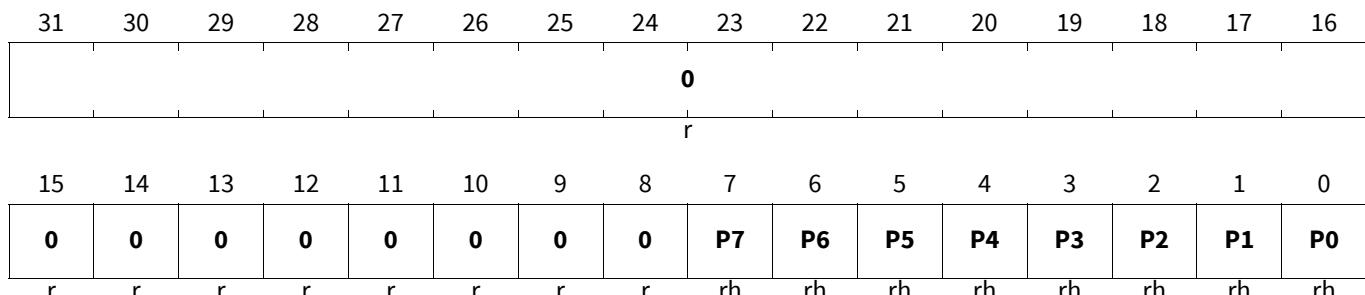
**Port 23 Input Register** (024<sub>H</sub>) Application Reset Value: 0000 00XX<sub>H</sub>

### P32\_IN

**Port 32 Input Register** (024<sub>H</sub>) Application Reset Value: 0000 00XX<sub>H</sub>

### P34\_IN

**Port 34 Input Register** (024<sub>H</sub>) Application Reset Value: 0000 00XX<sub>H</sub>



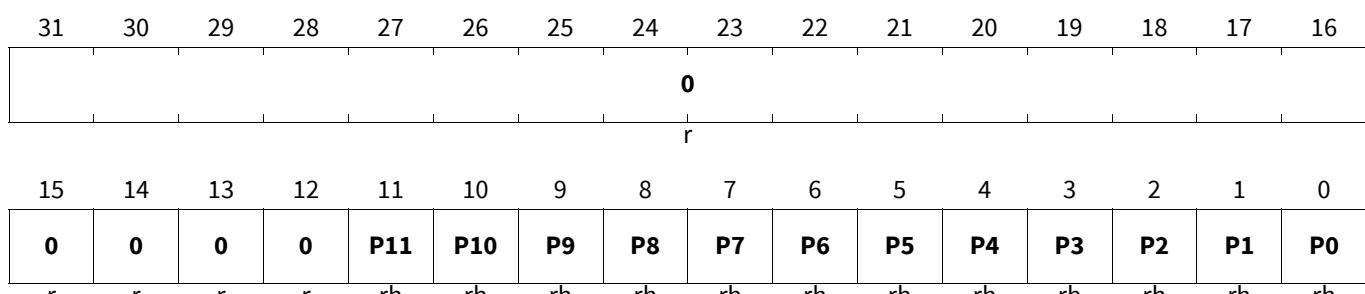
Field	Bits	Type	Description
Px (x=0-7)	x	rh	<b>Input Bit x</b> This bit indicates the level at the input pin Pn.x. $0_B$ The input level of Pn.x is 0. $1_B$ The input level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

### P22\_IN

**Port 22 Input Register** (024<sub>H</sub>) Application Reset Value: 0000 0XXX<sub>H</sub>

### P41\_IN

**Port 41 Input Register** (024<sub>H</sub>) Application Reset Value: 0000 0XXX<sub>H</sub>



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
Px (x=0-11)	x	rh	<b>Input Bit x</b> This bit indicates the level at the input pin Pn.x. $0_B$ The input level of Pn.x is 0. $1_B$ The input level of Pn.x is 1.
0	15, 14, 13, 12, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

### Port 00 Pad Driver Mode Register 0

#### P00\_PDR0

Port 00 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P01\_PDR0

Port 01 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P02\_PDR0

Port 02 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P10\_PDR0

Port 10 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P11\_PDR0

Port 11 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P13\_PDR0

Port 13 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P14\_PDR0

Port 14 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P15\_PDR0

Port 15 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P20\_PDR0

Port 20 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

#### P21\_PDR0

Port 21 Pad Driver Mode Register 0  $(040_H)$  Reset Value: [Table 151](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL7	PD7	PL6	PD6	PL5	PD5	PL4	PD4								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL3	PD3	PL2	PD2	PL1	PD1	PL0	PD0								

Field	Bits	Type	Description
PDx (x=0-7)	$4^*x+1:4^*x$	rw	<b>Pad Driver Mode for Pin x</b>
PLx (x=0-7)	$4^*x+3:4^*x+2$	rw	<b>Pad Level Selection for Pin x</b>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 150 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_PDR0](#)

Applies to [P01\\_PDR0](#)

Applies to [P02\\_PDR0](#)

Applies to [P10\\_PDR0](#)

Applies to [P11\\_PDR0](#)

Applies to [P13\\_PDR0](#)

Applies to [P14\\_PDR0](#)

Applies to [P15\\_PDR0](#)

Applies to [P20\\_PDR0](#)

Applies to [P21\\_PDR0](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-7), PLx (x=0-7)
Otherwise (default)	r	PDx (x=0-7), PLx (x=0-7)

**Table 151 Reset Values**

Applies to [P00\\_PDR0](#)

Applies to [P01\\_PDR0](#)

Applies to [P02\\_PDR0](#)

Applies to [P10\\_PDR0](#)

Applies to [P11\\_PDR0](#)

Applies to [P13\\_PDR0](#)

Applies to [P14\\_PDR0](#)

Applies to [P15\\_PDR0](#)

Applies to [P20\\_PDR0](#)

Applies to [P21\\_PDR0](#)

Reset Type	Reset Value	Note
After SSW execution	2222 2222 <sub>H</sub>	Initial value in largest package
After SSW execution	---- ---- <sub>H</sub>	Initial value package dependent

### Output Characteristics

The pad structure of the GPIO lines offers the possibility to select the output driver strength and the slew rate. These two parameters are controlled by the PDx bit fields in the pad driver mode registers Pn\_PDR0/1 for output modes. The available modes depend on the respective pad type.

**Table 152 Pad Driver Mode Selection for RFast Pads**

PDx.1	PDx.0	Speed Grade	Driver Setting
0	0	1	Strong driver, sharp edge ("ss")
0	1	2	Strong driver, medium edge ("sm")
1	0	3	Medium driver ("m")
1	1	4	RGMII driver.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 153 Pad Driver Mode Selection for Fast Pads**

PDx.1	PDx.0	Speed Grade	Driver Setting
0	0	1	Strong driver, sharp edge ("ss")
0	1	2	Strong driver, medium edge ("sm")
1	0	3	Medium driver ("m")
1	1	4	TC39x A-Step: Medium driver ("m") Else: Reserved when operating as output. When operating as input see below "Pad Level Selection for Input Function".

**Table 154 Pad Driver Mode Selection for Slow Pads**

PDx.1	PDx.0	Speed Grade	Driver Setting
X	0	1	Medium driver, sharp edge ("sm") <sup>1)</sup>
X	1	2	Medium driver ("m")

- 1) This setting is marked "sm" as the electrical characteristics are identical to the strong driver medium edge setting. The Data Sheet contains also only common "sm" tables.

Note: *The Data Sheet describes the DC characteristics of all pad classes.*

### TTL/Automotive Input Selection

The input function can operate with different VIH and VIL levels depending on the pad supply voltage, the pad type and the selection done by the PLx bits of the Pn\_PDRx as of [Table 155](#). PLx.1 changes additionally the pull-up and pull-down resistors.

**Table 155 Pad Level Selection for Input Function**

PLx.1	PLx.0	Input Levels
0	X	Automotive level "AL".
1	0	TTL level for 5V pad supply. Degraded TTL level used for CIF when pad supply is 3.3V
1	1	TTL level for 3.3V pad supply.
X	X	Only for pads with RGMII input buffer (marked "RGMII_Input" in the pinning table): <ul style="list-style-type: none"> <li>• when PDx.1=1 and PDx.0=1 the input level RGMII is selected.</li> <li>• for other PDx values the input level is determined by PLx as for all other pads (first three rows of this table).</li> </ul>

### LVDS

The default CMOS mode can be switched to LVDS mode in LVDS pads through the LPCRx register.

### Pad Driver Mode Registers

This is the general description of the PDR registers. Each port contains its own specific PDR registers, described additionally at each port, that can contain between one and eight PDx fields for PDR0 and PDR1 registers, respectively. Each PDx field controls 1 pin. For coding of PDx, see [Table 152](#), [Table 153](#) and [Table 154](#). Similarly, each PLx bit controls 1 pin. For coding of PLx, see [Table 155](#).

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

The boot software configures the reset value of Pn\_PDR0 and Pn\_PDR1 registers from 0000 0000<sub>H</sub> to 2222 2222<sub>H</sub> except for analog ports and if the package doesn't make any of the related pins available. The resulting value depends on the implemented port width. The documented value is valid for the largest package.

### P22\_PDR0

**Port 22 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P23\_PDR0

**Port 23 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P24\_PDR0

**Port 24 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P25\_PDR0

**Port 25 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P30\_PDR0

**Port 30 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P31\_PDR0

**Port 31 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P32\_PDR0

**Port 32 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P33\_PDR0

**Port 33 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P34\_PDR0

**Port 34 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 157](#)

### P40\_PDR0

**Port 40 Pad Driver Mode Register 0** (040<sub>H</sub>) **Reset Value:** [Table 158](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>PL7</b>	<b>PD7</b>	<b>PL6</b>	<b>PD6</b>	<b>PL5</b>	<b>PD5</b>	<b>PL4</b>	<b>PD4</b>								
rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PL3</b>	<b>PD3</b>	<b>PL2</b>	<b>PD2</b>	<b>PL1</b>	<b>PD1</b>	<b>PL0</b>	<b>PD0</b>								
rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>PDx (x=0-7)</b>	4*x+1:4*x	rw	<b>Pad Driver Mode for Pin x</b>
<b>PLx (x=0-7)</b>	4*x+3:4*x+2	rw	<b>Pad Level Selection for Pin x</b>

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 156 Access Mode Restrictions sorted by descending priority**Applies to [P22\\_PDR0](#)Applies to [P23\\_PDR0](#)Applies to [P24\\_PDR0](#)Applies to [P25\\_PDR0](#)Applies to [P30\\_PDR0](#)Applies to [P31\\_PDR0](#)Applies to [P32\\_PDR0](#)Applies to [P33\\_PDR0](#)Applies to [P34\\_PDR0](#)Applies to [P40\\_PDR0](#)

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-7), PLx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-7), PLx (x=0-7)	

**Table 157 Reset Values variant 1**Applies to [P22\\_PDR0](#)Applies to [P23\\_PDR0](#)Applies to [P24\\_PDR0](#)Applies to [P25\\_PDR0](#)Applies to [P30\\_PDR0](#)Applies to [P31\\_PDR0](#)Applies to [P32\\_PDR0](#)Applies to [P33\\_PDR0](#)Applies to [P34\\_PDR0](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
After SSW execution	2222 2222 <sub>H</sub>	Initial value in largest package
After SSW execution	----- <sub>H</sub>	Initial value package dependent

**Table 158 Reset Values of P40\_PDR0**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	----- <sub>H</sub>	Initial value package dependent

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P41\_PDR0

#### Port 41 Pad Driver Mode Register 0

(040<sub>H</sub>)

Reset Value: [Table 160](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>PL7</b>	<b>PD7</b>	<b>PL6</b>	<b>PD6</b>	<b>PL5</b>	<b>PD5</b>	<b>PL4</b>	<b>PD4</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PL3</b>	<b>PD3</b>	<b>PL2</b>	<b>PD2</b>	<b>PL1</b>	<b>PD1</b>	<b>PL0</b>	<b>PD0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>PDx (x=0-7)</b>	4*x+1:4*x	rw	<b>Pad Driver Mode for Pin x</b>
<b>PLx (x=0-7)</b>	4*x+3:4*x+2	rw	<b>Pad Level Selection for Pin x</b>

**Table 159 Access Mode Restrictions of P41\_PDR0 sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-7), PLx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-7), PLx (x=0-7)	

**Table 160 Reset Values of P41\_PDR0**

Reset Type	Reset Value	Note
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	----- <sub>H</sub>	Initial value package dependent

### P12\_PDR0

#### Port 12 Pad Driver Mode Register 0

(040<sub>H</sub>)

Reset Value: [Table 162](#)

### P26\_PDR0

#### Port 26 Pad Driver Mode Register 0

(040<sub>H</sub>)

Reset Value: [Table 162](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>				<b>0</b>				<b>0</b>				<b>0</b>			<b>0</b>
r				r				r				r			r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PL3</b>	<b>PD3</b>	<b>PL2</b>	<b>PD2</b>	<b>PL1</b>	<b>PD1</b>	<b>PL0</b>	<b>PD0</b>								

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PDx (x=0-3)</b>	4*x+1:4*x	rw	<b>Pad Driver Mode for Pin x</b>
<b>PLx (x=0-3)</b>	4*x+3:4*x+2	rw	<b>Pad Level Selection for Pin x</b>
<b>0</b>	31:28, 27:24, 23:20, 19:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 161 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_PDR0](#)

Applies to [P26\\_PDR0](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-3), PLx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-3), PLx (x=0-3)	

**Table 162 Reset Values**

Applies to [P12\\_PDR0](#)

Applies to [P26\\_PDR0](#)

Reset Type	Reset Value	Note
After SSW execution	0000 2222 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 ---- <sub>H</sub>	Initial value package dependent

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### Port 00 Pad Driver Mode Register 1

**P00\_PDR1**

**Port 00 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P01\_PDR1**

**Port 01 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P02\_PDR1**

**Port 02 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P10\_PDR1**

**Port 10 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P11\_PDR1**

**Port 11 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P13\_PDR1**

**Port 13 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P14\_PDR1**

**Port 14 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P15\_PDR1**

**Port 15 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P20\_PDR1**

**Port 20 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

**P24\_PDR1**

**Port 24 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 164](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>PL15</b>	<b>PD15</b>	<b>PL14</b>	<b>PD14</b>	<b>PL13</b>	<b>PD13</b>	<b>PL12</b>	<b>PD12</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PL11</b>	<b>PD11</b>	<b>PL10</b>	<b>PD10</b>	<b>PL9</b>	<b>PD9</b>	<b>PL8</b>	<b>PD8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>PDx (x=8-15)</b>	4*x-31:4*x-32	rw	<b>Pad Driver Mode for Pin x</b>
<b>PLx (x=8-15)</b>	4*x-29:4*x-30	rw	<b>Pad Level Selection for Pin x</b>

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 163 Access Mode Restrictions sorted by descending priority**Applies to [P00\\_PDR1](#)Applies to [P01\\_PDR1](#)Applies to [P02\\_PDR1](#)Applies to [P10\\_PDR1](#)Applies to [P11\\_PDR1](#)Applies to [P13\\_PDR1](#)Applies to [P14\\_PDR1](#)Applies to [P15\\_PDR1](#)Applies to [P20\\_PDR1](#)Applies to [P24\\_PDR1](#)

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8-15), PLx (x=8-15)	write access for enabled masters
Otherwise (default)	r	PDx (x=8-15), PLx (x=8-15)	

**Table 164 Reset Values**Applies to [P00\\_PDR1](#)Applies to [P01\\_PDR1](#)Applies to [P02\\_PDR1](#)Applies to [P10\\_PDR1](#)Applies to [P11\\_PDR1](#)Applies to [P13\\_PDR1](#)Applies to [P14\\_PDR1](#)Applies to [P15\\_PDR1](#)Applies to [P20\\_PDR1](#)Applies to [P24\\_PDR1](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
After SSW execution	2222 2222 <sub>H</sub>	Initial value in largest package
After SSW execution	----- <sub>H</sub>	Initial value package dependent

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P25\_PDR1

**Port 25 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 166](#)

### P30\_PDR1

**Port 30 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 166](#)

### P31\_PDR1

**Port 31 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 166](#)

### P33\_PDR1

**Port 33 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 166](#)

### P40\_PDR1

**Port 40 Pad Driver Mode Register 1** (044<sub>H</sub>) **Reset Value:** [Table 167](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>PL15</b>	<b>PD15</b>	<b>PL14</b>		<b>PD14</b>		<b>PL13</b>		<b>PD13</b>		<b>PL12</b>		<b>PD12</b>			
rw	rw	rw		rw											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PL11</b>	<b>PD11</b>	<b>PL10</b>		<b>PD10</b>		<b>PL9</b>		<b>PD9</b>		<b>PL8</b>		<b>PD8</b>			
rw	rw	rw		rw											

Field	Bits	Type	Description
<b>PDx (x=8-15)</b>	4*x-31:4*x-32	rw	<b>Pad Driver Mode for Pin x</b>
<b>PLx (x=8-15)</b>	4*x-29:4*x-30	rw	<b>Pad Level Selection for Pin x</b>

**Table 165 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_PDR1](#)

Applies to [P30\\_PDR1](#)

Applies to [P31\\_PDR1](#)

Applies to [P33\\_PDR1](#)

Applies to [P40\\_PDR1](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8-15), PLx (x=8-15)	write access for enabled masters
Otherwise (default)	r	PDx (x=8-15), PLx (x=8-15)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 166 Reset Values variant 1**

Applies to P25\_PDR1

Applies to P30\_PDR1

Applies to P31 PDR1

Applies to P33 PDR1

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
After SSW execution	2222 2222 <sub>H</sub>	Initial value in largest package
After SSW execution	---- ---- <sub>H</sub>	Initial value package dependent

**Table 167 Reset Values of P40 PDR1**

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	----- <sub>H</sub>	Initial value package dependent

P22 PDR1

## **Port 22 Pad Driver Mode Register 1**

(044<sub>H</sub>)

## **Reset Value: Table 169**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>PDx (x=8-11)</b>	4*x-31:4*x-32	rw	<b>Pad Driver Mode for Pin x</b>
<b>PLx (x=8-11)</b>	4*x-29:4*x-30	rw	<b>Pad Level Selection for Pin x</b>
<b>0</b>	31:28, 27:24, 23:20, 19:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 168 Access Mode Restrictions of P22\_PDR1 sorted by descending priority**

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8-11), PLx (x=8-11)	write access for enabled masters
Otherwise (default)	r	PDx (x=8-11), PLx (x=8-11)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 169 Reset Values of P22\_PDR1**

Reset Type	Reset Value	Note
After SSW execution	0000 2222 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 ---- <sub>H</sub>	Initial value package dependent

### P41\_PDR1

#### Port 41 Pad Driver Mode Register 1

(044<sub>H</sub>)

Reset Value: [Table 171](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			0			0			0			0			
			r			r			r			r			r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RL11</b>	<b>RD11</b>		<b>RL10</b>		<b>RD10</b>		<b>RL9</b>		<b>RD9</b>		<b>PL8</b>		<b>PD8</b>		
rw	rw		rw		rw		rw		rw		rw		rw		rw

Field	Bits	Type	Description
<b>PDx (x=8)</b>	4*x-31:4*x-32	rw	<b>Pad Driver Mode for Pin x</b>
<b>RDx (x=9-11)</b>	4*x-31:4*x-32	rw	<b>Reserved</b> Read as 0; should be written with 0.
<b>PLx (x=8)</b>	4*x-29:4*x-30	rw	<b>Pad Level Selection for Pin x</b>
<b>RLx (x=9-11)</b>	4*x-29:4*x-30	rw	<b>Reserved</b> Read as 0; should be written with 0.
<b>0</b>	31:28, 27:24, 23:20, 19:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 170 Access Mode Restrictions of P41\_PDR1 sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8), PLx (x=8), RDx (x=9-11), RLx (x=9-11)	write access for enabled masters
Otherwise (default)	r	PDx (x=8), PLx (x=8), RDx (x=9-11), RLx (x=9-11)	

**Table 171 Reset Values of P41\_PDR1**

Reset Type	Reset Value	Note
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 ---- <sub>H</sub>	Initial value package dependent

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### Port 00 Emergency Stop Register

P00\_ESR

Port 00 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P01\_ESR

Port 01 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P02\_ESR

Port 02 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P10\_ESR

Port 10 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P11\_ESR

Port 11 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P13\_ESR

Port 13 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P14\_ESR

Port 14 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P15\_ESR

Port 15 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P20\_ESR

Port 20 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

P24\_ESR

Port 24 Emergency Stop Register (050<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	ENO
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-15)	x	rw	<b>Emergency Stop Enable for Pin x</b> This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 <sub>B</sub> Emergency stop function for Pn.x is disabled. 1 <sub>B</sub> Emergency stop function for Pn.x is enabled.
0	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 172 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_ESR](#)

Applies to [P01\\_ESR](#)

Applies to [P02\\_ESR](#)

Applies to [P10\\_ESR](#)

Applies to [P11\\_ESR](#)

Applies to [P13\\_ESR](#)

Applies to [P14\\_ESR](#)

Applies to [P15\\_ESR](#)

Applies to [P20\\_ESR](#)

Applies to [P24\\_ESR](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-15) write access for enabled masters
Otherwise (default)	r	ENx (x=0-15)

Most GPIO lines have an emergency stop logic implemented (see Figure “General Structure of a Port Pin” in the Family chapter).

Each of these GPIO lines has its own emergency stop enable bit ENx that is located in the emergency stop register Pn\_ESR of Port n. If the emergency stop signal becomes active, one of two states can be selected:

- Emergency stop function disabled (ENx = 0):  
The output line remains connected (alternate function).
- Emergency stop function enabled (ENx = 1):  
The mapped output function is disconnected and the safe state is entered by switching to input function with internal pull-up connected or tri-state, depending on the configured reset value of the corresponding Pn\_IOCR register through PMSWCR5.TRISTREQ or setting of HWCFG[6].(the content of the corresponding PCx bit fields in register Pn\_IOCR will not be considered).

### Exceptions for Emergency Stop Implementation

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlayed with Testmode)
- Not available for P40.x and P41.x (analog input ANx overlayed with GPI)
- Not available for P32.0 and P32.1 when using EVRC regulator.
- Not available for P21.2 (used as EMGSTOPB pin).
- Not available for P33.8 (used as EMGSTOPA pin).
- Not available for dedicated I/O without General Purpose Output function (e.g ESRx, TMS, TCK)

The Emergency Stop function can be overruled on the following GPIO Ports:

- P00.x: Emergency Stop can be overruled by the VADC. Overruling can be disabled via the control register P00\_PCSR.
- P14.0 and P14.1: Emergency Stop can be overruled in the DXCPL (DAP over CAN physical layer) mode. No Overruling in the DXCM (Debug over can message) mode
- P21.6: Emergency Stop can be overruled in JTAG mode if this pin is used as TDI
- P21.7: Emergency Stop can be overruled in JTAG or Three Pin DAP mode.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

- P33.0-7, P33.9-15 and P34.1: Emergency Stop can be overruled by the 8-Bit Standby Controller (SCR), if implemented. Overruling can be disabled via the control register P33\_PCSR and P34\_PCSR.

On pins with LVDS TX pads the Emergency Stop affects only the CMOS driver not the LVDS driver. Thus only when LPCRx.TX\_EN selects CMOS mode the output is switched off. When TX\_EN selects LVDS mode the output is not switched off.

### P25\_ESR

**Port 25 Emergency Stop Register** **(050<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_ESR

**Port 30 Emergency Stop Register** **(050<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_ESR

**Port 31 Emergency Stop Register** **(050<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	ENO
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-15)	x	rw	<b>Emergency Stop Enable for Pin x</b> This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 <sub>B</sub> Emergency stop function for Pn.x is disabled. 1 <sub>B</sub> Emergency stop function for Pn.x is enabled.
0	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 173 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_ESR](#)

Applies to [P30\\_ESR](#)

Applies to [P31\\_ESR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw ENx (x=0-15)		write access for enabled masters
Otherwise (default)	r ENx (x=0-15)		

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P12\_ESR

**Port 12 Emergency Stop Register** **(050<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

### P26\_ESR

**Port 26 Emergency Stop Register** **(050<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-3)	x	rw	<b>Emergency Stop Enable for Pin x</b> This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 <sub>B</sub> Emergency stop function for Pn.x is disabled. 1 <sub>B</sub> Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 174 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_ESR](#)

Applies to [P26\\_ESR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-3)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-3)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P21\_ESR

#### Port 21 Emergency Stop Register

(050<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	EN7	EN6	EN5	EN4	EN3	0	EN1	ENO
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	r	rw	rw

Field	Bits	Type	Description
ENx (x=0-1,3-7)	x	rw	<b>Emergency Stop Enable for Pin x</b> This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 <sub>B</sub> Emergency stop function for Pn.x is disabled. 1 <sub>B</sub> Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 11, 10, 9, 8, 2, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

Table 175 Access Mode Restrictions of P21\_ESR sorted by descending priority

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-1,3-7)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-1,3-7)	

### P22\_ESR

#### Port 22 Emergency Stop Register

(050<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	ENO
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
ENx (x=0-11)	x	rw	<p><b>Emergency Stop Enable for Pin x</b></p> <p>This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function.</p> <p>0<sub>B</sub> Emergency stop function for Pn.x is disabled. 1<sub>B</sub> Emergency stop function for Pn.x is enabled.</p>
0	15, 14, 13, 12, 31:16	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

**Table 176 Access Mode Restrictions of P22\_ESR sorted by descending priority**

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-11)
Otherwise (default)	r	ENx (x=0-11)

### P23\_ESR

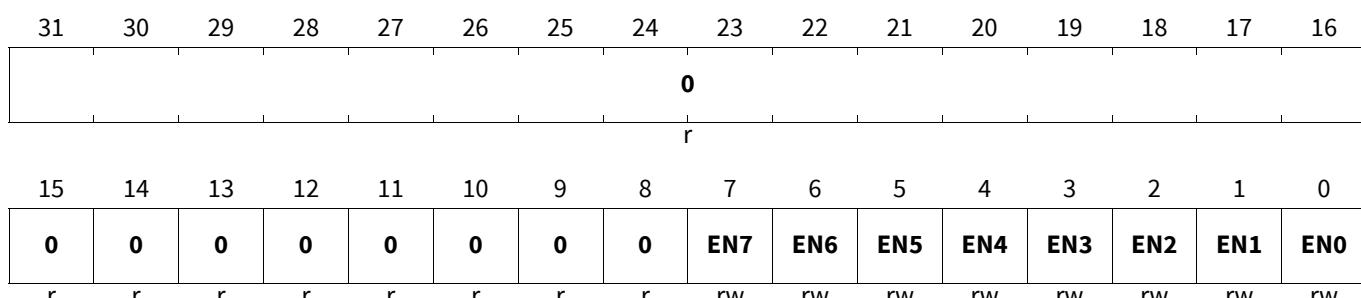
**Port 23 Emergency Stop Register** (050<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P32\_ESR

**Port 32 Emergency Stop Register** (050<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P34\_ESR

**Port 34 Emergency Stop Register** (050<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
ENx (x=0-7)	x	rw	<p><b>Emergency Stop Enable for Pin x</b></p> <p>This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function.</p> <p>0<sub>B</sub> Emergency stop function for Pn.x is disabled. 1<sub>B</sub> Emergency stop function for Pn.x is enabled.</p>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 177 Access Mode Restrictions sorted by descending priority**

Applies to [P23\\_ESR](#)

Applies to [P32\\_ESR](#)

Applies to [P34\\_ESR](#)

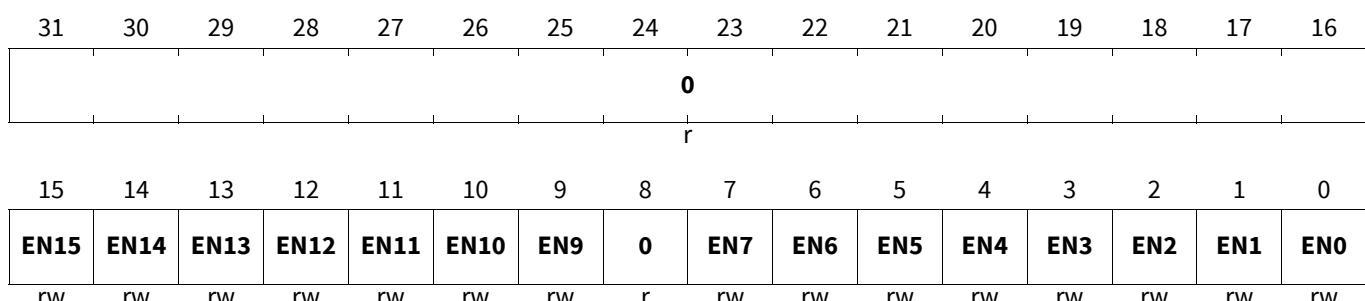
Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-7)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-7)	

### P33\_ESR

#### Port 33 Emergency Stop Register

(050<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>



Field	Bits	Type	Description
ENx (x=0-7,9-15)	x	rw	<b>Emergency Stop Enable for Pin x</b> This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 <sub>B</sub> Emergency stop function for Pn.x is disabled. 1 <sub>B</sub> Emergency stop function for Pn.x is enabled.
0	8, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 178 Access Mode Restrictions of P33\_ESR sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-7,9-15)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-7,9-15)	

### P40\_ESR

**Port 40 Emergency Stop Register** (050<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_ESR

**Port 41 Emergency Stop Register** (050<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 179 Access Mode Restrictions sorted by descending priority**

Applies to [P40\\_ESR](#)

Applies to [P41\\_ESR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	-	See bit field definitions above	write access for enabled masters
Otherwise (default)	-	See bit field definitions above	

### Port 00 Pin Function Decision Control Register

The pad structure of the GPIO lines offers the possibility to disable/enable port pad, select digital input or analog ADC input functionalities. Note that Class S pads have different characteristics than other digital input pads. For analog inputs, setting PDISx to 1 disables the Schmitt trigger input buffer, which would otherwise reduce analog input accuracy. For the ADC diagnostic features “PDD” and “MD” however the corresponding PDISx needs to be 0 to allow activation of their pull resistors. This feature can be controlled by individual bits in the Pn\_PDISC

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

register, independently from input/output and pull-up/pull-down control functionality as programmed in the Pn\_IOCR register. One Pn\_PDISC register is assigned to each port.

**Note:** After reset, all Px\_PDISC registers have the reset value of  $0000\ 0000_H$ . The startup software enables only the pads with digital input/output functionality which are available in that package. P40\_PDISC and P41\_PDISC are configured by the SSW for analog input function (kept disabled). The documented reset value shows the value in the largest package.

### P00\_PDISC

**Port 00 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P01\_PDISC

**Port 01 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P02\_PDISC

**Port 02 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P10\_PDISC

**Port 10 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P11\_PDISC

**Port 11 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P13\_PDISC

**Port 13 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P14\_PDISC

**Port 14 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P15\_PDISC

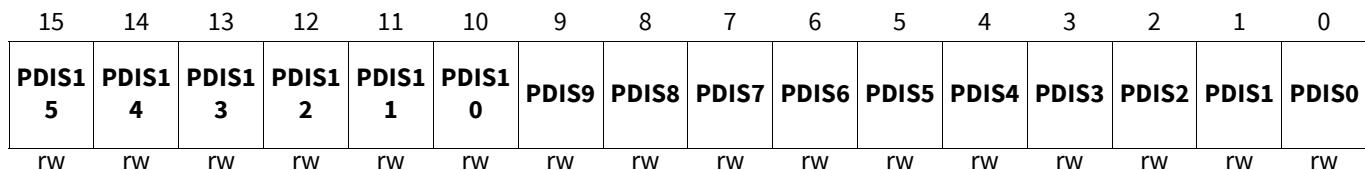
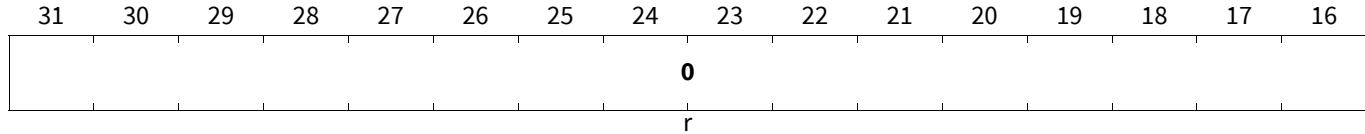
**Port 15 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P20\_PDISC

**Port 20 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)

### P24\_PDISC

**Port 24 Pin Function Decision Control Register (060<sub>H</sub>)** Reset Value: [Table 181](#)



Field	Bits	Type	Description
PDISx (x=0-15)	x	rw	<b>Pin Function Decision Control for Pin x</b> This bit selects the function of the port pad. 0 <sub>B</sub> Digital functionality of pad Pn.x is enabled. 1 <sub>B</sub> Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

---

**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 180 Access Mode Restrictions sorted by descending priority**Applies to [P00\\_PDISC](#)Applies to [P01\\_PDISC](#)Applies to [P02\\_PDISC](#)Applies to [P10\\_PDISC](#)Applies to [P11\\_PDISC](#)Applies to [P13\\_PDISC](#)Applies to [P14\\_PDISC](#)Applies to [P15\\_PDISC](#)Applies to [P20\\_PDISC](#)Applies to [P24\\_PDISC](#)

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-15)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-15)	

**Table 181 Reset Values**Applies to [P00\\_PDISC](#)Applies to [P01\\_PDISC](#)Applies to [P02\\_PDISC](#)Applies to [P10\\_PDISC](#)Applies to [P11\\_PDISC](#)Applies to [P13\\_PDISC](#)Applies to [P14\\_PDISC](#)Applies to [P15\\_PDISC](#)Applies to [P20\\_PDISC](#)Applies to [P24\\_PDISC](#)

<b>Reset Type</b>	<b>Reset Value</b>	<b>Note</b>
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 ---- <sub>H</sub>	Initial value package dependent

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P25\_PDISC

**Port 25 Pin Function Decision Control Register (060<sub>H</sub>)**

Reset Value: [Table 183](#)

### P30\_PDISC

**Port 30 Pin Function Decision Control Register (060<sub>H</sub>)**

Reset Value: [Table 183](#)

### P31\_PDISC

**Port 31 Pin Function Decision Control Register (060<sub>H</sub>)**

Reset Value: [Table 183](#)

### P33\_PDISC

**Port 33 Pin Function Decision Control Register (060<sub>H</sub>)**

Reset Value: [Table 183](#)

### P40\_PDISC

**Port 40 Pin Function Decision Control Register (060<sub>H</sub>)**

Reset Value: [Table 184](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>PDIS15</b>	<b>PDIS14</b>	<b>PDIS13</b>	<b>PDIS12</b>	<b>PDIS11</b>	<b>PDIS10</b>	<b>PDIS9</b>	<b>PDIS8</b>	<b>PDIS7</b>	<b>PDIS6</b>	<b>PDIS5</b>	<b>PDIS4</b>	<b>PDIS3</b>	<b>PDIS2</b>	<b>PDIS1</b>	<b>PDIS0</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>PDISx (x=0-15)</b>	x	rw	<b>Pin Function Decision Control for Pin x</b> This bit selects the function of the port pad. 0 <sub>B</sub> Digital functionality of pad Pn.x is enabled. 1 <sub>B</sub> Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
<b>0</b>	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 182 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_PDISC](#)

Applies to [P30\\_PDISC](#)

Applies to [P31\\_PDISC](#)

Applies to [P33\\_PDISC](#)

Applies to [P40\\_PDISC](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-15)
Otherwise (default)	r	PDISx (x=0-15)

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 183 Reset Values variant 1**

Applies to [P25\\_PDISC](#)

Applies to [P30\\_PDISC](#)

Applies to [P31\\_PDISC](#)

Applies to [P33\\_PDISC](#)

Reset Type	Reset Value	Note
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 ---- <sub>H</sub>	Initial value package dependent

**Table 184 Reset Values of P40\_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 FFFF <sub>H</sub>	Initial value in largest package
After SSW execution	0000 ---- <sub>H</sub>	Initial value package dependent

### P12\_PDISC

**Port 12 Pin Function Decision Control Register (060<sub>H</sub>)**

**Reset Value: [Table 186](#)**

### P26\_PDISC

**Port 26 Pin Function Decision Control Register (060<sub>H</sub>)**

**Reset Value: [Table 186](#)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Bits	Type	Description
PDISx (x=0-3)	x	rw	<b>Pin Function Decision Control for Pin x</b> This bit selects the function of the port pad. 0 <sub>B</sub> Digital functionality of pad Pn.x is enabled. 1 <sub>B</sub> Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 185 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_PDISC](#)

Applies to [P26\\_PDISC](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-3)
Otherwise (default)	r	PDISx (x=0-3)

**Table 186 Reset Values**

Applies to [P12\\_PDISC](#)

Applies to [P26\\_PDISC](#)

Reset Type	Reset Value	Note
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 000- <sub>H</sub>	Initial value package dependent

### P21\_PDISC

**Port 21 Pin Function Decision Control Register (060<sub>H</sub>)**

**Reset Value:** [Table 188](#)

### P23\_PDISC

**Port 23 Pin Function Decision Control Register (060<sub>H</sub>)**

**Reset Value:** [Table 188](#)

### P32\_PDISC

**Port 32 Pin Function Decision Control Register (060<sub>H</sub>)**

**Reset Value:** [Table 188](#)

### P34\_PDISC

**Port 34 Pin Function Decision Control Register (060<sub>H</sub>)**

**Reset Value:** [Table 188](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PDIS7	PDIS6	PDIS5	PDIS4	PDIS3	PDIS2	PDIS1	PDISO
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PDISx (x=0-7)	x	rw	<b>Pin Function Decision Control for Pin x</b> This bit selects the function of the port pad. 0 <sub>B</sub> Digital functionality of pad Pn.x is enabled. 1 <sub>B</sub> Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.

### General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 187 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_PDISC](#)

Applies to [P23\\_PDISC](#)

Applies to [P32\\_PDISC](#)

Applies to [P34\\_PDISC](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-7)	

**Table 188 Reset Values**

Applies to [P21\\_PDISC](#)

Applies to [P23\\_PDISC](#)

Applies to [P32\\_PDISC](#)

Applies to [P34\\_PDISC](#)

Reset Type	Reset Value	Note
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 00-- <sub>H</sub>	Initial value package dependent

### P22\_PDISC

#### Port 22 Pin Function Decision Control Register (060<sub>H</sub>)

Reset Value: [Table 190](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

0	0	0	0	PDIS1 1	PDIS1 0	PDIS9	PDIS8	PDIS7	PDIS6	PDIS5	PDIS4	PDIS3	PDIS2	PDIS1	PDIS0
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PDISx (x=0-11)</b>	x	rw	<p><b>Pin Function Decision Control for Pin x</b></p> <p>This bit selects the function of the port pad.</p> <p>0<sub>B</sub> Digital functionality of pad Pn.x is enabled.</p> <p>1<sub>B</sub> Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.</p>
0	15, 14, 13, 12, 31:16	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

**Table 189 Access Mode Restrictions of P22\_PDISC sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-11)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-11)	

**Table 190 Reset Values of P22\_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 0000 <sub>H</sub>	Initial value in largest package
After SSW execution	0000 0--- <sub>H</sub>	Initial value package dependent

### P41\_PDISC

#### Port 41 Pin Function Decision Control Register (060<sub>H</sub>)

Reset Value: [Table 192](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>PDIS8</b>	<b>PDIS7</b>	<b>PDIS6</b>	<b>PDIS5</b>	<b>PDIS4</b>	<b>PDIS3</b>	<b>PDIS2</b>	<b>PDIS1</b>	<b>PDIS0</b>
r	r	r	r	r	r	r	rw								

Field	Bits	Type	Description
<b>PDISx (x=0-8)</b>	x	rw	<p><b>Pin Function Decision Control for Pin x</b></p> <p>This bit selects the function of the port pad.</p> <p>0<sub>B</sub> Digital functionality of pad Pn.x is enabled.</p> <p>1<sub>B</sub> Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.</p>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 191 Access Mode Restrictions of P41\_PDISC sorted by descending priority**

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-8)
Otherwise (default)	r	PDISx (x=0-8)

**Table 192 Reset Values of P41\_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 01FF <sub>H</sub>	Initial value in largest package
After SSW execution	0000 0--- <sub>H</sub>	Initial value package dependent

### Port 00 Pin Controller Select Register

This register has different functionality in each port:

- In Ports shared with the standby controller (SCR) it selects if the SCR or the Tricore system control data and control functions of these port lines.
- In Ports with analog inputs to the EVADC it enables control of pull by the EVADC for the Pull Down Diagnostics (PDD) / Multiplexer Diagnostics (MD) feature.
- In Ports with Ethernet output it selects between alternate output and fast RGMII/RMII/MII mode.
- In Ports with SMU FSP pin (P33.8) the PCSR.SEL bit enables the SMU to override pad configuration signals. Therefore this bit has the reset value 1<sub>B</sub> and shall be kept 1<sub>B</sub> by the application. The SMU override is documented in the SMU chapter (see SMU\_PCTL.PCFG and Figure “SMU/PAD Control Interface to the PADs”).

### P00\_PCSR

#### Port 00 Pin Controller Select Register

(064<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>								<b>0</b>							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	R14	R13	R12	SEL11	SEL10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
SELx (x=10-11)	x	rw	<b>Output Select for Pin x</b> This bit enables or disables EVADC control of the pulls for Pull Down Diagnostics (PDD) / Multiplexer Diagnostics (MD) feature. 0 <sub>B</sub> Disable EVADC PDD/MD feature of pin x. 1 <sub>B</sub> Enable EVADC PDD/MD feature of pin x.
Rx (x=0-9,12-15)	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
0	30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

Table 193 Access Mode Restrictions of P00\_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-9,12-15)	write access only for masters with supervisor mode
	rw	SELx (x=10-11)	
Otherwise (default)	r	Rx (x=0-9,12-15), SELx (x=10-11)	

**P01\_PCSR**

**Port 01 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P02\_PCSR**

**Port 02 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P10\_PCSR**

**Port 10 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P13\_PCSR**

**Port 13 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P14\_PCSR**

**Port 14 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P15\_PCSR**

**Port 15 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P20\_PCSR**

**Port 20 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P24\_PCSR**

**Port 24 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P25\_PCSR**

**Port 25 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**P30\_PCSR**

**Port 30 Pin Controller Select Register** (064<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

<b>0</b>	<b>0</b>														
r	r														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
Rx (x=0-15)	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
0	30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 194 Access Mode Restrictions sorted by descending priority**

Applies to [P01\\_PCSR](#)

Applies to [P02\\_PCSR](#)

Applies to [P10\\_PCSR](#)

Applies to [P13\\_PCSR](#)

Applies to [P14\\_PCSR](#)

Applies to [P15\\_PCSR](#)

Applies to [P20\\_PCSR](#)

Applies to [P24\\_PCSR](#)

Applies to [P25\\_PCSR](#)

Applies to [P30\\_PCSR](#)

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-15)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-15)	

### P31\_PCSR

Port 31 Pin Controller Select Register (064<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>							<b>0</b>								
r							r								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>R15</b>	<b>R14</b>	<b>R13</b>	<b>R12</b>	<b>R11</b>	<b>R10</b>	<b>R9</b>	<b>R8</b>	<b>R7</b>	<b>R6</b>	<b>R5</b>	<b>R4</b>	<b>R3</b>	<b>R2</b>	<b>R1</b>	<b>R0</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-15)	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
0	30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 195 Access Mode Restrictions of P31\_PCSR sorted by descending priority**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-15)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-15)	

### P11\_PCSR

Port 11 Pin Controller Select Register (064 <sub>H</sub> ) Application Reset Value: 0000 0000 <sub>H</sub>															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>								<b>0</b>							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>R15</b>	<b>R14</b>	<b>R13</b>	<b>R12</b>	<b>R11</b>	<b>R10</b>	<b>R9</b>	<b>R8</b>	<b>R7</b>	<b>SEL6</b>	<b>R5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-4,6)</b>	x	rw	<b>Output Select for Pin x</b> This bit enables or disables alternate/fast Ethernet output. $0_B$ Ethernet output via ports alternate output of pin x. $1_B$ Ethernet output via fast RGMII/RMII/MII mode of pin x.
<b>Rx (x=5,7-15)</b>	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
<b>0</b>	30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 196 Access Mode Restrictions of P11\_PCSR sorted by descending priority**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=5,7-15)	write access only for masters with supervisor mode
	rw	SELx (x=0-4,6)	
Otherwise (default)	r	Rx (x=5,7-15), SELx (x=0-4,6)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P12\_PCSR

**Port 12 Pin Controller Select Register** **(064<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

### P26\_PCSR

**Port 26 Pin Controller Select Register** **(064<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>								<b>0</b>							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>R3</b>	<b>R2</b>	<b>R1</b>	<b>R0</b>
r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-3)	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
<b>0</b>	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 197 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_PCSR](#)

Applies to [P26\\_PCSR](#)

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r Rx (x=0-3)		write access only for masters with supervisor mode
Otherwise (default)	r Rx (x=0-3)		

### P21\_PCSR

**Port 21 Pin Controller Select Register** **(064<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_PCSR

**Port 23 Pin Controller Select Register** **(064<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_PCSR

**Port 32 Pin Controller Select Register** **(064<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>							<b>0</b>								
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>R7</b>	<b>R6</b>	<b>R5</b>	<b>R4</b>	<b>R3</b>	<b>R2</b>	<b>R1</b>	<b>R0</b>
r	r	r	r	r	r	r	r	rw							

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
Rx (x=0-7)	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
0	15, 14, 13, 12, 11, 10, 9, 8, 30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 198 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_PCSR](#)

Applies to [P23\\_PCSR](#)

Applies to [P32\\_PCSR](#)

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-7)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-7)	

### P22\_PCSR

**Port 22 Pin Controller Select Register** (064<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

### P41\_PCSR

**Port 41 Pin Controller Select Register** (064<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>								<b>0</b>							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>R11</b>	<b>R10</b>	<b>R9</b>	<b>R8</b>	<b>R7</b>	<b>R6</b>	<b>R5</b>	<b>R4</b>	<b>R3</b>	<b>R2</b>	<b>R1</b>	<b>R0</b>
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-11)	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
0	15, 14, 13, 12, 30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 199 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_PCSR](#)

Applies to [P41\\_PCSR](#)

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-11)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-11)	

### P33\_PCSR

Port 33 Pin Controller Select Register (064 <sub>H</sub> ) Application Reset Value: 0000 0100 <sub>H</sub>															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>LCK</b>								<b>0</b>							
rh							r								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>	<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-7,9-15)</b>	x	rw	<b>Output Select for Pin x</b> This bit enables or disables SCR control. 0 <sub>B</sub> Tricore selected for data and control of pin x and not SCR. 1 <sub>B</sub> SCR selected for data and control of pin x.
<b>SELx (x=8)</b>	x	rw	<b>Output Select for Pin x</b> This bit enables or disables SMU to override pad configuration. 0 <sub>B</sub> Disable SMU override of pad configuration for FSP pin x. 1 <sub>B</sub> Enable SMU to override pad configuration for FSP pin x.
<b>LCK</b>	31	rh	<b>Lock Status</b> This bit indicates if the register can be updated with a new value or if the register is locked due to an ongoing transfer to the SCR and a write action from the bus has no effect. In Ports without SCR overlay this bit is always 0 <sub>B</sub> . 0 <sub>B</sub> The register is unlocked and can be updated. 1 <sub>B</sub> The register is locked (a write transfer to SCR is ongoing) and can not be updated.
<b>0</b>	30:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 200 Access Mode Restrictions of P33\_PCSR sorted by descending priority**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	rh	LCK	write access only for masters with supervisor mode
	rw	SELx (x=0-7,9-15), SELx (x=8)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 200 Access Mode Restrictions of P33\_PCSR sorted by descending priority (cont'd)**

Mode Name	Access Mode		Description
Otherwise (default)	r	SELx (x=0-7,9-15), SELx (x=8)	
	rh	LCK	

### P34\_PCSR

#### Port 34 Pin Controller Select Register

(064<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>LCK</b>								<b>0</b>							
rh								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>R7</b>	<b>R6</b>	<b>R5</b>	<b>R4</b>	<b>R3</b>	<b>R2</b>	<b>SEL1</b>	<b>R0</b>
r	r	r	r	r	r	r	r	rw	rw						

Field	Bits	Type	Description
<b>SELx (x=1)</b>	x	rw	<b>Output Select for Pin x</b> This bit enables or disables SCR control. $0_B$ Tricore selected for data and control of pin x and not SCR. $1_B$ SCR selected for data and control of pin x.
<b>Rx (x=0,2-7)</b>	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
<b>LCK</b>	31	rh	<b>Lock Status</b> This bit indicates if the register can be updated with a new value or if the register is locked due to an ongoing transfer to the SCR and a write action from the bus has no effect. In Ports without SCR overlay this bit is always $0_B$ . $0_B$ The register is unlocked and can be updated. $1_B$ The register is locked (a write transfer to SCR is ongoing) and can not be updated.
<b>0</b>	15, 14, 13, 12, 11, 10, 9, 8, 30:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 201 Access Mode Restrictions of P34\_PCSR sorted by descending priority**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0,2-7)	write access only for masters with supervisor mode
	rh	LCK	
	rw	SELx (x=1)	
Otherwise (default)	r	Rx (x=0,2-7), SELx (x=1)	
	rh	LCK	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P40\_PCSR

#### Port 40 Pin Controller Select Register

(064<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL15	R14	R13	SEL12	SEL11	SEL10	R9	R8	R7	R6	SEL5	R4	SEL3	SEL2	SEL1	R0

Field	Bits	Type	Description
SELx (x=1-3,5,10-12,15)	x	rw	<b>Output Select for Pin x</b> This bit enables or disables EVADC control of the pulls for Pull Down Diagnostics (PDD) / Multiplexer Diagnostics (MD) feature. 0 <sub>B</sub> Disable EVADC PDD/MD feature of pin x. 1 <sub>B</sub> Enable EVADC PDD/MD feature of pin x.
Rx (x=0,4,6-9,13-14)	x	rw	<b>Reserved</b> Read as 0; should be written with 0.
0	30:16, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 202 Access Mode Restrictions of P40\_PCSR sorted by descending priority**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0,4,6-9,13-14)	write access only for masters with supervisor mode
	rw	SELx (x=1-3,5,10-12,15)	
Otherwise (default)	r	Rx (x=0,4,6-9,13-14), SELx (x=1-3,5,10-12,15)	

### Port 00 Output Modification Set Register 0

The port output modification set register x, (x = 0, 4, 8, 12) contains control bits to individually set the logic state of a single port line by manipulating the output register.

Note: Registers Pn\_OMSRx (x = 0, 4, 8, 12) are virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Register Pn\_OMSR0 sets the logic state of Pn.[3:0] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_OMSR0

**Port 00 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P01\_OMSR0

**Port 01 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P02\_OMSR0

**Port 02 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P10\_OMSR0

**Port 10 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P11\_OMSR0

**Port 11 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P12\_OMSR0

**Port 12 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P13\_OMSR0

**Port 13 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P14\_OMSR0

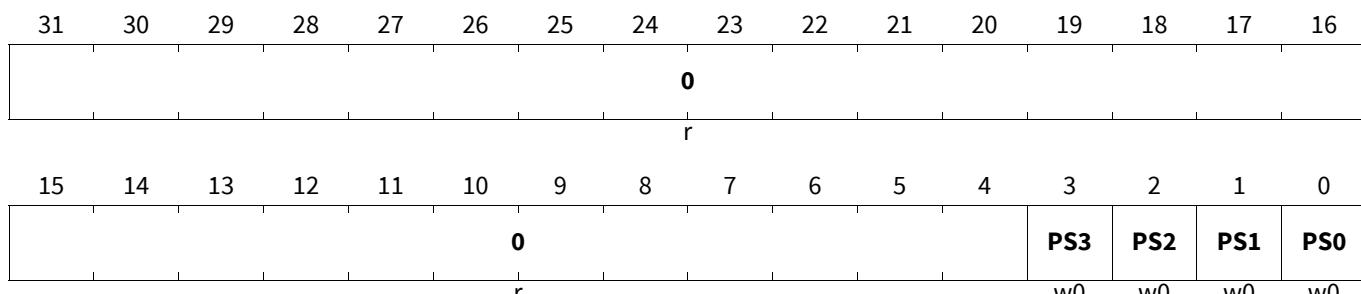
**Port 14 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P15\_OMSR0

**Port 15 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P20\_OMSR0

**Port 20 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
PSx (x=0-3)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
0	31:4	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 203 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMSR0](#)

Applies to [P01\\_OMSR0](#)

Applies to [P02\\_OMSR0](#)

Applies to [P10\\_OMSR0](#)

Applies to [P11\\_OMSR0](#)

Applies to [P12\\_OMSR0](#)

Applies to [P13\\_OMSR0](#)

Applies to [P14\\_OMSR0](#)

Applies to [P15\\_OMSR0](#)

Applies to [P20\\_OMSR0](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	w0	PSx (x=0-3)
Otherwise (default)	r0	PSx (x=0-3)

### P21\_OMSR0

**Port 21 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P22\_OMSR0

**Port 22 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_OMSR0

**Port 23 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P24\_OMSR0

**Port 24 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P25\_OMSR0

**Port 25 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P26\_OMSR0

**Port 26 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMSR0

**Port 30 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMSR0

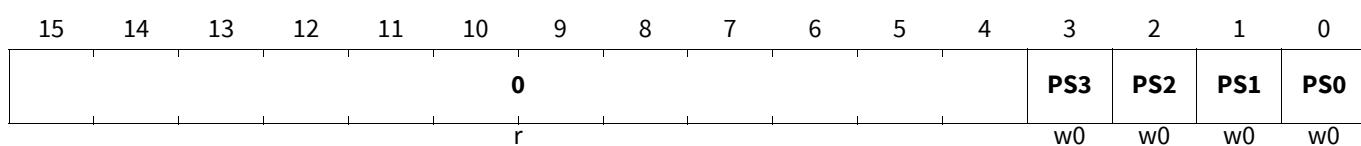
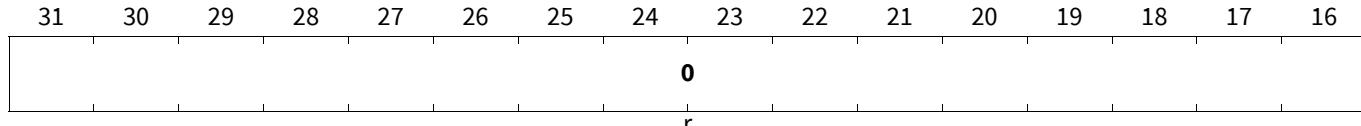
**Port 31 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_OMSR0

**Port 32 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMSR0

**Port 33 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PSx (x=0-3)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. $0_B$ No operation $1_B$ Sets Pn_OUT.Px
0	31:4	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 204 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_OMSR0](#)

Applies to [P22\\_OMSR0](#)

Applies to [P23\\_OMSR0](#)

Applies to [P24\\_OMSR0](#)

Applies to [P25\\_OMSR0](#)

Applies to [P26\\_OMSR0](#)

Applies to [P30\\_OMSR0](#)

Applies to [P31\\_OMSR0](#)

Applies to [P32\\_OMSR0](#)

Applies to [P33\\_OMSR0](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

### P34\_OMSR0

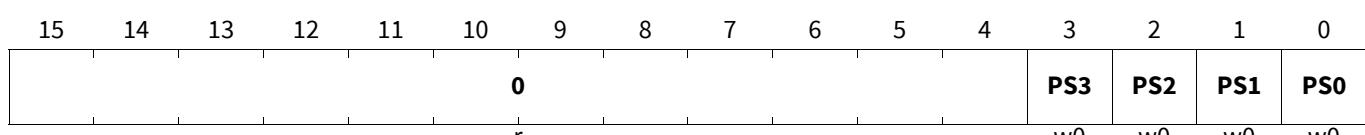
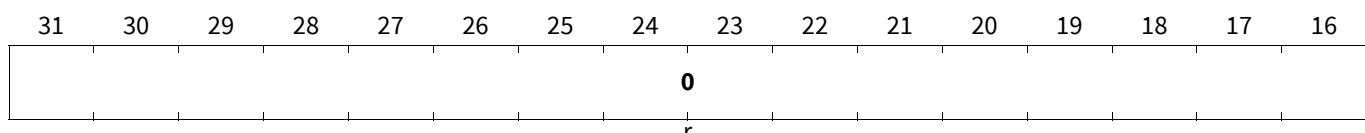
**Port 34 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMSR0

**Port 40 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_OMSR0

**Port 41 Output Modification Set Register 0** (070<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PSx (x=0-3)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. $0_B$ No operation $1_B$ Sets Pn_OUT.Px
0	31:4	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 205 Access Mode Restrictions sorted by descending priority**

Applies to [P34\\_OMSR0](#)

Applies to [P40\\_OMSR0](#)

Applies to [P41\\_OMSR0](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

## Port 00 Output Modification Set Register 4

Register Pn\_OMSR4 sets the logic state of Pn.[7:4] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_OMSR4

**Port 00 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P01\_OMSR4

**Port 01 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P02\_OMSR4

**Port 02 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P10\_OMSR4

**Port 10 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P11\_OMSR4

**Port 11 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P13\_OMSR4

**Port 13 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P14\_OMSR4

**Port 14 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P15\_OMSR4

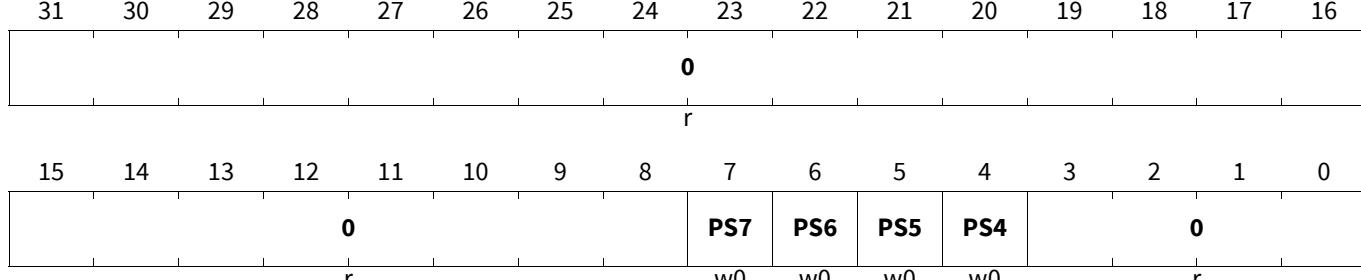
**Port 15 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P20\_OMSR4

**Port 20 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P21\_OMSR4

**Port 21 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
PSx (x=4-7)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
0	3:0, 31:8	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 206 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMSR4](#)

Applies to [P01\\_OMSR4](#)

Applies to [P02\\_OMSR4](#)

Applies to [P10\\_OMSR4](#)

Applies to [P11\\_OMSR4](#)

Applies to [P13\\_OMSR4](#)

Applies to [P14\\_OMSR4](#)

Applies to [P15\\_OMSR4](#)

Applies to [P20\\_OMSR4](#)

Applies to [P21\\_OMSR4](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	w0	PSx (x=4-7)
Otherwise (default)	r0	PSx (x=4-7)

### P22\_OMSR4

**Port 22 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_OMSR4

**Port 23 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P24\_OMSR4

**Port 24 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P25\_OMSR4

**Port 25 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMSR4

**Port 30 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMSR4

**Port 31 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_OMSR4

**Port 32 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMSR4

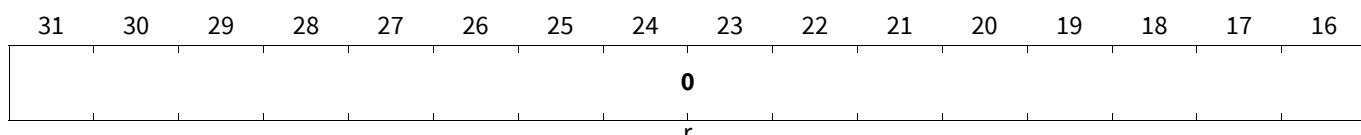
**Port 33 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P34\_OMSR4

**Port 34 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMSR4

**Port 40 Output Modification Set Register 4** (074<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PSx (x=4-7)</b>	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
<b>0</b>	3:0, 31:8	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 207 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_OMSR4](#)

Applies to [P23\\_OMSR4](#)

Applies to [P24\\_OMSR4](#)

Applies to [P25\\_OMSR4](#)

Applies to [P30\\_OMSR4](#)

Applies to [P31\\_OMSR4](#)

Applies to [P32\\_OMSR4](#)

Applies to [P33\\_OMSR4](#)

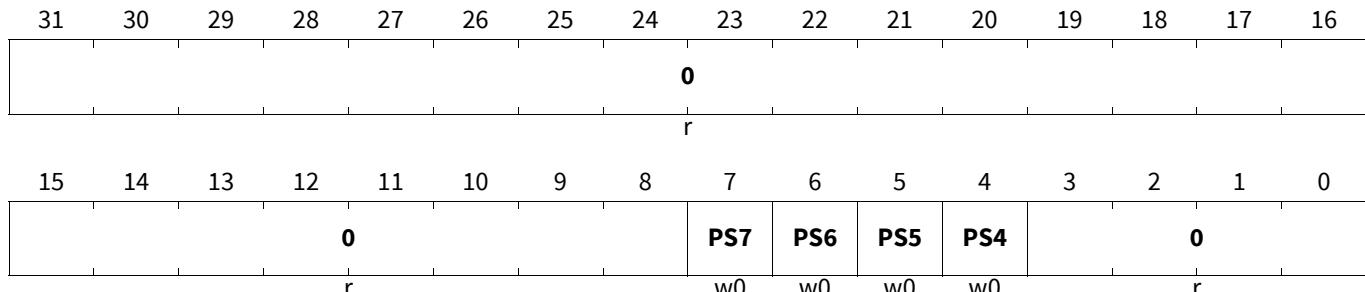
Applies to [P34\\_OMSR4](#)

Applies to [P40\\_OMSR4](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PSx (x=4-7)	

### P41\_OMSR4

**Port 41 Output Modification Set Register 4 (074<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
<b>PSx (x=4-7)</b>	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
<b>0</b>	3:0, 31:8	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 208 Access Mode Restrictions of P41\_OMSR4 sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=4-7)	
Otherwise (default)	r0	PSx (x=4-7)	

### Port 00 Output Modification Set Register 8

Register Pn\_OMSR8 sets the logic state of Pn.[11:8] port lines

#### P00\_OMSR8

**Port 00 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P01\_OMSR8

**Port 01 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P02\_OMSR8

**Port 02 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P10\_OMSR8

**Port 10 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P11\_OMSR8

**Port 11 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P13\_OMSR8

**Port 13 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P14\_OMSR8

**Port 14 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P15\_OMSR8

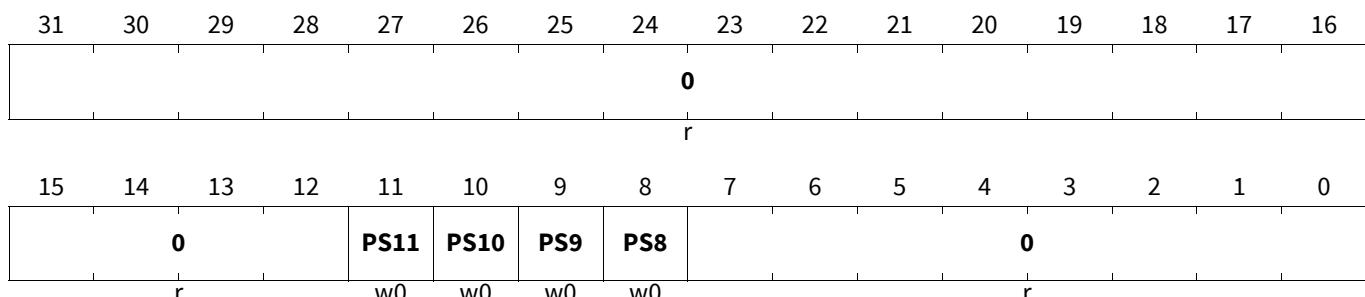
**Port 15 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P20\_OMSR8

**Port 20 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P22\_OMSR8

**Port 22 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
PSx (x=8-11)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
0	7:0, 31:12	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 209 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMSR8](#)

Applies to [P01\\_OMSR8](#)

Applies to [P02\\_OMSR8](#)

Applies to [P10\\_OMSR8](#)

Applies to [P11\\_OMSR8](#)

Applies to [P13\\_OMSR8](#)

Applies to [P14\\_OMSR8](#)

Applies to [P15\\_OMSR8](#)

Applies to [P20\\_OMSR8](#)

Applies to [P22\\_OMSR8](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PSx (x=8-11)	

### P24\_OMSR8

**Port 24 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P25\_OMSR8

**Port 25 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMSR8

**Port 30 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMSR8

**Port 31 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMSR8

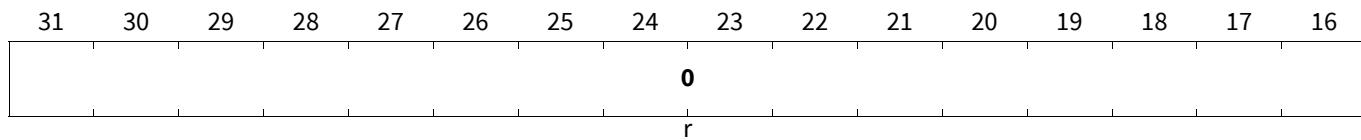
**Port 33 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMSR8

**Port 40 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_OMSR8

**Port 41 Output Modification Set Register 8** (078<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
PSx (x=8-11)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	7:0, 31:12	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 210 Access Mode Restrictions sorted by descending priority**

Applies to [P24\\_OMSR8](#)

Applies to [P25\\_OMSR8](#)

Applies to [P30\\_OMSR8](#)

Applies to [P31\\_OMSR8](#)

Applies to [P33\\_OMSR8](#)

Applies to [P40\\_OMSR8](#)

Applies to [P41\\_OMSR8](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PSx (x=8-11)	

## Port 00 Output Modification Set Register 12

Register Pn\_OMSR12 sets the logic state of Pn.[15:12] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_OMSR12

**Port 00 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P01\_OMSR12

**Port 01 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P02\_OMSR12

**Port 02 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P10\_OMSR12

**Port 10 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P11\_OMSR12

**Port 11 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P13\_OMSR12

**Port 13 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P14\_OMSR12

**Port 14 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P15\_OMSR12

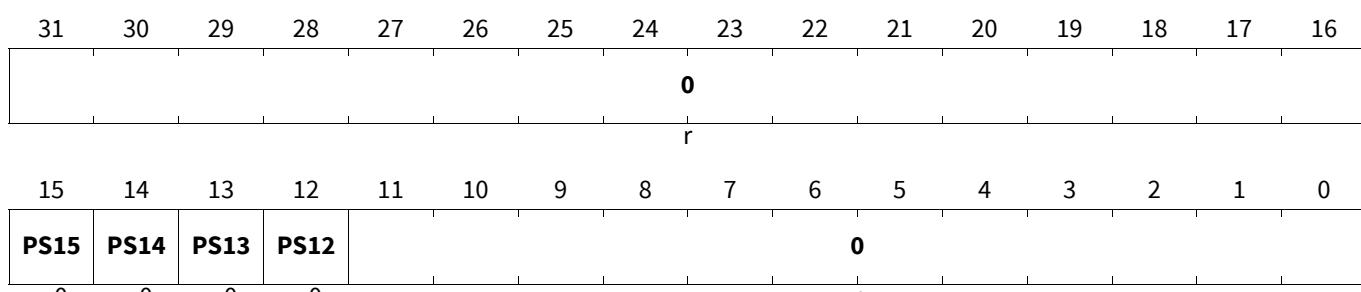
**Port 15 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P20\_OMSR12

**Port 20 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P24\_OMSR12

**Port 24 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
PSx (x=12-15)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
0	11:0, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 211 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMSR12](#)

Applies to [P01\\_OMSR12](#)

Applies to [P02\\_OMSR12](#)

Applies to [P10\\_OMSR12](#)

Applies to [P11\\_OMSR12](#)

Applies to [P13\\_OMSR12](#)

Applies to [P14\\_OMSR12](#)

Applies to [P15\\_OMSR12](#)

Applies to [P20\\_OMSR12](#)

Applies to [P24\\_OMSR12](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	w0	PSx (x=12-15) write access for enabled masters
Otherwise (default)	r0	PSx (x=12-15)

### P25\_OMSR12

**Port 25 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMSR12

**Port 30 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMSR12

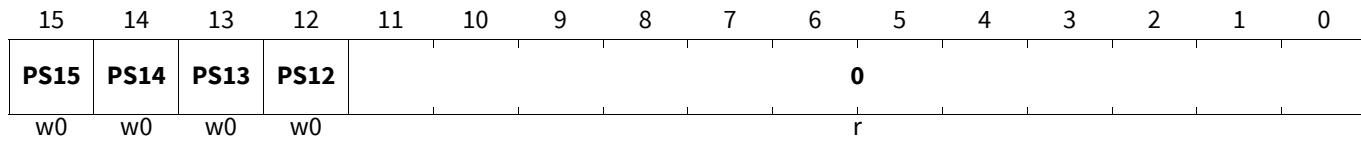
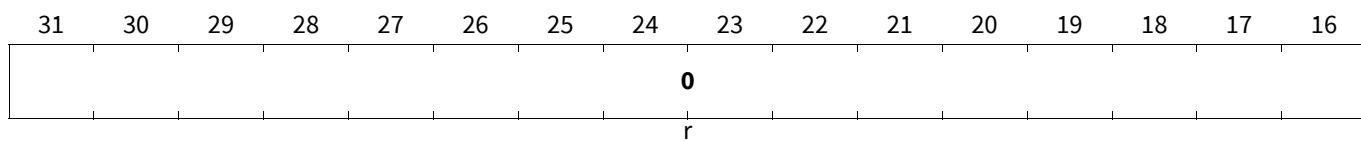
**Port 31 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMSR12

**Port 33 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMSR12

**Port 40 Output Modification Set Register 12** (07C<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
PSx (x=12-15)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
0	11:0, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 212 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_OMSR12](#)

Applies to [P30\\_OMSR12](#)

Applies to [P31\\_OMSR12](#)

Applies to [P33\\_OMSR12](#)

Applies to [P40\\_OMSR12](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN	w0 PSx (x=12-15)	write access for enabled masters
Otherwise (default)	r0 PSx (x=12-15)	

### Port 00 Output Modification Clear Register 0

The port output modification clear register x, (x = 0, 4, 8, 12) contains control bits to individually clear the logic state of a single port line by manipulating the output register.

**Note:** Registers  $Pn\_OMCRx$  ( $x = 0, 4, 8, 12$ ) are virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Register  $Pn\_OMCR0$  clears the logic state of  $Pn.[3:0]$  port lines

#### P00\_OMCR0

**Port 00 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P01\_OMCR0

**Port 01 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P02\_OMCR0

**Port 02 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P10\_OMCR0

**Port 10 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P11\_OMCR0

**Port 11 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P12\_OMCR0

**Port 12 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P13\_OMCR0

**Port 13 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P14\_OMCR0

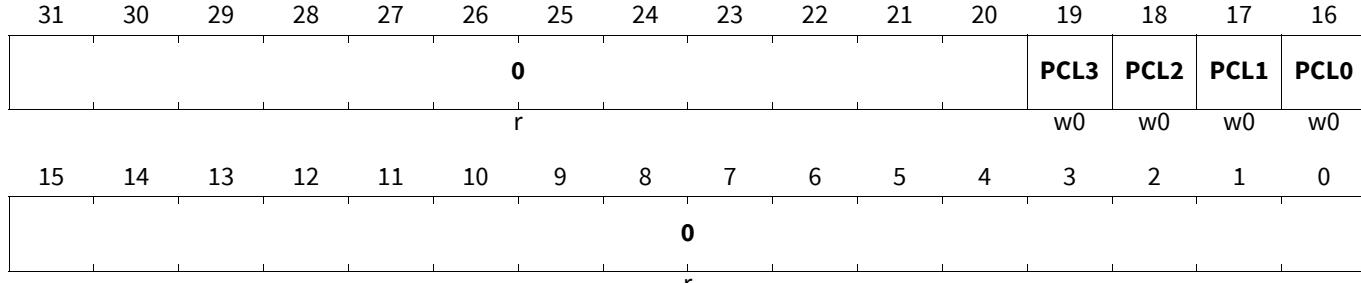
**Port 14 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P15\_OMCR0

**Port 15 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

#### P20\_OMCR0

**Port 20 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. $0_B$ No operation $1_B$ Clears Pn_OUT.Px
0	15:0, 31:20	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 213 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMCRO](#)

Applies to [P01\\_OMCRO](#)

Applies to [P02\\_OMCRO](#)

Applies to [P10\\_OMCRO](#)

Applies to [P11\\_OMCRO](#)

Applies to [P12\\_OMCRO](#)

Applies to [P13\\_OMCRO](#)

Applies to [P14\\_OMCRO](#)

Applies to [P15\\_OMCRO](#)

Applies to [P20\\_OMCRO](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P21\_OMCR0

**Port 21 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P22\_OMCR0

**Port 22 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P23\_OMCR0

**Port 23 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P24\_OMCR0

**Port 24 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P25\_OMCR0

**Port 25 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P26\_OMCR0

**Port 26 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P30\_OMCR0

**Port 30 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P31\_OMCR0

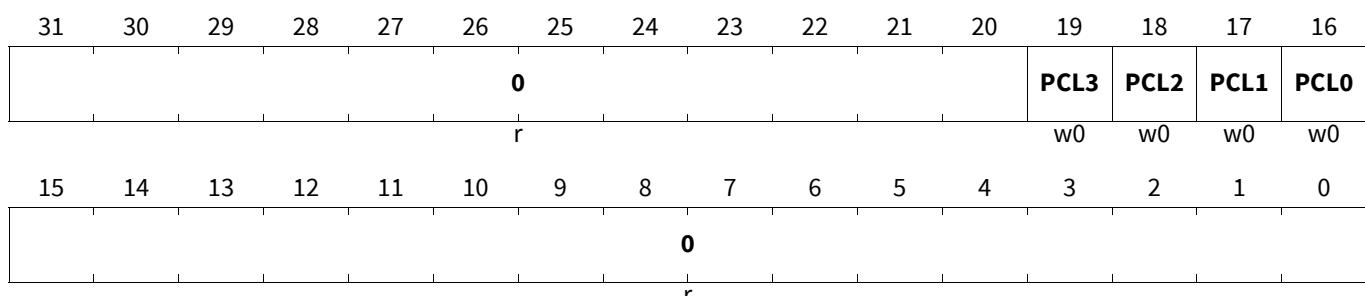
**Port 31 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P32\_OMCR0

**Port 32 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P33\_OMCR0

**Port 33 Output Modification Clear Register 0** (080<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
0	15:0, 31:20	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 214 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_OMCR0](#)

Applies to [P22\\_OMCR0](#)

Applies to [P23\\_OMCR0](#)

Applies to [P24\\_OMCR0](#)

Applies to [P25\\_OMCR0](#)

Applies to [P26\\_OMCR0](#)

Applies to [P30\\_OMCR0](#)

Applies to [P31\\_OMCR0](#)

Applies to [P32\\_OMCR0](#)

Applies to [P33\\_OMCR0](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

### P34\_OMCR0

**Port 34 Output Modification Clear Register 0 (080<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMCR0

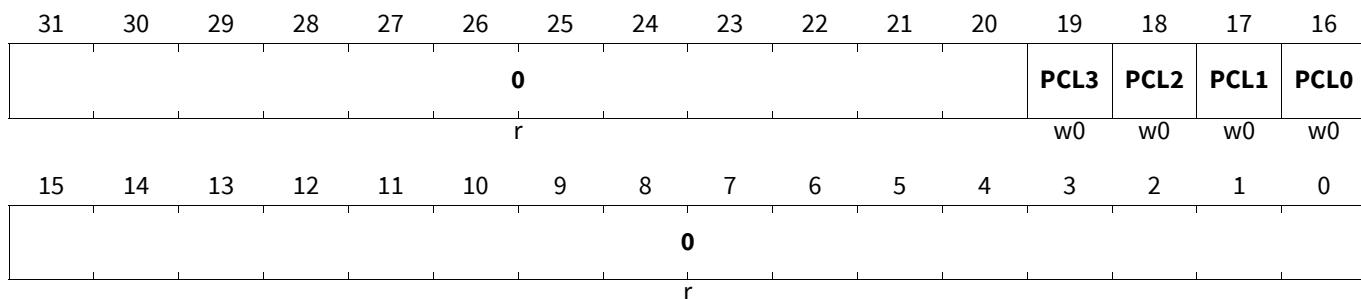
**Port 40 Output Modification Clear Register 0 (080<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_OMCR0

**Port 41 Output Modification Clear Register 0 (080<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
0	15:0, 31:20	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 215 Access Mode Restrictions sorted by descending priority**

Applies to [P34\\_OMCR0](#)

Applies to [P40\\_OMCR0](#)

Applies to [P41\\_OMCR0](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

### Port 00 Output Modification Clear Register 4

Register Pn\_OMCR4 clears the logic state of Pn.[7:4] port lines

#### P00\_OMCR4

**Port 00 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P01\_OMCR4

**Port 01 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P02\_OMCR4

**Port 02 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P10\_OMCR4

**Port 10 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P11\_OMCR4

**Port 11 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P13\_OMCR4

**Port 13 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P14\_OMCR4

**Port 14 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P15\_OMCR4

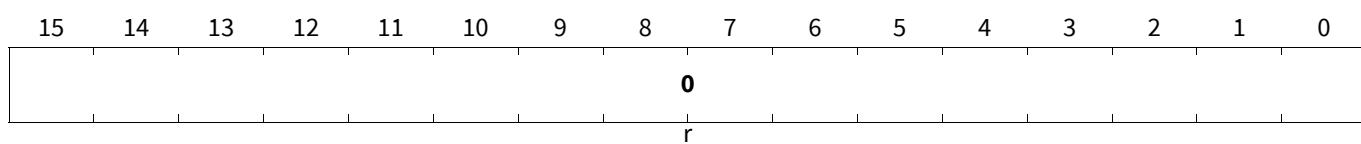
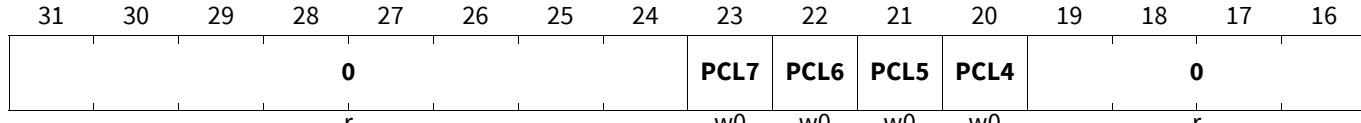
**Port 15 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P20\_OMCR4

**Port 20 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

#### P21\_OMCR4

**Port 21 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=4-7)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
0	19:0, 31:24	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 216 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMCR4](#)

Applies to [P01\\_OMCR4](#)

Applies to [P02\\_OMCR4](#)

Applies to [P10\\_OMCR4](#)

Applies to [P11\\_OMCR4](#)

Applies to [P13\\_OMCR4](#)

Applies to [P14\\_OMCR4](#)

Applies to [P15\\_OMCR4](#)

Applies to [P20\\_OMCR4](#)

Applies to [P21\\_OMCR4](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=4-7)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P22\_OMCR4

**Port 22 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P23\_OMCR4

**Port 23 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P24\_OMCR4

**Port 24 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P25\_OMCR4

**Port 25 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P30\_OMCR4

**Port 30 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P31\_OMCR4

**Port 31 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P32\_OMCR4

**Port 32 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P33\_OMCR4

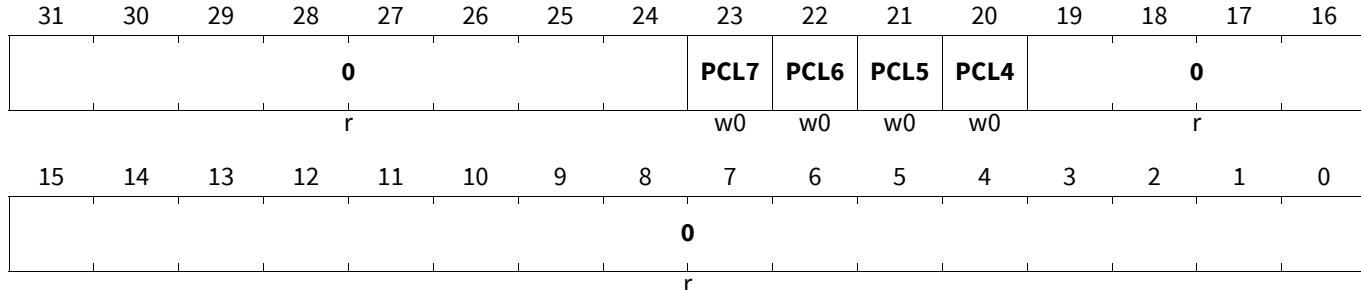
**Port 33 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P34\_OMCR4

**Port 34 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P40\_OMCR4

**Port 40 Output Modification Clear Register 4** (084<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
PCLx (x=4-7)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
0	19:0, 31:24	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 217 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_OMCR4](#)

Applies to [P23\\_OMCR4](#)

Applies to [P24\\_OMCR4](#)

Applies to [P25\\_OMCR4](#)

Applies to [P30\\_OMCR4](#)

Applies to [P31\\_OMCR4](#)

Applies to [P32\\_OMCR4](#)

Applies to [P33\\_OMCR4](#)

Applies to [P34\\_OMCR4](#)

Applies to [P40\\_OMCR4](#)

Mode Name	Access Mode		Description	
Master enabled in ACCEN	w0	PCLx (x=4-7)	write access for enabled masters	
Otherwise (default)	r0	PCLx (x=4-7)		

### P41\_OMCR4

#### Port 41 Output Modification Clear Register 4 (084<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
									PCL7	PCL6	PCL5	PCL4		0	
				r				w0	w0	w0	w0	w0		r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0							
															r

Field	Bits	Type	Description
PCLx (x=4-7)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
0	19:0, 31:24	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 218 Access Mode Restrictions of P41\_OMCR4 sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=4-7)	

### Port 00 Output Modification Clear Register 8

Register Pn\_OMCR8 clears the logic state of Pn.[11:8] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_OMCR8

**Port 00 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P01\_OMCR8

**Port 01 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P02\_OMCR8

**Port 02 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P10\_OMCR8

**Port 10 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P11\_OMCR8

**Port 11 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P13\_OMCR8

**Port 13 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P14\_OMCR8

**Port 14 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P15\_OMCR8

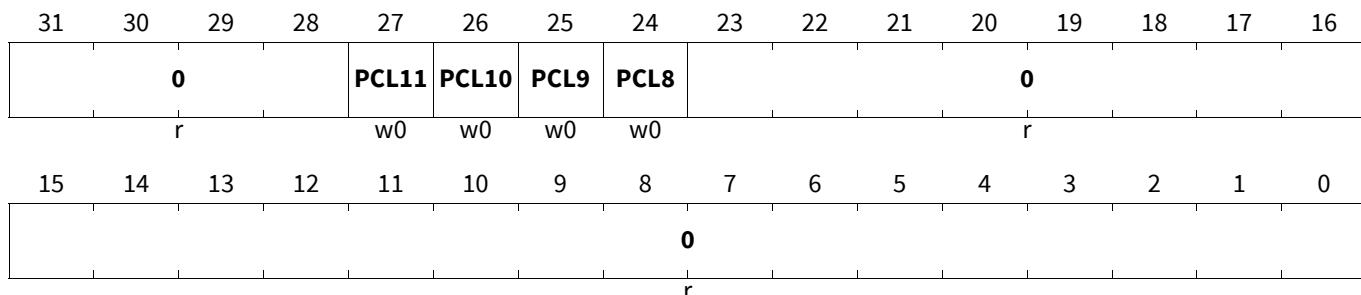
**Port 15 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P20\_OMCR8

**Port 20 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P22\_OMCR8

**Port 22 Output Modification Clear Register 8** (088<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
PCLx (x=8-11)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
0	23:0, 31:28	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 219 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMCR8](#)

Applies to [P01\\_OMCR8](#)

Applies to [P02\\_OMCR8](#)

Applies to [P10\\_OMCR8](#)

Applies to [P11\\_OMCR8](#)

Applies to [P13\\_OMCR8](#)

Applies to [P14\\_OMCR8](#)

Applies to [P15\\_OMCR8](#)

Applies to [P20\\_OMCR8](#)

Applies to [P22\\_OMCR8](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=8-11)	

### P24\_OMCR8

**Port 24 Output Modification Clear Register 8 (088<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P25\_OMCR8

**Port 25 Output Modification Clear Register 8 (088<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMCR8

**Port 30 Output Modification Clear Register 8 (088<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMCR8

**Port 31 Output Modification Clear Register 8 (088<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMCR8

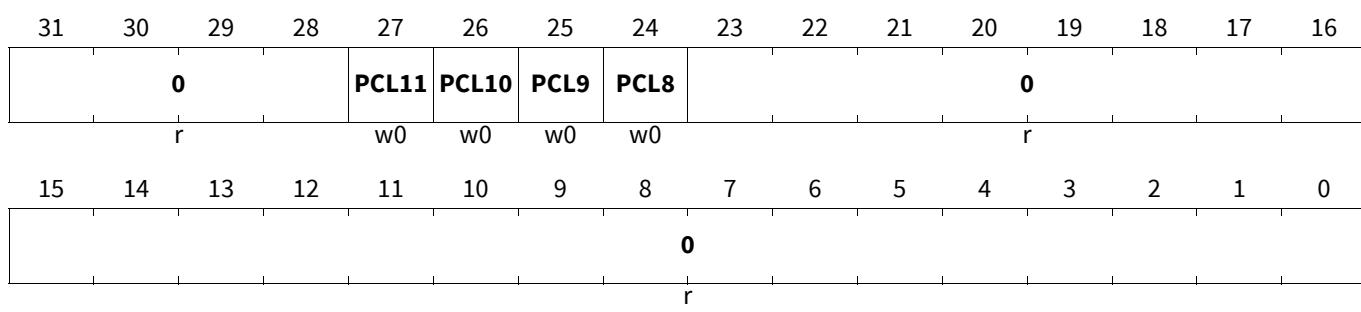
**Port 33 Output Modification Clear Register 8 (088<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMCR8

**Port 40 Output Modification Clear Register 8 (088<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_OMCR8

**Port 41 Output Modification Clear Register 8 (088<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
PCLx (x=8-11)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	23:0, 31:28	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 220 Access Mode Restrictions sorted by descending priority**

Applies to [P24\\_OMCR8](#)

Applies to [P25\\_OMCR8](#)

Applies to [P30\\_OMCR8](#)

Applies to [P31\\_OMCR8](#)

Applies to [P33\\_OMCR8](#)

Applies to [P40\\_OMCR8](#)

Applies to [P41\\_OMCR8](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=8-11)	

### Port 00 Output Modification Clear Register 12

Register Pn\_OMCR12 clears the logic state of Pn.[15:12] port lines

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_OMCR12

**Port 00 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P01\_OMCR12

**Port 01 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P02\_OMCR12

**Port 02 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P10\_OMCR12

**Port 10 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P11\_OMCR12

**Port 11 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P13\_OMCR12

**Port 13 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P14\_OMCR12

**Port 14 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P15\_OMCR12

**Port 15 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P20\_OMCR12

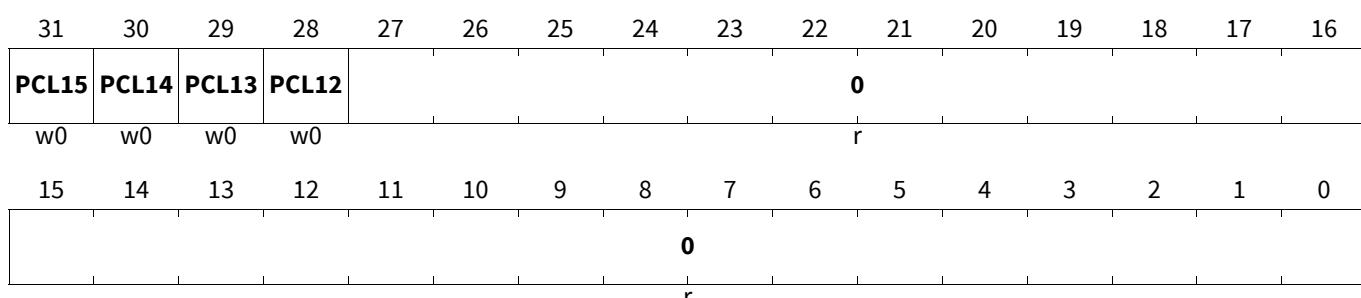
**Port 20 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P24\_OMCR12

**Port 24 Output Modification Clear Register 12** (08C<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
<b>PCLx (x=12-15)</b>	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
<b>0</b>	27:0	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 221 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMCR12](#)

Applies to [P01\\_OMCR12](#)

Applies to [P02\\_OMCR12](#)

Applies to [P10\\_OMCR12](#)

Applies to [P11\\_OMCR12](#)

Applies to [P13\\_OMCR12](#)

Applies to [P14\\_OMCR12](#)

Applies to [P15\\_OMCR12](#)

Applies to [P20\\_OMCR12](#)

Applies to [P24\\_OMCR12](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=12-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=12-15)	

### P25\_OMCR12

**Port 25 Output Modification Clear Register 12 (08C<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMCR12

**Port 30 Output Modification Clear Register 12 (08C<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMCR12

**Port 31 Output Modification Clear Register 12 (08C<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMCR12

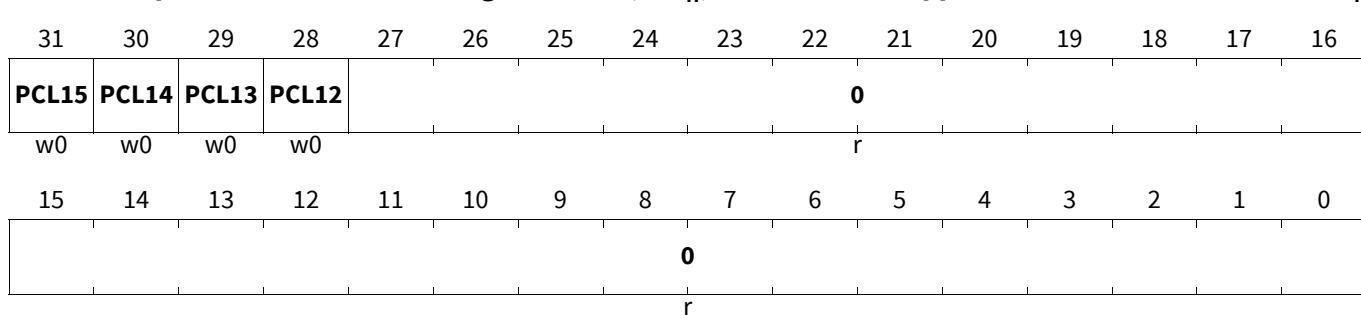
**Port 33 Output Modification Clear Register 12 (08C<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMCR12

**Port 40 Output Modification Clear Register 12 (08C<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
PCLx (x=12-15)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px
0	27:0	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 222 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_OMCR12](#)

Applies to [P30\\_OMCR12](#)

Applies to [P31\\_OMCR12](#)

Applies to [P33\\_OMCR12](#)

Applies to [P40\\_OMCR12](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=12-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=12-15)	

### Port 00 Output Modification Set Register

The port output modification set register contains control bits that make it possible to individually set the logic state of a single port line by manipulating the output register.

Note: *Register Pn\_OMSR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.*

#### P00\_OMSR

**Port 00 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P01\_OMSR

**Port 01 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P02\_OMSR

**Port 02 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P10\_OMSR

**Port 10 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P11\_OMSR

**Port 11 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P13\_OMSR

**Port 13 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P14\_OMSR

**Port 14 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P15\_OMSR

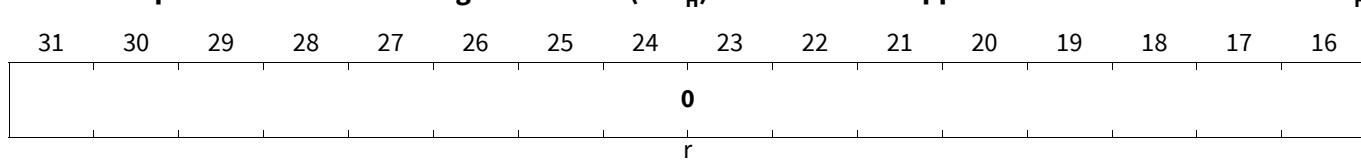
**Port 15 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P20\_OMSR

**Port 20 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

#### P24\_OMSR

**Port 24 Output Modification Set Register** **(090<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PSx (x=0-15)</b>	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
<b>0</b>	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 223 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMSR](#)

Applies to [P01\\_OMSR](#)

Applies to [P02\\_OMSR](#)

Applies to [P10\\_OMSR](#)

Applies to [P11\\_OMSR](#)

Applies to [P13\\_OMSR](#)

Applies to [P14\\_OMSR](#)

Applies to [P15\\_OMSR](#)

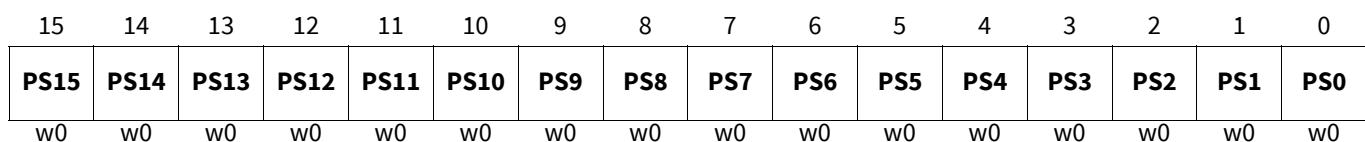
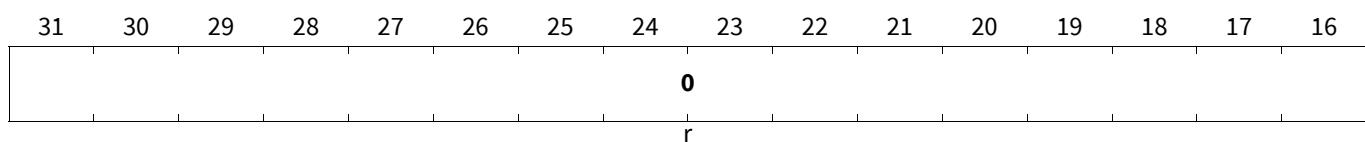
Applies to [P20\\_OMSR](#)

Applies to [P24\\_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-15)	

### P25\_OMSR

Port 25 Output Modification Set Register	(090 <sub>H</sub> )	Application Reset Value: 0000 0000 <sub>H</sub>
P30_OMSR		
Port 30 Output Modification Set Register	(090 <sub>H</sub> )	Application Reset Value: 0000 0000 <sub>H</sub>
P31_OMSR		
Port 31 Output Modification Set Register	(090 <sub>H</sub> )	Application Reset Value: 0000 0000 <sub>H</sub>
P33_OMSR		
Port 33 Output Modification Set Register	(090 <sub>H</sub> )	Application Reset Value: 0000 0000 <sub>H</sub>
P40_OMSR		
Port 40 Output Modification Set Register	(090 <sub>H</sub> )	Application Reset Value: 0000 0000 <sub>H</sub>



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PSx (x=0-15)</b>	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
<b>0</b>	31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 224 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_OMSR](#)

Applies to [P30\\_OMSR](#)

Applies to [P31\\_OMSR](#)

Applies to [P33\\_OMSR](#)

Applies to [P40\\_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-15)	

### P12\_OMSR

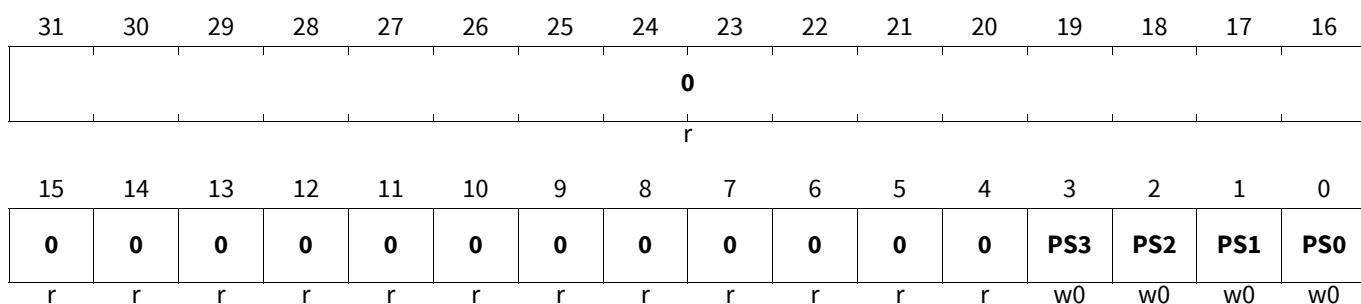
**Port 12 Output Modification Set Register** (090<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>

### P26\_OMSR

**Port 26 Output Modification Set Register** (090<sub>H</sub>)

**Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
<b>PSx (x=0-3)</b>	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
<b>0</b>	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 225 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_OMSR](#)

Applies to [P26\\_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	
Otherwise (default)	r0	PSx (x=0-3)	

### P21\_OMSR

**Port 21 Output Modification Set Register (090<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_OMSR

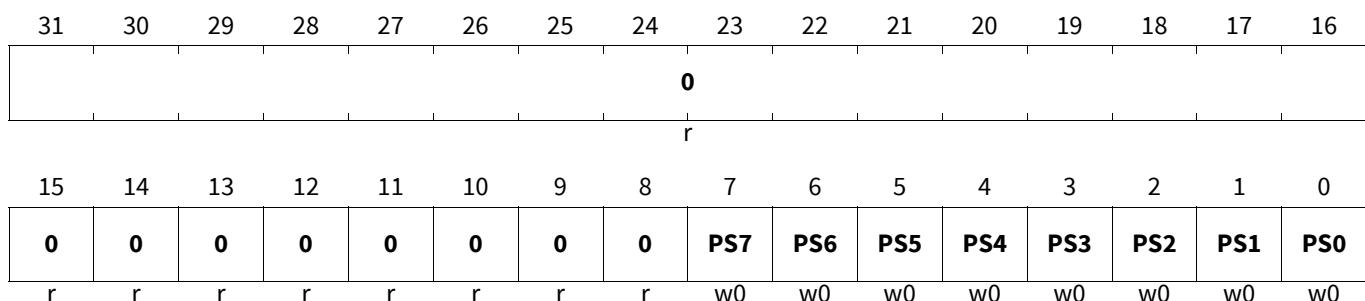
**Port 23 Output Modification Set Register (090<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_OMSR

**Port 32 Output Modification Set Register (090<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P34\_OMSR

**Port 34 Output Modification Set Register (090<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**



Field	Bits	Type	Description
PSx (x=0-7)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. $0_B$ No operation $1_B$ Sets Pn_OUT.Px
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 226 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_OMSR](#)

Applies to [P23\\_OMSR](#)

Applies to [P32\\_OMSR](#)

Applies to [P34\\_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-7)	
Otherwise (default)	r0	PSx (x=0-7)	

### P22\_OMSR

**Port 22 Output Modification Set Register (090<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_OMSR

**Port 41 Output Modification Set Register (090<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-11)	x	w0	<b>Set Bit x</b> Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Sets Pn_OUT.Px
0	15, 14, 13, 12, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0.

**Table 227 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_OMSR](#)

Applies to [P41\\_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-11)	
Otherwise (default)	r0	PSx (x=0-11)	

### Port 00 Output Modification Clear Register

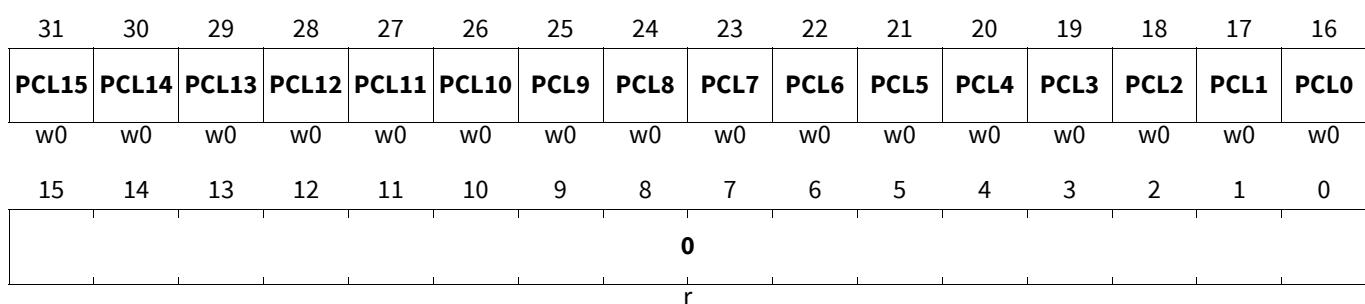
The port output modification clear register contains control bits that make it possible to individually clear the logic state of a single port line by manipulating the output register.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Note: Register Pn\_OMCR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

### P00\_OMCR

<b>Port 00 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P01_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 01 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P02_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 02 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P10_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 10 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P11_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 11 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P13_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 13 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P14_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 14 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P15_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 15 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P20_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 20 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>P24_OMCR</b>		<b>Application Reset Value: 0000 0000<sub>H</sub></b>
<b>Port 24 Output Modification Clear Register</b>	(094 <sub>H</sub> )	<b>Application Reset Value: 0000 0000<sub>H</sub></b>



Field	Bits	Type	Description
PCLx (x=0-15)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px.
0	15:0	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 228 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_OMCR](#)

Applies to [P01\\_OMCR](#)

Applies to [P02\\_OMCR](#)

Applies to [P10\\_OMCR](#)

Applies to [P11\\_OMCR](#)

Applies to [P13\\_OMCR](#)

Applies to [P14\\_OMCR](#)

Applies to [P15\\_OMCR](#)

Applies to [P20\\_OMCR](#)

Applies to [P24\\_OMCR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15)	

### P25\_OMCR

**Port 25 Output Modification Clear Register (094<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_OMCR

**Port 30 Output Modification Clear Register (094<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_OMCR

**Port 31 Output Modification Clear Register (094<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_OMCR

**Port 33 Output Modification Clear Register (094<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P40\_OMCR

**Port 40 Output Modification Clear Register (094<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCL15	PCL14	PCL13	PCL12	PCL11	PCL10	PCL9	PCL8	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=0-15)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px.
0	15:0	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 229 Access Mode Restrictions sorted by descending priority**

Applies to [P25\\_OMCR](#)

Applies to [P30\\_OMCR](#)

Applies to [P31\\_OMCR](#)

Applies to [P33\\_OMCR](#)

Applies to [P40\\_OMCR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15)	

### P12\_OMCR

**Port 12 Output Modification Clear Register (094<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

### P26\_OMCR

**Port 26 Output Modification Clear Register (094<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	PCL3	PCL2	PCL1	PCL0
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															

Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 230 Access Mode Restrictions sorted by descending priority**

Applies to [P12\\_OMCR](#)

Applies to [P26\\_OMCR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P21\_OMCR

**Port 21 Output Modification Clear Register** (094<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_OMCR

**Port 23 Output Modification Clear Register** (094<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_OMCR

**Port 32 Output Modification Clear Register** (094<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P34\_OMCR

**Port 34 Output Modification Clear Register** (094<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=0-7)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28, 27, 26, 25, 24	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 231 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_OMCR](#)

Applies to [P23\\_OMCR](#)

Applies to [P32\\_OMCR](#)

Applies to [P34\\_OMCR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-7)	

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P22\_OMCR

**Port 22 Output Modification Clear Register (094<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

### P41\_OMCR

**Port 41 Output Modification Clear Register (094<sub>H</sub>)**

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	PCL11	PCL10	PCL9	PCL8	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0							

Field	Bits	Type	Description
PCLx (x=0-11)	x+16	w0	<b>Clear Bit x</b> Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 <sub>B</sub> No operation 1 <sub>B</sub> Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 232 Access Mode Restrictions sorted by descending priority**

Applies to [P22\\_OMCR](#)

Applies to [P41\\_OMCR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-11)	

### Port 13 LVDS Pad Control Register x

The LVDS Pad Control Register controls the RX or TX functions of the LVDS pads. For usage of RX pad, bit field [7:0] are applicable. If used for TX pad, bit field [15:7] apply.

The sleep functionality of the LVDS pads is not controllable via this register. This is exclusively controlled by the HSCT module when this is connected.

The register x controls in general the pad pair 2\*x and 2\*x+1 of the port n.

Exceptionally when available the pad pair P14.9 and P14.10 is controlled by P14\_LPCR5.

**Attention:** *The bit field P21\_LPCR2.PS configures the pad supply for the LVDS bias distributor for all (not-RIF) LVDS pads and for the oscillator. Therefore even if no LVDS pad is used, this field has to be configured to the correct pad supply level.*

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P13\_LPCR<sub>x</sub> (x=0-3)

**Port 13 LVDS Pad Control Register x** (0A0<sub>H</sub>+x\*4) **Reset Value:** [Table 234](#)

### P15\_LPCR<sub>x</sub> (x=5-6)

**Port 15 LVDS Pad Control Register x** (0A0<sub>H</sub>+x\*4) **Reset Value:** [Table 234](#)

### P22\_LPCR<sub>x</sub> (x=0)

**Port 22 LVDS Pad Control Register x** (0A0<sub>H</sub>+x\*4) **Reset Value:** [Table 234](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>TX_P WDPD</b>	<b>TX_PD</b>	<b>VOSEX T</b>	<b>VOSDY N</b>	<b>VDIFFADJ</b>	<b>TX_EN</b>	<b>TEN_C TRL</b>	<b>PS</b>	<b>0</b>		<b>0</b>		<b>0</b>	<b>0</b>	<b>0</b>	
rw	rw	rw	rw	rw	rw	rw	rw	r		r		r	r	r	r

Field	Bits	Type	Description
<b>PS</b>	7	rw	<b>Pad Supply Selection</b> Selects between 5V or 3.3V supply on $V_{EXT}$ for the pad-pair. Used in RX and TX pads! 0 <sub>B</sub> 3.3V supply 1 <sub>B</sub> 5V supply
<b>TEN_CTRL</b>	8	rw	<b>LVDS TX_EN controller</b> The LVDS TX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). 0 <sub>B</sub> Port controlled 1 <sub>B</sub> Reserved
<b>TX_EN</b>	9	rw	<b>Enable Transmit LVDS</b> Enable the transmit LVDS / disable CMOS path. If this bit is set to 0 - no transfer on LVDS data path can be initiated and the LVDS driver is disabled (powered down). 0 <sub>B</sub> disable LVDS / enable CMOS mode 1 <sub>B</sub> enable LVDS / disable CMOS mode
<b>VDIFFADJ</b>	11:10	rw	<b>LVDS Output Amplitude Tuning</b> With these two configuration bits the LVDS output current/amplitude can be adjusted. The voltage swing depending on VDIFFADJ setting is documented in the Data Sheet, see parameter $V_{OD}$ .
<b>VOSDYN</b>	12	rw	<b>Tune Bit of VOS Control Loop Static/Dynamic</b> Tune bit to change $V_{OS}$ control loop between static and dynamic mode. Don't change reset value.
<b>VOSEXT</b>	13	rw	<b>Tune Bit of VOS Control Loop Internal/External</b> Tune bit to change $V_{OS}$ control loop. Don't change reset value.

### General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
TX_PD	14	rw	<b>LVDS Power Down</b> Unused in this device. LVDS disabled by TX_EN means power down. 0 <sub>B</sub> LVDS power on 1 <sub>B</sub> LVDS power down (default)
TX_PWDPD	15	rw	<b>Enable TX Power down pull down.</b> This function disables or enables the LVDS pull down resistor. The application code must disable TX power down pull down resistor with a power up. With a LVDS Power Down configuration the pull down function must be enabled, if required. 0 <sub>B</sub> disabled TX Power down pull down resistor. 1 <sub>B</sub> enabled TX Power down pull down resistor.
0	0, 1, 2, 5:3, 6, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 233 Access Mode Restrictions sorted by descending priority**

Applies to [P13\\_LPCR<sub>x</sub> \(x=0-3\)](#)

Applies to [P15\\_LPCR<sub>x</sub> \(x=5-6\)](#)

Applies to [P22\\_LPCR<sub>x</sub> \(x=0\)](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT	write access for enabled masters
Otherwise (default)	r	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT	

**Table 234 Reset Values**

Applies to [P13\\_LPCR<sub>x</sub> \(x=0-3\)](#)

Applies to [P15\\_LPCR<sub>x</sub> \(x=5-6\)](#)

Applies to [P22\\_LPCR<sub>x</sub> \(x=0\)](#)

Reset Type	Reset Value	Note
After SSW execution	0000 5480 <sub>H</sub>	Initial value of RX depends on trimming

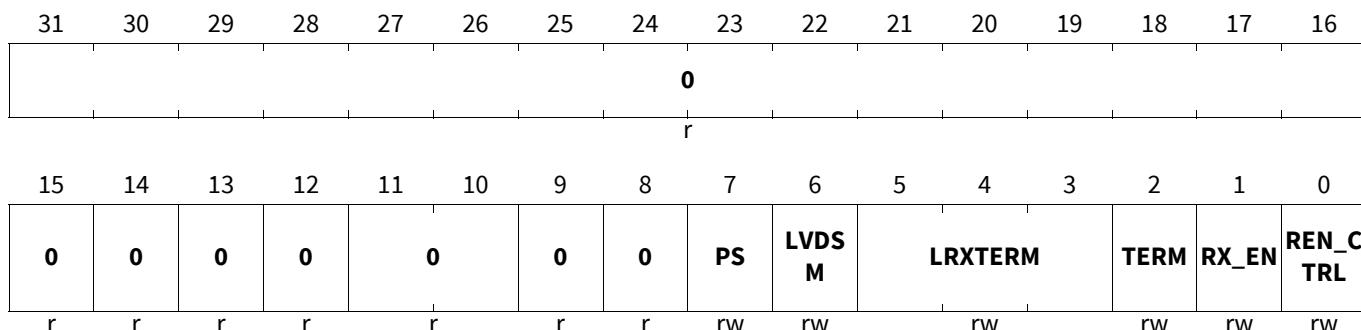
## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P14\_LPCR<sub>x</sub> (x=5)

**Port 14 LVDS Pad Control Register x**

(0A0<sub>H</sub>+x\*4)

Reset Value: [Table 236](#)



Field	Bits	Type	Description
<b>REN_CTRL</b>	0	rw	<b>LVDS RX_EN controller</b> The LVDS RX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). 0 <sub>B</sub> Port controlled 1 <sub>B</sub> Reserved
<b>RX_EN</b>	1	rw	<b>Enable Receive LVDS</b> Enable the receive LVDS / disable CMOS path. If this bit is set to 0 – no transfer from the LVDS sender can be received and the receiver LVDS is in low power state. 0 <sub>B</sub> disable LVDS / enable CMOS mode (reserved for pads without CMOS input stage) 1 <sub>B</sub> enable LVDS / disable CMOS mode
<b>TERM</b>	2	rw	<b>Select Receiver Termination Mode</b> Selects a suitable internal load resistor between both pads. 0 <sub>B</sub> external termination - on the PCB 1 <sub>B</sub> 100 Ω Receiver internal termination
<b>LRXTERM</b>	5:3	rw	<b>LVDS RX Poly-resistor configuration value</b> Programming bits for the on die poly resistor termination. The value is configured during production test. Each chip configuration on this bit field is unique and configured during production testing.  <i>Note:</i> The configuration value shall not be changed by user after start-up for a guaranteed behavior.
<b>LVDSM</b>	6	rw	<b>LVDS-M Mode</b> Selects reduced frequency mode “LVDS-M” of the receiver. This mode reduces the static current of the RX pad. The max data rate is reduced to 160 Mbps (80 MHz). 0 <sub>B</sub> LVDS-H Mode 1 <sub>B</sub> LVDS-M Mode
<b>PS</b>	7	rw	<b>Pad Supply Selection</b> Selects between 5V or 3.3V supply on V <sub>EXT</sub> for the pad-pair. Used in RX and TX pads! 0 <sub>B</sub> 3.3V supply 1 <sub>B</sub> 5V supply

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	8, 9, 11:10, 12, 13, 14, 15, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 235 Access Mode Restrictions of P14\_LPCR<sub>x</sub> (x=5) sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM	write access for enabled masters
Otherwise (default)	r	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM	

**Table 236 Reset Values of P14\_LPCR<sub>x</sub> (x=5)**

Reset Type	Reset Value	Note
After SSW execution	0000 0000 0000 0000 0000 0000 11XX X000 <sub>B</sub>	Initial value of RX depends on trimming

### P21\_LPCR<sub>x</sub> (x=0-1)

**Port 21 LVDS Pad Control Register x** **(0A0<sub>H</sub>+x\*4)** **Reset Value: Table 238**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0		0	0	PS	LVDS M	LRXTERM	TERM	RX_EN	REN_C TRL		
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
REN_CTRL	0	rw	<b>LVDS RX_EN controller</b> The LVDS RX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). 0 <sub>B</sub> Port controlled 1 <sub>B</sub> HSCT controlled

### General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
RX_EN	1	rw	<p><b>Enable Receive LVDS</b></p> <p>Enable the receive LVDS / disable CMOS path. If this bit is set to 0 – no transfer from the LVDS sender can be received and the receiver LVDS is in low power state.</p> <p>0<sub>B</sub> disable LVDS / enable CMOS mode (reserved for pads without CMOS input stage)</p> <p>1<sub>B</sub> enable LVDS / disable CMOS mode</p>
TERM	2	rw	<p><b>Select Receiver Termination Mode</b></p> <p>Selects a suitable internal load resistor between both pads.</p> <p>0<sub>B</sub> external termination - on the PCB</p> <p>1<sub>B</sub> 100 Ω Receiver internal termination</p>
LRXTERM	5:3	rw	<p><b>LVDS RX Poly-resistor configuration value</b></p> <p>Programming bits for the on die poly resistor termination. The value is configured during production test. Each chip configuration on this bit field is unique and configured during production testing.</p> <p><i>Note:</i> The configuration value shall not be changed by user after start-up for a guaranteed behavior.</p>
LVDSM	6	rw	<p><b>LVDS-M Mode</b></p> <p>Selects reduced frequency mode “LVDS-M” of the receiver. This mode reduces the static current of the RX pad. The max data rate is reduced to 160 Mbps (80 MHz).</p> <p>0<sub>B</sub> LVDS-H Mode</p> <p>1<sub>B</sub> LVDS-M Mode</p>
PS	7	rw	<p><b>Pad Supply Selection</b></p> <p>Selects between 5V or 3.3V supply on <math>V_{EXT}</math> for the pad-pair. Used in RX and TX pads!</p> <p>0<sub>B</sub> 3.3V supply</p> <p>1<sub>B</sub> 5V supply</p>
0	8, 9, 11:10, 12, 13, 14, 15, 31:16	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0</p>

**Table 237 Access Mode Restrictions of P21\_LPCRx (x=0-1) sorted by descending priority**

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM
Otherwise (default)	r	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 238 Reset Values of P21\_LPCR<sub>x</sub> (x=0-1)**

Reset Type	Reset Value	Note
After SSW execution	0000 0000 0000 0000 0000 0000 11XX X000 <sub>B</sub>	Initial value of RX depends on trimming

### P21\_LPCR<sub>x</sub> (x=2)

**Port 21 LVDS Pad Control Register x** **(0A0<sub>H</sub>+x\*4)** **Reset Value: Table 240**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>TX_P WDPD</b>	<b>TX_PD</b>	<b>VOSEX T</b>	<b>VOSDY N</b>	<b>VDIFFADJ</b>	<b>TX_EN</b>	<b>TEN_C TRL</b>	<b>PS</b>	<b>0</b>		<b>0</b>		<b>0</b>	<b>0</b>	<b>0</b>	
rw	rw	rw	rw	rw	rw	rw	rw	r		r		r	r	r	r

Field	Bits	Type	Description
<b>PS</b>	7	rw	<b>Pad Supply Selection</b> Selects between 5V or 3.3V supply on $V_{EXT}$ for the pad-pair. Used in RX and TX pads! $0_B$ 3.3V supply $1_B$ 5V supply
<b>TEN_CTRL</b>	8	rw	<b>LVDS TX_EN controller</b> The LVDS TX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). $0_B$ Port controlled $1_B$ HSCT controlled
<b>TX_EN</b>	9	rw	<b>Enable Transmit LVDS</b> Enable the transmit LVDS / disable CMOS path. If this bit is set to 0 - no transfer on LVDS data path can be initiated and the LVDS driver is disabled (powered down). $0_B$ disable LVDS / enable CMOS mode $1_B$ enable LVDS / disable CMOS mode
<b>VDIFFADJ</b>	11:10	rw	<b>LVDS Output Amplitude Tuning</b> With these two configuration bits the LVDS output current/amplitude can be adjusted. The voltage swing depending on VDIFFADJ setting is documented in the Data Sheet, see parameter $V_{OD}$ .
<b>VOSDYN</b>	12	rw	<b>Tune Bit of VOS Control Loop Static/Dynamic</b> Tune bit to change $V_{OS}$ control loop between static and dynamic mode. Don't change reset value.
<b>VOSEXT</b>	13	rw	<b>Tune Bit of VOS Control Loop Internal/External</b> Tune bit to change $V_{OS}$ control loop. Don't change reset value.

### General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>TX_PD</b>	14	rw	<b>LVDS Power Down</b> Unused in this device. LVDS disabled by TX_EN means power down. $0_B$ LVDS power on $1_B$ LVDS power down (default)
<b>TX_PWDPD</b>	15	rw	<b>Enable TX Power down pull down.</b> This function disables or enables the LVDS pull down resistor. The application code must disable TX power down pull down resistor with a power up. With a LVDS Power Down configuration the pull down function must be enabled, if required. $0_B$ disabled TX Power down pull down resistor. $1_B$ enabled TX Power down pull down resistor.
<b>0</b>	0, 1, 2, 5:3, 6, 31:16	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 239 Access Mode Restrictions of P21\_LPCR<sub>x</sub> (x=2) sorted by descending priority**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT	write access for enabled masters
Otherwise (default)	r	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT	

**Table 240 Reset Values of P21\_LPCR<sub>x</sub> (x=2)**

Reset Type	Reset Value	Note
After SSW execution	0000 5480 <sub>H</sub>	Initial value of RX depends on trimming

### P22\_LPCR<sub>x</sub> (x=1)

**Port 22 LVDS Pad Control Register x** (0A0<sub>H</sub>+x\*4) Reset Value: [Table 242](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>															
<b>TX_PWDPD</b>	<b>TX_PD</b>	<b>VOSEX<sub>T</sub></b>	<b>VOSDY<sub>N</sub></b>	<b>VDIFFADJ</b>	<b>TX_EN</b>	<b>TEN_CTRL</b>	<b>PS</b>	<b>0</b>							
rw	rw	rw	rw	rw	rw	rw	r	r	r	r	r	r	r	r	r

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
<b>PS</b>	7	rw	<p><b>Pad Supply Selection</b>            Selects between 5V or 3.3V supply on <math>V_{EXT}</math> for the pad-pair. Used in RX and TX pads!</p> <p><math>0_B</math> 3.3V supply  <math>1_B</math> 5V supply</p>
<b>TEN_CTRL</b>	8	rw	<p><b>LVDS TX_EN controller</b>            The LVDS TX_EN control function can be selected from the Port (default) or HSCT module (where this is connected).</p> <p><math>0_B</math> Port controlled. Additionally the data path is switched from HSCT to port multiplexer controlled by IOCR.  <math>1_B</math> HSCT controlled</p>
<b>TX_EN</b>	9	rw	<p><b>Enable Transmit LVDS</b>            Enable the transmit LVDS / disable CMOS path. If this bit is set to 0 - no transfer on LVDS data path can be initiated and the LVDS driver is disabled (powered down).</p> <p><math>0_B</math> disable LVDS / enable CMOS mode  <math>1_B</math> enable LVDS / disable CMOS mode</p>
<b>VDIFFADJ</b>	11:10	rw	<p><b>LVDS Output Amplitude Tuning</b>            With these two configuration bits the LVDS output current/amplitude can be adjusted. The voltage swing depending on VDIFFADJ setting is documented in the Data Sheet, see parameter <math>V_{OD}</math>.</p>
<b>VOSDYN</b>	12	rw	<p><b>Tune Bit of VOS Control Loop Static/Dynamic</b>            Tune bit to change <math>V_{OS}</math> control loop between static and dynamic mode.            Don't change reset value.</p>
<b>VOSEXT</b>	13	rw	<p><b>Tune Bit of VOS Control Loop Internal/External</b>            Tune bit to change <math>V_{OS}</math> control loop.            Don't change reset value.</p>
<b>TX_PD</b>	14	rw	<p><b>LVDS Power Down</b>            Unused in this device. LVDS disabled by TX_EN means power down.</p> <p><math>0_B</math> LVDS power on  <math>1_B</math> LVDS power down (default)</p>
<b>TX_PWDPD</b>	15	rw	<p><b>Enable TX Power down pull down.</b>            This function disables or enables the LVDS pull down resistor. The application code must disable TX power down pull down resistor with a power up. With a LVDS Power Down configuration the pull down function must be enabled, if required.</p> <p><math>0_B</math> disabled TX Power down pull down resistor.  <math>1_B</math> enabled TX Power down pull down resistor.</p>
<b>0</b>	0, 1, 2, 5:3, 6, 31:16	r	<p><b>Reserved</b>            Read as 0; should be written with 0</p>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 241 Access Mode Restrictions of P22\_LPCR<sub>x</sub> (x=1) sorted by descending priority**

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT
Otherwise (default)	r	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT

**Table 242 Reset Values of P22\_LPCR<sub>x</sub> (x=1)**

Reset Type	Reset Value	Note
After SSW execution	0000 5480 <sub>H</sub>	Initial value of RX depends on trimming

### Port 00 Access Enable Register 1

Each port has its own dedicated ACCEN0 and ACCEN1 registers.

The Access Enable Register 1 controls write<sup>1)</sup> access for transactions with the on chip bus master TAG ID 100000B to 111111B (see On Chip Bus chapter for the products TAG ID <-> master peripheral mapping). The BPI\_FPI is prepared for a 6-bit TAG ID. ACCEN1 is not implemented with register bits as the related TAG IDs are not used in this product.

Mapping of TAG IDs to ACCEN1.ENx: EN0 -> TAG ID 100000B, EN1 -> TAG ID 100001B, ... ,EN31 -> TAG ID 111111B.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

### P00\_ACCEN1

**Port 00 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P01\_ACCEN1

**Port 01 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P02\_ACCEN1

**Port 02 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P10\_ACCEN1

**Port 10 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P11\_ACCEN1

**Port 11 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P12\_ACCEN1

**Port 12 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P13\_ACCEN1

**Port 13 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P14\_ACCEN1

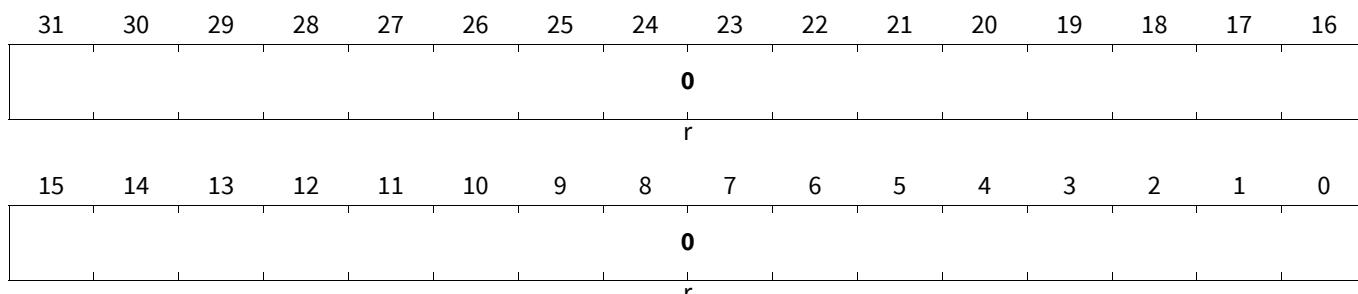
**Port 14 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P15\_ACCEN1

**Port 15 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

### P20\_ACCEN1

**Port 20 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>



Field	Bits	Type	Description
0	31:0	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 243 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_ACCEN1](#)

Applies to [P01\\_ACCEN1](#)

Applies to [P02\\_ACCEN1](#)

Applies to [P10\\_ACCEN1](#)

Applies to [P11\\_ACCEN1](#)

Applies to [P12\\_ACCEN1](#)

Applies to [P13\\_ACCEN1](#)

Applies to [P14\\_ACCEN1](#)

Applies to [P15\\_ACCEN1](#)

Applies to [P20\\_ACCEN1](#)

Mode Name	Access Mode	Description
Supervisor Mode and Safety ENDINIT	-	See bit field definitions above write access only for masters with supervisor mode
Otherwise (default)	-	See bit field definitions above

### P21\_ACCEN1

**Port 21 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P22\_ACCEN1

**Port 22 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P23\_ACCEN1

**Port 23 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P24\_ACCEN1

**Port 24 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P25\_ACCEN1

**Port 25 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P26\_ACCEN1

**Port 26 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P30\_ACCEN1

**Port 30 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P31\_ACCEN1

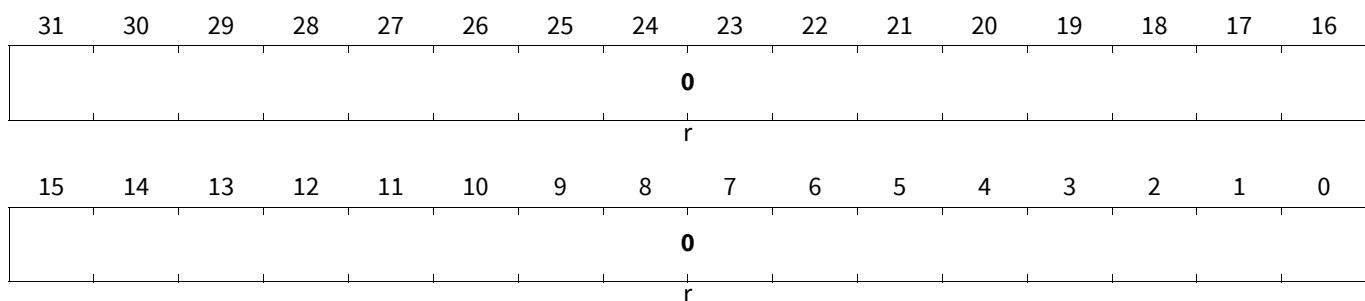
**Port 31 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P32\_ACCEN1

**Port 32 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**

### P33\_ACCEN1

**Port 33 Access Enable Register 1** (0F8<sub>H</sub>) **Application Reset Value: 0000 0000<sub>H</sub>**



## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	31:0	r	<b>Reserved</b> Read as 0; should be written with 0

**Table 244 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_ACCEN1](#)

Applies to [P22\\_ACCEN1](#)

Applies to [P23\\_ACCEN1](#)

Applies to [P24\\_ACCEN1](#)

Applies to [P25\\_ACCEN1](#)

Applies to [P26\\_ACCEN1](#)

Applies to [P30\\_ACCEN1](#)

Applies to [P31\\_ACCEN1](#)

Applies to [P32\\_ACCEN1](#)

Applies to [P33\\_ACCEN1](#)

Mode Name	Access Mode	Description
Supervisor Mode and Safety ENDINIT	-	See bit field definitions above write access only for masters with supervisor mode
Otherwise (default)	-	See bit field definitions above

### P34\_ACCEN1

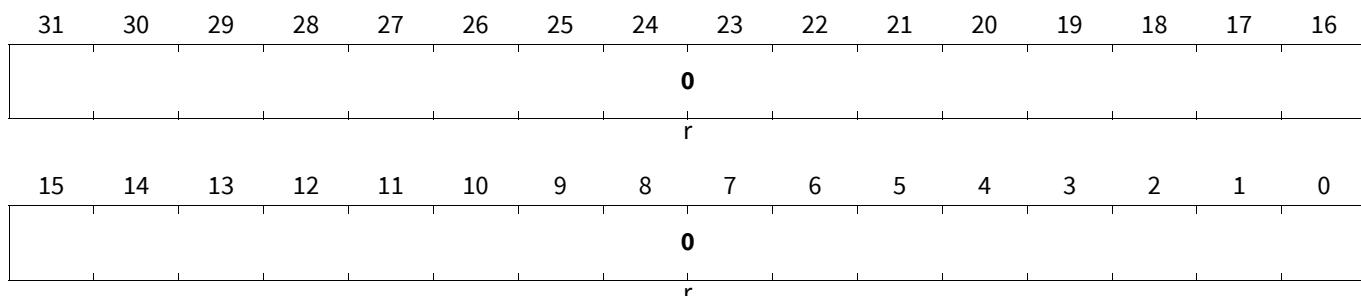
**Port 34 Access Enable Register 1** **Application Reset Value: 0000 0000<sub>H</sub>** (0F8<sub>H</sub>)

### P40\_ACCEN1

**Port 40 Access Enable Register 1** **Application Reset Value: 0000 0000<sub>H</sub>** (0F8<sub>H</sub>)

### P41\_ACCEN1

**Port 41 Access Enable Register 1** **Application Reset Value: 0000 0000<sub>H</sub>** (0F8<sub>H</sub>)



Field	Bits	Type	Description
0	31:0	r	<b>Reserved</b> Read as 0; should be written with 0

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 245 Access Mode Restrictions sorted by descending priority**

Applies to [P34\\_ACCEN1](#)

Applies to [P40\\_ACCEN1](#)

Applies to [P41\\_ACCEN1](#)

Mode Name	Access Mode	Description
Supervisor Mode and Safety ENDINIT	-	See bit field definitions above write access only for masters with supervisor mode
Otherwise (default)	-	See bit field definitions above

### Port 00 Access Enable Register 0

Each port has its own dedicated ACCEN0 and ACCEN1 registers.

The Access Enable Register 0 controls write<sup>1)</sup> access for transactions with the on chip bus master TAG ID 000000B to 011111B (see On Chip Bus chapter for the products TAG ID <-> master peripheral mapping). The BPI\_FPI is prepared for a 6-bit TAG ID. The registers ACCEN0 and ACCEN1 are providing one enable bit for each possible 6-bit TAG ID encoding.

Mapping of TAG IDs to ACCEN0.ENx: EN0 -> TAG ID 000000B, EN1 -> TAG ID 000001B , ... ,EN31 -> TAG ID 011111B.

1) The BPI\_FPI Access Enable functionality controls only write transactions to the kernel registers. Read transactions are not influenced. SW has to take care for destructive/modifying read functionality in kernel registers.

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00\_ACCENO

Port 00 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P01\_ACCENO

Port 01 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P02\_ACCENO

Port 02 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P10\_ACCENO

Port 10 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P11\_ACCENO

Port 11 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P12\_ACCENO

Port 12 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P13\_ACCENO

Port 13 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P14\_ACCENO

Port 14 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P15\_ACCENO

Port 15 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

P20\_ACCENO

Port 20 Access Enable Register 0 (0FC<sub>H</sub>) Application Reset Value: FFFF FFFF<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN31	EN30	EN29	EN28	EN27	EN26	EN25	EN24	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	ENO
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-31)	x	rw	<p><b>Access Enable for Master TAG ID x</b></p> <p>This bit enables write access to the module kernel addresses for transactions with the Master TAG ID n</p> <p>0<sub>B</sub> Write access will not be executed 1<sub>B</sub> Write access will be executed</p>

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

**Table 246 Access Mode Restrictions sorted by descending priority**

Applies to [P00\\_ACCENO](#)

Applies to [P01\\_ACCENO](#)

Applies to [P02\\_ACCENO](#)

Applies to [P10\\_ACCENO](#)

Applies to [P11\\_ACCENO](#)

Applies to [P12\\_ACCENO](#)

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Applies to [P23](#)

## General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
ENx (x=0-31)	x	rw	<p><b>Access Enable for Master TAG ID x</b></p> <p>This bit enables write access to the module kernel addresses for transactions with the Master TAG ID n</p> <p>0<sub>B</sub> Write access will not be executed 1<sub>B</sub> Write access will be executed</p>

**Table 247 Access Mode Restrictions sorted by descending priority**

Applies to [P21\\_ACCENO](#)

Applies to [P22\\_ACCENO](#)

Applies to [P23\\_ACCENO](#)

Applies to [P24\\_ACCENO](#)

Applies to [P25\\_ACCENO](#)

Applies to [P26\\_ACCENO](#)

Applies to [P30\\_ACCENO](#)

Applies to [P31\\_ACCENO](#)

Applies to [P32\\_ACCENO](#)

Applies to [P33\\_ACCENO](#)

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	rw	ENx (x=0-31)	write access only for masters with supervisor mode
Otherwise (default)	r	ENx (x=0-31)	

### P34\_ACCENO

**Port 34 Access Enable Register 0** (0FC<sub>H</sub>) **Application Reset Value: FFFF FFFF<sub>H</sub>**

### P40\_ACCENO

**Port 40 Access Enable Register 0** (0FC<sub>H</sub>) **Application Reset Value: FFFF FFFF<sub>H</sub>**

### P41\_ACCENO

**Port 41 Access Enable Register 0** (0FC<sub>H</sub>) **Application Reset Value: FFFF FFFF<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN31	EN30	EN29	EN28	EN27	EN26	EN25	EN24	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	ENO

Field	Bits	Type	Description
ENx (x=0-31)	x	rw	<p><b>Access Enable for Master TAG ID x</b></p> <p>This bit enables write access to the module kernel addresses for transactions with the Master TAG ID n</p> <p>0<sub>B</sub> Write access will not be executed 1<sub>B</sub> Write access will be executed</p>

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**
**Table 248 Access Mode Restrictions sorted by descending priority**Applies to [P34\\_ACCEN0](#)Applies to [P40\\_ACCEN0](#)Applies to [P41\\_ACCEN0](#)

<b>Mode Name</b>	<b>Access Mode</b>		<b>Description</b>
Supervisor Mode and Safety ENDINIT	rw	ENx (x=0-31)	write access only for masters with supervisor mode
Otherwise (default)	r	ENx (x=0-31)	

## 14.4 Connectivity

The connectivity of the Ports is documented in the Pinning documentation of each device.

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**General Purpose I/O Ports and Peripheral I/O Lines (Ports)**

## 14.5 Revision History

**Table 249 Revision History V1.8.19 to the latest revision**

Reference	Changes to Previous Version	Comment
<b>V1.8.20</b>		
<a href="#">Page 163</a>	Revision History entries up to V1.8.19 removed.	
<a href="#">Page 52</a>	Removed confusing phrase “, only input selection apply.” from register IOCRx from bitfield description of PC.	
-	Only cosmetic change: register documentation generator merges more reserved bit fields (e.g. “0” or “1” bit fields).	
<b>V1.8.21</b>		
-	No content of this Appx changed. TC3Ax Appx added to delivery package and change in Feature List of family chapter.	

## Safety Management Unit (SMU)

# 15 Safety Management Unit (SMU)

This chapter describes the Safety Management Unit (short SMU) module of the TC39x-B.

## 15.1 TC39x-B Specific IP Configuration

See features in family spec.

## 15.2 TC39x-B Specific Register Set

### SMU\_core Specific Register Set

The following tables show an overview of the SMU\_core registers and their address space.

#### Register Address Space Table

**Table 250 Register Address Space - SMU**

Module	Base Address	End Address	Note
SMU	F0036800 <sub>H</sub>	F0036FFF <sub>H</sub>	FPI slave interface

#### Register Overview Table

**Table 251 Register Overview - SMU (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SMU_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
SMU_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SMU_CMD	Command Register	020 <sub>H</sub>	U,SV	SV,P,32	Application Reset	See Family Spec
SMU_STS	Status Register	024 <sub>H</sub>	U,SV	SV,P,32	Application Reset	See Family Spec
SMU_FSP	Fault Signaling Protocol	028 <sub>H</sub>	U,SV	SV,P,SE,32	PowerOn Reset	See Family Spec
SMU_AGC	Alarm Global Configuration	02C <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec

**Safety Management Unit (SMU)****Table 251 Register Overview - SMU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SMU_RTC	Recovery Timer Configuration	030 <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_KEYS	Key Register	034 <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_DBG	Debug Register	038 <sub>H</sub>	U,SV	BE	PowerOn Reset	See Family Spec
SMU_PCTL	Port Control	03C <sub>H</sub>	U,SV	SV,P,SE,32	PowerOn Reset	See Family Spec
SMU_AFCNT	Alarm and Fault Counter	040 <sub>H</sub>	U,SV	BE	PowerOn Reset	See Family Spec
SMU_RTAC00	Recovery Timer 0 Alarm Configuration 0	060 <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC01	Recovery Timer 0 Alarm Configuration 1	064 <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC10	Recovery Timer 1 Alarm Configuration 0	068 <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC11	Recovery Timer 1 Alarm Configuration 1	06C <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_AEX	Alarm Executed Status Register	070 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
SMU_AEXCLR	Alarm Executed Status Clear Register	074 <sub>H</sub>	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_AGiCFj (i=0-5;j=0-2) (i=6;j=0-2) (i=7;j=0-2) (i=8;j=0-2) (i=9;j=0-2) (i=10;j=0-2) (i=11;j=0-2)	Alarm Configuration Register	100 <sub>H</sub> +i*1 2+j*4	U,SV	SV,P,SE,32	Application Reset	4
SMU_AGiFSP (i=0-11)	SMU_core FSP Configuration Register	190 <sub>H</sub> +i*4	U,SV	SV,P,SE,32	Application Reset	8

## Safety Management Unit (SMU)

**Table 251 Register Overview - SMU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SMU_AGi (i=0-11)	Alarm Status Register	$1C0_H + i * 4$	U,SV	SV,P,SE,32	Application Reset	<a href="#">11</a>
SMU_ADi (i=0-11)	Alarm Debug Register	$200_H + i * 4$	U,SV	BE	PowerOn Reset	<a href="#">14</a>
SMU_RMCTL	Register Monitor Control	$300_H$	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RMEF	Register Monitor Error Flags	$304_H$	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RMSTS	Register Monitor Self Test Status	$308_H$	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_OCS	OCDS Control and Status	$7E8_H$	U,SV	SV,P,OEN	Debug Reset	See Family Spec
SMU_ACCEN1	SMU_core Access Enable Register 1	$7F8_H$	U,SV	BE	Application Reset	See Family Spec
SMU_ACCEN0	SMU_core Access Enable Register 0	$7FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

### SMU\_stdby Specific Register Set

For SMU\_stdby specific register set refer to the Power Management System chapter.

## 15.3 TC39x-B Specific Registers

## Safety Management Unit (SMU)

### 15.3.1 TC39x-B Specific Registers

#### 15.3.1.1 FPI slave interface

##### Alarm Configuration Register

**SMU\_AGiCFj (i=0-5;j=0-2)**

Alarm Configuration Register

( $100_H + i * 12 + j * 4$ )

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	CF24	CF23	CF22	0	0	0	0	0	0
r	r	r	r	r	r	r	rw	rw	rw	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	0	CF2	CF1	CF0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-2,4-14,22-24)	z	rw	<b>Configuration flag x (x=0-2) for alarm z belonging to alarm group i.</b> The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 <sub>B</sub> Configuration flag x (x=0-2) is set to 0 1 <sub>B</sub> Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGiCFj (i=6;j=0-2)**

Alarm Configuration Register

( $100_H + i * 12 + j * 4$ )

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	CF25	CF24	CF23	0	CF21	CF20	CF19	CF18	CF17	CF16
r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	CF14	CF13	CF12	CF11	CF10	0	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

## Safety Management Unit (SMU)

Field	Bits	Type	Description
CFz (z=0-8,10-21,23-25)	z	rw	<b>Configuration flag x (x=0-2) for alarm z belonging to alarm group i.</b> The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 <sub>B</sub> Configuration flag x (x=0-2) is set to 0 1 <sub>B</sub> Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 22, 9	r	<b>Reserved</b> Read as 0; should be written with 0.

## SMU\_AGiCFj (i=7;j=0-2)

Alarm Configuration Register      (100<sub>H</sub>+i\*12+j\*4)      Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24	CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	CF14	CF13	CF12	0	0	0	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
rw	rw	rw	rw	r	r	r	rw								

Field	Bits	Type	Description
CFz (z=0-8,12-31)	z	rw	<b>Configuration flag x (x=0-2) for alarm z belonging to alarm group i.</b> The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 <sub>B</sub> Configuration flag x (x=0-2) is set to 0 1 <sub>B</sub> Configuration flag x (x=0-2) is set to 1
0	11, 10, 9	r	<b>Reserved</b> Read as 0; should be written with 0.

## SMU\_AGiCFj (i=8;j=0,2)

Alarm Configuration Register      (100<sub>H</sub>+i\*12+j\*4)      Application Reset Value: 0001 FC00<sub>H</sub>

## SMU\_AGiCFj (i=8;j=1)

Alarm Configuration Register      (100<sub>H</sub>+i\*12+j\*4)      Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF31	CF30	CF29	CF28	CF27	CF26	CF25	0	CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
rw	rw	rw	rw	rw	rw	rw	r	rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

**Safety Management Unit (SMU)**

Field	Bits	Type	Description
CFz (z=0-23,25-31)	z	rw	<b>Configuration flag x (x=0-2) for alarm z belonging to alarm group i.</b> The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 <sub>B</sub> Configuration flag x (x=0-2) is set to 0 1 <sub>B</sub> Configuration flag x (x=0-2) is set to 1
0	24	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGiCFj (i=9;j=0-2)****Alarm Configuration Register****(100<sub>H</sub>+i\*12+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>CF31</b>	<b>CF30</b>	<b>CF29</b>	<b>CF28</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>CF23</b>	<b>CF22</b>	<b>CF21</b>	<b>CF20</b>	<b>0</b>	<b>0</b>	<b>CF17</b>	<b>CF16</b>
rw	rw	rw	rw	r	r	r	r	rw	rw	rw	rw	r	r	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CF15</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>CF5</b>	<b>0</b>	<b>CF3</b>	<b>0</b>	<b>CF1</b>	<b>CF0</b>
rw	r	r	r	r	r	r	r	r	r	rw	r	rw	r	rw	rw

Field	Bits	Type	Description
CFz (z=0-1,3,5,15-17,20-23,28-31)	z	rw	<b>Configuration flag x (x=0-2) for alarm z belonging to alarm group i.</b> The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 <sub>B</sub> Configuration flag x (x=0-2) is set to 0 1 <sub>B</sub> Configuration flag x (x=0-2) is set to 1
0	27, 26, 25, 24, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	<b>Reserved</b> Read as 0; should be written with 0.

## Safety Management Unit (SMU)

**SMU\_AGiCFj (i=10;j=0)****Alarm Configuration Register** $(100_H + i * 12 + j * 4)$ **Application Reset Value: 0000 0000<sub>H</sub>****SMU\_AGiCFj (i=10;j=1-2)****Alarm Configuration Register** $(100_H + i * 12 + j * 4)$ **Application Reset Value: 0003 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>CF22</b>	<b>CF21</b>	<b>CF20</b>	<b>0</b>	<b>CF18</b>	<b>CF17</b>	<b>CF16</b>
r	r	r	r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CF15</b>	<b>CF14</b>	<b>CF13</b>	<b>CF12</b>	<b>CF11</b>	<b>CF10</b>	<b>CF9</b>	<b>CF8</b>	<b>CF7</b>	<b>CF6</b>	<b>CF5</b>	<b>CF4</b>	<b>CF3</b>	<b>CF2</b>	<b>CF1</b>	<b>CF0</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>CFz (z=0-18,20-22)</b>	<b>z</b>	<b>rw</b>	<b>Configuration flag x (x=0-2) for alarm z belonging to alarm group i.</b> The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group.  $0_B$ Configuration flag x (x=0-2) is set to 0 $1_B$ Configuration flag x (x=0-2) is set to 1
<b>0</b>	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGiCFj (i=11;j=0-2)****Alarm Configuration Register** $(100_H + i * 12 + j * 4)$ **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>0</b>	<b>CF13</b>	<b>CF12</b>	<b>CF11</b>	<b>CF10</b>	<b>CF9</b>	<b>CF8</b>	<b>CF7</b>	<b>CF6</b>	<b>CF5</b>	<b>CF4</b>	<b>CF3</b>	<b>CF2</b>	<b>CF1</b>	<b>CF0</b>
r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>CFz (z=0-13)</b>	<b>z</b>	<b>rw</b>	<b>Configuration flag x (x=0-2) for alarm z belonging to alarm group i.</b> The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group.  $0_B$ Configuration flag x (x=0-2) is set to 0 $1_B$ Configuration flag x (x=0-2) is set to 1

**Safety Management Unit (SMU)**

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_core FSP Configuration Register****SMU\_AGiFSP (i=0-5)****SMU\_core FSP Configuration Register (190<sub>H</sub>+i\*4) Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	FE24	FE23	FE22	0	0	0	0	0	0
r	r	r	r	r	r	r	rw	rw	rw	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FE14	FE13	FE12	FE11	FE10	FE9	FE8	FE7	FE6	FE5	FE4	0	FE2	FE1	FE0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-2,4-14,22-24)	z	rw	<b>Fault signaling configuration flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> FSP disabled for this alarm event 1 <sub>B</sub> FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGiFSP (i=6)****SMU\_core FSP Configuration Register (190<sub>H</sub>+i\*4) Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	FE25	FE24	FE23	0	FE21	FE20	FE19	FE18	FE17	FE16
r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	FE14	FE13	FE12	FE11	FE10	0	FE8	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

## **Safety Management Unit (SMU)**

Field	Bits	Type	Description
<b>FEz (z=0-8,10-21,23-25)</b>	z	rw	<p><b>Fault signaling configuration flag for alarm z belonging to alarm group i.</b></p> <p><math>0_B</math> FSP disabled for this alarm event  <math>1_B</math> FSP enabled for this alarm event</p>
<b>0</b>	31, 30, 29, 28, 27, 26, 22, 9	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

SMU\_AGiFSP (i=7)

## **SMU\_core FSP Configuration Register**

(190<sub>H</sub>+i\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
<b>FEz (z=0-8,12-31)</b>	z	rw	<p><b>Fault signaling configuration flag for alarm z belonging to alarm group i.</b></p> <p>0<sub>B</sub> FSP disabled for this alarm event 1<sub>B</sub> FSP enabled for this alarm event</p>
<b>0</b>	11, 10, 9	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

**SMU\_AGiFSP (i=8)**

## **SMU\_core FSP Configuration Register**

(190<sub>H</sub>+i\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
FEz (z=0-23,25-31)	z	rw	<p><b>Fault signaling configuration flag for alarm z belonging to alarm group i.</b></p> <p>0<sub>B</sub> FSP disabled for this alarm event</p> <p>1<sub>B</sub> FSP enabled for this alarm event</p>

**Safety Management Unit (SMU)**

Field	Bits	Type	Description
0	24	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGiFSP (i=9)**
**SMU\_core FSP Configuration Register** **(190<sub>H</sub>+i\*4)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FE31	FE30	FE29	FE28	0	0	0	0	FE23	FE22	FE21	FE20	0	0	FE17	FE16
rw	rw	rw	rw	r	r	r	r	rw	rw	rw	rw	r	r	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	0	0	0	0	0	0	0	0	0	FE5	0	FE3	0	FE1	FE0
rw	r	r	r	r	r	r	r	r	r	rw	r	rw	r	rw	rw

Field	Bits	Type	Description
FEz (z=0-1,3,5,15-17,20-23,28-31)	z	rw	<b>Fault signaling configuration flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> FSP disabled for this alarm event 1 <sub>B</sub> FSP enabled for this alarm event
0	27, 26, 25, 24, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGiFSP (i=10)**
**SMU\_core FSP Configuration Register** **(190<sub>H</sub>+i\*4)** **Application Reset Value: 0003 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	FE22	FE21	FE20	0	FE18	FE17	FE16
r	r	r	r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-18,20-22)	z	rw	<b>Fault signaling configuration flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> FSP disabled for this alarm event 1 <sub>B</sub> FSP enabled for this alarm event

**Safety Management Unit (SMU)**

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGiFSP (i=11)**

**SMU\_core FSP Configuration Register** **(190<sub>H</sub>+i\*4)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	FE13	FE12	FE11	FE10	FE9	FE8	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-13)	z	rw	<b>Fault signaling configuration flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> FSP disabled for this alarm event 1 <sub>B</sub> FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14	r	<b>Reserved</b> Read as 0; should be written with 0.

**Alarm Status Register**

Refer to Alarm Status Registers for the conditions to set and reset the status flag by software.

**SMU\_AGi (i=0-5)**

**Alarm Status Register** **(1C0<sub>H</sub>+i\*4)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	SF24	SF23	SF22	0	0	0	0	0	0
r	r	r	r	r	r	r	rwh	rwh	rwh	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SF14	SF13	SF12	SF11	SF10	SF9	SF8	SF7	SF6	SF5	SF4	0	SF2	SF1	SF0
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh

## Safety Management Unit (SMU)

Field	Bits	Type	Description
SFz (z=0-2,4-14,22-24)	z	rwh	<b>Status flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	<b>Reserved</b> Read as 0; should be written with 0.

## SMU\_AGi (i=6)

## Alarm Status Register

(1C0<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	SF25	SF24	SF23	0	SF21	SF20	SF19	SF18	SF17	SF16
r	r	r	r	r	r	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	SF14	SF13	SF12	SF11	SF10	0	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-8,10-21,23-25)	z	rwh	<b>Status flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 22, 9	r	<b>Reserved</b> Read as 0; should be written with 0.

## SMU\_AGi (i=7)

## Alarm Status Register

(1C0<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SF31	SF30	SF29	SF28	SF27	SF26	SF25	SF24	SF23	SF22	SF21	SF20	SF19	SF18	SF17	SF16
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	SF14	SF13	SF12	0	0	0	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
rwh	rwh	rwh	rwh	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-8,12-31)	z	rwh	<b>Status flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition

**Safety Management Unit (SMU)**

Field	Bits	Type	Description
0	11, 10, 9	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGi (i=8)**
**Alarm Status Register** **(1C0<sub>H</sub>+i\*4)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SF31</b>	<b>SF30</b>	<b>SF29</b>	<b>SF28</b>	<b>SF27</b>	<b>SF26</b>	<b>SF25</b>	<b>0</b>	<b>SF23</b>	<b>SF22</b>	<b>SF21</b>	<b>SF20</b>	<b>SF19</b>	<b>SF18</b>	<b>SF17</b>	<b>SF16</b>
rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SF15</b>	<b>SF14</b>	<b>SF13</b>	<b>SF12</b>	<b>SF11</b>	<b>SF10</b>	<b>SF9</b>	<b>SF8</b>	<b>SF7</b>	<b>SF6</b>	<b>SF5</b>	<b>SF4</b>	<b>SF3</b>	<b>SF2</b>	<b>SF1</b>	<b>SF0</b>
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
<b>SFz (z=0-23,25-31)</b>	z	rwh	<b>Status flag for alarm z belonging to alarm group i.</b> $0_B$ Status flag z does not report a fault condition $1_B$ Status flag z reports a fault condition
0	24	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGi (i=9)**
**Alarm Status Register** **(1C0<sub>H</sub>+i\*4)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SF31</b>	<b>SF30</b>	<b>SF29</b>	<b>SF28</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>SF23</b>	<b>SF22</b>	<b>SF21</b>	<b>SF20</b>	<b>0</b>	<b>0</b>	<b>SF17</b>	<b>SF16</b>
rwh	rwh	rwh	rwh	r	r	r	r	rwh	rwh	rwh	rwh	r	r	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SF15</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>SF5</b>	<b>0</b>	<b>SF3</b>	<b>0</b>	<b>SF1</b>	<b>SF0</b>
rwh	r	r	r	r	r	r	r	r	r	rwh	r	rwh	r	rwh	rwh

Field	Bits	Type	Description
<b>SFz (z=0-1,3,5,15-17,20-23,28-31)</b>	z	rwh	<b>Status flag for alarm z belonging to alarm group i.</b> $0_B$ Status flag z does not report a fault condition $1_B$ Status flag z reports a fault condition
0	27, 26, 25, 24, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	<b>Reserved</b> Read as 0; should be written with 0.

**Safety Management Unit (SMU)****SMU\_AGi (i=10)****Alarm Status Register****(1C0<sub>H</sub>+i\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	SF22	SF21	SF20	0	SF18	SF17	SF16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	SF14	SF13	SF12	SF11	SF10	SF9	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0

Field	Bits	Type	Description
SFz (z=0-18,20-22)	z	rwh	<b>Status flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_AGi (i=11)****Alarm Status Register****(1C0<sub>H</sub>+i\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SF13	SF12	SF11	SF10	SF9	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0

Field	Bits	Type	Description
SFz (z=0-13)	z	rwh	<b>Status flag for alarm z belonging to alarm group i.</b> 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14	r	<b>Reserved</b> Read as 0; should be written with 0.

**Alarm Debug Register**

Note: Writing to this register has no effect

**Safety Management Unit (SMU)****SMU\_Ad*i* (i=0-5)****Alarm Debug Register**(200<sub>H</sub>+i\*4)PowerOn Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	DF24	DF23	DF22	0	0	0	0	0	0
r	r	r	r	r	r	r	rh	rh	rh	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DF14	DF13	DF12	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	0	DF2	DF1	DF0
r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-2,4-14,22-24)	z	rh	<p><b>Diagnosis flag for alarm z belonging to alarm group i.</b></p> <p>The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place.</p> <p>0<sub>B</sub> Status flag z does not report a fault condition</p> <p>1<sub>B</sub> Status flag z reports a fault condition</p>
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

**SMU\_Ad*i* (i=6)****Alarm Debug Register**(200<sub>H</sub>+i\*4)PowerOn Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	DF25	DF24	DF23	0	DF21	DF20	DF19	DF18	DF17	DF16
r	r	r	r	r	r	rh	rh	rh	r	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	DF14	DF13	DF12	DF11	DF10	0	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
rh	rh	rh	rh	rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-8,10-21,23-25)	z	rh	<p><b>Diagnosis flag for alarm z belonging to alarm group i.</b></p> <p>The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place.</p> <p>0<sub>B</sub> Status flag z does not report a fault condition</p> <p>1<sub>B</sub> Status flag z reports a fault condition</p>
0	31, 30, 29, 28, 27, 26, 22, 9	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

**Safety Management Unit (SMU)****SMU\_Ad*i* (i=7)****Alarm Debug Register**(200<sub>H</sub>+i\*4)PowerOn Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DF31	DF30	DF29	DF28	DF27	DF26	DF25	DF24	DF23	DF22	DF21	DF20	DF19	DF18	DF17	DF16
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	DF14	DF13	DF12	0	0	0	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
rh	rh	rh	rh	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-8,12-31)	z	rh	<b>Diagnosis flag for alarm z belonging to alarm group i.</b> The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
0	11, 10, 9	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_Ad*i* (i=8)****Alarm Debug Register**(200<sub>H</sub>+i\*4)PowerOn Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DF31	DF30	DF29	DF28	DF27	DF26	DF25	0	DF23	DF22	DF21	DF20	DF19	DF18	DF17	DF16
rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	DF14	DF13	DF12	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-23,25-31)	z	rh	<b>Diagnosis flag for alarm z belonging to alarm group i.</b> The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
0	24	r	<b>Reserved</b> Read as 0; should be written with 0.

**Safety Management Unit (SMU)****SMU\_Ad*i* (i=9)****Alarm Debug Register**(200<sub>H</sub>+i\*4)PowerOn Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>DF31</b>	<b>DF30</b>	<b>DF29</b>	<b>DF28</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>DF23</b>	<b>DF22</b>	<b>DF21</b>	<b>DF20</b>	<b>0</b>	<b>0</b>	<b>DF17</b>	<b>DF16</b>
rh	rh	rh	rh	r	r	r	r	rh	rh	rh	rh	r	r	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>DF15</b>	<b>0</b>	<b>DF5</b>	<b>0</b>	<b>DF3</b>	<b>0</b>	<b>DF1</b>	<b>DF0</b>								
rh	r	r	r	r	r	r	r	r	r	rh	r	rh	r	rh	rh

Field	Bits	Type	Description
<b>DFz (z=0-1,3,5,15-17,20-23,28-31)</b>	z	rh	<b>Diagnosis flag for alarm z belonging to alarm group i.</b> The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place.  0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
<b>0</b>	27, 26, 25, 24, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_Ad*i* (i=10)****Alarm Debug Register**(200<sub>H</sub>+i\*4)PowerOn Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>DF22</b>	<b>DF21</b>	<b>DF20</b>	<b>0</b>	<b>DF18</b>	<b>DF17</b>	<b>DF16</b>
r	r	r	r	r	r	r	r	r	rh	rh	rh	r	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>DF15</b>	<b>DF14</b>	<b>DF13</b>	<b>DF12</b>	<b>DF11</b>	<b>DF10</b>	<b>DF9</b>	<b>DF8</b>	<b>DF7</b>	<b>DF6</b>	<b>DF5</b>	<b>DF4</b>	<b>DF3</b>	<b>DF2</b>	<b>DF1</b>	<b>DF0</b>
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
<b>DFz (z=0-18,20-22)</b>	z	rh	<b>Diagnosis flag for alarm z belonging to alarm group i.</b> The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place.  0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition

**Safety Management Unit (SMU)**

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	<b>Reserved</b> Read as 0; should be written with 0.

**SMU\_Ad*i* (i=11)**

**Alarm Debug Register** (200<sub>H</sub>+i\*4) PowerOn Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	DF13	DF12	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-13)	z	rh	<b>Diagnosis flag for alarm z belonging to alarm group i.</b> The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 <sub>B</sub> Status flag z does not report a fault condition 1 <sub>B</sub> Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14	r	<b>Reserved</b> Read as 0; should be written with 0.

**15.4 TC39x-B Specific Alarm Mapping**

This section defines the mapping between the alarm signals at the input of the SMU in the TC39x-B and the alarm. For that purpose alarm groups are defined. There is a one-to-one relationship between an alarm group index ALM<n>[index] signal and the alarm configuration and status registers (AG<n>[index]). A group is made of up to 32 alarms; for convenience some entries may be reserved.

**15.4.1 TC39x-B Specific Pre-Alarms**

There are situations where it is not necessary to implement configuration and status registers for every internal alarm event; a typical case is a module with multiple SRAMs. For that, alarm inputs, called pre-alarms, are combined together with a logical OR internally in SMU. The result is then connected to the alarm group.

**Safety Management Unit (SMU)****MTU Pre-Alarm Mapping****Table 252 MTU Pre-Alarm Mapping**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
CPU0.DMEM - Correctable error CPU0.DLMU - Correctable error CPU0.DMEM1 - Correctable error	OR	<b>ALM0[9]</b>
CPU0.DMEM - Uncorrectable Critical error CPU0.DLMU - Uncorrectable Critical error CPU0.DMEM1 - Uncorrectable Critical error	OR	<b>ALM0[10]</b>
CPU0.DMEM - Miscellaneous error CPU0.DLMU - Miscellaneous error CPU0.DMEM1 - Miscellaneous error	OR	<b>ALM0[11]</b>
CPU1.DMEM - Correctable error CPU1.DLMU - Correctable error CPU1.DMEM1 - Correctable error	OR	<b>ALM1[9]</b>
CPU1.DMEM - Uncorrectable Critical error CPU1.DLMU - Uncorrectable Critical error CPU1.DMEM1 - Uncorrectable Critical error	OR	<b>ALM1[10]</b>
CPU1.DMEM - Miscellaneous error CPU1.DLMU - Miscellaneous error CPU1.DMEM1 - Miscellaneous error	OR	<b>ALM1[11]</b>
CPU2.DMEM - Correctable error CPU2.DLMU - Correctable error	OR	<b>ALM2[9]</b>
CPU2.DMEM - Uncorrectable Critical error CPU2.DLMU - Uncorrectable Critical error	OR	<b>ALM2[10]</b>
CPU2.DMEM - Miscellaneous error CPU2.DLMU - Miscellaneous error	OR	<b>ALM2[11]</b>
CPU3.DMEM - Correctable error CPU3.DLMU - Correctable error	OR	<b>ALM3[9]</b>
CPU3.DMEM - Uncorrectable Critical error CPU3.DLMU - Uncorrectable Critical error	OR	<b>ALM3[10]</b>
CPU3.DMEM - Miscellaneous error CPU3.DLMU - Miscellaneous error	OR	<b>ALM3[11]</b>
CPU4.DMEM - Correctable error CPU4.DLMU - Correctable error	OR	<b>ALM4[9]</b>
CPU4.DMEM - Unrecoverable error CPU4.DLMU - Uncorrectable Critical error	OR	<b>ALM4[10]</b>
CPU4.DMEM - Miscellaneous error CPU4.DLMU - Miscellaneous error	OR	<b>ALM4[11]</b>
CPU5.DMEM - Correctable error CPU5.DLMU - Correctable error	OR	<b>ALM5[9]</b>
CPU5.DMEM - Uncorrectable Critical error CPU5.DLMU - Uncorrectable Critical error	OR	<b>ALM5[10]</b>

**Safety Management Unit (SMU)****Table 252 MTU Pre-Alarm Mapping (cont'd)**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
CPU5.DMEM - Miscellaneous error CPU5.DLMU - Miscellaneous error	OR	<b>ALM5[11]</b>
LMU_RAM0 - Correctable error LMU_RAM1 - Correctable error LMU_RAM2 - Correctable error DAM0 - Correctable error DAM1 - Correctable error FSI_RAM - Correctable error	OR	<b>ALM7[0]</b>
LMU_RAM0 - Uncorrectable critical error LMU_RAM1 - Uncorrectable critical error LMU_RAM2 - Uncorrectable critical error DAM0 - Uncorrectable critical error DAM1 - Uncorrectable critical error FSI_RAM - Uncorrectable critical error	OR	<b>ALM7[1]</b>
LMU_RAM0 - Miscellaneous error LMU_RAM1 - Miscellaneous error LMU_RAM2 - Miscellaneous error DAM0 - Miscellaneous error DAM1 - Miscellaneous error FSI_RAM - Miscellaneous error	OR	<b>ALM7[2]</b>
DMA - Correctable error MCDS - Correctable error PSI5 - Correctable error SCR.XRAM - Correctable error SCR.RAMINT - Correctable error GIGETHERNET.RX0 - Correctable error GIGETHERNET.TX0 - Correctable error SDMMC - Correctable error	OR	<b>ALM6[19]</b>
DMA - Uncorrectable Critical error MCDS - Uncorrectable Critical error PSI5 - Uncorrectable Critical error SCR.XRAM - Uncorrectable critical error SCR.RAMINT - Uncorrectable Critical error GIGETHERNET.RX0 - Uncorrectable Critical error GIGETHERNET.TX0 - Uncorrectable Critical error SDMMC - Uncorrectable Critical error	OR	<b>ALM6[20]</b>
DMA - Miscellaneous error MCDS - Miscellaneous error PSI5 - Miscellaneous error SCR.XRAM - Miscellaneous error SCR.RAMINT - Miscellaneous error GIGETHERNET.RX0 - Miscellaneous error GIGETHERNET.TX0 - Miscellaneous error SDMMC - Miscellaneous error	OR	<b>ALM6[21]</b>

**Safety Management Unit (SMU)****Table 252 MTU Pre-Alarm Mapping (cont'd)**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
EMEM0 - Correctable error EMEM1 - Correctable error EMEM2 - Correctable error EMEM3 - Correctable error EMEM_XTM - Correctable error	OR	<b>ALM7[3]</b>
EMEM0 - Uncorrectable Critical error EMEM1 - Uncorrectable Critical error EMEM2 - Uncorrectable Critical error EMEM3 - Uncorrectable Critical error EMEM_XTM - Uncorrectable Critical error	OR	<b>ALM7[4]</b>
EMEM0 - Miscellaneous error EMEM1 - Miscellaneous error EMEM2 - Miscellaneous error EMEM3 - Miscellaneous error EMEM_XTM - Miscellaneous error	OR	<b>ALM7[5]</b>
SPU_BUFFER0 - Correctable error SPU_BUFFER1 - Correctable error SPU_CONFIG0 - Correctable error SPU_CONFIG1 - Correctable error HSDPM - Correctable error SPU_FFT_RAM0 - Correctable error SPU_FFT_RAM1 - Correctable error SPU_FFT_RAM2 - Correctable error SPU_FFT_RAM3 - Correctable error SPU_FFT_RAM4 - Correctable error SPU_FFT_RAM5 - Correctable error SPU_FFT_RAM6 - Correctable error SPU_FFT_RAM7 - Correctable error	OR	<b>ALM7[6]</b>
SPU_BUFFER0 - Uncorrectable Critical error SPU_BUFFER1 - Uncorrectable Critical error SPU_CONFIG0 - Uncorrectable Critical error SPU_CONFIG1 - Uncorrectable critical error HSDPM - Uncorrectable Critical error SPU_FFT_RAM0 - Uncorrectable Critical error SPU_FFT_RAM1 - Uncorrectable Critical error SPU_FFT_RAM2 - Uncorrectable Critical error SPU_FFT_RAM3 - Uncorrectable Critical error SPU_FFT_RAM4 - Uncorrectable Critical error SPU_FFT_RAM5 - Uncorrectable Critical error SPU_FFT_RAM6 - Uncorrectable Critical error SPU_FFT_RAM7 - Uncorrectable Critical error	OR	<b>ALM7[7]</b>

**Safety Management Unit (SMU)****Table 252 MTU Pre-Alarm Mapping (cont'd)**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
SPU_BUFFER0 - Miscellaneous error SPU_BUFFER1 - Miscellaneous error SPU_CONFIG0 - Miscellaneous error SPU_CONFIG1 - Miscellaneous error HSDPM - Miscellaneous error SPU_FFT_RAM0 - Miscellaneous error SPU_FFT_RAM1 - Miscellaneous error SPU_FFT_RAM2 - Miscellaneous error SPU_FFT_RAM3 - Miscellaneous error SPU_FFT_RAM4 - Miscellaneous error SPU_FFT_RAM5 - Miscellaneous error SPU_FFT_RAM6 - Miscellaneous error SPU_FFT_RAM7 - Miscellaneous error	OR	<b>ALM7[8]</b>
GTM.FIFO - Correctable error GTM.MCS0S - Correctable error GTM.MCS0F - Correctable error GTM.MCS1S - Correctable error GTM.MCS1F - Correctable error GTM.DPLL1A - Correctable error GTM.DPLL1BC - Correctable error GTM.DPLL2 - Correctable error	OR	<b>ALM6[10]</b>
GTM.FIFO - Uncorrectable Critical error GTM.MCS0S - Uncorrectable Critical error GTM.MCS0F - Uncorrectable Critical error GTM.MCS1S - Uncorrectable Critical error GTM.MCS1F - Uncorrectable Critical error GTM.DPLL1A - Uncorrectable Critical error GTM.DPLL1BC - Uncorrectable Critical error GTM.DPLL2 - Uncorrectable Critical error	OR	<b>ALM6[11]</b>
GTM.FIFO - Miscellaneous error GTM.MCS0S - Miscellaneous error GTM.MCS0F - Miscellaneous error GTM.MCS1S - Miscellaneous error GTM.MCS1F - Miscellaneous error GTM.DPLL1A - Miscellaneous error GTM.DPLL1BC - Miscellaneous error GTM.DPLL2 - Miscellaneous error	OR	<b>ALM6[12]</b>
CAN.MCAN0 - Correctable error CAN.MCAN1 - Correctable error CAN.MCAN2 - Correctable error	OR	<b>ALM6[16]</b>
CAN.MCAN0 - Uncorrectable critical error CAN.MCAN1 - Uncorrectable critical error CAN.MCAN2 - Uncorrectable critical error	OR	<b>ALM6[17]</b>
CAN.MCAN0 - Miscellaneous error CAN.MCAN1 - Miscellaneous error CAN.MCAN2 - Miscellaneous error	OR	<b>ALM6[18]</b>

**Safety Management Unit (SMU)****Table 252 MTU Pre-Alarm Mapping (cont'd)**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
ERAY.OBF0 - Correctable error ERAY.OBF1 - Correctable error ERAY.TBF_IBF0 - Correctable error ERAY.TBF_IBF1 - Correctable error ERAY.MBF0 - Correctable error ERAY.MBF1 - Correctable error	OR	<b>ALM6[13]</b>
ERAY.OBF0 - Uncorrectable Critical error ERAY.OBF1 - Uncorrectable Critical error ERAY.TBF_IBF0 - Uncorrectable Critical error ERAY.TBF_IBF1 - Uncorrectable Critical error ERAY.MBF0 - Uncorrectable Critical error ERAY.MBF1 - Uncorrectable Critical error	OR	<b>ALM6[14]</b>
ERAY.OBF0 - Miscellaneous error ERAY.OBF1 - Miscellaneous error ERAY.TBF_IBF0 - Miscellaneous error ERAY.TBF_IBF1 - Miscellaneous error ERAY.MBF0 - Miscellaneous error ERAY.MBF1 - Miscellaneous error	OR	<b>ALM6[15]</b>

**Safety Flip-flop Pre-Alarm Mapping****Table 253 Safety Flip-flop Pre-Alarm Mapping**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
MTU - Safety flip-flop uncorrectable error IOM - Safety flip-flop uncorrectable error EMEM - Safety flip-flop uncorrectable error IR - Safety flip-flop uncorrectable error SCU - Safety flip-flop uncorrectable error PMS - Safety flip-flop uncorrectable error DMA - Safety flip-flop uncorrectable error SYS_PLL.PER_PLL - Safety flip-flop uncorrectable error CERBERUS - Safety flip-flop uncorrectable error CCU - Safety flip-flop uncorrectable error SMU_core - Safety flip-flop uncorrectable error	OR	<b>ALM10[21]</b>

**Safety Management Unit (SMU)****LMU Pre-Alarm Mapping****Table 254 LMU Pre-Alarm Mapping**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
LMU.RAM0 - Lockstep Comparator error LMU.RAM1 - Lockstep Comparator error LMU.RAM2 - Lockstep Comparator error LMU.EMEM0 - Lockstep Comparator error LMU.EMEM1 - Lockstep Comparator error LMU.EMEM2 - Lockstep Comparator error LMU.EMEM3 - Lockstep Comparator error	OR	<b>ALM7[12]</b>
LMU.RAM0 - Lockstep Control error LMU.RAM1 - Lockstep Control error LMU.RAM2 - Lockstep Control error LMU.EMEM0 - Lockstep Control error LMU.EMEM1 - Lockstep Control error LMU.EMEM2 - Lockstep Control error LMU.EMEM3 - Lockstep Control error	OR	<b>ALM7[13]</b>
LMU.RAM0 - ECC error LMU.RAM1 - ECC error LMU.RAM2 - ECC error LMU.EMEM0 - ECC error LMU.EMEM1 - ECC error LMU.EMEM2 - ECC error LMU.EMEM3 - ECC error	OR	<b>ALM7[14]</b>
LMU.RAM0 - MPU violation LMU.RAM1 - MPU violation LMU.RAM2 - MPU violation LMU.DAM0 - MPU violation LMU.DAM1 - MPU violation LMU.EMEM0 - MPU violation LMU.EMEM1 - MPU violation LMU.EMEM2 - MPU violation LMU.EMEM3 - MPU violation	OR	<b>ALM7[15]</b>
LMU.RAM0 - EDC Read Phase Error LMU.RAM1 - EDC Read Phase Error LMU.RAM2 - EDC Read Phase Error LMU.EMEM0 - EDC Read Phase Error LMU.EMEM1 - EDC Read Phase Error LMU.EMEM2 - EDC Read Phase Error LMU.EMEM3 - EDC Read Phase Error	OR	<b>ALM7[16]</b>

**Safety Management Unit (SMU)****Table 254 LMU Pre-Alarm Mapping (cont'd)**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
LMU.RAM0 - SRI Slave Address Phase Error LMU.RAM1 - SRI Slave Address Phase Error LMU.RAM2 - SRI Slave Address Phase Error LMU.DAM0 - SRI Slave Address Phase Error LMU.DAM1 - SRI Slave Address Phase Error LMU.EMEM0 - SRI Slave Address Phase Error LMU.EMEM1 - SRI Slave Address Phase Error LMU.EMEM2 - SRI Slave Address Phase Error LMU.EMEM3 - SRI Slave Address Phase Error	OR	<b>ALM11[0]</b>
LMU.RAM0 - SRI Slave Write Data Phase Error LMU.RAM1 - SRI Slave Write Data Phase Error LMU.RAM2 - SRI Slave Write Data Phase Error LMU.DAM0 - SRI Slave Write Data Phase Error LMU.DAM1 - SRI Slave Write Data Phase Error LMU.EMEM0 - SRI Slave Write Data Phase Error LMU.EMEM1 - SRI Slave Write Data Phase Error LMU.EMEM2 - SRI Slave Write Data Phase Error LMU.EMEM3 - SRI Slave Write Data Phase Error	OR	<b>ALM11[1]</b>
LMU.DAM0 - EDC Read Phase Error LMU.DAM1 - EDC Read Phase Error	OR	<b>ALM11[8]</b>

**XBAR Pre-Alarm Mapping****Table 255 XBAR Pre-Alarm Mapping**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
XBAR.XBAR0 - Address Phase error XBAR.XBAR1 - Address Phase error XBAR.XBAR2 - Address Phase error	OR	<b>ALM11[2]</b>
XBAR.XBAR0 - Write Phase error XBAR.XBAR1 - Write Phase error XBAR.XBAR2 - Write Phase error	OR	<b>ALM11[3]</b>
XBAR.XBAR0 - Sota Swap error XBAR.XBAR1 - Sota Swap error XBAR.XBAR2 - Sota Swap error	OR	<b>ALM11[13]</b>

**Module Access Enable Pre-Alarm Mapping****Table 256 Module Access Enable Pre-Alarm Mapping**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
IR - Access Enable error	OR	<b>ALM10[22]</b>
HSM - Access Enable error		

**Safety Management Unit (SMU)****EMEM Pre-Alarm Mapping****Table 257 EMEM Pre-Alarm Mapping**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
EMEM.EMEM0 - Unexpected Write error EMEM.EMEM1 - Unexpected Write error EMEM.EMEM2 - Unexpected Write error EMEM.EMEM3 - Unexpected Write error	OR	<b>ALM9[20]</b>
EMEM.EMEM0 - SEP Control error EMEM.EMEM1 - SEP Control error EMEM.EMEM2 - SEP Control error EMEM.EMEM3 - SEP Control error	OR	<b>ALM9[21]</b>
EMEM.EMEM0 - Lockstep Control Logic inputs error EMEM.EMEM1 - Lockstep Control Logic inputs error EMEM.EMEM2 - Lockstep Control Logic inputs error EMEM.EMEM3 - Lockstep Control Logic inputs error	OR	<b>ALM9[22]</b>

**PMS Pre-Alarm Mapping****Table 258 PMS Pre-Alarm Mapping**

<b>Alarm Source</b>	<b>Logic</b>	<b>Alarm Index</b>
PMS - Uncorrectable error SMU.SMU_stby - Safety flip-flop Uncorrectable error	OR	<b>ALM21[7]</b>
HSM.VDD - Under Voltage HSM.VDDP3 - Under Voltage HSM.VEXT - Under Voltage	OR	<b>ALM9[17]</b>
HSM.VDD - Over Voltage HSM.VDDP3 - Over Voltage HSM.VEXT - Over Voltage	OR	<b>ALM9[16]</b>
PMS.VDD - Over voltage PMS.VDDPD - Over voltage PMS.VDDP3 - Over voltage PMS.VDDM - Over voltage PMS.VEXT - Over voltage PMS.VEVRSB - Over voltage	OR	<b>ALM9[3]</b>
PMS.VDD - Under voltage PMS.VDDPD - Under voltage PMS.VDDP3 - Under voltage PMS.VDDM - Under voltage PMS.VEXT - Under voltage PMS.VEVRSB - Under voltage	OR	<b>ALM9[5]</b>
PMS.EVRC - Short to Low PMS.EVRC - Short to High PMS.EVR33 - Short to Low PMS.EVR33 - Short to High	OR	<b>ALM9[15]</b>

## Safety Management Unit (SMU)

### 15.4.2 TC39x-B Specific Alarms

The following tables fully specify the mapping between the alarms provided by the safety mechanisms implemented by the microcontroller and the alarm groups.

In the following tables the column “Safety Mechanism & Error Indication” indicates to which safety mechanism the alarm is related. If multiple safety mechanisms are indicated, the alarm corresponds to the detection of an error by one of the listed safety mechanisms.

For some safety mechanisms different terms are used in the microcontroller documents; the following list provides a guideline between the term used in the alarm tables and the other definitions, in bold the definition used in the alarm tables.

- Register Access Protection or alternatively called Safety Register Protection
  - Purpose: Monitors the master identifier of a given bus-master during a write access to a configuration register. The master identifier is a hard-coded information that is provided during any bus access. If the master identifier is not enabled by the Register Access Protection configuration registers (ACCEN0) the write is aborted. Most of the modules do not provide a dedicated alarm for this event and instead will generate a bus error. Therefore the Register Access Protection is only documented where a dedicated alarm is available.
  - Note: for peripherals that implement memory-mapped SRAMs, the write accesses to the memories are monitored as well.
- Bus-level Memory Protection Unit (MPU) or alternatively called Safety Memory Protection
  - Purpose: Monitors the master identifier and the address of a given bus-master during a write access to a local SRAM. The master identifier is a hard-coded information that is provided during any bus access. If the master identifier is enabled by the Bus-level MPU configuration registers and the address is within the valid address range the write is accepted, otherwise the write is aborted and a Bus-level MPU alarm is issued.
  - The SRAMs monitored are the {PSPR, DSPR, DLMU} SRAMs of each CPU and the LMU SRAMs when available in the product.

#### Alarm Mapping related to ALM0 group

**Table 259 Alarm Mapping related to ALM0 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM0[0]	cpu_pfi_pfrwb_0	Safety Mechanism: Lockstep CPU Alarm: CPU0 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM0[1]	cpu_pfi_pfrwb_0	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU0 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse
ALM0[2]	cpu_pfi_pfrwb_0	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU0 PFLASH0 Read Path Error Alarm Type: Pulse

## Safety Management Unit (SMU)

**Table 259 Alarm Mapping related to ALM0 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM0[3]	Reserved	Reserved
ALM0[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM0[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM0[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM0[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM0[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM0[9]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM0[10]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM0[11]	<a href="#">Page 19</a>	Safety Mechanism(s): SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM0[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Single bit error correction Alarm Type: Level
ALM0[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM0[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM0[21:15]	Reserved	Reserved
ALM0[22]	cpu_pfi_pfrwb_0	Safety Mechanism: SRI End-to-End EDC Alarm: CPU0 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM0[23]	cpu_pfi_pfrwb_0	Safety Mechanism: SRI End-to-End EDC Alarm: CPU0 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse

## Safety Management Unit (SMU)

**Table 259 Alarm Mapping related to ALM0 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM0[24]	cpu_pfi_pfrwb_0	Safety Mechanism: Exception Monitor Alarm: CPU0 exception (interrupt/trap) Alarm Type: Pulse
ALM0[31:25]	Reserved	Reserved

### Alarm Mapping related to ALM1 group

**Table 260 Alarm Mapping related to ALM1 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[0]	cpu_pfi_pfrwb_1	Safety Mechanism: Lockstep CPU Alarm: CPU1 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. Moreover If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting LCL1 bitfield in SCU_LCLTEST Register. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM1[1]	cpu_pfi_pfrwb_1	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU1 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse
ALM1[2]	cpu_pfi_pfrwb_1	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU1 PFLASH1 Read Path Error Alarm Type: Pulse Note: If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting PLCLT1 bitfield in SCU_LCLTEST Register.
ALM1[3]	Reserved	Reserved
ALM1[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM1[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM1[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM1[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level

## Safety Management Unit (SMU)

**Table 260 Alarm Mapping related to ALM1 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM1[9]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM1[10]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM1[11]	<a href="#">Page 19</a>	Safety Mechanism(s): SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM1[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Single bit error correction Alarm Type: Level
ALM1[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM1[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM1[21:15]	Reserved	Reserved
ALM1[22]	cpu_pfi_pfrwb_1	Safety Mechanism: SRI End-to-End EDC Alarm: CPU1 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM1[23]	cpu_pfi_pfrwb_1	Safety Mechanism: SRI End-to-End EDC Alarm: CPU1 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM1[24]	cpu_pfi_pfrwb_1	Safety Mechanism: Exception Monitor Alarm: CPU1 exception (interrupt/trap) Alarm Type: Pulse
ALM1[31:25]	Reserved	Reserved

## Safety Management Unit (SMU)

### Alarm Mapping related to ALM2 group

**Table 261 Alarm Mapping related to ALM2 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM2[0]	cpu_pfi_pfrwb_2	<p>Safety Mechanism: Lockstep CPU            Alarm: CPU2 Lockstep Comparator Error            Alarm Type: Pulse</p> <p>Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. Moreover If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting LCL2 bitfield in SCU_LCLTEST Register. For more details about the CPU lockstep alarm, please refer to the CPU chapter.</p>
ALM2[1]	cpu_pfi_pfrwb_2	<p>Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection            Alarm: CPU2 Bus-level MPU violation / Access Protection violation            Alarm Type: Pulse</p>
ALM2[2]	cpu_pfi_pfrwb_2	<p>Safety Mechanism: PFLASH Read Path Monitor            Alarm: CPU2 PFLASH2 Read Path Error            Alarm Type: Pulse</p> <p>Note: If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting PLCLT2 bitfield in SCU_LCLTEST Register.</p>
ALM2[3]	Reserved	Reserved
ALM2[4]	MTU	<p>Safety Mechanism: SRAM Monitor            Alarm: CPU2 PCACHE TAG Uncorrectable critical error detection            Alarm Type: Level</p>
ALM2[5]	MTU	<p>Safety Mechanism: SRAM Monitor            Alarm: CPU2 PCACHE TAG Miscellaneous error detection            Alarm Type: Level</p>
ALM2[6]	MTU	<p>Safety Mechanism: SRAM Monitor            Alarm: CPU2 PSPR/PCACHE Single bit error correction            Alarm Type: Level</p>
ALM2[7]	MTU	<p>Safety Mechanism: SRAM Monitor            Alarm: CPU2 PSPR/PCACHE Uncorrectable critical error detection            Alarm Type: Level</p>
ALM2[8]	MTU	<p>Safety Mechanism: SRAM Monitor            Alarm: CPU2 PSPR/PCACHE Miscellaneous critical error detection            Alarm Type: Level</p>
ALM2[9]	<a href="#">Page 19</a>	<p>Safety Mechanism: SRAM Monitor            Alarm: CPU2 DSPR/DCACHE/DLMU Single bit error correction            Alarm Type: Level</p>
ALM2[10]	<a href="#">Page 19</a>	<p>Safety Mechanism: SRAM Monitor            Alarm: CPU2 DSPR/DCACHE/DLMU Uncorrectable critical error detection            Alarm Type: Level</p>

## Safety Management Unit (SMU)

**Table 261 Alarm Mapping related to ALM2 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM2[11]	<a href="#">Page 19</a>	Safety Mechanism(s): SRAM Monitor Alarm: CPU2 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM2[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU2 DCACHE TAG Single bit error correction Alarm Type: Level
ALM2[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU2 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM2[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU2 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM2[21:15]	Reserved	Reserved
ALM2[22]	cpu_pfi_pfrwb_2	Safety Mechanism: SRI End-to-End EDC Alarm: CPU2 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM2[23]	cpu_pfi_pfrwb_2	Safety Mechanism: SRI End-to-End EDC Alarm: CPU2 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM2[24]	cpu_pfi_pfrwb_2	Safety Mechanism: Exception Monitor Alarm: CPU2 exception (interrupt/trap) Alarm Type: Pulse
ALM2[31:25]	Reserved	Reserved

## Alarm Mapping related to ALM3 group

**Table 262 Alarm Mapping related to ALM3 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM3[0]	cpu_pfi_pfrwb_3	Safety Mechanism: Lockstep CPU Alarm: CPU3 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. Moreover If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting LCL3 bitfield in SCU_LCLTEST Register. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM3[1]	cpu_pfi_pfrwb_3	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU3 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse

**Safety Management Unit (SMU)****Table 262 Alarm Mapping related to ALM3 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM3[2]	cpu_pfi_pfrwb_3	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU3 PFLASH3 Read Path Error Alarm Type: Pulse Note: If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting PLCLT3 bitfield in SCU_LCLTEST Register.
ALM3[3]	Reserved	Reserved
ALM3[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM3[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM3[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM3[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM3[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM3[9]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU3 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM3[10]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU3 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM3[11]	<a href="#">Page 19</a>	Safety Mechanism(s): SRAM Monitor Alarm: CPU3 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM3[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 DCACHE TAG Single bit error correction Alarm Type: Level
ALM3[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM3[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU3 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM3[21:15]	Reserved	Reserved

## Safety Management Unit (SMU)

**Table 262 Alarm Mapping related to ALM3 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM3[22]	cpu_pfi_pfrwb_3	Safety Mechanism: SRI End-to-End EDC Alarm: CPU3 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM3[23]	cpu_pfi_pfrwb_3	Safety Mechanism: SRI End-to-End EDC Alarm: CPU3 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM3[24]	cpu_pfi_pfrwb_3	Safety Mechanism: Exception Monitor Alarm: CPU3 exception (interrupt/trap) Alarm Type: Pulse
ALM3[31:25]	Reserved	Reserved

## Alarm Mapping related to ALM4 group

**Table 263 Alarm Mapping related to ALM4 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM4[0]	cpu_pfi_pfrwb_4	Safety Mechanism: Lockstep CPU Alarm: CPU4 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. Moreover If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting LCL4 bitfield in SCU_LCLTEST Register. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM4[1]	cpu_pfi_pfrwb_4	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU4 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse
ALM4[2]	cpu_pfi_pfrwb_4	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU4 PFLASH4 Read Path Error Alarm Type: Pulse Note: If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting PLCLT4 bitfield in SCU_LCLTEST Register.
ALM4[3]	Reserved	Reserved
ALM4[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM4[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 PCACHE TAG Miscellaneous error detection Alarm Type: Level

**Safety Management Unit (SMU)****Table 263 Alarm Mapping related to ALM4 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM4[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM4[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM4[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM4[9]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU4 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM4[10]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU4 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM4[11]	<a href="#">Page 19</a>	Safety Mechanism(s): SRAM Monitor Alarm: CPU4 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM4[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 DCACHE TAG Single bit error correction Alarm Type: Level
ALM4[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM4[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU4 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM4[21:15]	Reserved	Reserved
ALM4[22]	cpu_pfi_pfrwb_4	Safety Mechanism: SRI End-to-End EDC Alarm: CPU4 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM4[23]	cpu_pfi_pfrwb_4	Safety Mechanism: SRI End-to-End EDC Alarm: CPU4 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM4[24]	cpu_pfi_pfrwb_4	Safety Mechanism: Exception Monitor Alarm: CPU4 exception (interrupt/trap) Alarm Type: Pulse
ALM4[31:25]	Reserved	Reserved

## Safety Management Unit (SMU)

### Alarm Mapping related to ALM5 group

**Table 264 Alarm Mapping related to ALM5 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM5[0]	cpu_pfi_pfrwb_5	Safety Mechanism: Lockstep CPU Alarm: CPU5 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. Moreover If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting LCL5 bitfield in SCU_LCLTEST Register. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM5[1]	cpu_pfi_pfrwb_5	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU5 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse
ALM5[2]	cpu_pfi_pfrwb_5	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU5 PFLASH5 Read Path Error Alarm Type: Pulse Note: If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting PLCLT5 bitfield in SCU_LCLTEST Register.
ALM5[3]	Reserved	Reserved
ALM5[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM5[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM5[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM5[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM5[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM5[9]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU5 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM5[10]	<a href="#">Page 19</a>	Safety Mechanism: SRAM Monitor Alarm: CPU5 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level

## Safety Management Unit (SMU)

**Table 264 Alarm Mapping related to ALM5 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM5[11]	<a href="#">Page 20</a>	Safety Mechanism(s): SRAM Monitor Alarm: CPU5 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM5[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 DCACHE TAG Single bit error correction Alarm Type: Level
ALM5[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM5[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU5 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM5[21:15]	Reserved	Reserved
ALM5[22]	cpu_pfi_pfrwb_5	Safety Mechanism: SRI End-to-End EDC Alarm: CPU5 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM5[23]	cpu_pfi_pfrwb_5	Safety Mechanism: SRI End-to-End EDC Alarm: CPU5 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM5[24]	cpu_pfi_pfrwb_5	Safety Mechanism: Exception Monitor Alarm: CPU5 exception (interrupt/trap) Alarm Type: Pulse
ALM5[31:25]	Reserved	Reserved

## Alarm Mapping related to ALM6 group

**Table 265 Alarm Mapping related to ALM6 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM6[0]	MTU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[1]	IOM	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[2]	INT	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[3]	EMEMWRAPPER	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[4]	SCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level

## Safety Management Unit (SMU)

**Table 265 Alarm Mapping related to ALM6 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM6[5]	PMS	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[6]	DMA	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[7]	SMU_CORE	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[8]	CCU	Safety Mechanism: Safety Flip-flop Alarm: SYS_PLL.PER_PLL - Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[9]	Reserved	Reserved
ALM6[10]	<a href="#">Page 22</a>	Safety Mechanism: SRAM Monitor Alarm: GTM Single bit error correction Alarm Type: Level
ALM6[11]	<a href="#">Page 22</a>	Safety Mechanism: SRAM Monitor Alarm: GTM Uncorrectable critical error detection Alarm Type: Level
ALM6[12]	<a href="#">Page 22</a>	Safety Mechanism: SRAM Monitor Alarm: GTM Miscellaneous error detection Alarm Type: Level
ALM6[13]	<a href="#">Page 23</a>	Safety Mechanism: SRAM Monitor Alarm: ERAY Single bit error correction Alarm Type: Level
ALM6[14]	<a href="#">Page 23</a>	Safety Mechanism: SRAM Monitor Alarm: ERAY Uncorrectable critical error detection Alarm Type: Level
ALM6[15]	<a href="#">Page 23</a>	Safety Mechanism: SRAM Monitor Alarm: ERAY Miscellaneous error detection Alarm Type: Level
ALM6[16]	<a href="#">Page 22</a>	Safety Mechanism: SRAM Monitor Alarm: CAN Single bit error correction Alarm Type: Level
ALM6[17]	<a href="#">Page 22</a>	Safety Mechanism: SRAM Monitor Alarm: CAN Uncorrectable critical error detection Alarm Type: Level
ALM6[18]	<a href="#">Page 22</a>	Safety Mechanism: SRAM Monitor Alarm: CAN Miscellaneous error detection Alarm Type: Level
ALM6[19]	<a href="#">Page 20</a>	Safety Mechanism: SRAM Monitor Alarm: MISC Single bit error correction Alarm Type: Level

**Safety Management Unit (SMU)****Table 265 Alarm Mapping related to ALM6 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM6[20]	<a href="#">Page 20</a>	Safety Mechanism: SRAM Monitor Alarm: MISC Uncorrectable critical error detection Alarm Type: Level
ALM6[21]	<a href="#">Page 20</a>	Safety Mechanism: SRAM Monitor Alarm: MISC Miscellaneous error detection Alarm Type: Level
ALM6[22]	Reserved	Reserved
ALM6[23]	CBS	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[24]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop correctable error detected Alarm Type: Level
ALM6[25]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[31:26]	Reserved	Reserved

**Alarm Mapping related to ALM7 group****Table 266 Alarm Mapping related to ALM7 group**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM7[0]	<a href="#">Page 20</a>	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Single bit error correction Alarm Type: Level
ALM7[1]	<a href="#">Page 20</a>	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Uncorrectable critical error detection Alarm Type: Level
ALM7[2]	<a href="#">Page 20</a>	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Miscellaneous error detection Alarm Type: Level
ALM7[3]	<a href="#">Page 21</a>	Safety Mechanism: SRAM Monitor Alarm: EMEM Single bit error correction Alarm Type: Level
ALM7[4]	<a href="#">Page 21</a>	Safety Mechanism: SRAM Monitor Alarm: EMEM Uncorrectable critical error detection Alarm Type: Level
ALM7[5]	<a href="#">Page 21</a>	Safety Mechanism: SRAM Monitor Alarm: EMEM Miscellaneous error detection Alarm Type: Level
ALM7[6]	<a href="#">Page 21</a>	Safety Mechanism: SRAM Monitor Alarm: SPU/CIF Single bit error correction Alarm Type: Level

**Safety Management Unit (SMU)****Table 266 Alarm Mapping related to ALM7 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM7[7]	<a href="#">Page 21</a>	Safety Mechanism: SRAM Monitor Alarm: SPU/CIF Uncorrectable critical error detection Alarm Type: Level
ALM7[8]	<a href="#">Page 22</a>	Safety Mechanism: SRAM Monitor Alarm: SPU/CIF Miscellaneous error detection Alarm Type: Level
ALM7[11:9]	Reserved	Reserved
ALM7[12]	<a href="#">Page 24</a>	Safety Mechanism: LMU Lockstep Alarm: Lockstep Comparator Error Alarm Type: Pulse
ALM7[13]	<a href="#">Page 24</a>	Safety Mechanism: LMU Lockstep Alarm: Lockstep Control Error Alarm Type: Pulse
ALM7[14]	<a href="#">Page 24</a>	Safety Mechanism: SRAM ECC Monitor Alarm: ECC Error Alarm Type: Pulse
ALM7[15]	<a href="#">Page 24</a>	Safety Mechanism: Bus-level MPU Alarm: Bus-level MPU error Alarm Type: Pulse
ALM7[16]	<a href="#">Page 24</a>	Safety Mechanism: LMU Error Detection Code (EDC) Alarm: EDC Read Phase Error Alarm Type: Pulse
ALM7[17]	SRI	Safety Mechanism: Built-in SRI Error Detection Alarm: XBAR0 Bus Error Event Alarm Type: Pulse
ALM7[18]	SRI	Safety Mechanism: Built-in SRI Error Detection Alarm: XBAR1 Bus Error Event Alarm Type: Pulse
ALM7[19]	SRI	Safety Mechanism: Built-in SRI Error Detection Alarm: XBAR2 Bus Error Event Alarm Type: Pulse
ALM7[20]	SBCU	Safety Mechanism: Built-in SPB Error Detection Alarm: SPB Bus Error Event Alarm Type: Pulse
ALM7[21]	EBCU	Safety Mechanism: Built-in BBB Error Detection Alarm: BBB Bus Error Event Alarm Type: Pulse
ALM7[22]	FSI	Safety Mechanism: PFlash ECC Alarm: PFlash Single Bit Error Alarm Type: Level
ALM7[23]	FSI	Safety Mechanism: PFlash ECC Alarm: PFlash Double Bit Error Alarm Type: Level

**Safety Management Unit (SMU)****Table 266 Alarm Mapping related to ALM7 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM7[24]	FSI	Safety Mechanism: PFlash ECC Alarm: Single Bit Correction Tracking Buffer Full Alarm Type: Level
ALM7[25]	FSI	Safety Mechanism: PFlash ECC Alarm: Double Bit Correction Tracking Buffer Full Alarm Type: Level
ALM7[26]	FSI	Safety Mechanism: PFlash ECC Alarm: Multiple Bit Error Detection Tracking Buffer Full Alarm Type: Level
ALM7[27]	FSI	Safety Mechanism: PFlash ECC Alarm: Zero Bit Error Tracking Buffer Full Alarm Type: Level
ALM7[28]	FSI	Safety Mechanism: PFlash ECC Monitor Alarm: PFlash ECC Error Alarm Type: Level
ALM7[29]	FSI	Safety Mechanism: PFlash EDC Monitor Alarm: PFlash EDC Error Alarm Type: Level
ALM7[30]	FSI	Safety Mechanism: PFlash Configuration Monitor Alarm: CPU FLASHCON Configuration Error Alarm Type: Level
ALM7[31]	FSI	Safety Mechanism: PFlash Configuration Monitor Alarm: Flash Stored Configuration Error Alarm Type: Level

**Alarm Mapping related to ALM8 group****Table 267 Alarm Mapping related to ALM8 group**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM8[0]	SCU	Safety Mechanism: Clock Monitor Alarm: OSC clock frequency out of range Alarm Type: Pulse
ALM8[1]	CCU	Safety Mechanism: Clock Monitor Alarm: Back-up clock out-of-range alarm Alarm Type: Level
ALM8[2]	CCU	Safety Mechanism: Clock Alive Monitor Alarm: Back-up clock alive alarm Alarm Type: Level
ALM8[3]	SCU	Safety Mechanism: PLL loss of lock detection Alarm: System PLL DCO loss of lock event Alarm Type: Pulse
ALM8[4]	SCU	Safety Mechanism: PLL loss of lock detection Alarm: Peripheral PLL DCO loss of lock event Alarm Type: Pulse

**Safety Management Unit (SMU)****Table 267 Alarm Mapping related to ALM8 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM8[5]	SCU	Safety Mechanism: LBIST Safe Reset State Alarm: LBIST Alarm Alarm Type: Level
ALM8[6]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 0 Alarm Type: Pulse
ALM8[7]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 1 Alarm Type: Pulse
ALM8[8]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 2 Alarm Type: Pulse
ALM8[9]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 3 Alarm Type: Pulse
ALM8[10]	SCU	Safety Mechanism: Watchdog Alarm: CPU0 Watchdog Time-out Alarm Type: Pulse
ALM8[11]	SCU	Safety Mechanism: Watchdog Alarm: CPU1 Watchdog Time-out Alarm Type: Pulse
ALM8[12]	SCU	Safety Mechanism: Watchdog Alarm: CPU2 Watchdog Time-out Alarm Type: Pulse
ALM8[13]	SCU	Safety Mechanism: Watchdog Alarm: CPU3 Watchdog Time-out Alarm Type: Pulse
ALM8[14]	SCU	Safety Mechanism: Watchdog Alarm: CPU4 Watchdog Time-out Alarm Type: Pulse
ALM8[15]	SCU	Safety Mechanism: Watchdog Alarm: CPU5 Watchdog Time-out Alarm Type: Pulse
ALM8[16]	SCU	Safety Mechanism: Watchdog Alarm: Safety Watchdog Time-out Alarm Type: Pulse
ALM8[17]	SCU	Safety Mechanism: All Watchdogs Alarm: Watchdog Time-out. This alarm is a logical OR over all watchdog time-out alarms Alarm Type: Pulse
ALM8[18]	SCU	Safety Mechanism: Lockstep Dual Rail Monitor Alarm: Dual Rail Error Alarm Type: Pulse

**Safety Management Unit (SMU)****Table 267 Alarm Mapping related to ALM8 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM8[19]	SCU	Safety Mechanism: Emergency Stop Alarm: External Emergency Stop Signal Event Alarm Type: Pulse
ALM8[20]	SCU	Safety Mechanism: Pad Monitor Alarm: Pad Heating Alarm Alarm Type: Pulse Note: This alarm is triggered by the pad-heating enable signal of all core supply-pads. It will also be triggered by the enable signal for initialisation of security sensitive RAMs and TCU test enable signals
ALM8[21]	SCU	Safety Mechanism: LBIST Test Mode Alarm: LBIST Test Mode Alarm Alarm Type: Level Note: This alarm is also set if TCU related signals are activated in the SCU causing it to fail
ALM8[22]	INT	Safety Mechanism: Interrupt Monitor Alarm: EDC Configuration and Data Path Error Alarm Type: Pulse
ALM8[23]	DMA	Safety Mechanism: DMA SRI ECC Alarm: DMA SRI ECC Error Alarm Type: Pulse
ALM8[24]	Reserved	Reserved
ALM8[25]	IOM	Safety Mechanism: External Alarm Alarm: Pin Mismatch Indication Alarm Type: Level
ALM8[26]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 4 Alarm Type: Pulse
ALM8[27]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 5 Alarm Type: Pulse
ALM8[28]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 6 Alarm Type: Pulse
ALM8[29]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 7 Alarm Type: Pulse
ALM8[30]	SCU	Safety Mechanism: Core Domain Die Temperature Sensor Alarm: Under Temperature Alarm Alarm Type: Level
ALM8[31]	SCU	Safety Mechanism: Core Domain Die Temperature Sensor Alarm: Over Temperature Alarm Alarm Type: Level

**Safety Management Unit (SMU)****Alarm Mapping related to ALM9 group****Table 268 Alarm Mapping related to ALM9 group**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM9[0]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature Overflow Alarm Type: Level
ALM9[1]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature Underflow Alarm Type: Level
ALM9[2]	Reserved	Reserved
ALM9[3]	<a href="#">Page 26</a>	Safety Mechanism: Voltage Monitor Alarm: Over-voltage Alarm Alarm Type: Level
ALM9[4]	Reserved	Reserved
ALM9[5]	<a href="#">Page 26</a>	Safety Mechanism: Voltage Monitor Alarm: Under-voltage Alarm Alarm Type: Level
ALM9[14:6]	Reserved	Reserved
ALM9[15]	<a href="#">Page 26</a>	Safety Mechanism: Voltage Monitor Alarm: Short to Low/High Alarm Alarm Type: Level
ALM9[16]	<a href="#">Page 26</a>	Safety Mechanism: Voltage Monitor Alarm: Over-voltage Alarm Alarm Type: Level
ALM9[17]	<a href="#">Page 26</a>	Safety Mechanism: Voltage Monitor Alarm: Under-voltage Alarm Alarm Type: Level
ALM9[19:18]	Reserved	Reserved
ALM9[20]	<a href="#">Page 26</a>	Safety Mechanism: EMEM Monitor Alarm: Unexpected Write to EMEM Alarm Alarm Type: Pulse
ALM9[21]	<a href="#">Page 26</a>	Safety Mechanism: SEP Control Logic Monitor Alarm: SEP Control Logic Alarm Alarm Type: Pulse
ALM9[22]	<a href="#">Page 26</a>	Safety Mechanism: SPU Lockstep Control Logic Input Monitor Alarm: SPU Configuration Error Alarm Alarm Type: Pulse
ALM9[23]	SPULCKSTP	Safety Mechanism: Lockstep Alarm: Lockstep Comparator Alarm Alarm Type: Pulse
ALM9[26:24]	Reserved	Reserved
ALM9[27]	Reserved	Reserved

## Safety Management Unit (SMU)

**Table 268 Alarm Mapping related to ALM9 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM9[28]	SPU0	Safety Mechanism: SPU Safety Monitor Alarm: SPU0 Safety Alarm Alarm Type: Pulse
ALM9[29]	SPU1	Safety Mechanism: SPU Safety Monitor Alarm: SPU1 Safety Alarm Alarm Type: Pulse
ALM9[30]	RIF0	Safety Mechanism: RIF Safety Monitor Alarm: RIF0 Safety Alarm Alarm Type: Pulse
ALM9[31]	RIF1	Safety Mechanism: RIF Safety Monitor Alarm: RIF1 Safety Alarm Alarm Type: Pulse

## Alarm Mapping related to ALM10 group

**Table 269 Alarm Mapping related to ALM10 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM10[0]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 0 Alarm Type: Pulse
ALM10[1]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 1 Alarm Type: Pulse
ALM10[2]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 2 Alarm Type: Pulse
ALM10[3]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 3 Alarm Type: Pulse
ALM10[4]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 4 Alarm Type: Pulse
ALM10[5]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 5 Alarm Type: Pulse
ALM10[6]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 6 Alarm Type: Pulse
ALM10[7]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 7 Alarm Type: Pulse
ALM10[8]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 8 Alarm Type: Pulse

**Safety Management Unit (SMU)****Table 269 Alarm Mapping related to ALM10 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM10[9]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 9 Alarm Type: Pulse
ALM10[10]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 10 Alarm Type: Pulse
ALM10[11]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 11 Alarm Type: Pulse
ALM10[12]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 12 Alarm Type: Pulse
ALM10[13]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 13 Alarm Type: Pulse
ALM10[14]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 14 Alarm Type: Pulse
ALM10[15]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 15 Alarm Type: Pulse
ALM10[16]	SMU_CORE	Safety Mechanism: Recovery Timer 0 Alarm: Timer Time-out Alarm Type: Pulse
ALM10[17]	SMU_CORE	Safety Mechanism: Recovery Timer 1 Alarm: Timer Time-out Alarm Type: Pulse
ALM10[18]	FSP	Safety Mechanism: ErrorPin Alarm: ErrorPin Fault State Activation Alarm Type: Pulse
ALM10[19]	Reserved	Reserved
ALM10[20]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop correctable error detected Alarm Type: Level
ALM10[21]	<a href="#">Page 23</a>	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM10[22]	<a href="#">Page 25</a>	Safety Mechanism: Access Enable Protection Alarm: Access Enable error Alarm Type: Pulse
ALM10[31:23]	Reserved	Reserved

**Safety Management Unit (SMU)****Alarm Mapping related to ALM11 group****Table 270 Alarm Mapping related to ALM11 group**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM11[0]	<a href="#">Page 25</a>	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[1]	<a href="#">Page 25</a>	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[2]	<a href="#">Page 25</a>	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[3]	<a href="#">Page 25</a>	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[4]	DMU	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[5]	DMU	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[6]	SFIBRIDGE2	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[7]	SFIBRIDGE2	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[8]	<a href="#">Page 25</a>	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: LMU.DAM - EDC Read Phase Error Alarm Type: Pulse
ALM11[9]	SFIBRIDGE1	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Read Phase Error Alarm Type: Pulse
ALM11[10]	HSSL0	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: HSSL0 EDC Read Phase Error Alarm Type: Pulse
ALM11[11]	HSSL1	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: HSSL1 EDC Read Phase Error Alarm Type: Pulse
ALM11[12]	converter_0	Safety Mechanism: Converter Alarm: Phase Synchronizer Error Alarm Type: Level

**Safety Management Unit (SMU)****Table 270 Alarm Mapping related to ALM11 group (cont'd)**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM11[13]	<a href="#">Page 25</a>	Safety Mechanism: SRI SOTA Monitor Alarm: SOTA Swap Error Alarm Type: Pulse
ALM11[31:14]	Reserved	Reserved

**Alarm Mapping related to ALM20 group****Table 271 Alarm Mapping related to ALM20 group**

<b>Alarm Index</b>	<b>Module</b>	<b>Safety Mechanism &amp; Alarm Indication</b>
ALM20[3:0]	Reserved	Resreveed
ALM20[4]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDD Over-voltage Alarm Alarm Type: Level
ALM20[5]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDPD Over-voltage Alarm Alarm Type: Level
ALM20[6]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Over-voltage Alarm Alarm Type: Level
ALM20[7]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDM Over-voltage Alarm Alarm Type: Level
ALM20[8]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEXT Over-voltage Alarm Alarm Type: Level
ALM20[9]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEVRSB Over-voltage Alarm Alarm Type: Level
ALM20[10]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDD Under-voltage Alarm Alarm Type: Level
ALM20[11]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDPD Under-voltage Alarm Alarm Type: Level
ALM20[12]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Under-voltage Alarm Alarm Type: Level
ALM20[13]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDM Under-voltage Alarm Alarm Type: Level
ALM20[14]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEXT Under-voltage Alarm Alarm Type: Level

## Safety Management Unit (SMU)

**Table 271 Alarm Mapping related to ALM20 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM20[15]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEVRSB Under-voltage Alarm Alarm Type: Level
ALM20[31:16]	Reserved	Reserved

### Alarm Mapping related to ALM21 group

**Table 272 Alarm Mapping related to ALM21 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM21[0]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDD Under-voltage Alarm Alarm Type: Level
ALM21[1]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Under-voltage Alarm Alarm Type: Level
ALM21[2]	hsm	Safety Mechanism: Voltage Monitor Alarm: VEXT Under-voltage Alarm Alarm Type: Level
ALM21[3]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDD Over-voltage Alarm Alarm Type: Level
ALM21[4]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDDP3 over-voltage Alarm Alarm Type: Level
ALM21[5]	hsm	Safety Mechanism: Voltage Monitor Alarm: VEXT over-voltage Alarm Alarm Type: Level
ALM21[6]	Reserved	Reserved
ALM21[7]	<a href="#">Page 26</a>	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM21[8]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature underflow Alarm Type: Level
ALM21[9]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature overflow Alarm Type: Level
ALM21[10]	PMS	Safety Mechanism: Register Access Protection Alarm: Access Protection violation Alarm Type: Pulse
ALM21[11]	PMS	Safety Mechanism: Voltage Monitor Alarm: EVRC Short to Low Alarm Alarm Type: Level

## Safety Management Unit (SMU)

**Table 272 Alarm Mapping related to ALM21 group (cont'd)**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM21[12]	PMS	Safety Mechanism: Voltage Monitor Alarm: EVRC Short to High Alarm Alarm Type: Level
ALM21[13]	PMS	Safety Mechanism: Voltage Monitor Alarm: EV33 Short to Low Alarm Alarm Type: Level
ALM21[14]	PMS	Safety Mechanism: Voltage Monitor Alarm: EV33 Short to High Alarm Alarm Type: Level
ALM21[15]	CCU	Safety Mechanism: Clock Alive Monitor Alarm: PLLx/fSPB Alive Alarm (provided on fBACK clock with x = 0..2) Alarm Type: Level Note: This alarm is also set if TCU related signals are activated in the CCU causing the clocks to fail
ALM21[16]	SMU_CORE	Safety Mechanism: SMU_core Alive Monitor Alarm: SMU_core Alive Alarm Alarm Type: Pulse
ALM21[31:17]	Reserved	Reserved

## 15.5 Connectivity

**Table 273 Connections of SMU**

Interface Signals	connects		Description
SMU:FSP(0)	to	P33.8:HWOUT(0)	FSP[1..0] Output Signals - Generated by SMU_core
SMU:FSP(1)	to	P33.10:HWOUT(0)	FSP[1..0] Output Signals - Generated by SMU_core
SMU:FSP_STS(0)	from	P33.8:IN	FSP Status Input - Shows the actual state of the FSP ErroPin
SMU:FSP_STS(1)	from	P33.10:IN	FSP Status Input - Shows the actual state of the FSP ErroPin
SMU:RUNSTATE	to	SCU:smu_wdt_run	SMU_core RUN state indication
SMU:INT(2:0)	to	INT:smu.INT(2:0)	SMU Service Request

## 15.6 Revision History

**Table 274 Revision History**

Reference	Change to Previous Version	Comment
V4.0.17		
Page 44	Updated description of ALM9[22]	
Page 26	Updated PMS Pre-Alarm Mapping table	

**Safety Management Unit (SMU)****Table 274 Revision History (cont'd)**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
<b>V4.0.18</b>		
<a href="#">Page 49</a>	Updated description of ALM21[0] and ALM21[3]	
<a href="#">Page 49</a>	Added description for ALM21[6]	
<a href="#">Page 41</a>	Updated description for ALM8[20]	
<a href="#">Page 1</a>	Missing blank fixed	
<b>V4.0.19</b>		
<a href="#">Page 19</a> , <a href="#">Page 39</a>	Added FSI_RAM Alarms ALM7[0:2] which were not documented in the previous version	
<a href="#">Page 27</a>	Added Alarm Types in Alarm Mapping Tables	
<a href="#">Page 50</a>	Revision History updated	
<b>V4.0.20</b>		
-	No functional changes.	
<b>V4.0.21</b>		
-	No functional changes.	
<b>V4.0.22</b>		
<a href="#">Page 29</a> , <a href="#">Page 31</a> , <a href="#">Page 32</a> , <a href="#">Page 34</a> , <a href="#">Page 36</a>	Updated description of ALM1[0], ALM1[2], ALM2[0], ALM2[2], ALM3[0], ALM3[2], ALM4[0], ALM4[2], ALM5[0] and ALM5[2]	
<a href="#">Page 24</a> , <a href="#">Page 7</a>	Remove LMU.DAM0 and LMU.DAM1 related alarms ALM7[12:14], ALM7[16] as they don't exist in the device	
<b>V4.0.23</b>		
<a href="#">Page 37</a>	Updated description of ALM6[8]	
<a href="#">Page 47</a>	Updated description of ALM11[8]	

**Interrupt Router (INT)****16      Interrupt Router (INT)**

This chapter supplements the family documentation with device specific information for TC39x-B.

The Interrupt Router allocates two address ranges

- Interrupt Router System and OTGM register address range: 2 \* 256 byte address range covering the Interrupt Router system registers, ICU control registers and OTGM registers ([Chapter 16.2](#))
- SRC register address range: 8 KByte address range covering the Service Request Control registers ([Chapter 16.4](#))

**16.1    TC39x-B Specific Interrupt Router Configuration****Table 275 TC39x-B specific configuration of INT**

<b>Parameter</b>	<b>INT</b>
<b>Number of Interrupt Service Providers</b>	7
<b>Number of SRB groups</b>	6

**Table 276 TC39x-B specific configuration of SRC**

<b>Parameter</b>	<b>SRC</b>
<b>Number of Service Request Nodes</b>	1024

## Interrupt Router (INT)

### 16.2 TC39x-B Specific Control Registers

This chapter describes the TC39x-B specific Interrupt Router system, OTGM and ICU registers

#### List of used Access Protection Register abbreviations

- P0 -> ACCEN\_SRBy, write protection of the related SRBy register. Number of Service Request Broadcast registers (SRB) and the related ACCEN\_SRBy registers is equal to the number of implemented TriCore CPUs.
- P1 -> ACCEN\_CONFIG, write protection of all SRCx[15:0] and ICUx Error Capture registers (ECRx)
- P2 -> ACCEN\_SRC\_TOSx, write protects bits [31:16] of all SRCs that are mapped to TOSx (SCR.TOS=x). For each implemented Interrupt Control Unit, one ACCEN\_SRC\_TOSx register is implemented.

**Note:** A violation of the access protection will not be executed (e.g. a write to a 'Px' /ACCEN protected register by an SPB access with a disabled Master TAG-ID). In this case an access protection error is signaled to the SMU. Beside this signaling to the SMU, no other error, interrupt or trap is generated.

#### Interrupt Router Module Registers

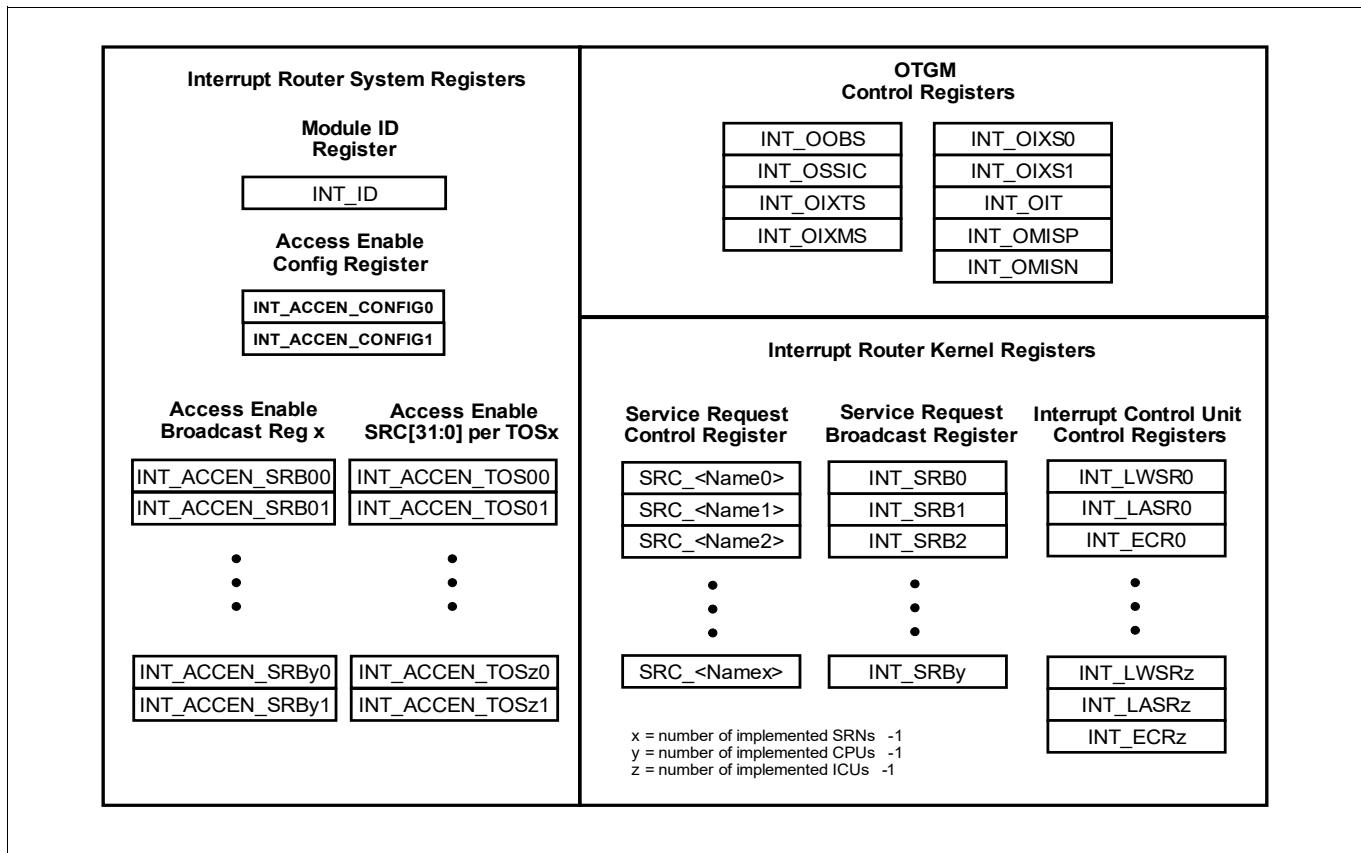


Figure 7 Interrupt Router module registers (SRC registers are described in [Chapter 16.4](#))

Table 277 Register Address Space - INT

Module	Base Address	End Address	Note
INT	F0037000 <sub>H</sub>	F0037FFF <sub>H</sub>	IR Status and Control Registers

**Interrupt Router (INT)****Table 278 Register Overview - INT (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
INT_ID	Module Identification Register	0008 <sub>H</sub>	U,SV	nBE	Application Reset	See Family Spec
INT_SRBy (x=0-5)	Service Request Broadcast Register x	0010 <sub>H</sub> +x *4	U,SV	SV,P0	Application Reset	See Family Spec
INT_OOBS	OTGM OTGB0/1 Status	0080 <sub>H</sub>	U,SV	nBE	Application Reset	See Family Spec
INT_OSSIC	OTGM SSI Control	0084 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_OIXTS	OTGM IRQ MUX Trigger Set Select	0088 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_OIXMS	OTGM IRQ MUX Missed IRQ Select	008C <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_OIXS0	OTGM IRQ MUX Select 0	0090 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_OIXS1	OTGM IRQ MUX Select 1	0094 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_OIT	OTGM IRQ Trace	00A0 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_OMISP	OTGM MCDS I/F Sensitivity Posedge	00A4 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_OMISN	OTGM MCDS I/F Sensitivity Negedge	00A8 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
INT_ACCEN_CON FIG0	Access Enable covering all INT_ECRx and all SRCy[15:0], Register 0	00F0 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_CON FIG1	Access Enable covering all INT_ECRx and all SRCy[15:0], Register 1	00F4 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRBy (x=0-5)	Access Enable covering SRBx, Register 0	0100 <sub>H</sub> +x *8	U,SV	SV,SE	Application Reset	See Family Spec

**Interrupt Router (INT)****Table 278 Register Overview - INT (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
INT_ACCEN_SR <sub>B</sub> x1 (x=0-5)	Access Enable covering SRB <sub>x</sub> , Register 1	0104 <sub>H</sub> +x *8	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRC _TOSx0 (x=0-6)	Access Enable covering all SRC <sub>x</sub> [31:16] mapped to ICU <sub>x</sub> , Register 0	0180 <sub>H</sub> +x *8	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRC _TOSx1 (x=0-6)	Access Enable covering all SRC <sub>x</sub> [31:16] mapped to ICU <sub>x</sub> , Register 1	0184 <sub>H</sub> +x *8	U,SV	SV,SE	Application Reset	See Family Spec
INT_LWSRx (x=0-6)	Latest Winning Service Request Register x, related to ICU <sub>x</sub>	0200 <sub>H</sub> +x *10 <sub>H</sub>	U,SV	nBE	Application Reset	See Family Spec
INT_LASRx (x=0-6)	Last Acknowledged Service Request Register x, related to ICU <sub>x</sub>	0204 <sub>H</sub> +x *10 <sub>H</sub>	U,SV	nBE	Application Reset	See Family Spec
INT_ECRx (x=0-6)	Error Capture Register x, related to ICU <sub>x</sub>	0208 <sub>H</sub> +x *10 <sub>H</sub>	U,SV	SV,P1	Application Reset	See Family Spec

**16.3 TC39x-B Specific Registers**

No deviations from the Family Spec

**Interrupt Router (INT)****16.4 TC39x-B Specific Service Request Control (SRC) registers**

**This chapter describes the TC39x-B Service Request Control (SRC) registers.**

**Table 280** shows all registers associated with the Interrupt Router module in the device. This chapter describes the Service Request Control registers including:

- Mapping of Aurix module interrupt triggers to SRC
- SRC offsets
- The index number of an SRC can be calculated with the SRC Offset: Index(SRC) = <SRC Address Offset> / 4

**List of used Access Protection Register abbreviations**

- P0 -> ACCEN\_SRBy, write protection of the related SRBy register. Number of Service Request Broadcast registers (SRB) and the related ACCEN\_SRBy registers is equal to the number of implemented TriCore CPUs.
- P1 -> ACCEN\_CONFIG, write protection of all SRCx[15:0] and ICUx Error Capture registers (ECRx)
- P2 -> ACCEN\_SRC\_TOSy, write protects bits [31:16] of all SRCs that are mapped to TOSy (SCR.TOS=y). For each implemented Interrupt Control Unit, one ACCEN\_SRC\_TOSy register is implemented.

**Note:** *A violation of the access protection will not be executed (e.g. a write to a 'Px'/ACCEN protected register from a disabled master). In this case an access protection error is signaled to the SMU. Beside this signaling to the SMU, no other error, interrupt or trap is generated.*

**Table 279 Register Address Space - SRC**

Module	Base Address	End Address	Note		
SRC	F0038000 <sub>H</sub>	F0039FFF <sub>H</sub>	IR Service Request Control Registers (SRC)		

**Table 280 Register Overview - SRC (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_CPUxSB (x=0-5)	CPUx Software Breakpoint Service Request	00000 <sub>H</sub> + x*4	U,SV	SV,P1,P2	Debug Reset	<a href="#">11</a>
SRC_BCUSPB	SBCU Service Request (SPB Bus Control Unit)	00020 <sub>H</sub>	U,SV	SV,P1,P2	Debug Reset	<a href="#">11</a>
SRC_BCUBBB	EBCU Service Request (BBB Bus Control Unit, on ED and ADAS devices only)	00024 <sub>H</sub>	U,SV	SV,P1,P2	Debug Reset	<a href="#">11</a>
SRC_AGBT	AGBT Service Request (on ED devices only)	0002C <sub>H</sub>	U,SV	SV,P1,P2	Debug Reset	<a href="#">11</a>
SRC_XBARx (x=0-2)	SRI Domain x Service Request	00030 <sub>H</sub> + x*4	U,SV	SV,P1,P2	Debug Reset	<a href="#">11</a>
SRC_CERBERUSy (y=0-1)	Cerberus Service Request y	00040 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Debug Reset	<a href="#">11</a>
SRC_ASCLINxTX (x=0-11)	ASCLINx Transmit Service Request	00050 <sub>H</sub> + x*12	U,SV	SV,P1,P2	Application Reset	<a href="#">11</a>
SRC_ASCLINxRX (x=0-11)	ASCLINx Receive Service Request	00054 <sub>H</sub> + x*12	U,SV	SV,P1,P2	Application Reset	<a href="#">11</a>

**Interrupt Router (INT)****Table 280 Register Overview - SRC (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SRC_ASCLINxER R (x=0-11)	ASCLINx Error Service Request	00058 <sub>H</sub> + x*12	U,SV	SV,P1,P2	Application Reset	<a href="#">11</a>
SRC_MTUDONE	MTU Done Service Request	000EC <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">11</a>
SRC_QSPIxTX (x=0-5)	QSPIx Transmit Service Request	000F0 <sub>H</sub> + x*14 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_QSPIxRX (x=0-5)	QSPIx Receive Service Request	000F4 <sub>H</sub> + x*14 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_QSPIxERR (x=0-5)	QSPIx Error Service Request	000F8 <sub>H</sub> + x*14 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_QSPIxPT (x=0-5)	QSPIx Phase Transition Service Request	000FC <sub>H</sub> + x*14 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_QSPIxU (x=0-5)	QSPIx User Defined Service Request	00100 <sub>H</sub> + x*14 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_QSPI2HC	QSPI2 High Speed Capture Service Request	00178 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_QSPI3HC	QSPI3 High Speed Capture Service Request	0017C <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_HSCTx (x=0-1)	HSCTx Service Request	00180 <sub>H</sub> + x*4	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_HSSLxCOKy (x=0-1;y=0-3)	HSSLx Channel y OK Service Request	00190 <sub>H</sub> + x*44 <sub>H</sub> +y* 10 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_HSSLxRDly (x=0-1;y=0-3)	HSSLx Channel y Read Data Service Request	00194 <sub>H</sub> + x*44 <sub>H</sub> +y* 10 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">14</a>
SRC_HSSLxERRy (x=0-1;y=0-3)	HSSLx Channel y Error Service Request	00198 <sub>H</sub> + x*44 <sub>H</sub> +y* 10 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">16</a>
SRC_HSSLxTRGy (x=0-1;y=0-3)	HSSLx Channel y Trigger Interrupt Service Request	0019C <sub>H</sub> + x*44 <sub>H</sub> +y* 10 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">16</a>
SRC_HSSLxEXI (x=0-1)	HSSLx Exception Service Request	001D0 <sub>H</sub> + x*44 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">16</a>
SRC_I2CxDTR (x=0-1)	I2Cx Data Transfer Request	00220 <sub>H</sub> + x*10 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">16</a>
SRC_I2CxERR (x=0-1)	I2Cx Error Service Request	00224 <sub>H</sub> + x*10 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">16</a>
SRC_I2CxP (x=0-1)	I2Cx Protocol Service Request	00228 <sub>H</sub> + x*10 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">16</a>

**Interrupt Router (INT)****Table 280 Register Overview - SRC (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SRC_SENTx (x=0-9)	SENT TRIGx Service Request	00240 <sub>H</sub> + x*4	U,SV	SV,P1,P2	Application Reset	<b>16</b>
SRC_MSCxSRy (x=0-3;y=0-4)	MSCx Service Request y	00270 <sub>H</sub> + x*14 <sub>H</sub> +y*4	U,SV	SV,P1,P2	Application Reset	<b>16</b>
SRC_CCU6xSRy (x=0-1;y=0-3)	CCUx Service Request y	002C0 <sub>H</sub> + x*10 <sub>H</sub> +y*4	U,SV	SV,P1,P2	Application Reset	<b>16</b>
SRC_GPT120CIRQ	GPT120 CAPREL Service Request	002E0 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>16</b>
SRC_GPT120T2	GPT120 Timer 2 Service Request	002E4 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_GPT120T3	GPT120 Timer 3 Service Request	002E8 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_GPT120T4	GPT120 Timer 4 Service Request	002EC <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_GPT120T5	GPT120 Timer 5 Service Request	002F0 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_GPT120T6	GPT120 Timer 6 Service Request	002F4 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_STMxSRy (x=0-5;y=0-1)	System Timer x Service Request y	00300 <sub>H</sub> + x*8+y*4	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_FCE0	FCE0 Error Service Request	00330 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_DMAERRy (y=0-3)	DMA Error Service Request y	00340 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_DMACHy (y=0-127)	DMA Channel y Service Request	00370 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_SDMMCERR	SDMMC Error Service Request	00570 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>19</b>
SRC_SDMMCDMA	SDMMC DMA Ready Service Request	00574 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<b>21</b>
SRC_GETHy (y=0-9)	GETH Service Request y	00580 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Application Reset	<b>21</b>
SRC_CANxINTy (x=0-2;y=0-15)	CANx Service Request y	005B0 <sub>H</sub> + x*40 <sub>H</sub> +y*4	U,SV	SV,P1,P2	Application Reset	<b>21</b>
SRC_VADCGxSRy (x=0-11;y=0-3)	EVADC Group x Service Request y	00670 <sub>H</sub> + x*10 <sub>H</sub> +y*4	U,SV	SV,P1,P2	Application Reset	<b>21</b>

**Interrupt Router (INT)****Table 280 Register Overview - SRC (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SRC_VADCFCxSR 0 (x=0-7)	EVADC Fast Compare x Service Request SR0	00730 <sub>H</sub> + x*4	U,SV	SV,P1,P2	Application Reset	<a href="#">21</a>
SRC_VADCCGxSR y (x=0-1;y=0-3)	EVADC Common Group x Service Request y	00750 <sub>H</sub> + x*10 <sub>H</sub> +y*4	U,SV	SV,P1,P2	Application Reset	<a href="#">21</a>
SRC_DSADCxSRM x (x=0-13)	DSADC SRMx Service Request	00770 <sub>H</sub> + x*8	U,SV	SV,P1,P2	Application Reset	<a href="#">21</a>
SRC_DSADCxSRAx (x=0-13)	DSADC SRAx Service Request	00774 <sub>H</sub> + x*8	U,SV	SV,P1,P2	Application Reset	<a href="#">21</a>
SRC_ERAYxINT0 (x=0-1)	E-RAY x Service Request 0	00800 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">21</a>
SRC_ERAYxINT1 (x=0-1)	E-RAY x Service Request 1	00804 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">21</a>
SRC_ERAYxTINT0 (x=0-1)	E-RAY x Timer Interrupt 0 Service Request	00808 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_ERAYxTINT1 (x=0-1)	E-RAY x Timer Interrupt 1 Service Request	0080C <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_ERAYxNDAT 0 (x=0-1)	E-RAY x New Data 0 Service Request	00810 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_ERAYxNDAT 1 (x=0-1)	E-RAY x New Data 1 Service Request	00814 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_ERAYxMBSC 0 (x=0-1)	E-RAY x Message Buffer Status Changed 0 Service Request	00818 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_ERAYxMBSC 1 (x=0-1)	E-RAY x Message Buffer Status Changed 1 Service Request	0081C <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_ERAYxOBUS Y (x=0-1)	E-RAY x Output Buffer Busy	00820 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_ERAYxIBUSY (x=0-1)	E-RAY x Input Buffer Busy	00824 <sub>H</sub> + x*30 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_DMUHOST	DMU Host Service Request	00860 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_DMUFSI	DMU FSI Service Request	00864 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">24</a>
SRC_HSMY (y=0-1)	HSM Service Request y	00870 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>

**Interrupt Router (INT)****Table 280 Register Overview - SRC (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SRC_SCUERUx (x=0-3)	SCU ERU Service Request x	00880 <sub>H</sub> + x*4	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_PMSDTS	PMS DTS Service Request	008AC <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_PMSx (x=0-3)	Power Management System Service Request x	008B0 <sub>H</sub> + x*4	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_SCR	Stand By Controller Service Request	008C0 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_SMUy (y=0-2)	SMU Service Request y	008D0 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_PSI5y (y=0-7)	PSI5 Service Request y	008E0 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_HSPDM0BF R	HSPDM0 Buffer Service Request	00900 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_HSPDM0RA MP	HSPDM0 RAMP Events Service Request	00904 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_HSPDM0ER R	HSPDM0 Error / RAM Overflow Service Request	00908 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">26</a>
SRC_DAMxLI0 (x=0-1)	DAMx Limit 0 Service Request	00910 <sub>H</sub> + x*18 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_DAMxRI0 (x=0-1)	DAMx Ready 0 Service Reques	00914 <sub>H</sub> + x*18 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_DAMxLI1 (x=0-1)	DAMx Limit 1 Service Request	00918 <sub>H</sub> + x*18 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_DAMxRI1 (x=0-1)	DAMx Ready 1 Service Request	0091C <sub>H</sub> + x*18 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_DAMxDR (x=0-1)	DAMx DMA Ready Service Request	00920 <sub>H</sub> + x*18 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_DAMxERR (x=0-1)	DAMx Error Service Request	00924 <sub>H</sub> + x*18 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_PSI5Sy (y=0-7)	PSI5-S Service Request y	00950 <sub>H</sub> + y*4	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_RIFxERR (x=0-1)	Radar Interface x Error Service Request	00970 <sub>H</sub> + x*8	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_RIFxINT (x=0-1)	Radar Interface x Service Request	00974 <sub>H</sub> + x*8	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_SPUxINT (x=0-1)	SPU x Service Request	00980 <sub>H</sub> + x*8	U,SV	SV,P1,P2	Application Reset	<a href="#">29</a>
SRC_SPUxERR (x=0-1)	SPU x Error Service Request	00984 <sub>H</sub> + x*8	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>

**Interrupt Router (INT)****Table 280 Register Overview - SRC (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
SRC_GPSRxy (x=0-5;y=0-7)	General Purpose Group x Service Request y	00990 <sub>H</sub> + x*20 <sub>H</sub> +y* 4	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTMAEIIRQ	AEI Shared Service Request	00A70 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTMARUIRQ w (w=0-2)	ARU Shared Service Request w	00A74 <sub>H</sub> + w*4	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTMBRCIRQ	BRC Shared Service Request	00A80 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTMCMPIR Q	CMP Shared Service Request Q	00A84 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTMSPEwIR Q (w=0-5)	SPEw Shared Service Request	00A88 <sub>H</sub> + w*4	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTPPSMwx (w=0-2;x=0-7)	PSMw Shared Service Request x	00AA0 <sub>H</sub> + w*20 <sub>H</sub> +x* 4	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTMDPLLw (w=0-26)	DPLL Service Request w	00B00 <sub>H</sub> + w*4	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GTMERR	Error Service Request	00B70 <sub>H</sub>	U,SV	SV,P1,P2	Application Reset	<a href="#">31</a>
SRC_GMTTIMwx (w=0-7;x=0-7)	TIMw Shared Service Request x	00B90 <sub>H</sub> + w*20 <sub>H</sub> +x* 4	U,SV	SV,P1,P2	Application Reset	<a href="#">34</a>
SRC_GTMMCSwx (w=0-9;x=0-7)	MCSw Shared Service Request x	00CB0 <sub>H</sub> + w*20 <sub>H</sub> +x* 4	U,SV	SV,P1,P2	Application Reset	<a href="#">34</a>
SRC_GMTTOMwx (w=0-5;x=0-7)	TOMw Shared Service Request x	00E10 <sub>H</sub> + w*20 <sub>H</sub> +x* 4	U,SV	SV,P1,P2	Application Reset	<a href="#">34</a>
SRC_GTMATOMw x (w=0-11;x=0-3)	ATOMw Shared Service Request x	00EF0 <sub>H</sub> + w*10 <sub>H</sub> +x* 4	U,SV	SV,P1,P2	Application Reset	<a href="#">34</a>
SRC_GTMMCSW w (w=0-9)	GTM Multi Channel Sequencer Service Request w	00FD0 <sub>H</sub> + w*4	U,SV	SV,P1,P2	Application Reset	<a href="#">34</a>

**Interrupt Router (INT)****16.5 TC39x-B Specific Registers****16.5.1 IR Service Request Control Registers (SRC)****CPUx Software Breakpoint Service Request****SRC\_CPUxSB (x=0-5)**CPUx Software Breakpoint Service Request ( $00000_H + x^*4$ )Debug Reset Value:  $0000\ 0000_H$ **SRC\_BCUSPB**SBCU Service Request [SPB Bus Control Unit] ( $00020_H$ )Debug Reset Value:  $0000\ 0000_H$ **SRC\_BCUBBB**EBCU Service Request [BBB Bus Control Unit, on ED and ADAS devices only] ( $00024_H$ ) Debug Reset Value: $0000\ 0000_H$ **SRC\_AGBT**AGBT Service Request [on ED devices only] ( $0002C_H$ )Debug Reset Value:  $0000\ 0000_H$ **SRC\_XBARx (x=0-2)**SRI Domain x Service Request ( $00030_H + x^*4$ )Debug Reset Value:  $0000\ 0000_H$ **SRC\_CERBERUSy (y=0-1)**Cerberus Service Request y ( $00040_H + y^*4$ )Debug Reset Value:  $0000\ 0000_H$ **SRC\_ASCLINxTX (x=0-11)**ASCLINx Transmit Service Request ( $00050_H + x^*12$ )Application Reset Value:  $0000\ 0000_H$ **SRC\_ASCLINxRX (x=0-11)**ASCLINx Receive Service Request ( $00054_H + x^*12$ )Application Reset Value:  $0000\ 0000_H$ **SRC\_ASCLINxERR (x=0-11)**ASCLINx Error Service Request ( $00058_H + x^*12$ )Application Reset Value:  $0000\ 0000_H$ **SRC\_MTUDONE**MTU Done Service Request ( $000EC_H$ )Application Reset Value:  $0000\ 0000_H$ 

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSC LR	SWS	IOVCL R	IOV	SETR	CLRR	SRR	0					ECC		
r	w	rh	w	rh	w	w	rh	r					rwh		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS		SRE	0						SRPN				
r		rw		rw	r						rw				

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SRPN</b>	7:0	rw	<p><b>Service Request Priority Number</b>  The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):  <math>00_H</math> -&gt; Service request is on lowest priority  ...  <math>FF_H</math> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU <math>01_H</math> is the lowest priority as <math>00_H</math> is never serviced.  For a DMA <math>00_H</math> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
<b>SRE</b>	10	rw	<p><b>Service Request Enable</b>  <math>0_B</math> Service request is disabled  <math>1_B</math> Service request is enabled</p>
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b>  The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:  <math>000_B</math> CPU0 service is initiated  <math>001_B</math> DMA service is initiated  <math>010_B</math> CPU1 service is initiated  <math>011_B</math> CPU2 service is initiated  <math>100_B</math> CPU3 service is initiated  <math>101_B</math> CPU4 service is initiated  <math>110_B</math> CPU5 service is initiated  <b>Others</b>, Reserved (no action)</p>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b>  The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>Write or Read-Modify-Write to SRC[31:0]</li> <li>Write to SRC[15:0] (16-bit write)</li> <li>Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b>  The SRR bit shows the status of the Service Request.  <math>0_B</math> No service request is pending  <math>1_B</math> A service request is pending</p>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b>  The CLRR bit is required to reset <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SETR</b>	26	w	<p><b>Request Set Bit</b>            The SETR bit is required to set <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b>            The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.  <math>0_B</math> No Interrupt Trigger Overflow detected  <math>1_B</math> Interrupt Overflow Detected.</p>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b>            IOVCLR is required to reset <b>IOV</b>.  <math>0_B</math> No action  <math>1_B</math> Clear IOV; bit value is not stored; read always returns 0.</p>
<b>SWS</b>	29	rh	<p><b>SW Sticky Bit</b>            The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit.            This bit can be cleared by writing with 1 to <b>SWSCLR</b>.            Writing to SWS has no effect.  <math>0_B</math> No interrupt was initiated via SETR  <math>1_B</math> Interrupt was initiated via SETR</p>
<b>SWSCLR</b>	30	w	<p><b>SW Sticky Clear Bit</b>            SWSCLR is required to reset <b>SWS</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SWS; bit value is not stored; read always returns 0.</p>
<b>0</b>	9:8, 15:14, 23:21, 31	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

## Interrupt Router (INT)

**SRC\_QSPIxTX (x=0-5)**

**QSPIx Transmit Service Request** ( $000F0_H+x*14_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_QSPIxRX (x=0-5)**

**QSPIx Receive Service Request** ( $000F4_H+x*14_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_QSPIxERR (x=0-5)**

**QSPIx Error Service Request** ( $000F8_H+x*14_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_QSPIxPT (x=0-5)**

**QSPIx Phase Transition Service Request** ( $000FC_H+x*14_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_QSPIxU (x=0-5)**

**QSPIx User Defined Service Request** ( $00100_H+x*14_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_QSPI2HC**

**QSPI2 High Speed Capture Service Request** ( $00178_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_QSPI3HC**

**QSPI3 High Speed Capture Service Request** ( $0017C_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_HSCTx (x=0-1)**

**HSCTx Service Request** ( $00180_H+x*4$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_HSSLxCOKy (x=0-1;y=0-3)**

**HSSLx Channel y OK Service Request** ( $00190_H+x*44_H+y*10_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_HSSLxRDIy (x=0-1;y=0-3)**

**HSSLx Channel y Read Data Service Request** ( $00194_H+x*44_H+y*10_H$ ) **Application Reset Value:** 0000 0000<sub>H</sub>

															31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSC LR	SWS	IOVCL R	IOV	SETR	CLRR	SRR		0							ECC														
r	w	rh	w	rh	w	w	w	rh	r							rwh														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
0		TOS		SRE		0									SRPN															
r		rw		rw		r									rw															

Field	Bits	Type	Description
SRPN	7:0	rw	<p><b>Service Request Priority Number</b>            The SRPN bit field defines the priority of a service request with respect to service requests with the same service provider (same SRC.TOS configuration):  <math>00_H \rightarrow</math> Service request is on lowest priority            ...  <math>FF_H \rightarrow</math> Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU <math>01_H</math> is the lowest priority as <math>00_H</math> is never serviced.            For a DMA <math>00_H</math> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
SRE	10	rw	<p><b>Service Request Enable</b>  <math>0_B</math> Service request is disabled  <math>1_B</math> Service request is enabled</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b></p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <ul style="list-style-type: none"> <li>000<sub>B</sub> CPU0 service is initiated</li> <li>001<sub>B</sub> DMA service is initiated</li> <li>010<sub>B</sub> CPU1 service is initiated</li> <li>011<sub>B</sub> CPU2 service is initiated</li> <li>100<sub>B</sub> CPU3 service is initiated</li> <li>101<sub>B</sub> CPU4 service is initiated</li> <li>110<sub>B</sub> CPU5 service is initiated</li> <li><b>Others</b>, Reserved (no action)</li> </ul>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b></p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>• Write or Read-Modify-Write to SRC[31:0]</li> <li>• Write to SRC[15:0] (16-bit write)</li> <li>• Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b></p> <p>The SRR bit shows the status of the Service Request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No service request is pending</li> <li>1<sub>B</sub> A service request is pending</li> </ul>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b></p> <p>The CLRR bit is required to reset <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</li> </ul>
<b>SETR</b>	26	w	<p><b>Request Set Bit</b></p> <p>The SETR bit is required to set <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</li> </ul>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b></p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No Interrupt Trigger Overflow detected</li> <li>1<sub>B</sub> Interrupt Overflow Detected.</li> </ul>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b></p> <p>IOVCLR is required to reset <b>IOV</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear IOV; bit value is not stored; read always returns 0.</li> </ul>

## Interrupt Router (INT)

Field	Bits	Type	Description
<b>SWS</b>	29	rh	<b>SW Sticky Bit</b> The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit. This bit can be cleared by writing with 1 to <b>SWSLCR</b> . Writing to SWS has no effect. 0 <sub>B</sub> No interrupt was initiated via SETR 1 <sub>B</sub> Interrupt was initiated via SETR
<b>SWSLCR</b>	30	w	<b>SW Sticky Clear Bit</b> SWSLCR is required to reset <b>SWS</b> . 0 <sub>B</sub> No action 1 <sub>B</sub> Clear SWS; bit value is not stored; read always returns 0.
<b>0</b>	9:8, 15:14, 23:21, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**SRC\_HSSLxERRy (x=0-1;y=0-3)**HSSLx Channel y Error Service Request (00198<sub>H</sub>+x\*44<sub>H</sub>+y\*10<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_HSSLxTRGy (x=0-1;y=0-3)**HSSLx Channel y Trigger Interrupt Service Request(0019C<sub>H</sub>+x\*44<sub>H</sub>+y\*10<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_HSSLxEXI (x=0-1)**HSSLx Exception Service Request (001D0<sub>H</sub>+x\*44<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_I2CxDT Ry (x=0-1)**I2Cx Data Transfer Request (00220<sub>H</sub>+x\*10<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_I2CxERR (x=0-1)**I2Cx Error Service Request (00224<sub>H</sub>+x\*10<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_I2CxP (x=0-1)**I2Cx Protocol Service Request (00228<sub>H</sub>+x\*10<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_SENTx (x=0-9)**SENT TRIGx Service Request (00240<sub>H</sub>+x\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_MSCxSRy (x=0-3;y=0-4)**MSCx Service Request y (00270<sub>H</sub>+x\*14<sub>H</sub>+y\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_CCU6xSRy (x=0-1;y=0-3)**CCUx Service Request y (002C0<sub>H</sub>+x\*10<sub>H</sub>+y\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GPT120CIRQ**GPT120 CAPREL Service Request (002E0<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSLCR	SWS	IOVCLR	IOV	SETR	CLRR	SRR	0						ECC	
r	w	rh	w	rh	w	w	rh	r						rwh	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS		SRE	0								SRPN		

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SRPN</b>	7:0	rw	<p><b>Service Request Priority Number</b>            The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):  <math>00_H</math> -&gt; Service request is on lowest priority            ...  <math>FF_H</math> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU <math>01_H</math> is the lowest priority as <math>00_H</math> is never serviced.            For a DMA <math>00_H</math> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
<b>SRE</b>	10	rw	<p><b>Service Request Enable</b>  <math>0_B</math> Service request is disabled  <math>1_B</math> Service request is enabled</p>
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b>            The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <ul style="list-style-type: none"> <li><math>000_B</math> CPU0 service is initiated</li> <li><math>001_B</math> DMA service is initiated</li> <li><math>010_B</math> CPU1 service is initiated</li> <li><math>011_B</math> CPU2 service is initiated</li> <li><math>100_B</math> CPU3 service is initiated</li> <li><math>101_B</math> CPU4 service is initiated</li> <li><math>110_B</math> CPU5 service is initiated</li> </ul> <p><b>Others</b>, Reserved (no action)</p>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b>            The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>• Write or Read-Modify-Write to SRC[31:0]</li> <li>• Write to SRC[15:0] (16-bit write)</li> <li>• Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b>            The SRR bit shows the status of the Service Request.</p> <p><math>0_B</math> No service request is pending  <math>1_B</math> A service request is pending</p>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b>            The CLRR bit is required to reset <b>SRR</b>.</p> <p><math>0_B</math> No action  <math>1_B</math> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SETR</b>	26	w	<p><b>Request Set Bit</b>            The SETR bit is required to set <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b>            The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.  <math>0_B</math> No Interrupt Trigger Overflow detected  <math>1_B</math> Interrupt Overflow Detected.</p>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b>            IOVCLR is required to reset <b>IOV</b>.  <math>0_B</math> No action  <math>1_B</math> Clear IOV; bit value is not stored; read always returns 0.</p>
<b>SWS</b>	29	rh	<p><b>SW Sticky Bit</b>            The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit.            This bit can be cleared by writing with 1 to <b>SWSCLR</b>.            Writing to SWS has no effect.  <math>0_B</math> No interrupt was initiated via SETR  <math>1_B</math> Interrupt was initiated via SETR</p>
<b>SWSCLR</b>	30	w	<p><b>SW Sticky Clear Bit</b>            SWSCLR is required to reset <b>SWS</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SWS; bit value is not stored; read always returns 0.</p>
<b>0</b>	9:8, 15:14, 23:21, 31	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

## Interrupt Router (INT)

**SRC\_GPT120T2**

**GPT120 Timer 2 Service Request** (002E4<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_GPT120T3**

**GPT120 Timer 3 Service Request** (002E8<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_GPT120T4**

**GPT120 Timer 4 Service Request** (002EC<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_GPT120T5**

**GPT120 Timer 5 Service Request** (002F0<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_GPT120T6**

**GPT120 Timer 6 Service Request** (002F4<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_STMxSRy (x=0-5;y=0-1)**

**System Timer x Service Request y** (00300<sub>H</sub>+x\*8+y\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_FCE0**

**FCE0 Error Service Request** (00330<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_DMAERRy (y=0-3)**

**DMA Error Service Request y** (00340<sub>H</sub>+y\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_DMACHy (y=0-127)**

**DMA Channel y Service Request** (00370<sub>H</sub>+y\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_SDMMCERR**

**SDMMC Error Service Request** (00570<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	<b>SWSC LR</b>	<b>SWS</b>	<b>IOVCLR</b>	<b>IOV</b>	<b>SETR</b>	<b>CLRR</b>	<b>SRR</b>		0					ECC	
r	w	rh	w	rh	w	w	w	rh	r					rwh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			<b>TOS</b>		<b>SRE</b>		0							<b>SRPN</b>	
r			rw		rw		r							rw	

Field	Bits	Type	Description
<b>SRPN</b>	7:0	rw	<p><b>Service Request Priority Number</b>            The SRPN bit field defines the priority of a service request with respect to service requests with the same service provider (same SRC.TOS configuration):            00<sub>H</sub> -&gt; Service request is on lowest priority            ...            FF<sub>H</sub> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU 01<sub>H</sub> is the lowest priority as 00<sub>H</sub> is never serviced.            For a DMA 00<sub>H</sub> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
<b>SRE</b>	10	rw	<p><b>Service Request Enable</b>            0<sub>B</sub> Service request is disabled            1<sub>B</sub> Service request is enabled</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b></p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <ul style="list-style-type: none"> <li>000<sub>B</sub> CPU0 service is initiated</li> <li>001<sub>B</sub> DMA service is initiated</li> <li>010<sub>B</sub> CPU1 service is initiated</li> <li>011<sub>B</sub> CPU2 service is initiated</li> <li>100<sub>B</sub> CPU3 service is initiated</li> <li>101<sub>B</sub> CPU4 service is initiated</li> <li>110<sub>B</sub> CPU5 service is initiated</li> <li><b>Others</b>, Reserved (no action)</li> </ul>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b></p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>• Write or Read-Modify-Write to SRC[31:0]</li> <li>• Write to SRC[15:0] (16-bit write)</li> <li>• Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b></p> <p>The SRR bit shows the status of the Service Request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No service request is pending</li> <li>1<sub>B</sub> A service request is pending</li> </ul>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b></p> <p>The CLRR bit is required to reset <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</li> </ul>
<b>SETR</b>	26	w	<p><b>Request Set Bit</b></p> <p>The SETR bit is required to set <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</li> </ul>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b></p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No Interrupt Trigger Overflow detected</li> <li>1<sub>B</sub> Interrupt Overflow Detected.</li> </ul>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b></p> <p>IOVCLR is required to reset <b>IOV</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear IOV; bit value is not stored; read always returns 0.</li> </ul>

## Interrupt Router (INT)

Field	Bits	Type	Description
<b>SWS</b>	29	rh	<b>SW Sticky Bit</b> The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit. This bit can be cleared by writing with 1 to <b>SWSLCR</b> . Writing to SWS has no effect. 0 <sub>B</sub> No interrupt was initiated via SETR 1 <sub>B</sub> Interrupt was initiated via SETR
<b>SWSLCR</b>	30	w	<b>SW Sticky Clear Bit</b> SWSLCR is required to reset <b>SWS</b> . 0 <sub>B</sub> No action 1 <sub>B</sub> Clear SWS; bit value is not stored; read always returns 0.
<b>0</b>	9:8, 15:14, 23:21, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**SRC\_SDMMC DMA**

<b>SDMMC DMA Ready Service Request</b>	(00574 <sub>H</sub> )	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_GETHy (y=0-9)</b>		
<b>GETH Service Request y</b>	(00580 <sub>H</sub> +y*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_CANxINTy (x=0-2;y=0-15)</b>		
<b>CANx Service Request y</b>	(005B0 <sub>H</sub> +x*40 <sub>H</sub> +y*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_VADCGxSRy (x=0-11;y=0-3)</b>		
<b>EVADC Group x Service Request y</b>	(00670 <sub>H</sub> +x*10 <sub>H</sub> +y*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_VADCFCxSR0 (x=0-7)</b>		
<b>EVADC Fast Compare x Service Request SR0</b>	(00730 <sub>H</sub> +x*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_VADCCGxSRy (x=0-1;y=0-3)</b>		
<b>EVADC Common Group x Service Request y</b>	(00750 <sub>H</sub> +x*10 <sub>H</sub> +y*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_DSADC SRMx (x=0-13)</b>		
<b>DSADC SRMx Service Request</b>	(00770 <sub>H</sub> +x*8)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_DSADC SRAx (x=0-13)</b>		
<b>DSADC SRAx Service Request</b>	(00774 <sub>H</sub> +x*8)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_ERAYxINT0 (x=0-1)</b>		
<b>E-RAY x Service Request 0</b>	(00800 <sub>H</sub> +x*30 <sub>H</sub> )	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>SRC_ERAYxINT1 (x=0-1)</b>		
<b>E-RAY x Service Request 1</b>	(00804 <sub>H</sub> +x*30 <sub>H</sub> )	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>	<b>SWSLCR</b>	<b>SWS</b>	<b>IOVCLR</b>	<b>IOV</b>	<b>SETR</b>	<b>CLRR</b>	<b>SRR</b>		<b>0</b>					<b>ECC</b>	
r	w	rh	w	rh	w	w	w	rh	r					rwh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>			<b>TOS</b>		<b>SRE</b>	<b>0</b>								<b>SRPN</b>	
r			rw		rw	r								rw	

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SRPN</b>	7:0	rw	<p><b>Service Request Priority Number</b>  The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):  <math>00_H</math> -&gt; Service request is on lowest priority  ...  <math>FF_H</math> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU <math>01_H</math> is the lowest priority as <math>00_H</math> is never serviced.  For a DMA <math>00_H</math> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
<b>SRE</b>	10	rw	<p><b>Service Request Enable</b>  <math>0_B</math> Service request is disabled  <math>1_B</math> Service request is enabled</p>
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b>  The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:  <math>000_B</math> CPU0 service is initiated  <math>001_B</math> DMA service is initiated  <math>010_B</math> CPU1 service is initiated  <math>011_B</math> CPU2 service is initiated  <math>100_B</math> CPU3 service is initiated  <math>101_B</math> CPU4 service is initiated  <math>110_B</math> CPU5 service is initiated  <b>Others</b>, Reserved (no action)</p>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b>  The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>Write or Read-Modify-Write to SRC[31:0]</li> <li>Write to SRC[15:0] (16-bit write)</li> <li>Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b>  The SRR bit shows the status of the Service Request.  <math>0_B</math> No service request is pending  <math>1_B</math> A service request is pending</p>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b>  The CLRR bit is required to reset <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SETR</b>	26	w	<p><b>Request Set Bit</b>            The SETR bit is required to set <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b>            The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.  <math>0_B</math> No Interrupt Trigger Overflow detected  <math>1_B</math> Interrupt Overflow Detected.</p>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b>            IOVCLR is required to reset <b>IOV</b>.  <math>0_B</math> No action  <math>1_B</math> Clear IOV; bit value is not stored; read always returns 0.</p>
<b>SWS</b>	29	rh	<p><b>SW Sticky Bit</b>            The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit.            This bit can be cleared by writing with 1 to <b>SWSCLR</b>.            Writing to SWS has no effect.  <math>0_B</math> No interrupt was initiated via SETR  <math>1_B</math> Interrupt was initiated via SETR</p>
<b>SWSCLR</b>	30	w	<p><b>SW Sticky Clear Bit</b>            SWSCLR is required to reset <b>SWS</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SWS; bit value is not stored; read always returns 0.</p>
<b>0</b>	9:8, 15:14, 23:21, 31	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

**Interrupt Router (INT)****SRC\_ERAYxTINT0 (x=0-1)****E-RAY x Timer Interrupt 0 Service Request (00808<sub>H</sub>+x\*30<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>****SRC\_ERAYxTINT1 (x=0-1)****E-RAY x Timer Interrupt 1 Service Request (0080C<sub>H</sub>+x\*30<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>****SRC\_ERAYxNDAT0 (x=0-1)****E-RAY x New Data 0 Service Request (00810<sub>H</sub>+x\*30<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>****SRC\_ERAYxNDAT1 (x=0-1)****E-RAY x New Data 1 Service Request (00814<sub>H</sub>+x\*30<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>****SRC\_ERAYxMBSC0 (x=0-1)****E-RAY x Message Buffer Status Changed 0 Service Request(00818<sub>H</sub>+x\*30<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>****SRC\_ERAYxMBSC1 (x=0-1)****E-RAY x Message Buffer Status Changed 1 Service Request(0081C<sub>H</sub>+x\*30<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>****SRC\_ERAYxOBUSY (x=0-1)****E-RAY x Output Buffer Busy (00820<sub>H</sub>+x\*30<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>****SRC\_ERAYxIBUSY (x=0-1)****E-RAY x Input Buffer Busy (00824<sub>H</sub>+x\*30<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>****DMUHOST****DMU Host Service Request (00860<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>****SRC\_DMUFSI****DMU FSI Service Request (00864<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>**

															16
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSC LR	SWS	IOVCL R	IOV	SETR	CLRR	SRR		0						ECC
r	w	rh	w	rh	w	w	w	rh	r						rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS		SRE		0									SRPN
r		rw		rw		r									rw

Field	Bits	Type	Description
SRPN	7:0	rw	<p><b>Service Request Priority Number</b></p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with the same service provider (same SRC.TOS configuration):</p> <p>00<sub>H</sub> -&gt; Service request is on lowest priority</p> <p>...</p> <p>FF<sub>H</sub> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU 01<sub>H</sub> is the lowest priority as 00<sub>H</sub> is never serviced.</li> <li>For a DMA 00<sub>H</sub> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SRE</b>	10	rw	<b>Service Request Enable</b> 0 <sub>B</sub> Service request is disabled 1 <sub>B</sub> Service request is enabled
<b>TOS</b>	13:11	rw	<b>Type of Service Control</b> The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000 <sub>B</sub> CPU0 service is initiated 001 <sub>B</sub> DMA service is initiated 010 <sub>B</sub> CPU1 service is initiated 011 <sub>B</sub> CPU2 service is initiated 100 <sub>B</sub> CPU3 service is initiated 101 <sub>B</sub> CPU4 service is initiated 110 <sub>B</sub> CPU5 service is initiated <b>Others</b> , Reserved (no action)
<b>ECC</b>	20:16	rwh	<b>Error Correction Code</b> The ECC bit field will be updated by the SRN under the following conditions: <ul style="list-style-type: none"> <li>• Write or Read-Modify-Write to SRC[31:0]</li> <li>• Write to SRC[15:0] (16-bit write)</li> <li>• Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<b>Service Request Flag</b> The SRR bit shows the status of the Service Request. 0 <sub>B</sub> No service request is pending 1 <sub>B</sub> A service request is pending
<b>CLRR</b>	25	w	<b>Request Clear Bit</b> The CLRR bit is required to reset <b>SRR</b> . 0 <sub>B</sub> No action 1 <sub>B</sub> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
<b>SETR</b>	26	w	<b>Request Set Bit</b> The SETR bit is required to set <b>SRR</b> . 0 <sub>B</sub> No action 1 <sub>B</sub> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.
<b>IOV</b>	27	rh	<b>Interrupt Trigger Overflow Bit</b> The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request. 0 <sub>B</sub> No Interrupt Trigger Overflow detected 1 <sub>B</sub> Interrupt Overflow Detected.
<b>IOVCLR</b>	28	w	<b>Interrupt Trigger Overflow Clear Bit</b> IOVCLR is required to reset <b>IOV</b> . 0 <sub>B</sub> No action 1 <sub>B</sub> Clear IOV; bit value is not stored; read always returns 0.

## Interrupt Router (INT)

Field	Bits	Type	Description
<b>SWS</b>	29	rh	<b>SW Sticky Bit</b> The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit. This bit can be cleared by writing with 1 to <b>SWSLCR</b> . Writing to SWS has no effect. 0 <sub>B</sub> No interrupt was initiated via SETR 1 <sub>B</sub> Interrupt was initiated via SETR
<b>SWSLCR</b>	30	w	<b>SW Sticky Clear Bit</b> SWSLCR is required to reset <b>SWS</b> . 0 <sub>B</sub> No action 1 <sub>B</sub> Clear SWS; bit value is not stored; read always returns 0.
<b>0</b>	9:8, 15:14, 23:21, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**SRC\_HSM<sub>y</sub> (y=0-1)**

**HSM Service Request y** (00870<sub>H</sub>+y\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_SCUERU<sub>x</sub> (x=0-3)**

**SCU ERU Service Request x** (00880<sub>H</sub>+x\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_PMSDTS**

**PMS DTS Service Request** (008AC<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_PMS<sub>x</sub> (x=0-3)**

**Power Management System Service Request x**(008B0<sub>H</sub>+x\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_SCR**

**Stand By Controller Service Request** (008C0<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_SMU<sub>y</sub> (y=0-2)**

**SMU Service Request y** (008D0<sub>H</sub>+y\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_PSI5<sub>y</sub> (y=0-7)**

**PSI5 Service Request y** (008E0<sub>H</sub>+y\*4) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_HSPDM0BFR**

**HSPDM0 Buffer Service Request** (00900<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_HSPDM0RAMP**

**HSPDM0 RAMP Events Service Request** (00904<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

**SRC\_HSPDM0ERR**

**HSPDM0 Error / RAM Overflow Service Request** (00908<sub>H</sub>) **Application Reset Value:** 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>0</b>	<b>SWSLCR</b>	<b>SWS</b>	<b>IOVCLR</b>	<b>IOV</b>	<b>SETR</b>	<b>CLRR</b>	<b>SRR</b>		<b>0</b>					<b>ECC</b>	
r	w	rh	w	rh	w	w	w	rh	r					rwh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>TOS</b>				<b>SRE</b>	<b>0</b>							<b>SRPN</b>		
r													rw		

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SRPN</b>	7:0	rw	<p><b>Service Request Priority Number</b>  The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):  <math>00_H</math> -&gt; Service request is on lowest priority  ...  <math>FF_H</math> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU <math>01_H</math> is the lowest priority as <math>00_H</math> is never serviced.  For a DMA <math>00_H</math> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
<b>SRE</b>	10	rw	<p><b>Service Request Enable</b>  <math>0_B</math> Service request is disabled  <math>1_B</math> Service request is enabled</p>
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b>  The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:  <math>000_B</math> CPU0 service is initiated  <math>001_B</math> DMA service is initiated  <math>010_B</math> CPU1 service is initiated  <math>011_B</math> CPU2 service is initiated  <math>100_B</math> CPU3 service is initiated  <math>101_B</math> CPU4 service is initiated  <math>110_B</math> CPU5 service is initiated  <b>Others</b>, Reserved (no action)</p>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b>  The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>Write or Read-Modify-Write to SRC[31:0]</li> <li>Write to SRC[15:0] (16-bit write)</li> <li>Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b>  The SRR bit shows the status of the Service Request.  <math>0_B</math> No service request is pending  <math>1_B</math> A service request is pending</p>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b>  The CLRR bit is required to reset <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SETR</b>	26	w	<p><b>Request Set Bit</b>            The SETR bit is required to set <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b>            The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.  <math>0_B</math> No Interrupt Trigger Overflow detected  <math>1_B</math> Interrupt Overflow Detected.</p>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b>            IOVCLR is required to reset <b>IOV</b>.  <math>0_B</math> No action  <math>1_B</math> Clear IOV; bit value is not stored; read always returns 0.</p>
<b>SWS</b>	29	rh	<p><b>SW Sticky Bit</b>            The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit.            This bit can be cleared by writing with 1 to <b>SWSCLR</b>.            Writing to SWS has no effect.  <math>0_B</math> No interrupt was initiated via SETR  <math>1_B</math> Interrupt was initiated via SETR</p>
<b>SWSCLR</b>	30	w	<p><b>SW Sticky Clear Bit</b>            SWSCLR is required to reset <b>SWS</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SWS; bit value is not stored; read always returns 0.</p>
<b>0</b>	9:8, 15:14, 23:21, 31	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

## Interrupt Router (INT)

**SRC\_DAMxLI0 (x=0-1)**DAMx Limit 0 Service Request (00910<sub>H</sub>+x\*18<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_DAMxRI0 (x=0-1)**DAMx Ready 0 Service Requests (00914<sub>H</sub>+x\*18<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_DAMxLI1 (x=0-1)**DAMx Limit 1 Service Request (00918<sub>H</sub>+x\*18<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_DAMxRI1 (x=0-1)**DAMx Ready 1 Service Request (0091C<sub>H</sub>+x\*18<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_DAMxDR (x=0-1)**DAMx DMA Ready Service Request (00920<sub>H</sub>+x\*18<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_DAMxERR (x=0-1)**DAMx Error Service Request (00924<sub>H</sub>+x\*18<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_PS15Sy (y=0-7)**PS15-S Service Request y (00950<sub>H</sub>+y\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_RIFxERR (x=0-1)**Radar Interface x Error Service Request (00970<sub>H</sub>+x\*8) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_RIFxINT (x=0-1)**Radar Interface x Service Request (00974<sub>H</sub>+x\*8) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_SPUxINT (x=0-1)**SPU x Service Request (00980<sub>H</sub>+x\*8) Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSC LR	SWS	IOVCLR	IOV	SETR	CLRR	SRR	0					ECC		
r	w	rh	w	rh	w	w	rh	r					rwh		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS		SRE	0								SRPN		
r		rw		rw	r								rw		

Field	Bits	Type	Description
SRPN	7:0	rw	<p><b>Service Request Priority Number</b>            The SRPN bit field defines the priority of a service request with respect to service requests with the same service provider (same SRC.TOS configuration):            00<sub>H</sub> -&gt; Service request is on lowest priority            ...            FF<sub>H</sub> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU 01<sub>H</sub> is the lowest priority as 00<sub>H</sub> is never serviced.            For a DMA 00<sub>H</sub> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
SRE	10	rw	<p><b>Service Request Enable</b>            0<sub>B</sub> Service request is disabled            1<sub>B</sub> Service request is enabled</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b></p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <ul style="list-style-type: none"> <li>000<sub>B</sub> CPU0 service is initiated</li> <li>001<sub>B</sub> DMA service is initiated</li> <li>010<sub>B</sub> CPU1 service is initiated</li> <li>011<sub>B</sub> CPU2 service is initiated</li> <li>100<sub>B</sub> CPU3 service is initiated</li> <li>101<sub>B</sub> CPU4 service is initiated</li> <li>110<sub>B</sub> CPU5 service is initiated</li> <li><b>Others</b>, Reserved (no action)</li> </ul>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b></p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>• Write or Read-Modify-Write to SRC[31:0]</li> <li>• Write to SRC[15:0] (16-bit write)</li> <li>• Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b></p> <p>The SRR bit shows the status of the Service Request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No service request is pending</li> <li>1<sub>B</sub> A service request is pending</li> </ul>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b></p> <p>The CLRR bit is required to reset <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</li> </ul>
<b>SETR</b>	26	w	<p><b>Request Set Bit</b></p> <p>The SETR bit is required to set <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</li> </ul>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b></p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No Interrupt Trigger Overflow detected</li> <li>1<sub>B</sub> Interrupt Overflow Detected.</li> </ul>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b></p> <p>IOVCLR is required to reset <b>IOV</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear IOV; bit value is not stored; read always returns 0.</li> </ul>

## Interrupt Router (INT)

Field	Bits	Type	Description
<b>SWS</b>	29	rh	<b>SW Sticky Bit</b> The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit. This bit can be cleared by writing with 1 to <b>SWSLCR</b> . Writing to SWS has no effect. 0 <sub>B</sub> No interrupt was initiated via SETR 1 <sub>B</sub> Interrupt was initiated via SETR
<b>SWSLCR</b>	30	w	<b>SW Sticky Clear Bit</b> SWSLCR is required to reset <b>SWS</b> . 0 <sub>B</sub> No action 1 <sub>B</sub> Clear SWS; bit value is not stored; read always returns 0.
<b>0</b>	9:8, 15:14, 23:21, 31	r	<b>Reserved</b> Read as 0; should be written with 0.

**SRC\_SPUxERR (x=0-1)**SPU x Error Service Request (00984<sub>H</sub>+x\*8) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GPSRxy (x=0-5;y=0-7)**General Purpose Group x Service Request y(00990<sub>H</sub>+x\*20<sub>H</sub>+y\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMAEIIRQ**AEI Shared Service Request (00A70<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMARUIRQw (w=0-2)**ARU Shared Service Request w (00A74<sub>H</sub>+w\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMBCRCIRQ**BRC Shared Service Request (00A80<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMCMPIRQ**CMP Shared Service Request (00A84<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMSPPEwIRQ (w=0-5)**SPEw Shared Service Request (00A88<sub>H</sub>+w\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMPSMwx (w=0-2;x=0-7)**PSMw Shared Service Request x (00AA0<sub>H</sub>+w\*20<sub>H</sub>+x\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMDPLLw (w=0-26)**DPLL Service Request w (00B00<sub>H</sub>+w\*4) Application Reset Value: 0000 0000<sub>H</sub>**SRC\_GTMERR**Error Service Request (00B70<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	<b>SWSLCR</b>	<b>SWS</b>	<b>IOVCLR</b>	<b>IOV</b>	<b>SETR</b>	<b>CLRR</b>	<b>SRR</b>		0					ECC	
r	w	rh	w	rh	w	w	rh		r					rwh	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS			SRE	0						SRPN			

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SRPN</b>	7:0	rw	<p><b>Service Request Priority Number</b>            The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):  <math>00_H</math> -&gt; Service request is on lowest priority            ...  <math>FF_H</math> -&gt; Service request is on highest priority</p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>For a CPU <math>01_H</math> is the lowest priority as <math>00_H</math> is never serviced.            For a DMA <math>00_H</math> triggers channel 0.</li> <li>For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>
<b>SRE</b>	10	rw	<p><b>Service Request Enable</b>  <math>0_B</math> Service request is disabled  <math>1_B</math> Service request is enabled</p>
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b>            The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <ul style="list-style-type: none"> <li><math>000_B</math> CPU0 service is initiated</li> <li><math>001_B</math> DMA service is initiated</li> <li><math>010_B</math> CPU1 service is initiated</li> <li><math>011_B</math> CPU2 service is initiated</li> <li><math>100_B</math> CPU3 service is initiated</li> <li><math>101_B</math> CPU4 service is initiated</li> <li><math>110_B</math> CPU5 service is initiated</li> </ul> <p><b>Others</b>, Reserved (no action)</p>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b>            The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>• Write or Read-Modify-Write to SRC[31:0]</li> <li>• Write to SRC[15:0] (16-bit write)</li> <li>• Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b>            The SRR bit shows the status of the Service Request.</p> <p><math>0_B</math> No service request is pending  <math>1_B</math> A service request is pending</p>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b>            The CLRR bit is required to reset <b>SRR</b>.</p> <p><math>0_B</math> No action  <math>1_B</math> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SETR</b>	26	w	<p><b>Request Set Bit</b>            The SETR bit is required to set <b>SRR</b>.  <math>0_B</math> No action  <math>1_B</math> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b>            The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.  <math>0_B</math> No Interrupt Trigger Overflow detected  <math>1_B</math> Interrupt Overflow Detected.</p>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b>            IOVCLR is required to reset <b>IOV</b>.  <math>0_B</math> No action  <math>1_B</math> Clear IOV; bit value is not stored; read always returns 0.</p>
<b>SWS</b>	29	rh	<p><b>SW Sticky Bit</b>            The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit.            This bit can be cleared by writing with 1 to <b>SWSCLR</b>.            Writing to SWS has no effect.  <math>0_B</math> No interrupt was initiated via SETR  <math>1_B</math> Interrupt was initiated via SETR</p>
<b>SWSCLR</b>	30	w	<p><b>SW Sticky Clear Bit</b>            SWSCLR is required to reset <b>SWS</b>.  <math>0_B</math> No action  <math>1_B</math> Clear SWS; bit value is not stored; read always returns 0.</p>
<b>0</b>	9:8, 15:14, 23:21, 31	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

## **Interrupt Router (INT)**

<b>SRC_GTM TIM Wx (w=0-7;x=0-7)</b>	(00B90 <sub>H</sub> +w*20 <sub>H</sub> +x*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>TIMw Shared Service Request x</b>		
<b>SRC_GTM MCS Wx (w=0-9;x=0-7)</b>	(00CB0 <sub>H</sub> +w*20 <sub>H</sub> +x*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>MCSw Shared Service Request x</b>		
<b>SRC_GTM TOM Wx (w=0-5;x=0-7)</b>	(00E10 <sub>H</sub> +w*20 <sub>H</sub> +x*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>TOMw Shared Service Request x</b>		
<b>SRC_GTM ATOM Wx (w=0-11;x=0-3)</b>	(00EF0 <sub>H</sub> +w*10 <sub>H</sub> +x*4)	<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>
<b>ATOMw Shared Service Request x</b>		
<b>SRC_GTM MCSW w (w=0-9)</b>		
<b>GTM Multi Channel Sequencer Service Request w(00FD0<sub>H</sub>+w*4)</b>		<b>Application Reset Value:</b> 0000 0000 <sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	<b>SWSC LR</b>	<b>SWS</b>	<b>IOVCL R</b>	<b>IOV</b>	<b>SETR</b>	<b>CLRR</b>	<b>SRR</b>		0				<b>ECC</b>		
r	w	rh	w	rh	w	w	rh		r				rwh		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		<b>TOS</b>		<b>SRE</b>		0						<b>SRPN</b>			
r		rw		rw		r						rw			

Field	Bits	Type	Description				
SRPN	7:0	rw	<p><b>Service Request Priority Number</b></p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <ul style="list-style-type: none"> <li><math>00_H</math> -&gt; Service request is on lowest priority</li> <li>...</li> <li><math>FF_H</math> -&gt; Service request is on highest priority</li> </ul> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>1. For a CPU <math>01_H</math> is the lowest priority as <math>00_H</math> is never serviced. For a DMA <math>00_H</math> triggers channel 0.</li> <li>2. For DMA, SRPN must not be greater than the highest implemented DMA channel number.</li> </ol>				
SRE	10	rw	<p><b>Service Request Enable</b></p> <table> <tr> <td><math>0_B</math></td> <td>Service request is disabled</td> </tr> <tr> <td><math>1_B</math></td> <td>Service request is enabled</td> </tr> </table>	$0_B$	Service request is disabled	$1_B$	Service request is enabled
$0_B$	Service request is disabled						
$1_B$	Service request is enabled						

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>TOS</b>	13:11	rw	<p><b>Type of Service Control</b></p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <ul style="list-style-type: none"> <li>000<sub>B</sub> CPU0 service is initiated</li> <li>001<sub>B</sub> DMA service is initiated</li> <li>010<sub>B</sub> CPU1 service is initiated</li> <li>011<sub>B</sub> CPU2 service is initiated</li> <li>100<sub>B</sub> CPU3 service is initiated</li> <li>101<sub>B</sub> CPU4 service is initiated</li> <li>110<sub>B</sub> CPU5 service is initiated</li> <li><b>Others</b>, Reserved (no action)</li> </ul>
<b>ECC</b>	20:16	rwh	<p><b>Error Correction Code</b></p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> <li>• Write or Read-Modify-Write to SRC[31:0]</li> <li>• Write to SRC[15:0] (16-bit write)</li> <li>• Write to SRC[15:8] or write to SRC[7:0] (byte write)</li> </ul>
<b>SRR</b>	24	rh	<p><b>Service Request Flag</b></p> <p>The SRR bit shows the status of the Service Request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No service request is pending</li> <li>1<sub>B</sub> A service request is pending</li> </ul>
<b>CLRR</b>	25	w	<p><b>Request Clear Bit</b></p> <p>The CLRR bit is required to reset <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</li> </ul>
<b>SETR</b>	26	w	<p><b>Request Set Bit</b></p> <p>The SETR bit is required to set <b>SRR</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</li> </ul>
<b>IOV</b>	27	rh	<p><b>Interrupt Trigger Overflow Bit</b></p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or <b>SETR</b> bit while the SRN has still an pending service request.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No Interrupt Trigger Overflow detected</li> <li>1<sub>B</sub> Interrupt Overflow Detected.</li> </ul>
<b>IOVCLR</b>	28	w	<p><b>Interrupt Trigger Overflow Clear Bit</b></p> <p>IOVCLR is required to reset <b>IOV</b>.</p> <ul style="list-style-type: none"> <li>0<sub>B</sub> No action</li> <li>1<sub>B</sub> Clear IOV; bit value is not stored; read always returns 0.</li> </ul>

**Interrupt Router (INT)**

Field	Bits	Type	Description
<b>SWS</b>	29	rh	<p><b>SW Sticky Bit</b>            The Software Sticky Bit is set when the <b>SRR</b> bit has been set via the <b>SETR</b> bit.            This bit can be cleared by writing with 1 to <b>SWSLCR</b>.            Writing to SWS has no effect.</p> <p>0<sub>B</sub> No interrupt was initiated via SETR            1<sub>B</sub> Interrupt was initiated via SETR</p>
<b>SWSLCR</b>	30	w	<p><b>SW Sticky Clear Bit</b>            SWSLCR is required to reset <b>SWS</b>.</p> <p>0<sub>B</sub> No action            1<sub>B</sub> Clear SWS; bit value is not stored; read always returns 0.</p>
<b>0</b>	9:8, 15:14, 23:21, 31	r	<p><b>Reserved</b>            Read as 0; should be written with 0.</p>

**16.6 Revision History****Table 281 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.2.6</b>	- No functional changes	
<b>V1.2.7</b>	No functional change	
<b>V1.2.8</b>	Removed connection table.	
<b>Page 11</b>	Changed SRC.TOS register description to describe all not used TOS encodings as 'Reserved' -> added 'Others -> Reserved (no action)'.	
<b>V1.2.9</b>	No changes.	
<b>V1.2.10</b>	- No functional changes.	
<b>V1.2.11</b>		
<b>Page 5</b>	Updated bullet list item.	

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**Flexible CRC Engine (FCE)****17        Flexible CRC Engine (FCE)**

For the general description of the module and the registers, please refer to the family spec.

**17.1      TC39x-B Specific IP Configuration**

There are no device specific IP configurations.

**Flexible CRC Engine (FCE)****17.2 TC39x-B Specific Register Set****Table 282 Register Address Space - FCE**

Module	Base Address	End Address	Note
FCE	F0000000 <sub>H</sub>	F00001FF <sub>H</sub>	FPI slave interface

**Table 283 Register Overview - FCE (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FCE_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	E,SV,P	Application Reset	See Family Spec
FCE_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
FCE_CHSTS	Channels Status Register	020 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
FCE_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
FCE_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
FCE_IRi (i=0-7)	Input Register i	100 <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_RESi (i=0-7)	CRC Result Register i	104 <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
FCE_CFGi (i=0-7)	CRC Configuration Register i	108 <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	P,E,SV	Application Reset	See Family Spec
FCE_STSi (i=0-7)	CRC Status Register i	10C <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec

## Flexible CRC Engine (FCE)

**Table 283 Register Overview - FCE (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
FCE_LENGTH <i>i</i> (i=0-7)	CRC Length Register i	110 <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CHECK <i>i</i> (i=0-7)	CRC Check Register i	114 <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CRC <i>i</i> (i=0-7)	CRC Register i	118 <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CTR <i>i</i> (i=0-7)	CRC Test Register i	11C <sub>H</sub> +i*2 0 <sub>H</sub>	U,SV	P,U,SV	Application Reset	See Family Spec

## 17.3 TC39x-B Specific Registers

No deviations from the Family Spec

## 17.4 Connectivity

**Table 284 Connections of FCE**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
FCE:SRC_FCE	to	INT:fce0.SRC_FCE	FCE Service Request

## 17.5 Revision History

**Table 285 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
V4.2.9		
	No changes.	

## Direct Memory Access (DMA)

### 18 Direct Memory Access (DMA)

This is the TC39x-B specific information related to the DMA module of the AURIXTC3XX product family.

#### 18.1 TC39x-B Specific IP Configuration

The TC39x-B DMA contains 128 DMA channels.

#### 18.2 TC39x-B Specific Register Set

**Table 286 Register Address Space - DMA**

Module	Base Address	End Address	Note
DMA	F0010000 <sub>H</sub>	F0013FFF <sub>H</sub>	FPI slave interface

**Table 287 Register Overview - DMA (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_CLC	DMA Clock Control Register	0000 <sub>H</sub>	U,SV	SV,E,P00,P01	Application Reset	See Family Spec
DMA_ID	DMA Identification Register	0008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_ACCENr0 (r=0-3)	RP r Access Enable Register 0	0040 <sub>H</sub> +r*8	U,SV	SV,SE	Application Reset	See Family Spec
DMA_ACCENr1 (r=0-3)	RP r Access Enable Register 1	0044 <sub>H</sub> +r*8	U,SV	nBE	Application Reset	See Family Spec
DMA_EERm (m=0-1)	ME m Enable Error Register	0120 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
DMA_ERRSRm (m=0-1)	ME m Error Status Register	0124 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_CLREm (m=0-1)	ME m Clear Error Register	0128 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
DMA_MEmSR (m=0-1)	ME m Status Register	0130 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEm0R (m=0-1)	ME m Read Register 0	0140 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec

**Direct Memory Access (DMA)****Table 287 Register Overview - DMA (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMA_MEm1R (m=0-1)	ME m Read Register 1	0144 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEm2R (m=0-1)	ME m Read Register 2	0148 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEm3R (m=0-1)	ME m Read Register 3	014C <sub>H</sub> + m*1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEm4R (m=0-1)	ME m Read Register 4	0150 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEm5R (m=0-1)	ME m Read Register 5	0154 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEm6R (m=0-1)	ME m Read Register 6	0158 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEm7R (m=0-1)	ME m Read Register 7	015C <sub>H</sub> + m*1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEmRDCR C (m=0-1)	ME m Channel Read Data CRC Register	0180 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSDCR C (m=0-1)	ME m Channel Source and Destination Address CRC Register	0184 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSADR (m=0-1)	ME m Channel Source Address Register	0188 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEmDADR (m=0-1)	ME m Channel Destination Address Register	018C <sub>H</sub> + m*1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEmADICR (m=0-1)	ME m Channel Address and Interrupt Control Register	0190 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEmCHCR (m=0-1)	ME m Channel Control Register	0194 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSHAD R (m=0-1)	ME m Channel Shadow Address Register	0198 <sub>H</sub> +m *1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec

**Direct Memory Access (DMA)****Table 287 Register Overview - DMA (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMA_MEmCHSR (m=0-1)	ME m Channel Status Register	019C <sub>H</sub> + m*1000 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_OTSS	DMA OCDS Trigger Set Select	1200 <sub>H</sub>	U,SV	SV	See Family Spec	See Family Spec
DMA_PRR0	DMA Pattern Read Register 0	1208 <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
DMA_PRR1	DMA Pattern Read Register 1	120C <sub>H</sub>	U,SV	SV	Application Reset	See Family Spec
DMA_TIME	DMA Time Register	1210 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
DMA_MODEr (r=0-3)	RP r Mode Register	1300 <sub>H</sub> +r* 4	U,SV	SV,SE,P00, P01	Application Reset	See Family Spec
DMA_ERRINTRr (r=0-3)	RP r Error Interrupt Set Register	1320 <sub>H</sub> +r* 4	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_HRRc (c=000-127)	DMA Channel c Resource Partition Register	1800 <sub>H</sub> +c *4	U,SV	SV,SE,P00, P01	Application Reset	See Family Spec
DMA_SUSENRc (c=000-127)	DMA Channel c Suspend Enable Register	1A00 <sub>H</sub> +c *4	U,SV	SV,E,Pr	See Family Spec	See Family Spec
DMA_SUSACRc (c=000-127)	DMA Channel c Suspend Acknowledge Register	1C00 <sub>H</sub> +c *4	U,SV	BE	See Family Spec	See Family Spec
DMA_TSRC (c=000-127)	DMA Channel c Transaction State Register	1E00 <sub>H</sub> +c *4	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_RDCRCRc (c=000-127)	DMARAM Channel c Read Data CRC Register	2000 <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SDCRCRc (c=000-127)	DMARAM Channel c Source and Destination Address CRC Register	2004 <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SADRC (c=000-127)	DMARAM Channel c Source Address Register	2008 <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec

## Direct Memory Access (DMA)

**Table 287 Register Overview - DMA (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
DMA_DADRC <sub>c</sub> (c=000-127)	DMARAM Channel c Destination Address Register	200C <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_ADICRC <sub>c</sub> (c=000-127)	DMARAM Channel c Address and Interrupt Control Register	2010 <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_CHCFGRC <sub>c</sub> (c=000-127)	DMARAM Channel c Configuration Register	2014 <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SHADRC <sub>c</sub> (c=000-127)	DMARAM Channel c Shadow Address Register	2018 <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_CHCSRC <sub>c</sub> (c=000-127)	DMARAM Channel c Control and Status Register	201C <sub>H</sub> +c *20 <sub>H</sub>	U,SV	SV,Pr	Application Reset	See Family Spec

## 18.3 TC39x-B Specific Registers

No deviations from the Family Spec

## 18.4 Connectivity

**Table 288 Connections of DMA**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
DMA:fpi0_sleep_n	from	SCU:scu_syst_sleep_n	Sleep Control
DMA:ERR_INT(3:0)	to	INT:dma.ERR_INT(3:0)	DMA Error Service Request
DMA:CH_INT(127:0)	to	INT:dma.CH_INT(127:0)	DMA Channel Service Request

## 18.5 Revision History

**Table 289 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
<b>V0.1.15</b>		
-	No functional changes.	
<b>V0.1.16</b>		
-	No functional changes.	
<b>V0.1.17</b>		
-	No functional changes.	
<b>V0.1.18</b>		
-	No functional changes.	

**RESTRICTED**

**AURIX™ TC39x-B**

**NDA Required**



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**Direct Memory Access (DMA)**

## Signal Processing Unit (SPU)

### 19 Signal Processing Unit (SPU)

This is the device specific information related to the AURIX™TC39x-B version of the SPU.

#### 19.1 TC39x-B Specific IP Configuration

There is no specific configuration of the SPU for this device

#### 19.2 TC39x-B Specific Register Set

**Table 290 Register Address Space - SPU**

Module	Base Address	End Address	Note
SPU0	FA800000 <sub>H</sub>	FA8007FF <sub>H</sub>	BBB Slave Interface to the SPU Special Function Registers
(SPU0)	FAA00000 <sub>H</sub>	FAA0FFFF <sub>H</sub>	BBB Slave Interface for Accessing the SPU Config RAM
SPU1	FAC00000 <sub>H</sub>	FAC007FF <sub>H</sub>	BBB Slave Interface to the SPU Special Function Registers
(SPU1)	FAE00000 <sub>H</sub>	FAE0FFFF <sub>H</sub>	BBB Slave Interface for Accessing the SPU Config RAM

**Table 291 Register Overview - SPU0 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
SPU0_CLC	Clock Control	00000 <sub>H</sub>	See Family Spec
SPU0_MODID	Module Identification Register	00004 <sub>H</sub>	See Family Spec
SPU0_STAT	Status and Reporting	00008 <sub>H</sub>	See Family Spec
SPU0_ID_CONF	Input DMA Configuration	00030 <sub>H</sub>	See Family Spec
SPU0_ID_CONF2	Input DMA Configuration 2	00034 <sub>H</sub>	See Family Spec
SPU0_ID_RM_CONF	Input DMA Configuration: Radar Memory	00038 <sub>H</sub>	See Family Spec
SPU0_ID_RM_ILO	Inner Loop Address Offset	0003C <sub>H</sub>	See Family Spec
SPU0_ID_RM_OLO	Outer Loop Address Offset	00040 <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 291 Register Overview - SPU0 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU0_ID_RM_BLO	Bin Offset Address Configuration	00044 <sub>H</sub>	See Family Spec
SPU0_ID_RM_IOLR	Inner and Outer Loop Repeat	00048 <sub>H</sub>	See Family Spec
SPU0_ID_RM_BLR	Bin Loop Repeat	0004C <sub>H</sub>	See Family Spec
SPU0_ID_RM_ACFG0	Spare Configuration Register	00050 <sub>H</sub>	See Family Spec
SPU0_ID_RM_ACFG1	Spare Configuration Register	00054 <sub>H</sub>	See Family Spec
SPU0_PACTR	Partial-Acquisition Counter	00058 <sub>H</sub>	See Family Spec
SPU0_DPASS_CONF	Double Pass Configuration	0005C <sub>H</sub>	See Family Spec
SPU0_BEx_LDR_CON F (x=0-1)	Loader Configuration	00060 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_LDR_CON F2 (x=0-1)	Loader Configuration Extended	00064 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_Aj_ANTOF ST (j=0-3;x=0-1)	Antenna Offset	00068 <sub>H</sub> +x*40 <sub>H</sub> +j*4	See Family Spec
SPU0_BEx_UNLDR_C ONF (x=0-1)	Unloader Configuration	00078 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_UNLDR_C ONF2 (x=0-1)	Unloader Configuration 2	0007C <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_UNLDR_A CFG (x=0-1)	Spare Configuration Register	00080 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_ODP_CO NF (x=0-1)	Output Data Processor Configuration	00084 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 291 Register Overview - SPU0 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU0_BEx_NCICTRL (x=0-1)	NCI Control	00088 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_SUMCTRL (x=0-1)	Summation Unit Control	0008C <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_PWRSUM (x=0-1)	Power Summation	00090 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_PWRCTRL (x=0-1)	Power Information Channel Control	00094 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_CFARCTR L (x=0-1)	CFAR Module Control	00098 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BEx_SBCTRL (x=0-1)	Sideband Control	0009C <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU0_BINm_REJ (m=0-63)	Bin Rejection Mask	000E0 <sub>H</sub> +m*4	See Family Spec
SPU0_MAGAPPROX	Magnitude Approximation Constants	001E0 <sub>H</sub>	See Family Spec
SPU0_NCISCALAR0	NCI Antennae Scaling Factor	001E4 <sub>H</sub>	See Family Spec
SPU0_NCISCALAR1	NCI Antennae Scaling Factor	001E8 <sub>H</sub>	See Family Spec
SPU0_NCISCALAR2	NCI Antennae Scaling Factor	001EC <sub>H</sub>	See Family Spec
SPU0_NCISCALAR3	NCI Antennae Scaling Factor	001F0 <sub>H</sub>	See Family Spec
SPU0_CFARCFG	CFAR Configuration	001F4 <sub>H</sub>	See Family Spec
SPU0_CFARCFG2	CFAR Configuration 2	001F8 <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 291 Register Overview - SPU0 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU0_CFARCFG3	CFAR Configuration 3	001FC <sub>H</sub>	See Family Spec
SPU0_SCALARADD	Scalar Addition Operand	00200 <sub>H</sub>	See Family Spec
SPU0_SCALARMULT	Scalar Multiplication Operand	00204 <sub>H</sub>	See Family Spec
SPU0_BINREJCTRL	Bin Rejection Unit Control	00208 <sub>H</sub>	See Family Spec
SPU0_LCLMAX	Local Maximum Control	0020C <sub>H</sub>	See Family Spec
SPU0_ACFG2	Spare Configuration Register	00210 <sub>H</sub>	See Family Spec
SPU0_REGCRC	Register CRC	00218 <sub>H</sub>	See Family Spec
SPU0_CTRL	SPU Control	0021C <sub>H</sub>	See Family Spec
SPU0_MDq_METADATA TA (q=0-1)	Dataset Metadata	00220 <sub>H</sub> +q*88 <sub>H</sub>	See Family Spec
SPU0_MDq_BINCOU NT (q=0-1)	Bin Rejection Unit Tracking	00224 <sub>H</sub> +q*88 <sub>H</sub>	See Family Spec
SPU0_MDq_MASKm_ ACCEPT (m=0-31;q=0-1)	Bin Acceptance Mask	00228 <sub>H</sub> +q*88 <sub>H</sub> +m*4	See Family Spec
SPU0_IDMCNT	Input DMA Count	00330 <sub>H</sub>	See Family Spec
SPU0_IBMCNT	Input Buffer Memory Count	00334 <sub>H</sub>	See Family Spec
SPU0_LDRCNT	Input Buffer Memory Read Count	00338 <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 291 Register Overview - SPU0 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU0_FFTWCNT	FFT Load Count	0033C <sub>H</sub>	See Family Spec
SPU0_FFTRCNT	FFT Unload Count	00340 <sub>H</sub>	See Family Spec
SPU0_ULDRCNT	Output Buffer Memory Write Count	00344 <sub>H</sub>	See Family Spec
SPU0_ODMCNT	Output Buffer Memory Read Count	00348 <sub>H</sub>	See Family Spec
SPU0_BRCNT	Bin Rejection Unit Load Count	0034C <sub>H</sub>	See Family Spec
SPU0_CFARCNT	CFAR Unit Load Count	00350 <sub>H</sub>	See Family Spec
SPU0_ODMACNTp (p=0-7)	Output DMA Port Write Count	00354 <sub>H</sub> +p*4	See Family Spec
SPU0_CNTCLR	Safety Counter Clear	00374 <sub>H</sub>	See Family Spec
SPU0_MONITOR	SPU Monitor	00378 <sub>H</sub>	See Family Spec
SPU0_SMCTRL	Safety Mechanism Control Functions	0037C <sub>H</sub>	See Family Spec
SPU0_SMSTAT	Safety Mechanism Status	00380 <sub>H</sub>	See Family Spec
SPU0_SMUSER	Safety Mechanism Control Functions (User)	00384 <sub>H</sub>	See Family Spec
SPU0_DATAd_CRC (d=0-85)	Monitor CRC Register	00388 <sub>H</sub> +d*4	See Family Spec
SPU0_CTRLe_CRC (e=0-24)	Monitor CRC Register	00500 <sub>H</sub> +e*4	See Family Spec

## Signal Processing Unit (SPU)

**Table 291 Register Overview - SPU0 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU0_USROTC	User OCDS Trace Control	007E0 <sub>H</sub>	See Family Spec
SPU0_ACCENO	Access Enable Register 0	007E4 <sub>H</sub>	See Family Spec
SPU0_ACCEN1	Access Enable Register 1	007E8 <sub>H</sub>	See Family Spec
SPU0_OCS	OCDS Control and Status	007EC <sub>H</sub>	See Family Spec
SPU0_ODA	OCDS Debug Access Register	007F0 <sub>H</sub>	See Family Spec
SPU0_KRST0	Kernel Reset Register 0	007F4 <sub>H</sub>	See Family Spec
SPU0_KRST1	Kernel Reset Register 1	007F8 <sub>H</sub>	See Family Spec
SPU0_KRSTCLR	Kernel Reset Clear	007FC <sub>H</sub>	See Family Spec

**Table 292 Register Overview - SPU1 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
SPU1_CLC	Clock Control	00000 <sub>H</sub>	See Family Spec
SPU1_MODID	Module Identification Register	00004 <sub>H</sub>	See Family Spec
SPU1_STAT	Status and Reporting	00008 <sub>H</sub>	See Family Spec
SPU1_ID_CONF	Input DMA Configuration	00030 <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 292 Register Overview - SPU1 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU1_ID_CONF2	Input DMA Configuration 2	00034 <sub>H</sub>	See Family Spec
SPU1_ID_RM_CONF	Input DMA Configuration: Radar Memory	00038 <sub>H</sub>	See Family Spec
SPU1_ID_RM_ILO	Inner Loop Address Offset	0003C <sub>H</sub>	See Family Spec
SPU1_ID_RM_OLO	Outer Loop Address Offset	00040 <sub>H</sub>	See Family Spec
SPU1_ID_RM_BLO	Bin Offset Address Configuration	00044 <sub>H</sub>	See Family Spec
SPU1_ID_RM_IOLR	Inner and Outer Loop Repeat	00048 <sub>H</sub>	See Family Spec
SPU1_ID_RM_BLR	Bin Loop Repeat	0004C <sub>H</sub>	See Family Spec
SPU1_ID_RM_ACFG0	Spare Configuration Register	00050 <sub>H</sub>	See Family Spec
SPU1_ID_RM_ACFG1	Spare Configuration Register	00054 <sub>H</sub>	See Family Spec
SPU1_PACTR	Partial-Acquisition Counter	00058 <sub>H</sub>	See Family Spec
SPU1_DPASS_CONF	Double Pass Configuration	0005C <sub>H</sub>	See Family Spec
SPU1_BEx_LDR_CON F (x=0-1)	Loader Configuration	00060 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_LDR_CON F2 (x=0-1)	Loader Configuration Extended	00064 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_Aj_ANTOF ST (j=0-3;x=0-1)	Antenna Offset	00068 <sub>H</sub> +x*40 <sub>H</sub> +j*4	See Family Spec

## Signal Processing Unit (SPU)

**Table 292 Register Overview - SPU1 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU1_BEx_UNLDR_C ONF (x=0-1)	Unloader Configuration	00078 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_UNLDR_C ONF2 (x=0-1)	Unloader Configuration 2	0007C <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_UNLDR_A CFG (x=0-1)	Spare Configuration Register	00080 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_ODP_CO NF (x=0-1)	Output Data Processor Configuration	00084 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_NCICTRL (x=0-1)	NCI Control	00088 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_SUMCTRL (x=0-1)	Summation Unit Control	0008C <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_PWRSUM (x=0-1)	Power Summation	00090 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_PWRCTRL (x=0-1)	Power Information Channel Control	00094 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_CFARCTR L (x=0-1)	CFAR Module Control	00098 <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BEx_SBCTRL (x=0-1)	Sideband Control	0009C <sub>H</sub> +x*40 <sub>H</sub>	See Family Spec
SPU1_BINm_REJ (m=0-63)	Bin Rejection Mask	000E0 <sub>H</sub> +m*4	See Family Spec
SPU1_MAGAPPROX	Magnitude Approximation Constants	001E0 <sub>H</sub>	See Family Spec
SPU1_NCISCALAR0	NCI Antennae Scaling Factor	001E4 <sub>H</sub>	See Family Spec
SPU1_NCISCALAR1	NCI Antennae Scaling Factor	001E8 <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 292 Register Overview - SPU1 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU1_NCISCALAR2	NCI Antennae Scaling Factor	001EC <sub>H</sub>	See Family Spec
SPU1_NCISCALAR3	NCI Antennae Scaling Factor	001F0 <sub>H</sub>	See Family Spec
SPU1_CFARCFG	CFAR Configuration	001F4 <sub>H</sub>	See Family Spec
SPU1_CFARCFG2	CFAR Configuration 2	001F8 <sub>H</sub>	See Family Spec
SPU1_CFARCFG3	CFAR Configuration 3	001FC <sub>H</sub>	See Family Spec
SPU1_SCALARADD	Scalar Addition Operand	00200 <sub>H</sub>	See Family Spec
SPU1_SCALARMULT	Scalar Multiplication Operand	00204 <sub>H</sub>	See Family Spec
SPU1_BINREJCTRL	Bin Rejection Unit Control	00208 <sub>H</sub>	See Family Spec
SPU1_LCLMAX	Local Maximum Control	0020C <sub>H</sub>	See Family Spec
SPU1_ACFG2	Spare Configuration Register	00210 <sub>H</sub>	See Family Spec
SPU1_REGCRC	Register CRC	00218 <sub>H</sub>	See Family Spec
SPU1_CTRL	SPU Control	0021C <sub>H</sub>	See Family Spec
SPU1_MDq_METADA TA (q=0-1)	Dataset Metadata	00220 <sub>H</sub> +q*88 <sub>H</sub>	See Family Spec
SPU1_MDq_BINCOU NT (q=0-1)	Bin Rejection Unit Tracking	00224 <sub>H</sub> +q*88 <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 292 Register Overview - SPU1 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU1_MDq_MASKm_ACCEPT (m=0-31;q=0-1)	Bin Acceptance Mask	00228 <sub>H</sub> +q*88 <sub>H</sub> +m*4	See Family Spec
SPU1_IDMCNT	Input DMA Count	00330 <sub>H</sub>	See Family Spec
SPU1_IBMCNT	Input Buffer Memory Count	00334 <sub>H</sub>	See Family Spec
SPU1_LDRCNT	Input Buffer Memory Read Count	00338 <sub>H</sub>	See Family Spec
SPU1_FFTWCNT	FFT Load Count	0033C <sub>H</sub>	See Family Spec
SPU1_FFTRCNT	FFT Unload Count	00340 <sub>H</sub>	See Family Spec
SPU1_ULDRCNT	Output Buffer Memory Write Count	00344 <sub>H</sub>	See Family Spec
SPU1_ODMCNT	Output Buffer Memory Read Count	00348 <sub>H</sub>	See Family Spec
SPU1_BRCNT	Bin Rejection Unit Load Count	0034C <sub>H</sub>	See Family Spec
SPU1_CFARCNT	CFAR Unit Load Count	00350 <sub>H</sub>	See Family Spec
SPU1_ODMACNTp (p=0-7)	Output DMA Port Write Count	00354 <sub>H</sub> +p*4	See Family Spec
SPU1_CNTCLR	Safety Counter Clear	00374 <sub>H</sub>	See Family Spec
SPU1_MONITOR	SPU Monitor	00378 <sub>H</sub>	See Family Spec
SPU1_SMCTRL	Safety Mechanism Control Functions	0037C <sub>H</sub>	See Family Spec

## Signal Processing Unit (SPU)

**Table 292 Register Overview - SPU1 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
SPU1_SMSTAT	Safety Mechanism Status	00380 <sub>H</sub>	See Family Spec
SPU1_SMUSER	Safety Mechanism Control Functions (User)	00384 <sub>H</sub>	See Family Spec
SPU1_DATAd_CRC (d=0-85)	Monitor CRC Register	00388 <sub>H</sub> +d*4	See Family Spec
SPU1_CTRLe_CRC (e=0-24)	Monitor CRC Register	00500 <sub>H</sub> +e*4	See Family Spec
SPU1_USROTC	User OCDS Trace Control	007E0 <sub>H</sub>	See Family Spec
SPU1_ACCEN0	Access Enable Register 0	007E4 <sub>H</sub>	See Family Spec
SPU1_ACCEN1	Access Enable Register 1	007E8 <sub>H</sub>	See Family Spec
SPU1_OCS	OCDS Control and Status	007EC <sub>H</sub>	See Family Spec
SPU1_ODA	OCDS Debug Access Register	007F0 <sub>H</sub>	See Family Spec
SPU1_KRST0	Kernel Reset Register 0	007F4 <sub>H</sub>	See Family Spec
SPU1_KRST1	Kernel Reset Register 1	007F8 <sub>H</sub>	See Family Spec
SPU1_KRSTCLR	Kernel Reset Clear	007FC <sub>H</sub>	See Family Spec

### 19.3 TC39x-B Specific Registers

No deviations from the Family Spec

### 19.4 Connectivity

Connectivity of the SPUs in the AURIX™TC39x-B is as follows

## Signal Processing Unit (SPU)

**Table 293 Connections of SPU0**

Interface Signals	connects		Description
SPU0:SD	to	SPU0:SDI0	SPU Done Output
		SPU1:SDI0	
SPU0:SDI0	from	SPU0:SD	Done indication from SPU0
SPU0:SDI1	from	SPU1:SD	Done Indication from SPU1
SPU0:safety_alarm	to	SMU:safety_alarm=SMU:spu.spu0_safety_alarm.safety_alarm	SPU Alarm
SPU0:INT	to	INT:spu0.INT	SPU Service Request
SPU0:ERR		INT:spu0.ERR	

**Table 294 Connections of SPU1**

Interface Signals	connects		Description
SPU1:SD	to	SPU0:SDI1	SPU Done Output
		SPU1:SDI1	
SPU1:SDI0	from	SPU0:SD	Done indication from SPU0
SPU1:SDI1	from	SPU1:SD	Done Indication from SPU1
SPU1:safety_alarm	to	SMU:safety_alarm=SMU:spu.spu1_safety_alarm.safety_alarm	SPU Alarm
SPU1:INT	to	INT:spu1.INT	SPU Service Request
SPU1:ERR		INT:spu1.ERR	

## 19.5 Revision History

**Table 295 Revision History**

Reference	Change to Previous Version	Comment
V1.1.20		
<a href="#">Page 12</a>	Previous versions removed from revision history.	
V1.1.21		
All	Text Insets updated for new tools and source versions. All tables updated. No functional changes.	
V1.1.22		
All	Text Insets updated as part of document generation flow. All tables updated. No functional changes.	
V1.1.23		
<a href="#">Page 11</a>	<a href="#">Section 19.4</a> Tables updated to fix formatting error in interrupt connections	
V1.1.24		

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**Signal Processing Unit (SPU)****Table 295 Revision History (cont'd)**

Reference	Change to Previous Version	Comment
All	Text Insets updated as part of document generation flow. All tables updated. No functional changes.	

**V1.1.25**

All	Text Insets updated as part of document generation flow. All tables updated. No functional changes.	
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## SPU Lockstep Module (SPULCKSTP)

### 20 SPU Lockstep Module (SPULCKSTP)

This describes the TC39x specific customisations of the lockstep module for the SPU.

#### 20.1 TC39x-B Specific IP Configuration

There is no device specific customisation

#### 20.2 TC39x-B Specific Register Set

**Table 296 Register Address Space - SPULCKSTP**

Module	Base Address	End Address	Note
SPULCKSTP	FA700000 <sub>H</sub>	FA7000FF <sub>H</sub>	SPU LOCKSTEP SFR Registers

**Table 297 Register Overview - SPULCKSTP (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
SPULCKSTP_CLC	Clock Control	000 <sub>H</sub>	See Family Spec
SPULCKSTP_MODID	Module Identification Register	004 <sub>H</sub>	See Family Spec
SPULCKSTP_CTRL	SPU Lockstep Control	010 <sub>H</sub>	See Family Spec
SPULCKSTP_ERROR	Error Monitoring Register	018 <sub>H</sub>	See Family Spec
SPULCKSTP_ERRCLR	Error Clear	01C <sub>H</sub>	See Family Spec
SPULCKSTP_TEST	Alarm Test Register	020 <sub>H</sub>	See Family Spec
SPULCKSTP_SPUCTR_L	SPU Control	024 <sub>H</sub>	See Family Spec
SPULCKSTP_ACCEN0	Access Enable Register 0	0E4 <sub>H</sub>	See Family Spec
SPULCKSTP_ACCEN1	Access Enable Register 1	0E8 <sub>H</sub>	See Family Spec

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**SPU Lockstep Module (SPULCKSTP)****20.3 TC39x-B Specific Registers**

There are no registers specific to the TC39x

**20.4 Connectivity**

Empty section

**20.5 Revision History****Table 298 Revision History**

Reference	Change to Previous Version	Comment
V1.2.5		
All	No changes to previous version.	

## Extended Memory (EMEM)

### 21 Extended Memory (EMEM)

This is the TC39x-B specific information related to the EMEM module of the AURIXTC3XX product family.

#### 21.1 TC39x-B Specific IP Configuration

The TC39x-B EMEM contains 4 Mbyte of extension memory in four instances of the EMEM module.

#### 21.2 TC39x-B Specific Register Set

**Table 299 Register Address Space - EMEM**

Module	Base Address	End Address	Note
EMEM	FA006000 <sub>H</sub>	FA0060FF <sub>H</sub>	BPI SFF (access to EMEM core registers)

**Table 300 Register Address Space - EMEM\_MPU**

Module	Base Address	End Address	Note
EMEMMPU0	FB000000 <sub>H</sub>	FB00FFFF <sub>H</sub>	SRI slave interface 0 (access to EMEM module registers)
EMEMMPU1	FB010000 <sub>H</sub>	FB01FFFF <sub>H</sub>	SRI slave interface 1 (access to EMEM module registers)
EMEMMPU2	FB020000 <sub>H</sub>	FB02FFFF <sub>H</sub>	SRI slave interface 2 (access to EMEM module registers)
EMEMMPU3	FB030000 <sub>H</sub>	FB03FFFF <sub>H</sub>	SRI slave interface 3 (access to EMEM module registers)

**Table 301 Register Address Space - EMEM\_RAM**

Module	Base Address	End Address	Note
(EMEMRAM0)	99000000 <sub>H</sub>	990FFFFF <sub>H</sub>	BBB slave interface 0 (access to EMEM module RAM, cached segment)
	99000000 <sub>H</sub>	990FFFFF <sub>H</sub>	SRI slave interface 0 (access to EMEM module RAM, cached segment)
	B9000000 <sub>H</sub>	B90FFFFF <sub>H</sub>	BBB slave interface 0 (access to EMEM module RAM, non-cached segment)
	B9000000 <sub>H</sub>	B90FFFFF <sub>H</sub>	SRI slave interface 0 (access to EMEM module RAM, non-cached segment)
(EMEMRAM1)	99100000 <sub>H</sub>	991FFFFF <sub>H</sub>	BBB slave interface 1 (access to EMEM module RAM, cached segment)
	99100000 <sub>H</sub>	991FFFFF <sub>H</sub>	SRI slave interface 1 (access to EMEM module RAM, cached segment)
	B9100000 <sub>H</sub>	B91FFFFF <sub>H</sub>	BBB slave interface 1 (access to EMEM module RAM, non-cached segment)
	B9100000 <sub>H</sub>	B91FFFFF <sub>H</sub>	SRI slave interface 1 (access to EMEM module RAM, non-cached segment)
(EMEMRAM2)	99200000 <sub>H</sub>	992FFFFF <sub>H</sub>	BBB slave interface 2 (access to EMEM module RAM, cached segment)
	99200000 <sub>H</sub>	992FFFFF <sub>H</sub>	SRI slave interface 2 (access to EMEM module RAM, cached segment)

## Extended Memory (EMEM)

**Table 301 Register Address Space - EMEM\_RAM (cont'd)**

Module	Base Address	End Address	Note
	B9200000 <sub>H</sub>	B92FFFFF <sub>H</sub>	BBB slave interface 2 (access to EMEM module RAM, non-cached segment)
	B9200000 <sub>H</sub>	B92FFFFF <sub>H</sub>	SRI slave interface 2 (access to EMEM module RAM, non-cached segment)
(EMEMRAM3)	99300000 <sub>H</sub>	993FFFFF <sub>H</sub>	BBB slave interface 3 (access to EMEM module RAM, cached segment)
	99300000 <sub>H</sub>	993FFFFF <sub>H</sub>	SRI slave interface 3 (access to EMEM module RAM, cached segment)
	B9300000 <sub>H</sub>	B93FFFFF <sub>H</sub>	BBB slave interface 3 (access to EMEM module RAM, non-cached segment)
	B9300000 <sub>H</sub>	B93FFFFF <sub>H</sub>	SRI slave interface 3 (access to EMEM module RAM, non-cached segment)

**Table 302 Register Address Space - XTM**

Module	Base Address	End Address	Note
(XTM)	B9400000 <sub>H</sub>	B947FFFF <sub>H</sub>	XTM FPI slave interface

**Table 303 Register Overview - EMEM (ascending Offset Address)**

Short Name	Description	Offset Address	Access Mode		Page Number
			Read	Write	
EMEM_CLC	EMEM Core Clock Control Register	0000 <sub>H</sub>	U,SV	SV,E,P	See Family Spec
EMEM_ID	EMEM Core Module Identification Register	0008 <sub>H</sub>	U,SV	BE	See Family Spec
EMEM_TILECONFIG	EMEM Core Tile Configuration Register	0020 <sub>H</sub>	U,SV	U,SV,P	See Family Spec
EMEM_TILECC	EMEM Core Tile Control Common Memory Register	0024 <sub>H</sub>	U,SV	U,SV,P	See Family Spec
EMEM_TILECT	EMEM Core Tile Control Trace Memory Register	0028 <sub>H</sub>	U,SV	U,SV,P	See Family Spec
EMEM_TILESTA	EMEM Core Tile Status Register	002C <sub>H</sub>	U,SV	BE	See Family Spec
EMEM_SBRCTR	EMEM Core Standby RAM Control Register	0034 <sub>H</sub>	U,SV	U,SV,P	See Family Spec

**Extended Memory (EMEM)****Table 303 Register Overview - EMEM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Description</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Page Number</b>
			<b>Read</b>	<b>Write</b>	
EMEM_ACCEN1	EMEM Core Access Enable Register 1	00F8 <sub>H</sub>	U,SV	BE	See Family Spec
EMEM_ACCENO	EMEM Core Access Enable Register 0	00FC <sub>H</sub>	U,SV	SV,SE	See Family Spec

**Table 304 Register Overview - EMEMMPU0 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU0_CLC	EMEM Module Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU0_MO DID	EMEM Module ID Register	00008 <sub>H</sub>	SV	R	Application Reset	See Family Spec
EMEMMPU0_ACC EN0	EMEM Module Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU0_ACC EN1	EMEM Module Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU0_ME MCON	EMEM Module Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU0_SCT RL	EMEM Module Safety Control Register	00024 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGN LAi (i=0-7)	EMEM Module Region i Lower Address Register	00050 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGN UAi (i=0-7)	EMEM Module Region i Upper Address Register	00054 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGN ACCENWAI (i=0-7)	EMEM Module Region i Write Access Enable Register 0	00058 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGN ACCENWBi (i=0-7)	EMEM Module Region i Write Access Enable Register 1	0005C <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Extended Memory (EMEM)****Table 304 Register Overview - EMEMMPU0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU0_RGN ACCENRAi (i=0-7)	EMEM Module Region i Read Access Enable Register 0	000D8 <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGN ACCENRBi (i=0-7)	EMEM Module Region i Read Access Enable Register 1	000DC <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Table 305 Register Overview - EMEMMPU1 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU1_CLC	EMEM Module Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU1_MO DID	EMEM Module ID Register	00008 <sub>H</sub>	SV	R	Application Reset	See Family Spec
EMEMMPU1_ACC ENO	EMEM Module Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU1_ACC EN1	EMEM Module Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU1_ME MCON	EMEM Module Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU1_SCT RL	EMEM Module Safety Control Register	00024 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU1_RGN LAi (i=0-7)	EMEM Module Region i Lower Address Register	00050 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU1_RGN UAi (i=0-7)	EMEM Module Region i Upper Address Register	00054 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU1_RGN ACCENWAi (i=0-7)	EMEM Module Region i Write Access Enable Register 0	00058 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU1_RGN ACCENWBi (i=0-7)	EMEM Module Region i Write Access Enable Register 1	0005C <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Extended Memory (EMEM)****Table 305 Register Overview - EMEMMPU1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU1_RGN ACCENRAi (i=0-7)	EMEM Module Region i Read Access Enable Register 0	000D8 <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU1_RGN ACCENRBi (i=0-7)	EMEM Module Region i Read Access Enable Register 1	000DC <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Table 306 Register Overview - EMEMMPU2 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU2_CLC	EMEM Module Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU2_MO DID	EMEM Module ID Register	00008 <sub>H</sub>	SV	R	Application Reset	See Family Spec
EMEMMPU2_ACC ENO	EMEM Module Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU2_ACC EN1	EMEM Module Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU2_ME MCON	EMEM Module Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU2_SCT RL	EMEM Module Safety Control Register	00024 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU2_RGN LAi (i=0-7)	EMEM Module Region i Lower Address Register	00050 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU2_RGN UAi (i=0-7)	EMEM Module Region i Upper Address Register	00054 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU2_RGN ACCENWAi (i=0-7)	EMEM Module Region i Write Access Enable Register 0	00058 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU2_RGN ACCENWBi (i=0-7)	EMEM Module Region i Write Access Enable Register 1	0005C <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Extended Memory (EMEM)****Table 306 Register Overview - EMEMMPU2 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU2_RGN ACCENRAi (i=0-7)	EMEM Module Region i Read Access Enable Register 0	000D8 <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU2_RGN ACCENRBi (i=0-7)	EMEM Module Region i Read Access Enable Register 1	000DC <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

**Table 307 Register Overview - EMEMMPU3 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU3_CLC	EMEM Module Clock Control Register	00000 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU3_MO DID	EMEM Module ID Register	00008 <sub>H</sub>	SV	R	Application Reset	See Family Spec
EMEMMPU3_ACC ENO	EMEM Module Access Enable Register 0	00010 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU3_ACC EN1	EMEM Module Access Enable Register 1	00014 <sub>H</sub>	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU3_ME MCON	EMEM Module Memory Control Register	00020 <sub>H</sub>	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU3_SCT RL	EMEM Module Safety Control Register	00024 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU3_RGN LAi (i=0-7)	EMEM Module Region i Lower Address Register	00050 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU3_RGN UAi (i=0-7)	EMEM Module Region i Upper Address Register	00054 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU3_RGN ACCENWAi (i=0-7)	EMEM Module Region i Write Access Enable Register 0	00058 <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU3_RGN ACCENWBi (i=0-7)	EMEM Module Region i Write Access Enable Register 1	0005C <sub>H</sub> +i *10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

## Extended Memory (EMEM)

**Table 307 Register Overview - EMEMMPU3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EMEMMPU3_RGN ACCENRAi (i=0-7)	EMEM Module Region i Read Access Enable Register 0	000D8 <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU3_RGN ACCENRBi (i=0-7)	EMEM Module Region i Read Access Enable Register 1	000DC <sub>H</sub> + i*10 <sub>H</sub>	SV	SV,SE,P	Application Reset	See Family Spec

### 21.3 TC39x-B Specific Registers

There are no TC39x-B specific registers in the EMEM.

### 21.4 Connectivity

Nothing included at this release

### 21.5 Revision History

**Table 308 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
V1.3.12		Updated to align with EMEM_AURIXTC3XX V1.3.12 specification chapter.
V1.3.13	No changes.	
V1.3.14	No changes.	
V1.4.1	Page 2	Add extra registers TILESTATE1 and TILECONFIG1 to support increased memory size.
V1.4.2	-	No functional changes.
V1.4.3	-	No functional changes.
V1.4.4	-	No functional changes.

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**Radar Interface (RIF)**

## 22 Radar Interface (RIF)

This chapter describes the Radar Interface (RIF) module of the TC39x-B.

### 22.1 TC39x-B Specific IP Configuration

See features in the family spec.

**Table 309 TC39x-B specific configuration of RIF**

Parameter	RIFO	RIF1
<b>Software Triggered Reset of the Module Kernel</b> This reset does not affect the bus interfaces and therefore cannot cause a protocol violation. Other outputs are synchronously forced to the idle state	Kernel Reset (software controlled by KRST0-1 registers)	Kernel Reset (software controlled by KRST0-1 registers)

### 22.2 TC39x-B Specific Register Set

#### 22.2.1 Address Map

**Table 310 Register Address Space - RIF**

Module	Base Address	End Address	Note
RIFO	FA040000 <sub>H</sub>	FA0401FF <sub>H</sub>	FPI slave interface
RIF1	FA040200 <sub>H</sub>	FA0403FF <sub>H</sub>	FPI slave interface

*Note:* The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

### 22.3 TC39x-B Specific Registers

No deviations from the Family Spec

### 22.4 Connectivity

**Table 311 Connections of RIFO**

Interface Signals	connects		Description
RIFO:RAMP1B	from	P02.6:IN	External RAMP B input
RIFO:safety_alarm	to	SMU:rif0_safety_alarm	RIF Alarm
RIFO:ERR	to	INT:rif0.ERR	Radar Interface Service Request
RIFO:INT		INT:rif0.INT	

**Radar Interface (RIF)****Table 312 Connections of RIF0**

Interface Signals	connects		Description
RIF0:CLKN	from	TC39x-B:P50.4	LVDS RX Input (inverted Serial Clock)
RIF0:CLKP	from	TC39x-B:P50.5	LVDS RX Input (Serial Clock)
RIF0:D1N	from	TC39x-B:P50.0	LVDS RX Input (inverted Data Bits of Channel #0)
RIF0:D2N	from	TC39x-B:P50.2	LVDS RX Input (inverted Data Bits of Channel #1)
RIF0:D3N	from	TC39x-B:P50.8	LVDS RX Input (inverted Data Bits of Channel #2)
RIF0:D4N	from	TC39x-B:P50.10	LVDS RX Input (inverted Data Bits of Channel #3)
RIF0:D1P	from	TC39x-B:P50.1	LVDS RX Input (Data Bits of Channel #0)
RIF0:D2P	from	TC39x-B:P50.3	LVDS RX Input (Data Bits of Channel #1)
RIF0:D3P	from	TC39x-B:P50.9	LVDS RX Input (Data Bits of Channel #2)
RIF0:D4P	from	TC39x-B:P50.11	LVDS RX Input (Data Bits of Channel #3)
RIF0:FRN	from	TC39x-B:P50.6	LVDS RX Input (inverted FrameClock)
RIF0:FRP	from	TC39x-B:P50.7	LVDS RX Input (FrameClock)

**Table 313 Connections of RIF1**

Interface Signals	connects		Description
RIF1:RAMP1B	from	P10.8:IN	External RAMP B input
RIF1:safety_alarm	to	SMU:rif1_safety_alarm	RIF Alarm
RIF1:ERR	to	INT:rif1.ERR	Radar Interface Service Request
RIF1:INT		INT:rif1.INT	

**Table 314 Connections of RIF1**

Interface Signals	connects		Description
RIF1:CLKN	from	TC39x-B:P51.4	LVDS RX Input (inverted Serial Clock)
RIF1:CLKP	from	TC39x-B:P51.5	LVDS RX Input (Serial Clock)
RIF1:D1N	from	TC39x-B:P51.0	LVDS RX Input (inverted Data Bits of Channel #0)
RIF1:D2N	from	TC39x-B:P51.2	LVDS RX Input (inverted Data Bits of Channel #1)
RIF1:D3N	from	TC39x-B:P51.8	LVDS RX Input (inverted Data Bits of Channel #2)
RIF1:D4N	from	TC39x-B:P51.10	LVDS RX Input (inverted Data Bits of Channel #3)
RIF1:D1P	from	TC39x-B:P51.1	LVDS RX Input (Data Bits of Channel #0)
RIF1:D2P	from	TC39x-B:P51.3	LVDS RX Input (Data Bits of Channel #1)
RIF1:D3P	from	TC39x-B:P51.9	LVDS RX Input (Data Bits of Channel #2)

**Radar Interface (RIF)****Table 314 Connections of RIF1 (cont'd)**

Interface Signals	connects		Description
RIF1:D4P	from	TC39x-B:P51.11	LVDS RX Input (Data Bits of Channel #3)
RIF1:FRN	from	TC39x-B:P51.6	LVDS RX Input (inverted FrameClock)
RIF1:FRP	from	TC39x-B:P51.7	LVDS RX Input (FrameClock)

**22.5 Revision History****Table 315 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.0.36</b>		
All	Register and Connectivity Tables updated	
<b>V1.0.37</b>		
-	No functional changes.	-
<b>V1.0.38</b>		
-	No functional changes.	-
<b>V1.0.39</b>		
-	Device specific registers (RIF0_FLM, RIF1_FLM, RIF0_INTCON, RIF1_INTCON, RIF0_FLAGSSET, RIF1_FLAGSSET) are moved from the family spec to the appendix. No functional changes.	-
<b>V1.0.40</b>		
-	For registers from ESI to REGCRC, Kernel reset values are added for clarification.	
-	Device specific registers, RIF0_FLAGSCL and RIF1_FLAGSCL are moved from the family spec to the appendix.	
-	Device specific registers (RIF0_DBGDLY0, RIF1_DBGDLY0, RIF0_DBGDLY1, RIF1_DBGDLY1) are moved from the family spec to the appendix.	
-	Device specific registers, RIF0_ESI and RIF1_ESI are moved from the family spec to the appendix.	
-	No functional changes.	-
<b>V1.0.41</b>		
-	No functional changes.	-
<b>V1.0.42</b>		
-	No functional changes.	-
<b>V1.0.43</b>		
-	References to TC3Ax are removed	

## High Speed Pulse Density Modulation Module (HSPDM)

### 23 High Speed Pulse Density Modulation Module (HSPDM)

Text with reference to family spec.

#### 23.1 TC39x-B Specific IP Configuration

See features in the family spec.

**Table 316 TC39x-B specific configuration of HSPDM**

Parameter	HSPDM
HSPDM ram	F0280000 <sub>H</sub>
HSPDM ram size	2000 <sub>H</sub>
HSPDM BPI registers	F0282000 <sub>H</sub>
HSPDM BPI registers size	100 <sub>H</sub>
SRAM size in byte	8192

#### 23.2 TC39x-B Specific Register Set

There are no specific register set.

##### 23.2.1 Address Map

**Table 317 Register Address Space - HSPDM**

Module	Base Address	End Address	Note
(HSPDM)	F0280000 <sub>H</sub>	F0281FFF <sub>H</sub>	FPI slave interface for SRAM access
HSPDM	F0282000 <sub>H</sub>	F02820FF <sub>H</sub>	FPI slave interface for BPI registers access

*Note:* The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

HSPDM RAM takes 8KBytes address space starting from 0xF028 0000 to 0xF028 1FFF.

#### 23.3 TC39x-B Specific Registers

There are no device specific registers for HSPDM in TC39x-B.

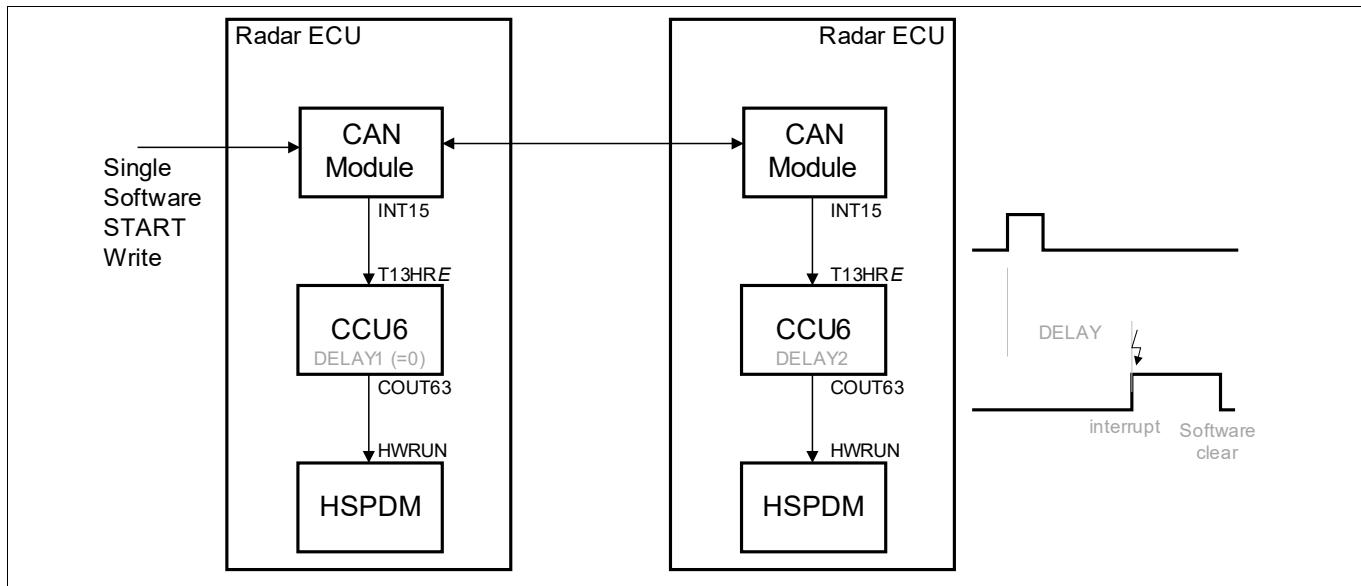
#### 23.4 Connectivity

There will be connections to the VADC.

##### 23.4.1 Connections Regarding Hardware Run Feature

HSPDM module can be started by a CAN message. The reception (or transmission) of CAN message can trigger an interrupt. The interrupt signal can be delayed by a CCU6 timer module for a programmable time interval. The delayed interrupt signal can be used for starting the HSPDM module.

## High Speed Pulse Density Modulation Module (HSPDM)



**Figure 8** Hardware Run Connections

### 23.4.2 Pinning and Layout

The output signals of the HSPDM module are connected to the following pads:

- P22.3 - MUTE
- P22.4 - BS0
- P22.5 - BS1

## 23.5 Revision History

**Table 318** Revision History

Reference	Change to Previous Version	Comment
V0.7.8	No change in appendix	
Page 2	Typo “Histroy” fixed.	

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**Camera and ADC Interface (CIF)****24      Camera and ADC Interface (CIF)**

This device doesn't contain a CIF module.

## System Timer (STM)

# 25 System Timer (STM)

This chapter describes the device specific details in TC39x-B.

## 25.1 TC39x-B Specific IP Configuration

See features in family spec

## 25.2 TC39x-B Specific Register Set

### Register Address Space Table

The address space for the module registers is defined below

**Table 319 Register Address Space - STM**

Module	Base Address	End Address	Note
STM0	F0001000 <sub>H</sub>	F00010FF <sub>H</sub>	FPI slave interface
STM1	F0001100 <sub>H</sub>	F00011FF <sub>H</sub>	FPI slave interface
STM2	F0001200 <sub>H</sub>	F00012FF <sub>H</sub>	FPI slave interface
STM3	F0001300 <sub>H</sub>	F00013FF <sub>H</sub>	FPI slave interface
STM4	F0001400 <sub>H</sub>	F00014FF <sub>H</sub>	FPI slave interface
STM5	F0001500 <sub>H</sub>	F00015FF <sub>H</sub>	FPI slave interface

### Register Overview Table

There are no product specific register for this module.

## 25.3 TC39x-B Specific Registers

There are no product specific register for this module.

## 25.4 Connectivity

The tables below list all the connections of STM instances.

**Table 320 Connections of STM0**

Interface Signals	connects			Description
STM0:SR0_INT	to	CAN0:STM0.SR0_INT		System Timer Service Request 0
		CAN1:STM0.SR0_INT		
		CAN2:STM0.SR0_INT		
		INT:stm0.SR0_INT		
STM0:SR1_INT	to	CAN0:STM0.SR1_INT		System Timer Service Request 1
		CAN1:STM0.SR1_INT		
		CAN2:STM0.SR1_INT		
		INT:stm0.SR1_INT		

**System Timer (STM)****Table 321 Connections of STM1**

<b>Interface Signals</b>	<b>connects</b>			<b>Description</b>
STM1:SR0_INT	to	CAN0:STM1.SR0_INT		System Timer Service Request 0
		CAN1:STM1.SR0_INT		
		CAN2:STM1.SR0_INT		
		INT:stm1.SR0_INT		
STM1:SR1_INT	to	CAN0:STM1.SR1_INT		System Timer Service Request 1
		CAN1:STM1.SR1_INT		
		CAN2:STM1.SR1_INT		
		INT:stm1.SR1_INT		

**Table 322 Connections of STM2**

<b>Interface Signals</b>	<b>connects</b>			<b>Description</b>
STM2:SR0_INT	to	CAN0:STM2.SR0_INT		System Timer Service Request 0
		CAN1:STM2.SR0_INT		
		CAN2:STM2.SR0_INT		
		INT:stm2.SR0_INT		
STM2:SR1_INT	to	CAN0:STM2.SR1_INT		System Timer Service Request 1
		CAN1:STM2.SR1_INT		
		CAN2:STM2.SR1_INT		
		INT:stm2.SR1_INT		

**Table 323 Connections of STM3**

<b>Interface Signals</b>	<b>connects</b>			<b>Description</b>
STM3:SR0_INT	to	INT:stm3.SR0_INT		System Timer Service Request 0
STM3:SR1_INT	to	INT:stm3.SR1_INT		System Timer Service Request 1

**Table 324 Connections of STM4**

<b>Interface Signals</b>	<b>connects</b>			<b>Description</b>
STM4:SR0_INT	to	INT:stm4.SR0_INT		System Timer Service Request 0
STM4:SR1_INT	to	INT:stm4.SR1_INT		System Timer Service Request 1

**Table 325 Connections of STM5**

<b>Interface Signals</b>	<b>connects</b>			<b>Description</b>
STM5:SR0_INT	to	INT:stm5.SR0_INT		System Timer Service Request 0
STM5:SR1_INT	to	INT:stm5.SR1_INT		System Timer Service Request 1

---

**System Timer (STM)****25.5 Revision History****Table 326 Revision History**

Reference	Change to Previous Version	Comment
V9.2.3		
<a href="#">Page 1</a>	Connection tables updated.	
V9.2.4		
-	No changes.	

## Generic Timer Module (GTM)

### 26 Generic Timer Module (GTM)

The following chapter describes the specific TC39x GTM configuration. For the GTM IP functionalities, please refer to the Family specification.

#### 26.1 TC39x Specific IP Configuration

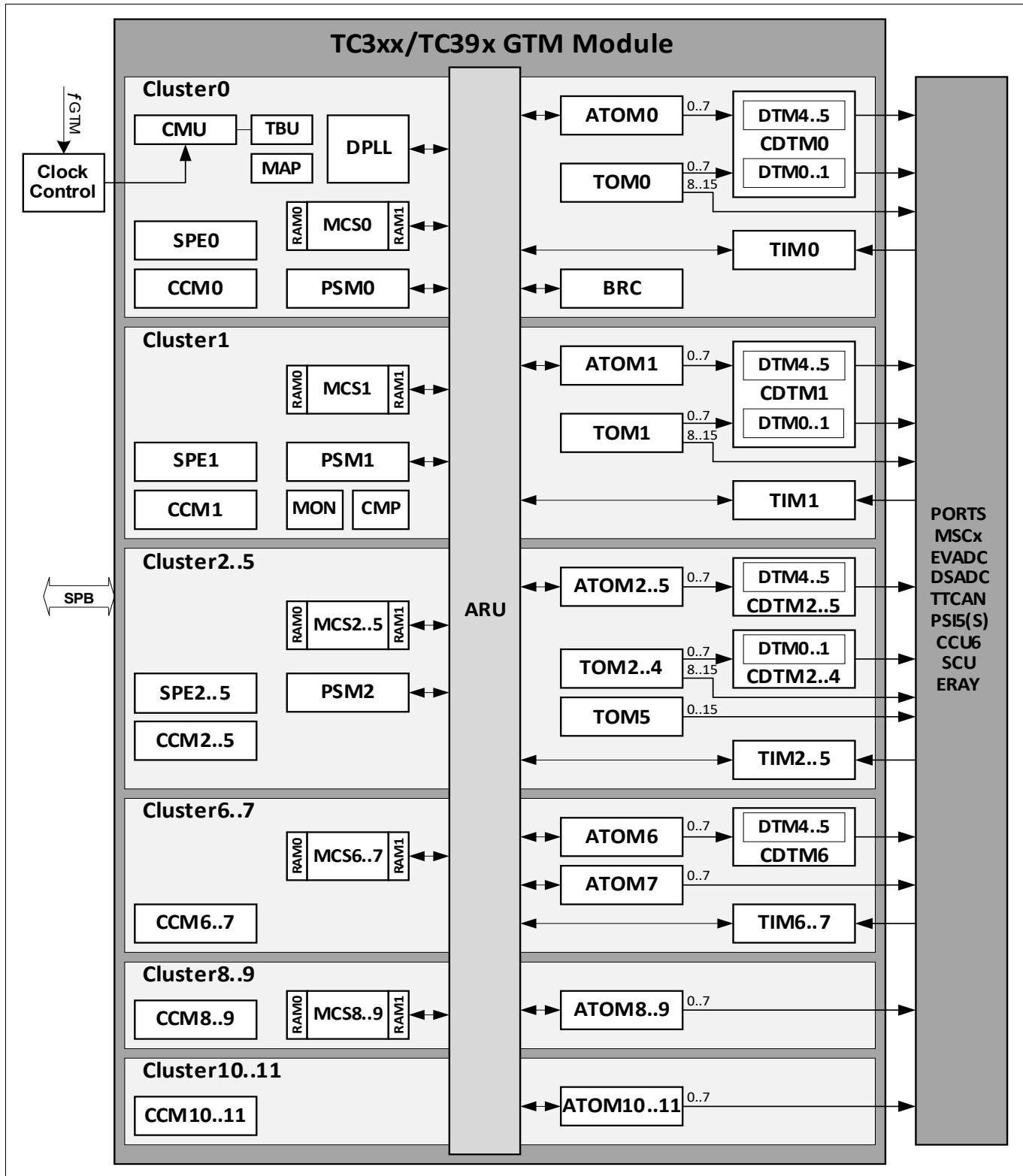


Figure 9 GTM IP Block Diagram (TC39x)

**Generic Timer Module (GTM)****Table 327 GTM Configuration by AURIX TC39x Product**

GTM Modules	TC39x
TIM	8x8 ch. (TIM0-7)
TOM	6x16 ch. (TOM0-5)
ATOM	12x8 ch. (ATOM0-11)
DTM/CDTM	5x4 ch., 2x2 ch./7xCDTM
MCS	10x8 ch. (MCS0-9)
SPE	6 (SPE0-5)
PSM	3 (PSM0-2)
DPLL	1
TBU	4 (TBU0-3)
BRC	1
MON	1
CMP	1
GTM Clusters (max speed)	12 (CCM0-11) CCM0-4: 200 MHz max CCM5-11: 100 MHz max
ARU Latency (round robin)	128x10ns => 1280ns @100MHz, (ARU_CADDR_END= 127)

**Table 328 CDTM Connections by AURIX TC39x Product**

TC39x GTM (A)TOM Modules	CDTM
TOM0_CH0..CH3	CDTM0_DTM0
TOM0_CH4..CH7	CDTM0_DTM1
TOM1_CH0..CH3	CDTM1_DTM0
TOM1_CH4..CH7	CDTM1_DTM1
TOM2_CH0..CH3	CDTM2_DTM0
TOM2_CH4..CH7	CDTM2_DTM1
TOM3_CH0..CH3	CDTM3_DTM0
TOM3_CH4..CH7	CDTM3_DTM1
TOM4_CH0..CH3	CDTM4_DTM0
TOM4_CH4..CH7	CDTM4_DTM1
ATOM0_CH0..CH3	CDTM0_DTM4
ATOM0_CH4..CH7	CDTM0_DTM5
ATOM1_CH0..CH3	CDTM1_DTM4
ATOM1_CH4..CH7	CDTM1_DTM5
ATOM2_CH0..CH3	CDTM2_DTM4
ATOM2_CH4..CH7	CDTM2_DTM5

**Generic Timer Module (GTM)****Table 328 CDTM Connections by AURIX TC39x Product (cont'd)**

TC39x GTM (A)TOM Modules	CDTM
ATOM3_CH0..CH3	CDTM3_DTM4
ATOM3_CH4..CH7	CDTM3_DTM5
ATOM4_CH0..CH3	CDTM4_DTM4
ATOM4_CH4..CH7	CDTM4_DTM5
ATOM5_CH0..CH3	CDTM5_DTM4
ATOM5_CH4..CH7	CDTM5_DTM5
ATOM6_CH0..CH3	CDTM6_DTM4
ATOM6_CH4..CH7	CDTM6_DTM5
Total DTM Channels	24

**Table 329 TC39x-B specific configuration of GTM**

Parameter	GTM
<b>Number of MCS modules</b>	10
<b>Number of DPLL modules</b>	1
<b>Number of PSM modules</b>	3
<b>Number of TIM modules</b>	8
<b>Number of ATOM DTM modules</b>	7
<b>Number of TOM DTM modules</b>	5
<b>Number of DSADC channels</b>	14
<b>Number of primary EVADC groups</b>	8
<b>Number of secondary EVADC groups</b>	4
<b>Number of MOSEL controlled trigger outputs</b>	4
<b>Number of TOUT signals</b>	272
<b>Number of SCU trigger outputs</b>	4
<b>Number of CAN modules</b>	3
<b>Number of MCS SET signals</b>	9
<b>Number of Fast Compare Channels of EVADC</b>	8
<b>Number of MSC modules</b>	4
<b>Number of DSADCINSEL registers</b>	6
<b>Number of PSI5/PSI5S modules</b>	1
<b>Number of EDSADC modules</b>	1
<b>Channel 3 of TBU is not available.</b>	0
<b>Number of CCM modules</b>	12
<b>Indicate cluster with high clock frequency</b>	1,1,1,1,0,0,0,0,0,0
<b>Number of ARU modules</b>	1
<b>Number of ATOM modules</b>	12
<b>Number of BRC modules</b>	1
<b>Number of TOM modules</b>	6

**Generic Timer Module (GTM)****Table 329 TC39x-B specific configuration of GTM (cont'd)**

Parameter	GTM
<b>Number of SPE modules</b>	6
<b>Number of CMP modules</b>	1
<b>Number of MON modules</b>	1
<b>Number of Address range protectors per CCM</b>	10
<b>Number of CDTM modules</b>	7
<b>List of DTM instances available within CDTM instance</b>	(0,1,4,5),(0,1,4,5),(0,1,4,5),(0,1,4,5),(0,1,4,5),(4,5),(4,5)
<b>Number of MAP modules</b>	1
<b>Number of MCS channel in MCS module instance</b>	8,8,8,8,8,8,8,8
<b>Number of MCFG modules</b>	1
<b>List element 1 of MCS</b>	8
<b>List element 2 of MCS</b>	8
<b>List element 3 of MCS</b>	8
<b>List element 4 of MCS</b>	8
<b>List element 5 of MCS</b>	8
<b>List element 6 of MCS</b>	8
<b>List element 7 of MCS</b>	8
<b>List element 8 of MCS</b>	8
<b>List element 9 of MCS</b>	8
<b>List element 10 of MCS</b>	8
<b>Number of Interrupt Groups for registers</b>	3
<b>ICM IRQG_CLS_k_MEI</b>	
<b>CCM0_CFG Reset Value</b>	131199
<b>CCM1_CFG Reset Value</b>	131279
<b>CCM2_CFG Reset Value</b>	131151
<b>CCM3_CFG Reset Value</b>	131087
<b>CCM4_CFG Reset Value</b>	131087
<b>CCM5_CFG Reset Value</b>	131087
<b>CCM6_CFG Reset Value</b>	131085
<b>CCM7_CFG Reset Value</b>	131085
<b>CCM8_CFG Reset Value</b>	131084
<b>CCM9_CFG Reset Value</b>	131084
<b>CCM10_CFG Reset Value</b>	131076
<b>CCM11_CFG Reset Value</b>	131076
<b>Fast Clock in Cluster 0</b>	1
<b>Fast Clock in Cluster 9</b>	0
<b>Fast Clock in Cluster 10</b>	0
<b>Fast Clock in Cluster 11</b>	0

**Generic Timer Module (GTM)****Table 329 TC39x-B specific configuration of GTM (cont'd)**

Parameter	GTM
<b>Fast Clock in Cluster 1</b>	1
<b>Fast Clock in Cluster 2</b>	1
<b>Fast Clock in Cluster 3</b>	1
<b>Fast Clock in Cluster 4</b>	1
<b>Fast Clock in Cluster 5</b>	0
<b>Fast Clock in Cluster 6</b>	0
<b>Fast Clock in Cluster 7</b>	0
<b>Fast Clock in Cluster 8</b>	0

**Generic Timer Module (GTM)****26.2 TC39x-B Specific Registers Set****Table 330 Register Address Space - GTM**

Module	Base Address	End Address	Note
GTM	F0100000 <sub>H</sub>	F01FFFFF <sub>H</sub>	FPI slave interface

**Register Overview Tables of GTM****Table 331 Register Overview - GTM (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_REV	GTM Version Control Register	000000 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_RST	GTM Global Reset Register	000004 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CTRL	GTM Global Control Register	000008 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_AEI_ADDR_XPT	GTM AEI Timeout Exception Address Register	00000C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_IRQ_NOTIF_Y	GTM Interrupt Notification Register	000010 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_IRQ_EN	GTM Interrupt Enable Register	000014 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_IRQ_FORCI_NT	GTM Software Interrupt Generation Register	000018 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_IRQ_MODE	GTM Top Level Interrupts Mode Selection Register	00001C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_EIRQ_EN	GTM Error Interrupt Enable Register	000020 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_HW_CONF	GTM Hardware Configuration Register	000024 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_CFG	GTM Configuration Register	000028 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_AEI_STA_XPT	GTM AEI Non Zero Status Register	00002C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_BRIDGE_MODE	GTM AEI Bridge Mode Register	000030 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRIDGE_PTR1	GTM AEI Bridge Pointer 1 Register	000034 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_BRIDGE_PTR2	GTM AEI Bridge Pointer 2 Register	000038 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_MCS_AEM_DIS	GTM MCS Master Port Disable Register	00003C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_AUX_IN_SRC(i=0-6)	GTM TIM i Module AUX_IN Source Selection Register	000040 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_EXT_CAP_EN_i(i=0-7)	GTM External Capture Trigger Enable i	00005C <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_OUT(i=0-5)	GTM TOM i Output Level	000080 <sub>H</sub> +i*4	U,SV,32		Application Reset	See Family Spec
GTM_ATOM0_OUT	GTM ATOM 0 Output Level	000098 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ATOM2_OUT	GTM ATOM 2 Output Level	00009C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ATOM4_OUT	GTM ATOM 4 Output Level	0000A0 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ATOM6_OUT	GTM ATOM 6 Output Level	0000A4 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ATOM8_OUT	GTM ATOM 8 Output Level	0000A8 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ATOM10_OUT	GTM ATOM 10 Output Level	0000AC <sub>H</sub>	U,SV,32		Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_CLS_CLK_CFG	GTM Cluster Clock Configuration	0000B0 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CHEN	TBU Global Channel Enable	000100 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH0_CTRL	TBU Channel 0 Control Register	000104 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH0_BASE	TBU Channel 0 Base Register	000108 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH1_CTRL	TBU Channel 1 Control Register	00010C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH1_BASE	TBU Channel 1 Base Register	000110 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH2_CTRL	TBU Channel 2 Control Register	000114 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH2_BASE	TBU Channel 2 Base Register	000118 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_CTRL	TBU Channel 3 Control Register	00011C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_BASE	TBU Channel 3 Base Register	000120 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_BASE_MARK	TBU Channel 3 Modulo Value Register	000124 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_BASE_CAPTURE	TBU Channel 3 Base Captured Register	000128 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_MON_STATUS	Monitor Status Register	000180 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MON_ACTIVITY_0	Monitor Activity Register 0	000184 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_MON_ACTIVITY_1	Monitor Activity Register 1	000188 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MON_ACTIVITY_MCSz (z=0-9)	Monitor Activity Register for MCS z	00018C <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_EN	CMP Comparator Enable Register	000200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_IRQ_NOTIFY	CMP Event Notification Register	000204 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_IRQ_EN	CMP Interrupt Enable Register	000208 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_IRQ_FORCINT	CMP Interrupt Force Register	00020C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_IRQ_MODE	CMP Interrupt Mode Configuration Register	000210 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_EIRQ_EN	CMP error interrupt enable register	000214 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_ACCESS	ARU Access Register	000280 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DATA_H	ARU Access Register Upper Data Word	000284 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DATA_L	ARU Access Register Lower Data Word	000288 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DBG_ACCESS0	ARU Debug Access Channel 0	00028C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DBG_DATA0_H	ARU Debug Access 0 Transfer Register Upper Data Word	000290 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ARU_DBG_DATA0_L	ARU Debug Access 0 Transfer Register Lower Data Word	000294 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_ARU_DBG_ACCESS1	ARU Debug Access Channel 1	000298 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DBG_DATA1_H	ARU Debug Access 1 Transfer Register Upper Data Word	00029C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ARU_DBG_DATA1_L	ARU Debug Access 1 Transfer Register Lower Data Word	0002A0 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ARU_IRQ_NOTIFY	ARU Interrupt Notification Register	0002A4 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_IRQ_EN	ARU Interrupt Enable Register	0002A8 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_IRQ_FORCINT	ARU Force Interrupt Register	0002AC <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_IRQ_MODE	ARU Interrupt Mode Register	0002B0 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_CADDR_END	ARU caddr Counter End Value Register	0002B4 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_CTRL	ARU Enable Dynamic Routing Register	0002BC <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN_CTRL (z=0-1)	ARU z Dynamic Routing Control Register	0002C0 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN_ROUTE_LOW (z=0-1)	ARU z Lower Bits of DYN_ROUTE Register	0002C8 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN_ROUTE_HIGH (z=0-1)	ARU z Higher Bits of DYN_ROUTE Register	0002D0 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN_ROUTE_SR_LOW (z=0-1)	ARU z Shadow Register for ARU_z_DYN_ROUTE_LOW	0002D8 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ARU_z_DYN_ROUTE_SR_HIGH (z=0-1)	ARU z Shadow Register for ARU_z_DYN_ROUTE_HIGH	0002E0 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN_RDADDR (z=0-1)	ARU z Read ID for Dynamic Routing	0002E8 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_CADDR	ARU caddr Counter Value	0002FC <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_CMU_CLK_EN	CMU Clock Enable Register	000300 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_GCLK_NUM	CMU Global Clock Control Numerator	000304 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_GCLK_DEN	CMU Global Clock Control Denominator	000308 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_CLK_z_CTRL (z=0-7)	CMU Control for Clock Source z	00030C <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	48
GTM_CMU_ECLK_z_NUM (z=0-2)	CMU External Clock z Control Numerator	00032C <sub>H</sub> +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_ECLK_z_DEN (z=0-2)	CMU External Clock z Control Denominator	000330 <sub>H</sub> +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_FXCLK_K_CTRL	CMU Control FXCLK Sub-Unit Input Clock	000344 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_GLB_CTRL	CMU Synchronizing ARU and Clock Source	000348 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_CLK_CTRL	CMU Control for Clock Source Selection	00034C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_SRC_z_ADDR (z=0-11)	BRC Read Address for Input Channel z	000400 <sub>H</sub> +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_SRC_z_DEST (z=0-11)	BRC Destination Channels for Input Channel z	000404 <sub>H</sub> +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_BRC_IRQ_N OTIFY	BRC Interrupt Notification Register	000460 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_IRQ_E N	BRC Interrupt Enable Register	000464 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_IRQ_F ORCINT	BRC Force Interrupt Register	000468 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_IRQ_MODE	BRC Interrupt Mode Configuration Register	00046C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_RST	BRC Software Reset Register	000470 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_EIRQ_EN	BRC Error Interrupt Enable Register	000474 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ICM_IRQG_0	ICM Interrupt Group Register Covering Infrastructural and Safety Components ARU, BRC, AEI, PSM0, PSM1, MAP, CMP, SPE	000600 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_1	ICM Interrupt Group Register Covering DPLL	000604 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_2	ICM Interrupt Group Register Covering TIM0, TIM1, TIM2, TIM3	000608 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_3	ICM Interrupt Group Register Covering TIM4, TIM5, TIM6, TIM7	00060C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_4	ICM Interrupt Group Register Covering MCS0 to MCS3 Sub-Modules	000610 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_5	ICM Interrupt Group Register Covering MCS4 to MCS6 Sub-Modules	000614 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_6	ICM Interrupt Group Register Covering GTM Output Sub-Modules TOM0 to TOM1	000618 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_ICM_IRQG_7	ICM Interrupt Group Register Covering GTM Output Sub-Modules TOM2 to TOM3	00061C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_8	ICM Interrupt Group Register Covering GTM Output Sub-Modules TOM4 to TOM5	000620 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_9	ICM Interrupt Group Register Covering GTM Output Sub-Modules ATOM0, ATOM1, ATOM2 and ATOM3	000624 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_10	ICM Interrupt Group Register Covering GTM Output Sub-Modules ATOM4 to ATOM7	000628 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_11	ICM Interrupt Group Register Covering GTM Output Sub-Modules ATOM8 to ATOM11	00062C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_MEI	ICM Interrupt Group Register for Module Error Interrupt Information	000630 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI0	ICM Interrupt Group Register 0 for Channel Error Interrupt Information	000634 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI1	ICM Interrupt Group Register 1 for Channel Error Interrupt Information	000638 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI2	ICM Interrupt Group Register 2 for Channel Error Interrupt Information	00063C <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI3	ICM Interrupt Group Register 3 for Channel Error Interrupt Information	000640 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI4	ICM Interrupt Group Register 4 for Channel Error Interrupt Information	000644 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_MCSI_CEI (i=0-9)	ICM Interrupt Group MCS i for Channel Error Interrupt information	000664 <sub>H</sub> +i*4	U,SV,32		Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ICM_IRQG_PSM_k_CEI (k=0)	ICM Interrupt Group PSM 0 for Channel Error Interrupt information of FIFO0, FIFO1, FIFO2	0006A4 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_SPE_CEI	ICM Interrupt Group SPE for Module Error Interrupt Information	0006B4 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CLS_k_MEI (k=0-2)	ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm	000710 <sub>H</sub> +k*4	U,SV,32		Application Reset	50
GTM_ICM_IRQG_MCSi_CI (i=0-9)	ICM Interrupt Group MCS i for Channel Interrupt Information	000720 <sub>H</sub> +i*4	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_PSM_k_CI (k=0)	ICM Interrupt Group PSM 0 for Channel Interrupt Information of FIFO0, FIFO1, FIFO2	000760 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_SPE_CI	ICM Interrupt Group SPE for Module Interrupt Information	000770 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_ATOM_k_CI (k=0-2)	ICM Interrupt Group ATOM k for Channel Interrupt Information of ATOMm	000790 <sub>H</sub> +k*4	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_TOM_k_CI (k=0-2)	ICM Interrupt Group TOM k for Channel Interrupt Information of TOMm	0007A0 <sub>H</sub> +k*4	U,SV,32		Application Reset	See Family Spec
GTM_SPEi_CTRL_STAT (i=0-5)	SPEi Control Status Register	000800 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_PAT (i=0-5)	SPEi Input Pattern Definition Register	000804 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_OUT_PATz (i=0-5;z=0-7)	SPEi Output Definition Register z	000808 <sub>H</sub> +i*80 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_OUT_CTRL (i=0-5)	SPEi Output Control Register	000828 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_IRQ_NOTIFY (i=0-5)	SPEi Interrupt Notification Register	00082C <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_SPEi_IRQ_E_N (i=0-5)	SPEi Interrupt Enable Register	000830 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_IRQ_F_ORCINT (i=0-5)	SPEi Interrupt Generation by Software	000834 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_IRQ_MODE (i=0-5)	SPEi Interrupt Mode Configuration Register	000838 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_EIRQ_EN (i=0-5)	SPEi Error Interrupt Enable Register	00083C <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_REV_CNT (i=0-5)	SPEi Input Revolution Counter	000840 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_REV_CMP (i=0-5)	SPEi Revolution Counter Compare Value	000844 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_CTRL_STAT2 (i=0-5)	SPEi Control Status Register 2	000848 <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_CMD (i=0-5)	SPEi Command register	00084C <sub>H</sub> +i*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MAP_CTRL	MAP Control Register	000F00 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCFG_CTR_L	MCFG Memory Layout Configuration Register	000F40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_GPR0 (i=0-7;x=0-7)	TIMi Channel x General Purpose 0 Register	001000 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_GPR1 (i=0-7;x=0-7)	TIMi Channel x General Purpose 1 Register	001004 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_CNT (i=0-7;x=0-7)	TIMi Channel x SMU Counter Register	001008 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_TIMi_CHx_ECNT (i=0-7;x=0-7)	TIMi Channel x SMU Edge Counter Register	00100C <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_TIMi_CHx_CNTS (i=0-7;x=0-7)	TIMi Channel x SMU Shadow Counter Register	001010 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_TDUC (i=0-7;x=0-7)	TIMi Channel x TDU Counter Register	001014 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_TDUV (i=0-7;x=0-7)	TIMi Channel x TDU Control Register	001018 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_FLT_RE (i=0-7;x=0-7)	TIMi Channel x Filter Parameter 0 Register	00101C <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_FLT_FE (i=0-7;x=0-7)	TIMi Channel x Filter Parameter 1 Register	001020 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_CTRL (i=0;x=0-7) (i=1-7;x=0-7)	TIMi Channel x Control Register	001024 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	91 and Family Spec
GTM_TIMi_CHx_ECTRL (i=0-7;x=0-7)	TIMi Channel x Extended Control Register	001028 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_I_RQ_NOTIFY (i=0-7;x=0-7)	TIMi Channel x Interrupt Notification Register	00102C <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_I_RQ_EN (i=0-7;x=0-7)	TIMi Channel x Interrupt Enable Register	001030 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_I_RQ_FORCINT (i=0-7;x=0-7)	TIMi Channel x Force Interrupt Register	001034 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_I_RQ_MODE (i=0-7;x=0-7)	TIMi Channel x Interrupt Mode Configuration Register	001038 <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_EIRQ_EN (i=0-7;x=0-7)	TIMi Channel x Error Interrupt Enable Register	00103C <sub>H</sub> +i*800 <sub>H</sub> + x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_INP_V_AL (i=0-7)	TIMi Input Value Observation Register	001074 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_TIMi_IN_SR_C (i=0-7)	TIMi AUX IN Source Selection Register	001078 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_TIMi_RST (i=0-7)	TIMi Global Software Reset Register	00107C <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_CTRL (i=0-5;x=0-15)	TOMi Channel x Control Register	008000 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_SR0 (i=0-5;x=0-15)	TOMi Channel x CCU0 Compare Shadow Register	008004 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_SR1 (i=0-5;x=0-15)	TOMi Channel x CCU1 Compare Shadow Register	008008 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_CM0 (i=0-5;x=0-15)	TOMi Channel x CCU0 Compare Register	00800C <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_CM1 (i=0-5;x=0-15)	TOMi Channel x CCU1 Compare Register	008010 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_CNO (i=0-5;x=0-15)	TOMi Channel x CCU0 Counter Register	008014 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_STAT (i=0-5;x=0-15)	TOMi Channel x Status Register	008018 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_NOTIFY (i=0-5;x=0-15)	TOMi Channel x Interrupt Notification Register	00801C <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_EN (i=0-5;x=0-15)	TOMi Channel x Interrupt Enable Register	008020 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_FORCINT (i=0-5;x=0-15)	TOMi Channel x Force Interrupt Register	008024 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_MODE (i=0-5;x=0-15)	TOMi Channel x Interrupt Mode Register	008028 <sub>H</sub> +i*800 <sub>H</sub> + x*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_GLB_CTRL (i=0-5)	TOMi TGC0 Global Control Register	008030 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_ACT_TB (i=0-5)	TOMi TGC0 Action Time Base Register	008034 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_TOMi_TGC0_FUPD_CTRL (i=0-5)	TOMi TGC0 Force Update Control Register	008038 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_INT_TRIG (i=0-5)	TOMi TGC0 Internal Trigger Control Register	00803C <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_ENDIS_CTRL (i=0-5)	TOMi TGC0 Enable/Disable Control Register	008070 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_ENDIS_STAT (i=0-5)	TOMi TGC0 Enable/Disable Status Register	008074 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_OUTEN_CTRL (i=0-5)	TOMi TGC0 Output Enable Control Register	008078 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_OUTEN_STAT (i=0-5)	TOMi TGC0 Output Enable Status Register	00807C <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_GLB_CTRL (i=0-5)	TOMi TGC1 Global Control Register	008230 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_ACT_TB (i=0-5)	TOMi TGC1 Action Time Base Register	008234 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_FUPD_CTRL (i=0-5)	TOMi TGC1 Force Update Control Register	008238 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_INT_TRIG (i=0-5)	TOMi TGC1 Internal Trigger Control Register	00823C <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_ENDIS_CTRL (i=0-5)	TOMi TGC1 Enable/Disable Control Register	008270 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_ENDIS_STAT (i=0-5)	TOMi TGC1 Enable/Disable Status Register	008274 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_OUTEN_CTRL (i=0-5)	TOMi TGC1 Output Enable Control Register	008278 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_OUTEN_STAT (i=0-5)	TOMi TGC1 Output Enable Status Register	00827C <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_F2Ai_CHz_ARU_RD_FIFO (i=0-2;z=0-7)	F2Ai Stream z Read Address Register	018000 <sub>H</sub> +i*4000 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_F2Ai_CHz_STR_CFG (i=0-2;z=0-7)	F2Ai Stream z Configuration Register	018020 <sub>H</sub> +i*4000 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_F2Ai_ENABLE (i=0-2)	F2Ai Stream Activation Register	018040 <sub>H</sub> +i*4000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_F2Ai_CTRL (i=0-2)	F2Ai Stream Control Register	018044 <sub>H</sub> +i*4000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_AFDi_CHx_BUF_ACC (i=0-2;x=0-7)	AFDi FIFO x Buffer Access Register	018080 <sub>H</sub> +i*4000 <sub>H</sub> +x*10 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_CTRL (i=0-2;z=0-7)	FIFOi Channel z Control Register	018400 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_END_ADDR (i=0-2;z=0-7)	FIFOi Channel z End Address Register	018404 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_START_ADDR (i=0-2;z=0-7)	FIFOi Channel z Start Address Register	018408 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_UPPER_WM (i=0-2;z=0-7)	FIFOi Channel z Upper Watermark Register	01840C <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_LOWER_WM (i=0-2;z=0-7)	FIFOi Channel z Lower Watermark Register	018410 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_STATUS (i=0-2;z=0-7)	FIFOi Channel z Status Register	018414 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_FIFOi_CHz_FILL_LEVEL (i=0-2;z=0-7)	FIFOi Channel z Fill Level Register	018418 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_FIFOi_CHz_WR_PTR (i=0-2;z=0-7)	FIFOi Channel z Write Pointer Register	01841C <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_FIFOi_CHz_RD_PTR (i=0-2;z=0-7)	FIFOi Channel z Read Pointer Register	018420 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_FIFOi_CHz_IRQ_NOTIFY (i=0-2;z=0-7)	FIFOi Channel z Interrupt Notification Register	018424 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_IRQ_EN (i=0-2;z=0-7)	FIFOi Channel z Interrupt Enable Register	018428 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_IRQ_FORCINT (i=0-2;z=0-7)	FIFOi Channel z Force Interrupt Register	01842C <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_IRQ_MODE (i=0-2;z=0-7)	FIFOi Channel z Interrupt Mode Control Register	018430 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_EIRQ_EN (i=0-2;z=0-7)	FIFOi Channel z Error Interrupt Enable Register	018434 <sub>H</sub> +i*4000 <sub>H</sub> +z*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_PSM_FIFOi_MEMORY (i=0-2)	Mapped section of FIFO RAM (001000 <sub>H</sub> Byte)	019000 <sub>H</sub> +i*4000 <sub>H</sub>	U,SV	U,SV		
GTM_DPLL_CTRL_0	DPLL Control Register 0	028000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_1	DPLL Control Register 1	028004 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_2	DPLL Control Register 2	028008 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_3	DPLL Control Register 3	02800C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_4	DPLL Control Register 4	028010 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_5	DPLL Control Register 5	028014 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ACT_STA	DPLL ACTION Status Register with Connected Shadow Register	028018 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_OSW	DPLL Offset and Switch Old/New Address Register	02801C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_DPLL_AOSV_2	DPLL Address Offset Register of RAM 2 Regions	028020 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_APT	DPLL Actual RAM Pointer Address for TRIGGER	028024 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLAPS	DPLL Actual RAM Pointer Address for STATE	028028 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APT_2C	DPLL Actual RAM Pointer for Region 2C	02802C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLAPS_1C3	DPLL Actual RAM Pointer for RAM Region 1C3	028030 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NUTC	DPLL Number of Recent TRIGGER Events Used for Calculations	028034 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NUSC	DPLL Number of Recent STATE Events Used for Calculations	028038 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NTI_CNT	DPLL Number of Active TRIGGER Events to Interrupt	02803C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_NOTIFY	DPLL Interrupt Notification Register	028040 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_EN	DPLL Interrupt Enable Register	028044 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_FORCINT	DPLL Interrupt Force Register	028048 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_MODE	DPLL Interrupt Mode Register	02804C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_EIRQ_EN	DPLL Error Interrupt Enable Register	028050 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_INC_CNT1	DPLL Counter for Pulses for TBU_CH1_BASE to be Sent in Automatic End Mode	0280B0 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_INC_CNT2	DPLL Counter for Pulses for TBU_TS2 to be Sent in Automatic End Mode	0280B4 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APT_SYNC	DPLL Old RAM Pointer and Offset Value for TRIGGER	0280B8 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLAPS_SYNC	DPLL Old RAM Pointer and Offset Value for STATE	0280BC <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_TBU_TS0_T	DPLL TBU_TS0 Value at Last TRIGGER Event	0280C0 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_TBU_TS0_S	DPLL TBU_TS0 Value at Last STATE Event	0280C4 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ADD_IN_LD1	DPLL Direct Load Input Value for SUB_INC1	0280C8 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ADD_IN_LD2	DPLL Direct Load Input Value for SUB_INC2	0280CC <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_STATUS	DPLL Status Register	0280FC <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ID_P_MTR_z (z=0-31)	DPLL ID Information for Input Signal PMT z Register	028100 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_0_SHADOW_TRIGGER	DPLL Control 0 Shadow Trigger Register	0281E0 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_CTRL_0_SHADOW_STATE	DPLL Control 0 Shadow STATE Register	0281E4 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_CTRL_1_SHADOW_TRIGGER	DPLL Control 1 Shadow TRIGGER Register	0281E8 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_CTRL_1_SHADOW_STATE	DPLL Control 1 Shadow STATE Register	0281EC <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_RAMINI	DPLL RAM Initialization Register	0281FC <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_DPLL_PSAi (i=0-31)	DPLL ACTION_i Position/Value Request	028200 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DLAI (i=0-31)	DPLL ACTION_i Time to React before PSAi	028280 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NAI (i=0-31)	DPLL Calculated Number of TRIGGER/STATE Increments to ACTION_i	028300 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DTAi (i=0-31)	DPLL Calculated Relative TIME to ACTION_i	028380 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_T	DPLL Actual TRIGGER Time Stamp Value	028400 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_T_OLD	DPLL Previous TRIGGER Time Stamp Value	028404 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_FTV_T	DPLL Actual TRIGGER Filter Value	028408 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_S	DPLL Actual STATE Time Stamp	028410 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_S_OLD	DPLL Previous STATE Time Stamp	028414 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_FTV_S	DPLL Actual STATE Filter Value	028418 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_THMI	DPLL TRIGGER Hold Time Minimum Value	028420 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_THMA	DPLL TRIGGER Hold Time Maximum Value	028424 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_THVAL	DPLL Measured TRIGGER Hold Time Value	028428 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TOV	DPLL Time Out Value of Active TRIGGER Slope	028430 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_DPLL_TOV_S	DPLL Time Out Value of Active STATE Slope	028434 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_ADD_IN_CAL1	DPLL Calculated ADD_IN Value for SUB_INC1 Generation	028438 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_ADD_IN_CAL2	DPLL Calculated ADD_IN Value for SUB_INC2 Generation	02843C <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MPVAL1	DPLL Missing Pulses to be Added or Subtracted Directly 1	028440 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MPVAL2	DPLL Missing Pulses to be Added or Subtracted Directly 2	028444 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_T_TAR	DPLL Target Number of Pulses to be Sent in Normal Mode	028448 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_T_TAR_OLD	DPLL Last but One Target Number of Pulses to be Sent in Normal Mode	02844C <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_S_TAR	DPLL Target Number of Pulses to be Sent in Emergency Mode	028450 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_S_TAR_OLD	DPLL Last but One Target Number of Pulses to be Sent in Emergency Mode	028454 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCDT_TX	DPLL Reciprocal Value of the Expected Increment Duration of TRIGGER	028460 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCDT_SX	DPLL Reciprocal Value of the Expected Increment Duration of STATE	028464 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCDT_TX_NOM	DPLL Reciprocal Value of the Expected Nominal Increment Duration of TRIGGER	028468 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCDT_SX_NOM	DPLL Reciprocal Value of the Expected Nominal Increment Duration of STATE	02846C <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_DPLL_RDT_T_ACT	DPLL Reciprocal Value of the Last Increment of TRIGGER	028470 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RDT_S_ACT	DPLL Reciprocal Value of the Last Increment of STATE	028474 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DT_T_ACT	DPLL Duration of the Last TRIGGER Increment	028478 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DT_S_ACT	DPLL Duration of the Last STATE Increment	02847C <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_EDT_T	DPLL Difference of Prediction to Actual Value of the Last TRIGGER Increment	028480 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MED_T_T	DPLL Weighted Difference of Prediction Errors of TRIGGER	028484 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_EDT_S	DPLL Difference of Prediction to Actual Value of the Last STATE Increment	028488 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MED_T_S	DPLL Weighted Difference of Prediction Errors of STATE	02848C <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_TX	DPLL Prediction of the Actual TRIGGER Increment Duration	028490 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_SX	DPLL Prediction of the Actual STATE Increment Duration	028494 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_TX_NOM	DPLL Prediction of the Nominal TRIGGER Increment Duration	028498 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_SX_NOM	DPLL Prediction of the Nominal STATE Increment Duration	02849C <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TLR	DPLL TRIGGER Locking Range	0284A0 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_SLR	DPLL STATE Locking Range	0284A4 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_PDT_z (z=0-31)	DPLL Projected Increment Sum Relations for Action z	028500 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MLS1	DPLL Calculated Number of Sub-Pulses between two Nominal STATE Events for SMC = 0	0285C0 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MLS2	DPLL Calculated Number of Sub-Pulses between two Nominal STATE Events for SMC = 1 and RMO = 1	0285C4 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CNT_NUM_1	DPLL Number of Sub-Pulses of SUB_INC1 in Continuous Mode	0285C8 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CNT_NUM_2	DPLL Number of Sub-Pulses of SUB_INC2 in Continuous Mode	0285CC <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PVT	DPLL Plausibility Value of Next TRIGGER Slope	0285D0 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSTC	DPLL Actual Calculated Position Stamp of TRIGGER	0285E0 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSSC	DPLL Actual Calculated Position Stamp of STATE	0285E4 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSTM	DPLL Measured Position Stamp at Last TRIGGER Input	0285E8 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSTM_OLD	DPLL Measured Position Stamp at Last but One TRIGGER Input	0285EC <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSSM	DPLL Measured Position Stamp at Last STATE Input	0285F0 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSSM_OLD	DPLL Measured Position Stamp at Last but One STATE Input	0285F4 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_T	DPLL Number of Pulses to be Sent in Normal Mode	0285F8 <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_DPLL_NMB_S	DPLL Number of Pulses to be Sent in Emergency Mode	0285FC <sub>H</sub>	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RDT_Si (i=0-63)	DPLL Reciprocal Values of the Nominal STATE i Increment Duration in FULL_SCALE	028600 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TSF_Si (i=0-63)	DPLL Time Stamp Values of the Nominal STATE i Events in FULL_SCALE	028700 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_ADT_Si (i=0-63)	DPLL Adapt and Profile Values of the STATE i Increments in FULL_SCALE	028800 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DT_Si (i=0-63)	DPLL Nominal STATE i Increment Duration in FULL_SCALE	028900 <sub>H</sub> +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TSAC_z (z=0-31)	DPLL Calculated Time Value to start Action z Register	028E00 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_PSAC_z (z=0-31)	DPLL ACTION Position/Value Action z Request Register	028E80 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ACB_z (z=0-7)	DPLL Control Bits Register z for up to 32 Actions	028F00 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_11	DPLL Control Register 11	028F20 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_THVA_L2	DPLL Immediate THVAL Value Register	028F24 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_TIDE_L	DPLL Additional TRIGGER Input Delay Register	028F28 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_SIDE_L	DPLL Additional STATE Input Delay Register	028F2C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APSSYNC_EXT	DPLL Extension Register for DPLL_APSSYNC	028F30 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_EXT	DPLL Extension Register for DPLL_CTRL	028F34 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)****Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_DPLLAPS_EXT	DPLL Extension Register for DPLL_APS	028F38 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLAPS_1C3_EXT	DPLL Extension Register for DPLL_APS_1C3	028F3C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLSTA	DPLL Status of the State Machine States Register	028F40 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_DPLLINCF1_OFFSET	DPLL Start Value of the ADD_IN_ADDER1 Register	028F44 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLINCF2_OFFSET	DPLL Start Value of the ADD_IN_ADDER2 Register	028F48 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLDTTSTART	DPLL Start Value of DPLL_DT_T_ACT for the First Increment after SIP1 is Set to 1	028F4C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLDTSSTART	DPLL Start Value of DPLL_DT_S_ACT for the First Increment after SIP2 is Set to 1	028F50 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLSTA_MASK	DPLL Trigger Masks for Signals DPLL_STA_T and DPLL_STA_S	028F54 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLSTAFLAG	DPLL STA Flag Register	028F58 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLINC_CNT1_MASK	DPLL INC_CNT1 Trigger Mask	028F5C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLINC_CNT2_MASK	DPLL INC_CNT2 Trigger Mask	028F60 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLNUSC_EXT1	DPLL Extension Register Number 1 for DPLL_NUSC 4	028F64 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLLNUSC_EXT2	DPLL Extension Register Number 2 for DPLL_NUSC 4	028F68 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_CTN_MIN	DPLL Minimum CDT_T Nominal Value Register	028F6C <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTN_MAX	DPLL Maximum CDT_T Nominal Value Register	028F70 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CSN_MIN	DPLL Minimum CDT_S Nominal Value Register	028F74 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CSN_MAX	DPLL Maximum CDT_S Nominal Value Register	028F78 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_RR2	RAM based TRIGGER data (004000 <sub>H</sub> Byte)	02C000 <sub>H</sub>	U,SV	U,SV		
GTM_MCSI_MEM(i=0-9)	Mapped section of embedded RAM 0 (002000 <sub>H</sub> Byte)	038000 <sub>H</sub> +i*8000 <sub>H</sub>	U,SV	U,SV		
GTM_MCSI_MEM1(i=0-9)	Mapped section of embedded RAM 1 (001000 <sub>H</sub> Byte)	03A000 <sub>H</sub> +i*8000 <sub>H</sub>	U,SV	U,SV		
GTM_CLC	Clock Control Register	09FD00 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_RESET_CLR	Kernel Reset Status Clear Register	09FD04 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_RESET1	Kernel Reset Register 0	09FD08 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_RESET2	Kernel Reset Register 1	09FD0C <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_ACCEN0	Access Enable Register 0	09FD10 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
GTM_ACCEN1	Access Enable Register 1	09FD14 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
GTM_OTBU0T	OCDS TBU0 Trigger Register	09FD18 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_OTBU1T	OCDS TBU1 Trigger Register	09FD1C <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTBU2T	OCDS TBU2 Trigger Register	09FD20 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTBU3T	OCDS TBU3 Trigger Register	09FD24 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTSS	OCDS Trigger Set Select Register	09FD28 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTSC0	OCDS Trigger Set Control 0 Register	09FD2C <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTSC1	OCDS Trigger Set Control 1 Register	09FD30 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
GTM_ODA	OCDS Debug Access Register	09FD34 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OCS	OCDS Control and Status	09FD38 <sub>H</sub>	U,SV	SV,P,OEN	Debug Reset	See Family Spec
GTM_TIMnINSEL (n=0-7)	TIMn Input Select Register	09FD40 <sub>H</sub> +n*4	U,SV	U,SV,P	Application Reset	58
GTM_TOUTSELn (n=0-33)	Timer Output Select Register	09FD60 <sub>H</sub> +n*4	U,SV	U,SV,P	Application Reset	97
GTM_DSADCINSE Li (i=0-5)	DSADC Input Select i Register	09FE00 <sub>H</sub> +i*4	U,SV	U,SV,P	Application Reset	341
GTM_DSADCOUT SELi0 (i=0-3)	DSADC Output Select i0 Register	09FE20 <sub>H</sub> +i*8	U,SV	U,SV,P	Application Reset	369
GTM_DSADCOUT SELi1 (i=0-3)	DSADC Output Select i1 Register	09FE24 <sub>H</sub> +i*8	U,SV	U,SV,P	Application Reset	370
GTM_ADCTRIGiO UT0 (i=0-4)	ADC Trigger i Output Select 0 Register	09FE40 <sub>H</sub> +i*8	U,SV	U,SV,P	Application Reset	380

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ADCTRIGiO UT1 (i=0-4)	ADC Trigger i Output Select 1 Register	09FE44 <sub>H</sub> +i*8	U,SV	U,SV,P	Application Reset	<a href="#">382</a>
GTM_DXOUTCON	Data Exchange Output Control Register	09FE70 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_TRIGOUTn (n=0-9)	Trigger Output Register n	09FE74 <sub>H</sub> +n*4	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_INTERRUPTn (n=0-9)	Interrupt Output Register n	09FE9C <sub>H</sub> +n*4	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_MCSTRIGO UTSEL	Trigger Output Select Register	09FEC4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">52</a>
GTM_MCSINTSTA T	MCS Interrupt Status Register	09FEC8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_MCSINTCLR	MCS Interrupt Clear Register	09FECC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_DXINCON	Data Exchange Input Control Register	09FED0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_DATAINn (n=0-9)	Data Input n Register	09FED4 <sub>H</sub> +n*4	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_MSCSETiCO Nj (i=0;j=0-3) (i=1;j=0-3) (i=2;j=0-3) (i=3;j=0-3) (i=4;j=0-3) (i=5;j=0-3) (i=6;j=0-3) (i=7;j=0-3) (i=8;j=0-3)	MSC Set i Control j Register	09FF00 <sub>H</sub> +i*10 <sub>H</sub> +j*4	U,SV	U,SV,P	Application Reset	<a href="#">278</a>
GTM_MSCiINLCO N (i=0-3)	MSCi Input Low Control Register	09FF90 <sub>H</sub> +i*12	U,SV	U,SV,P	Application Reset	<a href="#">334</a>
GTM_MSCiINHCO N (i=0-3)	MSCi Input High Control Register	09FF94 <sub>H</sub> +i*12	U,SV	U,SV,P	Application Reset	<a href="#">334</a>

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_MSCiINLEX TCON (i=0-3)	MSCi Input Low Extended Control Register	09FF98 <sub>H</sub> +i*12	U,SV	U,SV,P	Application Reset	<a href="#">335</a>
GTM_PSI5OUTSEL	PSI5 Output Select Register	09FFCC <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">405</a>
GTM_PSI5SOUTSEL	PSI5-S Output Select Register	09FFD0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">406</a>
GTM_LCDCDCOUTSEL	LCDCDC Output Select Register	09FFD4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">409</a>
GTM_DTMAUXINSEL	DTM_AUX Input Selection Register	09FFD8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">270</a>
GTM_CANOUTSEL0	CAN0/CAN1 Output Select Register	09FFDC <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">398</a>
GTM_CANOUTSEL1	CAN2 Output Select Register	09FFE0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">401</a>
GTM_CCMi_ARPz_CTRL (i=0-9;z=0-9)	CCMi Address Range Protector z Control Register	0E2000 <sub>H</sub> +i*200 <sub>H</sub> + z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_ARPz_PROT (i=0-9;z=0-9)	CCMi Address Range Protector z Protection Register	0E2004 <sub>H</sub> +i*200 <sub>H</sub> + z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_AEIM_STA (i=0-9)	CCMi MCS Bus Master Status Register	0E21D8 <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_HW_CONF (i=0-11)	CCMi Hardware Configuration Register	0E21DC <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_CCMi_TIM_AUX_IN_SRC (i=0-7)	CCMi TIM Module AUX_IN Source Selection Register	0E21E0 <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_EXT_CAP_EN (i=0-7)	CCMi External Capture Trigger Enable Register	0E21E4 <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	<a href="#">47</a> and Family Spec
GTM_CCMi_TOM_OUT (i=0-5)	CCMi TOM Output Level Register	0E21E8 <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32		Application Reset	<a href="#">49</a>
GTM_CCMi_ATOM_OUT (i=0-11)	CCMi ATOM Output Level Register	0E21EC <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_CCMi_CMU_CLK_CFG (i=0-11)	CCMi CMU Clock Configuration Register	0E21F0 <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_CCMi_CMU_FXCLK_CFG (i=0-11)	CCMi CMU Fixed Clock Configuration Register	0E21F4 <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_CFG (i=0-11)	CCMi Configuration Register	0E21F8 <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	<a href="#">38</a>
GTM_CCMi_PRO_T (i=0-11)	CCMi Protection Register	0E21FC <sub>H</sub> +i*200 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_CTRL (i=0-4;j=0-1,4-5) (i=5-6;j=4-5)	CDTMi DTMj Global Configuration and Control Register	0E4000 <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_CH_CTRL1 (i=0-4;j=0-1,4-5) (i=5-6;j=4-5)	CDTMi DTMj Channel Control Register 1	0E4004 <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_CH_CTRL2 (i=0-4;j=0-1,4-5) (i=5-6;j=4-5)	CDTMi DTMj Channel Control Register 2	0E4008 <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_CH_CTRL2_SHADOW (i=0-4;j=0-1,4-5) (i=5-6;j=4-5)	CDTMi DTMj Channel Control Register 2 Shadow	0E400C <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_PS_CTRL (i=0-4;j=0-1,4-5) (i=5-6;j=4-5)	CDTMi DTMj Phase Shift Unit Configuration and Control Register	0E4010 <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_CHz_DTV (i=0-4;j=0-1,4-5;z=0-3) (i=5-6;j=4-5;z=0-3)	CDTMi DTMj Channel z Dead Time Reload Values	0E4014 <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub> +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_CH_SR (i=0-4;j=0-1,4-5) (i=5-6;j=4-5)	CDTMi DTMj Channel Shadow Register	0E4024 <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT_Mj_CH_CTRL3 (i=0-4;j=0-1,4-5) (i=5-6;j=4-5)	CDTMi DTMj Channel Control Register 3	0E4028 <sub>H</sub> +i*400 <sub>H</sub> +j*40 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ATOMi_CHx_RDADDR (i=0-11;x=0-7)	ATOMi Channel x ARU read address Register	0E8000 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_CTRL (i=0-11;x=0-7)	ATOMi Channel x Control Register	0E8004 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SOMB (i=0-11;x=0-7)	ATOMi Channel x Control Register in SOMB Mode	0E8004 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SOMC (i=0-11;x=0-7)	ATOMi Channel x Control Register in SOMC Mode	0E8004 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SOMI (i=0-11;x=0-7)	ATOMi Channel x Control Register in SOMI Mode	0E8004 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SOMP (i=0-11;x=0-7)	ATOMi Channel x Control Register in SOMP Mode	0E8004 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SOMS (i=0-11;x=0-7)	ATOMi Channel x Control Register in SOMS Mode	0E8004 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SR0 (i=0-11;x=0-7)	ATOMi Channel x CCU0 Compare Shadow Register	0E8008 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SR1 (i=0-11;x=0-7)	ATOMi Channel x CCU1 Compare Shadow Register	0E800C <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_CM0 (i=0-11;x=0-7)	ATOMi Channel x CCU0 Compare Register	0E8010 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_CM1 (i=0-11;x=0-7)	ATOMi Channel x CCU1 Compare Register	0E8014 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_CNO (i=0-11;x=0-7)	ATOMi Channel x CCU0 Counter Register	0E8018 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_STAT (i=0-11;x=0-7)	ATOMi Channel x Status Register	0E801C <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_IRQ_NOTIFY (i=0-11;x=0-7)	ATOMi Channel x Interrupt Notification Register	0E8020 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ATOMi_CHx_IRQ_EN (i=0-11;x=0-7)	ATOMi Channel x Interrupt Enable Register	0E8024 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_IRQ_FORCINT (i=0-11;x=0-7)	ATOMi Channel x Software Interrupt Generation Register	0E8028 <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_IRQ_MODE (i=0-11;x=0-7)	ATOMi Channel x Interrupt Mode Configuration Register	0E802C <sub>H</sub> +i*800 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_GLB_CTRL (i=0-11)	ATOMi AGC Global Control Register	0E8040 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_ENDIS_CTRL (i=0-11)	ATOMi AGC Enable/Disable Control Register	0E8044 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_ENDIS_STAT (i=0-11)	ATOMi AGC Enable/Disable Status Register	0E8048 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_ACT_TB (i=0-11)	ATOMi AGC Action Time Base Register	0E804C <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_OUTEN_CTRL (i=0-11)	ATOMi AGC Output Enable Control Register	0E8050 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_OUTEN_STAT (i=0-11)	ATOMi AGC Output Enable Status Register	0E8054 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_FUPD_CTRL (i=0-11)	ATOMi AGC Force Update Control Register	0E8058 <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_INT_TRIG (i=0-11)	ATOMi AGC Internal Trigger Control Register	0E805C <sub>H</sub> +i*800 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_Ry (i=0-9;x=0-7;y=0-7)	MCSI Channel x General Purpose Register y	0F0000 <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub> +y*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_CTRL (i=0-9;x=0-7)	MCSI Channel x Control Register	0F0020 <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_ACB (i=0-9;x=0-7)	MCSI Channel x ARU Control Bit Register	0F0024 <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec

## Generic Timer Module (GTM)

Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_MCSI_CTRG (i=0-9)	MCSi Clear Trigger Control Register	0F0028 <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_STRG (i=0-9)	MCSi Set Trigger Control Register	0F002C <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_MHB (i=0-9;x=0-7)	MCSi Channel x Memory High Byte Register	0F003C <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32		Application Reset	See Family Spec
GTM_MCSI_CHx_PC (i=0-9;x=0-7)	MCSi Channel x Program Counter Register	0F0040 <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	55
GTM_MCSI_CHx_IRQ_NOTIFY (i=0-9;x=0-7)	MCSi Channel x Interrupt Notification Register	0F0044 <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_IRQ_EN (i=0-9;x=0-7)	MCSi Channel x Interrupt Enable Register	0F0048 <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_IRQ_FORCINT (i=0-9;x=0-7)	MCSi Channel x Force Interrupt Register	0F004C <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_IRQ_MODE (i=0-9;x=0-7)	MCSi Channel x Interrupt Mode Configuration Register	0F0050 <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CHx_EIRQ_EN (i=0-9;x=0-7)	MCSi Channel x Error Interrupt Enable Register	0F0054 <sub>H</sub> +i*1000 <sub>H</sub> +x*80 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_REG_PROT (i=0-9)	MCSi Write Protection Register	0F0060 <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CTRL_STAT (i=0-9)	MCSi Control and Status Register	0F0064 <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_RESET (i=0-9)	MCSi Reset Register	0F0068 <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_CAT (i=0-9)	MCSi Cancel ARU Transfer Instruction Register	0F006C <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

**Generic Timer Module (GTM)**
**Table 331 Register Overview - GTM (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GTM_MCSI_CWT (i=0-9)	MCSI Cancel WURM Instruction Register	0F0070 <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSI_ERR (i=0-9)	MCSI error register	0F007C <sub>H</sub> +i*1000 <sub>H</sub>	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

## Generic Timer Module (GTM)

### 26.3 TC39x Specific Registers

#### 26.3.1 GTM IP Registers Specific Settings

##### CCMi Configuration Register

**NOTE:** The module specific clock enable registers (bit field **EN\_\***) are only implemented if the corresponding module is available in the i-th cluster.

**NOTE:** For the Clusters greater than 4, (only 100MHz capable), the only allowed settings for the **CLS\_CLK\_DIV** are 00 and 10 (clock divider 2).

##### GTM\_CCMi\_CFG (i=0)

**CCMi Configuration Register** **(0E21F8<sub>H</sub>+i\*200<sub>H</sub>)** **Application Reset Value: 0002 007F<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBU_D IR2	TBU_D IR1							0							CLS_CLK_DIV
r	r							r							r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0				0	EN_PS_M	EN_BR_C	EN_DP_LL_MA_P	EN_M_CS	EN_ATOM_A_DTM	EN_TOM_SPE_TDT_M	EN_TIM
				r				r	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>EN_TIM</b>	0	rw	<b>Enable TIM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.  0 <sub>B</sub> Disable clock signal for sub module TIM 1 <sub>B</sub> Enable clock signal for sub module TIM
<b>EN_TOM_SPE_TDTM</b>	1	rw	<b>Enable TOM, SPE and TDTM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.  0 <sub>B</sub> Disable clock signal for modules TOM, SPE, and their related DTM modules 1 <sub>B</sub> Enable clock signal for modules TOM, SPE, and their related DTM modules.
<b>EN_ATOM_AD_TTM</b>	2	rw	<b>Enable ATOM and ADTM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.  0 <sub>B</sub> Disable clock signal for modules ATOM and their related DTM modules. 1 <sub>B</sub> Enable clock signal for modules ATOM and their related DTM modules.

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>EN_MCS</b>	3	rw	<b>Enable MCS</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for module MCS 1 <sub>B</sub> Enable clock signal for module MCS
<b>EN_DPLL_MA P</b>	4	rw	<b>Enable DPLL and MAP</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for modules DPLL and MAP 1 <sub>B</sub> Enable clock signal for modules DPLL and MAP
<b>EN_BRC</b>	5	rw	<b>Enable BRC</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for module BRC 1 <sub>B</sub> Enable clock signal for module BRC
<b>EN_PSM</b>	6	rw	<b>Enable PSM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for module PSM 1 <sub>B</sub> Enable clock signal for module PSM
<b>CLS_CLK_DIV</b>	17:16	r	<b>Cluster Clock Divider</b> The value of this bit field mirrors the bit field <b>CLS[i]_CLK_DIV</b> of register <b>GTM_CLS_CLK_CFG</b> , whereas i equals the cluster index. 00 <sub>B</sub> Cluster is disabled 01 <sub>B</sub> Cluster is enabled without clock divider 10 <sub>B</sub> Cluster is enabled with clock divider 2 11 <sub>B</sub> Reserved, do not use.
<b>TBU_DIR1</b>	30	r	<b>DIR1 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>TBU_DIR2</b>	31	r	<b>DIR2 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>0</b>	7, 15:8, 29:18	r	<b>Reserved</b> Read as zero, shall be written as zero.

## Generic Timer Module (GTM)

## GTM\_CCMi\_CFG (i=1)

## CCMi Configuration Register

(0E21F8<sub>H</sub>+i\*200<sub>H</sub>)Application Reset Value: 0002 00CF<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBU_D IR2	TBU_D IR1						0								CLS_CLK_DIV
r	r						r								r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0				EN_C MP_M ON	EN_PS M	0	0	EN_M CS	EN_AT OM_A DTM	EN_TO M_SPE _TDT M	EN_TI M
				r				rw	rw	r	r	rw	rw	rw	rw

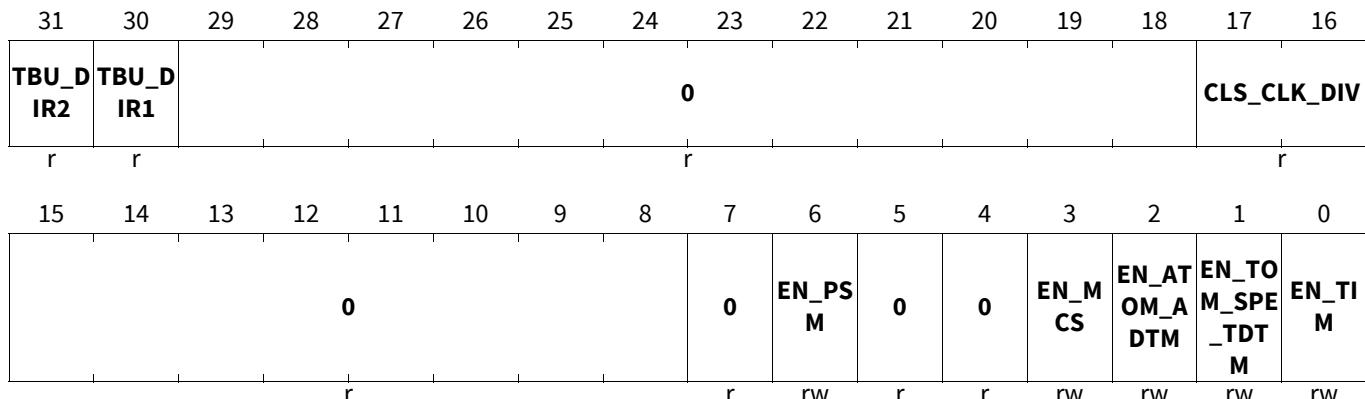
Field	Bits	Type	Description
EN_TIM	0	rw	<b>Enable TIM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for sub module TIM 1 <sub>B</sub> Enable clock signal for sub module TIM
EN_TOM_SPE _TDTM	1	rw	<b>Enable TOM, SPE and TDTM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for modules TOM, SPE, and their related DTM modules 1 <sub>B</sub> Enable clock signal for modules TOM, SPE, and their related DTM modules.
EN_ATOM_AD TM	2	rw	<b>Enable ATOM and ADTM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for modules ATOM and their related DTM modules. 1 <sub>B</sub> Enable clock signal for modules ATOM and their related DTM modules.
EN_MCS	3	rw	<b>Enable MCS</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for module MCS 1 <sub>B</sub> Enable clock signal for module MCS
EN_PSM	6	rw	<b>Enable PSM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for module PSM 1 <sub>B</sub> Enable clock signal for module PSM

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>EN_CMP_MON</b>	7	rw	<b>Enable CMP and MON</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for modules CMP and MON 1 <sub>B</sub> Enable clock signal for modules CMP and MON
<b>CLS_CLK_DIV</b>	17:16	r	<b>Cluster Clock Divider</b> The value of this bit field mirrors the bit field <b>CLS[i]_CLK_DIV</b> of register <b>GTM_CLS_CLK_CFG</b> , whereas i equals the cluster index. 00 <sub>B</sub> Cluster is disabled 01 <sub>B</sub> Cluster is enabled without clock divider 10 <sub>B</sub> Cluster is enabled with clock divider 2 11 <sub>B</sub> Reserved, do not use.
<b>TBU_DIR1</b>	30	r	<b>DIR1 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>TBU_DIR2</b>	31	r	<b>DIR2 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>0</b>	4, 5, 15:8, 29:18	r	<b>Reserved</b> Read as zero, shall be written as zero.

## GTM\_CCMi\_CFG (i=2)

## CCMi Configuration Register

(0E21F8<sub>H</sub>+i\*200<sub>H</sub>)Application Reset Value: 0002 004F<sub>H</sub>

Field	Bits	Type	Description
<b>EN_TIM</b>	0	rw	<b>Enable TIM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for sub module TIM 1 <sub>B</sub> Enable clock signal for sub module TIM

**Generic Timer Module (GTM)**

Field	Bits	Type	Description
<b>EN_TOM_SPE _TDTM</b>	1	rw	<p><b>Enable TOM, SPE and TDTM</b></p> <p>This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.</p> <p>0<sub>B</sub> Disable clock signal for modules TOM, SPE, and their related DTM modules</p> <p>1<sub>B</sub> Enable clock signal for modules TOM, SPE, and their related DTM modules.</p>
<b>EN_ATOM_AD TM</b>	2	rw	<p><b>Enable ATOM and ADTM</b></p> <p>This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.</p> <p>0<sub>B</sub> Disable clock signal for modules ATOM and their related DTM modules.</p> <p>1<sub>B</sub> Enable clock signal for modules ATOM and their related DTM modules.</p>
<b>EN_MCS</b>	3	rw	<p><b>Enable MCS</b></p> <p>This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.</p> <p>0<sub>B</sub> Disable clock signal for module MCS</p> <p>1<sub>B</sub> Enable clock signal for module MCS</p>
<b>EN_PSM</b>	6	rw	<p><b>Enable PSM</b></p> <p>This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.</p> <p>0<sub>B</sub> Disable clock signal for module PSM</p> <p>1<sub>B</sub> Enable clock signal for module PSM</p>
<b>CLS_CLK_DIV</b>	17:16	r	<p><b>Cluster Clock Divider</b></p> <p>The value of this bit field mirrors the bit field <b>CLS[i]_CLK_DIV</b> of register <b>GTM_CLS_CLK_CFG</b>, whereas i equals the cluster index.</p> <p>00<sub>B</sub> Cluster is disabled</p> <p>01<sub>B</sub> Cluster is enabled without clock divider</p> <p>10<sub>B</sub> Cluster is enabled with clock divider 2</p> <p>11<sub>B</sub> Reserved, do not use.</p>
<b>TBU_DIR1</b>	30	r	<p><b>DIR1 input signal of module TBU</b></p> <p>0<sub>B</sub> Indicating forward direction</p> <p>1<sub>B</sub> Indicating backward direction</p>
<b>TBU_DIR2</b>	31	r	<p><b>DIR2 input signal of module TBU</b></p> <p>0<sub>B</sub> Indicating forward direction</p> <p>1<sub>B</sub> Indicating backward direction</p>
<b>0</b>	4, 5, 7, 15:8, 29:18	r	<p><b>Reserved</b></p> <p>Read as zero, shall be written as zero.</p>

## Generic Timer Module (GTM)

## GTM\_CCMi\_CFG (i=3-5)

## CCMi Configuration Register

(0E21F8<sub>H</sub>+i\*200<sub>H</sub>)Application Reset Value: 0002 000F<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBU_D IR2	TBU_D IR1						0								CLS_CLK_DIV
r	r						r								r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0			0	0	0	0	0	EN_M_CS	EN_ATOM_A_DTM	EN_TOM_SPE_TDTM	EN_TIM
				r			r	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
EN_TIM	0	rw	<b>Enable TIM</b> This bit is only writable if bit field <b>CCM[i].PROT</b> of register <b>CCM[i].PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for sub module TIM 1 <sub>B</sub> Enable clock signal for sub module TIM
EN_TOM_SPE_TDTM	1	rw	<b>Enable TOM, SPE and TDTM</b> This bit is only writable if bit field <b>CCM[i].PROT</b> of register <b>CCM[i].PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for modules TOM, SPE, and their related DTM modules 1 <sub>B</sub> Enable clock signal for modules TOM, SPE, and their related DTM modules.
EN_ATOM_AD TM	2	rw	<b>Enable ATOM and ADTM</b> This bit is only writable if bit field <b>CCM[i].PROT</b> of register <b>CCM[i].PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for modules ATOM and their related DTM modules. 1 <sub>B</sub> Enable clock signal for modules ATOM and their related DTM modules.
EN_MCS	3	rw	<b>Enable MCS</b> This bit is only writable if bit field <b>CCM[i].PROT</b> of register <b>CCM[i].PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for module MCS 1 <sub>B</sub> Enable clock signal for module MCS
CLS_CLK_DIV	17:16	r	<b>Cluster Clock Divider</b> The value of this bit field mirrors the bit field <b>CCM[i].CLK_DIV</b> of register <b>GTM_CLS_CLK_CFG</b> , whereas i equals the cluster index. 00 <sub>B</sub> Cluster is disabled 01 <sub>B</sub> Cluster is enabled without clock divider 10 <sub>B</sub> Cluster is enabled with clock divider 2 11 <sub>B</sub> Reserved, do not use.

## Generic Timer Module (GTM)

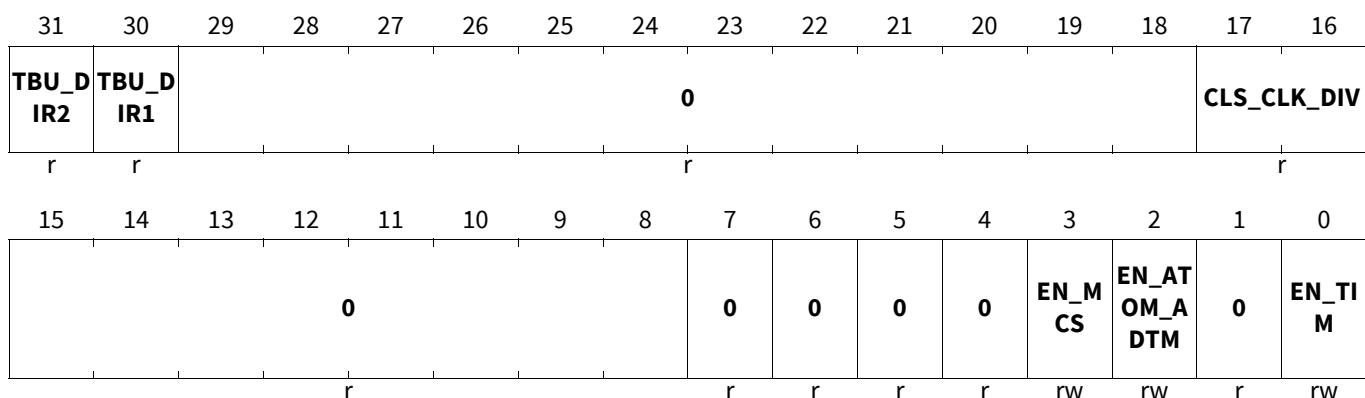
Field	Bits	Type	Description
TBU_DIR1	30	r	<b>DIR1 input signal of module TBU</b> $0_B$ Indicating forward direction $1_B$ Indicating backward direction
TBU_DIR2	31	r	<b>DIR2 input signal of module TBU</b> $0_B$ Indicating forward direction $1_B$ Indicating backward direction
0	4, 5, 6, 7, 15:8, 29:18	r	<b>Reserved</b> Read as zero, shall be written as zero.

## GTM\_CCMi\_CFG (i=6-7)

## CCMi Configuration Register

 $(0E21F8_H+i*200_H)$ 

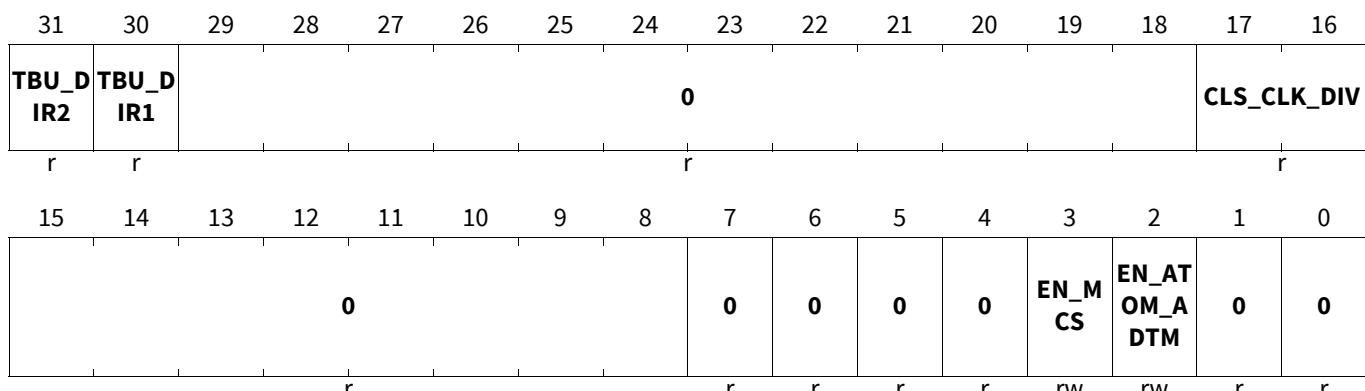
Application Reset Value: 0002 000D\_H



Field	Bits	Type	Description
EN_TIM	0	rw	<b>Enable TIM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i].PROT</b> is cleared. $0_B$ Disable clock signal for sub module TIM $1_B$ Enable clock signal for sub module TIM
EN_ATOM_ADTM	2	rw	<b>Enable ATOM and ADTM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i].PROT</b> is cleared. $0_B$ Disable clock signal for modules ATOM and their related DTM modules. $1_B$ Enable clock signal for modules ATOM and their related DTM modules.
EN_MCS	3	rw	<b>Enable MCS</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i].PROT</b> is cleared. $0_B$ Disable clock signal for module MCS $1_B$ Enable clock signal for module MCS

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CLS_CLK_DIV</b>	17:16	r	<b>Cluster Clock Divider</b> The value of this bit field mirrors the bit field <b>CLS[i]_CLK_DIV</b> of register <b>GTM_CCMi_CFG</b> , whereas i equals the cluster index. 00 <sub>B</sub> Cluster is disabled 01 <sub>B</sub> Cluster is enabled without clock divider 10 <sub>B</sub> Cluster is enabled with clock divider 2 11 <sub>B</sub> Reserved, do not use.
<b>TBU_DIR1</b>	30	r	<b>DIR1 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>TBU_DIR2</b>	31	r	<b>DIR2 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>0</b>	1, 4, 5, 6, 7, 15:8, 29:18	r	<b>Reserved</b> Read as zero, shall be written as zero.

**GTM\_CCMi\_CFG (i=8-9)****CCMi Configuration Register**(0E21F8<sub>H</sub>+i\*200<sub>H</sub>)Application Reset Value: 0002 000C<sub>H</sub>

Field	Bits	Type	Description
<b>EN_ATOM_AD TM</b>	2	rw	<b>Enable ATOM and ADTM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. 0 <sub>B</sub> Disable clock signal for modules ATOM and their related DTM modules. 1 <sub>B</sub> Enable clock signal for modules ATOM and their related DTM modules.

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>EN_MCS</b>	3	rw	<b>Enable MCS</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared.  0 <sub>B</sub> Disable clock signal for module MCS 1 <sub>B</sub> Enable clock signal for module MCS
<b>CLS_CLK_DIV</b>	17:16	r	<b>Cluster Clock Divider</b> The value of this bit field mirrors the bit field <b>CLS[i].CLK_DIV</b> of register <b>GTM_CLS_CLK_CFG</b> , whereas i equals the cluster index.  00 <sub>B</sub> Cluster is disabled 01 <sub>B</sub> Cluster is enabled without clock divider 10 <sub>B</sub> Cluster is enabled with clock divider 2 11 <sub>B</sub> Reserved, do not use.
<b>TBU_DIR1</b>	30	r	<b>DIR1 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>TBU_DIR2</b>	31	r	<b>DIR2 input signal of module TBU</b> 0 <sub>B</sub> Indicating forward direction 1 <sub>B</sub> Indicating backward direction
<b>0</b>	0, 1, 4, 5, 6, 7, 15:8, 29:18	r	<b>Reserved</b> Read as zero, shall be written as zero.

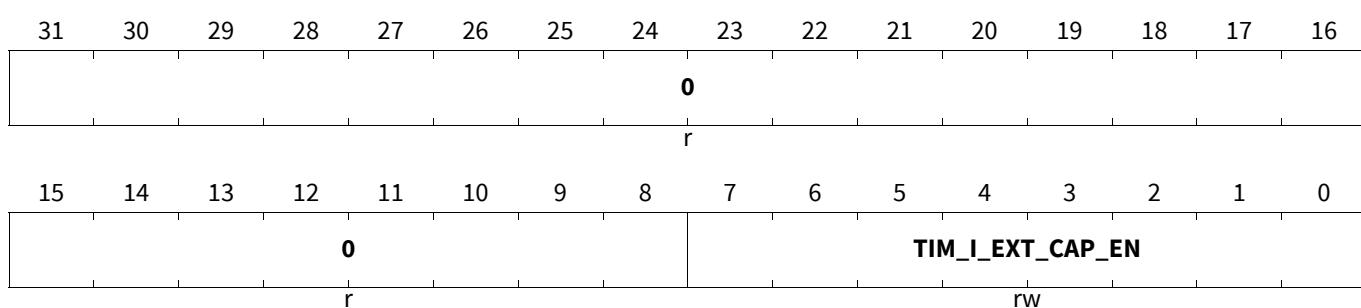
**GTM\_CCMi\_CFG (i=10-11)****CCMi Configuration Register**(0E21F8<sub>H</sub>+i\*200<sub>H</sub>)Application Reset Value: 0002 0004<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>TBU_D IR2</b>	<b>TBU_D IR1</b>							<b>0</b>							<b>CLS_CLK_DIV</b>
r	r							r							r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>EN_AT OM_A DTM</b>	<b>0</b>	<b>0</b>
							r	r	r	r	r	r	rw	r	r

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>EN_ATOM_AD TM</b>	2	rw	<b>Enable ATOM and ADTM</b> This bit is only writable if bit field <b>CLS_PROT</b> of register <b>CCM[i]_PROT</b> is cleared. $0_B$ Disable clock signal for modules ATOM and their related DTM modules. $1_B$ Enable clock signal for modules ATOM and their related DTM modules.
<b>CLS_CLK_DIV</b>	17:16	r	<b>Cluster Clock Divider</b> The value of this bit field mirrors the bit field <b>CLS[i]_CLK_DIV</b> of register <b>GTM_CLS_CLK_CFG</b> , whereas i equals the cluster index. $00_B$ Cluster is disabled $01_B$ Cluster is enabled without clock divider $10_B$ Cluster is enabled with clock divider 2 $11_B$ Reserved, do not use.
<b>TBU_DIR1</b>	30	r	<b>DIR1 input signal of module TBU</b> $0_B$ Indicating forward direction $1_B$ Indicating backward direction
<b>TBU_DIR2</b>	31	r	<b>DIR2 input signal of module TBU</b> $0_B$ Indicating forward direction $1_B$ Indicating backward direction
<b>0</b>	0, 1, 3, 4, 5, 6, 7, 15:8, 29:18	r	<b>Reserved</b> Read as zero, shall be written as zero.

## CCMi External Capture Trigger Enable Register

**GTM\_CCMi\_EXT\_CAP\_EN (i=7)****CCMi External Capture Trigger Enable Register(0E21E4<sub>H</sub>+i\*200<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>TIM_I_EXT_CA_P_EN</b>	7:0	rw	<b>TIM[i].EXT_CAPTURE signal forwarding enable</b> Note: The trigger event forwarding is possible from TIM[i] and TIM[i+1] to MCS[i]. 00 <sub>H</sub> Disable forwarding of signal TIM[i].EXT_CAPTURE to MCS[i] 01 <sub>H</sub> Enable forwarding of signal TIM[i].EXT_CAPTURE to MCS[i]
<b>0</b>	15:8, 31:16	r	<b>Reserved</b> Read as zero, shall be written as zero.

## CMU Control for Clock Source z

**GTM\_CMU\_CLK\_z\_CTRL (z=0-5)**

## CMU Control for Clock Source z

(00030C<sub>H</sub>+z\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				0				<b>CLK_CNT</b>							
r				r											rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CLK_CNT</b>															
r															

Field	Bits	Type	Description
<b>CLK_CNT</b>	23:0	rw	<b>Clock count</b> Defines count value for the clock divider. Value can only be modified when clock enable <b>EN_CLKz</b> and <b>EN_ECLK1</b> are disabled.
<b>0</b>	25:24, 31:26	r	<b>Reserved</b> Read as zero, shall be written as zero.

**GTM\_CMU\_CLK\_z\_CTRL (z=6)**

## CMU Control for Clock Source z

(00030C<sub>H</sub>+z\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				<b>CLK_SEL</b>				<b>CLK_CNT</b>							
r				rw											rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CLK_CNT</b>															
r															

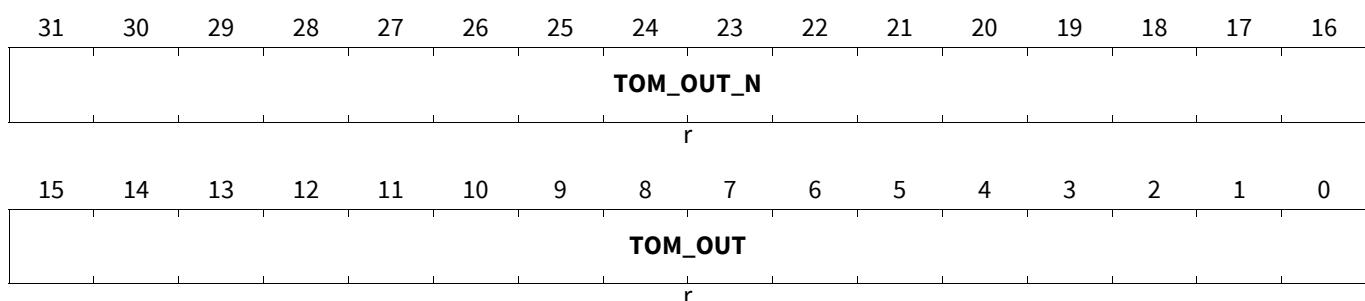
## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CLK_CNT</b>	23:0	rw	<b>Clock count</b> Defines count value for the clock divider. Value can only be modified when clock enable <b>EN_CLKz</b> and <b>EN_ECLK1</b> are disabled.
<b>CLK_SEL</b>	25:24	rw	<b>Clock source selection for CMU_CLKz</b> Value can only be modified when clock enable <b>EN_CLKz</b> and <b>EN_ECLK1</b> are disabled. <i>Note: The existence and interpretation of this bit field depends on z. z&gt;5</i> 00 <sub>B</sub> Use Clock Source 6 Divider 01 <sub>B</sub> Use signal SUB_INC2 of module DPLL / If no DPLL: Reserved, do not use. 10 <sub>B</sub> Use signal SUB_INC1c of module DPLL / If no DPLL: Reserved, do not use 11 <sub>B</sub> Use signal CCM0_CMU_CLK6 of sub-module CCM0
<b>0</b>	31:26	r	<b>Reserved</b> Read as zero, shall be written as zero.

## CCMi TOM Output Level Register

## GTM\_CCMi\_TOM\_OUT (i=0-5)

## CCMi TOM Output Level Register

(0E21E8<sub>H</sub>+i\*200<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

Field	Bits	Type	Description
<b>TOM_OUT</b>	15:0	r	<b>Output level snapshot of TOM[i].OUT all channels</b>
<b>TOM_OUT_N</b>	31:16	r	<b>Output level snapshot of TOM[i].OUT_N all channels</b>

**Generic Timer Module (GTM)****ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm****GTM\_ICM IRQG\_CLS\_k\_MEI (k=0)****ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm****(000710<sub>H</sub>+k\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				0		SPE_M_3_EIR_Q	MCS_M3_EI_RQ	TIM_M3_EIR_Q		0		FIFO_M2_EI_RQ	SPE_M2_EIR_Q	MCS_M2_EI_RQ	TIM_M2_EIR_Q
r				r	r	r	r	r		r		r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
				0		FIFO_M1_EI_RQ	SPE_M1_EIR_Q	MCS_M1_EI_RQ	TIM_M1_EIR_Q		0		FIFO_M0_EI_RQ	SPE_M0_EIR_Q	MCS_M0_EI_RQ	TIM_M0_EIR_Q
r				r	r	r	r	r		r		r	r	r	r	

Field	Bits	Type	Description
<b>TIM_Mj_EIRQ (j=0-3)</b>	8*j	r	<b>Error interrupt TIMm_EIRQ (m=4*0+j)</b> This bit is only set when the error interrupt is enabled in the error interrupt enable register of the corresponding sub-module. 0 <sub>B</sub> No error interrupt occurred 1 <sub>B</sub> Error interrupt was raised by the corresponding sub-module
<b>MCS_Mj_EIRQ (j=0-3)</b>	8*j+1	r	<b>Error interrupt MCSm_EIRQ (m=4*0+j)</b> Coding see bit 0.
<b>SPE_Mj_EIRQ (j=0-3)</b>	8*j+2	r	<b>Error interrupt SPEm_EIRQ (m=4*0+j)</b> Coding see bit 0.
<b>FIFO_Mj_EIRQ (j=0-2)</b>	8*j+3	r	<b>Error interrupt FIFOm_EIRQ (m=4*0+j)</b> Coding see bit 0.
<b>0</b>	27, 31:28, 23:20, 15:12, 7:4	r	<b>Reserved</b> Read as zero, shall be written as zero.

## Generic Timer Module (GTM)

**GTM\_ICM\_IRQG\_CLS\_k\_MEI (k=1)**

**ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm**  
 $(000710_H + k \cdot 4)$       **Application Reset Value: 0000 0000\_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
					0	0	MCS_M3_EI_RQ	TIM_M3_EIR_Q		0		0	0	MCS_M2_EI_RQ	TIM_M2_EIR_Q	
r				r	r	r	r	r	r	r	r	r	r	r	r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
				0	0	SPE_M1_EI_RQ	MCS_M1_EI_RQ	TIM_M1_EIR_Q		0		0	0	SPE_M0_EI_RQ	MCS_M0_EI_RQ	TIM_M0_EIR_Q
r				r	r	r	r	r	r	r	r	r	r	r	r	

Field	Bits	Type	Description
<b>TIM_Mj_EIRQ (j=0-3)</b>	$8^*j$	r	<b>Error interrupt TIMm_EIRQ (m=4*1+j)</b> This bit is only set when the error interrupt is enabled in the error interrupt enable register of the corresponding sub-module. 0 <sub>B</sub> No error interrupt occurred 1 <sub>B</sub> Error interrupt was raised by the corresponding sub-module
<b>MCS_Mj_EIRQ (j=0-3)</b>	$8^*j+1$	r	<b>Error interrupt MCSm_EIRQ (m=4*1+j)</b> Coding see bit 0.
<b>SPE_Mj_EIRQ (j=0-1)</b>	$8^*j+2$	r	<b>Error interrupt SPEm_EIRQ (m=4*1+j)</b> Coding see bit 0.
0	26, 18, 27, 19, 11, 3, 31:28, 23:20, 15:12, 7:4	r	<b>Reserved</b> Read as zero, shall be written as zero.

**GTM\_ICM\_IRQG\_CLS\_k\_MEI (k=2)**

**ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm**  
 $(000710_H + k \cdot 4)$       **Application Reset Value: 0000 0000\_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				0	0	0	0		0		0	0	0	0	0
r				r	r	r	r		r		r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0	0	0	MCS_M1_EI_RQ	0		0		0	0	MCS_M0_EI_RQ	0
r				r	r	r	r	r		r		r	r	r	r

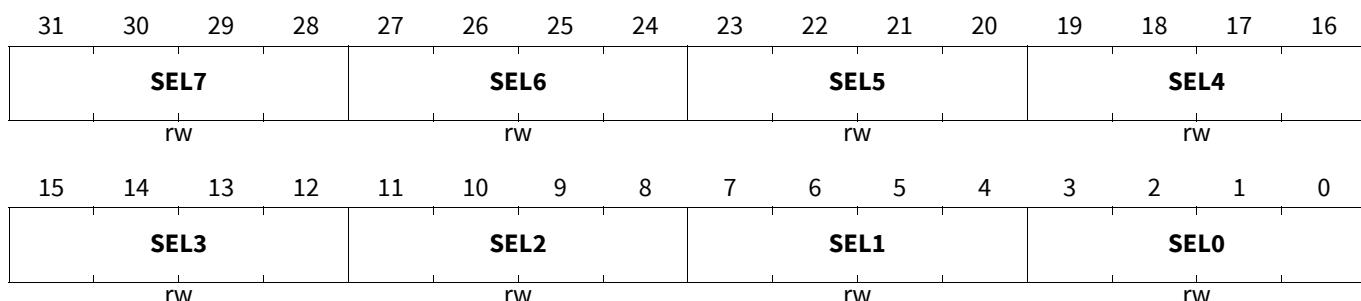
## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>MCS_Mj_EIRQ (j=0-1)</b>	8*j+1	r	<b>Error interrupt MCSm_EIRQ (m=4*2+j)</b> Coding see bit 0.
<b>0</b>	24, 16, 8, 0, 25, 17, 26, 18, 10, 2, 27, 19, 11, 3, 31:28, 23:20, 15:12, 7:4	r	<b>Reserved</b> Read as zero, shall be written as zero.

## Trigger Output Select Register

**GTM\_MCSTRIGOUTSEL**

## Trigger Output Select Register

(09FEC4<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

Field	Bits	Type	Description
<b>SELk (k=0)</b>	4*k+3:4*k	rw	<b>Selects which MCS triggers go to FCkBFDAT/SEL</b> 0 <sub>H</sub> <b>TRG0_01</b> , TRIGOUT0_TRIGO/1 1 <sub>H</sub> <b>TRG1_01</b> , TRIGOUT1_TRIGO/1 2 <sub>H</sub> <b>TRG2_01</b> , TRIGOUT2_TRIGO/1 3 <sub>H</sub> <b>TRG3_01</b> , TRIGOUT3_TRIGO/1 4 <sub>H</sub> <b>TRG4_01</b> , TRIGOUT4_TRIGO/1 5 <sub>H</sub> <b>TRG5_01</b> , TRIGOUT5_TRIGO/1 6 <sub>H</sub> <b>TRG6_01</b> , TRIGOUT6_TRIGO/1 7 <sub>H</sub> <b>TRG7_01</b> , TRIGOUT7_TRIGO/1 8 <sub>H</sub> <b>TRG8_01</b> , TRIGOUT8_TRIGO/1 9 <sub>H</sub> <b>TRG9_01</b> , TRIGOUT9_TRIGO/1 A <sub>H</sub> Reserved, do not use ... F <sub>H</sub> Reserved, do not use

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=1)</b>	4*k+3:4*k	rw	<b>Selects which MCS triggers go to FCkBFDAT/SEL</b> 0 <sub>H</sub> <b>TRG0_23</b> , TRIGOUT0_TRIG2/3 1 <sub>H</sub> <b>TRG1_23</b> , TRIGOUT1_TRIG2/3 2 <sub>H</sub> <b>TRG2_23</b> , TRIGOUT2_TRIG2/3 3 <sub>H</sub> <b>TRG3_23</b> , TRIGOUT3_TRIG2/3 4 <sub>H</sub> <b>TRG4_23</b> , TRIGOUT4_TRIG2/3 5 <sub>H</sub> <b>TRG5_23</b> , TRIGOUT5_TRIG2/3 6 <sub>H</sub> <b>TRG6_23</b> , TRIGOUT6_TRIG2/3 7 <sub>H</sub> <b>TRG7_23</b> , TRIGOUT7_TRIG2/3 8 <sub>H</sub> <b>TRG8_23</b> , TRIGOUT8_TRIG2/3 9 <sub>H</sub> <b>TRG9_23</b> , TRIGOUT9_TRIG2/3 A <sub>H</sub> Reserved, do not use ... F <sub>H</sub> Reserved, do not use
<b>SELk (k=2)</b>	4*k+3:4*k	rw	<b>Selects which MCS triggers go to FCkBFDAT/SEL</b> 0 <sub>H</sub> <b>TRG0_45</b> , TRIGOUT0_TRIG4/5 1 <sub>H</sub> <b>TRG1_45</b> , TRIGOUT1_TRIG4/5 2 <sub>H</sub> <b>TRG2_45</b> , TRIGOUT2_TRIG4/5 3 <sub>H</sub> <b>TRG3_45</b> , TRIGOUT3_TRIG4/5 4 <sub>H</sub> <b>TRG4_45</b> , TRIGOUT4_TRIG4/5 5 <sub>H</sub> <b>TRG5_45</b> , TRIGOUT5_TRIG4/5 6 <sub>H</sub> <b>TRG6_45</b> , TRIGOUT6_TRIG4/5 7 <sub>H</sub> <b>TRG7_45</b> , TRIGOUT7_TRIG4/5 8 <sub>H</sub> <b>TRG8_45</b> , TRIGOUT8_TRIG4/5 9 <sub>H</sub> <b>TRG9_45</b> , TRIGOUT9_TRIG4/5 A <sub>H</sub> Reserved, do not use ... F <sub>H</sub> Reserved, do not use
<b>SELk (k=3)</b>	4*k+3:4*k	rw	<b>Selects which MCS triggers go to FCkBFDAT/SEL</b> 0 <sub>H</sub> <b>TRG0_67</b> , TRIGOUT0_TRIG6/7 1 <sub>H</sub> <b>TRG1_67</b> , TRIGOUT1_TRIG6/7 2 <sub>H</sub> <b>TRG2_67</b> , TRIGOUT2_TRIG6/7 3 <sub>H</sub> <b>TRG3_67</b> , TRIGOUT3_TRIG6/7 4 <sub>H</sub> <b>TRG4_67</b> , TRIGOUT4_TRIG6/7 5 <sub>H</sub> <b>TRG5_67</b> , TRIGOUT5_TRIG6/7 6 <sub>H</sub> <b>TRG6_67</b> , TRIGOUT6_TRIG6/7 7 <sub>H</sub> <b>TRG7_67</b> , TRIGOUT7_TRIG6/7 8 <sub>H</sub> <b>TRG8_67</b> , TRIGOUT8_TRIG6/7 9 <sub>H</sub> <b>TRG9_67</b> , TRIGOUT9_TRIG6/7 A <sub>H</sub> Reserved, do not use ... F <sub>H</sub> Reserved, do not use

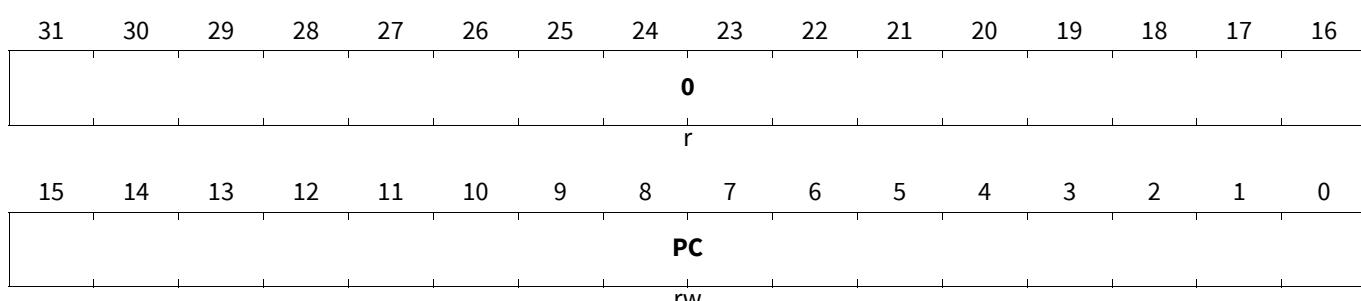
## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=4)</b>	4*k+3:4*k	rw	<p><b>Selects which MCS triggers go to FCkBFDAT/SEL</b></p> <p>0<sub>H</sub> <b>TRG0_89</b>, TRIGOUT0_TRIG8/9      1<sub>H</sub> <b>TRG1_89</b>, TRIGOUT1_TRIG8/9      2<sub>H</sub> <b>TRG2_89</b>, TRIGOUT2_TRIG8/9      3<sub>H</sub> <b>TRG3_89</b>, TRIGOUT3_TRIG8/9      4<sub>H</sub> <b>TRG4_89</b>, TRIGOUT4_TRIG8/9      5<sub>H</sub> <b>TRG5_89</b>, TRIGOUT5_TRIG8/9      6<sub>H</sub> <b>TRG6_89</b>, TRIGOUT6_TRIG8/9      7<sub>H</sub> <b>TRG7_89</b>, TRIGOUT7_TRIG8/9      8<sub>H</sub> <b>TRG8_89</b>, TRIGOUT8_TRIG8/9      9<sub>H</sub> <b>TRG9_89</b>, TRIGOUT9_TRIG8/9      A<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use</p>
<b>SELk (k=5)</b>	4*k+3:4*k	rw	<p><b>Selects which MCS triggers go to FCkBFDAT/SEL</b></p> <p>0<sub>H</sub> <b>TRG0_AB</b>, TRIGOUT0_TRIG10/11      1<sub>H</sub> <b>TRG1_AB</b>, TRIGOUT1_TRIG10/11      2<sub>H</sub> <b>TRG2_AB</b>, TRIGOUT2_TRIG10/11      3<sub>H</sub> <b>TRG3_AB</b>, TRIGOUT3_TRIG10/11      4<sub>H</sub> <b>TRG4_AB</b>, TRIGOUT4_TRIG10/11      5<sub>H</sub> <b>TRG5_AB</b>, TRIGOUT5_TRIG10/11      6<sub>H</sub> <b>TRG6_AB</b>, TRIGOUT6_TRIG10/11      7<sub>H</sub> <b>TRG7_AB</b>, TRIGOUT7_TRIG10/11      8<sub>H</sub> <b>TRG8_AB</b>, TRIGOUT8_TRIG10/11      9<sub>H</sub> <b>TRG9_AB</b>, TRIGOUT9_TRIG10/11      A<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use</p>
<b>SELk (k=6)</b>	4*k+3:4*k	rw	<p><b>Selects which MCS triggers go to FCkBFDAT/SEL</b></p> <p>0<sub>H</sub> <b>TRG0_CD</b>, TRIGOUT0_TRIG12/13      1<sub>H</sub> <b>TRG1_CD</b>, TRIGOUT1_TRIG12/13      2<sub>H</sub> <b>TRG2_CD</b>, TRIGOUT2_TRIG12/13      3<sub>H</sub> <b>TRG3_CD</b>, TRIGOUT3_TRIG12/13      4<sub>H</sub> <b>TRG4_CD</b>, TRIGOUT4_TRIG12/13      5<sub>H</sub> <b>TRG5_CD</b>, TRIGOUT5_TRIG12/13      6<sub>H</sub> <b>TRG6_CD</b>, TRIGOUT6_TRIG12/13      7<sub>H</sub> <b>TRG7_CD</b>, TRIGOUT7_TRIG12/13      8<sub>H</sub> <b>TRG8_CD</b>, TRIGOUT8_TRIG12/13      9<sub>H</sub> <b>TRG9_CD</b>, TRIGOUT9_TRIG12/13      A<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use</p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=7)</b>	4*k+3:4*k	rw	<b>Selects which MCS triggers go to FCkBFDAT/SEL</b> 0 <sub>H</sub> <b>TRG0_EF</b> , TRIGOUT0_TRIG14/15 1 <sub>H</sub> <b>TRG1_EF</b> , TRIGOUT1_TRIG14/15 2 <sub>H</sub> <b>TRG2_EF</b> , TRIGOUT2_TRIG14/15 3 <sub>H</sub> <b>TRG3_EF</b> , TRIGOUT3_TRIG14/15 4 <sub>H</sub> <b>TRG4_EF</b> , TRIGOUT4_TRIG14/15 5 <sub>H</sub> <b>TRG5_EF</b> , TRIGOUT5_TRIG14/15 6 <sub>H</sub> <b>TRG6_EF</b> , TRIGOUT6_TRIG14/15 7 <sub>H</sub> <b>TRG7_EF</b> , TRIGOUT7_TRIG14/15 8 <sub>H</sub> <b>TRG8_EF</b> , TRIGOUT8_TRIG14/15 9 <sub>H</sub> <b>TRG9_EF</b> , TRIGOUT9_TRIG14/15 A <sub>H</sub> Reserved, do not use ... F <sub>H</sub> Reserved, do not use

## MCS0 Channel 0 Program Counter Register

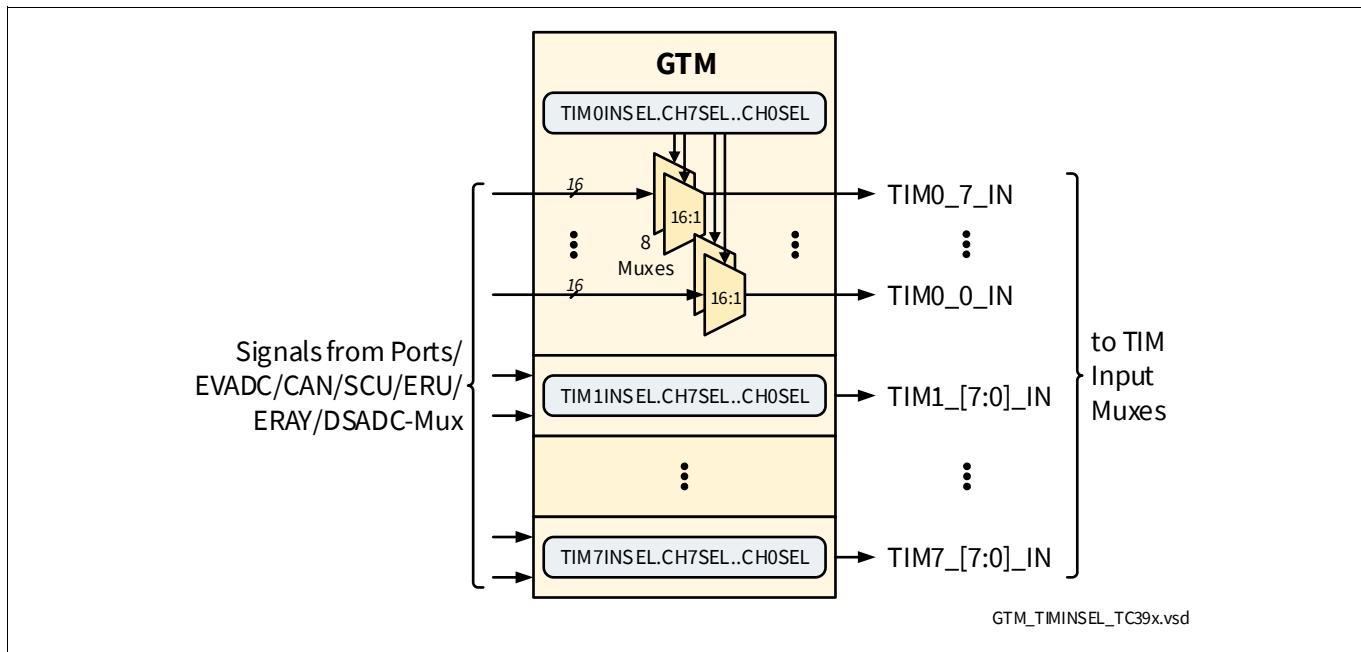
**GTM\_MCSI\_CH0\_PC (i=0-9)**MCSi Channel 0 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>) Application Reset Value: 0000 0000<sub>H</sub>**GTM\_MCSI\_CH1\_PC (i=0-9)**MCSi Channel 1 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>+80<sub>H</sub>) Application Reset Value: 0000 0004<sub>H</sub>**GTM\_MCSI\_CH2\_PC (i=0-9)**MCSi Channel 2 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>+100<sub>H</sub>) Application Reset Value: 0000 0008<sub>H</sub>**GTM\_MCSI\_CH3\_PC (i=0-9)**MCSi Channel 3 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>+180<sub>H</sub>) Application Reset Value: 0000 000C<sub>H</sub>**GTM\_MCSI\_CH4\_PC (i=0-9)**MCSi Channel 4 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>+200<sub>H</sub>) Application Reset Value: 0000 0010<sub>H</sub>**GTM\_MCSI\_CH5\_PC (i=0-9)**MCSi Channel 5 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>+280<sub>H</sub>) Application Reset Value: 0000 0014<sub>H</sub>**GTM\_MCSI\_CH6\_PC (i=0-9)**MCSi Channel 6 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>+300<sub>H</sub>) Application Reset Value: 0000 0018<sub>H</sub>**GTM\_MCSI\_CH7\_PC (i=0-9)**MCSi Channel 7 Program Counter Register(0F0040<sub>H</sub>+i\*1000<sub>H</sub>+380<sub>H</sub>) Application Reset Value: 0000 001C<sub>H</sub>

## Generic Timer Module (GTM)

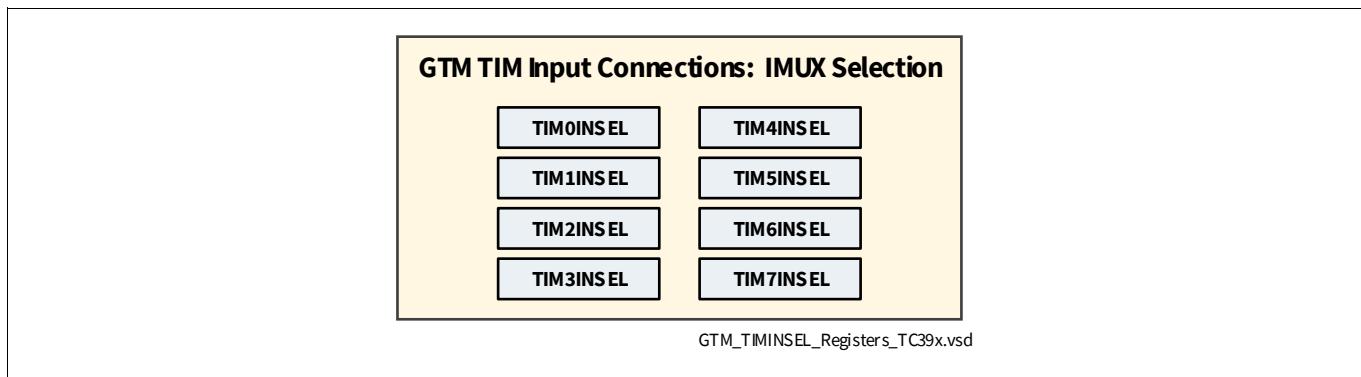
Field	Bits	Type	Description
<b>PC</b>	15:0	rw	<p><b>Current Program Counter</b></p> <p><i>Note: The program counter is only writable if the corresponding MCS-channel is disabled. The bits 0 and 1 are always written as zeros.</i></p> <p><i>Note: The actual width of the program counter depends on the MCS configuration. The actual width is RAW+USR+2 bits meaning that only the bits 0 to RAW+USR+1 are available and the other bits (RAW+USR+2 to 31) are reserved.</i></p>
<b>0</b>	31:16	r	<p><b>Reserved</b></p> <p>Read as zero, shall be written as zero.</p>

## Generic Timer Module (GTM)

### 26.3.2 Port to GTM TIM Connections



**Figure 10** Port to GTM TIM Connections Overview



**Figure 11** Port to GTM TIM Connections Registers Overview

**Table 332** Port to GTM TIM Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
TIM0INSEL	TIM0 Input Select Register (n=0)	CH0SEL..CH7SEL	<a href="#">Page 58</a>
TIM1INSEL	TIM1 Input Select Register (n=1)	CH0SEL..CH7SEL	<a href="#">Page 62</a>
TIM2INSEL	TIM2 Input Select Register (n=2)	CH0SEL..CH7SEL	<a href="#">Page 67</a>
TIM3INSEL	TIM3 Input Select Register (n=3)	CH0SEL..CH7SEL	<a href="#">Page 71</a>
TIM4INSEL	TIM4 Input Select Register (n=4)	CH0SEL..CH7SEL	<a href="#">Page 76</a>
TIM5INSEL	TIM5 Input Select Register (n=5)	CH0SEL..CH7SEL	<a href="#">Page 80</a>
TIM6INSEL	TIM6 Input Select Register (n=6)	CH0SEL..CH7SEL	<a href="#">Page 85</a>
TIM7INSEL	TIM7 Input Select Register (n=7)	CH0SEL..CH7SEL	<a href="#">Page 88</a>
TIMi_CHx_CTRL	TIMi Channel x Control Register (i=1-7;x=0-7)		<a href="#">Page 91</a>

## Generic Timer Module (GTM)

### TIMn Input Select Register

#### GTM\_TIMnINSEL (n=0)

##### TIMn Input Select Register

(09FD40<sub>H</sub>+n\*4)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>CH7SEL</b>				<b>CH6SEL</b>				<b>CH5SEL</b>				<b>CH4SEL</b>			
rw				rw				rw					rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CH3SEL</b>				<b>CH2SEL</b>				<b>CH1SEL</b>				<b>CH0SEL</b>			
rw				rw				rw					rw		

Field	Bits	Type	Description
<b>CHxSEL (x=0)</b>	4*x+3:4*x	rw	<b>TIM Channel x Input Selection</b> This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module. 0 <sub>H</sub> <b>FC0BFL</b> , EVADC boundary flag level of FC channel 0 1 <sub>H</sub> <b>P00.9</b> , Port pad input 2 <sub>H</sub> <b>P02.0</b> , Port pad input 3 <sub>H</sub> <b>P10.7</b> , Port pad input (no QFP144) 4 <sub>H</sub> <b>P14.5</b> , Port pad input 5 <sub>H</sub> <b>P14.7</b> , Port pad input (no QFP144) 6 <sub>H</sub> <b>P15.6</b> , Port pad input 7 <sub>H</sub> <b>P21.2</b> , Port pad input 8 <sub>H</sub> <b>P22.1</b> , Port pad input 9 <sub>H</sub> <b>P33.10</b> , Port pad input A <sub>H</sub> <b>P33.4</b> , Port pad input B <sub>H</sub> <b>P13.12</b> , Port pad input (BGA516 only) C <sub>H</sub> <b>PDOUT0</b> , SCU/ERU pattern detection output 0 D <sub>H</sub> Reserved, do not use E <sub>H</sub> <b>IMUX0_0</b> , DSADC input IMUX0_OUT0 F <sub>H</sub> <b>C0SR0</b> , EVADC service request 0 of common block 0

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=1)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC1BFL</b>, EVADC boundary flag level of FC channel 1</li> <li>1<sub>H</sub> <b>P00.10</b>, Port pad input (no QFP144)</li> <li>2<sub>H</sub> <b>P02.1</b>, Port pad input</li> <li>3<sub>H</sub> <b>P10.1</b>, Port pad input</li> <li>4<sub>H</sub> <b>P14.6</b>, Port pad input</li> <li>5<sub>H</sub> <b>P15.7</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.3</b>, Port pad input</li> <li>7<sub>H</sub> <b>P22.0</b>, Port pad input</li> <li>8<sub>H</sub> <b>P33.5</b>, Port pad input</li> <li>9<sub>H</sub> <b>P33.9</b>, Port pad input</li> <li>A<sub>H</sub> <b>P10.9</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>C<sub>H</sub> <b>PDOUT1</b>, SCU/ERU pattern detection output 1</li> <li>D<sub>H</sub> <b>INT_O12</b>, CAN interrupt output INT_O12</li> <li>E<sub>H</sub> <b>IMUX0_1</b>, DSADC input IMUX0_OUT1</li> <li>F<sub>H</sub> <b>C1SR0</b>, EVADC service request 0 of common block 1</li> </ul>
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC2BFL</b>, EVADC boundary flag level of FC channel 2</li> <li>1<sub>H</sub> <b>P00.11</b>, Port pad input (no QFP144)</li> <li>2<sub>H</sub> <b>P02.2</b>, Port pad input</li> <li>3<sub>H</sub> <b>P10.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P10.5</b>, Port pad input</li> <li>5<sub>H</sub> <b>P15.8</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.4</b>, Port pad input</li> <li>7<sub>H</sub> <b>P23.5</b>, Port pad input (no QFP144)</li> <li>8<sub>H</sub> <b>P33.11</b>, Port pad input</li> <li>9<sub>H</sub> <b>P33.6</b>, Port pad input</li> <li>A<sub>H</sub> <b>P02.9</b>, Port pad input (no QFP)</li> <li>B<sub>H</sub> <b>P10.10</b>, Port pad input (BGA516 only)</li> <li>C<sub>H</sub> <b>PDOUT2</b>, SCU/ERU pattern detection output 2</li> <li>D<sub>H</sub> <b>INT_O13</b>, CAN interrupt output INT_O13</li> <li>E<sub>H</sub> <b>IMUX0_2</b>, DSADC input IMUX0_OUT2</li> <li>F<sub>H</sub> <b>C0SR1</b>, EVADC service request 1 of common block 0</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC3BFL</b>, EVADC boundary flag level of FC channel 3</li> <li>1<sub>H</sub> <b>P00.12</b>, Port pad input</li> <li>2<sub>H</sub> <b>P02.3</b>, Port pad input</li> <li>3<sub>H</sub> <b>P10.3</b>, Port pad input</li> <li>4<sub>H</sub> <b>P10.6</b>, Port pad input</li> <li>5<sub>H</sub> <b>P14.0</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.5</b>, Port pad input</li> <li>7<sub>H</sub> <b>P22.2</b>, Port pad input</li> <li>8<sub>H</sub> <b>P32.2</b>, Port pad input (no QFP144)</li> <li>9<sub>H</sub> <b>P33.7</b>, Port pad input</li> <li>A<sub>H</sub> <b>P02.10</b>, Port pad input (no QFP)</li> <li>B<sub>H</sub> <b>P10.14</b>, Port pad input (BGA516 only)</li> <li>C<sub>H</sub> <b>PDOUT3</b>, SCU/ERU pattern detection output 3</li> <li>D<sub>H</sub> <b>INT_O14</b>, CAN interrupt output INT_O14</li> <li>E<sub>H</sub> <b>IMUX0_3</b>, DSADC input IMUX0_OUT3</li> <li>F<sub>H</sub> <b>C1SR1</b>, EVADC service request 1 of common block 1</li> </ul>
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC4BFL</b>, EVADC boundary flag level of FC channel 4</li> <li>1<sub>H</sub> <b>P02.4</b>, Port pad input</li> <li>2<sub>H</sub> <b>P10.0</b>, Port pad input (no QFP144)</li> <li>3<sub>H</sub> <b>P14.1</b>, Port pad input</li> <li>4<sub>H</sub> <b>P22.3</b>, Port pad input</li> <li>5<sub>H</sub> <b>P32.3</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P33.0</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P33.8</b>, Port pad input</li> <li>8<sub>H</sub> <b>P21.6</b>, Port pad input</li> <li>9<sub>H</sub> <b>P10.13</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> Reserved, do not use</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>C<sub>H</sub> <b>PDOUT4</b>, SCU/ERU pattern detection output 4</li> <li>D<sub>H</sub> <b>INT_O15</b>, CAN interrupt output INT_O15</li> <li>E<sub>H</sub> <b>IMUX0_4</b>, DSADC input IMUX0_OUT4</li> <li>F<sub>H</sub> <b>C0SR2</b>, EVADC service request 2 of common block 0</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC5BFL</b>, EVADC boundary flag level of FC channel 5</li> <li>1<sub>H</sub> <b>P02.5</b>, Port pad input</li> <li>2<sub>H</sub> <b>P10.8</b>, Port pad input (no QFP144)</li> <li>3<sub>H</sub> <b>P14.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P23.0</b>, Port pad input (no QFP144)</li> <li>5<sub>H</sub> <b>P32.4</b>, Port pad input</li> <li>6<sub>H</sub> <b>P33.1</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P21.7</b>, Port pad input</li> <li>8<sub>H</sub> <b>P01.3</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P10.11</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> Reserved, do not use</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>C<sub>H</sub> <b>PDOUT5</b>, SCU/ERU pattern detection output 5</li> <li>D<sub>H</sub> Reserved, do not use</li> <li>E<sub>H</sub> <b>IMUX0_5</b>, DSADC input IMUX0_OUT5</li> <li>F<sub>H</sub> <b>C1SR2</b>, EVADC service request 2 of common block 1</li> </ul>
<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC6BFL</b>, EVADC boundary flag level of FC channel 6</li> <li>1<sub>H</sub> <b>P02.6</b>, Port pad input</li> <li>2<sub>H</sub> <b>P10.4</b>, Port pad input (no QFP144)</li> <li>3<sub>H</sub> <b>P14.3</b>, Port pad input</li> <li>4<sub>H</sub> <b>P23.1</b>, Port pad input</li> <li>5<sub>H</sub> <b>P23.2</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P33.2</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P20.0</b>, Port pad input</li> <li>8<sub>H</sub> <b>P01.4</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P10.15</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> Reserved, do not use</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>C<sub>H</sub> <b>PDOUT6</b>, SCU/ERU pattern detection output 6</li> <li>D<sub>H</sub> Reserved, do not use</li> <li>E<sub>H</sub> <b>IMUX0_6</b>, DSADC input IMUX0_OUT6</li> <li>F<sub>H</sub> <b>C0SR3</b>, EVADC service request 3 of common block 0</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC7BFL</b>, EVADC boundary flag level of FC channel 7</li> <li>1<sub>H</sub> <b>P02.7</b>, Port pad input</li> <li>2<sub>H</sub> <b>P14.4</b>, Port pad input</li> <li>3<sub>H</sub> <b>P20.8</b>, Port pad input</li> <li>4<sub>H</sub> <b>P23.3</b>, Port pad input (no QFP144)</li> <li>5<sub>H</sub> <b>P23.4</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P33.3</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P02.11</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P11.15</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>WUTUFLOW</b>, PMS: Underflow output to support WUT calibration</li> <li>A<sub>H</sub> Reserved, do not use</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>C<sub>H</sub> <b>PDOUT7</b>, SCU/ERU pattern detection output 7</li> <li>D<sub>H</sub> <b>MTO</b>, ERAY0 macrotick clock from CC</li> <li>E<sub>H</sub> <b>IMUX0_7</b>, DSADC input IMUX0_OUT7</li> <li>F<sub>H</sub> <b>C1SR3</b>, EVADC service request 3 of common block 1</li> </ul>

### GTM\_TIMnINSEL (n=1)

# **TIMn Input Select Register**

(09FD40<sub>H</sub>+n\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>CH7SEL</b>				<b>CH6SEL</b>				<b>CH5SEL</b>				<b>CH4SEL</b>			
				rw				rw				rw			rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CH3SEL</b>				<b>CH2SEL</b>				<b>CH1SEL</b>				<b>CH0SEL</b>			
				rw				rw				rw			rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=0)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC0BFL</b>, EVADC boundary flag level of FC channel 0</li> <li>1<sub>H</sub> <b>P00.9</b>, Port pad input</li> <li>2<sub>H</sub> <b>P02.0</b>, Port pad input</li> <li>3<sub>H</sub> <b>P10.7</b>, Port pad input (no QFP144)</li> <li>4<sub>H</sub> <b>P14.5</b>, Port pad input</li> <li>5<sub>H</sub> <b>P14.7</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P15.6</b>, Port pad input</li> <li>7<sub>H</sub> <b>P21.2</b>, Port pad input</li> <li>8<sub>H</sub> <b>P22.1</b>, Port pad input</li> <li>9<sub>H</sub> <b>P33.10</b>, Port pad input</li> <li>A<sub>H</sub> <b>P33.4</b>, Port pad input</li> <li>B<sub>H</sub> <b>IMUX1_0</b>, DSADC input IMUX1_OUT0</li> <li>C<sub>H</sub> <b>C0SR2</b>, EVADC service request 2 of common block 0</li> <li>D<sub>H</sub> <b>CBFLOUT0</b>, EVADC common boundary flag output 0</li> <li>E<sub>H</sub> Reserved, do not use</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=1)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC1BFL</b>, EVADC boundary flag level of FC channel 1</li> <li>1<sub>H</sub> <b>P00.10</b>, Port pad input (no QFP144)</li> <li>2<sub>H</sub> <b>P02.1</b>, Port pad input</li> <li>3<sub>H</sub> <b>P10.1</b>, Port pad input</li> <li>4<sub>H</sub> <b>P14.6</b>, Port pad input</li> <li>5<sub>H</sub> <b>P15.7</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.3</b>, Port pad input</li> <li>7<sub>H</sub> <b>P22.0</b>, Port pad input</li> <li>8<sub>H</sub> <b>P33.5</b>, Port pad input</li> <li>9<sub>H</sub> <b>P33.9</b>, Port pad input</li> <li>A<sub>H</sub> Reserved, do not use</li> <li>B<sub>H</sub> <b>IMUX1_1</b>, DSADC input IMUX1_OUT1</li> <li>C<sub>H</sub> <b>C1SR2</b>, EVADC service request 2 of common block 1</li> <li>D<sub>H</sub> <b>INT_O12</b>, CAN interrupt output INT_O12</li> <li>E<sub>H</sub> <b>CBFLOUT1</b>, EVADC common boundary flag output 1</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC2BFL</b>, EVADC boundary flag level of FC channel 2</li> <li>1<sub>H</sub> <b>P00.11</b>, Port pad input (no QFP144)</li> <li>2<sub>H</sub> <b>P02.2</b>, Port pad input</li> <li>3<sub>H</sub> <b>P10.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P10.5</b>, Port pad input</li> <li>5<sub>H</sub> <b>P15.8</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.4</b>, Port pad input</li> <li>7<sub>H</sub> <b>P23.5</b>, Port pad input (no QFP144)</li> <li>8<sub>H</sub> <b>P33.11</b>, Port pad input</li> <li>9<sub>H</sub> <b>P33.6</b>, Port pad input</li> <li>A<sub>H</sub> <b>P23.6</b>, Port pad input (no QFP)</li> <li>B<sub>H</sub> <b>IMUX1_2</b>, DSADC input IMUX1_OUT2</li> <li>C<sub>H</sub> <b>C0SR3</b>, EVADC service request 3 of common block 0</li> <li>D<sub>H</sub> <b>INT_O13</b>, CAN interrupt output INT_O13</li> <li>E<sub>H</sub> <b>CBFLOUT2</b>, EVADC common boundary flag output 2</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC3BFL</b>, EVADC boundary flag level of FC channel 3</li> <li>1<sub>H</sub> <b>P00.12</b>, Port pad input</li> <li>2<sub>H</sub> <b>P02.3</b>, Port pad input</li> <li>3<sub>H</sub> <b>P10.3</b>, Port pad input</li> <li>4<sub>H</sub> <b>P10.6</b>, Port pad input</li> <li>5<sub>H</sub> <b>P14.0</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.5</b>, Port pad input</li> <li>7<sub>H</sub> <b>P22.2</b>, Port pad input</li> <li>8<sub>H</sub> <b>P32.2</b>, Port pad input (no QFP144)</li> <li>9<sub>H</sub> <b>P33.7</b>, Port pad input</li> <li>A<sub>H</sub> <b>P23.7</b>, Port pad input (no QFP)</li> <li>B<sub>H</sub> <b>CBFLOUT3</b>, EVADC common boundary flag output 3</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>INT_O14</b>, CAN interrupt output INT_O14</li> <li>E<sub>H</sub> <b>IMUX1_3</b>, DSADC input IMUX1_OUT3</li> <li>F<sub>H</sub> <b>C1SR3</b>, EVADC service request 3 of common block 1</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC4BFL</b>, EVADC boundary flag level of FC channel 4</li> <li>1<sub>H</sub> <b>P02.4</b>, Port pad input</li> <li>2<sub>H</sub> <b>P10.0</b>, Port pad input (no QFP144)</li> <li>3<sub>H</sub> <b>P14.1</b>, Port pad input</li> <li>4<sub>H</sub> <b>P22.3</b>, Port pad input</li> <li>5<sub>H</sub> <b>P32.3</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P33.0</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P33.8</b>, Port pad input</li> <li>8<sub>H</sub> <b>P21.6</b>, Port pad input</li> <li>9<sub>H</sub> <b>P20.0</b>, Port pad input</li> <li>A<sub>H</sub> <b>C0SR0</b>, EVADC service request 0 of common block 0</li> <li>B<sub>H</sub> <b>CBFLOUT0</b>, EVADC common boundary flag output 0</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>INT_O15</b>, CAN interrupt output INT_O15</li> <li>E<sub>H</sub> <b>IMUX1_4</b>, DSADC input IMUX1_OUT4</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC5BFL</b>, EVADC boundary flag level of FC channel 5</li> <li>1<sub>H</sub> <b>P02.5</b>, Port pad input</li> <li>2<sub>H</sub> <b>P10.8</b>, Port pad input (no QFP144)</li> <li>3<sub>H</sub> <b>P14.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P23.0</b>, Port pad input (no QFP144)</li> <li>5<sub>H</sub> <b>P32.4</b>, Port pad input</li> <li>6<sub>H</sub> <b>P33.1</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P21.7</b>, Port pad input</li> <li>8<sub>H</sub> <b>P20.7</b>, Port pad input</li> <li>9<sub>H</sub> <b>CBFLOUT1</b>, EVADC common boundary flag output 1</li> <li>A<sub>H</sub> <b>C1SR0</b>, EVADC service request 0 of common block 1</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>D<sub>H</sub> Reserved, do not use</li> <li>E<sub>H</sub> <b>IMUX1_5</b>, DSADC input IMUX1_OUT5</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC6BFL</b>, EVADC boundary flag level of FC channel 6</li> <li>1<sub>H</sub> <b>P02.6</b>, Port pad input</li> <li>2<sub>H</sub> <b>P10.4</b>, Port pad input (no QFP144)</li> <li>3<sub>H</sub> <b>P14.3</b>, Port pad input</li> <li>4<sub>H</sub> <b>P23.1</b>, Port pad input</li> <li>5<sub>H</sub> <b>P23.2</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P33.2</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P20.0</b>, Port pad input</li> <li>8<sub>H</sub> <b>CBFLOUT2</b>, EVADC common boundary flag output 2</li> <li>9<sub>H</sub> Reserved, do not use</li> <li>A<sub>H</sub> <b>C0SR1</b>, EVADC service request 1 of common block 0</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>D<sub>H</sub> Reserved, do not use</li> <li>E<sub>H</sub> <b>IMUX1_6</b>, DSADC input IMUX1_OUT6</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC7BFL</b>, EVADC boundary flag level of FC channel 7</li> <li>1<sub>H</sub> <b>P02.7</b>, Port pad input</li> <li>2<sub>H</sub> <b>P14.4</b>, Port pad input</li> <li>3<sub>H</sub> <b>P20.8</b>, Port pad input</li> <li>4<sub>H</sub> <b>P23.3</b>, Port pad input (no QFP144)</li> <li>5<sub>H</sub> <b>P23.4</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P33.3</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>CBFLOUT3</b>, EVADC common boundary flag output 3</li> <li>8<sub>H</sub> Reserved, do not use</li> <li>9<sub>H</sub> Reserved, do not use</li> <li>A<sub>H</sub> <b>C1SR1</b>, EVADC service request 1 of common block 1</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>MT0</b>, ERAY0 macrotick clock from CC</li> <li>E<sub>H</sub> <b>IMUX1_7</b>, DSADC input IMUX1_OUT7</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

## GTM\_TIMnINSEL (n=2)

## TIMn Input Select Register

(09FD40<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

CH7SEL	rw	CH6SEL	rw	CH5SEL	rw	CH4SEL	rw

CH3SEL	rw	CH2SEL	rw	CH1SEL	rw	CHOSEL	rw

Field	Bits	Type	Description
CHxSEL (x=0)	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC0BFL</b>, EVADC boundary flag level of FC channel 0</li> <li>1<sub>H</sub> <b>P00.0</b>, Port pad input</li> <li>2<sub>H</sub> <b>P02.8</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.3</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.5</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.12</b>, Port pad input</li> <li>6<sub>H</sub> <b>P33.12</b>, Port pad input</li> <li>7<sub>H</sub> <b>P11.0</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P33.14</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P11.10</b>, Port pad input</li> <li>A<sub>H</sub> <b>C0SR0</b>, EVADC service request 0 of common block 0</li> <li>B<sub>H</sub> <b>IMUX2_0</b>, DSADC input IMUX2_OUT0</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>P31.0</b>, Port pad input (BGA516 only)</li> <li>E<sub>H</sub> <b>P01.3</b>, Port pad input (no QFP)</li> <li>F<sub>H</sub> <b>CBFLOUT0</b>, EVADC common boundary flag output 0</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=1)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC1BFL</b>, EVADC boundary flag level of FC channel 1</li> <li>1<sub>H</sub> <b>P00.1</b>, Port pad input</li> <li>2<sub>H</sub> <b>P00.2</b>, Port pad input</li> <li>3<sub>H</sub> <b>P11.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P20.13</b>, Port pad input</li> <li>5<sub>H</sub> <b>P33.13</b>, Port pad input</li> <li>6<sub>H</sub> <b>P11.1</b>, Port pad input (no QFP)</li> <li>7<sub>H</sub> <b>P33.15</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P15.10</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P31.1</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>C1SR0</b>, EVADC service request 0 of common block 1</li> <li>B<sub>H</sub> <b>IMUX2_1</b>, DSADC input IMUX2_OUT1</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>INT_O12</b>, CAN interrupt output INT_O12</li> <li>E<sub>H</sub> <b>P01.4</b>, Port pad input (no QFP)</li> <li>F<sub>H</sub> <b>CBFLOUT1</b>, EVADC common boundary flag output 1</li> </ul>
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC2BFL</b>, EVADC boundary flag level of FC channel 2</li> <li>1<sub>H</sub> <b>P00.3</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.3</b>, Port pad input</li> <li>3<sub>H</sub> <b>P14.8</b>, Port pad input (no QFP144)</li> <li>4<sub>H</sub> <b>P20.14</b>, Port pad input</li> <li>5<sub>H</sub> <b>P32.0</b>, Port pad input</li> <li>6<sub>H</sub> <b>P11.4</b>, Port pad input (no QFP)</li> <li>7<sub>H</sub> <b>P01.5</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P15.11</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P31.2</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>C0SR1</b>, EVADC service request 1 of common block 0</li> <li>B<sub>H</sub> <b>IMUX2_2</b>, DSADC input IMUX2_OUT2</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>INT_O13</b>, CAN interrupt output INT_O13</li> <li>E<sub>H</sub> <b>P15.6</b>, Port pad input</li> <li>F<sub>H</sub> <b>CBFLOUT2</b>, EVADC common boundary flag output 2</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC3BFL</b>, EVADC boundary flag level of FC channel 3</li> <li>1<sub>H</sub> <b>P00.4</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.6</b>, Port pad input</li> <li>3<sub>H</sub> <b>P14.9</b>, Port pad input (no QFP144)</li> <li>4<sub>H</sub> <b>P15.0</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.1</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P15.12</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P01.5</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P11.5</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P34.1</b>, Port pad input (no QFP)</li> <li>A<sub>H</sub> <b>C1SR1</b>, EVADC service request 1 of common block 1</li> <li>B<sub>H</sub> <b>IMUX2_3</b>, DSADC input IMUX2_OUT3</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>INT_O14</b>, CAN interrupt output INT_O14</li> <li>E<sub>H</sub> <b>P31.3</b>, Port pad input (BGA516 only)</li> <li>F<sub>H</sub> <b>CBFLOUT3</b>, EVADC common boundary flag output 3</li> </ul>
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC4BFL</b>, EVADC boundary flag level of FC channel 4</li> <li>1<sub>H</sub> <b>P00.5</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.9</b>, Port pad input</li> <li>3<sub>H</sub> <b>P14.10</b>, Port pad input (no QFP144)</li> <li>4<sub>H</sub> <b>P15.1</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.3</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.0</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P11.7</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P34.2</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P15.13</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>C0SR2</b>, EVADC service request 2 of common block 0</li> <li>B<sub>H</sub> <b>IMUX2_4</b>, DSADC input IMUX2_OUT4</li> <li>C<sub>H</sub> <b>P31.4</b>, Port pad input (BGA516 only)</li> <li>D<sub>H</sub> <b>INT_O15</b>, CAN interrupt output INT_O15</li> <li>E<sub>H</sub> <b>P02.14</b>, Port pad input (BGA516 only)</li> <li>F<sub>H</sub> <b>CBFLOUT0</b>, EVADC common boundary flag output 0</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC5BFL</b>, EVADC boundary flag level of FC channel 5</li> <li>1<sub>H</sub> <b>P00.6</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.10</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.0</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.2</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.9</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.1</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P01.6</b>, Port pad input</li> <li>8<sub>H</sub> <b>P11.8</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P34.3</b>, Port pad input (no QFP)</li> <li>A<sub>H</sub> <b>C1SR2</b>, EVADC service request 2 of common block 1</li> <li>B<sub>H</sub> <b>IMUX2_5</b>, DSADC input IMUX2_OUT5</li> <li>C<sub>H</sub> <b>P15.14</b>, Port pad input (BGA516 only)</li> <li>D<sub>H</sub> <b>P31.5</b>, Port pad input (BGA516 only)</li> <li>E<sub>H</sub> <b>P02.15</b>, Port pad input (BGA516 only)</li> <li>F<sub>H</sub> <b>CBFLOUT1</b>, EVADC common boundary flag output 1</li> </ul>
<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC6BFL</b>, EVADC boundary flag level of FC channel 6</li> <li>1<sub>H</sub> <b>P00.7</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.11</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.1</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.3</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.6</b>, Port pad input</li> <li>6<sub>H</sub> <b>P20.10</b>, Port pad input</li> <li>7<sub>H</sub> <b>P11.13</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P34.4</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P15.15</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>C0SR3</b>, EVADC service request 3 of common block 0</li> <li>B<sub>H</sub> <b>IMUX2_6</b>, DSADC input IMUX2_OUT6</li> <li>C<sub>H</sub> <b>P31.6</b>, Port pad input (BGA516 only)</li> <li>D<sub>H</sub> <b>P01.0</b>, Port pad input</li> <li>E<sub>H</sub> <b>P22.6</b>, Port pad input (no QFP)</li> <li>F<sub>H</sub> <b>CBFLOUT2</b>, EVADC common boundary flag output 2</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC7BFL</b>, EVADC boundary flag level of FC channel 7</li> <li>1<sub>H</sub> <b>P00.8</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.12</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.4</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.7</b>, Port pad input</li> <li>6<sub>H</sub> <b>P20.11</b>, Port pad input</li> <li>7<sub>H</sub> <b>P01.7</b>, Port pad input</li> <li>8<sub>H</sub> <b>P11.14</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P34.5</b>, Port pad input (no QFP)</li> <li>A<sub>H</sub> <b>C1SR3</b>, EVADC service request 3 of common block 1</li> <li>B<sub>H</sub> <b>IMUX2_7</b>, DSADC input IMUX2_OUT7</li> <li>C<sub>H</sub> <b>P13.9</b>, Port pad input (BGA516 only)</li> <li>D<sub>H</sub> <b>MTO</b>, ERAY0 macrotick clock from CC</li> <li>E<sub>H</sub> <b>P31.7</b>, Port pad input (BGA516 only)</li> <li>F<sub>H</sub> <b>CBFLOUT3</b>, EVADC common boundary flag output 3</li> </ul>

**GTM\_TIMnINSEL (n=3)**

## **TIMn Input Select Register**

(09FD40<sub>H</sub>+n\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=0)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P00.0</b>, Port pad input</li> <li>2<sub>H</sub> <b>P02.8</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.3</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.5</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.12</b>, Port pad input</li> <li>6<sub>H</sub> <b>P33.12</b>, Port pad input</li> <li>7<sub>H</sub> <b>P12.0</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P22.4</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P13.11</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P02.6</b>, Port pad input</li> <li>B<sub>H</sub> <b>P00.5</b>, Port pad input</li> <li>C<sub>H</sub> <b>P25.0</b>, Port pad input (BGA516 only)</li> <li>D<sub>H</sub> <b>P33.0</b>, Port pad input (no QFP144)</li> <li>E<sub>H</sub> <b>P11.11</b>, Port pad input</li> <li>F<sub>H</sub> <b>IMUX3_0</b>, DSADC input IMUX3_OUT0</li> </ul>
<b>CHxSEL (x=1)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>IMUX3_1</b>, DSADC input IMUX3_OUT1</li> <li>1<sub>H</sub> <b>P00.1</b>, Port pad input</li> <li>2<sub>H</sub> <b>P00.2</b>, Port pad input</li> <li>3<sub>H</sub> <b>P11.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P20.13</b>, Port pad input</li> <li>5<sub>H</sub> <b>P33.13</b>, Port pad input</li> <li>6<sub>H</sub> <b>P12.1</b>, Port pad input (no QFP)</li> <li>7<sub>H</sub> <b>P22.5</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P13.10</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P14.11</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P02.7</b>, Port pad input</li> <li>B<sub>H</sub> <b>P25.1</b>, Port pad input (BGA516 only)</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>INT_O12</b>, CAN interrupt output INT_O12</li> <li>E<sub>H</sub> <b>P00.6</b>, Port pad input</li> <li>F<sub>H</sub> <b>P33.1</b>, Port pad input (no QFP144)</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P00.3</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.3</b>, Port pad input</li> <li>3<sub>H</sub> <b>P14.8</b>, Port pad input (no QFP144)</li> <li>4<sub>H</sub> <b>P20.14</b>, Port pad input</li> <li>5<sub>H</sub> <b>P32.0</b>, Port pad input</li> <li>6<sub>H</sub> <b>P22.6</b>, Port pad input (no QFP)</li> <li>7<sub>H</sub> <b>P13.14</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P14.14</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P25.2</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P02.8</b>, Port pad input</li> <li>B<sub>H</sub> <b>P00.7</b>, Port pad input</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>INT_O13</b>, CAN interrupt output INT_O13</li> <li>E<sub>H</sub> <b>P33.2</b>, Port pad input (no QFP144)</li> <li>F<sub>H</sub> <b>IMUX3_2</b>, DSADC input IMUX3_OUT2</li> </ul>
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC3BFL</b>, EVADC boundary flag level of FC channel 3</li> <li>1<sub>H</sub> <b>P00.4</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.6</b>, Port pad input</li> <li>3<sub>H</sub> <b>P14.9</b>, Port pad input (no QFP144)</li> <li>4<sub>H</sub> <b>P15.0</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.1</b>, Port pad input (no QFP144)</li> <li>6<sub>H</sub> <b>P14.13</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P22.7</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P13.4</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P25.3</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P02.9</b>, Port pad input (no QFP)</li> <li>B<sub>H</sub> <b>P00.8</b>, Port pad input</li> <li>C<sub>H</sub> <b>P33.3</b>, Port pad input (no QFP144)</li> <li>D<sub>H</sub> <b>INT_O14</b>, CAN interrupt output INT_O14</li> <li>E<sub>H</sub> <b>IMUX3_3</b>, DSADC input IMUX3_OUT3</li> <li>F<sub>H</sub> <b>P32.1</b>, Port pad input</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC4BFL</b>, EVADC boundary flag level of FC channel 4</li> <li>1<sub>H</sub> <b>P00.5</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.9</b>, Port pad input</li> <li>3<sub>H</sub> <b>P14.10</b>, Port pad input (no QFP144)</li> <li>4<sub>H</sub> <b>P15.1</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.3</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.0</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P22.8</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P14.12</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P13.5</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P25.4</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>P02.10</b>, Port pad input (no QFP)</li> <li>C<sub>H</sub> <b>P34.1</b>, Port pad input (no QFP)</li> <li>D<sub>H</sub> <b>INT_O15</b>, CAN interrupt output INT_O15</li> <li>E<sub>H</sub> <b>IMUX3_4</b>, DSADC input IMUX3_OUT4</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC5BFL</b>, EVADC boundary flag level of FC channel 5</li> <li>1<sub>H</sub> <b>P00.6</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.10</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.0</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.2</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.9</b>, Port pad input</li> <li>6<sub>H</sub> <b>P21.1</b>, Port pad input (no QFP144)</li> <li>7<sub>H</sub> <b>P22.9</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P32.5</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P13.13</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P13.6</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>P25.5</b>, Port pad input (BGA516 only)</li> <li>C<sub>H</sub> <b>P02.11</b>, Port pad input (no QFP)</li> <li>D<sub>H</sub> <b>P34.2</b>, Port pad input (no QFP)</li> <li>E<sub>H</sub> <b>IMUX3_5</b>, DSADC input IMUX3_OUT5</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC6BFL</b>, EVADC boundary flag level of FC channel 6</li> <li>1<sub>H</sub> <b>P00.7</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.11</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.1</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.3</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.6</b>, Port pad input</li> <li>6<sub>H</sub> <b>P20.10</b>, Port pad input</li> <li>7<sub>H</sub> <b>P22.10</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P32.6</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P14.15</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P13.7</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>P26.0</b>, Port pad input (BGA516 only)</li> <li>C<sub>H</sub> <b>P02.12</b>, Port pad input (BGA516 only)</li> <li>D<sub>H</sub> <b>P34.3</b>, Port pad input (no QFP)</li> <li>E<sub>H</sub> <b>P25.6</b>, Port pad input (BGA516 only)</li> <li>F<sub>H</sub> <b>IMUX3_6</b>, DSADC input IMUX3_OUT6</li> </ul>
<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC7BFL</b>, EVADC boundary flag level of FC channel 7</li> <li>1<sub>H</sub> <b>P00.8</b>, Port pad input</li> <li>2<sub>H</sub> <b>P11.12</b>, Port pad input</li> <li>3<sub>H</sub> <b>P13.2</b>, Port pad input</li> <li>4<sub>H</sub> <b>P15.4</b>, Port pad input</li> <li>5<sub>H</sub> <b>P20.7</b>, Port pad input</li> <li>6<sub>H</sub> <b>P20.11</b>, Port pad input</li> <li>7<sub>H</sub> <b>P22.11</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P32.7</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P13.15</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P25.7</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>P02.13</b>, Port pad input (BGA516 only)</li> <li>C<sub>H</sub> <b>P34.4</b>, Port pad input (no QFP)</li> <li>D<sub>H</sub> <b>MT0</b>, ERAY0 macrotick clock from CC</li> <li>E<sub>H</sub> <b>IMUX3_7</b>, DSADC input IMUX3_OUT7</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

## GTM\_TIMnINSEL (n=4)

TIMn Input Select Register

(09FD40<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

CH7SEL	rw	CH6SEL	rw	CH5SEL	rw	CH4SEL	rw

CH3SEL	rw	CH2SEL	rw	CH1SEL	rw	CHOSEL	rw

Field	Bits	Type	Description
CHxSEL (x=0)	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> <b>FC0BFL</b>, EVADC boundary flag level of FC channel 0</p> <p>1<sub>H</sub> <b>P00.13</b>, Port pad input (BGA516 only)</p> <p>2<sub>H</sub> <b>P01.12</b>, Port pad input (BGA516 only)</p> <p>3<sub>H</sub> <b>P02.12</b>, Port pad input (BGA516 only)</p> <p>4<sub>H</sub> <b>P11.0</b>, Port pad input (no QFP)</p> <p>5<sub>H</sub> <b>P12.0</b>, Port pad input (no QFP)</p> <p>6<sub>H</sub> <b>P13.12</b>, Port pad input (BGA516 only)</p> <p>7<sub>H</sub> <b>P00.9</b>, Port pad input</p> <p>8<sub>H</sub> <b>P24.0</b>, Port pad input (BGA516 only)</p> <p>9<sub>H</sub> <b>P25.8</b>, Port pad input (BGA516 only)</p> <p>A<sub>H</sub> <b>P30.0</b>, Port pad input (BGA516 only)</p> <p>B<sub>H</sub> <b>P21.0</b>, Port pad input (no QFP144)</p> <p>C<sub>H</sub> <b>P10.0</b>, Port pad input (no QFP144)</p> <p>D<sub>H</sub> <b>P10.8</b>, Port pad input (no QFP144)</p> <p>E<sub>H</sub> <b>IMUX4_0</b>, DSADC input IMUX4_OUT0</p> <p>F<sub>H</sub> <b>P32.7</b>, Port pad input (no QFP)</p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=1)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC1BFL</b>, EVADC boundary flag level of FC channel 1</li> <li>1<sub>H</sub> <b>P00.15</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P01.1</b>, Port pad input(BGA516 only)</li> <li>3<sub>H</sub> <b>P02.15</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P10.9</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P11.1</b>, Port pad input (no QFP)</li> <li>6<sub>H</sub> <b>P12.1</b>, Port pad input (no QFP)</li> <li>7<sub>H</sub> <b>P15.10</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P24.1</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P25.9</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P30.1</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>P00.10</b>, Port pad input (no QFP144)</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>D<sub>H</sub> <b>P21.1</b>, Port pad input (no QFP144)</li> <li>E<sub>H</sub> <b>P32.5</b>, Port pad input (no QFP)</li> <li>F<sub>H</sub> <b>IMUX4_1</b>, DSADC input IMUX4_OUT1</li> </ul>
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC2BFL</b>, EVADC boundary flag level of FC channel 2</li> <li>1<sub>H</sub> <b>P01.9</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P02.9</b>, Port pad input (no QFP)</li> <li>3<sub>H</sub> <b>P02.13</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P10.10</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P11.4</b>, Port pad input (no QFP)</li> <li>6<sub>H</sub> <b>P15.11</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P23.6</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P24.2</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P25.10</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P30.2</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>P00.11</b>, Port pad input (no QFP144)</li> <li>C<sub>H</sub> <b>P21.6</b>, Port pad input</li> <li>D<sub>H</sub> <b>P10.6</b>, Port pad input</li> <li>E<sub>H</sub> <b>IMUX4_2</b>, DSADC input IMUX4_OUT2</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC3BFL</b>, EVADC boundary flag level of FC channel 3</li> <li>1<sub>H</sub> <b>P01.13</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P02.10</b>, Port pad input (no QFP)</li> <li>3<sub>H</sub> <b>P02.14</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P10.14</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P11.5</b>, Port pad input (no QFP)</li> <li>6<sub>H</sub> <b>P15.12</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P23.7</b>, Port pad input (no QFP)</li> <li>8<sub>H</sub> <b>P24.3</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P25.11</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P30.3</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>P00.12</b>, Port pad input</li> <li>C<sub>H</sub> <b>P21.7</b>, Port pad input</li> <li>D<sub>H</sub> <b>P10.5</b>, Port pad input</li> <li>E<sub>H</sub> <b>IMUX4_3</b>, DSADC input IMUX4_OUT3</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC4BFL</b>, EVADC boundary flag level of FC channel 4</li> <li>1<sub>H</sub> <b>P01.0</b>, Port pad input</li> <li>2<sub>H</sub> <b>P01.8</b>, Port pad input (BGA516 only)</li> <li>3<sub>H</sub> <b>P02.11</b>, Port pad input (no QFP)</li> <li>4<sub>H</sub> <b>P10.13</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P11.7</b>, Port pad input (no QFP)</li> <li>6<sub>H</sub> <b>P15.13</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P24.4</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P25.12</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P30.4</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P33.4</b>, Port pad input</li> <li>B<sub>H</sub> <b>P20.1</b>, Port pad input (no QFP144)</li> <li>C<sub>H</sub> <b>P10.1</b>, Port pad input</li> <li>D<sub>H</sub> <b>IMUX4_4</b>, DSADC input IMUX4_OUT4</li> <li>E<sub>H</sub> <b>P33.10</b>, Port pad input</li> <li>F<sub>H</sub> <b>P32.6</b>, Port pad input (no QFP)</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC5BFL</b>, EVADC boundary flag level of FC channel 5</li> <li>1<sub>H</sub> <b>P01.2</b>, Port pad input</li> <li>2<sub>H</sub> <b>P01.3</b>, Port pad input (no QFP)</li> <li>3<sub>H</sub> <b>P01.10</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P10.11</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P11.8</b>, Port pad input (no QFP)</li> <li>6<sub>H</sub> <b>P15.14</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P24.5</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P25.13</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P30.5</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P33.5</b>, Port pad input</li> <li>B<sub>H</sub> <b>P20.3</b>, Port pad input</li> <li>C<sub>H</sub> <b>P10.2</b>, Port pad input</li> <li>D<sub>H</sub> <b>IMUX4_5</b>, DSADC input IMUX4_OUT5</li> <li>E<sub>H</sub> <b>P33.14</b>, Port pad input (no QFP)</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>FC6BFL</b>, EVADC boundary flag level of FC channel 6</li> <li>1<sub>H</sub> <b>P01.15</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P01.4</b>, Port pad input (no QFP)</li> <li>3<sub>H</sub> <b>P01.14</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P10.15</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P11.13</b>, Port pad input (no QFP)</li> <li>6<sub>H</sub> <b>P15.15</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P24.6</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P25.14</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P30.6</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P10.3</b>, Port pad input</li> <li>B<sub>H</sub> <b>IMUX4_6</b>, DSADC input IMUX4_OUT6</li> <li>C<sub>H</sub> <b>P33.15</b>, Port pad input (no QFP)</li> <li>D<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																																
<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>FC7BFL</b>, EVADC boundary flag level of FC channel 7</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>P00.14</b>, Port pad input (BGA516 only)</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>P01.11</b>, Port pad input (BGA516 only)</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>P10.4</b>, Port pad input (no QFP144)</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>P11.14</b>, Port pad input (no QFP)</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>P11.15</b>, Port pad input (no QFP)</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>P13.9</b>, Port pad input (BGA516 only)</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>P24.7</b>, Port pad input (BGA516 only)</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>P25.15</b>, Port pad input (BGA516 only)</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>P30.7</b>, Port pad input (BGA516 only)</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>P14.7</b>, Port pad input (no QFP144)</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>IMUX4_7</b>, DSADC input IMUX4_OUT7</td> </tr> <tr> <td>C<sub>H</sub></td> <td><b>P34.5</b>, Port pad input (no QFP)</td> </tr> <tr> <td>D<sub>H</sub></td> <td><b>MT1</b>, ERAY1 macrotick clock from CC</td> </tr> <tr> <td>E<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>F<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>FC7BFL</b> , EVADC boundary flag level of FC channel 7	1 <sub>H</sub>	<b>P00.14</b> , Port pad input (BGA516 only)	2 <sub>H</sub>	<b>P01.11</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P10.4</b> , Port pad input (no QFP144)	4 <sub>H</sub>	<b>P11.14</b> , Port pad input (no QFP)	5 <sub>H</sub>	<b>P11.15</b> , Port pad input (no QFP)	6 <sub>H</sub>	<b>P13.9</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	<b>P24.7</b> , Port pad input (BGA516 only)	8 <sub>H</sub>	<b>P25.15</b> , Port pad input (BGA516 only)	9 <sub>H</sub>	<b>P30.7</b> , Port pad input (BGA516 only)	A <sub>H</sub>	<b>P14.7</b> , Port pad input (no QFP144)	B <sub>H</sub>	<b>IMUX4_7</b> , DSADC input IMUX4_OUT7	C <sub>H</sub>	<b>P34.5</b> , Port pad input (no QFP)	D <sub>H</sub>	<b>MT1</b> , ERAY1 macrotick clock from CC	E <sub>H</sub>	Reserved, do not use	F <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>FC7BFL</b> , EVADC boundary flag level of FC channel 7																																		
1 <sub>H</sub>	<b>P00.14</b> , Port pad input (BGA516 only)																																		
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8 <sub>H</sub>	<b>P25.15</b> , Port pad input (BGA516 only)																																		
9 <sub>H</sub>	<b>P30.7</b> , Port pad input (BGA516 only)																																		
A <sub>H</sub>	<b>P14.7</b> , Port pad input (no QFP144)																																		
B <sub>H</sub>	<b>IMUX4_7</b> , DSADC input IMUX4_OUT7																																		
C <sub>H</sub>	<b>P34.5</b> , Port pad input (no QFP)																																		
D <sub>H</sub>	<b>MT1</b> , ERAY1 macrotick clock from CC																																		
E <sub>H</sub>	Reserved, do not use																																		
F <sub>H</sub>	Reserved, do not use																																		

### GTM\_TIMnINSEL (n=5)

# **TIMn Input Select Register**

(09FD40<sub>H</sub>+n\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>CH7SEL</b>				<b>CH6SEL</b>				<b>CH5SEL</b>				<b>CH4SEL</b>			
				rw				rw				rw			rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CH3SEL</b>				<b>CH2SEL</b>				<b>CH1SEL</b>				<b>CH0SEL</b>			
				rw				rw				rw			rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=0)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P00.13</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P01.12</b>, Port pad input (BGA516 only)</li> <li>3<sub>H</sub> <b>P02.12</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P22.8</b>, Port pad input (no QFP)</li> <li>5<sub>H</sub> <b>P24.8</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P30.8</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P31.8</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P33.14</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P13.11</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> <b>P01.8</b>, Port pad input (BGA516 only)</li> <li>B<sub>H</sub> <b>IMUX5_0</b>, DSADC input IMUX5_OUT0</li> <li>C<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=1)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P00.15</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P01.1</b>, Port pad input (BGA516 only)</li> <li>3<sub>H</sub> <b>P02.15</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P14.11</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P13.10</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P24.9</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P30.9</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P31.9</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P33.15</b>, Port pad input (no QFP)</li> <li>A<sub>H</sub> <b>P22.9</b>, Port pad input (no QFP)</li> <li>B<sub>H</sub> <b>P01.9</b>, Port pad input (BGA516 only)</li> <li>C<sub>H</sub> <b>IMUX5_1</b>, DSADC input IMUX5_OUT1</li> <li>D<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P01.9</b>, Port pad input (BGA516 only)      2<sub>H</sub> <b>P02.13</b>, Port pad input (BGA516 only)      3<sub>H</sub> <b>P14.14</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P13.14</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P24.10</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P30.10</b>, Port pad input (BGA516 only)      7<sub>H</sub> <b>P31.10</b>, Port pad input (BGA516 only)      8<sub>H</sub> <b>P22.10</b>, Port pad input (no QFP)      9<sub>H</sub> <b>P01.10</b>, Port pad input (BGA516 only)      A<sub>H</sub> <b>IMUX5_2</b>, DSADC input IMUX5_OUT2      B<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P01.13</b>, Port pad input (BGA516 only)      2<sub>H</sub> <b>P01.5</b>, Port pad input (no QFP)      3<sub>H</sub> <b>P02.14</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P13.4</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P14.13</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P24.11</b>, Port pad input (BGA516 only)      7<sub>H</sub> <b>P30.11</b>, Port pad input (BGA516 only)      8<sub>H</sub> <b>P31.11</b>, Port pad input (BGA516 only)      9<sub>H</sub> <b>P34.1</b>, Port pad input (no QFP)      A<sub>H</sub> <b>P22.11</b>, Port pad input (no QFP)      B<sub>H</sub> <b>P01.11</b>, Port pad input (BGA516 only)      C<sub>H</sub> <b>IMUX5_3</b>, DSADC input IMUX5_OUT3      D<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																																
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P01.0</b>, Port pad input</td></tr> <tr><td>2<sub>H</sub></td><td><b>P01.8</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>IMUX5_4</b>, DSADC input IMUX5_OUT4</td></tr> <tr><td>4<sub>H</sub></td><td><b>P13.5</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P14.12</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td><b>P24.12</b>, Port pad input (BGA516 only)</td></tr> <tr><td>7<sub>H</sub></td><td><b>P30.12</b>, Port pad input (BGA516 only)</td></tr> <tr><td>8<sub>H</sub></td><td><b>P31.12</b>, Port pad input (BGA516 only)</td></tr> <tr><td>9<sub>H</sub></td><td><b>P34.2</b>, Port pad input (no QFP)</td></tr> <tr><td>A<sub>H</sub></td><td><b>P00.0</b>, Port pad input</td></tr> <tr><td>B<sub>H</sub></td><td><b>P21.2</b>, Port pad input</td></tr> <tr><td>C<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P01.0</b> , Port pad input	2 <sub>H</sub>	<b>P01.8</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>IMUX5_4</b> , DSADC input IMUX5_OUT4	4 <sub>H</sub>	<b>P13.5</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P14.12</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	<b>P24.12</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	<b>P30.12</b> , Port pad input (BGA516 only)	8 <sub>H</sub>	<b>P31.12</b> , Port pad input (BGA516 only)	9 <sub>H</sub>	<b>P34.2</b> , Port pad input (no QFP)	A <sub>H</sub>	<b>P00.0</b> , Port pad input	B <sub>H</sub>	<b>P21.2</b> , Port pad input	C <sub>H</sub>	Reserved, do not use	...		F <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	Reserved, do not use																																		
1 <sub>H</sub>	<b>P01.0</b> , Port pad input																																		
2 <sub>H</sub>	<b>P01.8</b> , Port pad input (BGA516 only)																																		
3 <sub>H</sub>	<b>IMUX5_4</b> , DSADC input IMUX5_OUT4																																		
4 <sub>H</sub>	<b>P13.5</b> , Port pad input (BGA516 only)																																		
5 <sub>H</sub>	<b>P14.12</b> , Port pad input (BGA516 only)																																		
6 <sub>H</sub>	<b>P24.12</b> , Port pad input (BGA516 only)																																		
7 <sub>H</sub>	<b>P30.12</b> , Port pad input (BGA516 only)																																		
8 <sub>H</sub>	<b>P31.12</b> , Port pad input (BGA516 only)																																		
9 <sub>H</sub>	<b>P34.2</b> , Port pad input (no QFP)																																		
A <sub>H</sub>	<b>P00.0</b> , Port pad input																																		
B <sub>H</sub>	<b>P21.2</b> , Port pad input																																		
C <sub>H</sub>	Reserved, do not use																																		
...																																			
F <sub>H</sub>	Reserved, do not use																																		
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P01.2</b>, Port pad input</td></tr> <tr><td>2<sub>H</sub></td><td><b>P01.10</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>P01.6</b>, Port pad input</td></tr> <tr><td>4<sub>H</sub></td><td><b>P13.6</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P13.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td><b>P24.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>7<sub>H</sub></td><td><b>P30.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>8<sub>H</sub></td><td><b>P31.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>9<sub>H</sub></td><td><b>P32.5</b>, Port pad input (no QFP)</td></tr> <tr><td>A<sub>H</sub></td><td><b>P34.3</b>, Port pad input (no QFP)</td></tr> <tr><td>B<sub>H</sub></td><td><b>P00.1</b>, Port pad input</td></tr> <tr><td>C<sub>H</sub></td><td><b>P21.3</b>, Port pad input</td></tr> <tr><td>D<sub>H</sub></td><td><b>IMUX5_5</b>, DSADC input IMUX5_OUT5</td></tr> <tr><td>E<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P01.2</b> , Port pad input	2 <sub>H</sub>	<b>P01.10</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P01.6</b> , Port pad input	4 <sub>H</sub>	<b>P13.6</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P13.13</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	<b>P24.13</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	<b>P30.13</b> , Port pad input (BGA516 only)	8 <sub>H</sub>	<b>P31.13</b> , Port pad input (BGA516 only)	9 <sub>H</sub>	<b>P32.5</b> , Port pad input (no QFP)	A <sub>H</sub>	<b>P34.3</b> , Port pad input (no QFP)	B <sub>H</sub>	<b>P00.1</b> , Port pad input	C <sub>H</sub>	<b>P21.3</b> , Port pad input	D <sub>H</sub>	<b>IMUX5_5</b> , DSADC input IMUX5_OUT5	E <sub>H</sub>	Reserved, do not use	F <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	Reserved, do not use																																		
1 <sub>H</sub>	<b>P01.2</b> , Port pad input																																		
2 <sub>H</sub>	<b>P01.10</b> , Port pad input (BGA516 only)																																		
3 <sub>H</sub>	<b>P01.6</b> , Port pad input																																		
4 <sub>H</sub>	<b>P13.6</b> , Port pad input (BGA516 only)																																		
5 <sub>H</sub>	<b>P13.13</b> , Port pad input (BGA516 only)																																		
6 <sub>H</sub>	<b>P24.13</b> , Port pad input (BGA516 only)																																		
7 <sub>H</sub>	<b>P30.13</b> , Port pad input (BGA516 only)																																		
8 <sub>H</sub>	<b>P31.13</b> , Port pad input (BGA516 only)																																		
9 <sub>H</sub>	<b>P32.5</b> , Port pad input (no QFP)																																		
A <sub>H</sub>	<b>P34.3</b> , Port pad input (no QFP)																																		
B <sub>H</sub>	<b>P00.1</b> , Port pad input																																		
C <sub>H</sub>	<b>P21.3</b> , Port pad input																																		
D <sub>H</sub>	<b>IMUX5_5</b> , DSADC input IMUX5_OUT5																																		
E <sub>H</sub>	Reserved, do not use																																		
F <sub>H</sub>	Reserved, do not use																																		

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P01.15</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P01.6</b>, Port pad input</li> <li>3<sub>H</sub> <b>P01.14</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P13.7</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P14.15</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P24.14</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P30.14</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P31.14</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P32.6</b>, Port pad input (no QFP)</li> <li>A<sub>H</sub> <b>P34.4</b>, Port pad input (no QFP)</li> <li>B<sub>H</sub> <b>P00.2</b>, Port pad input</li> <li>C<sub>H</sub> <b>P21.4</b>, Port pad input</li> <li>D<sub>H</sub> <b>IMUX5_6</b>, DSADC input IMUX5_OUT6</li> <li>E<sub>H</sub> Reserved, do not use</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P00.14</b>, Port pad input (BGA516 only)</li> <li>2<sub>H</sub> <b>P01.7</b>, Port pad input</li> <li>3<sub>H</sub> <b>P01.11</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P13.15</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P24.15</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P30.15</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P31.15</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P32.7</b>, Port pad input (no QFP)</li> <li>9<sub>H</sub> <b>P34.5</b>, Port pad input (no QFP)</li> <li>A<sub>H</sub> <b>P00.3</b>, Port pad input</li> <li>B<sub>H</sub> <b>P21.5</b>, Port pad input</li> <li>C<sub>H</sub> <b>IMUX5_7</b>, DSADC input IMUX5_OUT7</li> <li>D<sub>H</sub> <b>MT1</b>, ERAY1 macrotick clock from CC</li> <li>E<sub>H</sub> Reserved, do not use</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

## GTM\_TIMnINSEL (n=6)

## TIMn Input Select Register

(09FD40<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

CH7SEL	rw	CH6SEL	rw	CH5SEL	rw	CH4SEL	rw

CH3SEL	rw	CH2SEL	rw	CH1SEL	rw	CHOSEL	rw

Field	Bits	Type	Description
CHxSEL (x=0)	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P20.6</b>, Port pad input</li> <li>2<sub>H</sub> <b>P23.7</b>, Port pad input (no QFP)</li> <li>3<sub>H</sub> <b>P01.12</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P13.4</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P10.9</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P24.0</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P25.0</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P30.8</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P31.8</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
CHxSEL (x=1)	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P20.7</b>, Port pad input</li> <li>2<sub>H</sub> <b>P23.6</b>, Port pad input (no QFP)</li> <li>3<sub>H</sub> <b>P01.13</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P13.5</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P10.10</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P24.1</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P25.1</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P30.9</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> <b>P31.9</b>, Port pad input (BGA516 only)</li> <li>A<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P20.8</b>, Port pad input      2<sub>H</sub> <b>P23.5</b>, Port pad input (no QFP144)      3<sub>H</sub> <b>P01.14</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P13.6</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P10.11</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P24.2</b>, Port pad input (BGA516 only)      7<sub>H</sub> <b>P25.2</b>, Port pad input (BGA516 only)      8<sub>H</sub> <b>P30.10</b>, Port pad input (BGA516 only)      9<sub>H</sub> <b>P31.10</b>, Port pad input (BGA516 only)      A<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P20.9</b>, Port pad input      2<sub>H</sub> <b>P23.4</b>, Port pad input (no QFP144)      3<sub>H</sub> <b>P01.15</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P13.7</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P10.13</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P24.3</b>, Port pad input (BGA516 only)      7<sub>H</sub> <b>P25.3</b>, Port pad input (BGA516 only)      8<sub>H</sub> <b>P30.11</b>, Port pad input (BGA516 only)      9<sub>H</sub> <b>P31.11</b>, Port pad input (BGA516 only)      A<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P00.4</b>, Port pad input      2<sub>H</sub> <b>P23.3</b>, Port pad input (no QFP144)      3<sub>H</sub> <b>P14.12</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P13.9</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P24.4</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P25.4</b>, Port pad input (BGA516 only)      7<sub>H</sub> <b>P30.12</b>, Port pad input (BGA516 only)      8<sub>H</sub> <b>P31.12</b>, Port pad input (BGA516 only)      9<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																										
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P23.2</b>, Port pad input (no QFP144)</td></tr> <tr><td>2<sub>H</sub></td><td><b>P00.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>P14.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>4<sub>H</sub></td><td><b>P13.10</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P24.5</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td><b>P25.5</b>, Port pad input (BGA516 only)</td></tr> <tr><td>7<sub>H</sub></td><td><b>P30.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>8<sub>H</sub></td><td><b>P31.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P23.2</b> , Port pad input (no QFP144)	2 <sub>H</sub>	<b>P00.13</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P14.13</b> , Port pad input (BGA516 only)	4 <sub>H</sub>	<b>P13.10</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P24.5</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	<b>P25.5</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	<b>P30.13</b> , Port pad input (BGA516 only)	8 <sub>H</sub>	<b>P31.13</b> , Port pad input (BGA516 only)	9 <sub>H</sub>	Reserved, do not use	...		F <sub>H</sub>	Reserved, do not use		
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<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P23.1</b>, Port pad input</td></tr> <tr><td>2<sub>H</sub></td><td><b>P00.14</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>P14.14</b>, Port pad input (BGA516 only)</td></tr> <tr><td>4<sub>H</sub></td><td><b>P13.11</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P24.6</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td><b>P25.6</b>, Port pad input (BGA516 only)</td></tr> <tr><td>7<sub>H</sub></td><td><b>P30.14</b>, Port pad input (BGA516 only)</td></tr> <tr><td>8<sub>H</sub></td><td><b>P31.14</b>, Port pad input (BGA516 only)</td></tr> <tr><td>9<sub>H</sub></td><td><b>P26.0</b>, Port pad input (BGA516 only)</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P23.1</b> , Port pad input	2 <sub>H</sub>	<b>P00.14</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P14.14</b> , Port pad input (BGA516 only)	4 <sub>H</sub>	<b>P13.11</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P24.6</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	<b>P25.6</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	<b>P30.14</b> , Port pad input (BGA516 only)	8 <sub>H</sub>	<b>P31.14</b> , Port pad input (BGA516 only)	9 <sub>H</sub>	<b>P26.0</b> , Port pad input (BGA516 only)	A <sub>H</sub>	Reserved, do not use	...		F <sub>H</sub>	Reserved, do not use
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A <sub>H</sub>	Reserved, do not use																												
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<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P23.0</b>, Port pad input (no QFP144)</td></tr> <tr><td>2<sub>H</sub></td><td><b>P00.15</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>P14.15</b>, Port pad input (BGA516 only)</td></tr> <tr><td>4<sub>H</sub></td><td><b>P13.12</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P24.7</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td><b>P25.7</b>, Port pad input (BGA516 only)</td></tr> <tr><td>7<sub>H</sub></td><td><b>P30.15</b>, Port pad input (BGA516 only)</td></tr> <tr><td>8<sub>H</sub></td><td><b>P31.15</b>, Port pad input (BGA516 only)</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P23.0</b> , Port pad input (no QFP144)	2 <sub>H</sub>	<b>P00.15</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P14.15</b> , Port pad input (BGA516 only)	4 <sub>H</sub>	<b>P13.12</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P24.7</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	<b>P25.7</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	<b>P30.15</b> , Port pad input (BGA516 only)	8 <sub>H</sub>	<b>P31.15</b> , Port pad input (BGA516 only)	9 <sub>H</sub>	Reserved, do not use	...		F <sub>H</sub>	Reserved, do not use		
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## Generic Timer Module (GTM)

## GTM\_TIMnINSEL (n=7)

## TIMn Input Select Register

(09FD40<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

CH7SEL	rw	CH6SEL	rw	CH5SEL	rw	CH4SEL	rw

CH3SEL	rw	CH2SEL	rw	CH1SEL	rw	CHOSEL	rw

Field	Bits	Type	Description
CHxSEL (x=0)	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P22.3</b>, Port pad input</li> <li>2<sub>H</sub> <b>P15.10</b>, Port pad input (BGA516 only)</li> <li>3<sub>H</sub> <b>P13.13</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P10.14</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P24.8</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P25.8</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P30.0</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P31.0</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
CHxSEL (x=1)	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> Reserved, do not use</li> <li>1<sub>H</sub> <b>P22.2</b>, Port pad input</li> <li>2<sub>H</sub> <b>P15.11</b>, Port pad input (BGA516 only)</li> <li>3<sub>H</sub> <b>P13.14</b>, Port pad input (BGA516 only)</li> <li>4<sub>H</sub> <b>P10.15</b>, Port pad input (BGA516 only)</li> <li>5<sub>H</sub> <b>P24.9</b>, Port pad input (BGA516 only)</li> <li>6<sub>H</sub> <b>P25.9</b>, Port pad input (BGA516 only)</li> <li>7<sub>H</sub> <b>P30.1</b>, Port pad input (BGA516 only)</li> <li>8<sub>H</sub> <b>P31.1</b>, Port pad input (BGA516 only)</li> <li>9<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

**Generic Timer Module (GTM)**

Field	Bits	Type	Description
<b>CHxSEL (x=2)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P22.1</b>, Port pad input      2<sub>H</sub> <b>P15.12</b>, Port pad input (BGA516 only)      3<sub>H</sub> <b>P13.15</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P24.10</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P25.10</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P30.2</b>, Port pad input (BGA516 only)      7<sub>H</sub> <b>P31.2</b>, Port pad input (BGA516 only)      8<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>
<b>CHxSEL (x=3)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P22.0</b>, Port pad input      2<sub>H</sub> <b>P12.0</b>, Port pad input (no QFP)      3<sub>H</sub> <b>P15.13</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P24.11</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P25.11</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P30.3</b>, Port pad input (BGA516 only)      7<sub>H</sub> <b>P31.3</b>, Port pad input (BGA516 only)      8<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>
<b>CHxSEL (x=4)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0<sub>H</sub> Reserved, do not use      1<sub>H</sub> <b>P12.1</b>, Port pad input (no QFP)      2<sub>H</sub> <b>P15.14</b>, Port pad input (BGA516 only)      3<sub>H</sub> <b>P24.12</b>, Port pad input (BGA516 only)      4<sub>H</sub> <b>P25.12</b>, Port pad input (BGA516 only)      5<sub>H</sub> <b>P30.4</b>, Port pad input (BGA516 only)      6<sub>H</sub> <b>P31.4</b>, Port pad input (BGA516 only)      7<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use   </p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																				
<b>CHxSEL (x=5)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P11.0</b>, Port pad input (no QFP)</td></tr> <tr><td>2<sub>H</sub></td><td><b>P15.15</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>P24.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>4<sub>H</sub></td><td><b>P25.13</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P30.5</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td><b>P31.5</b>, Port pad input (BGA516 only)</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P11.0</b> , Port pad input (no QFP)	2 <sub>H</sub>	<b>P15.15</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P24.13</b> , Port pad input (BGA516 only)	4 <sub>H</sub>	<b>P25.13</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P30.5</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	<b>P31.5</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	Reserved, do not use	...		F <sub>H</sub>	Reserved, do not use
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...																							
F <sub>H</sub>	Reserved, do not use																						
<b>CHxSEL (x=6)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P11.1</b>, Port pad input (no QFP)</td></tr> <tr><td>2<sub>H</sub></td><td><b>P14.11</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>P24.14</b>, Port pad input (BGA516 only)</td></tr> <tr><td>4<sub>H</sub></td><td><b>P25.14</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P30.6</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td><b>P31.6</b>, Port pad input (BGA516 only)</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P11.1</b> , Port pad input (no QFP)	2 <sub>H</sub>	<b>P14.11</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P24.14</b> , Port pad input (BGA516 only)	4 <sub>H</sub>	<b>P25.14</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P30.6</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	<b>P31.6</b> , Port pad input (BGA516 only)	7 <sub>H</sub>	Reserved, do not use	...		F <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	Reserved, do not use																						
1 <sub>H</sub>	<b>P11.1</b> , Port pad input (no QFP)																						
2 <sub>H</sub>	<b>P14.11</b> , Port pad input (BGA516 only)																						
3 <sub>H</sub>	<b>P24.14</b> , Port pad input (BGA516 only)																						
4 <sub>H</sub>	<b>P25.14</b> , Port pad input (BGA516 only)																						
5 <sub>H</sub>	<b>P30.6</b> , Port pad input (BGA516 only)																						
6 <sub>H</sub>	<b>P31.6</b> , Port pad input (BGA516 only)																						
7 <sub>H</sub>	Reserved, do not use																						
...																							
F <sub>H</sub>	Reserved, do not use																						
<b>CHxSEL (x=7)</b>	4*x+3:4*x	rw	<p><b>TIM Channel x Input Selection</b></p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <table> <tr><td>0<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>1<sub>H</sub></td><td><b>P11.4</b>, Port pad input (no QFP)</td></tr> <tr><td>2<sub>H</sub></td><td><b>P24.15</b>, Port pad input (BGA516 only)</td></tr> <tr><td>3<sub>H</sub></td><td><b>P24.14</b>, Port pad input (BGA516 only)</td></tr> <tr><td>4<sub>H</sub></td><td><b>P30.7</b>, Port pad input (BGA516 only)</td></tr> <tr><td>5<sub>H</sub></td><td><b>P31.7</b>, Port pad input (BGA516 only)</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	Reserved, do not use	1 <sub>H</sub>	<b>P11.4</b> , Port pad input (no QFP)	2 <sub>H</sub>	<b>P24.15</b> , Port pad input (BGA516 only)	3 <sub>H</sub>	<b>P24.14</b> , Port pad input (BGA516 only)	4 <sub>H</sub>	<b>P30.7</b> , Port pad input (BGA516 only)	5 <sub>H</sub>	<b>P31.7</b> , Port pad input (BGA516 only)	6 <sub>H</sub>	Reserved, do not use	...		F <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	Reserved, do not use																						
1 <sub>H</sub>	<b>P11.4</b> , Port pad input (no QFP)																						
2 <sub>H</sub>	<b>P24.15</b> , Port pad input (BGA516 only)																						
3 <sub>H</sub>	<b>P24.14</b> , Port pad input (BGA516 only)																						
4 <sub>H</sub>	<b>P30.7</b> , Port pad input (BGA516 only)																						
5 <sub>H</sub>	<b>P31.7</b> , Port pad input (BGA516 only)																						
6 <sub>H</sub>	Reserved, do not use																						
...																							
F <sub>H</sub>	Reserved, do not use																						

## Generic Timer Module (GTM)

## TIMi Channel x Control Register

GTM\_TIMi\_CHx\_CTRL (i=1-7;x=0-7)

TIMi Channel x Control Register

(001024<sub>H</sub>+i\*800<sub>H</sub>+x\*80<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>TOCTRL</b>	<b>EGPR1_SEL</b>	<b>EGPRO_SEL</b>	<b>FR_ECNT_OF_L</b>			<b>CLK_SEL</b>	<b>FLT_CTR_FE</b>	<b>FLT_MODE_FE</b>	<b>FLT_CTR_RE</b>	<b>FLT_MODE_RE</b>	<b>EXT_CAP_EN</b>	<b>FLT_CNT_FRQ</b>		<b>FLT_EN</b>	
rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>ECNT_RESET</b>	<b>ISL</b>	<b>DSL</b>	<b>CNTS_SEL</b>	<b>GPR1_SEL</b>	<b>GPRO_SEL</b>	0	<b>CICTRL</b>	<b>ARUEN</b>	<b>OSM</b>		<b>TIM_MODE</b>		<b>TIM_EN</b>		
rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>TIM_EN</b>	0	rw	<b>TIM channel x enable</b> Enabling of the channel resets the registers <b>ECNT</b> , <b>TIM[i].CH[x].CNT</b> , <b>TIM[i].CH[x].GPRO</b> , and <b>TIM[i].CH[x].GPR1</b> to their reset values. After finishing the action in one-shot mode the <b>TIM_EN</b> bit is cleared automatically. Otherwise, the bit must be cleared manually.  0 <sub>B</sub> Channel disabled 1 <sub>B</sub> Channel enabled
<b>TIM_MODE</b>	3:1	rw	<b>TIM channel x mode</b> If an undefined value is written to the <b>TIM_MODE</b> register, the hardware switches automatically to <b>TIM_MODE = 0b000</b> (TPWM mode). The <b>TIM_MODE</b> register should not be changed while the TIM channel is enabled.  If the TIM channel is enabled and operating in TPWM or TPIM mode after the first valid edge defined by DSL has occurred, a reconfiguration of DSL,ISL,TIM_MODE will not change the channel behavior. Reading these bit fields after reconfiguration will show the newly configured settings but the initial channel behavior will not change. Only a disabling of the TIM channel by setting <b>TIM_EN= 0</b> and reenabling with <b>TIM_EN= 1</b> will change the channel operation mode.  000 <sub>B</sub> PWM Measurement Mode (TPWM) 001 <sub>B</sub> Pulse Integration Mode (TPIM) 010 <sub>B</sub> Input Event Mode (TIEM) 011 <sub>B</sub> Input Prescaler Mode (TIPM) 100 <sub>B</sub> Bit Compression Mode (TBCM) 101 <sub>B</sub> Gated Periodic Sampling Mode (TGPS) 110 <sub>B</sub> Serial Shift Mode (TSSM)
<b>OSM</b>	4	rw	<b>One-shot mode</b> After finishing the action in one-shot mode the <b>TIM_EN</b> bit is cleared automatically. 0 <sub>B</sub> Continuous operation mode 1 <sub>B</sub> One-shot mode

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>ARU_EN</b>	5	rw	<b>GPRO and GPR1 register values routed to ARU</b> $0_B$ Registers content not routed $1_B$ Registers content routed
<b>CICTRL</b>	6	rw	<b>Channel Input Control</b> $0_B$ Use signal TIM_IN(x) as input for channel x $1_B$ Use signal TIM_IN(x-1) as input for channel x (or TIM_IN(m-1) if x is 0)
<b>GPRO_SEL</b>	9:8	rw	<b>Selection for GPRO register</b> If EGPRO_SEL =0 / EGPRO_SEL =1 : If a reserved value is written to the EGPRO_SEL, GPRO_SEL bit fields, the hardware will use TBU_TS0 input. $00_B$ Use TBU_TS0 as input / use ECNT as input $01_B$ Use TBU_TS1 as input / use TIM_INP_VAL as input $10_B$ Use TBU_TS2 as input / reserved $11_B$ Use CNTS as input; if TGPS mode in channel = 0 is selected, use TIM Filter F_OUT as input / reserved
<b>GPR1_SEL</b>	11:10	rw	<b>Selection for GPR1 register</b> If EGPR1_SEL =0 / EGPR1_SEL =1: If a reserved value is written to the EGPR1_SEL, GPR1_SEL bit fields, the hardware will use TBU_TS0 input. Note: In TBCM mode: EGPR1_SEL=1, GPR1_SEL=01 selects TIM_INP_VAL as input; in all other cases, TIM Filter F_OUT is used. $00_B$ Use TBU_TS0 as input / use ECNT as input $01_B$ Use TBU_TS1 as input / use TIM_INP_VAL as input $10_B$ Use TBU_TS2 as input / reserved $11_B$ Use CNT as input / reserved
<b>CNTS_SEL</b>	12	rw	<b>Selection for CNTS register</b> The functionality of the <b>CNTS_SEL</b> is disabled in the modes TIPM,TGPS and TBCM. <b>CNTS_SEL</b> in TSSM mode selects the source signal for registered or latched shift out operation. $0_B$ use F_OUTx $1_B$ use TIM_INx $0_B$ Use CNT register as input $1_B$ Use TBU_TS0 as input
<b>DSL</b>	13	rw	<b>Signal level control</b> In TIM_MODE=0b110 (TSSM), the bit field DSL defines the shift direction. $0_B$ Shift left $1_B$ Shift right $0_B$ Measurement starts with falling edge (low level measurement) $1_B$ Measurement starts with rising edge (high level measurement)
<b>ISL</b>	14	rw	<b>Ignore signal level</b> This bit is mode dependent and will have different meanings (see details in the TIM Channel mode description). $0_B$ Use DSL bit for selecting active signal level (TIEM) $1_B$ Ignore DSL and treat both edges as active edge (TIEM)

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>ECNT_RESET</b>	15	rw	<p><b>Enables resetting of counter in certain modes</b></p> <p>If TIM_MODE=0b101 (TGPS) / TIM_MODE=0b000 (TPWM)  else ECNT counter operating in wrap around mode;  In TIM_MODE=0b110 (TSSM), the bit field ECNT_RESET defines the initial polarity for the shift register.</p> <p>0<sub>B</sub> ECNT counter operating in wrap around mode / ECNT counter operating in wrap around mode, CNT is reset on active input edge defined by DSL</p> <p>1<sub>B</sub> ECNT counter is reset with periodic sampling / ECNT counter operating in wrap around mode, CNT is reset on active and inactive input edge</p>
<b>FLT_EN</b>	16	rw	<p><b>Filter enable for channel x</b></p> <p>If the filter is disabled, all filter related units (including CSU) are bypassed, which means that the signal <i>F_IN</i> is directly routed to signal <i>F_OUT</i>.</p> <p>0<sub>B</sub> Filter disabled and internal states are reset  1<sub>B</sub> Filter enabled</p>
<b>FLT_CNT_FRQ</b>	18:17	rw	<p><b>Filter counter frequency select</b></p> <p>00<sub>B</sub> FLT_CNT counts with CMU_CLK0  01<sub>B</sub> FLT_CNT counts with CMU_CLK1  10<sub>B</sub> FLT_CNT counts with CMU_CLK6  11<sub>B</sub> FLT_CNT counts with CMU_CLK7</p>
<b>EXT_CAP_EN</b>	19	rw	<p><b>Enables external capture mode</b></p> <p>The selected TIM mode is only sensitive to external capture pulses the input event changes are ignored.</p> <p>0<sub>B</sub> External capture disabled  1<sub>B</sub> External capture enabled</p>
<b>FLT_MODE_R_E</b>	20	rw	<p><b>Filter mode for rising edge</b></p> <p>Coding see Family Spec.</p>
<b>FLT_CTR_RE</b>	21	rw	<p><b>Filter counter mode for rising edge</b></p> <p>Coding see Family Spec.</p>
<b>FLT_MODE_F_E</b>	22	rw	<p><b>Filter mode for falling edge</b></p> <p>Coding see Family Spec.</p>
<b>FLT_CTR_FE</b>	23	rw	<p><b>Filter counter mode for falling edge</b></p> <p>Coding see Family Spec.</p>
<b>CLK_SEL</b>	26:24	rw	<p><b>CMU clock source select for channel</b></p> <p>If ECLK_SEL =0 / ECLK_SEL =1:</p> <p>000<sub>B</sub> CMU_CLK0 selected / tdu_sample_evt of TDU selected  001<sub>B</sub> CMU_CLK1 selected / reserved  010<sub>B</sub> CMU_CLK2 selected / reserved  011<sub>B</sub> CMU_CLK3 selected / reserved  100<sub>B</sub> CMU_CLK4 selected / reserved  101<sub>B</sub> CMU_CLK5 selected / reserved  110<sub>B</sub> CMU_CLK6 selected / reserved  111<sub>B</sub> CMU_CLK7 selected / reserved</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>FR_ECNT_OFL</b>	27	rw	<b>Extended Edge counter overflow behavior</b> $0_B$ Overflow will be signaled on ECNT bit width = 8 $1_B$ Overflow will be signaled on EECNT bit width (full range)
<b>EGPRO_SEL</b>	28	rw	<b>Extension of GPRO_SEL bit field</b> Details described in GPRO_SEL bit field.
<b>EGPR1_SEL</b>	29	rw	<b>Extension of GPR1_SEL bit field</b> Details described in GPR1_SEL bit field.
<b>TOCTRL</b>	31:30	rw	<b>Timeout control</b> It has to be mentioned that writing of TOCTRL=0 will every time stop the TDU, independent of the previous state of TOCTRL. $00_B$ Timeout feature disabled $01_B$ Timeout feature enabled for rising edge only $10_B$ Timeout feature enabled for falling edge only $11_B$ Timeout feature enabled for both edges
<b>0</b>	7	r	<b>Reserved</b> Read as zero, shall be written as zero.

## Generic Timer Module (GTM)

## 26.3.3 GTM to Port Connections

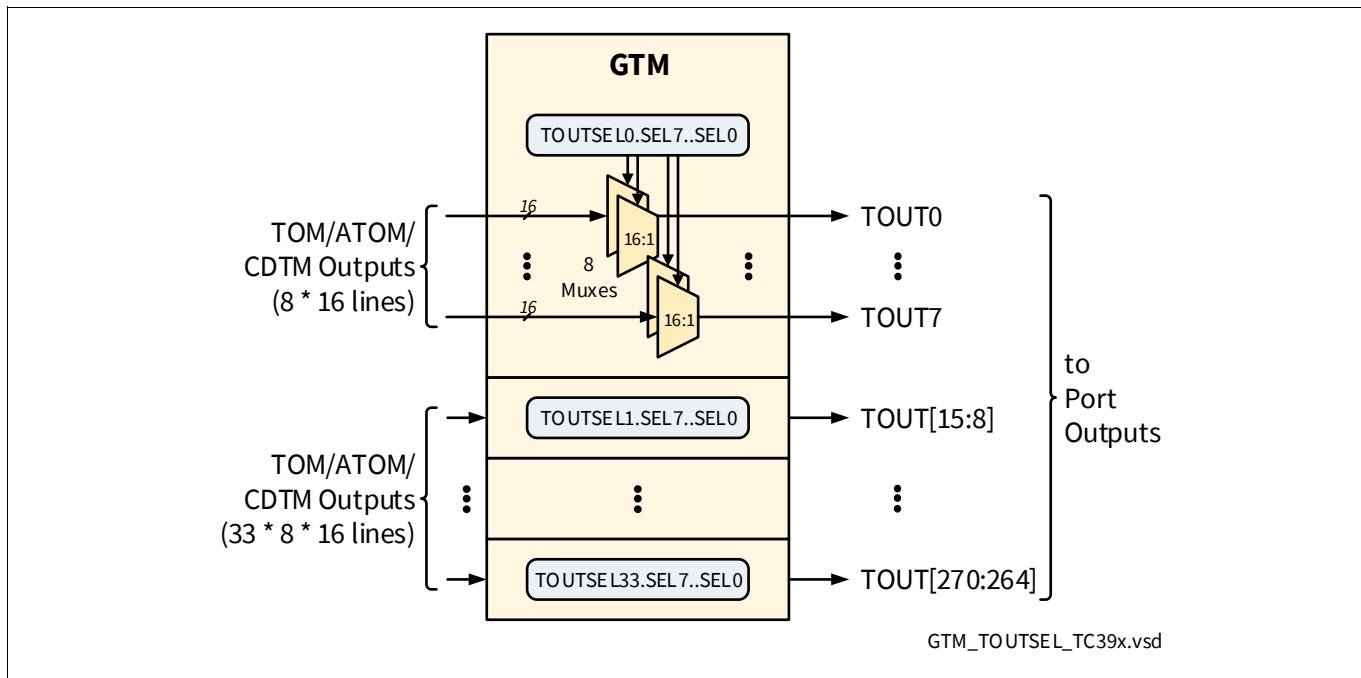


Figure 12 GTM to Port Connections Overview

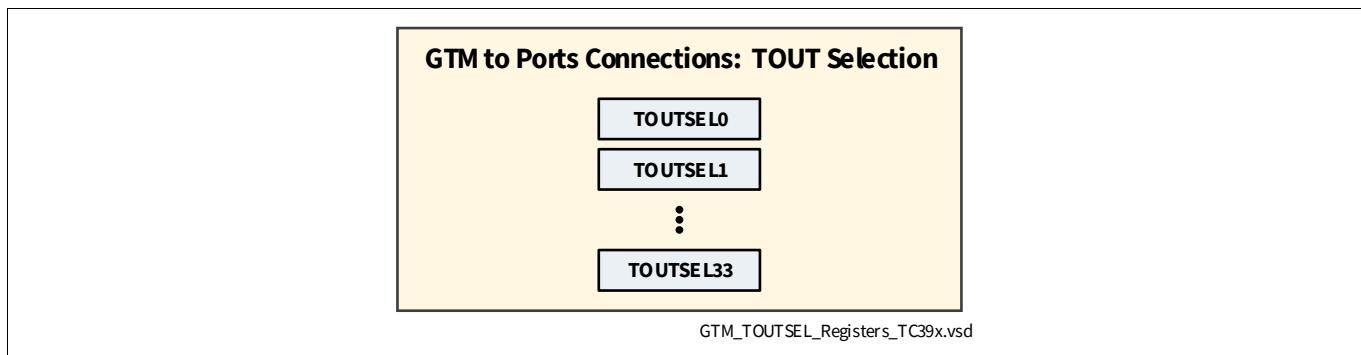


Figure 13 GTM to Port Connections Registers Overview

Table 333 Assignment of TOUTSELn Registers and SELx Bitfields to TOUTy Outputs

Register	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TOUTSEL0, <a href="#">Page 97</a>	TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0
TOUTSEL1, <a href="#">Page 102</a>	TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8
TOUTSEL2, <a href="#">Page 110</a>	TOUT23	TOUT22	TOUT21	TOUT20	TOUT19	TOUT18	TOUT17	TOUT16
TOUTSEL3, <a href="#">Page 115</a>	TOUT31	TOUT30	TOUT29	TOUT28	TOUT27	TOUT26	TOUT25	TOUT24
TOUTSEL4, <a href="#">Page 123</a>	TOUT39	TOUT38	TOUT37	TOUT36	TOUT35	TOUT34	TOUT33	TOUT32
TOUTSEL5, <a href="#">Page 128</a>	TOUT47	TOUT46	TOUT45	TOUT44	TOUT43	TOUT42	TOUT41	TOUT40
TOUTSEL6, <a href="#">Page 134</a>	TOUT55	TOUT54	TOUT53	TOUT52	TOUT51	TOUT50	TOUT49	TOUT48
TOUTSEL7, <a href="#">Page 140</a>	TOUT63	TOUT62	TOUT61	TOUT60	TOUT59	TOUT58	TOUT57	TOUT56
TOUTSEL8, <a href="#">Page 147</a>	TOUT71	TOUT70	TOUT69	TOUT68	TOUT67	TOUT66	TOUT65	TOUT64

## Generic Timer Module (GTM)

**Table 333 Assignment of TOUTSEL<sub>n</sub> Registers and SEL<sub>x</sub> Bitfields to TOUT<sub>y</sub> Outputs (cont'd)**

Register	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TOUTSEL9, <a href="#">Page 151</a>	TOUT79	TOUT78	TOUT77	TOUT76	TOUT75	TOUT74	TOUT73	TOUT72
TOUTSEL10, <a href="#">Page 158</a>	TOUT87	TOUT86	TOUT85	TOUT84	TOUT83	TOUT82	TOUT81	TOUT80
TOUTSEL11, <a href="#">Page 163</a>	TOUT95	TOUT94 <sup>1)</sup>	TOUT93 <sup>1)</sup>	TOUT92 <sup>1)</sup>	TOUT91 <sup>1)</sup>	TOUT90	TOUT89	TOUT88
TOUTSEL12, <a href="#">Page 171</a>	TOUT103	TOUT102	TOUT101	TOUT100	TOUT99	TOUT98	TOUT97	TOUT96
TOUTSEL13, <a href="#">Page 178</a>	TOUT111 1)	TOUT110	TOUT109	TOUT108	TOUT107	TOUT106	TOUT105	TOUT104
TOUTSEL14, <a href="#">Page 184</a>	TOUT119	TOUT118 1)	TOUT117 1)	TOUT116 1)	TOUT115 1)	TOUT114 1)	TOUT113 1)	TOUT112 1)
TOUTSEL15, <a href="#">Page 189</a>	TOUT127	TOUT126	TOUT125	TOUT124	TOUT123	TOUT122	TOUT121	TOUT120
TOUTSEL16, <a href="#">Page 193</a>	TOUT135	TOUT134	TOUT133	TOUT132	TOUT131	TOUT130	TOUT129	TOUT128
TOUTSEL17, <a href="#">Page 198</a>	TOUT143	TOUT142	TOUT141	TOUT140	TOUT139	TOUT138	TOUT137	TOUT136
TOUTSEL18, <a href="#">Page 203</a>	TOUT151 (LFBGA5 16 only)	TOUT150	TOUT149	TOUT148	TOUT147	TOUT146	-	TOUT144

The following TOUT<sub>y</sub> outputs are only available in the LFBGA516 package:

TOUTSEL19, <a href="#">Page 208</a>	TOUT159	TOUT158	TOUT157	TOUT156	TOUT155	TOUT154	TOUT153	TOUT152
TOUTSEL20, <a href="#">Page 213</a>	TOUT167	TOUT166	TOUT165	TOUT164	TOUT163	TOUT162	TOUT161	TOUT160
TOUTSEL21, <a href="#">Page 218</a>	TOUT175	TOUT174	-	-	-	-	-	TOUT168
TOUTSEL22, <a href="#">Page 220</a>	TOUT183	TOUT182	TOUT181	TOUT180	TOUT179	TOUT178	TOUT177	TOUT176
TOUTSEL23, <a href="#">Page 224</a>	TOUT191	TOUT190	TOUT189	TOUT188	TOUT187	TOUT186	TOUT185	TOUT184
TOUTSEL24, <a href="#">Page 229</a>	TOUT199	TOUT198	TOUT197	TOUT196	TOUT195	TOUT194	TOUT193	TOUT192
TOUTSEL25, <a href="#">Page 233</a>	TOUT207	TOUT206	TOUT205	TOUT204	TOUT203	TOUT202	TOUT201	TOUT200
TOUTSEL26, <a href="#">Page 237</a>	TOUT215	TOUT214	TOUT213	TOUT212	TOUT211	TOUT210	TOUT209	TOUT208
TOUTSEL27, <a href="#">Page 241</a>	TOUT223	TOUT222	TOUT221	TOUT220	TOUT219	TOUT218	TOUT217	TOUT216
TOUTSEL28, <a href="#">Page 246</a>	TOUT231	TOUT230	TOUT229	TOUT228	TOUT227	TOUT226	TOUT225	TOUT224
TOUTSEL29, <a href="#">Page 250</a>	-	-	TOUT237	TOUT236	TOUT235	TOUT234	TOUT233	TOUT232
TOUTSEL30, <a href="#">Page 253</a>	TOUT247	TOUT246	TOUT245	TOUT244	TOUT243	TOUT242	-	-
TOUTSEL31, <a href="#">Page 257</a>	TOUT255	TOUT254	TOUT253	TOUT252	TOUT251	TOUT250	TOUT249	TOUT248
TOUTSEL32, <a href="#">Page 261</a>	TOUT263	TOUT262	TOUT261	TOUT260	TOUT259	TOUT258	-	TOUT256
TOUTSEL33, <a href="#">Page 265</a>	-	TOUT270	TOUT269	TOUT268	TOUT267	TOUT266	TOUT265	TOUT264

1) Not available in LFBGA292\_adas package

## Generic Timer Module (GTM)

### Timer Output Select Register

#### GTM\_TOUTSELn (n=0)

##### Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw					rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw					rw				rw				rw		

Field	Bits	Type	Description
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0<sub>H</sub> <b>TOM0_8</b>, Output of TOM0, channel 8  1<sub>H</sub> <b>TOM1_8</b>, Output of TOM1, channel 8  2<sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0  3<sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0  4<sub>H</sub> <b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0  5<sub>H</sub> <b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0  6<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4  7<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4  8<sub>H</sub> <b>CDTM0_DTM5_1_N, ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5  9<sub>H</sub> <b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5  A<sub>H</sub> Reserved, do not use  B<sub>H</sub> Reserved, do not use </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_9</b>, Output of TOM0, channel 9</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM1_9</b>, Output of TOM1, channel 9</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_2_N, ATOM0_6_N</b>, Inverted dead-time output of ATOM0, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_9</b> , Output of TOM0, channel 9	1 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9	2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	3 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	4 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	5 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6	9 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_9</b> , Output of TOM0, channel 9																										
1 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9																										
2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																										
3 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
4 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
5 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6																										
9 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_10</b>, Output of TOM0, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM1_10</b>, Output of TOM1, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_3_N, ATOM0_7_N</b>, Inverted dead-time output of ATOM0, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10	1 <sub>H</sub>	<b>TOM1_10</b> , Output of TOM1, channel 10	2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	3 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	4 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	5 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7	9 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10																										
1 <sub>H</sub>	<b>TOM1_10</b> , Output of TOM1, channel 10																										
2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																										
3 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																										
4 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
5 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																										
6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
8 <sub>H</sub>	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7																										
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A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_11</b>, Output of TOM0, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM1_11</b>, Output of TOM1, channel 11</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_0_N, ATOM0_4_N</b>, Inverted dead-time output of ATOM0, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11	1 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11	2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	3 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	4 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	5 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4	9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11																										
1 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11																										
2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																										
3 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
4 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
5 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
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8 <sub>H</sub>	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4																										
9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_12</b>, Output of TOM0, channel 12</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM1_12</b>, Output of TOM1, channel 12</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM4_1_N, ATOM1_1_N</b>, Inverted dead-time output of ATOM1, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_12</b> , Output of TOM0, channel 12	1 <sub>H</sub>	<b>TOM1_12</b> , Output of TOM1, channel 12	2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	3 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	6 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	7 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	9 <sub>H</sub>	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_12</b> , Output of TOM0, channel 12																										
1 <sub>H</sub>	<b>TOM1_12</b> , Output of TOM1, channel 12																										
2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
3 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
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8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
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A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_13</b>, Output of TOM0, channel 13</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM1_13</b>, Output of TOM1, channel 13</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13	1 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13	2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	4 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	6 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	7 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13																										
1 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13																										
2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																										
3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																										
4 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2																										
5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2																										
6 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
7 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2																										
9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_14</b>, Output of TOM0, channel 14</td> </tr> <tr> <td><math>1_H</math></td> <td><b>TOM1_14</b>, Output of TOM1, channel 14</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM1_DTM0_3_N, TOM1_3_N</b>, Inverted dead-time output of TOM1, channel 3</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM1_DTM4_3_N, ATOM1_3_N</b>, Inverted dead-time output of ATOM1, channel 3</td> </tr> <tr> <td><math>A_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_14</b> , Output of TOM0, channel 14	$1_H$	<b>TOM1_14</b> , Output of TOM1, channel 14	$2_H$	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	$3_H$	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	$4_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	$5_H$	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3	$6_H$	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	$7_H$	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	$8_H$	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3	$9_H$	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_14</b> , Output of TOM0, channel 14																										
$1_H$	<b>TOM1_14</b> , Output of TOM1, channel 14																										
$2_H$	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																										
$3_H$	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6																										
$4_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
$5_H$	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3																										
$6_H$	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
$7_H$	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
$8_H$	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3																										
$9_H$	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3																										
$A_H$	Reserved, do not use																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM0_15</b>, Output of TOM0, channel 15</td></tr> <tr><td><math>1_H</math></td><td><b>TOM1_15</b>, Output of TOM1, channel 15</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM1_DTM0_0_N, TOM1_0_N</b>, Inverted dead-time output of TOM1, channel 0</td></tr> <tr><td><math>6_H</math></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td><math>7_H</math></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM0_DTM4_0_N, ATOM0_0_N</b>, Inverted dead-time output of ATOM0, channel 0</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM1_DTM4_0_N, ATOM1_0_N</b>, Inverted dead-time output of ATOM1, channel 0</td></tr> <tr><td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM0_15</b> , Output of TOM0, channel 15	$1_H$	<b>TOM1_15</b> , Output of TOM1, channel 15	$2_H$	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	$3_H$	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	$4_H$	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	$5_H$	<b>CDTM1_DTM0_0_N, TOM1_0_N</b> , Inverted dead-time output of TOM1, channel 0	$6_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	$7_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	$8_H$	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0	$9_H$	<b>CDTM1_DTM4_0_N, ATOM1_0_N</b> , Inverted dead-time output of ATOM1, channel 0	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_15</b> , Output of TOM0, channel 15																										
$1_H$	<b>TOM1_15</b> , Output of TOM1, channel 15																										
$2_H$	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																										
$3_H$	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																										
$4_H$	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
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$A_H$	Reserved, do not use																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=1)**

Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				<b>SEL7</b>		<b>SEL6</b>		<b>SEL5</b>		<b>SEL4</b>					
				rw		rw		rw		rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				<b>SEL3</b>		<b>SEL2</b>		<b>SEL1</b>		<b>SEL0</b>					
				rw		rw		rw		rw					

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_8</b>, Output of TOM0, channel 8</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM3_DTM0_0_N, TOM3_0_N</b>, Inverted dead-time output of TOM3, channel 0</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM5_1_N, ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_8</b> , Output of TOM0, channel 8	1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	2 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0	3 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	4 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4	5 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0	6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	8 <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5	9 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_8</b> , Output of TOM0, channel 8																										
1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																										
2 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0																										
3 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0																										
4 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4																										
5 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0																										
6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5																										
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A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_8</b>, Output of TOM0, channel 8</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM5_1_N, ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_8</b> , Output of TOM0, channel 8	1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	2 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0	3 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	5 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	6 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	8 <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5	9 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5	A <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_8</b> , Output of TOM0, channel 8																										
1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																										
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6 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5																										
9 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5																										
A <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_9</b>, Output of TOM0, channel 9</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM0_DTM5_2_N, ATOM0_6_N</b>, Inverted dead-time output of ATOM0, channel 6</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9	$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	$2_H$	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	$3_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	$5_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	$6_H$	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	$7_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	$8_H$	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6	$9_H$	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	$A_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9																										
$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
$2_H$	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																										
$3_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
$5_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
$6_H$	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
$7_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
$8_H$	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6																										
$9_H$	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										
$A_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_9</b>, Output of TOM0, channel 9</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM0_DTM5_2_N, ATOM0_6_N</b>, Inverted dead-time output of ATOM0, channel 6</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9	$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	$2_H$	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	$3_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	$4_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	$5_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	$6_H$	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	$7_H$	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	$8_H$	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6	$9_H$	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	$A_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9																										
$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
$2_H$	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																										
$3_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
$4_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2																										
$5_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
$6_H$	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
$7_H$	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
$8_H$	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6																										
$9_H$	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										
$A_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_10</b>, Output of TOM0, channel 10</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM0_DTM5_3_N, ATOM0_7_N</b>, Inverted dead-time output of ATOM0, channel 7</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM2_DTM4_0_N, ATOM2_0_N</b>, Inverted dead-time output of ATOM2, channel 0</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_10</b> , Output of TOM0, channel 10	$1_H$	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	$2_H$	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	$3_H$	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	$4_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	$5_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	$6_H$	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	$7_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	$8_H$	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7	$9_H$	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	$A_H$	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_10</b> , Output of TOM0, channel 10																										
$1_H$	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																										
$2_H$	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																										
$3_H$	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																										
$4_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
$5_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
$6_H$	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
$7_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
$8_H$	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7																										
$9_H$	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7																										
$A_H$	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>  This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_11</b>, Output of TOM0, channel 11</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td> </tr> <tr> <td><math>4_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM0_DTM5_0_N, ATOM0_4_N</b>, Inverted dead-time output of ATOM0, channel 4</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td> </tr> <tr> <td><math>A_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_11</b> , Output of TOM0, channel 11	$1_H$	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	$2_H$	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	$3_H$	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	$4_H$	Reserved, do not use	$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	$6_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	$7_H$	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	$8_H$	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4	$9_H$	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_11</b> , Output of TOM0, channel 11																										
$1_H$	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
$2_H$	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																										
$3_H$	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
$4_H$	Reserved, do not use																										
$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
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$A_H$	Reserved, do not use																										
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## Generic Timer Module (GTM)

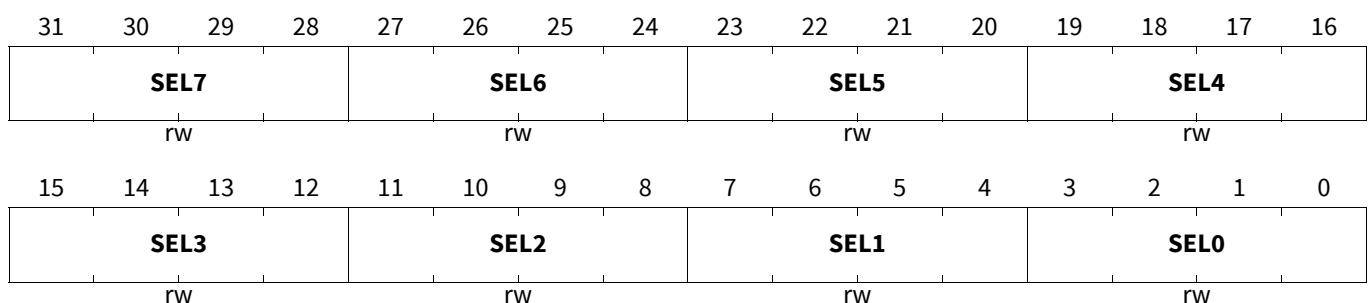
Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_12</b>, Output of TOM0, channel 12</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM1_DTM4_1_N, ATOM1_1_N</b>, Inverted dead-time output of ATOM1, channel 1</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_12</b> , Output of TOM0, channel 12	$1_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	$2_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	$3_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	$5_H$	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	$6_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	$7_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	$8_H$	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	$9_H$	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1	$A_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_12</b> , Output of TOM0, channel 12																										
$1_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
$2_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
$3_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
$5_H$	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
$6_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
$7_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
$8_H$	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
$9_H$	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1																										
$A_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_13</b>, Output of TOM0, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13	1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	4 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2	A <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13																										
1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																										
3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																										
4 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2																										
5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2																										
6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2																										
9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2																										
A <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## GTM\_TOUTSELn (n=2)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_14</b>, Output of TOM0, channel 14</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM0_3_N, TOM1_3_N</b>, Inverted dead-time output of TOM1, channel 3</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM1_DTM4_3_N, ATOM1_3_N</b>, Inverted dead-time output of ATOM1, channel 3</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14	1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	3 <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	5 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3	6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	7 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	8 <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3	9 <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3	A <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14																										
1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																										
2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																										
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4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
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6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
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A <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=1)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>TOM0_15</b>, Output of TOM0, channel 15</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM1_DTM0_0_N, TOM1_0_N</b>, Inverted dead-time output of TOM1, channel 0</td></tr> <tr> <td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM0_DTM4_0_N, ATOM0_0_N</b>, Inverted dead-time output of ATOM0, channel 0</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM1_DTM4_0_N, ATOM1_0_N</b>, Inverted dead-time output of ATOM1, channel 0</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM0_15</b> , Output of TOM0, channel 15	$1_H$	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	$2_H$	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	$3_H$	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	$4_H$	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	$5_H$	<b>CDTM1_DTM0_0_N, TOM1_0_N</b> , Inverted dead-time output of TOM1, channel 0	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0	$9_H$	<b>CDTM1_DTM4_0_N, ATOM1_0_N</b> , Inverted dead-time output of ATOM1, channel 0	$A_H$	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_15</b> , Output of TOM0, channel 15																										
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$A_H$	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0																										
$B_H$	Reserved, do not use																										
<b>SELx (x=2)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0</td></tr> <tr> <td><math>4_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td></tr> <tr> <td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM4_DTM5_1_N, ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</td></tr> <tr> <td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	$1_H$	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	$2_H$	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0	$3_H$	<b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0	$4_H$	Reserved, do not use	$5_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	$9_H$	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																										
$1_H$	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																										
$2_H$	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0																										
$3_H$	<b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0																										
$4_H$	Reserved, do not use																										
$5_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5																										
$9_H$	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5																										
$A_H$	Reserved, do not use																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td></tr> <tr> <td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM3_DTM5_2_N, ATOM3_6_N</b>, Inverted dead-time output of ATOM3, channel 6</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM4_DTM5_2_N, ATOM4_6_N</b>, Inverted dead-time output of ATOM4, channel 6</td></tr> <tr> <td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	1 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	2 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1	3 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6	9 <sub>H</sub>	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
1 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
2 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1																										
3 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6																										
9 <sub>H</sub>	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</td></tr> <tr> <td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM3_DTM5_3_N, ATOM3_7_N</b>, Inverted dead-time output of ATOM3, channel 7</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM4_DTM5_3_N, ATOM4_7_N</b>, Inverted dead-time output of ATOM4, channel 7</td></tr> <tr> <td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2	3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7	9 <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																										
2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2																										
3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7																										
9 <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM3_DTM5_0_N, ATOM3_4_N</b>, Inverted dead-time output of ATOM3, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	1 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	2 <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3	3 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4	9 <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
1 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
2 <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3																										
3 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4																										
9 <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	1 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	2 <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	3 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	9 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
1 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
2 <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																										
3 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
9 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr><td><math>1_H</math></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td></tr> <tr><td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td></tr> <tr><td><math>B_H</math></td><td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	$1_H$	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	$2_H$	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	$3_H$	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	$4_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	$5_H$	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	$9_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	$A_H$	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	$B_H$	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2
$0_H$	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
$1_H$	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
$2_H$	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																										
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$6_H$	Reserved, do not use																										
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## GTM\_TOUTSELn (n=3)

Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				<b>SEL7</b>		<b>SEL6</b>		<b>SEL5</b>		<b>SEL4</b>					
				rw		rw		rw		rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				<b>SEL3</b>		<b>SEL2</b>		<b>SEL1</b>		<b>SEL0</b>					
				rw		rw		rw		rw					

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM0_3_N, TOM1_3_N</b>, Inverted dead-time output of TOM1, channel 3</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM1_DTM4_3_N, ATOM1_3_N</b>, Inverted dead-time output of ATOM1, channel 3</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	3 <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	5 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	9 <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	A <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3	B <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3
0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																										
2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																										
3 <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6																										
4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
5 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3																										
6 <sub>H</sub>	Reserved, do not use																										
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8 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
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B <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM0_0_N, TOM1_0_N</b>, Inverted dead-time output of TOM1, channel 0</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM4_0_N, ATOM2_0_N</b>, Inverted dead-time output of ATOM2, channel 0</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	2 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	3 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	5 <sub>H</sub>	<b>CDTM1_DTM0_0_N, TOM1_0_N</b> , Inverted dead-time output of TOM1, channel 0	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0	9 <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
2 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																										
3 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																										
4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
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6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0																										
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A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_1_N, ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM5_1_N, ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	2 <sub>H</sub>	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0	3 <sub>H</sub>	<b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0	4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	5 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5	9 <sub>H</sub>	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	A <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5	B <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_2_N, ATOM2_6_N</b>, Inverted dead-time output of ATOM2, channel 6</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_2_N, ATOM3_6_N</b>, Inverted dead-time output of ATOM3, channel 6</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM5_2_N, ATOM0_6_N</b>, Inverted dead-time output of ATOM0, channel 6</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	1 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	2 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1	3 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6	9 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6	A <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6	B <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6
0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
1 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
2 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1																										
3 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1																										
4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
8 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6																										
9 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6																										
A <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6																										
B <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_3_N, ATOM2_7_N</b>, Inverted dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_3_N, ATOM3_7_N</b>, Inverted dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM5_3_N, ATOM0_7_N</b>, Inverted dead-time output of ATOM0, channel 7</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2	3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2	4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7	9 <sub>H</sub>	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7	A <sub>H</sub>	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7	B <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																										
2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2																										
3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2																										
4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
7 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
8 <sub>H</sub>	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7																										
9 <sub>H</sub>	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7																										
A <sub>H</sub>	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7																										
B <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7																										

## Generic Timer Module (GTM)

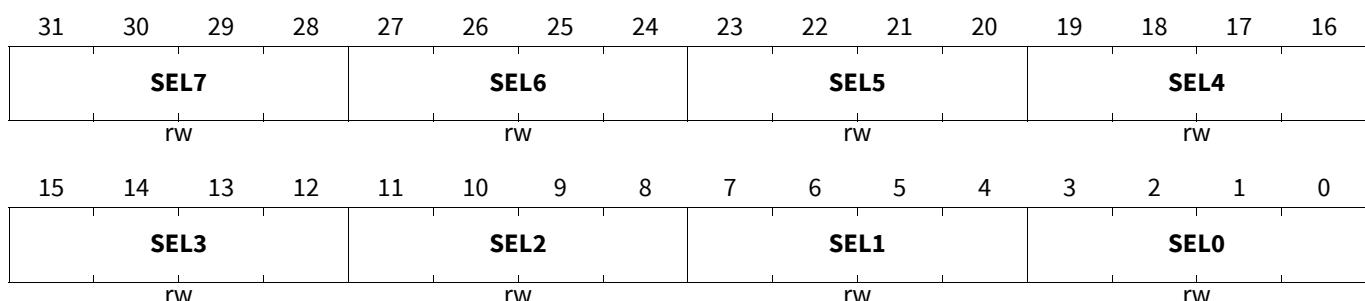
Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr> <td><math>7_H</math></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM2_DTM5_0_N, ATOM2_4_N</b>, Inverted dead-time output of ATOM2, channel 4</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM3_DTM5_0_N, ATOM3_4_N</b>, Inverted dead-time output of ATOM3, channel 4</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr> <td><math>B_H</math></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	$1_H$	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	$2_H$	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3	$3_H$	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3	$4_H$	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	$6_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	$7_H$	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	$8_H$	<b>CDTM2_DTM5_0_N, ATOM2_4_N</b> , Inverted dead-time output of ATOM2, channel 4	$9_H$	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4	$A_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	$B_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4
$0_H$	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
$1_H$	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
$2_H$	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3																										
$3_H$	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3																										
$4_H$	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
$6_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
$7_H$	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																										
$8_H$	<b>CDTM2_DTM5_0_N, ATOM2_4_N</b> , Inverted dead-time output of ATOM2, channel 4																										
$9_H$	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4																										
$A_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
$B_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr> <td><math>7_H</math></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td></tr> <tr> <td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	$1_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	$5_H$	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	$6_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	$7_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	$8_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	$9_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
$1_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																										
$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
$5_H$	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
$6_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
$7_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
$8_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
$9_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										
$A_H$	Reserved, do not use																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	1 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	3 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	8 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	9 <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	A <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
1 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																										
3 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
8 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
9 <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
A <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

**GTM\_TOUTSELn (n=4)****Timer Output Select Register****(09FD60<sub>H</sub>+n\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM4_0_N, ATOM2_0_N</b>, Inverted dead-time output of ATOM2, channel 0</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	2 <sub>H</sub>	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0	3 <sub>H</sub>	<b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0	4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	5 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	7 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	8 <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0	9 <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																										
1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																										
2 <sub>H</sub>	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0																										
3 <sub>H</sub>	<b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0																										
4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
5 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
7 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
8 <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0																										
9 <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	3 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	9 <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																										
2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																										
3 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																										
4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
9 <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_12</b>, Output of TOM1, channel 12</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_12</b>, Output of TOM2, channel 12</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_0_N, TOM1_0_N</b>, Inverted dead-time output of TOM1, channel 0</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_12</b> , Output of TOM1, channel 12	1 <sub>H</sub>	<b>TOM2_12</b> , Output of TOM2, channel 12	2 <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	3 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	5 <sub>H</sub>	<b>CDTM1_DTM0_0_N, TOM1_0_N</b> , Inverted dead-time output of TOM1, channel 0	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	9 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_12</b> , Output of TOM1, channel 12																										
1 <sub>H</sub>	<b>TOM2_12</b> , Output of TOM2, channel 12																										
2 <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																										
3 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
5 <sub>H</sub>	<b>CDTM1_DTM0_0_N, TOM1_0_N</b> , Inverted dead-time output of TOM1, channel 0																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
9 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_13</b>, Output of TOM1, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_13</b>, Output of TOM2, channel 13</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13	1 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13	2 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	3 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	9 <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13																										
1 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13																										
2 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5																										
3 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
9 <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_14</b>, Output of TOM1, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_14</b>, Output of TOM2, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14	1 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14	2 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6	4 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	5 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	9 <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14																										
1 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14																										
2 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																										
3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																										
4 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
5 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
9 <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM1_15</b>, Output of TOM1, channel 15</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM2_15</b>, Output of TOM2, channel 15</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_0_N, ATOM2_0_N</b>, Inverted dead-time output of ATOM2, channel 0</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15	1 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15	2 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	3 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7	4 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	5 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	9 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7	A <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0	B <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0
0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15																										
1 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15																										
2 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																										
3 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7																										
4 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
5 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
7 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
8 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																										
9 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7																										
A <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0																										
B <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	1 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	3 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	6 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use						
0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
1 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																										
3 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr><td><math>1_H</math></td><td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr><td><math>6_H</math></td><td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td></tr> <tr><td><math>7_H</math></td><td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM1_DTM4_1_N, ATOM1_1_N</b>, Inverted dead-time output of ATOM1, channel 1</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	$1_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	$2_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	$3_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	$4_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	$5_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	$6_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	$7_H$	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	$8_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	$9_H$	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	$A_H$	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
$1_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
$2_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
$3_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
$4_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
$5_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
$6_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
$7_H$	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
$8_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																										
$9_H$	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
$A_H$	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=5)****Timer Output Select Register****(09FD60<sub>H</sub>+n\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td></tr> <tr> <td>7<sub>H</sub></td><td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	6 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	7 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	8 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	9 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	A <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																										
3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																										
4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
6 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2																										
7 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2																										
8 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																										
9 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2																										
A <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_10</b>, Output of TOM0, channel 10</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td> </tr> <tr> <td>4<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10	1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	9 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	A <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	B <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2
0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10																										
1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																										
3 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
9 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																										
A <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2																										
B <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr> <td><math>1_H</math></td><td><b>TOM0_15</b>, Output of TOM0, channel 15</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</td></tr> <tr> <td><math>B_H</math></td><td><b>CDTM1_DTM4_3_N, ATOM1_3_N</b>, Inverted dead-time output of ATOM1, channel 3</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	$1_H$	<b>TOM0_15</b> , Output of TOM0, channel 15	$2_H$	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	$3_H$	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	$4_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	$5_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	$6_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	$7_H$	Reserved, do not use	$8_H$	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	$9_H$	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	$A_H$	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3	$B_H$	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3
$0_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
$1_H$	<b>TOM0_15</b> , Output of TOM0, channel 15																										
$2_H$	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																										
$3_H$	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6																										
$4_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
$5_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
$6_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																										
$9_H$	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2																										
$A_H$	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3																										
$B_H$	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3																										

## Generic Timer Module (GTM)

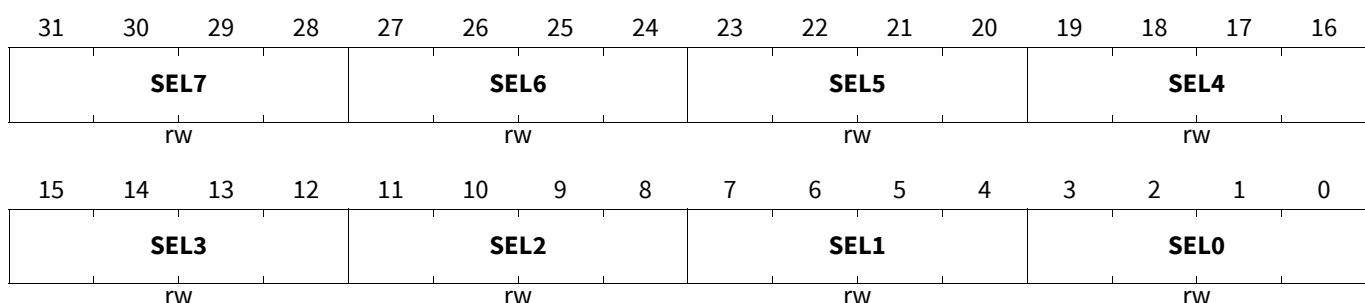
Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_11</b>, Output of TOM0, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM0_3_N, TOM1_3_N</b>, Inverted dead-time output of TOM1, channel 3</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_0_N, ATOM0_0_N</b>, Inverted dead-time output of ATOM0, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11	1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	2 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1	3 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	4 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	5 <sub>H</sub>	Reserved, do not use	6 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0	9 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11																										
1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																										
2 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1																										
3 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1																										
4 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
5 <sub>H</sub>	Reserved, do not use																										
6 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0																										
9 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_12</b>, Output of TOM0, channel 12</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_12</b> , Output of TOM0, channel 12	1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2	3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2	4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	9 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	A <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_12</b> , Output of TOM0, channel 12																										
1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2																										
3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2																										
4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2																										
9 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
A <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_3_N, TOM2_3_N</b>, Inverted dead-time output of TOM2, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM4_2_N, ATOM4_2_N</b>, Inverted dead-time output of ATOM4, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	2 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	3 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	4 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3	9 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	A <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
2 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																										
3 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																										
4 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3																										
9 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5																										
A <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_10</b>, Output of TOM0, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_2_N, TOM2_2_N</b>, Inverted dead-time output of TOM2, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>8<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM4_3_N, ATOM4_3_N</b>, Inverted dead-time output of ATOM4, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10	1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	4 <sub>H</sub>	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2	5 <sub>H</sub>	Reserved, do not use	...		8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	A <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3	B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10																										
1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																										
3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2																										
4 <sub>H</sub>	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6																										
A <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description														
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>            This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).  <i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM0_9</b>, Output of TOM0, channel 9</td></tr> <tr><td><math>1_H</math></td><td><b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr><td><math>4_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9	$1_H$	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1	$2_H$	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	$3_H$	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	$4_H$	Reserved, do not use	...		$B_H$	Reserved, do not use
$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9																
$1_H$	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1																
$2_H$	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																
$3_H$	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																
$4_H$	Reserved, do not use																
...																	
$B_H$	Reserved, do not use																

**GTM\_TOUTSELn (n=6)****Timer Output Select Register****(09FD60<sub>H</sub>+n\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description																						
<b>SELx (x=0)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>            This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).  <i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM0_8</b>, Output of TOM0, channel 8</td></tr> <tr><td><math>1_H</math></td><td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td></tr> <tr><td><math>4_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>6_H</math></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr><td><math>7_H</math></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr><td><math>8_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM0_8</b> , Output of TOM0, channel 8	$1_H$	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	$2_H$	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0	$3_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	$4_H$	Reserved, do not use	$5_H$	Reserved, do not use	$6_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	$7_H$	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	$8_H$	Reserved, do not use	...		$B_H$	Reserved, do not use
$0_H$	<b>TOM0_8</b> , Output of TOM0, channel 8																								
$1_H$	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																								
$2_H$	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0																								
$3_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																								
$4_H$	Reserved, do not use																								
$5_H$	Reserved, do not use																								
$6_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																								
$7_H$	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																								
$8_H$	Reserved, do not use																								
...																									
$B_H$	Reserved, do not use																								

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_11</b>, Output of TOM0, channel 11</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</td> </tr> <tr> <td>4<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>5<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td>8<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11	1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	3 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	Reserved, do not use	6 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	7 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	8 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11																										
1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																										
3 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	Reserved, do not use																										
6 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
7 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
8 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_12</b>, Output of TOM0, channel 12</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td> </tr> <tr> <td>8<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_12</b> , Output of TOM0, channel 12	1 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	4 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	5 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1	A <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_12</b> , Output of TOM0, channel 12																										
1 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
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5 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1																										
A <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>            This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_8</b>, Output of TOM0, channel 8</td> </tr> <tr> <td><math>1_H</math></td> <td><b>TOM2_8</b>, Output of TOM2, channel 8</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td> </tr> <tr> <td><math>6_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>7_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM4_DTM4_3_N, ATOM4_3_N</b>, Inverted dead-time output of ATOM4, channel 3</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_8</b> , Output of TOM0, channel 8	$1_H$	<b>TOM2_8</b> , Output of TOM2, channel 8	$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	$4_H$	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	$5_H$	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	$9_H$	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3	$A_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_8</b> , Output of TOM0, channel 8																										
$1_H$	<b>TOM2_8</b> , Output of TOM2, channel 8																										
$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																										
$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
$4_H$	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
$5_H$	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
$9_H$	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3																										
$A_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>            This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_9</b>, Output of TOM0, channel 9</td> </tr> <tr> <td><math>1_H</math></td> <td><b>TOM2_9</b>, Output of TOM2, channel 9</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td> </tr> <tr> <td><math>6_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>7_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM4_DTM4_2_N, ATOM4_2_N</b>, Inverted dead-time output of ATOM4, channel 2</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9	$1_H$	<b>TOM2_9</b> , Output of TOM2, channel 9	$2_H$	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	$3_H$	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	$4_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	$5_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	$9_H$	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2	$A_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_9</b> , Output of TOM0, channel 9																										
$1_H$	<b>TOM2_9</b> , Output of TOM2, channel 9																										
$2_H$	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5																										
$3_H$	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
$4_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
$5_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
$9_H$	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2																										
$A_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
$B_H$	Reserved, do not use																										

**Generic Timer Module (GTM)**

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	1 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	2 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0	3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	6 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	9 <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																										
1 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																										
2 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0																										
3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																										
4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
6 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
9 <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_0_N, ATOM0_0_N</b>, Inverted dead-time output of ATOM0, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	1 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1	2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	8 <sub>H</sub>	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
1 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1																										
2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																										
3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																										
4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
5 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	5 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
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...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=7)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description																								
SELx (x=0)	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr> <td>7<sub>H</sub></td><td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	3 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3	4 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	9 <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	A <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
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8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2																										
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B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_0_N, ATOM2_4_N</b>, Inverted dead-time output of ATOM2, channel 4</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_0_N, ATOM3_4_N</b>, Inverted dead-time output of ATOM3, channel 4</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	1 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	5 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_0_N, ATOM2_4_N</b> , Inverted dead-time output of ATOM2, channel 4	9 <sub>H</sub>	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4	A <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	B <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1
0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
1 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
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A <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
B <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM0_2_N, TOM2_2_N</b>, Inverted dead-time output of TOM2, channel 2</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM4_2_N, ATOM4_2_N</b>, Inverted dead-time output of ATOM4, channel 2</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	1 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5	2 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	3 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	4 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	5 <sub>H</sub>	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	9 <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM0_3_N, TOM2_3_N</b>, Inverted dead-time output of TOM2, channel 3</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_1_N, ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM4_DTM4_3_N, ATOM4_3_N</b>, Inverted dead-time output of ATOM4, channel 3</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	3 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	5 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5	9 <sub>H</sub>	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	A <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3	B <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3
0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																										
3 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6																										
4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
5 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5																										
9 <sub>H</sub>	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5																										
A <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3																										
B <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM1_11</b>, Output of TOM1, channel 11</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_2_N, ATOM2_6_N</b>, Inverted dead-time output of ATOM2, channel 6</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_2_N, ATOM3_6_N</b>, Inverted dead-time output of ATOM3, channel 6</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11	1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	3 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6	9 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11																										
1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																										
3 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6																										
9 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>TOM1_12</b>, Output of TOM1, channel 12</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM2_DTM5_3_N, ATOM2_7_N</b>, Inverted dead-time output of ATOM2, channel 7</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM3_DTM5_3_N, ATOM3_7_N</b>, Inverted dead-time output of ATOM3, channel 7</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td></tr> <tr> <td><math>B_H</math></td><td><b>CDTM1_DTM4_1_N, ATOM1_1_N</b>, Inverted dead-time output of ATOM1, channel 1</td></tr> </tbody> </table>	$0_H$	<b>TOM1_12</b> , Output of TOM1, channel 12	$1_H$	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	$2_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	$3_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	$4_H$	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	$5_H$	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	$6_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	$7_H$	Reserved, do not use	$8_H$	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7	$9_H$	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7	$A_H$	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	$B_H$	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1
$0_H$	<b>TOM1_12</b> , Output of TOM1, channel 12																										
$1_H$	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
$2_H$	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
$3_H$	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
$4_H$	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
$5_H$	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
$6_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7																										
$9_H$	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7																										
$A_H$	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
$B_H$	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM1_10</b>, Output of TOM1, channel 10</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM2_10</b>, Output of TOM2, channel 10</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td> </tr> <tr> <td>5<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</td> </tr> <tr> <td>9<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_10</b> , Output of TOM1, channel 10	1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10	2 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6	4 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	B <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3
0 <sub>H</sub>	<b>TOM1_10</b> , Output of TOM1, channel 10																										
1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10																										
2 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																										
3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																										
4 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
B <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM1_11</b>, Output of TOM1, channel 11</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM2_11</b>, Output of TOM2, channel 11</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td> </tr> <tr> <td>5<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</td> </tr> <tr> <td>9<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11	1 <sub>H</sub>	<b>TOM2_11</b> , Output of TOM2, channel 11	2 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	3 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7	4 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11																										
1 <sub>H</sub>	<b>TOM2_11</b> , Output of TOM2, channel 11																										
2 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																										
3 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7																										
4 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
5 <sub>H</sub>	Reserved, do not use																										
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8 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=8)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description																								
SELx (x=0)	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr> <td>0<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td></tr> <tr> <td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	1 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	2 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	3 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	4 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1	5 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	6 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	9 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
1 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
2 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																										
3 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																										
4 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1																										
5 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
6 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1																										
9 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13</li> <li>1<sub>H</sub> <b>TOM2_13</b>, Output of TOM2, channel 13</li> <li>2<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</li> <li>3<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</li> <li>4<sub>H</sub> <b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</li> <li>5<sub>H</sub> <b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</li> <li>6<sub>H</sub> <b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</li> <li>7<sub>H</sub> Reserved, do not use</li> <li>8<sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0</li> <li>9<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</li> <li>A<sub>H</sub> <b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</li> <li>B<sub>H</sub> <b>CDTM4_DTM4_2_N, ATOM4_2_N</b>, Inverted dead-time output of ATOM4, channel 2</li> </ul>
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14</li> <li>1<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14</li> <li>2<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</li> <li>3<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</li> <li>4<sub>H</sub> Reserved, do not use</li> <li>5<sub>H</sub> <b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</li> <li>6<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</li> <li>7<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>9<sub>H</sub> Reserved, do not use</li> <li>A<sub>H</sub> <b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</li> <li>B<sub>H</sub> <b>CDTM4_DTM4_3_N, ATOM4_3_N</b>, Inverted dead-time output of ATOM4, channel 3</li> </ul>

## Generic Timer Module (GTM)

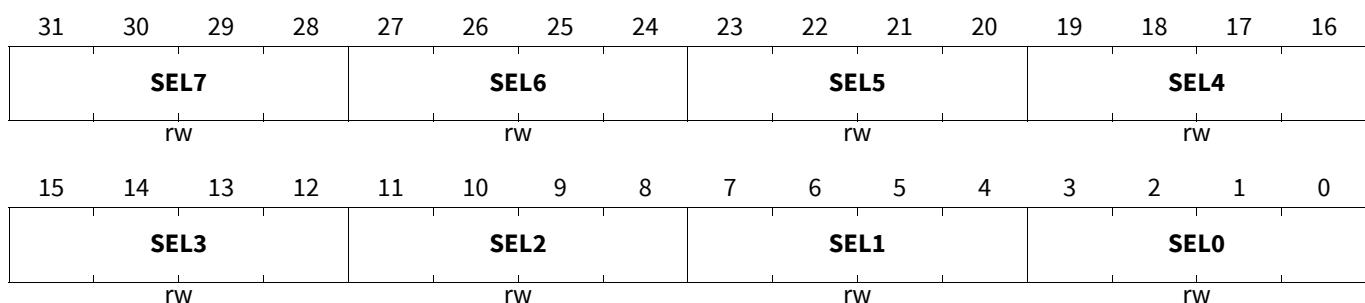
Field	Bits	Type	Description																				
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_15</b>, Output of TOM1, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_15</b>, Output of TOM2, channel 15</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15	1 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15	2 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	3 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	6 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	7 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15																						
1 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15																						
2 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																						
3 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																						
4 <sub>H</sub>	Reserved, do not use																						
5 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																						
6 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																						
7 <sub>H</sub>	Reserved, do not use																						
...																							
B <sub>H</sub>	Reserved, do not use																						
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_8</b>, Output of TOM2, channel 8</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	1 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8	2 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	6 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	7 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																						
1 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8																						
2 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0																						
3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																						
4 <sub>H</sub>	Reserved, do not use																						
5 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																						
6 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																						
7 <sub>H</sub>	Reserved, do not use																						
...																							
B <sub>H</sub>	Reserved, do not use																						

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_9</b>, Output of TOM2, channel 9</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	1 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9	2 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	6 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	7 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																						
1 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9																						
2 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																						
3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																						
4 <sub>H</sub>	Reserved, do not use																						
5 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																						
6 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																						
7 <sub>H</sub>	Reserved, do not use																						
...																							
B <sub>H</sub>	Reserved, do not use																						
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_10</b>, Output of TOM2, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10	2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	6 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	7 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																						
1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10																						
2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																						
3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2																						
4 <sub>H</sub>	Reserved, do not use																						
5 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																						
6 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																						
7 <sub>H</sub>	Reserved, do not use																						
...																							
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td></tr> <tr><td><math>1_H</math></td><td><b>TOM2_11</b>, Output of TOM2, channel 11</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td><math>6_H</math></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td><math>7_H</math></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr><td><math>8_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	$1_H$	<b>TOM2_11</b> , Output of TOM2, channel 11	$2_H$	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	$3_H$	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3	$4_H$	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	$6_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	$7_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	$8_H$	Reserved, do not use	$9_H$	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	$A_H$	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	$B_H$	Reserved, do not use
$0_H$	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
$1_H$	<b>TOM2_11</b> , Output of TOM2, channel 11																										
$2_H$	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
$3_H$	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3																										
$4_H$	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
$6_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
$7_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
$8_H$	Reserved, do not use																										
$9_H$	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
$A_H$	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=9)****Timer Output Select Register****(09FD60<sub>H</sub>+n\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM2_12</b>, Output of TOM2, channel 12</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td> </tr> <tr> <td>8<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM1_DTM4_1_N, ATOM1_1_N</b>, Inverted dead-time output of ATOM1, channel 1</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	1 <sub>H</sub>	<b>TOM2_12</b> , Output of TOM2, channel 12	2 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	6 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1	A <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
1 <sub>H</sub>	<b>TOM2_12</b> , Output of TOM2, channel 12																										
2 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
5 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
6 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1																										
A <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM2_13</b>, Output of TOM2, channel 13</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td> </tr> <tr> <td>8<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM4_DTM4_2_N, ATOM4_2_N</b>, Inverted dead-time output of ATOM4, channel 2</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	1 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13	2 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	3 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2	A <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
1 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13																										
2 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																										
3 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5																										
4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
5 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2																										
6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2																										
A <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_14</b>, Output of TOM2, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_3_N, TOM1_3_N</b>, Inverted dead-time output of TOM1, channel 3</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr><td>8<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM4_3_N, ATOM1_3_N</b>, Inverted dead-time output of ATOM1, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM4_3_N, ATOM4_3_N</b>, Inverted dead-time output of ATOM4, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	1 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14	2 <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	3 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	4 <sub>H</sub>	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	5 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3	6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3	A <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																										
1 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14																										
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8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3																										
A <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_15</b>, Output of TOM2, channel 15</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM0_0_N, TOM1_0_N</b>, Inverted dead-time output of TOM1, channel 0</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>8<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	1 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15	2 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	3 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	5 <sub>H</sub>	<b>CDTM1_DTM0_0_N, TOM1_0_N</b> , Inverted dead-time output of TOM1, channel 0	6 <sub>H</sub>	Reserved, do not use	...		8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	A <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
1 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15																										
2 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																										
3 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																										
4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
5 <sub>H</sub>	<b>CDTM1_DTM0_0_N, TOM1_0_N</b> , Inverted dead-time output of TOM1, channel 0																										
6 <sub>H</sub>	Reserved, do not use																										
...																											
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
A <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td></tr> <tr> <td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr> <td><math>7_H</math></td><td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM4_DTM5_1_N, ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	$1_H$	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	$2_H$	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	$3_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	$4_H$	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	$5_H$	Reserved, do not use	$6_H$	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	$7_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	$8_H$	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0	$9_H$	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5	$A_H$	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																										
$1_H$	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																										
$2_H$	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0																										
$3_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																										
$4_H$	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
$5_H$	Reserved, do not use																										
$6_H$	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
$7_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
$8_H$	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0																										
$9_H$	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5																										
$A_H$	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM2_DTM0_3_N, TOM2_3_N</b>, Inverted dead-time output of TOM2, channel 3</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td><math>7_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM4_DTM5_1_N, ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	$1_H$	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	$2_H$	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	$3_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	$4_H$	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3	$5_H$	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	$6_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	$7_H$	Reserved, do not use	$8_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	$9_H$	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5	$A_H$	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																										
$1_H$	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																										
$2_H$	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0																										
$3_H$	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																										
$4_H$	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3																										
$5_H$	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
$6_H$	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
$9_H$	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5																										
$A_H$	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

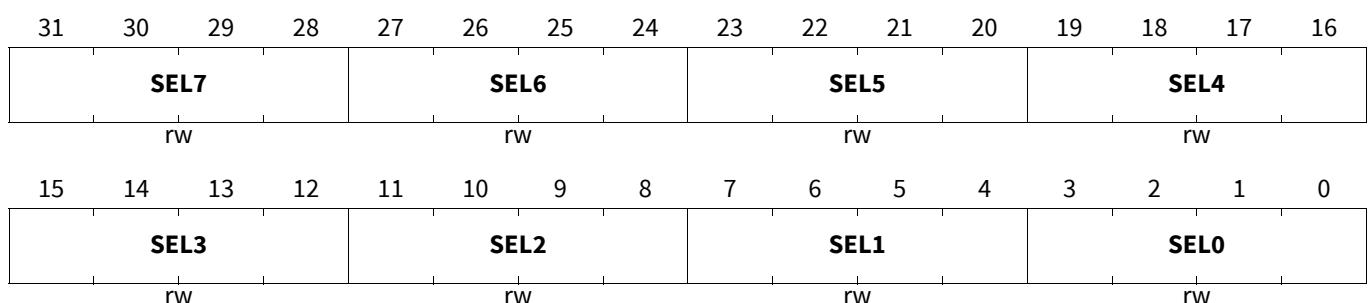
Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM2_DTM0_2_N, TOM2_2_N</b>, Inverted dead-time output of TOM2, channel 2</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM4_DTM5_2_N, ATOM4_6_N</b>, Inverted dead-time output of ATOM4, channel 6</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	$2_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	$3_H$	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	$4_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2	$5_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	$6_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	$7_H$	Reserved, do not use	$8_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	$9_H$	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	$A_H$	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
$2_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
$3_H$	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																										
$4_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2																										
$5_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
$6_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
$9_H$	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										
$A_H$	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM5_3_N, ATOM4_7_N</b>, Inverted dead-time output of ATOM4, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	2 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	5 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	6 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	9 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	A <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																										
2 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																										
4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
5 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
6 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										
9 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7																										
A <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7																										
B <sub>H</sub>	Reserved, do not use																										

**GTM\_TOUTSELn (n=10)**

Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM4_DTM4_3_N, ATOM4_3_N</b>, Inverted dead-time output of ATOM4, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	1 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	4 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
1 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																										
3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2																										
4 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
5 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM4_DTM4_2_N, ATOM4_2_N</b>, Inverted dead-time output of ATOM4, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	1 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	4 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	5 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
1 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
2 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
4 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
5 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																		
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	3 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3	4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	6 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																				
1 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																				
2 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																				
3 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3																				
4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																				
5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																				
6 <sub>H</sub>	Reserved, do not use																				
...																					
B <sub>H</sub>	Reserved, do not use																				
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td></tr> <tr> <td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	4 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use				
0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																				
1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																				
2 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																				
3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2																				
4 <sub>H</sub>	Reserved, do not use																				
...																					
B <sub>H</sub>	Reserved, do not use																				

## Generic Timer Module (GTM)

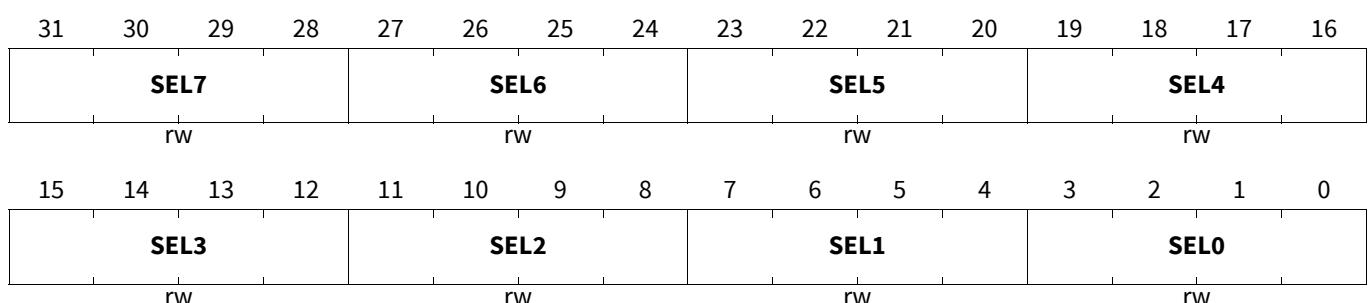
Field	Bits	Type	Description																						
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	6 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use				
0 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																								
1 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																								
2 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																								
3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																								
4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																								
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6 <sub>H</sub>	Reserved, do not use																								
...																									
B <sub>H</sub>	Reserved, do not use																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td></tr> <tr> <td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td></tr> <tr> <td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0	2 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0	3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	4 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																								
1 <sub>H</sub>	<b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0																								
2 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0																								
3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																								
4 <sub>H</sub>	Reserved, do not use																								
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>  This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr> <td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM2_DTM5_0_N, ATOM2_4_N</b>, Inverted dead-time output of ATOM2, channel 4</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM3_DTM5_0_N, ATOM3_4_N</b>, Inverted dead-time output of ATOM3, channel 4</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	$2_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	$3_H$	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	$4_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	$5_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM2_DTM5_0_N, ATOM2_4_N</b> , Inverted dead-time output of ATOM2, channel 4	$9_H$	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4	$A_H$	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
$1_H$	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
$2_H$	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
$3_H$	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																										
$4_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
$5_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM2_DTM5_0_N, ATOM2_4_N</b> , Inverted dead-time output of ATOM2, channel 4																										
$9_H$	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4																										
$A_H$	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM5_1_N, ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM4_0_N, ATOM4_0_N</b>, Inverted dead-time output of ATOM4, channel 0</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	1 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	2 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5	9 <sub>H</sub>	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	A <sub>H</sub>	<b>CDTM4_DTM4_0_N, ATOM4_0_N</b> , Inverted dead-time output of ATOM4, channel 0	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																										
1 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																										
2 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0																										
3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																										
4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5																										
9 <sub>H</sub>	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5																										
A <sub>H</sub>	<b>CDTM4_DTM4_0_N, ATOM4_0_N</b> , Inverted dead-time output of ATOM4, channel 0																										
B <sub>H</sub>	Reserved, do not use																										

**GTM\_TOUTSELn (n=11)****Timer Output Select Register**(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_2_N, ATOM2_6_N</b>, Inverted dead-time output of ATOM2, channel 6</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_2_N, ATOM3_6_N</b>, Inverted dead-time output of ATOM3, channel 6</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2	3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2	4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	5 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6	9 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2																										
3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2																										
4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
5 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6																										
9 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM5_3_N, ATOM2_7_N</b>, Inverted dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM5_3_N, ATOM3_7_N</b>, Inverted dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	2 <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3	3 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3	4 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7	9 <sub>H</sub>	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
2 <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3																										
3 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3																										
4 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7																										
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A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr> <td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td></tr> <tr> <td><math>B_H</math></td><td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	$1_H$	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	$5_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1	$9_H$	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	$A_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	$B_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1
$0_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
$1_H$	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																										
$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
$5_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1																										
$9_H$	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1																										
$A_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
$B_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	1 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5	2 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	3 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	5 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	6 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	7 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	8 <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	9 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	B <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2
0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
1 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5																										
2 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5																										
3 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
5 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
6 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
7 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
8 <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
9 <sub>H</sub>	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										
A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
B <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr> <td><math>7_H</math></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td></tr> <tr> <td><math>B_H</math></td><td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	$1_H$	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	$2_H$	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	$3_H$	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6	$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	$5_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	$6_H$	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	$7_H$	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	$8_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	$9_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	$A_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	$B_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3
$0_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
$1_H$	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
$2_H$	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																										
$3_H$	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																										
$4_H$	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
$5_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
$6_H$	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
$7_H$	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
$8_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
$9_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
$A_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
$B_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>  This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM2_DTM0_2_N, TOM2_2_N</b>, Inverted dead-time output of TOM2, channel 2</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td> </tr> <tr> <td><math>A_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	$1_H$	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	$2_H$	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	$3_H$	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7	$4_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	$5_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2	$6_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	$7_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	$8_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	$9_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
$1_H$	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
$2_H$	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																										
$3_H$	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7																										
$4_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2																										
$5_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2																										
$6_H$	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
$7_H$	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
$8_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
$9_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
$A_H$	Reserved, do not use																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

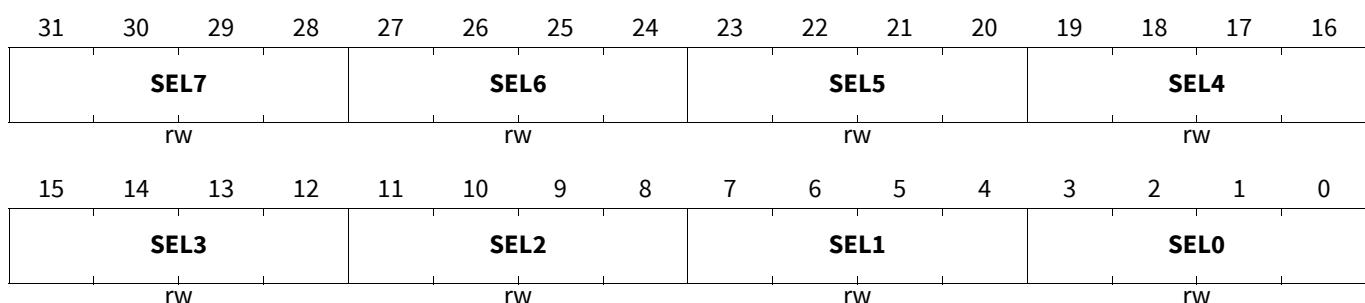
Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_8</b>, Output of TOM0, channel 8</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM2_DTM5_1_N, ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_8</b> , Output of TOM0, channel 8	$1_H$	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	$2_H$	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0	$3_H$	<b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0	$4_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	$5_H$	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	$6_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	$7_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	$8_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	$9_H$	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5	$A_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_8</b> , Output of TOM0, channel 8																										
$1_H$	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																										
$2_H$	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0																										
$3_H$	<b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0																										
$4_H$	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
$5_H$	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
$6_H$	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
$7_H$	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
$8_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5																										
$9_H$	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5																										
$A_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM0_8</b>, Output of TOM0, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM3_DTM5_2_N, ATOM3_6_N</b>, Inverted dead-time output of ATOM3, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM2_DTM5_2_N, ATOM2_6_N</b>, Inverted dead-time output of ATOM2, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_8</b> , Output of TOM0, channel 8	1 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1	2 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1	3 <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	4 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	5 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	6 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	8 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6	9 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6	A <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_8</b> , Output of TOM0, channel 8																										
1 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1																										
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4 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
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6 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6																										
9 <sub>H</sub>	<b>CDTM2_DTM5_2_N, ATOM2_6_N</b> , Inverted dead-time output of ATOM2, channel 6																										
A <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4																										
B <sub>H</sub>	Reserved, do not use																										

**GTM\_TOUTSELn (n=12)**

Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_10</b>, Output of TOM0, channel 10</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM3_DTM5_3_N, ATOM3_7_N</b>, Inverted dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM2_DTM5_3_N, ATOM2_7_N</b>, Inverted dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM5_DTM5_2_N, ATOM5_6_N</b>, Inverted dead-time output of ATOM5, channel 6</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10	1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2	3 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2	4 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	5 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM3_DTM5_3_N, ATOM3_7_N</b> , Inverted dead-time output of ATOM3, channel 7	9 <sub>H</sub>	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7	A <sub>H</sub>	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_10</b> , Output of TOM0, channel 10																										
1 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
2 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2																										
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4 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7																										
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6 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
7 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
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9 <sub>H</sub>	<b>CDTM2_DTM5_3_N, ATOM2_7_N</b> , Inverted dead-time output of ATOM2, channel 7																										
A <sub>H</sub>	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_11</b>, Output of TOM0, channel 11</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM3_DTM5_0_N, ATOM3_4_N</b>, Inverted dead-time output of ATOM3, channel 4</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM2_DTM5_0_N, ATOM2_4_N</b>, Inverted dead-time output of ATOM2, channel 4</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM4_DTM5_2_N, ATOM4_6_N</b>, Inverted dead-time output of ATOM4, channel 6</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11	1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	2 <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3	3 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3	4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	5 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	6 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	7 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	8 <sub>H</sub>	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4	9 <sub>H</sub>	<b>CDTM2_DTM5_0_N, ATOM2_4_N</b> , Inverted dead-time output of ATOM2, channel 4	A <sub>H</sub>	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_11</b> , Output of TOM0, channel 11																										
1 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
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4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
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A <sub>H</sub>	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(<math>n^*8 + x</math>) Output Selection</b>            This bit field defines which timer output is connected as TOUT(<math>n^*8+x</math>).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_12</b>, Output of TOM0, channel 12</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td> </tr> <tr> <td><math>A_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_12</b> , Output of TOM0, channel 12	$1_H$	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	$4_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	$5_H$	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	$6_H$	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	$7_H$	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	$8_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1	$9_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_12</b> , Output of TOM0, channel 12																										
$1_H$	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
$2_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																										
$3_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
$4_H$	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
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$A_H$	Reserved, do not use																										
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM0_13</b>, Output of TOM0, channel 13</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM2_DTM0_2_N, TOM2_2_N</b>, Inverted dead-time output of TOM2, channel 2</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td> </tr> <tr> <td><math>6_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td> </tr> <tr> <td><math>A_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>B_H</math></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	$0_H$	<b>TOM0_13</b> , Output of TOM0, channel 13	$1_H$	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5	$2_H$	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	$3_H$	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	$4_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2	$5_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	$6_H$	Reserved, do not use	$7_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	$8_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2	$9_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM0_13</b> , Output of TOM0, channel 13																										
$1_H$	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5																										
$2_H$	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5																										
$3_H$	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
$4_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2																										
$5_H$	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
$6_H$	Reserved, do not use																										
$7_H$	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
$8_H$	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
$9_H$	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
$A_H$	Reserved, do not use																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_14</b>, Output of TOM0, channel 14</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM0_3_N, TOM2_3_N</b>, Inverted dead-time output of TOM2, channel 3</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14	1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	2 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6	4 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3	5 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	8 <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	9 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14																										
1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
2 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																										
3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																										
4 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3																										
5 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
8 <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
9 <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM0_15</b>, Output of TOM0, channel 15</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM2_DTM4_0_N, ATOM2_0_N</b>, Inverted dead-time output of ATOM2, channel 0</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM0_15</b> , Output of TOM0, channel 15	1 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	2 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	3 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7	4 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	5 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	8 <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0	9 <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM0_15</b> , Output of TOM0, channel 15																										
1 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
2 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																										
3 <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7																										
4 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
5 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																										
8 <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0																										
9 <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_12</b>, Output of TOM2, channel 12</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM1_DTM4_1_N, ATOM1_1_N</b>, Inverted dead-time output of ATOM1, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM4_1_N, ATOM4_1_N</b>, Inverted dead-time output of ATOM4, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	1 <sub>H</sub>	<b>TOM2_12</b> , Output of TOM2, channel 12	2 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1	9 <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1	A <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
1 <sub>H</sub>	<b>TOM2_12</b> , Output of TOM2, channel 12																										
2 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
3 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1																										
9 <sub>H</sub>	<b>CDTM4_DTM4_1_N, ATOM4_1_N</b> , Inverted dead-time output of ATOM4, channel 1																										
A <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM2_9</b>, Output of TOM2, channel 9</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_2_N, ATOM4_6_N</b>, Inverted dead-time output of ATOM4, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	1 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9	2 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	9 <sub>H</sub>	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6	A <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1																										
1 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9																										
2 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
3 <sub>H</sub>	<b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5																										
6 <sub>H</sub>	Reserved, do not use																										
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8 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										
9 <sub>H</sub>	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6																										
A <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=13)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description																								
SELx (x=0)	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM2_10</b>, Output of TOM2, channel 10</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td></tr> <tr> <td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM4_DTM5_3_N, ATOM4_7_N</b>, Inverted dead-time output of ATOM4, channel 7</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10	2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	9 <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7	A <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10																										
2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																										
3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7																										
9 <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7																										
A <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM2_11</b>, Output of TOM2, channel 11</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</td> </tr> <tr> <td>4<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	1 <sub>H</sub>	<b>TOM2_11</b> , Output of TOM2, channel 11	2 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	3 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	9 <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	A <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
1 <sub>H</sub>	<b>TOM2_11</b> , Output of TOM2, channel 11																										
2 <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
3 <sub>H</sub>	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
9 <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4																										
A <sub>H</sub>	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_0_N, TOM0_0_N</b>, Inverted dead-time output of TOM0, channel 0</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM2_DTM0_3_N, TOM2_3_N</b>, Inverted dead-time output of TOM2, channel 3</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM1_DTM4_3_N, ATOM1_3_N</b>, Inverted dead-time output of ATOM1, channel 3</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM4_3_N, ATOM4_3_N</b>, Inverted dead-time output of ATOM4, channel 3</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	3 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0	5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	6 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3	9 <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3	A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	B <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6
0 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
2 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																										
3 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6																										
4 <sub>H</sub>	<b>CDTM0_DTM0_0_N, TOM0_0_N</b> , Inverted dead-time output of TOM0, channel 0																										
5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
6 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3																										
9 <sub>H</sub>	<b>CDTM4_DTM4_3_N, ATOM4_3_N</b> , Inverted dead-time output of ATOM4, channel 3																										
A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
B <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM2_10</b>, Output of TOM2, channel 10</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM0_DTM0_1_N, TOM0_1_N</b>, Inverted dead-time output of TOM0, channel 1</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM5_3_N, ATOM4_7_N</b>, Inverted dead-time output of ATOM4, channel 7</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10	2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2	4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1	5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	9 <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7	A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2																										
1 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10																										
2 <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																										
3 <sub>H</sub>	<b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2																										
4 <sub>H</sub>	<b>CDTM0_DTM0_1_N, TOM0_1_N</b> , Inverted dead-time output of TOM0, channel 1																										
5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7																										
9 <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7																										
A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

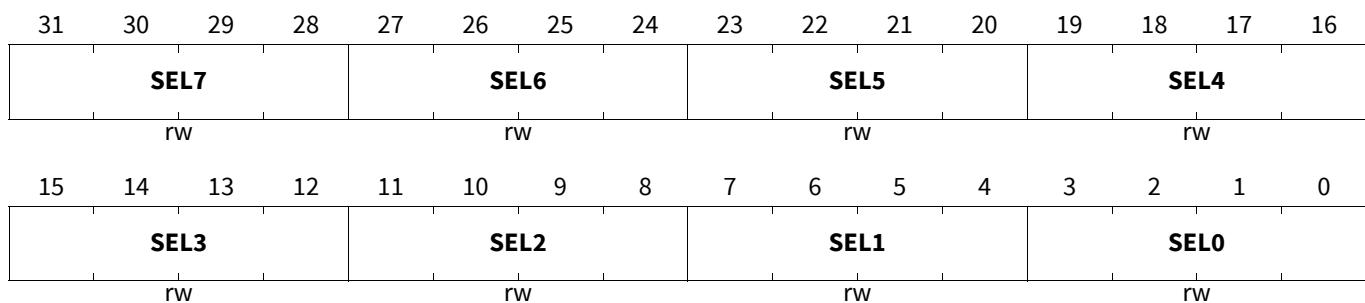
Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr> <td><math>1_H</math></td><td><b>TOM2_11</b>, Output of TOM2, channel 11</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr> <td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM2_DTM4_0_N, ATOM2_0_N</b>, Inverted dead-time output of ATOM2, channel 0</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	$1_H$	<b>TOM2_11</b> , Output of TOM2, channel 11	$2_H$	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	$3_H$	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3	$4_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	$5_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	$9_H$	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	$A_H$	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0	$B_H$	Reserved, do not use
$0_H$	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3																										
$1_H$	<b>TOM2_11</b> , Output of TOM2, channel 11																										
$2_H$	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
$3_H$	<b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3																										
$4_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2																										
$5_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
$9_H$	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4																										
$A_H$	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM2_8</b>, Output of TOM2, channel 8</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM4_DTM5_1_N, ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	1 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8	2 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0	4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	5 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5	9 <sub>H</sub>	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5	A <sub>H</sub>	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0																										
1 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8																										
2 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0																										
3 <sub>H</sub>	<b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0																										
4 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3																										
5 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5																										
9 <sub>H</sub>	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5																										
A <sub>H</sub>	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM2_13</b>, Output of TOM2, channel 13</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td></tr> <tr> <td>3<sub>H</sub></td><td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM4_DTM4_2_N, ATOM4_2_N</b>, Inverted dead-time output of ATOM4, channel 2</td></tr> <tr> <td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	1 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13	2 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	3 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	4 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0	5 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2	9 <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
1 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13																										
2 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																										
3 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5																										
4 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0																										
5 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2																										
9 <sub>H</sub>	<b>CDTM4_DTM4_2_N, ATOM4_2_N</b> , Inverted dead-time output of ATOM4, channel 2																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr><td><math>1_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td></tr> <tr><td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	$1_H$	Reserved, do not use	$2_H$	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	$3_H$	Reserved, do not use	$4_H$	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4	$5_H$	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	$9_H$	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
$1_H$	Reserved, do not use																										
$2_H$	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1																										
$3_H$	Reserved, do not use																										
$4_H$	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4																										
$5_H$	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
$9_H$	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																										
$A_H$	Reserved, do not use																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=14)****Timer Output Select Register**(09FD60<sub>H</sub>+n\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_0_N, TOM4_4_N</b>, Inverted dead-time output of TOM4, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_0_N, ATOM0_0_N</b>, Inverted dead-time output of ATOM0, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM4_0_N, ATOM1_0_N</b>, Inverted dead-time output of ATOM1, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2	1 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0	9 <sub>H</sub>	<b>CDTM1_DTM4_0_N, ATOM1_0_N</b> , Inverted dead-time output of ATOM1, channel 0	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2																										
1 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_0_N, ATOM0_0_N</b> , Inverted dead-time output of ATOM0, channel 0																										
9 <sub>H</sub>	<b>CDTM1_DTM4_0_N, ATOM1_0_N</b> , Inverted dead-time output of ATOM1, channel 0																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_1_N, TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM4_1_N, ATOM0_1_N</b>, Inverted dead-time output of ATOM0, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM4_1_N, ATOM1_1_N</b>, Inverted dead-time output of ATOM1, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3	1 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1	9 <sub>H</sub>	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3																										
1 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_1_N, ATOM0_1_N</b> , Inverted dead-time output of ATOM0, channel 1																										
9 <sub>H</sub>	<b>CDTM1_DTM4_1_N, ATOM1_1_N</b> , Inverted dead-time output of ATOM1, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td></tr> <tr> <td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM4_DTM1_2_N, TOM4_6_N</b>, Inverted dead-time output of TOM4, channel 6</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM0_DTM4_2_N, ATOM0_2_N</b>, Inverted dead-time output of ATOM0, channel 2</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM1_DTM4_2_N, ATOM1_2_N</b>, Inverted dead-time output of ATOM1, channel 2</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td></tr> <tr> <td>B<sub>H</sub></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	1 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6	5 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2	9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2	A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	B <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2
0 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
1 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6																										
5 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_2_N, ATOM0_2_N</b> , Inverted dead-time output of ATOM0, channel 2																										
9 <sub>H</sub>	<b>CDTM1_DTM4_2_N, ATOM1_2_N</b> , Inverted dead-time output of ATOM1, channel 2																										
A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
B <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5</td></tr> <tr> <td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM4_DTM1_3_N, TOM4_7_N</b>, Inverted dead-time output of TOM4, channel 7</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM0_DTM4_3_N, ATOM0_3_N</b>, Inverted dead-time output of ATOM0, channel 3</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM1_DTM4_3_N, ATOM1_3_N</b>, Inverted dead-time output of ATOM1, channel 3</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td></tr> <tr> <td>B<sub>H</sub></td><td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	1 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7	5 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3	9 <sub>H</sub>	<b>CDTM1_DTM4_3_N, ATOM1_3_N</b> , Inverted dead-time output of ATOM1, channel 3	A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	B <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3
0 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
1 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7																										
5 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM4_3_N, ATOM0_3_N</b> , Inverted dead-time output of ATOM0, channel 3																										
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A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
B <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5</td></tr> <tr> <td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM0_1_N, TOM3_1_N</b>, Inverted dead-time output of TOM3, channel 1</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM0_DTM5_2_N, ATOM0_6_N</b>, Inverted dead-time output of ATOM0, channel 6</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td></tr> <tr> <td>B<sub>H</sub></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	1 <sub>H</sub>	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	5 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1	6 <sub>H</sub>	<b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6	9 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	A <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	B <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1
0 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5																										
1 <sub>H</sub>	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5																										
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3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
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8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6																										
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A <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																										
B <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6</td></tr> <tr> <td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM0_2_N, TOM3_2_N</b>, Inverted dead-time output of TOM3, channel 2</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM0_DTM5_3_N, ATOM0_7_N</b>, Inverted dead-time output of ATOM0, channel 7</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr> <td>B<sub>H</sub></td><td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	1 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	5 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2	6 <sub>H</sub>	<b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7	9 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	A <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	B <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2
0 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6																										
1 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6																										
2 <sub>H</sub>	Reserved, do not use																										
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A <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																										
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</td></tr> <tr> <td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM0_3_N, TOM3_3_N</b>, Inverted dead-time output of TOM3, channel 3</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM0_DTM5_0_N, ATOM0_4_N</b>, Inverted dead-time output of ATOM0, channel 4</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td></tr> <tr> <td>B<sub>H</sub></td><td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	1 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	5 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3	6 <sub>H</sub>	<b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4	9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	A <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	B <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3
0 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																										
1 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7																										
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7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4																										
9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
A <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																										
B <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																										
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td></tr> <tr> <td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM5_DTM5_1_N, ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td></tr> <tr> <td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5	9 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
5 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
6 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5																										
9 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=15)

## **Timer Output Select Register**

(09FD60<sub>H</sub>+n\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
	rw				rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</td></tr> <tr> <td><math>1_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr> <td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td></tr> <tr> <td><math>6_H</math></td><td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM5_DTM5_2_N, ATOM5_6_N</b>, Inverted dead-time output of ATOM5, channel 6</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM2_DTM5_1_N, ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td></tr> <tr> <td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1	$1_H$	Reserved, do not use	$2_H$	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	$3_H$	Reserved, do not use	$4_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	$5_H$	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	$6_H$	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	$7_H$	Reserved, do not use	$8_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6	$9_H$	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5	$A_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	$B_H$	Reserved, do not use
$0_H$	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1																										
$1_H$	Reserved, do not use																										
$2_H$	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
$3_H$	Reserved, do not use																										
$4_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
$5_H$	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
$6_H$	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6																										
$9_H$	<b>CDTM2_DTM5_1_N, ATOM2_5_N</b> , Inverted dead-time output of ATOM2, channel 5																										
$A_H$	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5																										
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_3_N, ATOM5_7_N</b>, Inverted dead-time output of ATOM5, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM5_1_N, ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	5 <sub>H</sub>	Reserved, do not use	6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7																										
5 <sub>H</sub>	Reserved, do not use																										
6 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM2_DTM0_3_N, TOM2_3_N</b>, Inverted dead-time output of TOM2, channel 3</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_0_N, ATOM5_4_N</b>, Inverted dead-time output of ATOM5, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	5 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3	6 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
5 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3																										
6 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

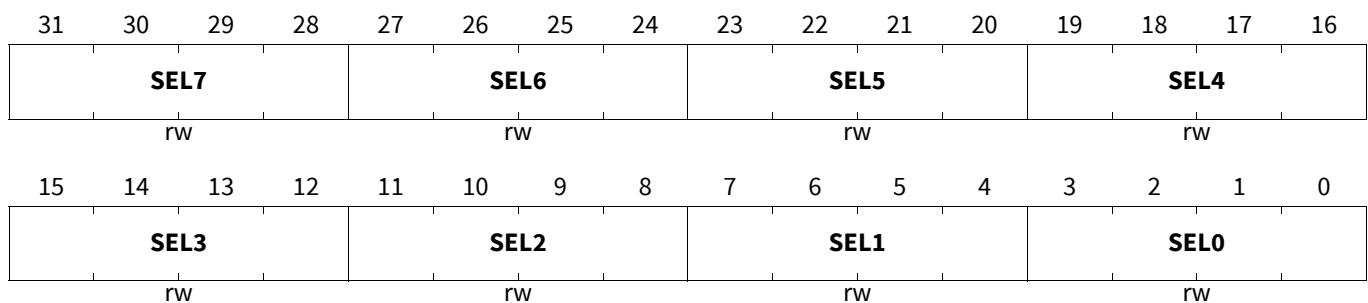
Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	5 <sub>H</sub>	Reserved, do not use	6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
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6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_2_N, TOM2_2_N</b>, Inverted dead-time output of TOM2, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM4_DTM5_3_N, ATOM4_7_N</b>, Inverted dead-time output of ATOM4, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2	5 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4	6 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	8 <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2																										
5 <sub>H</sub>	<b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4																										
6 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
7 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
8 <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM11_7</b>, Output of ATOM11, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	6 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0	9 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
5 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
6 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										
9 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																						
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM2_8</b>, Output of TOM2, channel 8</td></tr> <tr><td><math>1_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>8_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>9_H</math></td><td><b>ATOM11_6</b>, Output of ATOM11, channel 6</td></tr> <tr><td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM2_8</b> , Output of TOM2, channel 8	$1_H$	Reserved, do not use	$2_H$	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	$3_H$	Reserved, do not use	$4_H$	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1	$5_H$	Reserved, do not use	...		$8_H$	Reserved, do not use	$9_H$	<b>ATOM11_6</b> , Output of ATOM11, channel 6	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM2_8</b> , Output of TOM2, channel 8																								
$1_H$	Reserved, do not use																								
$2_H$	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																								
$3_H$	Reserved, do not use																								
$4_H$	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1																								
$5_H$	Reserved, do not use																								
...																									
$8_H$	Reserved, do not use																								
$9_H$	<b>ATOM11_6</b> , Output of ATOM11, channel 6																								
$A_H$	Reserved, do not use																								
$B_H$	Reserved, do not use																								

**GTM\_TOUTSELn (n=16)****Timer Output Select Register****(09FD60<sub>H</sub>+n\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_8</b>, Output of TOM1, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_8</b> , Output of TOM1, channel 8	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	3 <sub>H</sub>	Reserved, do not use	...		5 <sub>H</sub>	Reserved, do not use	6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	9 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	A <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_8</b> , Output of TOM1, channel 8																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1																										
3 <sub>H</sub>	Reserved, do not use																										
...																											
5 <sub>H</sub>	Reserved, do not use																										
6 <sub>H</sub>	<b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
9 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5																										
A <sub>H</sub>	<b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_9</b>, Output of TOM1, channel 9</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_0_N, ATOM5_4_N</b>, Inverted dead-time output of ATOM5, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	3 <sub>H</sub>	Reserved, do not use	...		5 <sub>H</sub>	Reserved, do not use	6 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4	9 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																										
3 <sub>H</sub>	Reserved, do not use																										
...																											
5 <sub>H</sub>	Reserved, do not use																										
6 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4																										
9 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6																										
A <sub>H</sub>	Reserved, do not use																										
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td> </tr> <tr> <td>1<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>4<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	1 <sub>H</sub>	Reserved, do not use	...		4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0	6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	7 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	8 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	9 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	A <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
1 <sub>H</sub>	Reserved, do not use																										
...																											
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0																										
6 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
7 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
8 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
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A <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM2_8</b>, Output of TOM2, channel 8</td> </tr> <tr> <td>1<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>2<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	4 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	5 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	9 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	A <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
4 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
5 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
9 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
A <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=4)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_9</b>, Output of TOM2, channel 9</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_0_N, ATOM4_4_N</b>, Inverted dead-time output of ATOM4, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	4 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5	5 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5	9 <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4	A <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
4 <sub>H</sub>	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5																										
5 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5																										
9 <sub>H</sub>	<b>CDTM4_DTM5_0_N, ATOM4_4_N</b> , Inverted dead-time output of ATOM4, channel 4																										
A <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_10</b>, Output of TOM2, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_1_N, ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6	4 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	5 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	9 <sub>H</sub>	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5	A <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																										
4 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
5 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										
9 <sub>H</sub>	<b>CDTM4_DTM5_1_N, ATOM4_5_N</b> , Inverted dead-time output of ATOM4, channel 5																										
A <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

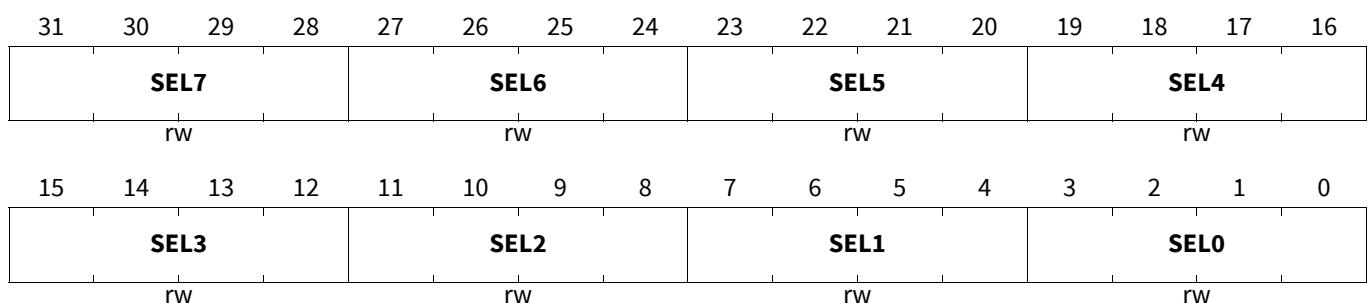
Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM2_11</b>, Output of TOM2, channel 11</td> </tr> <tr> <td><math>1_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>2_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM3_DTM0_0_N, TOM3_0_N</b>, Inverted dead-time output of TOM3, channel 0</td> </tr> <tr> <td><math>7_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM4_DTM5_2_N, ATOM4_6_N</b>, Inverted dead-time output of ATOM4, channel 6</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td> </tr> <tr> <td><math>B_H</math></td> <td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td> </tr> </tbody> </table>	$0_H$	<b>TOM2_11</b> , Output of TOM2, channel 11	$1_H$	Reserved, do not use	$2_H$	Reserved, do not use	$3_H$	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7	$4_H$	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	$5_H$	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	$6_H$	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0	$7_H$	Reserved, do not use	$8_H$	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	$9_H$	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6	$A_H$	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	$B_H$	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0
$0_H$	<b>TOM2_11</b> , Output of TOM2, channel 11																										
$1_H$	Reserved, do not use																										
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$6_H$	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7																										
$9_H$	<b>CDTM4_DTM5_2_N, ATOM4_6_N</b> , Inverted dead-time output of ATOM4, channel 6																										
$A_H$	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
$B_H$	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr><td><math>0_H</math></td><td><b>TOM2_12</b>, Output of TOM2, channel 12</td></tr> <tr><td><math>1_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>2_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM3_DTM5_0_N, ATOM3_4_N</b>, Inverted dead-time output of ATOM3, channel 4</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5</td></tr> <tr><td><math>6_H</math></td><td><b>CDTM3_DTM0_1_N, TOM3_1_N</b>, Inverted dead-time output of TOM3, channel 1</td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM0_DTM5_0_N, ATOM0_4_N</b>, Inverted dead-time output of ATOM0, channel 4</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM4_DTM5_3_N, ATOM4_7_N</b>, Inverted dead-time output of ATOM4, channel 7</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td><math>B_H</math></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> </table>	$0_H$	<b>TOM2_12</b> , Output of TOM2, channel 12	$1_H$	Reserved, do not use	$2_H$	Reserved, do not use	$3_H$	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4	$4_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	$5_H$	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5	$6_H$	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1	$7_H$	Reserved, do not use	$8_H$	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4	$9_H$	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7	$A_H$	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	$B_H$	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1
$0_H$	<b>TOM2_12</b> , Output of TOM2, channel 12																										
$1_H$	Reserved, do not use																										
$2_H$	Reserved, do not use																										
$3_H$	<b>CDTM3_DTM5_0_N, ATOM3_4_N</b> , Inverted dead-time output of ATOM3, channel 4																										
$4_H$	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
$5_H$	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5																										
$6_H$	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4																										
$9_H$	<b>CDTM4_DTM5_3_N, ATOM4_7_N</b> , Inverted dead-time output of ATOM4, channel 7																										
$A_H$	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
$B_H$	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										

## GTM\_TOUTSELn (n=17)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>TOM2_13</b>, Output of TOM2, channel 13</td> </tr> <tr> <td>1<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>2<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM3_DTM5_1_N, ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM3_DTM0_2_N, TOM3_2_N</b>, Inverted dead-time output of TOM3, channel 2</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM5_1_N, ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>9<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5	4 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	5 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6	6 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	B <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2
0 <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	<b>CDTM3_DTM5_1_N, ATOM3_5_N</b> , Inverted dead-time output of ATOM3, channel 5																										
4 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
5 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6																										
6 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2																										
7 <sub>H</sub>	Reserved, do not use																										
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9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
B <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_14</b>, Output of TOM2, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM3_DTM5_2_N, ATOM3_6_N</b>, Inverted dead-time output of ATOM3, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM3_DTM0_3_N, TOM3_3_N</b>, Inverted dead-time output of TOM3, channel 3</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_2_N, ATOM0_6_N</b>, Inverted dead-time output of ATOM0, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6	4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	5 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7	6 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7	B <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3
0 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14																										
1 <sub>H</sub>	Reserved, do not use																										
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3 <sub>H</sub>	<b>CDTM3_DTM5_2_N, ATOM3_6_N</b> , Inverted dead-time output of ATOM3, channel 6																										
4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
5 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7																										
6 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																										
B <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM3_13</b>, Output of TOM3, channel 13</td></tr> <tr><td>2<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_3</b>, Output of TOM5, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>8<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	1 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3	5 <sub>H</sub>	Reserved, do not use	...		8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5																										
1 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																										
A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM3_14</b>, Output of TOM3, channel 14</td> </tr> <tr> <td>2<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>3<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>TOM5_4</b>, Output of TOM5, channel 4</td> </tr> <tr> <td>5<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>8<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	1 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4	5 <sub>H</sub>	Reserved, do not use	...		8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																										
1 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6																										
A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>TOM3_15</b>, Output of TOM3, channel 15</td> </tr> <tr> <td>2<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>3<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>TOM5_0</b>, Output of TOM5, channel 0</td> </tr> <tr> <td>5<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	1 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15	2 <sub>H</sub>	Reserved, do not use	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	9 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																										
1 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15																										
2 <sub>H</sub>	Reserved, do not use																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
9 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

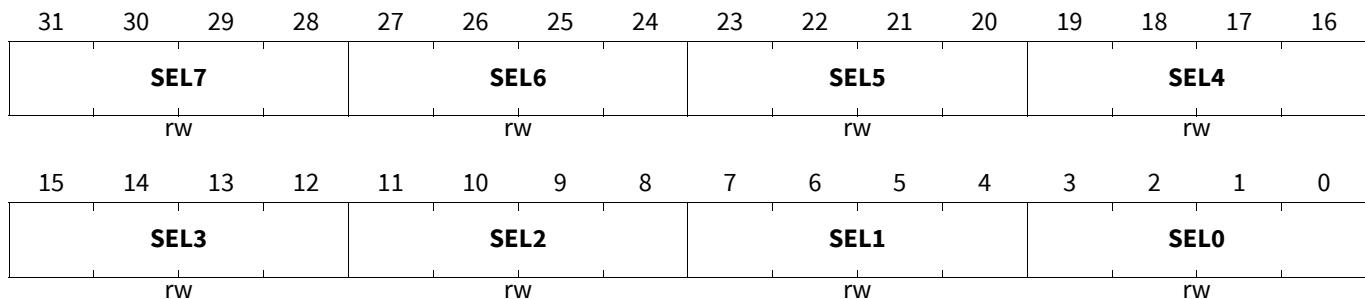
Field	Bits	Type	Description																						
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_8</b>, Output of TOM1, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_1</b>, Output of TOM5, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>8<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_8</b> , Output of TOM1, channel 8	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM5_1</b> , Output of TOM5, channel 1	5 <sub>H</sub>	Reserved, do not use	...		8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_8</b> , Output of TOM1, channel 8																								
1 <sub>H</sub>	Reserved, do not use																								
2 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																								
3 <sub>H</sub>	Reserved, do not use																								
4 <sub>H</sub>	<b>TOM5_1</b> , Output of TOM5, channel 1																								
5 <sub>H</sub>	Reserved, do not use																								
...																									
8 <sub>H</sub>	Reserved, do not use																								
9 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																								
A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																								
B <sub>H</sub>	Reserved, do not use																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_9</b>, Output of TOM1, channel 9</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_2</b>, Output of TOM5, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>8<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2	5 <sub>H</sub>	Reserved, do not use	...		8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7	A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9																								
1 <sub>H</sub>	Reserved, do not use																								
2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1																								
3 <sub>H</sub>	Reserved, do not use																								
4 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2																								
5 <sub>H</sub>	Reserved, do not use																								
...																									
8 <sub>H</sub>	Reserved, do not use																								
9 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																								
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B <sub>H</sub>	Reserved, do not use																								

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td> <td><b>TOM1_10</b>, Output of TOM1, channel 10</td> </tr> <tr> <td><math>1_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td> </tr> <tr> <td><math>3_H</math></td> <td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td> </tr> <tr> <td><math>4_H</math></td> <td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM0_DTM0_2_N, TOM0_2_N</b>, Inverted dead-time output of TOM0, channel 2</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td> </tr> <tr> <td><math>9_H</math></td> <td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td> </tr> <tr> <td><math>A_H</math></td> <td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td> </tr> <tr> <td><math>B_H</math></td> <td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td> </tr> </tbody> </table>	$0_H$	<b>TOM1_10</b> , Output of TOM1, channel 10	$1_H$	Reserved, do not use	$2_H$	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	$3_H$	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	$4_H$	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	$6_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2	$7_H$	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	$8_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	$9_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3	$A_H$	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	$B_H$	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6
$0_H$	<b>TOM1_10</b> , Output of TOM1, channel 10																										
$1_H$	Reserved, do not use																										
$2_H$	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																										
$3_H$	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
$4_H$	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
$5_H$	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
$6_H$	<b>CDTM0_DTM0_2_N, TOM0_2_N</b> , Inverted dead-time output of TOM0, channel 2																										
$7_H$	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2																										
$8_H$	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
$9_H$	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
$A_H$	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																										
$B_H$	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																										

## GTM\_TOUTSELn (n=18)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr><td>0<sub>H</sub></td><td><b>TOM1_11</b>, Output of TOM1, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM0_3_N, TOM0_3_N</b>, Inverted dead-time output of TOM0, channel 3</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM1_DTM0_3_N, TOM1_3_N</b>, Inverted dead-time output of TOM1, channel 3</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM4_0_N, ATOM2_0_N</b>, Inverted dead-time output of ATOM2, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM4_0_N, ATOM3_0_N</b>, Inverted dead-time output of ATOM3, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td></tr> </table>	0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	5 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	6 <sub>H</sub>	<b>CDTM0_DTM0_3_N, TOM0_3_N</b> , Inverted dead-time output of TOM0, channel 3	7 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3	8 <sub>H</sub>	<b>CDTM2_DTM4_0_N, ATOM2_0_N</b> , Inverted dead-time output of ATOM2, channel 0	9 <sub>H</sub>	<b>CDTM3_DTM4_0_N, ATOM3_0_N</b> , Inverted dead-time output of ATOM3, channel 0	A <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	B <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7
0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
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B <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p>																								

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_13</b>, Output of TOM1, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	9 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	A <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	B <sub>H</sub>	Reserved, do not use				
0 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																										
9 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																										
A <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_14</b>, Output of TOM1, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_0_N, TOM0_4_N</b>, Inverted dead-time output of TOM0, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_0_N, ATOM0_4_N</b>, Inverted dead-time output of ATOM0, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_0_N, ATOM1_4_N</b>, Inverted dead-time output of ATOM1, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4	5 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4	9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4	A <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM0_DTM1_0_N, TOM0_4_N</b> , Inverted dead-time output of TOM0, channel 4																										
5 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM5_0_N, ATOM0_4_N</b> , Inverted dead-time output of ATOM0, channel 4																										
9 <sub>H</sub>	<b>CDTM1_DTM5_0_N, ATOM1_4_N</b> , Inverted dead-time output of ATOM1, channel 4																										
A <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_15</b>, Output of TOM1, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_1_N, TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_1_N, TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_1_N, ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_1_N, ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5	5 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5	9 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5	A <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM0_DTM1_1_N, TOM0_5_N</b> , Inverted dead-time output of TOM0, channel 5																										
5 <sub>H</sub>	<b>CDTM1_DTM1_1_N, TOM1_5_N</b> , Inverted dead-time output of TOM1, channel 5																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM5_1_N, ATOM0_5_N</b> , Inverted dead-time output of ATOM0, channel 5																										
9 <sub>H</sub>	<b>CDTM1_DTM5_1_N, ATOM1_5_N</b> , Inverted dead-time output of ATOM1, channel 5																										
A <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_15</b>, Output of TOM2, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_0</b>, Output of ATOM7, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_2_N, TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_2_N, ATOM0_6_N</b>, Inverted dead-time output of ATOM0, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_2_N, ATOM1_6_N</b>, Inverted dead-time output of ATOM1, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6	5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6	9 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6	A <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_15</b> , Output of TOM2, channel 15																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM0_DTM1_2_N, TOM0_6_N</b> , Inverted dead-time output of TOM0, channel 6																										
5 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM0_DTM5_2_N, ATOM0_6_N</b> , Inverted dead-time output of ATOM0, channel 6																										
9 <sub>H</sub>	<b>CDTM1_DTM5_2_N, ATOM1_6_N</b> , Inverted dead-time output of ATOM1, channel 6																										
A <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_15</b>, Output of TOM1, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM0_DTM1_3_N, TOM0_7_N</b>, Inverted dead-time output of TOM0, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM0_DTM5_3_N, ATOM0_7_N</b>, Inverted dead-time output of ATOM0, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM1_DTM5_3_N, ATOM1_7_N</b>, Inverted dead-time output of ATOM1, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15	1 <sub>H</sub>	Reserved, do not use	2 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7	5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM0_DTM5_3_N, ATOM0_7_N</b> , Inverted dead-time output of ATOM0, channel 7	9 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7	A <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	B <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0
0 <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15																										
1 <sub>H</sub>	Reserved, do not use																										
2 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM0_DTM1_3_N, TOM0_7_N</b> , Inverted dead-time output of TOM0, channel 7																										
5 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
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9 <sub>H</sub>	<b>CDTM1_DTM5_3_N, ATOM1_7_N</b> , Inverted dead-time output of ATOM1, channel 7																										
A <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
B <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_14</b>, Output of TOM3, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_14</b>, Output of TOM4, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_6</b>, Output of ATOM8, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_0_N, TOM4_4_N</b>, Inverted dead-time output of TOM4, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_0_N, TOM3_4_N</b>, Inverted dead-time output of TOM3, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14	1 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14	2 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6	3 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6	4 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4	5 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4	6 <sub>H</sub>	<b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0	7 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use				
0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14																										
1 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14																										
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5 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4																										
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7 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=19)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description																								
SELx (x=0)	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr> <td>0<sub>H</sub></td><td><b>TOM3_15</b>, Output of TOM3, channel 15</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM4_15</b>, Output of TOM4, channel 15</td></tr> <tr> <td>2<sub>H</sub></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr> <td>3<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM4_DTM1_3_N, TOM4_7_N</b>, Inverted dead-time output of TOM4, channel 7</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM1_3_N, TOM3_7_N</b>, Inverted dead-time output of TOM3, channel 7</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM5_DTM5_3_N, ATOM5_7_N</b>, Inverted dead-time output of ATOM5, channel 7</td></tr> <tr> <td>B<sub>H</sub></td><td><b>CDTM6_DTM5_3_N, ATOM6_7_N</b>, Inverted dead-time output of ATOM6, channel 7</td></tr> </table>	0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15	1 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15	2 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7	3 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7	4 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7	5 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	9 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	A <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7	B <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7
0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15																										
1 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15																										
2 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7																										
3 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																										
4 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7																										
5 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
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8 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
9 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																										
A <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7																										
B <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																		
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_14</b>, Output of TOM3, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_14</b>, Output of TOM4, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_6</b>, Output of ATOM8, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_1_N, TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_1_N, TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14	1 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14	2 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6	3 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6	4 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5	5 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5	6 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14																				
1 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14																				
2 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6																				
3 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6																				
4 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5																				
5 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5																				
6 <sub>H</sub>	Reserved, do not use																				
...																					
B <sub>H</sub>	Reserved, do not use																				
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_15</b>, Output of TOM3, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_15</b>, Output of TOM4, channel 15</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_2_N, TOM4_6_N</b>, Inverted dead-time output of TOM4, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_2_N, TOM3_6_N</b>, Inverted dead-time output of TOM3, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15	1 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15	2 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7	3 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7	4 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6	5 <sub>H</sub>	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6	6 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15																				
1 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15																				
2 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7																				
3 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																				
4 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6																				
5 <sub>H</sub>	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6																				
6 <sub>H</sub>	Reserved, do not use																				
...																					
B <sub>H</sub>	Reserved, do not use																				

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_1_N, TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM1_1_N, TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_1_N, ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_1_N, ATOM6_5_N</b>, Inverted dead-time output of ATOM6, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0	1 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0	2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	3 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	4 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5	5 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5	9 <sub>H</sub>	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0																										
1 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0																										
2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
3 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																										
4 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5																										
5 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5																										
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A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_2_N, TOM3_6_N</b>, Inverted dead-time output of TOM3, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM1_2_N, TOM4_6_N</b>, Inverted dead-time output of TOM4, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_2_N, ATOM5_6_N</b>, Inverted dead-time output of ATOM5, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_2_N, ATOM6_6_N</b>, Inverted dead-time output of ATOM6, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	1 <sub>H</sub>	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1	2 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	3 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	4 <sub>H</sub>	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6	5 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6	9 <sub>H</sub>	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
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A <sub>H</sub>	Reserved, do not use																										
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**Generic Timer Module (GTM)**

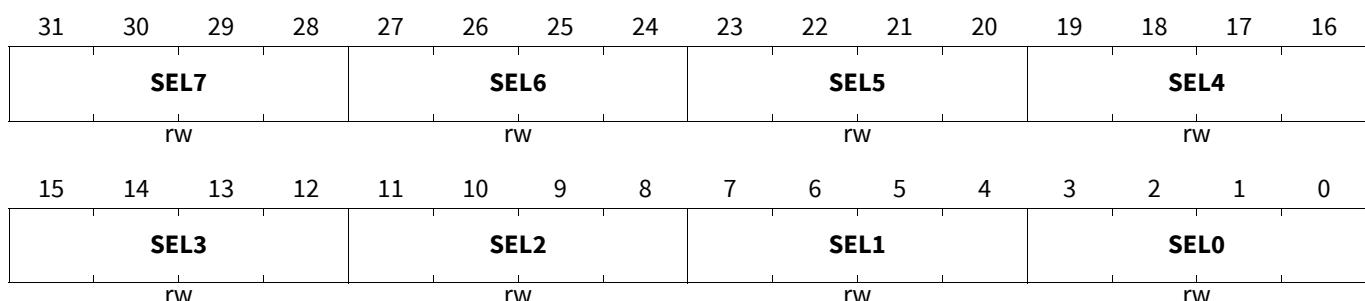
Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM3_DTM1_3_N, TOM3_7_N</b>, Inverted dead-time output of TOM3, channel 7</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM4_DTM1_3_N, TOM4_7_N</b>, Inverted dead-time output of TOM4, channel 7</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM5_DTM5_3_N, ATOM5_7_N</b>, Inverted dead-time output of ATOM5, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM6_DTM5_3_N, ATOM6_7_N</b>, Inverted dead-time output of ATOM6, channel 7</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	1 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2	2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	3 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	4 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7	5 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7	9 <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
1 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2																										
2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
3 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																										
4 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7																										
5 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7																										
9 <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td><math>0_H</math></td><td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td></tr> <tr> <td><math>1_H</math></td><td><b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4</td></tr> <tr> <td><math>2_H</math></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr> <td><math>3_H</math></td><td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td></tr> <tr> <td><math>4_H</math></td><td><b>CDTM3_DTM0_1_N, TOM3_1_N</b>, Inverted dead-time output of TOM3, channel 1</td></tr> <tr> <td><math>5_H</math></td><td><b>CDTM4_DTM0_1_N, TOM4_1_N</b>, Inverted dead-time output of TOM4, channel 1</td></tr> <tr> <td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr> <td><math>8_H</math></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr> <td><math>9_H</math></td><td><b>CDTM6_DTM4_1_N, ATOM6_1_N</b>, Inverted dead-time output of ATOM6, channel 1</td></tr> <tr> <td><math>A_H</math></td><td><b>CDTM5_DTM5_2_N, ATOM5_6_N</b>, Inverted dead-time output of ATOM5, channel 6</td></tr> <tr> <td><math>B_H</math></td><td><b>CDTM6_DTM5_2_N, ATOM6_6_N</b>, Inverted dead-time output of ATOM6, channel 6</td></tr> </tbody> </table>	$0_H$	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	$1_H$	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4	$2_H$	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	$3_H$	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	$4_H$	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1	$5_H$	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	$9_H$	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1	$A_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6	$B_H$	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6
$0_H$	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4																										
$1_H$	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4																										
$2_H$	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
$3_H$	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
$4_H$	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1																										
$5_H$	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
$9_H$	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1																										
$A_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6																										
$B_H$	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5</td></tr> <tr><td><math>1_H</math></td><td><b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td><math>3_H</math></td><td><b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM3_DTM0_2_N, TOM3_2_N</b>, Inverted dead-time output of TOM3, channel 2</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM4_DTM0_2_N, TOM4_2_N</b>, Inverted dead-time output of TOM4, channel 2</td></tr> <tr><td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM6_DTM4_2_N, ATOM6_2_N</b>, Inverted dead-time output of ATOM6, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5	$1_H$	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5	$2_H$	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	$3_H$	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5	$4_H$	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2	$5_H$	<b>CDTM4_DTM0_2_N, TOM4_2_N</b> , Inverted dead-time output of TOM4, channel 2	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	$9_H$	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
$0_H$	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5																										
$1_H$	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5																										
$2_H$	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
$3_H$	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5																										
$4_H$	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2																										
$5_H$	<b>CDTM4_DTM0_2_N, TOM4_2_N</b> , Inverted dead-time output of TOM4, channel 2																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										
$9_H$	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

**GTM\_TOUTSELn (n=20)****Timer Output Select Register**(09FD60<sub>H</sub>+n\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td><b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>CDTM3_DTM0_3_N, TOM3_3_N</b>, Inverted dead-time output of TOM3, channel 3</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM4_DTM0_3_N, TOM4_3_N</b>, Inverted dead-time output of TOM4, channel 3</td> </tr> <tr> <td>6<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM6_DTM4_3_N, ATOM6_3_N</b>, Inverted dead-time output of ATOM6, channel 3</td> </tr> <tr> <td>A<sub>H</sub></td> <td>Reserved, do not use</td> </tr> <tr> <td>B<sub>H</sub></td> <td>Reserved, do not use</td> </tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6	1 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6	2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	3 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6	4 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3	5 <sub>H</sub>	<b>CDTM4_DTM0_3_N, TOM4_3_N</b> , Inverted dead-time output of TOM4, channel 3	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	9 <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6																										
1 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6																										
2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
3 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6																										
4 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3																										
5 <sub>H</sub>	<b>CDTM4_DTM0_3_N, TOM4_3_N</b> , Inverted dead-time output of TOM4, channel 3																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
9 <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_0_N, TOM3_0_N</b>, Inverted dead-time output of TOM3, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM0_0_N, TOM4_0_N</b>, Inverted dead-time output of TOM4, channel 0</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_0_N, ATOM6_0_N</b>, Inverted dead-time output of ATOM6, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7	1 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7	2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7	3 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7	4 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0	5 <sub>H</sub>	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0	9 <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0	A <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7	B <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7
0 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7																										
1 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7																										
2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																										
3 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7																										
4 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0																										
5 <sub>H</sub>	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										
9 <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0																										
A <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7																										
B <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_8</b>, Output of TOM3, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_8</b>, Output of TOM4, channel 8</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_0</b>, Output of ATOM7, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_0</b>, Output of ATOM8, channel 0</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_1_N, ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM6_DTM5_1_N, ATOM6_5_N</b>, Inverted dead-time output of ATOM6, channel 5</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8	1 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8	2 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0	3 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0	4 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0	5 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	9 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	A <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5	B <sub>H</sub>	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5
0 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8																										
1 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8																										
2 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0																										
3 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0																										
4 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0																										
5 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
9 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																										
A <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5																										
B <sub>H</sub>	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_9</b>, Output of TOM3, channel 9</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_9</b>, Output of TOM4, channel 9</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_1</b>, Output of ATOM8, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_0_N, ATOM5_4_N</b>, Inverted dead-time output of ATOM5, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM6_DTM5_0_N, ATOM6_4_N</b>, Inverted dead-time output of ATOM6, channel 4</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9	1 <sub>H</sub>	<b>TOM4_9</b> , Output of TOM4, channel 9	2 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1	3 <sub>H</sub>	<b>ATOM8_1</b> , Output of ATOM8, channel 1	4 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	5 <sub>H</sub>	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	9 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	A <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4	B <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4
0 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9																										
1 <sub>H</sub>	<b>TOM4_9</b> , Output of TOM4, channel 9																										
2 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1																										
3 <sub>H</sub>	<b>ATOM8_1</b> , Output of ATOM8, channel 1																										
4 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
5 <sub>H</sub>	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
9 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																										
A <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4																										
B <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_10</b>, Output of TOM3, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_10</b>, Output of TOM4, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_2</b>, Output of ATOM7, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_2</b>, Output of ATOM8, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10	1 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10	2 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2	3 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2	4 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	5 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	9 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10																										
1 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10																										
2 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2																										
3 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2																										
4 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
5 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
9 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_0_N, TOM3_4_N</b>, Inverted dead-time output of TOM3, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM1_0_N, TOM4_4_N</b>, Inverted dead-time output of TOM4, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_0_N, ATOM5_4_N</b>, Inverted dead-time output of ATOM5, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_0_N, ATOM6_4_N</b>, Inverted dead-time output of ATOM6, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3	1 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3	2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	3 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	4 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4	5 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4	9 <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3																										
1 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3																										
2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
3 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																										
4 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4																										
5 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4																										
9 <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_11</b>, Output of TOM3, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_11</b>, Output of TOM4, channel 11</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_3</b>, Output of ATOM7, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_3</b>, Output of ATOM8, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_1_N, TOM4_1_N</b>, Inverted dead-time output of TOM4, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_1_N, TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM2_DTM4_2_N, ATOM2_2_N</b>, Inverted dead-time output of ATOM2, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM3_DTM4_2_N, ATOM3_2_N</b>, Inverted dead-time output of ATOM3, channel 2</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11	1 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11	2 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3	3 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3	4 <sub>H</sub>	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1	5 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	9 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2	B <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2
0 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11																										
1 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11																										
2 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3																										
3 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3																										
4 <sub>H</sub>	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1																										
5 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5																										
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9 <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																										
A <sub>H</sub>	<b>CDTM2_DTM4_2_N, ATOM2_2_N</b> , Inverted dead-time output of ATOM2, channel 2																										
B <sub>H</sub>	<b>CDTM3_DTM4_2_N, ATOM3_2_N</b> , Inverted dead-time output of ATOM3, channel 2																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM3_12</b>, Output of TOM3, channel 12</td></tr> <tr><td><math>1_H</math></td><td><b>TOM4_12</b>, Output of TOM4, channel 12</td></tr> <tr><td><math>2_H</math></td><td><b>ATOM7_4</b>, Output of ATOM7, channel 4</td></tr> <tr><td><math>3_H</math></td><td><b>ATOM8_4</b>, Output of ATOM8, channel 4</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM4_DTM0_0_N, TOM4_0_N</b>, Inverted dead-time output of TOM4, channel 0</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM2_DTM4_1_N, ATOM2_1_N</b>, Inverted dead-time output of ATOM2, channel 1</td></tr> <tr><td><math>B_H</math></td><td><b>CDTM3_DTM4_1_N, ATOM3_1_N</b>, Inverted dead-time output of ATOM3, channel 1</td></tr> </tbody> </table>	$0_H$	<b>TOM3_12</b> , Output of TOM3, channel 12	$1_H$	<b>TOM4_12</b> , Output of TOM4, channel 12	$2_H$	<b>ATOM7_4</b> , Output of ATOM7, channel 4	$3_H$	<b>ATOM8_4</b> , Output of ATOM8, channel 4	$4_H$	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0	$5_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	$9_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	$A_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1	$B_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1
$0_H$	<b>TOM3_12</b> , Output of TOM3, channel 12																										
$1_H$	<b>TOM4_12</b> , Output of TOM4, channel 12																										
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$4_H$	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0																										
$5_H$	Reserved, do not use																										
...																											
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																										
$9_H$	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																										
$A_H$	<b>CDTM2_DTM4_1_N, ATOM2_1_N</b> , Inverted dead-time output of ATOM2, channel 1																										
$B_H$	<b>CDTM3_DTM4_1_N, ATOM3_1_N</b> , Inverted dead-time output of ATOM3, channel 1																										

**GTM\_TOUTSELn (n=21)**

Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

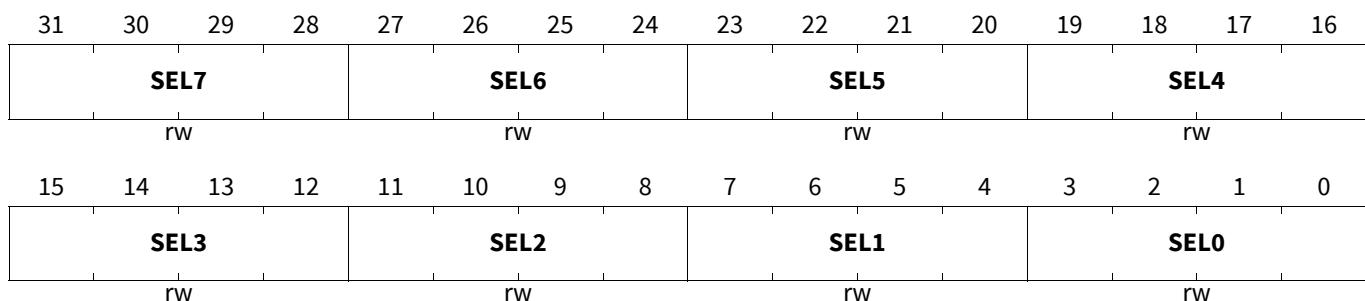
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				<b>SEL7</b>		<b>SEL6</b>		<b>SEL5</b>		<b>SEL4</b>					
				rw		rw		rw		rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				<b>SEL3</b>		<b>SEL2</b>		<b>SEL1</b>		<b>SEL0</b>					
				rw		rw		rw		rw					

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_13</b>, Output of TOM3, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_13</b>, Output of TOM4, channel 13</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_5</b>, Output of ATOM7, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_5</b>, Output of ATOM8, channel 5</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM2_DTM4_3_N, ATOM2_3_N</b>, Inverted dead-time output of ATOM2, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM3_DTM4_3_N, ATOM3_3_N</b>, Inverted dead-time output of ATOM3, channel 3</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13	1 <sub>H</sub>	<b>TOM4_13</b> , Output of TOM4, channel 13	2 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5	3 <sub>H</sub>	<b>ATOM8_5</b> , Output of ATOM8, channel 5	4 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	9 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6	A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3	B <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3		
0 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13																										
1 <sub>H</sub>	<b>TOM4_13</b> , Output of TOM4, channel 13																										
2 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5																										
3 <sub>H</sub>	<b>ATOM8_5</b> , Output of ATOM8, channel 5																										
4 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																										
9 <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																										
A <sub>H</sub>	<b>CDTM2_DTM4_3_N, ATOM2_3_N</b> , Inverted dead-time output of ATOM2, channel 3																										
B <sub>H</sub>	<b>CDTM3_DTM4_3_N, ATOM3_3_N</b> , Inverted dead-time output of ATOM3, channel 3																										
<b>SELx (x=1-5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p>																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_0</b>, Output of TOM5, channel 0</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_1_N, TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_0</b>, Output of ATOM10, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_1_N, ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0	1 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0	2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_0</b> , Output of ATOM10, channel 0	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0																										
1 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0																										
2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_0</b> , Output of ATOM10, channel 0																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_1</b>, Output of TOM5, channel 1</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM3_DTM1_2_N, TOM3_6_N</b>, Inverted dead-time output of TOM3, channel 6</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM10_1</b>, Output of ATOM10, channel 1</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM5_DTM5_2_N, ATOM5_6_N</b>, Inverted dead-time output of ATOM5, channel 6</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	$1_H$	<b>TOM5_1</b> , Output of TOM5, channel 1	$2_H$	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	$3_H$	Reserved, do not use	$4_H$	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6	$5_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM10_1</b> , Output of ATOM10, channel 1	$9_H$	Reserved, do not use	$A_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6	$B_H$	Reserved, do not use
$0_H$	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
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$A_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=22)****Timer Output Select Register**(09FD60<sub>H</sub>+n\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_2</b>, Output of TOM5, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_3_N, TOM3_7_N</b>, Inverted dead-time output of TOM3, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_2</b>, Output of ATOM10, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_3_N, ATOM5_7_N</b>, Inverted dead-time output of ATOM5, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	1 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2	2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_2</b> , Output of ATOM10, channel 2	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
1 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2																										
2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7																										
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7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_2</b> , Output of ATOM10, channel 2																										
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A <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_3</b>, Output of TOM5, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_0_N, TOM3_4_N</b>, Inverted dead-time output of TOM3, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_3</b>, Output of ATOM10, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_0_N, ATOM5_4_N</b>, Inverted dead-time output of ATOM5, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3	1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3	2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_3</b> , Output of ATOM10, channel 3	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3																										
1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3																										
2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
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...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_3</b> , Output of ATOM10, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_4</b>, Output of TOM5, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_1_N, TOM3_1_N</b>, Inverted dead-time output of TOM3, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_4</b>, Output of ATOM10, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4	2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_4</b> , Output of ATOM10, channel 4	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4																										
1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4																										
2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_4</b> , Output of ATOM10, channel 4																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_5</b>, Output of TOM5, channel 5</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_2_N, TOM3_2_N</b>, Inverted dead-time output of TOM3, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_5</b>, Output of ATOM10, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5	1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5	2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_5</b> , Output of ATOM10, channel 5	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5																										
1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5																										
2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_5</b> , Output of ATOM10, channel 5																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_6</b>, Output of TOM5, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_3_N, TOM3_3_N</b>, Inverted dead-time output of TOM3, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_6</b>, Output of ATOM10, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6	1 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6	2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_6</b> , Output of ATOM10, channel 6	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6																										
1 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6																										
2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_6</b> , Output of ATOM10, channel 6																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_7</b>, Output of TOM5, channel 7</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_0_N, TOM3_0_N</b>, Inverted dead-time output of TOM3, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_7</b>, Output of ATOM10, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7	1 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7	2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_7</b> , Output of ATOM10, channel 7	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7																										
1 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7																										
2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_7</b> , Output of ATOM10, channel 7																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM3_8</b>, Output of TOM3, channel 8</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_8</b>, Output of TOM5, channel 8</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM11_0</b>, Output of ATOM11, channel 0</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM6_DTM5_1_N, ATOM6_5_N</b>, Inverted dead-time output of ATOM6, channel 5</td></tr> <tr><td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM3_8</b> , Output of TOM3, channel 8	$1_H$	<b>TOM5_8</b> , Output of TOM5, channel 8	$2_H$	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	$3_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM11_0</b> , Output of ATOM11, channel 0	$9_H$	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM3_8</b> , Output of TOM3, channel 8																						
$1_H$	<b>TOM5_8</b> , Output of TOM5, channel 8																						
$2_H$	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																						
$3_H$	Reserved, do not use																						
...																							
$7_H$	Reserved, do not use																						
$8_H$	<b>ATOM11_0</b> , Output of ATOM11, channel 0																						
$9_H$	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5																						
$A_H$	Reserved, do not use																						
$B_H$	Reserved, do not use																						
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM3_9</b>, Output of TOM3, channel 9</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_9</b>, Output of TOM5, channel 9</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM11_1</b>, Output of ATOM11, channel 1</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM6_DTM5_2_N, ATOM6_6_N</b>, Inverted dead-time output of ATOM6, channel 6</td></tr> <tr><td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM3_9</b> , Output of TOM3, channel 9	$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9	$2_H$	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	$3_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM11_1</b> , Output of ATOM11, channel 1	$9_H$	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM3_9</b> , Output of TOM3, channel 9																						
$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9																						
$2_H$	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1																						
$3_H$	Reserved, do not use																						
...																							
$7_H$	Reserved, do not use																						
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$9_H$	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6																						
$A_H$	Reserved, do not use																						
$B_H$	Reserved, do not use																						

**GTM\_TOUTSELn (n=23)****Timer Output Select Register**(09FD60<sub>H</sub>+n\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_10</b>, Output of TOM3, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_10</b>, Output of TOM5, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_2</b>, Output of ATOM11, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_3_N, ATOM6_7_N</b>, Inverted dead-time output of ATOM6, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10	1 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10	2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2	9 <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10																						
1 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10																						
2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2																						
9 <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7																						
A <sub>H</sub>	Reserved, do not use																						
B <sub>H</sub>	Reserved, do not use																						
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_11</b>, Output of TOM3, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_11</b>, Output of TOM5, channel 11</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_3</b>, Output of ATOM11, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_0_N, ATOM6_4_N</b>, Inverted dead-time output of ATOM6, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11	1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11	2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3	9 <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11																						
1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11																						
2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3																						
9 <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4																						
A <sub>H</sub>	Reserved, do not use																						
B <sub>H</sub>	Reserved, do not use																						

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_12</b>, Output of TOM3, channel 12</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_12</b>, Output of TOM5, channel 12</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_8</b>, Output of TOM3, channel 8</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_8</b>, Output of TOM5, channel 8</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_4</b>, Output of ATOM11, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_1_N, ATOM6_1_N</b>, Inverted dead-time output of ATOM6, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_12</b> , Output of TOM3, channel 12	1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12	2 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8	5 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4	9 <sub>H</sub>	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_12</b> , Output of TOM3, channel 12																										
1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12																										
2 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8																										
5 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4																										
9 <sub>H</sub>	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_13</b>, Output of TOM3, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_13</b>, Output of TOM5, channel 13</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_9</b>, Output of TOM3, channel 9</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_9</b>, Output of TOM5, channel 9</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_5</b>, Output of ATOM11, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_2_N, ATOM6_2_N</b>, Inverted dead-time output of ATOM6, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13	1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13	2 <sub>H</sub>	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9	5 <sub>H</sub>	<b>TOM5_9</b> , Output of TOM5, channel 9	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_5</b> , Output of ATOM11, channel 5	9 <sub>H</sub>	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13																										
1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13																										
2 <sub>H</sub>	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9																										
5 <sub>H</sub>	<b>TOM5_9</b> , Output of TOM5, channel 9																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_5</b> , Output of ATOM11, channel 5																										
9 <sub>H</sub>	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_14</b>, Output of TOM3, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_14</b>, Output of TOM5, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_10</b>, Output of TOM3, channel 10</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_10</b>, Output of TOM5, channel 10</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_6</b>, Output of ATOM11, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_3_N, ATOM6_3_N</b>, Inverted dead-time output of ATOM6, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14	1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14	2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10	5 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6	9 <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14																										
1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14																										
2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10																										
5 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6																										
9 <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_15</b>, Output of TOM3, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_15</b>, Output of TOM5, channel 15</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_11</b>, Output of TOM3, channel 11</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_11</b>, Output of TOM5, channel 11</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_7</b>, Output of ATOM11, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_0_N, ATOM6_0_N</b>, Inverted dead-time output of ATOM6, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15	1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15	2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11	5 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7	9 <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15																										
1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15																										
2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11																										
5 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7																										
9 <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_0</b>, Output of TOM5, channel 0</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_0</b>, Output of ATOM7, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_1_N, TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_0</b>, Output of ATOM10, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0	1 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0	2 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_0</b> , Output of ATOM10, channel 0	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0																										
1 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0																										
2 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_0</b> , Output of ATOM10, channel 0																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_1</b>, Output of TOM5, channel 1</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_2_N, TOM4_6_N</b>, Inverted dead-time output of TOM4, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_1</b>, Output of ATOM10, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1	1 <sub>H</sub>	<b>TOM5_1</b> , Output of TOM5, channel 1	2 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_1</b> , Output of ATOM10, channel 1	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1																										
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3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6																										
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...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=24)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description																								
SELx (x=0)	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr> <td>0<sub>H</sub></td><td><b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM5_2</b>, Output of TOM5, channel 2</td></tr> <tr> <td>2<sub>H</sub></td><td><b>ATOM7_2</b>, Output of ATOM7, channel 2</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM4_DTM1_3_N, TOM4_7_N</b>, Inverted dead-time output of TOM4, channel 7</td></tr> <tr> <td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>ATOM10_2</b>, Output of ATOM10, channel 2</td></tr> <tr> <td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2	1 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2	2 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_2</b> , Output of ATOM10, channel 2	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2																										
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3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7																										
5 <sub>H</sub>	Reserved, do not use																										
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...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_3</b>, Output of TOM5, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_3</b>, Output of ATOM7, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_0_N, TOM4_4_N</b>, Inverted dead-time output of TOM4, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_3</b>, Output of ATOM10, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3	1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3	2 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_3</b> , Output of ATOM10, channel 3	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3																										
1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3																										
2 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4																										
5 <sub>H</sub>	Reserved, do not use																										
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9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_4</b>, Output of TOM5, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_4</b>, Output of ATOM7, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_1_N, TOM4_1_N</b>, Inverted dead-time output of TOM4, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_4</b>, Output of ATOM10, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4	1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4	2 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_4</b> , Output of ATOM10, channel 4	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4																										
1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4																										
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9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_5</b>, Output of TOM5, channel 5</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_5</b>, Output of ATOM7, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_2_N, TOM4_2_N</b>, Inverted dead-time output of TOM4, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_5</b>, Output of ATOM10, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5	1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5	2 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_2_N, TOM4_2_N</b> , Inverted dead-time output of TOM4, channel 2	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_5</b> , Output of ATOM10, channel 5	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5																										
1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5																										
2 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
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7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_5</b> , Output of ATOM10, channel 5																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_6</b>, Output of TOM5, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_3_N, TOM4_3_N</b>, Inverted dead-time output of TOM4, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_6</b>, Output of ATOM10, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6	1 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6	2 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_3_N, TOM4_3_N</b> , Inverted dead-time output of TOM4, channel 3	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_6</b> , Output of ATOM10, channel 6	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6																										
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## Generic Timer Module (GTM)

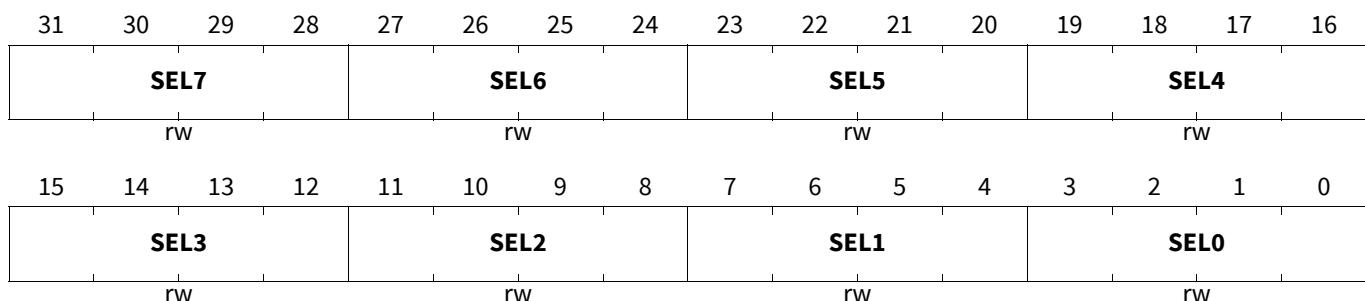
Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_7</b>, Output of TOM5, channel 7</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_0_N, TOM4_0_N</b>, Inverted dead-time output of TOM4, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_7</b>, Output of ATOM10, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7	1 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7	2 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_7</b> , Output of ATOM10, channel 7	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7																										
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...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_8</b>, Output of TOM4, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_8</b>, Output of TOM5, channel 8</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_0</b>, Output of ATOM8, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_0</b>, Output of ATOM11, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8	1 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8	2 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_0</b> , Output of ATOM11, channel 0	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use				
0 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8																										
1 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8																										
2 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0																										
3 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_0</b> , Output of ATOM11, channel 0																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM4_9</b>, Output of TOM4, channel 9</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_9</b>, Output of TOM5, channel 9</td></tr> <tr><td><math>2_H</math></td><td><b>ATOM8_1</b>, Output of ATOM8, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM11_1</b>, Output of ATOM11, channel 1</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM4_9</b> , Output of TOM4, channel 9	$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9	$2_H$	<b>ATOM8_1</b> , Output of ATOM8, channel 1	$3_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM11_1</b> , Output of ATOM11, channel 1	$9_H$	Reserved, do not use	...		$B_H$	Reserved, do not use
$0_H$	<b>TOM4_9</b> , Output of TOM4, channel 9																						
$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9																						
$2_H$	<b>ATOM8_1</b> , Output of ATOM8, channel 1																						
$3_H$	Reserved, do not use																						
...																							
$7_H$	Reserved, do not use																						
$8_H$	<b>ATOM11_1</b> , Output of ATOM11, channel 1																						
$9_H$	Reserved, do not use																						
...																							
$B_H$	Reserved, do not use																						

**GTM\_TOUTSELn (n=25)**

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

Field	Bits	Type	Description																				
<b>SELx (x=0)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM4_10</b>, Output of TOM4, channel 10</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_10</b>, Output of TOM5, channel 10</td></tr> <tr><td><math>2_H</math></td><td><b>ATOM8_2</b>, Output of ATOM8, channel 2</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM11_2</b>, Output of ATOM11, channel 2</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM4_10</b> , Output of TOM4, channel 10	$1_H$	<b>TOM5_10</b> , Output of TOM5, channel 10	$2_H$	<b>ATOM8_2</b> , Output of ATOM8, channel 2	$3_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM11_2</b> , Output of ATOM11, channel 2	$9_H$	Reserved, do not use	...		$B_H$	Reserved, do not use
$0_H$	<b>TOM4_10</b> , Output of TOM4, channel 10																						
$1_H$	<b>TOM5_10</b> , Output of TOM5, channel 10																						
$2_H$	<b>ATOM8_2</b> , Output of ATOM8, channel 2																						
$3_H$	Reserved, do not use																						
...																							
$7_H$	Reserved, do not use																						
$8_H$	<b>ATOM11_2</b> , Output of ATOM11, channel 2																						
$9_H$	Reserved, do not use																						
...																							
$B_H$	Reserved, do not use																						

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_11</b>, Output of TOM4, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_11</b>, Output of TOM5, channel 11</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_3</b>, Output of ATOM8, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_3</b>, Output of ATOM11, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11	1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11	2 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use				
0 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11																										
1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11																										
2 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3																										
3 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_12</b>, Output of TOM4, channel 12</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_12</b>, Output of TOM5, channel 12</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_4</b>, Output of ATOM8, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM4_8</b>, Output of TOM4, channel 8</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_8</b>, Output of TOM5, channel 8</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_4</b>, Output of ATOM11, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_12</b> , Output of TOM4, channel 12	1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12	2 <sub>H</sub>	<b>ATOM8_4</b> , Output of ATOM8, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8	5 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_12</b> , Output of TOM4, channel 12																										
1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12																										
2 <sub>H</sub>	<b>ATOM8_4</b> , Output of ATOM8, channel 4																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8																										
5 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

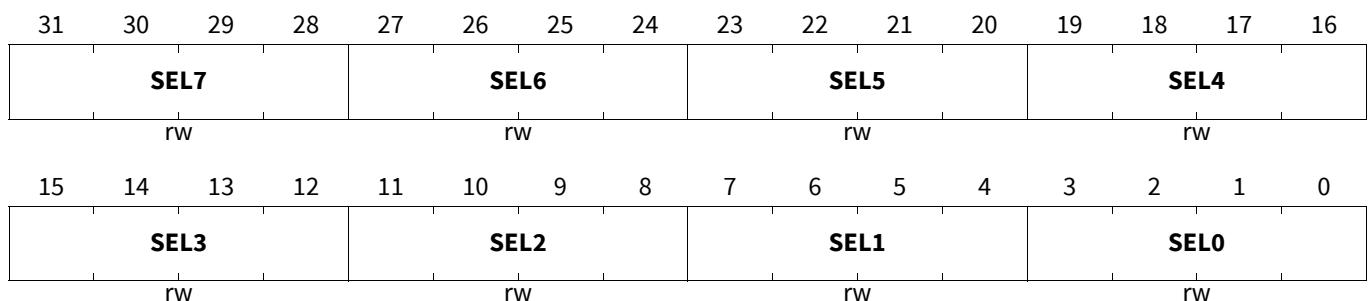
Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_13</b>, Output of TOM4, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_13</b>, Output of TOM5, channel 13</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_5</b>, Output of ATOM8, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM4_9</b>, Output of TOM4, channel 9</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_9</b>, Output of TOM5, channel 9</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_5</b>, Output of ATOM11, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_13</b> , Output of TOM4, channel 13	1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13	2 <sub>H</sub>	<b>ATOM8_5</b> , Output of ATOM8, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM4_9</b> , Output of TOM4, channel 9	5 <sub>H</sub>	<b>TOM5_9</b> , Output of TOM5, channel 9	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_5</b> , Output of ATOM11, channel 5	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_13</b> , Output of TOM4, channel 13																										
1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13																										
2 <sub>H</sub>	<b>ATOM8_5</b> , Output of ATOM8, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM4_9</b> , Output of TOM4, channel 9																										
5 <sub>H</sub>	<b>TOM5_9</b> , Output of TOM5, channel 9																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_5</b> , Output of ATOM11, channel 5																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_14</b>, Output of TOM4, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_14</b>, Output of TOM5, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_6</b>, Output of ATOM8, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM4_10</b>, Output of TOM4, channel 10</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_10</b>, Output of TOM5, channel 10</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_6</b>, Output of ATOM11, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14	1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14	2 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10	5 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14																										
1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14																										
2 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10																										
5 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_15</b>, Output of TOM4, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_15</b>, Output of TOM5, channel 15</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM4_11</b>, Output of TOM4, channel 11</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_11</b>, Output of TOM5, channel 11</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_7</b>, Output of ATOM11, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15	1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15	2 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11	5 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15																										
1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15																										
2 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11																										
5 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_0</b>, Output of TOM5, channel 0</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_1_N, TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_0</b>, Output of ATOM9, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_1_N, ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0	1 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0	2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_0</b> , Output of ATOM9, channel 0	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_0, TOM3_0</b> , Dead-time output of TOM3, channel 0																										
1 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0																										
2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_0</b> , Output of ATOM9, channel 0																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM5_1_N, ATOM5_5_N</b> , Inverted dead-time output of ATOM5, channel 5																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_1</b>, Output of TOM5, channel 1</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM3_DTM1_2_N, TOM3_6_N</b>, Inverted dead-time output of TOM3, channel 6</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM9_1</b>, Output of ATOM9, channel 1</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM5_DTM5_2_N, ATOM5_6_N</b>, Inverted dead-time output of ATOM5, channel 6</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	$1_H$	<b>TOM5_1</b> , Output of TOM5, channel 1	$2_H$	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	$3_H$	Reserved, do not use	$4_H$	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6	$5_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM9_1</b> , Output of ATOM9, channel 1	$9_H$	Reserved, do not use	$A_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6	$B_H$	Reserved, do not use
$0_H$	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
$1_H$	<b>TOM5_1</b> , Output of TOM5, channel 1																										
$2_H$	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
$3_H$	Reserved, do not use																										
$4_H$	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6																										
$5_H$	Reserved, do not use																										
...																											
$7_H$	Reserved, do not use																										
$8_H$	<b>ATOM9_1</b> , Output of ATOM9, channel 1																										
$9_H$	Reserved, do not use																										
$A_H$	<b>CDTM5_DTM5_2_N, ATOM5_6_N</b> , Inverted dead-time output of ATOM5, channel 6																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=26)****Timer Output Select Register**(09FD60<sub>H</sub>+n\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_2</b>, Output of TOM5, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_3_N, TOM3_7_N</b>, Inverted dead-time output of TOM3, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_2</b>, Output of ATOM9, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_3_N, ATOM5_7_N</b>, Inverted dead-time output of ATOM5, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	1 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2	2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_2</b> , Output of ATOM9, channel 2	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
1 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2																										
2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_2</b> , Output of ATOM9, channel 2																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM5_3_N, ATOM5_7_N</b> , Inverted dead-time output of ATOM5, channel 7																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_3</b>, Output of TOM5, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM1_0_N, TOM3_4_N</b>, Inverted dead-time output of TOM3, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_3</b>, Output of ATOM9, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM5_0_N, ATOM5_4_N</b>, Inverted dead-time output of ATOM5, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3	1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3	2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_3</b> , Output of ATOM9, channel 3	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3																										
1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3																										
2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_3</b> , Output of ATOM9, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_4</b>, Output of TOM5, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_1_N, TOM3_1_N</b>, Inverted dead-time output of TOM3, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_4</b>, Output of ATOM9, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4	2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_4</b> , Output of ATOM9, channel 4	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4																										
1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4																										
2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_4</b> , Output of ATOM9, channel 4																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_5</b>, Output of TOM5, channel 5</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_2_N, TOM3_2_N</b>, Inverted dead-time output of TOM3, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_5</b>, Output of ATOM9, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5	1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5	2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_5</b> , Output of ATOM9, channel 5	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5																										
1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5																										
2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2																										
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7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_5</b> , Output of ATOM9, channel 5																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_6</b>, Output of TOM5, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_3_N, TOM3_3_N</b>, Inverted dead-time output of TOM3, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_6</b>, Output of ATOM9, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>TOM5_3_N</b>, Inverted output of TOM5, channel 3 (OUT_T output)</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6	1 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6	2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_6</b> , Output of ATOM9, channel 6	9 <sub>H</sub>	<b>TOM5_3_N</b> , Inverted output of TOM5, channel 3 (OUT_T output)	A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6																										
1 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6																										
2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_6</b> , Output of ATOM9, channel 6																										
9 <sub>H</sub>	<b>TOM5_3_N</b> , Inverted output of TOM5, channel 3 (OUT_T output)																										
A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_7</b>, Output of TOM5, channel 7</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_0_N, TOM3_0_N</b>, Inverted dead-time output of TOM3, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_7</b>, Output of ATOM9, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7	1 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7	2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_7</b> , Output of ATOM9, channel 7	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7																										
1 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7																										
2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM3_DTM0_0_N, TOM3_0_N</b> , Inverted dead-time output of TOM3, channel 0																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_7</b> , Output of ATOM9, channel 7																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM3_8</b>, Output of TOM3, channel 8</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_8</b>, Output of TOM5, channel 8</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM11_0</b>, Output of ATOM11, channel 0</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM6_DTM5_1_N, ATOM6_5_N</b>, Inverted dead-time output of ATOM6, channel 5</td></tr> <tr><td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM3_8</b> , Output of TOM3, channel 8	$1_H$	<b>TOM5_8</b> , Output of TOM5, channel 8	$2_H$	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	$3_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM11_0</b> , Output of ATOM11, channel 0	$9_H$	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM3_8</b> , Output of TOM3, channel 8																						
$1_H$	<b>TOM5_8</b> , Output of TOM5, channel 8																						
$2_H$	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																						
$3_H$	Reserved, do not use																						
...																							
$7_H$	Reserved, do not use																						
$8_H$	<b>ATOM11_0</b> , Output of ATOM11, channel 0																						
$9_H$	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5																						
$A_H$	Reserved, do not use																						
$B_H$	Reserved, do not use																						
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM3_9</b>, Output of TOM3, channel 9</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_9</b>, Output of TOM5, channel 9</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM11_1</b>, Output of ATOM11, channel 1</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM6_DTM5_2_N, ATOM6_6_N</b>, Inverted dead-time output of ATOM6, channel 6</td></tr> <tr><td><math>A_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM3_9</b> , Output of TOM3, channel 9	$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9	$2_H$	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	$3_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM11_1</b> , Output of ATOM11, channel 1	$9_H$	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6	$A_H$	Reserved, do not use	$B_H$	Reserved, do not use
$0_H$	<b>TOM3_9</b> , Output of TOM3, channel 9																						
$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9																						
$2_H$	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1																						
$3_H$	Reserved, do not use																						
...																							
$7_H$	Reserved, do not use																						
$8_H$	<b>ATOM11_1</b> , Output of ATOM11, channel 1																						
$9_H$	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6																						
$A_H$	Reserved, do not use																						
$B_H$	Reserved, do not use																						

**GTM\_TOUTSELn (n=27)****Timer Output Select Register**(09FD60<sub>H</sub>+n\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_10</b>, Output of TOM3, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_10</b>, Output of TOM5, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_2</b>, Output of ATOM11, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_3_N, ATOM6_7_N</b>, Inverted dead-time output of ATOM6, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10	1 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10	2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2	9 <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10																						
1 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10																						
2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2																						
9 <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7																						
A <sub>H</sub>	Reserved, do not use																						
B <sub>H</sub>	Reserved, do not use																						
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_11</b>, Output of TOM3, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_11</b>, Output of TOM5, channel 11</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_3</b>, Output of ATOM11, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_0_N, ATOM6_4_N</b>, Inverted dead-time output of ATOM6, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11	1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11	2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3	9 <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11																						
1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11																						
2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3																						
9 <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4																						
A <sub>H</sub>	Reserved, do not use																						
B <sub>H</sub>	Reserved, do not use																						

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_12</b>, Output of TOM3, channel 12</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_12</b>, Output of TOM5, channel 12</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_8</b>, Output of TOM3, channel 8</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_8</b>, Output of TOM5, channel 8</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_4</b>, Output of ATOM11, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_1_N, ATOM6_1_N</b>, Inverted dead-time output of ATOM6, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_12</b> , Output of TOM3, channel 12	1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12	2 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8	5 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4	9 <sub>H</sub>	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_12</b> , Output of TOM3, channel 12																										
1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12																										
2 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8																										
5 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4																										
9 <sub>H</sub>	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_13</b>, Output of TOM3, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_13</b>, Output of TOM5, channel 13</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_9</b>, Output of TOM3, channel 9</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_9</b>, Output of TOM5, channel 9</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_5</b>, Output of ATOM11, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_2_N, ATOM6_2_N</b>, Inverted dead-time output of ATOM6, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13	1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13	2 <sub>H</sub>	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9	5 <sub>H</sub>	<b>TOM5_9</b> , Output of TOM5, channel 9	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_5</b> , Output of ATOM11, channel 5	9 <sub>H</sub>	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13																										
1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13																										
2 <sub>H</sub>	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9																										
5 <sub>H</sub>	<b>TOM5_9</b> , Output of TOM5, channel 9																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_5</b> , Output of ATOM11, channel 5																										
9 <sub>H</sub>	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_14</b>, Output of TOM3, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_14</b>, Output of TOM5, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_10</b>, Output of TOM3, channel 10</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_10</b>, Output of TOM5, channel 10</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_6</b>, Output of ATOM11, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_3_N, ATOM6_3_N</b>, Inverted dead-time output of ATOM6, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14	1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14	2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10	5 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6	9 <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14																										
1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14																										
2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10																										
5 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6																										
9 <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM3_15</b>, Output of TOM3, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_15</b>, Output of TOM5, channel 15</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM3_11</b>, Output of TOM3, channel 11</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_11</b>, Output of TOM5, channel 11</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_7</b>, Output of ATOM11, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM4_0_N, ATOM6_0_N</b>, Inverted dead-time output of ATOM6, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15	1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15	2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11	5 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7	9 <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM3_15</b> , Output of TOM3, channel 15																										
1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15																										
2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11																										
5 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_7</b> , Output of ATOM11, channel 7																										
9 <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_0</b>, Output of TOM5, channel 0</td></tr> <tr><td><math>2_H</math></td><td><b>ATOM7_0</b>, Output of ATOM7, channel 0</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM4_DTM1_1_N, TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM9_0</b>, Output of ATOM9, channel 0</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0	$1_H$	<b>TOM5_0</b> , Output of TOM5, channel 0	$2_H$	<b>ATOM7_0</b> , Output of ATOM7, channel 0	$3_H$	Reserved, do not use	$4_H$	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5	$5_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM9_0</b> , Output of ATOM9, channel 0	$9_H$	Reserved, do not use	...		$B_H$	Reserved, do not use
$0_H$	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0																										
$1_H$	<b>TOM5_0</b> , Output of TOM5, channel 0																										
$2_H$	<b>ATOM7_0</b> , Output of ATOM7, channel 0																										
$3_H$	Reserved, do not use																										
$4_H$	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5																										
$5_H$	Reserved, do not use																										
...																											
$7_H$	Reserved, do not use																										
$8_H$	<b>ATOM9_0</b> , Output of ATOM9, channel 0																										
$9_H$	Reserved, do not use																										
...																											
$B_H$	Reserved, do not use																										
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_1</b>, Output of TOM5, channel 1</td></tr> <tr><td><math>2_H</math></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM4_DTM1_2_N, TOM4_6_N</b>, Inverted dead-time output of TOM4, channel 6</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM9_1</b>, Output of ATOM9, channel 1</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1	$1_H$	<b>TOM5_1</b> , Output of TOM5, channel 1	$2_H$	<b>ATOM7_1</b> , Output of ATOM7, channel 1	$3_H$	Reserved, do not use	$4_H$	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6	$5_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>ATOM9_1</b> , Output of ATOM9, channel 1	$9_H$	Reserved, do not use	...		$B_H$	Reserved, do not use
$0_H$	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1																										
$1_H$	<b>TOM5_1</b> , Output of TOM5, channel 1																										
$2_H$	<b>ATOM7_1</b> , Output of ATOM7, channel 1																										
$3_H$	Reserved, do not use																										
$4_H$	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6																										
$5_H$	Reserved, do not use																										
...																											
$7_H$	Reserved, do not use																										
$8_H$	<b>ATOM9_1</b> , Output of ATOM9, channel 1																										
$9_H$	Reserved, do not use																										
...																											
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=28)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description																								
SELx (x=0)	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr> <td>0<sub>H</sub></td><td><b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM5_2</b>, Output of TOM5, channel 2</td></tr> <tr> <td>2<sub>H</sub></td><td><b>ATOM7_2</b>, Output of ATOM7, channel 2</td></tr> <tr> <td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM4_DTM1_3_N, TOM4_7_N</b>, Inverted dead-time output of TOM4, channel 7</td></tr> <tr> <td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>ATOM9_2</b>, Output of ATOM9, channel 2</td></tr> <tr> <td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2	1 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2	2 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_2</b> , Output of ATOM9, channel 2	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2																										
1 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2																										
2 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2																										
3 <sub>H</sub>	Reserved, do not use																										
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5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_2</b> , Output of ATOM9, channel 2																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_3</b>, Output of TOM5, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_3</b>, Output of ATOM7, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_0_N, TOM4_4_N</b>, Inverted dead-time output of TOM4, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_3</b>, Output of ATOM9, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3	1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3	2 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_3</b> , Output of ATOM9, channel 3	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3																										
1 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3																										
2 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_3</b> , Output of ATOM9, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_4</b>, Output of TOM5, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_4</b>, Output of ATOM7, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_1_N, TOM4_1_N</b>, Inverted dead-time output of TOM4, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_4</b>, Output of ATOM9, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4	1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4	2 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_4</b> , Output of ATOM9, channel 4	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4																										
1 <sub>H</sub>	<b>TOM5_4</b> , Output of TOM5, channel 4																										
2 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_4</b> , Output of ATOM9, channel 4																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

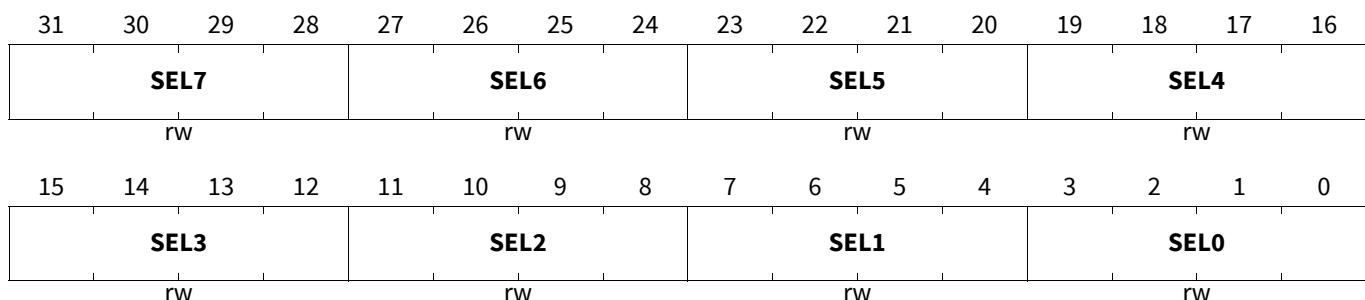
Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_5</b>, Output of TOM5, channel 5</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_5</b>, Output of ATOM7, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_2_N, TOM4_2_N</b>, Inverted dead-time output of TOM4, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_5</b>, Output of ATOM9, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5	1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5	2 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_2_N, TOM4_2_N</b> , Inverted dead-time output of TOM4, channel 2	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_5</b> , Output of ATOM9, channel 5	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5																										
1 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5																										
2 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM0_2_N, TOM4_2_N</b> , Inverted dead-time output of TOM4, channel 2																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_5</b> , Output of ATOM9, channel 5																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_6</b>, Output of TOM5, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_3_N, TOM4_3_N</b>, Inverted dead-time output of TOM4, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_6</b>, Output of ATOM9, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6	1 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6	2 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_3_N, TOM4_3_N</b> , Inverted dead-time output of TOM4, channel 3	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_6</b> , Output of ATOM9, channel 6	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6																										
1 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6																										
2 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM0_3_N, TOM4_3_N</b> , Inverted dead-time output of TOM4, channel 3																										
5 <sub>H</sub>	Reserved, do not use																										
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...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_7</b>, Output of TOM5, channel 7</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM0_0_N, TOM4_0_N</b>, Inverted dead-time output of TOM4, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM9_7</b>, Output of ATOM9, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7	1 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7	2 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM9_7</b> , Output of ATOM9, channel 7	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7																										
1 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7																										
2 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM9_7</b> , Output of ATOM9, channel 7																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_8</b>, Output of TOM4, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_8</b>, Output of TOM5, channel 8</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_0</b>, Output of ATOM8, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM4_12</b>, Output of TOM4, channel 12</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_12</b>, Output of TOM5, channel 12</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_0</b>, Output of ATOM10, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8	1 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8	2 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM4_12</b> , Output of TOM4, channel 12	5 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_0</b> , Output of ATOM10, channel 0	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8																										
1 <sub>H</sub>	<b>TOM5_8</b> , Output of TOM5, channel 8																										
2 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM4_12</b> , Output of TOM4, channel 12																										
5 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_0</b> , Output of ATOM10, channel 0																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM4_9</b>, Output of TOM4, channel 9</td></tr> <tr><td><math>1_H</math></td><td><b>TOM5_9</b>, Output of TOM5, channel 9</td></tr> <tr><td><math>2_H</math></td><td><b>ATOM8_1</b>, Output of ATOM8, channel 1</td></tr> <tr><td><math>3_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>4_H</math></td><td><b>TOM4_13</b>, Output of TOM4, channel 13</td></tr> <tr><td><math>5_H</math></td><td><b>TOM5_13</b>, Output of TOM5, channel 13</td></tr> <tr><td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM10_1</b>, Output of ATOM10, channel 1</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM4_9</b> , Output of TOM4, channel 9	$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9	$2_H$	<b>ATOM8_1</b> , Output of ATOM8, channel 1	$3_H$	Reserved, do not use	$4_H$	<b>TOM4_13</b> , Output of TOM4, channel 13	$5_H$	<b>TOM5_13</b> , Output of TOM5, channel 13	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>ATOM10_1</b> , Output of ATOM10, channel 1	$9_H$	Reserved, do not use	...		$B_H$	Reserved, do not use
$0_H$	<b>TOM4_9</b> , Output of TOM4, channel 9																										
$1_H$	<b>TOM5_9</b> , Output of TOM5, channel 9																										
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$3_H$	Reserved, do not use																										
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...																											
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=29)****Timer Output Select Register****(09FD60<sub>H</sub>+n\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_10</b>, Output of TOM4, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_10</b>, Output of TOM5, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_2</b>, Output of ATOM8, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM4_14</b>, Output of TOM4, channel 14</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_14</b>, Output of TOM5, channel 14</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_2</b>, Output of ATOM10, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10	1 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10	2 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14	5 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_2</b> , Output of ATOM10, channel 2	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10																										
1 <sub>H</sub>	<b>TOM5_10</b> , Output of TOM5, channel 10																										
2 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14																										
5 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14																										
6 <sub>H</sub>	Reserved, do not use																										
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...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_11</b>, Output of TOM4, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_11</b>, Output of TOM5, channel 11</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_3</b>, Output of ATOM8, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM4_15</b>, Output of TOM4, channel 15</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM5_15</b>, Output of TOM5, channel 15</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_3</b>, Output of ATOM10, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11	1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11	2 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3	3 <sub>H</sub>	Reserved, do not use	4 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15	5 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_3</b> , Output of ATOM10, channel 3	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_11</b> , Output of TOM4, channel 11																										
1 <sub>H</sub>	<b>TOM5_11</b> , Output of TOM5, channel 11																										
2 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3																										
3 <sub>H</sub>	Reserved, do not use																										
4 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15																										
5 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM10_3</b> , Output of ATOM10, channel 3																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_12</b>, Output of TOM4, channel 12</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_12</b>, Output of TOM5, channel 12</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_4</b>, Output of ATOM8, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_4</b>, Output of ATOM10, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_12</b> , Output of TOM4, channel 12	1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12	2 <sub>H</sub>	<b>ATOM8_4</b> , Output of ATOM8, channel 4	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_4</b> , Output of ATOM10, channel 4	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_12</b> , Output of TOM4, channel 12																						
1 <sub>H</sub>	<b>TOM5_12</b> , Output of TOM5, channel 12																						
2 <sub>H</sub>	<b>ATOM8_4</b> , Output of ATOM8, channel 4																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM10_4</b> , Output of ATOM10, channel 4																						
9 <sub>H</sub>	Reserved, do not use																						
...																							
B <sub>H</sub>	Reserved, do not use																						
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_13</b>, Output of TOM4, channel 13</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_13</b>, Output of TOM5, channel 13</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_5</b>, Output of ATOM8, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_5</b>, Output of ATOM10, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_13</b> , Output of TOM4, channel 13	1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13	2 <sub>H</sub>	<b>ATOM8_5</b> , Output of ATOM8, channel 5	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_5</b> , Output of ATOM10, channel 5	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_13</b> , Output of TOM4, channel 13																						
1 <sub>H</sub>	<b>TOM5_13</b> , Output of TOM5, channel 13																						
2 <sub>H</sub>	<b>ATOM8_5</b> , Output of ATOM8, channel 5																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM10_5</b> , Output of ATOM10, channel 5																						
9 <sub>H</sub>	Reserved, do not use																						
...																							
B <sub>H</sub>	Reserved, do not use																						
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM4_14</b>, Output of TOM4, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_14</b>, Output of TOM5, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_6</b>, Output of ATOM8, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_6</b>, Output of ATOM10, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14	1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14	2 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_6</b> , Output of ATOM10, channel 6	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14																						
1 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14																						
2 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM10_6</b> , Output of ATOM10, channel 6																						
9 <sub>H</sub>	Reserved, do not use																						
...																							
B <sub>H</sub>	Reserved, do not use																						

## Generic Timer Module (GTM)

Field	Bits	Type	Description																				
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr><td>0<sub>H</sub></td><td><b>TOM4_15</b>, Output of TOM4, channel 15</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM5_15</b>, Output of TOM5, channel 15</td></tr> <tr><td>2<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM10_7</b>, Output of ATOM10, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15	1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15	2 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7	3 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM10_7</b> , Output of ATOM10, channel 7	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM4_15</b> , Output of TOM4, channel 15																						
1 <sub>H</sub>	<b>TOM5_15</b> , Output of TOM5, channel 15																						
2 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																						
3 <sub>H</sub>	Reserved, do not use																						
...																							
7 <sub>H</sub>	Reserved, do not use																						
8 <sub>H</sub>	<b>ATOM10_7</b> , Output of ATOM10, channel 7																						
9 <sub>H</sub>	Reserved, do not use																						
...																							
B <sub>H</sub>	Reserved, do not use																						
<b>SELx (x=6-7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p>																				

## GTM\_TOUTSELn (n=30)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
rw				rw				rw				rw			

Field	Bits	Type	Description
<b>SELx (x=0-1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_0</b>, Output of TOM5, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_2_N, TOM3_6_N</b>, Inverted dead-time output of TOM3, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_2_N, TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM8_0</b>, Output of ATOM8, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM11_0</b>, Output of ATOM11, channel 0</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1	1 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	2 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	3 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1	4 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0	5 <sub>H</sub>	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6	6 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	9 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0	A <sub>H</sub>	<b>ATOM11_0</b> , Output of ATOM11, channel 0	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1																										
1 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
2 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
3 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1																										
4 <sub>H</sub>	<b>TOM5_0</b> , Output of TOM5, channel 0																										
5 <sub>H</sub>	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6																										
6 <sub>H</sub>	<b>CDTM1_DTM1_2_N, TOM1_6_N</b> , Inverted dead-time output of TOM1, channel 6																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																										
9 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0																										
A <sub>H</sub>	<b>ATOM11_0</b> , Output of ATOM11, channel 0																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_2</b>, Output of ATOM7, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_1</b>, Output of TOM5, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_3_N, TOM3_7_N</b>, Inverted dead-time output of TOM3, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_3_N, TOM1_7_N</b>, Inverted dead-time output of TOM1, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM8_5</b>, Output of ATOM8, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM11_1</b>, Output of ATOM11, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2	1 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	3 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2	4 <sub>H</sub>	<b>TOM5_1</b> , Output of TOM5, channel 1	5 <sub>H</sub>	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7	6 <sub>H</sub>	<b>CDTM1_DTM1_3_N, TOM1_7_N</b> , Inverted dead-time output of TOM1, channel 7	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5	9 <sub>H</sub>	<b>ATOM8_5</b> , Output of ATOM8, channel 5	A <sub>H</sub>	<b>ATOM11_1</b> , Output of ATOM11, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2																										
1 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
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B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_3</b>, Output of ATOM7, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_2</b>, Output of TOM5, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_0_N, TOM3_4_N</b>, Inverted dead-time output of TOM3, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM1_0_N, TOM1_4_N</b>, Inverted dead-time output of TOM1, channel 4</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM11_2</b>, Output of ATOM11, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3	1 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3	2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	3 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3	4 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2	5 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4	6 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7	9 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7	A <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3																										
1 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3																										
2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
3 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3																										
4 <sub>H</sub>	<b>TOM5_2</b> , Output of TOM5, channel 2																										
5 <sub>H</sub>	<b>CDTM3_DTM1_0_N, TOM3_4_N</b> , Inverted dead-time output of TOM3, channel 4																										
6 <sub>H</sub>	<b>CDTM1_DTM1_0_N, TOM1_4_N</b> , Inverted dead-time output of TOM1, channel 4																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7																										
9 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																										
A <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_4</b>, Output of ATOM7, channel 4</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM0_1_N, TOM3_1_N</b>, Inverted dead-time output of TOM3, channel 1</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM0_1_N, TOM1_1_N</b>, Inverted dead-time output of TOM1, channel 1</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM11_3</b>, Output of ATOM11, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4	1 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4	2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	3 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1	6 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	9 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1	A <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4																										
1 <sub>H</sub>	<b>CDTM3_DTM1_0, TOM3_4</b> , Dead-time output of TOM3, channel 4																										
2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
3 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1																										
6 <sub>H</sub>	<b>CDTM1_DTM0_1_N, TOM1_1_N</b> , Inverted dead-time output of TOM1, channel 1																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
9 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1																										
A <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_5</b>, Output of ATOM7, channel 5</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM0_2_N, TOM3_2_N</b>, Inverted dead-time output of TOM3, channel 2</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM0_2_N, TOM1_2_N</b>, Inverted dead-time output of TOM1, channel 2</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_2</b>, Output of ATOM7, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM11_4</b>, Output of ATOM11, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5	1 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5	2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	3 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2	6 <sub>H</sub>	<b>CDTM1_DTM0_2_N, TOM1_2_N</b> , Inverted dead-time output of TOM1, channel 2	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	9 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2	A <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5																										
1 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5																										
2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
3 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5																										
4 <sub>H</sub>	Reserved, do not use																										
5 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2																										
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7 <sub>H</sub>	Reserved, do not use																										
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9 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2																										
A <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=7)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM0_3_N, TOM3_3_N</b>, Inverted dead-time output of TOM3, channel 3</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM1_DTM0_3_N, TOM1_3_N</b>, Inverted dead-time output of TOM1, channel 3</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_3</b>, Output of ATOM7, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM11_5</b>, Output of ATOM11, channel 5</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	1 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6	2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	3 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6	4 <sub>H</sub>	Reserved, do not use	5 <sub>H</sub>	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3	6 <sub>H</sub>	<b>CDTM1_DTM0_3_N, TOM1_3_N</b> , Inverted dead-time output of TOM1, channel 3	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	9 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3	A <sub>H</sub>	<b>ATOM11_5</b> , Output of ATOM11, channel 5	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																										
1 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6																										
2 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
3 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6																										
4 <sub>H</sub>	Reserved, do not use																										
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9 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3																										
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B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

## GTM\_TOUTSELn (n=31)

## Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description																						
SELx (x=0)	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr> <td>0<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> <tr> <td>3<sub>H</sub></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr> <td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr> <td>9<sub>H</sub></td><td><b>ATOM7_4</b>, Output of ATOM7, channel 4</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	1 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7	2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7	3 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7	4 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	9 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4	A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																								
1 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7																								
2 <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																								
3 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7																								
4 <sub>H</sub>	Reserved, do not use																								
...																									
7 <sub>H</sub>	Reserved, do not use																								
8 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																								
9 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4																								
A <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																								
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_8</b>, Output of TOM1, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM3_8</b>, Output of TOM3, channel 8</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_0</b>, Output of ATOM7, channel 0</td></tr> <tr><td>4<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_8</b> , Output of TOM1, channel 8	1 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8	2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	3 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0	4 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	9 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6	A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>TOM1_8</b> , Output of TOM1, channel 8																										
1 <sub>H</sub>	<b>TOM3_8</b> , Output of TOM3, channel 8																										
2 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
3 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0																										
4 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
9 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6																										
A <sub>H</sub>	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_0</b>, Output of ATOM8, channel 0</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_1_N, TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM1_1_N, TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM6_DTM5_1_N, ATOM6_5_N</b>, Inverted dead-time output of ATOM6, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0	1 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0	2 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0	3 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0	4 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5	5 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	9 <sub>H</sub>	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5	A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0																										
1 <sub>H</sub>	<b>CDTM4_DTM0_0, TOM4_0</b> , Dead-time output of TOM4, channel 0																										
2 <sub>H</sub>	<b>CDTM6_DTM4_0, ATOM6_0</b> , Dead-time output of ATOM6, channel 0																										
3 <sub>H</sub>	<b>ATOM8_0</b> , Output of ATOM8, channel 0																										
4 <sub>H</sub>	<b>CDTM2_DTM1_1_N, TOM2_5_N</b> , Inverted dead-time output of TOM2, channel 5																										
5 <sub>H</sub>	<b>CDTM4_DTM1_1_N, TOM4_5_N</b> , Inverted dead-time output of TOM4, channel 5																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
9 <sub>H</sub>	<b>CDTM6_DTM5_1_N, ATOM6_5_N</b> , Inverted dead-time output of ATOM6, channel 5																										
A <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_1</b>, Output of ATOM8, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_2_N, TOM2_6_N</b>, Inverted dead-time output of TOM2, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM1_2_N, TOM4_6_N</b>, Inverted dead-time output of TOM4, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>8<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_5</b>, Output of ATOM7, channel 5</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM5_2_N, ATOM6_6_N</b>, Inverted dead-time output of ATOM6, channel 6</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1	1 <sub>H</sub>	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1	2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	3 <sub>H</sub>	<b>ATOM8_1</b> , Output of ATOM8, channel 1	4 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6	5 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6	6 <sub>H</sub>	Reserved, do not use	...		8 <sub>H</sub>	Reserved, do not use	9 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5	A <sub>H</sub>	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1																										
1 <sub>H</sub>	<b>CDTM4_DTM0_1, TOM4_1</b> , Dead-time output of TOM4, channel 1																										
2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1																										
3 <sub>H</sub>	<b>ATOM8_1</b> , Output of ATOM8, channel 1																										
4 <sub>H</sub>	<b>CDTM2_DTM1_2_N, TOM2_6_N</b> , Inverted dead-time output of TOM2, channel 6																										
5 <sub>H</sub>	<b>CDTM4_DTM1_2_N, TOM4_6_N</b> , Inverted dead-time output of TOM4, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
...																											
8 <sub>H</sub>	Reserved, do not use																										
9 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5																										
A <sub>H</sub>	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_2</b>, Output of ATOM8, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_3_N, TOM2_7_N</b>, Inverted dead-time output of TOM2, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM1_3_N, TOM4_7_N</b>, Inverted dead-time output of TOM4, channel 7</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM5_3_N, ATOM6_7_N</b>, Inverted dead-time output of ATOM6, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2	1 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2	2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	3 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2	4 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7	5 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7	6 <sub>H</sub>	Reserved, do not use	...		9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7	B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2																										
1 <sub>H</sub>	<b>CDTM4_DTM0_2, TOM4_2</b> , Dead-time output of TOM4, channel 2																										
2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																										
3 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2																										
4 <sub>H</sub>	<b>CDTM2_DTM1_3_N, TOM2_7_N</b> , Inverted dead-time output of TOM2, channel 7																										
5 <sub>H</sub>	<b>CDTM4_DTM1_3_N, TOM4_7_N</b> , Inverted dead-time output of TOM4, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
...																											
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_3</b>, Output of ATOM8, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM1_0_N, TOM2_4_N</b>, Inverted dead-time output of TOM2, channel 4</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM1_0_N, TOM4_4_N</b>, Inverted dead-time output of TOM4, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM5_0_N, ATOM6_4_N</b>, Inverted dead-time output of ATOM6, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3	1 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3	2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	3 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3	4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4	5 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	9 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1	A <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3																										
1 <sub>H</sub>	<b>CDTM4_DTM0_3, TOM4_3</b> , Dead-time output of TOM4, channel 3																										
2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																										
3 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3																										
4 <sub>H</sub>	<b>CDTM2_DTM1_0_N, TOM2_4_N</b> , Inverted dead-time output of TOM2, channel 4																										
5 <sub>H</sub>	<b>CDTM4_DTM1_0_N, TOM4_4_N</b> , Inverted dead-time output of TOM4, channel 4																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
9 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1																										
A <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=6)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_4</b>, Output of ATOM8, channel 4</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_1_N, TOM2_1_N</b>, Inverted dead-time output of TOM2, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM0_1_N, TOM4_1_N</b>, Inverted dead-time output of TOM4, channel 1</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_2</b>, Output of ATOM7, channel 2</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM4_1_N, ATOM6_1_N</b>, Inverted dead-time output of ATOM6, channel 1</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4	1 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4	2 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	3 <sub>H</sub>	<b>ATOM8_4</b> , Output of ATOM8, channel 4	4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1	5 <sub>H</sub>	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	9 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2	A <sub>H</sub>	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4																										
1 <sub>H</sub>	<b>CDTM4_DTM1_0, TOM4_4</b> , Dead-time output of TOM4, channel 4																										
2 <sub>H</sub>	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
3 <sub>H</sub>	<b>ATOM8_4</b> , Output of ATOM8, channel 4																										
4 <sub>H</sub>	<b>CDTM2_DTM0_1_N, TOM2_1_N</b> , Inverted dead-time output of TOM2, channel 1																										
5 <sub>H</sub>	<b>CDTM4_DTM0_1_N, TOM4_1_N</b> , Inverted dead-time output of TOM4, channel 1																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
9 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2																										
A <sub>H</sub>	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tr><td><math>0_H</math></td><td><b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</td></tr> <tr><td><math>1_H</math></td><td><b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</td></tr> <tr><td><math>3_H</math></td><td><b>ATOM8_5</b>, Output of ATOM8, channel 5</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM2_DTM0_2_N, TOM2_2_N</b>, Inverted dead-time output of TOM2, channel 2</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM4_DTM0_2_N, TOM4_2_N</b>, Inverted dead-time output of TOM4, channel 2</td></tr> <tr><td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td><math>9_H</math></td><td><b>ATOM7_3</b>, Output of ATOM7, channel 3</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM6_DTM4_2_N, ATOM6_2_N</b>, Inverted dead-time output of ATOM6, channel 2</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </table>	$0_H$	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5	$1_H$	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5	$2_H$	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5	$3_H$	<b>ATOM8_5</b> , Output of ATOM8, channel 5	$4_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2	$5_H$	<b>CDTM4_DTM0_2_N, TOM4_2_N</b> , Inverted dead-time output of TOM4, channel 2	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	$9_H$	<b>ATOM7_3</b> , Output of ATOM7, channel 3	$A_H$	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2	$B_H$	Reserved, do not use
$0_H$	<b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5																										
$1_H$	<b>CDTM4_DTM1_1, TOM4_5</b> , Dead-time output of TOM4, channel 5																										
$2_H$	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5																										
$3_H$	<b>ATOM8_5</b> , Output of ATOM8, channel 5																										
$4_H$	<b>CDTM2_DTM0_2_N, TOM2_2_N</b> , Inverted dead-time output of TOM2, channel 2																										
$5_H$	<b>CDTM4_DTM0_2_N, TOM4_2_N</b> , Inverted dead-time output of TOM4, channel 2																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
$9_H$	<b>ATOM7_3</b> , Output of ATOM7, channel 3																										
$A_H$	<b>CDTM6_DTM4_2_N, ATOM6_2_N</b> , Inverted dead-time output of ATOM6, channel 2																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=32)**

Timer Output Select Register

(09FD60<sub>H</sub>+n\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				<b>SEL7</b>		<b>SEL6</b>		<b>SEL5</b>		<b>SEL4</b>					
				rw		rw		rw		rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				<b>SEL3</b>		<b>SEL2</b>		<b>SEL1</b>		<b>SEL0</b>					
				rw		rw		rw		rw					

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_6</b>, Output of ATOM8, channel 6</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_3_N, TOM2_3_N</b>, Inverted dead-time output of TOM2, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM0_3_N, TOM4_3_N</b>, Inverted dead-time output of TOM4, channel 3</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM4_3_N, ATOM6_3_N</b>, Inverted dead-time output of ATOM6, channel 3</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	1 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6	2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6	3 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6	4 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3	5 <sub>H</sub>	<b>CDTM4_DTM0_3_N, TOM4_3_N</b> , Inverted dead-time output of TOM4, channel 3	6 <sub>H</sub>	Reserved, do not use	...		9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3	B <sub>H</sub>	Reserved, do not use		
0 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
1 <sub>H</sub>	<b>CDTM4_DTM1_2, TOM4_6</b> , Dead-time output of TOM4, channel 6																										
2 <sub>H</sub>	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6																										
3 <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6																										
4 <sub>H</sub>	<b>CDTM2_DTM0_3_N, TOM2_3_N</b> , Inverted dead-time output of TOM2, channel 3																										
5 <sub>H</sub>	<b>CDTM4_DTM0_3_N, TOM4_3_N</b> , Inverted dead-time output of TOM4, channel 3																										
6 <sub>H</sub>	Reserved, do not use																										
...																											
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p>																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_8</b>, Output of TOM2, channel 8</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_8</b>, Output of TOM4, channel 8</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_1</b>, Output of ATOM8, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_3</b>, Output of TOM5, channel 3</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_0</b>, Output of ATOM7, channel 0</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM5_2_N, ATOM6_6_N</b>, Inverted dead-time output of ATOM6, channel 6</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8	1 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8	2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1	3 <sub>H</sub>	<b>ATOM8_1</b> , Output of ATOM8, channel 1	4 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	9 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0	A <sub>H</sub>	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_8</b> , Output of TOM2, channel 8																										
1 <sub>H</sub>	<b>TOM4_8</b> , Output of TOM4, channel 8																										
2 <sub>H</sub>	<b>CDTM6_DTM4_1, ATOM6_1</b> , Dead-time output of ATOM6, channel 1																										
3 <sub>H</sub>	<b>ATOM8_1</b> , Output of ATOM8, channel 1																										
4 <sub>H</sub>	<b>TOM5_3</b> , Output of TOM5, channel 3																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																										
9 <sub>H</sub>	<b>ATOM7_0</b> , Output of ATOM7, channel 0																										
A <sub>H</sub>	<b>CDTM6_DTM5_2_N, ATOM6_6_N</b> , Inverted dead-time output of ATOM6, channel 6																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

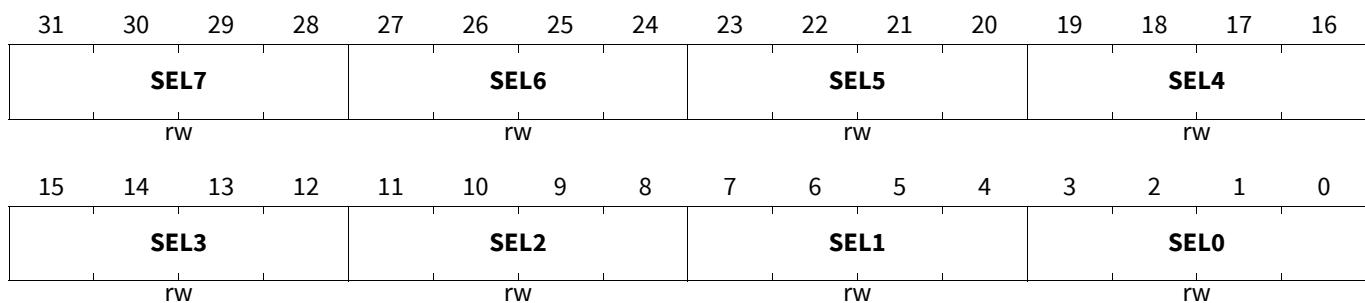
Field	Bits	Type	Description																								
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_9</b>, Output of TOM2, channel 9</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_9</b>, Output of TOM4, channel 9</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_2</b>, Output of ATOM8, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_6</b>, Output of TOM5, channel 6</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM5_3_N, ATOM6_7_N</b>, Inverted dead-time output of ATOM6, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9	1 <sub>H</sub>	<b>TOM4_9</b> , Output of TOM4, channel 9	2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2	3 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2	4 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_9</b> , Output of TOM2, channel 9																										
1 <sub>H</sub>	<b>TOM4_9</b> , Output of TOM4, channel 9																										
2 <sub>H</sub>	<b>CDTM6_DTM4_2, ATOM6_2</b> , Dead-time output of ATOM6, channel 2																										
3 <sub>H</sub>	<b>ATOM8_2</b> , Output of ATOM8, channel 2																										
4 <sub>H</sub>	<b>TOM5_6</b> , Output of TOM5, channel 6																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM6_DTM5_3_N, ATOM6_7_N</b> , Inverted dead-time output of ATOM6, channel 7																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_10</b>, Output of TOM2, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_10</b>, Output of TOM4, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_3</b>, Output of ATOM8, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM5_5</b>, Output of TOM5, channel 5</td></tr> <tr><td>5<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM5_0_N, ATOM6_4_N</b>, Inverted dead-time output of ATOM6, channel 4</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10	1 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10	2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3	3 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3	4 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5	5 <sub>H</sub>	Reserved, do not use	...		7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	9 <sub>H</sub>	Reserved, do not use	A <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_10</b> , Output of TOM2, channel 10																										
1 <sub>H</sub>	<b>TOM4_10</b> , Output of TOM4, channel 10																										
2 <sub>H</sub>	<b>CDTM6_DTM4_3, ATOM6_3</b> , Dead-time output of ATOM6, channel 3																										
3 <sub>H</sub>	<b>ATOM8_3</b> , Output of ATOM8, channel 3																										
4 <sub>H</sub>	<b>TOM5_5</b> , Output of TOM5, channel 5																										
5 <sub>H</sub>	Reserved, do not use																										
...																											
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
9 <sub>H</sub>	Reserved, do not use																										
A <sub>H</sub>	<b>CDTM6_DTM5_0_N, ATOM6_4_N</b> , Inverted dead-time output of ATOM6, channel 4																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=5)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM2_11</b>, Output of TOM2, channel 11</td></tr> <tr><td><math>1_H</math></td><td><b>TOM4_11</b>, Output of TOM4, channel 11</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</td></tr> <tr><td><math>3_H</math></td><td><b>ATOM8_4</b>, Output of ATOM8, channel 4</td></tr> <tr><td><math>4_H</math></td><td><b>TOM5_4</b>, Output of TOM5, channel 4</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td></tr> <tr><td><math>9_H</math></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM6_DTM4_1_N, ATOM6_1_N</b>, Inverted dead-time output of ATOM6, channel 1</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM2_11</b> , Output of TOM2, channel 11	$1_H$	<b>TOM4_11</b> , Output of TOM4, channel 11	$2_H$	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4	$3_H$	<b>ATOM8_4</b> , Output of ATOM8, channel 4	$4_H$	<b>TOM5_4</b> , Output of TOM5, channel 4	$5_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0	$9_H$	<b>ATOM7_7</b> , Output of ATOM7, channel 7	$A_H$	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1	$B_H$	Reserved, do not use
$0_H$	<b>TOM2_11</b> , Output of TOM2, channel 11																										
$1_H$	<b>TOM4_11</b> , Output of TOM4, channel 11																										
$2_H$	<b>CDTM6_DTM5_0, ATOM6_4</b> , Dead-time output of ATOM6, channel 4																										
$3_H$	<b>ATOM8_4</b> , Output of ATOM8, channel 4																										
$4_H$	<b>TOM5_4</b> , Output of TOM5, channel 4																										
$5_H$	Reserved, do not use																										
...																											
$7_H$	Reserved, do not use																										
$8_H$	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										
$9_H$	<b>ATOM7_7</b> , Output of ATOM7, channel 7																										
$A_H$	<b>CDTM6_DTM4_1_N, ATOM6_1_N</b> , Inverted dead-time output of ATOM6, channel 1																										
$B_H$	Reserved, do not use																										
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM2_12</b>, Output of TOM2, channel 12</td></tr> <tr><td><math>1_H</math></td><td><b>TOM4_12</b>, Output of TOM4, channel 12</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</td></tr> <tr><td><math>3_H</math></td><td><b>ATOM8_5</b>, Output of ATOM8, channel 5</td></tr> <tr><td><math>4_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM2_12</b> , Output of TOM2, channel 12	$1_H$	<b>TOM4_12</b> , Output of TOM4, channel 12	$2_H$	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5	$3_H$	<b>ATOM8_5</b> , Output of ATOM8, channel 5	$4_H$	Reserved, do not use	...		$B_H$	Reserved, do not use										
$0_H$	<b>TOM2_12</b> , Output of TOM2, channel 12																										
$1_H$	<b>TOM4_12</b> , Output of TOM4, channel 12																										
$2_H$	<b>CDTM6_DTM5_1, ATOM6_5</b> , Dead-time output of ATOM6, channel 5																										
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$4_H$	Reserved, do not use																										
...																											
$B_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM2_13</b>, Output of TOM2, channel 13</td></tr> <tr><td><math>1_H</math></td><td><b>TOM4_13</b>, Output of TOM4, channel 13</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</td></tr> <tr><td><math>3_H</math></td><td><b>ATOM8_6</b>, Output of ATOM8, channel 6</td></tr> <tr><td><math>4_H</math></td><td><b>TOM5_7</b>, Output of TOM5, channel 7</td></tr> <tr><td><math>5_H</math></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td><math>9_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>A_H</math></td><td><b>CDTM6_DTM4_3_N, ATOM6_3_N</b>, Inverted dead-time output of ATOM6, channel 3</td></tr> <tr><td><math>B_H</math></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM2_13</b> , Output of TOM2, channel 13	$1_H$	<b>TOM4_13</b> , Output of TOM4, channel 13	$2_H$	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6	$3_H$	<b>ATOM8_6</b> , Output of ATOM8, channel 6	$4_H$	<b>TOM5_7</b> , Output of TOM5, channel 7	$5_H$	Reserved, do not use	...		$7_H$	Reserved, do not use	$8_H$	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	$9_H$	Reserved, do not use	$A_H$	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3	$B_H$	Reserved, do not use
$0_H$	<b>TOM2_13</b> , Output of TOM2, channel 13																										
$1_H$	<b>TOM4_13</b> , Output of TOM4, channel 13																										
$2_H$	<b>CDTM6_DTM5_2, ATOM6_6</b> , Dead-time output of ATOM6, channel 6																										
$3_H$	<b>ATOM8_6</b> , Output of ATOM8, channel 6																										
$4_H$	<b>TOM5_7</b> , Output of TOM5, channel 7																										
$5_H$	Reserved, do not use																										
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$8_H$	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
$9_H$	Reserved, do not use																										
$A_H$	<b>CDTM6_DTM4_3_N, ATOM6_3_N</b> , Inverted dead-time output of ATOM6, channel 3																										
$B_H$	Reserved, do not use																										

**GTM\_TOUTSELn (n=33)****Timer Output Select Register****(09FD60<sub>H</sub>+n\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM2_14</b>, Output of TOM2, channel 14</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM4_14</b>, Output of TOM4, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM2_DTM0_0_N, TOM2_0_N</b>, Inverted dead-time output of TOM2, channel 0</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM0_0_N, TOM4_0_N</b>, Inverted dead-time output of TOM4, channel 0</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM4_0_N, ATOM5_0_N</b>, Inverted dead-time output of ATOM5, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM6_DTM4_0_N, ATOM6_0_N</b>, Inverted dead-time output of ATOM6, channel 0</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14	1 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14	2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7	3 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7	4 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0	5 <sub>H</sub>	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0	6 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	7 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7	8 <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0	9 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	A <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM2_14</b> , Output of TOM2, channel 14																										
1 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14																										
2 <sub>H</sub>	<b>CDTM6_DTM5_3, ATOM6_7</b> , Dead-time output of ATOM6, channel 7																										
3 <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																										
4 <sub>H</sub>	<b>CDTM2_DTM0_0_N, TOM2_0_N</b> , Inverted dead-time output of TOM2, channel 0																										
5 <sub>H</sub>	<b>CDTM4_DTM0_0_N, TOM4_0_N</b> , Inverted dead-time output of TOM4, channel 0																										
6 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
7 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7																										
8 <sub>H</sub>	<b>CDTM5_DTM4_0_N, ATOM5_0_N</b> , Inverted dead-time output of ATOM5, channel 0																										
9 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
A <sub>H</sub>	<b>CDTM6_DTM4_0_N, ATOM6_0_N</b> , Inverted dead-time output of ATOM6, channel 0																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>  This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_9</b>, Output of TOM1, channel 9</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM3_9</b>, Output of TOM3, channel 9</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_1</b>, Output of ATOM7, channel 1</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_0</b>, Output of ATOM11, channel 0</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9	1 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9	2 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	3 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1	4 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1	5 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_0</b> , Output of ATOM11, channel 0	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_9</b> , Output of TOM1, channel 9																										
1 <sub>H</sub>	<b>TOM3_9</b> , Output of TOM3, channel 9																										
2 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																										
3 <sub>H</sub>	<b>ATOM7_1</b> , Output of ATOM7, channel 1																										
4 <sub>H</sub>	<b>CDTM3_DTM0_1, TOM3_1</b> , Dead-time output of TOM3, channel 1																										
5 <sub>H</sub>	<b>CDTM3_DTM1_1, TOM3_5</b> , Dead-time output of TOM3, channel 5																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_0</b> , Output of ATOM11, channel 0																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
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## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=2)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_10</b>, Output of TOM1, channel 10</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM3_10</b>, Output of TOM3, channel 10</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_2</b>, Output of ATOM7, channel 2</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_1</b>, Output of ATOM11, channel 1</td></tr> <tr><td>9<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>...</td><td></td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_10</b> , Output of TOM1, channel 10	1 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10	2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	3 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2	4 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2	5 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_1</b> , Output of ATOM11, channel 1	9 <sub>H</sub>	Reserved, do not use	...		B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_10</b> , Output of TOM1, channel 10																										
1 <sub>H</sub>	<b>TOM3_10</b> , Output of TOM3, channel 10																										
2 <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																										
3 <sub>H</sub>	<b>ATOM7_2</b> , Output of ATOM7, channel 2																										
4 <sub>H</sub>	<b>CDTM3_DTM0_2, TOM3_2</b> , Dead-time output of TOM3, channel 2																										
5 <sub>H</sub>	<b>CDTM3_DTM1_2, TOM3_6</b> , Dead-time output of TOM3, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_1</b> , Output of ATOM11, channel 1																										
9 <sub>H</sub>	Reserved, do not use																										
...																											
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=3)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>TOM1_11</b>, Output of TOM1, channel 11</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM3_11</b>, Output of TOM3, channel 11</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>3<sub>H</sub></td><td><b>ATOM7_3</b>, Output of ATOM7, channel 3</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM3_DTM0_2_N, TOM3_2_N</b>, Inverted dead-time output of TOM3, channel 2</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM3_DTM1_2_N, TOM3_6_N</b>, Inverted dead-time output of TOM3, channel 6</td></tr> <tr><td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM11_4</b>, Output of ATOM11, channel 4</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM5_DTM5_0_N, ATOM5_4_N</b>, Inverted dead-time output of ATOM5, channel 4</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11	1 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11	2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	3 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3	4 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2	5 <sub>H</sub>	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4	9 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_11</b> , Output of TOM1, channel 11																										
1 <sub>H</sub>	<b>TOM3_11</b> , Output of TOM3, channel 11																										
2 <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																										
3 <sub>H</sub>	<b>ATOM7_3</b> , Output of ATOM7, channel 3																										
4 <sub>H</sub>	<b>CDTM3_DTM0_2_N, TOM3_2_N</b> , Inverted dead-time output of TOM3, channel 2																										
5 <sub>H</sub>	<b>CDTM3_DTM1_2_N, TOM3_6_N</b> , Inverted dead-time output of TOM3, channel 6																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_4</b> , Output of ATOM11, channel 4																										
9 <sub>H</sub>	<b>CDTM5_DTM5_0_N, ATOM5_4_N</b> , Inverted dead-time output of ATOM5, channel 4																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

## Generic Timer Module (GTM)

Field	Bits	Type	Description																								
<b>SELx (x=4)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>TOM1_12</b>, Output of TOM1, channel 12</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM3_12</b>, Output of TOM3, channel 12</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr> <td>3<sub>H</sub></td><td><b>ATOM7_4</b>, Output of ATOM7, channel 4</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM3_DTM0_1_N, TOM3_1_N</b>, Inverted dead-time output of TOM3, channel 1</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM1_1_N, TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>ATOM11_3</b>, Output of ATOM11, channel 3</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM5_DTM4_1_N, ATOM5_1_N</b>, Inverted dead-time output of ATOM5, channel 1</td></tr> <tr> <td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_12</b> , Output of TOM1, channel 12	1 <sub>H</sub>	<b>TOM3_12</b> , Output of TOM3, channel 12	2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	3 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4	4 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1	5 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3	9 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_12</b> , Output of TOM1, channel 12																										
1 <sub>H</sub>	<b>TOM3_12</b> , Output of TOM3, channel 12																										
2 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4																										
3 <sub>H</sub>	<b>ATOM7_4</b> , Output of ATOM7, channel 4																										
4 <sub>H</sub>	<b>CDTM3_DTM0_1_N, TOM3_1_N</b> , Inverted dead-time output of TOM3, channel 1																										
5 <sub>H</sub>	<b>CDTM3_DTM1_1_N, TOM3_5_N</b> , Inverted dead-time output of TOM3, channel 5																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_3</b> , Output of ATOM11, channel 3																										
9 <sub>H</sub>	<b>CDTM5_DTM4_1_N, ATOM5_1_N</b> , Inverted dead-time output of ATOM5, channel 1																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=5)</b>	4*x+3:4*x	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td><td><b>TOM1_13</b>, Output of TOM1, channel 13</td></tr> <tr> <td>1<sub>H</sub></td><td><b>TOM3_13</b>, Output of TOM3, channel 13</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr> <td>3<sub>H</sub></td><td><b>ATOM7_5</b>, Output of ATOM7, channel 5</td></tr> <tr> <td>4<sub>H</sub></td><td><b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</td></tr> <tr> <td>6<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>7<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>8<sub>H</sub></td><td><b>ATOM11_2</b>, Output of ATOM11, channel 2</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM5_DTM4_2_N, ATOM5_2_N</b>, Inverted dead-time output of ATOM5, channel 2</td></tr> <tr> <td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr> <td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13	1 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13	2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	3 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5	4 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3	5 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7	6 <sub>H</sub>	Reserved, do not use	7 <sub>H</sub>	Reserved, do not use	8 <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2	9 <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13																										
1 <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13																										
2 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5																										
3 <sub>H</sub>	<b>ATOM7_5</b> , Output of ATOM7, channel 5																										
4 <sub>H</sub>	<b>CDTM3_DTM0_3, TOM3_3</b> , Dead-time output of TOM3, channel 3																										
5 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7																										
6 <sub>H</sub>	Reserved, do not use																										
7 <sub>H</sub>	Reserved, do not use																										
8 <sub>H</sub>	<b>ATOM11_2</b> , Output of ATOM11, channel 2																										
9 <sub>H</sub>	<b>CDTM5_DTM4_2_N, ATOM5_2_N</b> , Inverted dead-time output of ATOM5, channel 2																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=6)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <table> <tbody> <tr><td><math>0_H</math></td><td><b>TOM1_14</b>, Output of TOM1, channel 14</td></tr> <tr><td><math>1_H</math></td><td><b>TOM3_14</b>, Output of TOM3, channel 14</td></tr> <tr><td><math>2_H</math></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td><math>3_H</math></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td><math>4_H</math></td><td><b>CDTM3_DTM0_3_N, TOM3_3_N</b>, Inverted dead-time output of TOM3, channel 3</td></tr> <tr><td><math>5_H</math></td><td><b>CDTM3_DTM1_3_N, TOM3_7_N</b>, Inverted dead-time output of TOM3, channel 7</td></tr> <tr><td><math>6_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>7_H</math></td><td>Reserved, do not use</td></tr> <tr><td><math>8_H</math></td><td><b>ATOM11_5</b>, Output of ATOM11, channel 5</td></tr> <tr><td><math>9_H</math></td><td><b>CDTM5_DTM4_3_N, ATOM5_3_N</b>, Inverted dead-time output of ATOM5, channel 3</td></tr> <tr><td>A<sub>H</sub></td><td>Reserved, do not use</td></tr> <tr><td>B<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	$0_H$	<b>TOM1_14</b> , Output of TOM1, channel 14	$1_H$	<b>TOM3_14</b> , Output of TOM3, channel 14	$2_H$	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	$3_H$	<b>ATOM7_6</b> , Output of ATOM7, channel 6	$4_H$	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3	$5_H$	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7	$6_H$	Reserved, do not use	$7_H$	Reserved, do not use	$8_H$	<b>ATOM11_5</b> , Output of ATOM11, channel 5	$9_H$	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3	A <sub>H</sub>	Reserved, do not use	B <sub>H</sub>	Reserved, do not use
$0_H$	<b>TOM1_14</b> , Output of TOM1, channel 14																										
$1_H$	<b>TOM3_14</b> , Output of TOM3, channel 14																										
$2_H$	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6																										
$3_H$	<b>ATOM7_6</b> , Output of ATOM7, channel 6																										
$4_H$	<b>CDTM3_DTM0_3_N, TOM3_3_N</b> , Inverted dead-time output of TOM3, channel 3																										
$5_H$	<b>CDTM3_DTM1_3_N, TOM3_7_N</b> , Inverted dead-time output of TOM3, channel 7																										
$6_H$	Reserved, do not use																										
$7_H$	Reserved, do not use																										
$8_H$	<b>ATOM11_5</b> , Output of ATOM11, channel 5																										
$9_H$	<b>CDTM5_DTM4_3_N, ATOM5_3_N</b> , Inverted dead-time output of ATOM5, channel 3																										
A <sub>H</sub>	Reserved, do not use																										
B <sub>H</sub>	Reserved, do not use																										
<b>SELx (x=7)</b>	$4^*x+3:4^*x$	rw	<p><b>TOUT(n*8 + x) Output Selection</b>            This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p>																								

## Generic Timer Module (GTM)

## 26.3.4 GTM DTMAUXINSEL Connections

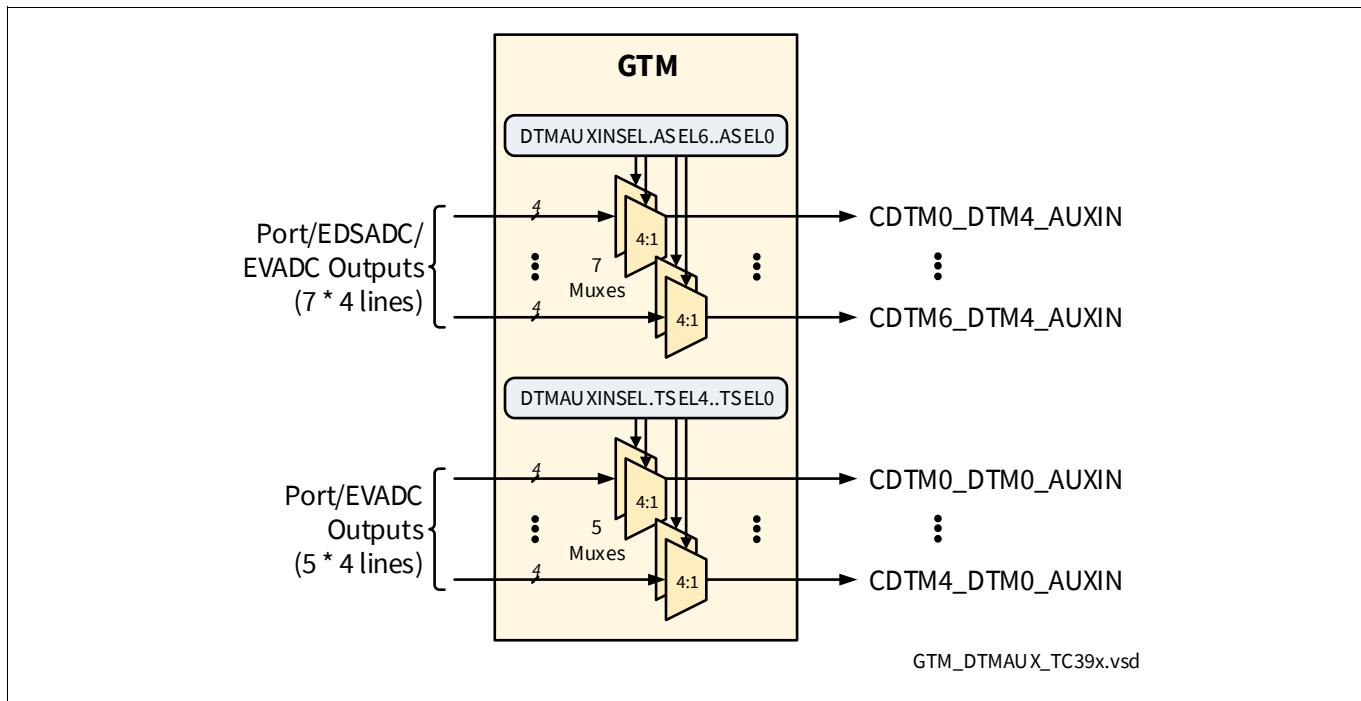


Figure 14 DTM\_AUXIN Connections Overview

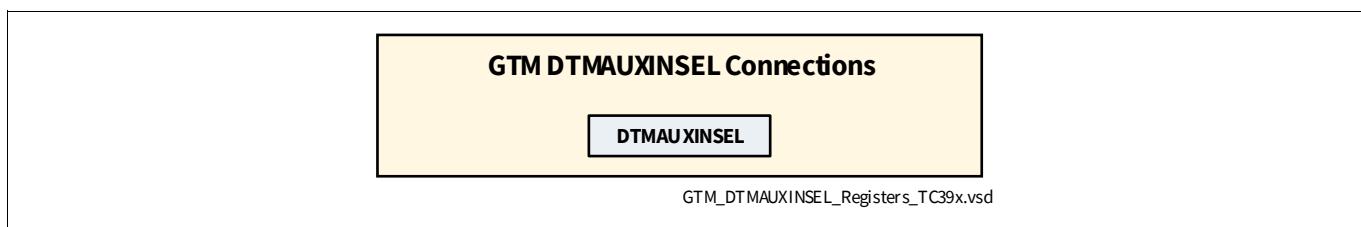


Figure 15 DTM\_AUXIN Connections Registers Overview

## DTM\_AUX Input Selection Register

## GTM\_DTMAUXINSEL

## DTM\_AUX Input Selection Register

(09FFD8<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							TSEL4	TSEL3	TSEL2	TSEL1	TSEL0				
							r	rw	rw	rw	rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ASEL6	ASEL5	ASEL4	ASEL3	ASEL2	ASEL1	ASEL0		
							r	rw	rw	rw	rw	rw	rw		

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>ASELx (x=0)</b>	2*x+1:2*x	rw	<b>CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 <sub>B</sub> <b>P02.0</b> , Port pad input 01 <sub>B</sub> <b>P02.8</b> , Port pad input 10 <sub>B</sub> <b>SWIB0</b> , EDSADC within-band signal 0 11 <sub>B</sub> <b>CBFLOUT0</b> , EVADC common boundary flag output 0
<b>ASELx (x=1)</b>	2*x+1:2*x	rw	<b>CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 <sub>B</sub> <b>P21.2</b> , Port pad input 01 <sub>B</sub> <b>P20.1</b> , Port pad input 10 <sub>B</sub> <b>SWIB1</b> , EDSADC within-band signal 1 11 <sub>B</sub> <b>CBFLOUT1</b> , EVADC common boundary flag output 1
<b>ASELx (x=2)</b>	2*x+1:2*x	rw	<b>CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 <sub>B</sub> <b>P14.5</b> , Port pad input 01 <sub>B</sub> <b>P11.0</b> , Port pad input 10 <sub>B</sub> <b>SWIB2</b> , EDSADC within-band signal 2 11 <sub>B</sub> <b>CBFLOUT2</b> , EVADC common boundary flag output 2
<b>ASELx (x=3)</b>	2*x+1:2*x	rw	<b>CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 <sub>B</sub> <b>P22.4</b> , Port pad input 01 <sub>B</sub> <b>P22.9</b> , Port pad input 10 <sub>B</sub> <b>SWIB3</b> , EDSADC within-band signal 3 11 <sub>B</sub> <b>CBFLOUT3</b> , EVADC common boundary flag output 3
<b>ASELx (x=4)</b>	2*x+1:2*x	rw	<b>CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 <sub>B</sub> <b>P12.0</b> , Port pad input 01 <sub>B</sub> <b>P21.1</b> , Port pad input 10 <sub>B</sub> <b>SWIB4</b> , EDSADC within-band signal 4 11 <sub>B</sub> <b>FC4BFLOUT</b> , EVADC boundary flag output of FC channel 4
<b>ASELx (x=5)</b>	2*x+1:2*x	rw	<b>CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 <sub>B</sub> <b>P00.4</b> , Port pad input (FC4BFLOUT) 01 <sub>B</sub> <b>P01.11</b> , Port pad input (BGA516 only) (FC7BFLOUT) 10 <sub>B</sub> <b>P10.0</b> , Port pad input (FC6BFLOUT) 11 <sub>B</sub> <b>FC5BFLOUT</b> , EVADC boundary flag output of FC channel 5

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>ASELx (x=6)</b>	$2^x+1:2^x$	rw	<b>CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 <sub>B</sub> <b>P00.6</b> , Port pad input (FC5BFLOUT) 01 <sub>B</sub> <b>P01.10</b> , Port pad input (BGA516 only) (FC6BFLOUT) 10 <sub>B</sub> <b>P01.11</b> , Port pad input (BGA516 only) (FC7BFLOUT) 11 <sub>B</sub> <b>FC6BFLOUT</b> , EVADC boundary flag output of FC channel 6
<b>TSELx (x=0)</b>	$2^x+17:2^x+16$	rw	<b>CDTMx_DTM0_AUX Input Selection (TOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM0_AUX input. 00 <sub>B</sub> <b>P14.4</b> , Port pad input 01 <sub>B</sub> <b>P10.1</b> , Port pad input (FC1BFLOUT) 10 <sub>B</sub> <b>P00.7</b> , Port pad input (FC2BFLOUT) 11 <sub>B</sub> <b>CBFLOUT0</b> , EVADC common boundary flag output 0
<b>TSELx (x=1)</b>	$2^x+17:2^x+16$	rw	<b>CDTMx_DTM0_AUX Input Selection (TOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM0_AUX input. 00 <sub>B</sub> <b>P34.0</b> , Reserved, do not use. (TC33x only) 01 <sub>B</sub> <b>P00.5</b> , Port pad input (FC0BFLOUT) 10 <sub>B</sub> <b>P33.0</b> , Port pad input (not QFP144) (FC2BFLOUT) 11 <sub>B</sub> <b>CBFLOUT1</b> , EVADC common boundary flag output 1
<b>TSELx (x=2)</b>	$2^x+17:2^x+16$	rw	<b>CDTMx_DTM0_AUX Input Selection (TOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM0_AUX input. 00 <sub>B</sub> <b>P33.4</b> , Port pad input (FC0BFLOUT) 01 <sub>B</sub> <b>P33.6</b> , Port pad input (FC1BFLOUT) 10 <sub>B</sub> <b>P10.2</b> , Port pad input (FC3BFLOUT) 11 <sub>B</sub> <b>CBFLOUT2</b> , EVADC common boundary flag output 2
<b>TSELx (x=3)</b>	$2^x+17:2^x+16$	rw	<b>CDTMx_DTM0_AUX Input Selection (TOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM0_AUX input. 00 <sub>B</sub> <b>P00.4</b> , Port pad input (FC4BFLOUT) 01 <sub>B</sub> <b>P00.6</b> , Port pad input (FC5BFLOUT) 10 <sub>B</sub> <b>P01.10</b> , Port pad input (FC6BFLOUT) 11 <sub>B</sub> <b>CBFLOUT3</b> , EVADC common boundary flag output 3
<b>TSELx (x=4)</b>	$2^x+17:2^x+16$	rw	<b>CDTMx_DTM0_AUX Input Selection (TOMx_CH0...3)</b> This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM0_AUX input. 00 <sub>B</sub> <b>P01.10</b> , Port pad input (BGA516 only) (FC6BFLOUT) 01 <sub>B</sub> <b>P01.11</b> , Port pad input (BGA516 only) (FC7BFLOUT) 10 <sub>B</sub> <b>P00.5</b> , Port pad input (BGA516 only) (FC0BFLOUT) 11 <sub>B</sub> <b>FC4BFLOUT</b> , EVADC boundary flag output of FC channel 4
<b>0</b>	15:14, 31:26	r	<b>Reserved</b> Read as 0, shall be written with 0.

## Generic Timer Module (GTM)

## 26.3.5 GTM to MSC (Micro Second Channel) Connections

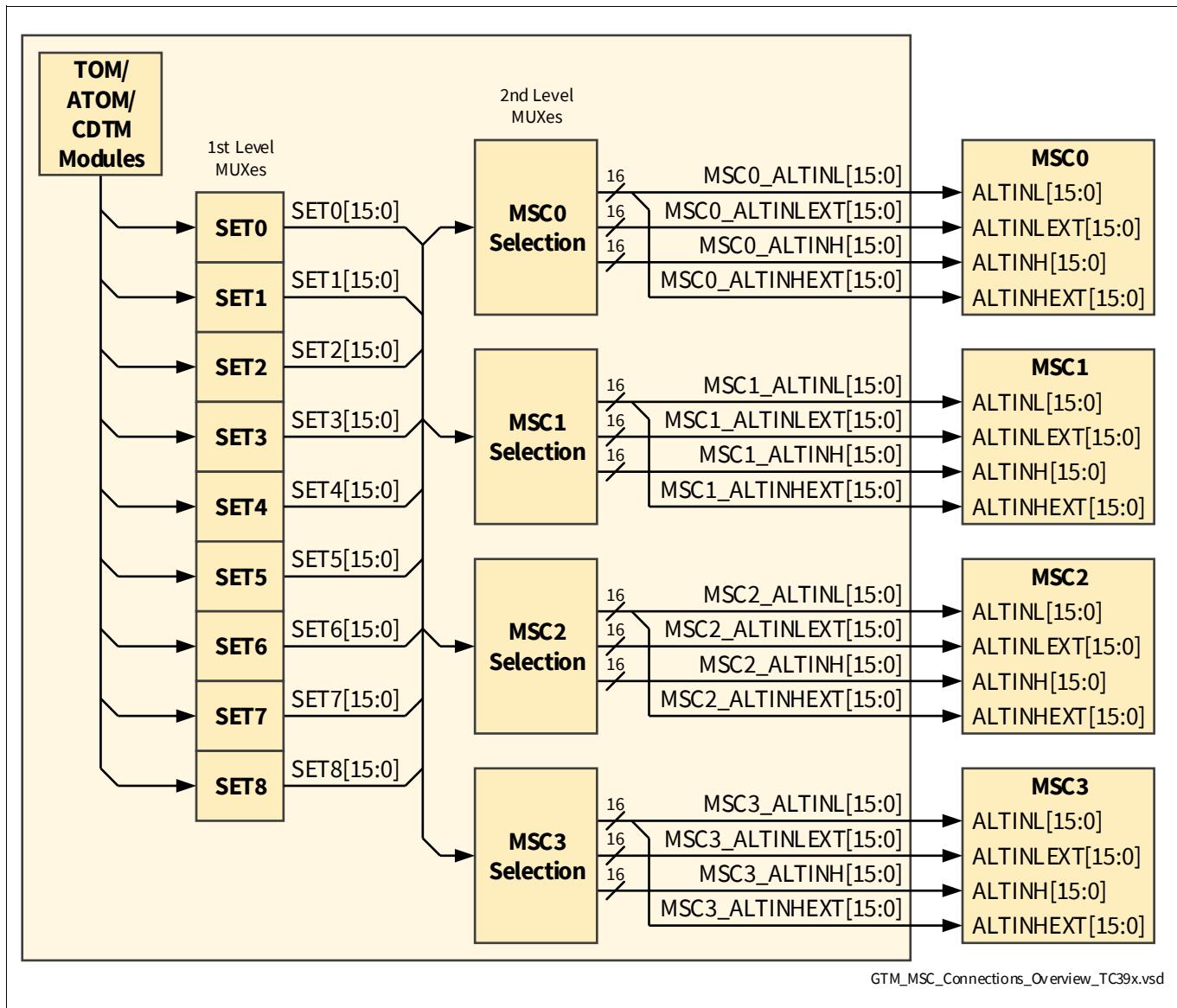


Figure 16 GTM to MSC Connections Overview

## Generic Timer Module (GTM)

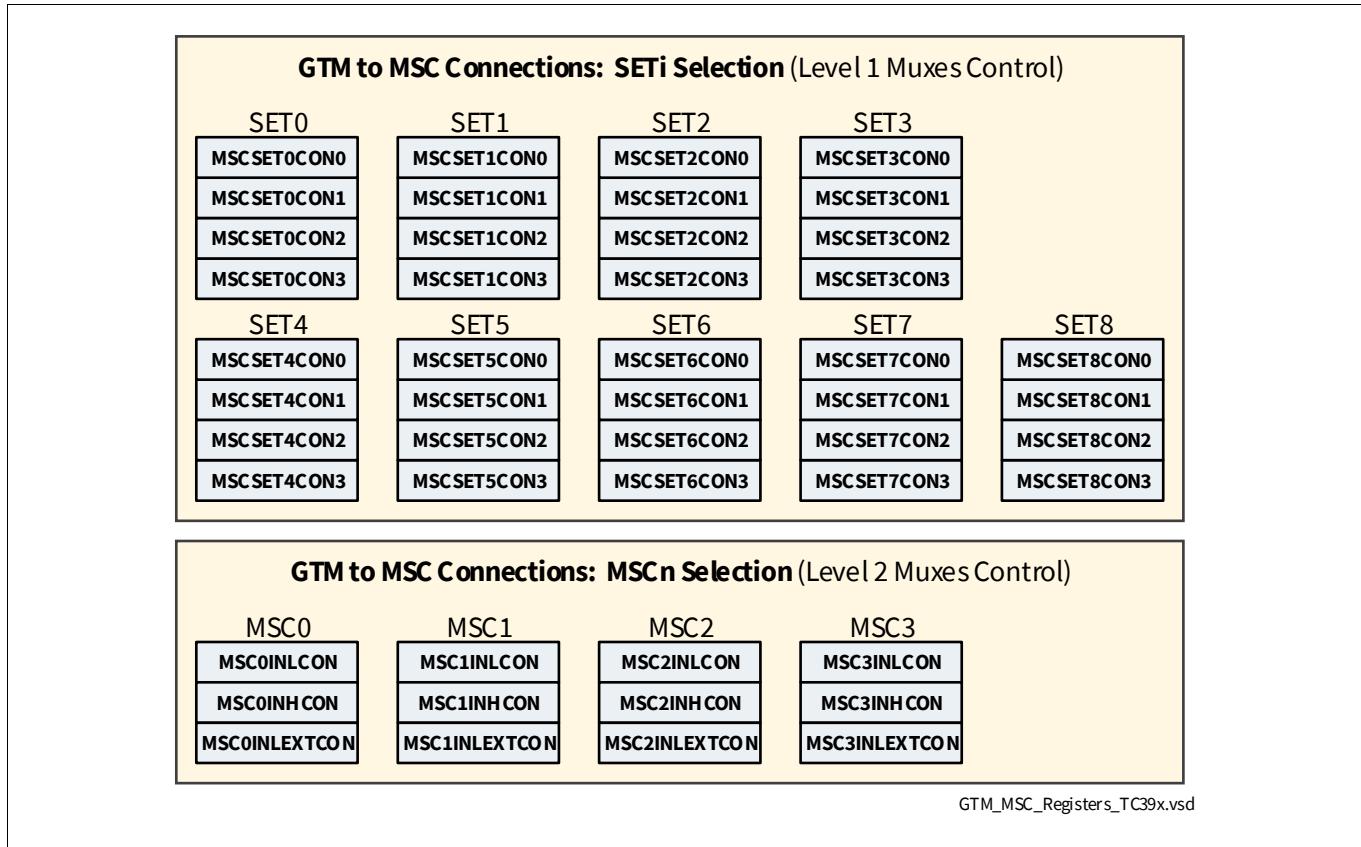
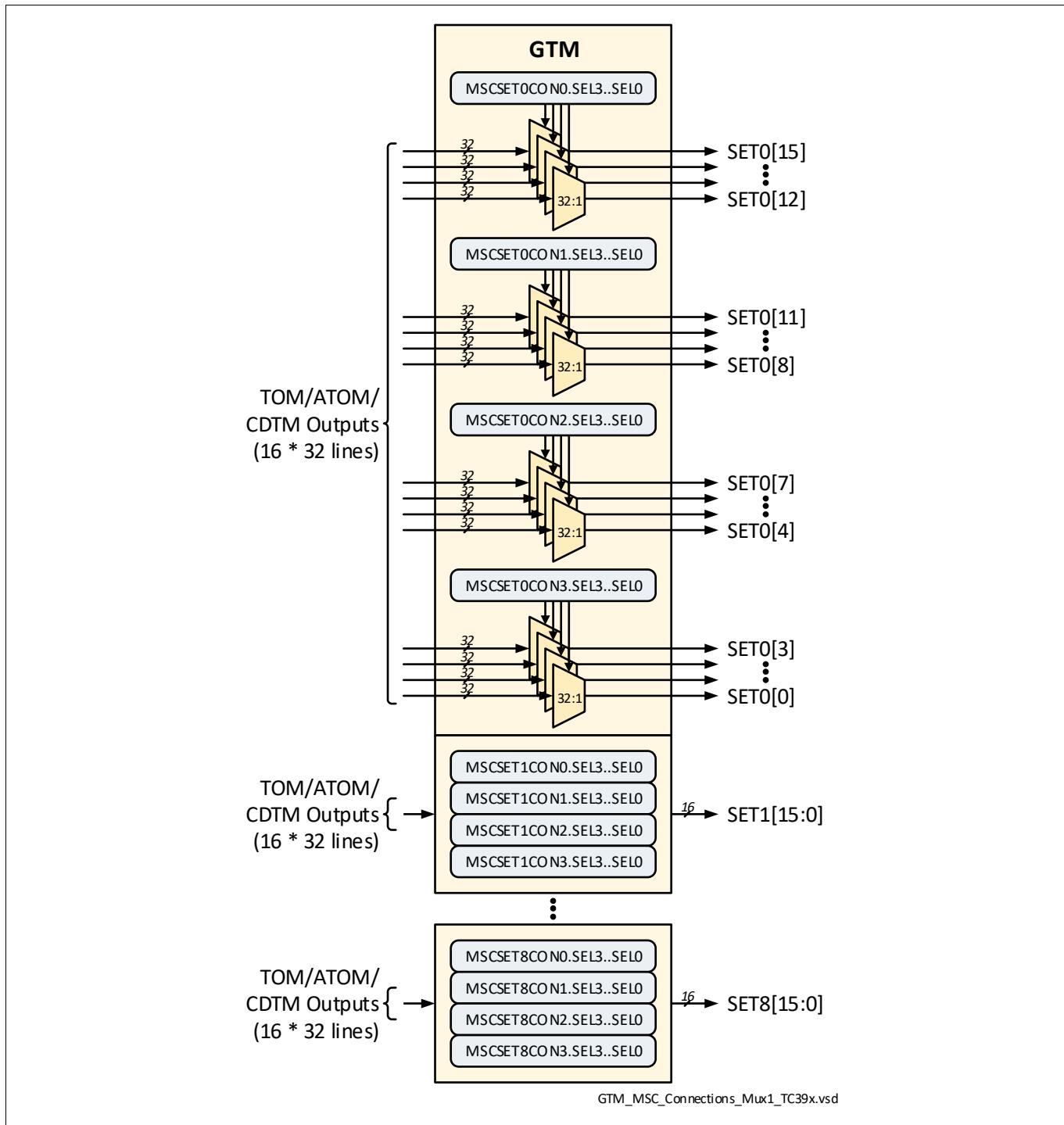


Figure 17 GTM to MSC Connections Registers Overview

**Generic Timer Module (GTM)**

**Figure 18 GTM to MSC Connections, 1st Level Muxes Overview**

## Generic Timer Module (GTM)

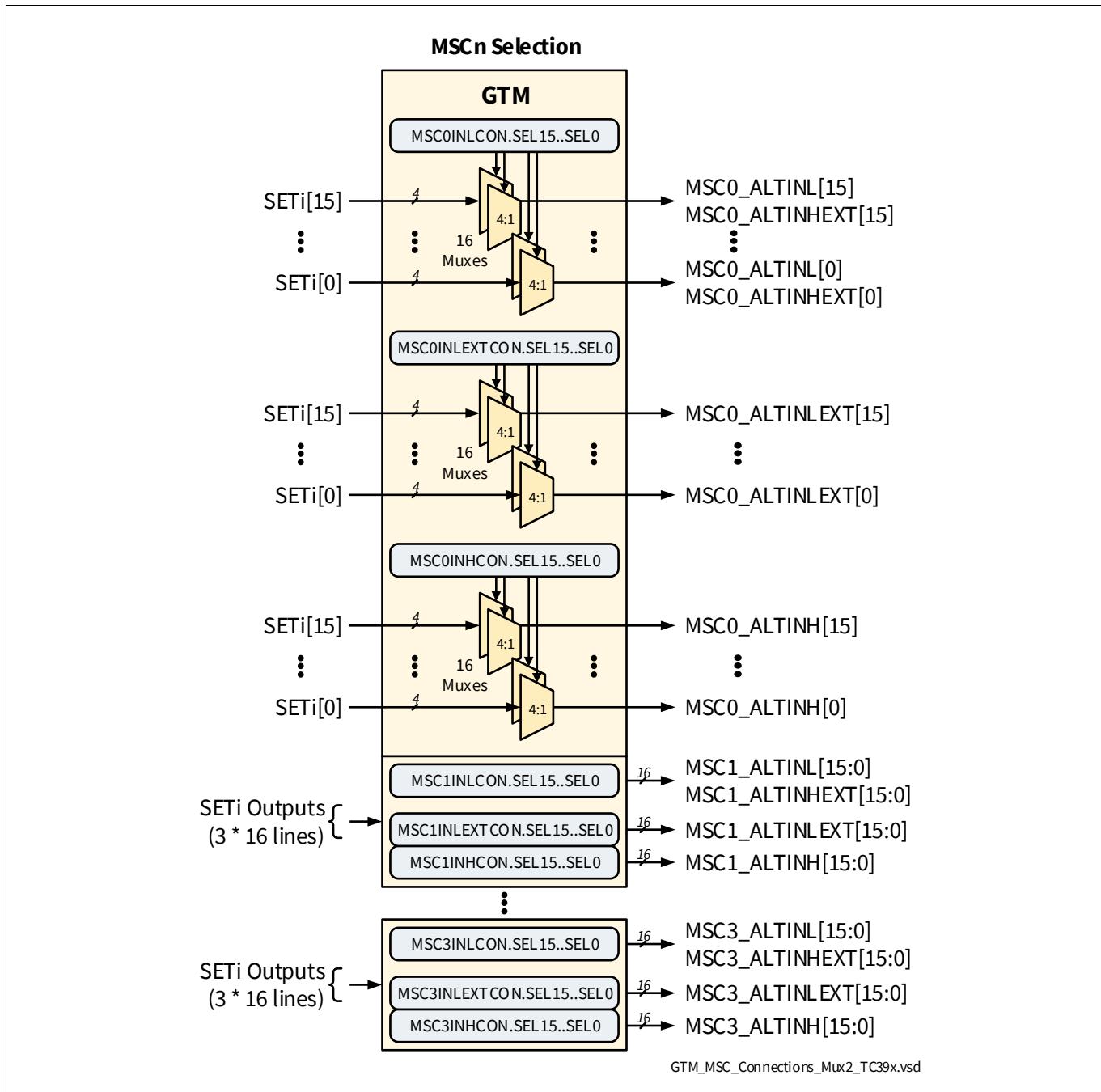


Figure 19 GTM to MSC Connections, 2nd Level Muxes Overview

Table 334 GTM to MSC Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
MSCSET0CON0	MSC Set 0 Control 0 Register (i=0;j=0)	SEL0..SEL3	<a href="#">Page 278</a>
MSCSET0CON1	MSC Set 0 Control 1 Register (i=0;j=1)	SEL4..SEL7	<a href="#">Page 280</a>
MSCSET0CON2	MSC Set 0 Control 2 Register (i=0;j=2)	SEL8..SEL11	<a href="#">Page 281</a>
MSCSET0CON3	MSC Set 0 Control 3 Register (i=0;j=3)	SEL12..SEL15	<a href="#">Page 283</a>
MSCSET1CON0	MSC Set 1 Control 0 Register (i=1;j=0)	SEL0..SEL3	<a href="#">Page 284</a>
MSCSET1CON1	MSC Set 1 Control 1 Register (i=1;j=1)	SEL4..SEL7	<a href="#">Page 286</a>

**Generic Timer Module (GTM)****Table 334 GTM to MSC Connections Registers Overview (cont'd)**

<b>Register</b>	<b>Long Name</b>	<b>Selection Bitfields</b>	<b>Page</b>
MSCSET1CON2	MSC Set 1 Control 2 Register (i=1;j=2)	SEL8..SEL11	<a href="#">Page 287</a>
MSCSET1CON3	MSC Set 1 Control 3 Register (i=1;j=3)	SEL12..SEL15	<a href="#">Page 289</a>
MSCSET2CON0	MSC Set 2 Control 0 Register (i=2;j=0)	SEL0..SEL3	<a href="#">Page 290</a>
MSCSET2CON1	MSC Set 2 Control 1 Register (i=2;j=1)	SEL4..SEL7	<a href="#">Page 292</a>
MSCSET2CON2	MSC Set 2 Control 2 Register (i=2;j=2)	SEL8..SEL11	<a href="#">Page 293</a>
MSCSET2CON3	MSC Set 2 Control 3 Register (i=2;j=3)	SEL12..SEL15	<a href="#">Page 295</a>
MSCSET3CON0	MSC Set 3 Control 0 Register (i=3;j=0)	SEL0..SEL3	<a href="#">Page 296</a>
MSCSET3CON1	MSC Set 3 Control 1 Register (i=3;j=1)	SEL4..SEL7	<a href="#">Page 298</a>
MSCSET3CON2	MSC Set 3 Control 2 Register (i=3;j=2)	SEL8..SEL11	<a href="#">Page 299</a>
MSCSET3CON3	MSC Set 3 Control 3 Register (i=3;j=3)	SEL12..SEL15	<a href="#">Page 301</a>
MSCSET4CON0	MSC Set 4 Control 0 Register (i=4;j=0)	SEL0..SEL3	<a href="#">Page 302</a>
MSCSET4CON1	MSC Set 4 Control 1 Register (i=4;j=1)	SEL4..SEL7	<a href="#">Page 304</a>
MSCSET4CON2	MSC Set 4 Control 2 Register (i=4;j=2)	SEL8..SEL11	<a href="#">Page 305</a>
MSCSET4CON3	MSC Set 4 Control 3 Register (i=4;j=3)	SEL12..SEL15	<a href="#">Page 307</a>
MSCSET5CON0	MSC Set 5 Control 0 Register (i=5;j=0)	SEL0..SEL3	<a href="#">Page 308</a>
MSCSET5CON1	MSC Set 5 Control 1 Register (i=5;j=1)	SEL4..SEL7	<a href="#">Page 310</a>
MSCSET5CON2	MSC Set 5 Control 2 Register (i=5;j=2)	SEL8..SEL11	<a href="#">Page 311</a>
MSCSET5CON3	MSC Set 5 Control 3 Register (i=5;j=3)	SEL12..SEL15	<a href="#">Page 313</a>
MSCSET6CON0	MSC Set 6 Control 0 Register (i=6;j=0)	SEL0..SEL3	<a href="#">Page 314</a>
MSCSET6CON1	MSC Set 6 Control 1 Register (i=6;j=1)	SEL4..SEL7	<a href="#">Page 316</a>
MSCSET6CON2	MSC Set 6 Control 2 Register (i=6;j=2)	SEL8..SEL11	<a href="#">Page 318</a>
MSCSET6CON3	MSC Set 6 Control 3 Register (i=6;j=3)	SEL12..SEL15	<a href="#">Page 320</a>
MSCSET7CON0	MSC Set 7 Control 0 Register (i=7;j=0)	SEL0..SEL3	<a href="#">Page 322</a>
MSCSET7CON1	MSC Set 7 Control 1 Register (i=7;j=1)	SEL4..SEL7	<a href="#">Page 323</a>
MSCSET7CON2	MSC Set 7 Control 2 Register (i=7;j=2)	SEL8..SEL11	<a href="#">Page 325</a>
MSCSET7CON3	MSC Set 7 Control 3 Register (i=7;j=3)	SEL12..SEL15	<a href="#">Page 326</a>
MSCSET8CON0	MSC Set 8 Control 0 Register (i=8;j=0)	SEL0..SEL3	<a href="#">Page 328</a>
MSCSET8CON1	MSC Set 8 Control 1 Register (i=8;j=1)	SEL4..SEL7	<a href="#">Page 329</a>
MSCSET8CON2	MSC Set 8 Control 2 Register (i=8;j=2)	SEL8..SEL11	<a href="#">Page 331</a>
MSCSET8CON3	MSC Set 8 Control 3 Register (i=8;j=3)	SEL12..SEL15	<a href="#">Page 332</a>
MSC0INLCON	MSC0 Input Low Control Register	SEL0..SEL15	<a href="#">Page 334</a>
MSC0INHCON	MSC0 Input High Control Register	SEL0..SEL15	<a href="#">Page 334</a>
MSC0INLEXTCON	MSC0 Input Low Extended Control Register	SEL0..SEL15	<a href="#">Page 335</a>
MSC1INLCON	MSC1 Input Low Control Register	SEL0..SEL15	<a href="#">Page 335</a>
MSC1INHCON	MSC1 Input High Control Register	SEL0..SEL15	<a href="#">Page 336</a>
MSC1INLEXTCON	MSC1 Input Low Extended Control Register	SEL0..SEL15	<a href="#">Page 336</a>
MSC2INLCON	MSC2 Input Low Control Register	SEL0..SEL15	<a href="#">Page 337</a>
MSC2INHCON	MSC2 Input High Control Register	SEL0..SEL15	<a href="#">Page 337</a>

## Generic Timer Module (GTM)

**Table 334 GTM to MSC Connections Registers Overview (cont'd)**

<b>Register</b>	<b>Long Name</b>	<b>Selection Bitfields</b>	<b>Page</b>
MSC2INLEXTCON	MSC2 Input Low Extended Control Register	SEL0..SEL15	<a href="#">Page 338</a>
MSC3INLCON	MSC3 Input Low Control Register	SEL0..SEL15	<a href="#">Page 338</a>
MSC3INHCON	MSC3 Input High Control Register	SEL0..SEL15	<a href="#">Page 339</a>
MSC3INLEXTCON	MSC3 Input Low Extended Control Register	SEL0..SEL15	<a href="#">Page 339</a>

## **MSC Set i Control j Register**

**GTM\_MSCSETiCONj (i=0;j=0)**

## **MSC Set i Control j Register**

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
					<b>SEL3</b>								<b>SEL2</b>		
	r				rw				r				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					<b>SEL1</b>								<b>SEL0</b>		
	r				rw				r				rw		

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 0[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0      01<sub>H</sub> <b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1      02<sub>H</sub> <b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2      03<sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3      04<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4      05<sub>H</sub> <b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5      06<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6      07<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7      08<sub>H</sub> <b>TOM0_8</b>, Output of TOM0, channel 8      09<sub>H</sub> <b>TOM0_9</b>, Output of TOM0, channel 9      0A<sub>H</sub> <b>TOM0_10</b>, Output of TOM0, channel 10      0B<sub>H</sub> <b>TOM0_11</b>, Output of TOM0, channel 11      0C<sub>H</sub> <b>TOM0_12</b>, Output of TOM0, channel 12      0D<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13      0E<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14      0F<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15      10<sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0      11<sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1      12<sub>H</sub> <b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2      13<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3      14<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      15<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      16<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      17<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7      18<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      19<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      1A<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      1B<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      1C<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4      1D<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5      1E<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6      1F<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=0;j=1)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					SEL7			0					SEL6		

r                            rw                            r                            rw

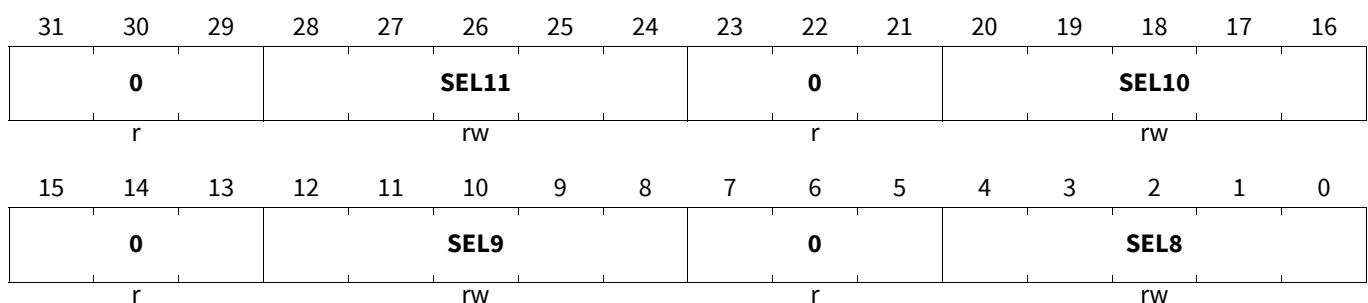
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													SEL4		

r                            rw                            r                            rw

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<b>Set 0[k] Input Selection</b> This bit field defines the GTM timer source configured as Set i signal k out. 00 <sub>H</sub> <b>CDTM0_DTM0_0, TOM0_0</b> , Dead-time output of TOM0, channel 0 01 <sub>H</sub> <b>CDTM0_DTM0_1, TOM0_1</b> , Dead-time output of TOM0, channel 1 02 <sub>H</sub> <b>CDTM0_DTM0_2, TOM0_2</b> , Dead-time output of TOM0, channel 2 03 <sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b> , Dead-time output of TOM0, channel 3 04 <sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b> , Dead-time output of TOM0, channel 4 05 <sub>H</sub> <b>CDTM0_DTM1_1, TOM0_5</b> , Dead-time output of TOM0, channel 5 06 <sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6 07 <sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7 08 <sub>H</sub> <b>TOM0_8</b> , Output of TOM0, channel 8 09 <sub>H</sub> <b>TOM0_9</b> , Output of TOM0, channel 9 0A <sub>H</sub> <b>TOM0_10</b> , Output of TOM0, channel 10 0B <sub>H</sub> <b>TOM0_11</b> , Output of TOM0, channel 11 0C <sub>H</sub> <b>TOM0_12</b> , Output of TOM0, channel 12 0D <sub>H</sub> <b>TOM0_13</b> , Output of TOM0, channel 13 0E <sub>H</sub> <b>TOM0_14</b> , Output of TOM0, channel 14 0F <sub>H</sub> <b>TOM0_15</b> , Output of TOM0, channel 15 10 <sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0 11 <sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1 12 <sub>H</sub> <b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2 13 <sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3 14 <sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4 15 <sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5 16 <sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6 17 <sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7 18 <sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0 19 <sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1 1A <sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2 1B <sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3 1C <sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4 1D <sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5 1E <sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6 1F <sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=0;j=2)****MSC Set i Control j Register****(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=8-11)</b>	8*k-60:8*k-64	rw	<p><b>Set 0[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0      01<sub>H</sub> <b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1      02<sub>H</sub> <b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2      03<sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3      04<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4      05<sub>H</sub> <b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5      06<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6      07<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7      08<sub>H</sub> <b>TOM0_8</b>, Output of TOM0, channel 8      09<sub>H</sub> <b>TOM0_9</b>, Output of TOM0, channel 9      0A<sub>H</sub> <b>TOM0_10</b>, Output of TOM0, channel 10      0B<sub>H</sub> <b>TOM0_11</b>, Output of TOM0, channel 11      0C<sub>H</sub> <b>TOM0_12</b>, Output of TOM0, channel 12      0D<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13      0E<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14      0F<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15      10<sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0      11<sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1      12<sub>H</sub> <b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2      13<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3      14<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      15<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      16<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      17<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7      18<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      19<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      1A<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      1B<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      1C<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4      1D<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5      1E<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6      1F<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## GTM\_MSCSETiCONj (i=0;j=3)

## **MSC Set i Control j Register**

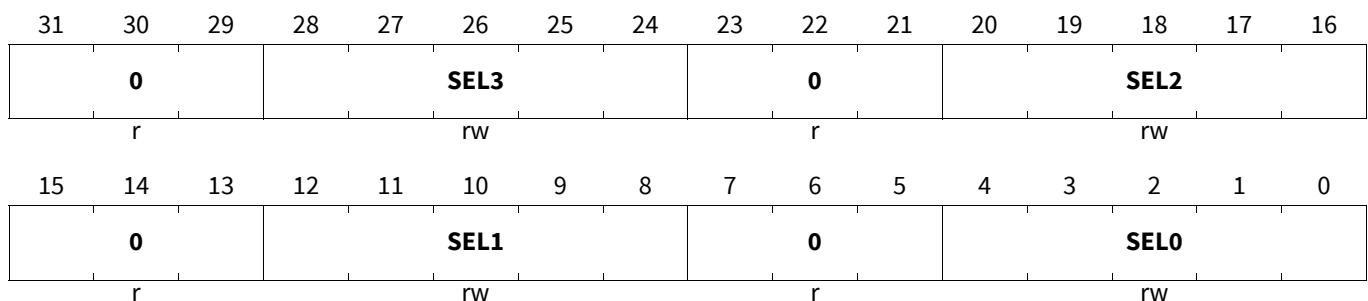
(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 0[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM0_DTM0_0, TOM0_0</b>, Dead-time output of TOM0, channel 0      01<sub>H</sub> <b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1      02<sub>H</sub> <b>CDTM0_DTM0_2, TOM0_2</b>, Dead-time output of TOM0, channel 2      03<sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3      04<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4      05<sub>H</sub> <b>CDTM0_DTM1_1, TOM0_5</b>, Dead-time output of TOM0, channel 5      06<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6      07<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7      08<sub>H</sub> <b>TOM0_8</b>, Output of TOM0, channel 8      09<sub>H</sub> <b>TOM0_9</b>, Output of TOM0, channel 9      0A<sub>H</sub> <b>TOM0_10</b>, Output of TOM0, channel 10      0B<sub>H</sub> <b>TOM0_11</b>, Output of TOM0, channel 11      0C<sub>H</sub> <b>TOM0_12</b>, Output of TOM0, channel 12      0D<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13      0E<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14      0F<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15      10<sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0      11<sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1      12<sub>H</sub> <b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2      13<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3      14<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      15<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      16<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      17<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7      18<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      19<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      1A<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      1B<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      1C<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4      1D<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5      1E<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6      1F<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=1;j=0)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 1[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0      01<sub>H</sub> <b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1      02<sub>H</sub> <b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2      03<sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3      04<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4      05<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5      06<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6      07<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7      08<sub>H</sub> <b>TOM1_8</b>, Output of TOM1, channel 8      09<sub>H</sub> <b>TOM1_9</b>, Output of TOM1, channel 9      0A<sub>H</sub> <b>TOM1_10</b>, Output of TOM1, channel 10      0B<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11      0C<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12      0D<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13      0E<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14      0F<sub>H</sub> <b>TOM1_15</b>, Output of TOM1, channel 15      10<sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0      11<sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1      12<sub>H</sub> <b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2      13<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3      14<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4      15<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5      16<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6      17<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7      18<sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0      19<sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1      1A<sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2      1B<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3      1C<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4      1D<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5      1E<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6      1F<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=1;j=1)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					SEL7			0					SEL6		

r                            rw                            r                            rw

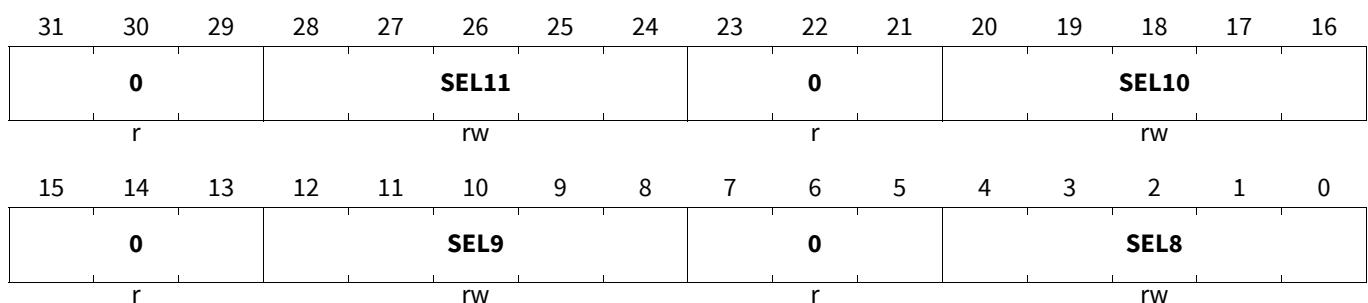
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													SEL4		

r                            rw                            r                            rw

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<b>Set 1[k] Input Selection</b> This bit field defines the GTM timer source configured as Set i signal k out. 00 <sub>H</sub> <b>CDTM1_DTM0_0, TOM1_0</b> , Dead-time output of TOM1, channel 0 01 <sub>H</sub> <b>CDTM1_DTM0_1, TOM1_1</b> , Dead-time output of TOM1, channel 1 02 <sub>H</sub> <b>CDTM1_DTM0_2, TOM1_2</b> , Dead-time output of TOM1, channel 2 03 <sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b> , Dead-time output of TOM1, channel 3 04 <sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b> , Dead-time output of TOM1, channel 4 05 <sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b> , Dead-time output of TOM1, channel 5 06 <sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6 07 <sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7 08 <sub>H</sub> <b>TOM1_8</b> , Output of TOM1, channel 8 09 <sub>H</sub> <b>TOM1_9</b> , Output of TOM1, channel 9 0A <sub>H</sub> <b>TOM1_10</b> , Output of TOM1, channel 10 0B <sub>H</sub> <b>TOM1_11</b> , Output of TOM1, channel 11 0C <sub>H</sub> <b>TOM1_12</b> , Output of TOM1, channel 12 0D <sub>H</sub> <b>TOM1_13</b> , Output of TOM1, channel 13 0E <sub>H</sub> <b>TOM1_14</b> , Output of TOM1, channel 14 0F <sub>H</sub> <b>TOM1_15</b> , Output of TOM1, channel 15 10 <sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0 11 <sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1 12 <sub>H</sub> <b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2 13 <sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3 14 <sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4 15 <sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5 16 <sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6 17 <sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7 18 <sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0 19 <sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1 1A <sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2 1B <sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3 1C <sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4 1D <sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5 1E <sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6 1F <sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=1;j=2)****MSC Set i Control j Register****(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=8-11)</b>	8*k-60:8*k-64	rw	<p><b>Set 1[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0      01<sub>H</sub> <b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1      02<sub>H</sub> <b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2      03<sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3      04<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4      05<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5      06<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6      07<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7      08<sub>H</sub> <b>TOM1_8</b>, Output of TOM1, channel 8      09<sub>H</sub> <b>TOM1_9</b>, Output of TOM1, channel 9      0A<sub>H</sub> <b>TOM1_10</b>, Output of TOM1, channel 10      0B<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11      0C<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12      0D<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13      0E<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14      0F<sub>H</sub> <b>TOM1_15</b>, Output of TOM1, channel 15      10<sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0      11<sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1      12<sub>H</sub> <b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2      13<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3      14<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4      15<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5      16<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6      17<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7      18<sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0      19<sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1      1A<sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2      1B<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3      1C<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4      1D<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5      1E<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6      1F<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=1;j=3)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0															

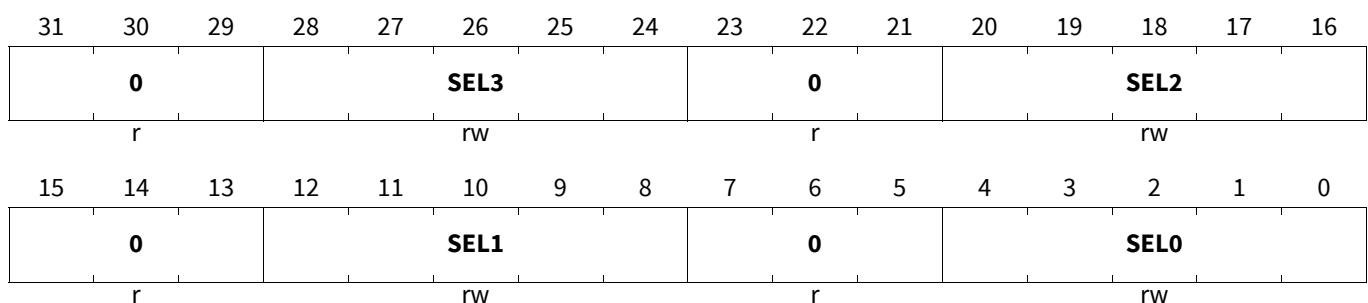
  

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 1[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM1_DTM0_0, TOM1_0</b>, Dead-time output of TOM1, channel 0  01<sub>H</sub> <b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1  02<sub>H</sub> <b>CDTM1_DTM0_2, TOM1_2</b>, Dead-time output of TOM1, channel 2  03<sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3  04<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4  05<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5  06<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6  07<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7  08<sub>H</sub> <b>TOM1_8</b>, Output of TOM1, channel 8  09<sub>H</sub> <b>TOM1_9</b>, Output of TOM1, channel 9  0A<sub>H</sub> <b>TOM1_10</b>, Output of TOM1, channel 10  0B<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11  0C<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12  0D<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13  0E<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14  0F<sub>H</sub> <b>TOM1_15</b>, Output of TOM1, channel 15  10<sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0  11<sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1  12<sub>H</sub> <b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2  13<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3  14<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4  15<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5  16<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6  17<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7  18<sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0  19<sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1  1A<sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2  1B<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3  1C<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4  1D<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5  1E<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6  1F<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=2;j=0)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 2[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0      01<sub>H</sub> <b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1      02<sub>H</sub> <b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2      03<sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3      04<sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4      05<sub>H</sub> <b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5      06<sub>H</sub> <b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6      07<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7      08<sub>H</sub> <b>TOM2_8</b>, Output of TOM2, channel 8      09<sub>H</sub> <b>TOM2_9</b>, Output of TOM2, channel 9      0A<sub>H</sub> <b>TOM2_10</b>, Output of TOM2, channel 10      0B<sub>H</sub> <b>TOM2_11</b>, Output of TOM2, channel 11      0C<sub>H</sub> <b>TOM2_12</b>, Output of TOM2, channel 12      0D<sub>H</sub> <b>TOM2_13</b>, Output of TOM2, channel 13      0E<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14      0F<sub>H</sub> <b>TOM2_15</b>, Output of TOM2, channel 15      10<sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0      11<sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1      12<sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2      13<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3      14<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4      15<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5      16<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6      17<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7      18<sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0      19<sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1      1A<sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2      1B<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3      1C<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4      1D<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5      1E<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6      1F<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=2;j=1)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					SEL7			0					SEL6		

r                            rw                            r                            rw

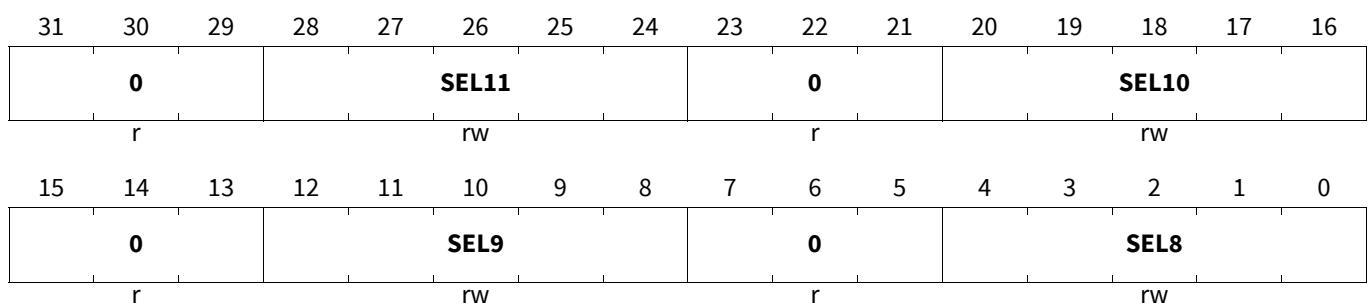
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													SEL4		

r                            rw                            r                            rw

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<b>Set 2[k] Input Selection</b> This bit field defines the GTM timer source configured as Set i signal k out. 00 <sub>H</sub> <b>CDTM2_DTM0_0, TOM2_0</b> , Dead-time output of TOM2, channel 0 01 <sub>H</sub> <b>CDTM2_DTM0_1, TOM2_1</b> , Dead-time output of TOM2, channel 1 02 <sub>H</sub> <b>CDTM2_DTM0_2, TOM2_2</b> , Dead-time output of TOM2, channel 2 03 <sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b> , Dead-time output of TOM2, channel 3 04 <sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b> , Dead-time output of TOM2, channel 4 05 <sub>H</sub> <b>CDTM2_DTM1_1, TOM2_5</b> , Dead-time output of TOM2, channel 5 06 <sub>H</sub> <b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6 07 <sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7 08 <sub>H</sub> <b>TOM2_8</b> , Output of TOM2, channel 8 09 <sub>H</sub> <b>TOM2_9</b> , Output of TOM2, channel 9 0A <sub>H</sub> <b>TOM2_10</b> , Output of TOM2, channel 10 0B <sub>H</sub> <b>TOM2_11</b> , Output of TOM2, channel 11 0C <sub>H</sub> <b>TOM2_12</b> , Output of TOM2, channel 12 0D <sub>H</sub> <b>TOM2_13</b> , Output of TOM2, channel 13 0E <sub>H</sub> <b>TOM2_14</b> , Output of TOM2, channel 14 0F <sub>H</sub> <b>TOM2_15</b> , Output of TOM2, channel 15 10 <sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b> , Dead-time output of ATOM4, channel 0 11 <sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b> , Dead-time output of ATOM4, channel 1 12 <sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b> , Dead-time output of ATOM4, channel 2 13 <sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b> , Dead-time output of ATOM4, channel 3 14 <sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4 15 <sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5 16 <sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6 17 <sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7 18 <sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b> , Dead-time output of ATOM3, channel 0 19 <sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b> , Dead-time output of ATOM3, channel 1 1A <sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b> , Dead-time output of ATOM3, channel 2 1B <sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b> , Dead-time output of ATOM3, channel 3 1C <sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4 1D <sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5 1E <sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6 1F <sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=2;j=2)****MSC Set i Control j Register****(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=8-11)</b>	8*k-60:8*k-64	rw	<p><b>Set 2[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0      01<sub>H</sub> <b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1      02<sub>H</sub> <b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2      03<sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3      04<sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4      05<sub>H</sub> <b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5      06<sub>H</sub> <b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6      07<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7      08<sub>H</sub> <b>TOM2_8</b>, Output of TOM2, channel 8      09<sub>H</sub> <b>TOM2_9</b>, Output of TOM2, channel 9      0A<sub>H</sub> <b>TOM2_10</b>, Output of TOM2, channel 10      0B<sub>H</sub> <b>TOM2_11</b>, Output of TOM2, channel 11      0C<sub>H</sub> <b>TOM2_12</b>, Output of TOM2, channel 12      0D<sub>H</sub> <b>TOM2_13</b>, Output of TOM2, channel 13      0E<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14      0F<sub>H</sub> <b>TOM2_15</b>, Output of TOM2, channel 15      10<sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0      11<sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1      12<sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2      13<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3      14<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4      15<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5      16<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6      17<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7      18<sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0      19<sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1      1A<sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2      1B<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3      1C<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4      1D<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5      1E<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6      1F<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## GTM\_MSCSETiCONj (i=2;j=3)

## **MSC Set i Control j Register**

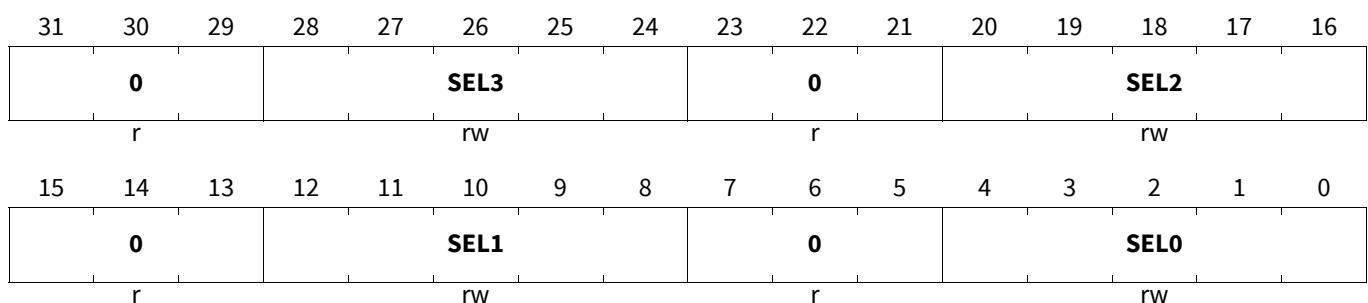
(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 2[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <ul style="list-style-type: none"> <li>00<sub>H</sub> <b>CDTM2_DTM0_0, TOM2_0</b>, Dead-time output of TOM2, channel 0</li> <li>01<sub>H</sub> <b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</li> <li>02<sub>H</sub> <b>CDTM2_DTM0_2, TOM2_2</b>, Dead-time output of TOM2, channel 2</li> <li>03<sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</li> <li>04<sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</li> <li>05<sub>H</sub> <b>CDTM2_DTM1_1, TOM2_5</b>, Dead-time output of TOM2, channel 5</li> <li>06<sub>H</sub> <b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</li> <li>07<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</li> <li>08<sub>H</sub> <b>TOM2_8</b>, Output of TOM2, channel 8</li> <li>09<sub>H</sub> <b>TOM2_9</b>, Output of TOM2, channel 9</li> <li>0A<sub>H</sub> <b>TOM2_10</b>, Output of TOM2, channel 10</li> <li>0B<sub>H</sub> <b>TOM2_11</b>, Output of TOM2, channel 11</li> <li>0C<sub>H</sub> <b>TOM2_12</b>, Output of TOM2, channel 12</li> <li>0D<sub>H</sub> <b>TOM2_13</b>, Output of TOM2, channel 13</li> <li>0E<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14</li> <li>0F<sub>H</sub> <b>TOM2_15</b>, Output of TOM2, channel 15</li> <li>10<sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</li> <li>11<sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</li> <li>12<sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</li> <li>13<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</li> <li>14<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</li> <li>15<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</li> <li>16<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</li> <li>17<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</li> <li>18<sub>H</sub> <b>CDTM3_DTM4_0, ATOM3_0</b>, Dead-time output of ATOM3, channel 0</li> <li>19<sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</li> <li>1A<sub>H</sub> <b>CDTM3_DTM4_2, ATOM3_2</b>, Dead-time output of ATOM3, channel 2</li> <li>1B<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</li> <li>1C<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</li> <li>1D<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</li> <li>1E<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</li> <li>1F<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</li> </ul>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=3;j=0)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description																																																																
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 3[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <table> <tr><td>00<sub>H</sub></td><td><b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0</td></tr> <tr><td>01<sub>H</sub></td><td><b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</td></tr> <tr><td>02<sub>H</sub></td><td><b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2</td></tr> <tr><td>03<sub>H</sub></td><td><b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</td></tr> <tr><td>04<sub>H</sub></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr><td>05<sub>H</sub></td><td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td></tr> <tr><td>06<sub>H</sub></td><td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td></tr> <tr><td>07<sub>H</sub></td><td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td></tr> <tr><td>08<sub>H</sub></td><td><b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0</td></tr> <tr><td>09<sub>H</sub></td><td><b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</td></tr> <tr><td>0A<sub>H</sub></td><td><b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2</td></tr> <tr><td>0B<sub>H</sub></td><td><b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</td></tr> <tr><td>0C<sub>H</sub></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> <tr><td>0D<sub>H</sub></td><td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td></tr> <tr><td>0E<sub>H</sub></td><td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td></tr> <tr><td>0F<sub>H</sub></td><td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td></tr> <tr><td>10<sub>H</sub></td><td><b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</td></tr> <tr><td>11<sub>H</sub></td><td><b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</td></tr> <tr><td>12<sub>H</sub></td><td><b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</td></tr> <tr><td>13<sub>H</sub></td><td><b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</td></tr> <tr><td>14<sub>H</sub></td><td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td></tr> <tr><td>15<sub>H</sub></td><td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td></tr> <tr><td>16<sub>H</sub></td><td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td></tr> <tr><td>17<sub>H</sub></td><td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td></tr> <tr><td>18<sub>H</sub></td><td><b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0</td></tr> <tr><td>19<sub>H</sub></td><td><b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1</td></tr> <tr><td>1A<sub>H</sub></td><td><b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2</td></tr> <tr><td>1B<sub>H</sub></td><td><b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</td></tr> <tr><td>1C<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr><td>1D<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td>1E<sub>H</sub></td><td><b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</td></tr> <tr><td>1F<sub>H</sub></td><td><b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</td></tr> </table>	00 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0	01 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1	02 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2	03 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3	04 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	05 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	06 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	07 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	08 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0	09 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1	0A <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2	0B <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3	0C <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	0D <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	0E <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	0F <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	10 <sub>H</sub>	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0	11 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1	12 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2	13 <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3	14 <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	15 <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	16 <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	17 <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	18 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0	19 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1	1A <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2	1B <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3	1C <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	1D <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	1E <sub>H</sub>	<b>CDTM5_DTM5_2, ATOM5_6</b> , Dead-time output of ATOM5, channel 6	1F <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7
00 <sub>H</sub>	<b>CDTM0_DTM4_0, ATOM0_0</b> , Dead-time output of ATOM0, channel 0																																																																		
01 <sub>H</sub>	<b>CDTM0_DTM4_1, ATOM0_1</b> , Dead-time output of ATOM0, channel 1																																																																		
02 <sub>H</sub>	<b>CDTM0_DTM4_2, ATOM0_2</b> , Dead-time output of ATOM0, channel 2																																																																		
03 <sub>H</sub>	<b>CDTM0_DTM4_3, ATOM0_3</b> , Dead-time output of ATOM0, channel 3																																																																		
04 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																																																																		
05 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																																																																		
06 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																																																																		
07 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																																																																		
08 <sub>H</sub>	<b>CDTM1_DTM4_0, ATOM1_0</b> , Dead-time output of ATOM1, channel 0																																																																		
09 <sub>H</sub>	<b>CDTM1_DTM4_1, ATOM1_1</b> , Dead-time output of ATOM1, channel 1																																																																		
0A <sub>H</sub>	<b>CDTM1_DTM4_2, ATOM1_2</b> , Dead-time output of ATOM1, channel 2																																																																		
0B <sub>H</sub>	<b>CDTM1_DTM4_3, ATOM1_3</b> , Dead-time output of ATOM1, channel 3																																																																		
0C <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																																																																		
0D <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																																																																		
0E <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6																																																																		
0F <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																																																																		
10 <sub>H</sub>	<b>CDTM2_DTM4_0, ATOM2_0</b> , Dead-time output of ATOM2, channel 0																																																																		
11 <sub>H</sub>	<b>CDTM2_DTM4_1, ATOM2_1</b> , Dead-time output of ATOM2, channel 1																																																																		
12 <sub>H</sub>	<b>CDTM2_DTM4_2, ATOM2_2</b> , Dead-time output of ATOM2, channel 2																																																																		
13 <sub>H</sub>	<b>CDTM2_DTM4_3, ATOM2_3</b> , Dead-time output of ATOM2, channel 3																																																																		
14 <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																																																																		
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18 <sub>H</sub>	<b>CDTM5_DTM4_0, ATOM5_0</b> , Dead-time output of ATOM5, channel 0																																																																		
19 <sub>H</sub>	<b>CDTM5_DTM4_1, ATOM5_1</b> , Dead-time output of ATOM5, channel 1																																																																		
1A <sub>H</sub>	<b>CDTM5_DTM4_2, ATOM5_2</b> , Dead-time output of ATOM5, channel 2																																																																		
1B <sub>H</sub>	<b>CDTM5_DTM4_3, ATOM5_3</b> , Dead-time output of ATOM5, channel 3																																																																		
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1F <sub>H</sub>	<b>CDTM5_DTM5_3, ATOM5_7</b> , Dead-time output of ATOM5, channel 7																																																																		
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>																																																																

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=3;j=1)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0															

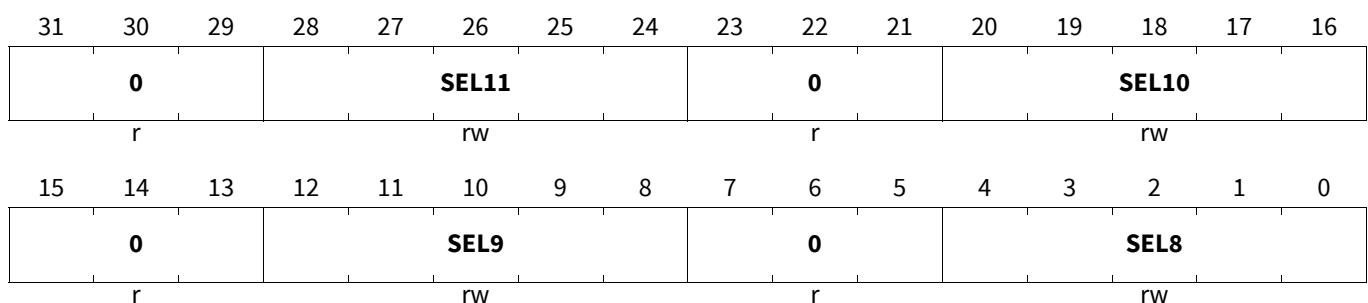
  

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<p><b>Set 3[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0      01<sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1      02<sub>H</sub> <b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2      03<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3      04<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      05<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      06<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      07<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7      08<sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0      09<sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1      0A<sub>H</sub> <b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2      0B<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3      0C<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4      0D<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5      0E<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6      0F<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7      10<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      11<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      12<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      13<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      14<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4      15<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5      16<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6      17<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7      18<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      19<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      1A<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      1B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      1C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      1D<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      1E<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      1F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p>

**Generic Timer Module (GTM)**

Field	Bits	Type	Description
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=3;j=2)**
**MSC Set i Control j Register**
**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**
**Application Reset Value: 0000 0000<sub>H</sub>**


## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=8-11)</b>	8*k-60:8*k-64	rw	<p><b>Set 3[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0      01<sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1      02<sub>H</sub> <b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2      03<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3      04<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      05<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      06<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      07<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7      08<sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0      09<sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1      0A<sub>H</sub> <b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2      0B<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3      0C<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4      0D<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5      0E<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6      0F<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7      10<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      11<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      12<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      13<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      14<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4      15<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5      16<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6      17<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7      18<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      19<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      1A<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      1B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      1C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      1D<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      1E<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      1F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=3;j=3)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0															

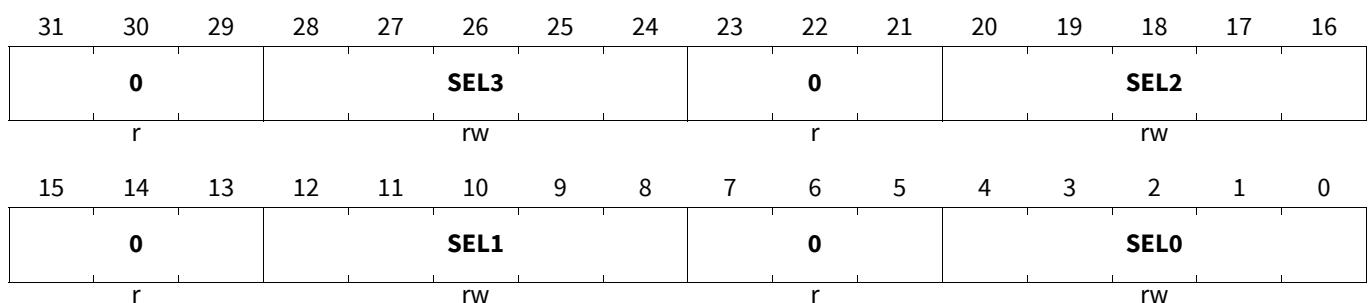
  

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 3[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM0_DTM4_0, ATOM0_0</b>, Dead-time output of ATOM0, channel 0      01<sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1      02<sub>H</sub> <b>CDTM0_DTM4_2, ATOM0_2</b>, Dead-time output of ATOM0, channel 2      03<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3      04<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      05<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      06<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      07<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7      08<sub>H</sub> <b>CDTM1_DTM4_0, ATOM1_0</b>, Dead-time output of ATOM1, channel 0      09<sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1      0A<sub>H</sub> <b>CDTM1_DTM4_2, ATOM1_2</b>, Dead-time output of ATOM1, channel 2      0B<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3      0C<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4      0D<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5      0E<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6      0F<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7      10<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      11<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      12<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      13<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      14<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4      15<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5      16<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6      17<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7      18<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      19<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      1A<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      1B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      1C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      1D<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      1E<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      1F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=4;j=0)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 4[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0      01<sub>H</sub> <b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1      02<sub>H</sub> <b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2      03<sub>H</sub> <b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3      04<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4      05<sub>H</sub> <b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5      06<sub>H</sub> <b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6      07<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7      08<sub>H</sub> <b>TOM3_8</b>, Output of TOM3, channel 8      09<sub>H</sub> <b>TOM3_9</b>, Output of TOM3, channel 9      0A<sub>H</sub> <b>TOM3_10</b>, Output of TOM3, channel 10      0B<sub>H</sub> <b>TOM3_11</b>, Output of TOM3, channel 11      0C<sub>H</sub> <b>TOM3_12</b>, Output of TOM3, channel 12      0D<sub>H</sub> <b>TOM3_13</b>, Output of TOM3, channel 13      0E<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14      0F<sub>H</sub> <b>TOM3_15</b>, Output of TOM3, channel 15      10<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      11<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      12<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      13<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      14<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      15<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      16<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      17<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7      18<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0      19<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1      1A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2      1B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3      1C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4      1D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5      1E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6      1F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=4;j=1)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		0			SEL7			0			SEL6				
r					rw			r			rw				

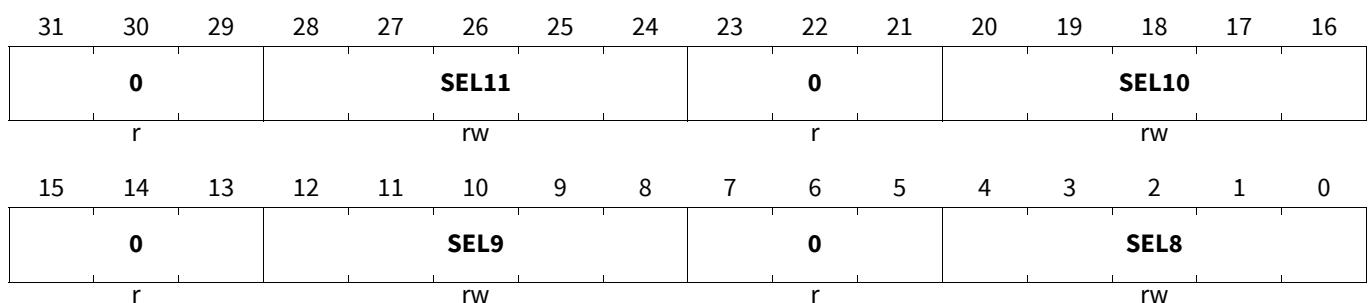
  

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		0			SEL5			0			SEL4				
r					rw			r			rw				

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<p><b>Set 4[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0      01<sub>H</sub> <b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1      02<sub>H</sub> <b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2      03<sub>H</sub> <b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3      04<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4      05<sub>H</sub> <b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5      06<sub>H</sub> <b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6      07<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7      08<sub>H</sub> <b>TOM3_8</b>, Output of TOM3, channel 8      09<sub>H</sub> <b>TOM3_9</b>, Output of TOM3, channel 9      0A<sub>H</sub> <b>TOM3_10</b>, Output of TOM3, channel 10      0B<sub>H</sub> <b>TOM3_11</b>, Output of TOM3, channel 11      0C<sub>H</sub> <b>TOM3_12</b>, Output of TOM3, channel 12      0D<sub>H</sub> <b>TOM3_13</b>, Output of TOM3, channel 13      0E<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14      0F<sub>H</sub> <b>TOM3_15</b>, Output of TOM3, channel 15      10<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      11<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      12<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      13<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      14<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      15<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      16<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      17<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7      18<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0      19<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1      1A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2      1B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3      1C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4      1D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5      1E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6      1F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=4;j=2)****MSC Set i Control j Register****(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=8-11)</b>	8*k-60:8*k-64	rw	<p><b>Set 4[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0      01<sub>H</sub> <b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1      02<sub>H</sub> <b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2      03<sub>H</sub> <b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3      04<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4      05<sub>H</sub> <b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5      06<sub>H</sub> <b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6      07<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7      08<sub>H</sub> <b>TOM3_8</b>, Output of TOM3, channel 8      09<sub>H</sub> <b>TOM3_9</b>, Output of TOM3, channel 9      0A<sub>H</sub> <b>TOM3_10</b>, Output of TOM3, channel 10      0B<sub>H</sub> <b>TOM3_11</b>, Output of TOM3, channel 11      0C<sub>H</sub> <b>TOM3_12</b>, Output of TOM3, channel 12      0D<sub>H</sub> <b>TOM3_13</b>, Output of TOM3, channel 13      0E<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14      0F<sub>H</sub> <b>TOM3_15</b>, Output of TOM3, channel 15      10<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      11<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      12<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      13<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      14<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      15<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      16<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      17<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7      18<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0      19<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1      1A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2      1B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3      1C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4      1D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5      1E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6      1F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## GTM\_MSCSETiCONj (i=4;j=3)

## **MSC Set i Control j Register**

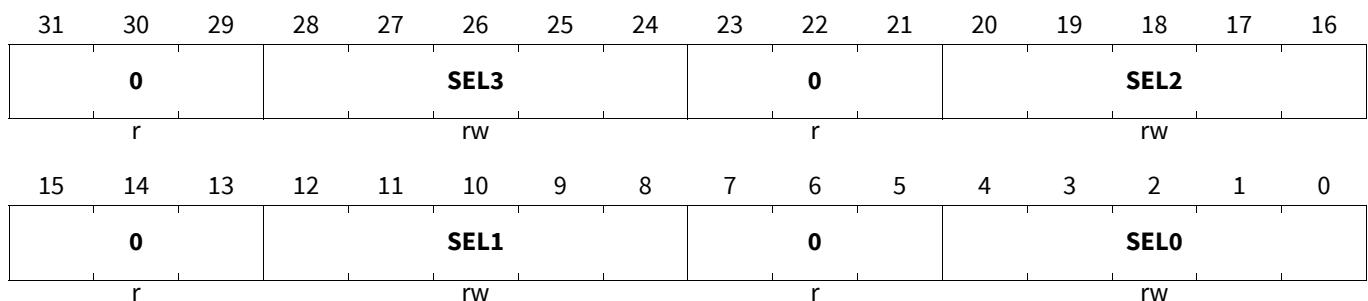
(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 4[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM3_DTM0_0, TOM3_0</b>, Dead-time output of TOM3, channel 0      01<sub>H</sub> <b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1      02<sub>H</sub> <b>CDTM3_DTM0_2, TOM3_2</b>, Dead-time output of TOM3, channel 2      03<sub>H</sub> <b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3      04<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4      05<sub>H</sub> <b>CDTM3_DTM1_1, TOM3_5</b>, Dead-time output of TOM3, channel 5      06<sub>H</sub> <b>CDTM3_DTM1_2, TOM3_6</b>, Dead-time output of TOM3, channel 6      07<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7      08<sub>H</sub> <b>TOM3_8</b>, Output of TOM3, channel 8      09<sub>H</sub> <b>TOM3_9</b>, Output of TOM3, channel 9      0A<sub>H</sub> <b>TOM3_10</b>, Output of TOM3, channel 10      0B<sub>H</sub> <b>TOM3_11</b>, Output of TOM3, channel 11      0C<sub>H</sub> <b>TOM3_12</b>, Output of TOM3, channel 12      0D<sub>H</sub> <b>TOM3_13</b>, Output of TOM3, channel 13      0E<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14      0F<sub>H</sub> <b>TOM3_15</b>, Output of TOM3, channel 15      10<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      11<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      12<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      13<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      14<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      15<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      16<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      17<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7      18<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0      19<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1      1A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2      1B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3      1C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4      1D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5      1E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6      1F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=5;j=0)****MSC Set i Control j Register****(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 5[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0      01<sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1      02<sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2      03<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3      04<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4      05<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5      06<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6      07<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7      08<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0      09<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1      0A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2      0B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3      0C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4      0D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5      0E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6      0F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7      10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0      11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1      12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2      13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3      14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4      15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5      16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6      17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7      18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0      19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1      1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2      1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3      1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4      1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5      1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6      1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=5;j=1)

MSC Set i Control j Register

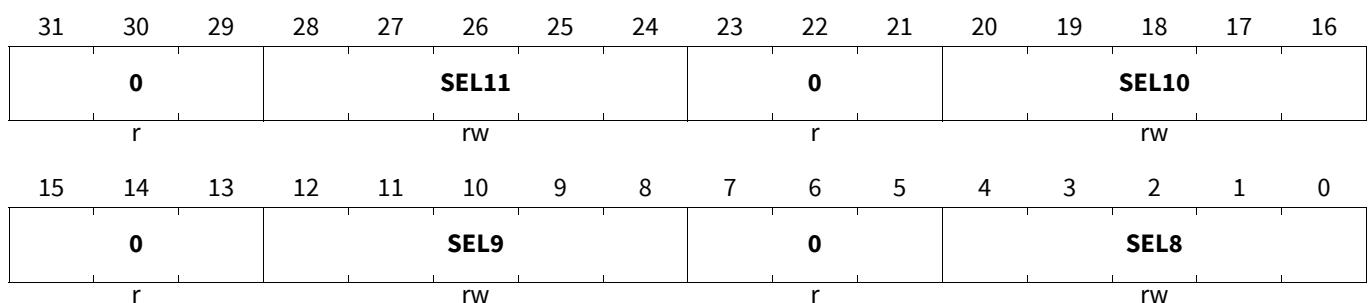
(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0				SEL7				0				SEL6		
r					rw				r				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0				SEL5				0				SEL4		
r					rw				r				rw		

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<p><b>Set 5[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <ul style="list-style-type: none"> <li>00<sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</li> <li>01<sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</li> <li>02<sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</li> <li>03<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</li> <li>04<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</li> <li>05<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</li> <li>06<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</li> <li>07<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</li> <li>08<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</li> <li>09<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</li> <li>0A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</li> <li>0B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</li> <li>0C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</li> <li>0D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</li> <li>0E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</li> <li>0F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</li> <li>10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0</li> <li>11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1</li> <li>12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2</li> <li>13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3</li> <li>14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4</li> <li>15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5</li> <li>16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6</li> <li>17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7</li> <li>18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0</li> <li>19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1</li> <li>1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2</li> <li>1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3</li> <li>1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4</li> <li>1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5</li> <li>1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6</li> <li>1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</li> </ul>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=5;j=2)****MSC Set i Control j Register****(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=8-11)</b>	8*k-60:8*k-64	rw	<p><b>Set 5[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0      01<sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1      02<sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2      03<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3      04<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4      05<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5      06<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6      07<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7      08<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0      09<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1      0A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2      0B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3      0C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4      0D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5      0E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6      0F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7      10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0      11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1      12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2      13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3      14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4      15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5      16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6      17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7      18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0      19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1      1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2      1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3      1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4      1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5      1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6      1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## GTM\_MSCSETiCONj (i=5;j=3)

## **MSC Set i Control j Register**

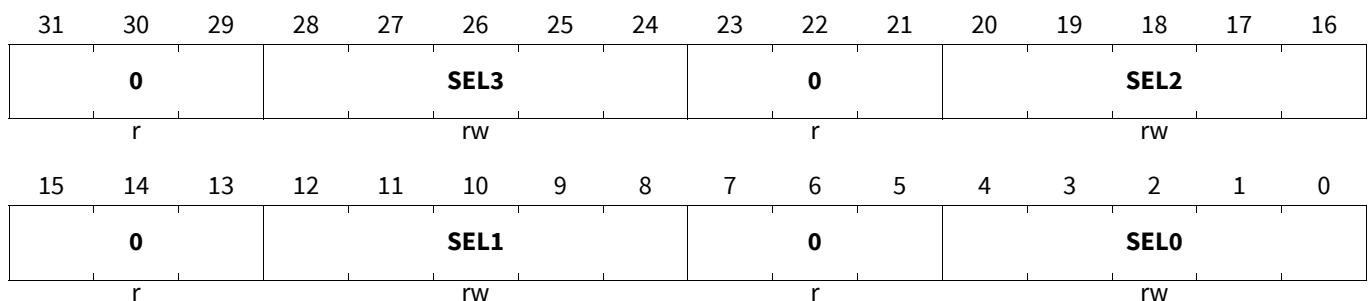
(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 5[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <ul style="list-style-type: none"> <li>00<sub>H</sub> <b>CDTM4_DTM4_0, ATOM4_0</b>, Dead-time output of ATOM4, channel 0</li> <li>01<sub>H</sub> <b>CDTM4_DTM4_1, ATOM4_1</b>, Dead-time output of ATOM4, channel 1</li> <li>02<sub>H</sub> <b>CDTM4_DTM4_2, ATOM4_2</b>, Dead-time output of ATOM4, channel 2</li> <li>03<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</li> <li>04<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</li> <li>05<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</li> <li>06<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</li> <li>07<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</li> <li>08<sub>H</sub> <b>CDTM6_DTM4_0, ATOM6_0</b>, Dead-time output of ATOM6, channel 0</li> <li>09<sub>H</sub> <b>CDTM6_DTM4_1, ATOM6_1</b>, Dead-time output of ATOM6, channel 1</li> <li>0A<sub>H</sub> <b>CDTM6_DTM4_2, ATOM6_2</b>, Dead-time output of ATOM6, channel 2</li> <li>0B<sub>H</sub> <b>CDTM6_DTM4_3, ATOM6_3</b>, Dead-time output of ATOM6, channel 3</li> <li>0C<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</li> <li>0D<sub>H</sub> <b>CDTM6_DTM5_1, ATOM6_5</b>, Dead-time output of ATOM6, channel 5</li> <li>0E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</li> <li>0F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</li> <li>10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0</li> <li>11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1</li> <li>12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2</li> <li>13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3</li> <li>14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4</li> <li>15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5</li> <li>16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6</li> <li>17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7</li> <li>18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0</li> <li>19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1</li> <li>1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2</li> <li>1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3</li> <li>1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4</li> <li>1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5</li> <li>1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6</li> <li>1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</li> </ul>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=6;j=0)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 6[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0      01<sub>H</sub> <b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1      02<sub>H</sub> <b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2      03<sub>H</sub> <b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3      04<sub>H</sub> <b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4      05<sub>H</sub> <b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5      06<sub>H</sub> <b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6      07<sub>H</sub> <b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7      08<sub>H</sub> <b>TOM4_8</b>, Output of TOM4, channel 8      09<sub>H</sub> <b>TOM4_9</b>, Output of TOM4, channel 9      0A<sub>H</sub> <b>TOM4_10</b>, Output of TOM4, channel 10      0B<sub>H</sub> <b>TOM4_11</b>, Output of TOM4, channel 11      0C<sub>H</sub> <b>TOM4_12</b>, Output of TOM4, channel 12      0D<sub>H</sub> <b>TOM4_13</b>, Output of TOM4, channel 13      0E<sub>H</sub> <b>TOM4_14</b>, Output of TOM4, channel 14      0F<sub>H</sub> <b>TOM4_15</b>, Output of TOM4, channel 15      10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0      11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1      12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2      13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3      14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4      15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5      16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6      17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7      18<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      19<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      1A<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      1B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      1C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      1D<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      1E<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      1F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=6;j=1)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0

SEL7

0

SEL6

r

rw

r

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0

SEL5

0

SEL4

r

rw

r

rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=4-7)</b>	8*k-28:8*k-32	rw	<p><b>Set 6[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0      01<sub>H</sub> <b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1      02<sub>H</sub> <b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2      03<sub>H</sub> <b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3      04<sub>H</sub> <b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4      05<sub>H</sub> <b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5      06<sub>H</sub> <b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6      07<sub>H</sub> <b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7      08<sub>H</sub> <b>TOM4_8</b>, Output of TOM4, channel 8      09<sub>H</sub> <b>TOM4_9</b>, Output of TOM4, channel 9      0A<sub>H</sub> <b>TOM4_10</b>, Output of TOM4, channel 10      0B<sub>H</sub> <b>TOM4_11</b>, Output of TOM4, channel 11      0C<sub>H</sub> <b>TOM4_12</b>, Output of TOM4, channel 12      0D<sub>H</sub> <b>TOM4_13</b>, Output of TOM4, channel 13      0E<sub>H</sub> <b>TOM4_14</b>, Output of TOM4, channel 14      0F<sub>H</sub> <b>TOM4_15</b>, Output of TOM4, channel 15      10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0      11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1      12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2      13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3      14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4      15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5      16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6      17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7      18<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      19<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      1A<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      1B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      1C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      1D<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      1E<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      1F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=6;j=2)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0

SEL11

0

SEL10

r

rw

r

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0

SEL9

0

SEL8

r

rw

r

rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=8-11)</b>	8*k-60:8*k-64	rw	<p><b>Set 6[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0      01<sub>H</sub> <b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1      02<sub>H</sub> <b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2      03<sub>H</sub> <b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3      04<sub>H</sub> <b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4      05<sub>H</sub> <b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5      06<sub>H</sub> <b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6      07<sub>H</sub> <b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7      08<sub>H</sub> <b>TOM4_8</b>, Output of TOM4, channel 8      09<sub>H</sub> <b>TOM4_9</b>, Output of TOM4, channel 9      0A<sub>H</sub> <b>TOM4_10</b>, Output of TOM4, channel 10      0B<sub>H</sub> <b>TOM4_11</b>, Output of TOM4, channel 11      0C<sub>H</sub> <b>TOM4_12</b>, Output of TOM4, channel 12      0D<sub>H</sub> <b>TOM4_13</b>, Output of TOM4, channel 13      0E<sub>H</sub> <b>TOM4_14</b>, Output of TOM4, channel 14      0F<sub>H</sub> <b>TOM4_15</b>, Output of TOM4, channel 15      10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0      11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1      12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2      13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3      14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4      15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5      16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6      17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7      18<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      19<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      1A<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      1B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      1C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      1D<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      1E<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      1F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=6;j=3)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0

SEL15

0

SEL14

r

rw

r

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0

SEL13

0

SEL12

r

rw

r

rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 6[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>CDTM4_DTM0_0, TOM4_0</b>, Dead-time output of TOM4, channel 0      01<sub>H</sub> <b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1      02<sub>H</sub> <b>CDTM4_DTM0_2, TOM4_2</b>, Dead-time output of TOM4, channel 2      03<sub>H</sub> <b>CDTM4_DTM0_3, TOM4_3</b>, Dead-time output of TOM4, channel 3      04<sub>H</sub> <b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4      05<sub>H</sub> <b>CDTM4_DTM1_1, TOM4_5</b>, Dead-time output of TOM4, channel 5      06<sub>H</sub> <b>CDTM4_DTM1_2, TOM4_6</b>, Dead-time output of TOM4, channel 6      07<sub>H</sub> <b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7      08<sub>H</sub> <b>TOM4_8</b>, Output of TOM4, channel 8      09<sub>H</sub> <b>TOM4_9</b>, Output of TOM4, channel 9      0A<sub>H</sub> <b>TOM4_10</b>, Output of TOM4, channel 10      0B<sub>H</sub> <b>TOM4_11</b>, Output of TOM4, channel 11      0C<sub>H</sub> <b>TOM4_12</b>, Output of TOM4, channel 12      0D<sub>H</sub> <b>TOM4_13</b>, Output of TOM4, channel 13      0E<sub>H</sub> <b>TOM4_14</b>, Output of TOM4, channel 14      0F<sub>H</sub> <b>TOM4_15</b>, Output of TOM4, channel 15      10<sub>H</sub> <b>ATOM7_0</b>, Output of ATOM7, channel 0      11<sub>H</sub> <b>ATOM7_1</b>, Output of ATOM7, channel 1      12<sub>H</sub> <b>ATOM7_2</b>, Output of ATOM7, channel 2      13<sub>H</sub> <b>ATOM7_3</b>, Output of ATOM7, channel 3      14<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4      15<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5      16<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6      17<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7      18<sub>H</sub> <b>CDTM5_DTM4_0, ATOM5_0</b>, Dead-time output of ATOM5, channel 0      19<sub>H</sub> <b>CDTM5_DTM4_1, ATOM5_1</b>, Dead-time output of ATOM5, channel 1      1A<sub>H</sub> <b>CDTM5_DTM4_2, ATOM5_2</b>, Dead-time output of ATOM5, channel 2      1B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      1C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4      1D<sub>H</sub> <b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5      1E<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      1F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## GTM\_MSCSETiCONj (i=7;j=0)

## **MSC Set i Control j Register**

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)

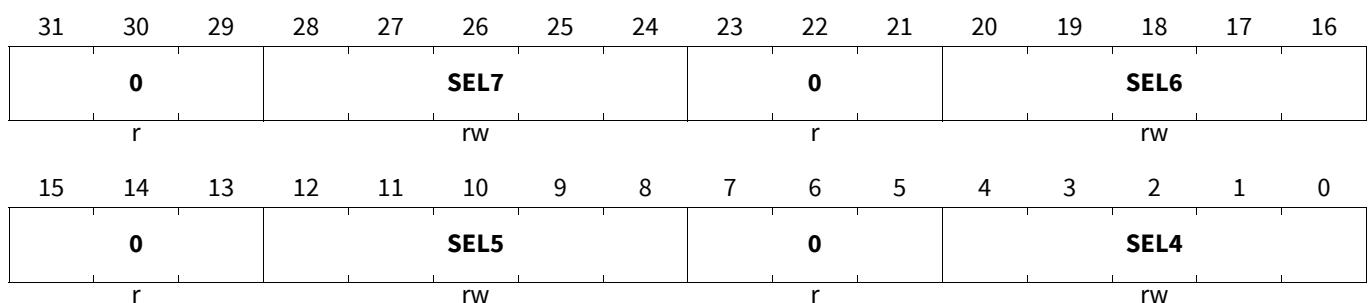
**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SEL3					SEL2		
r								rw					rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SEL1					SEL0		
r								rw					rw		

Field	Bits	Type	Description
<b>SELk (k=0-3)</b>	8*k+4:8*k	rw	<p><b>Set 7[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <ul style="list-style-type: none"> <li>00<sub>H</sub> <b>TOM5_0</b>, Output of TOM5, channel 0</li> <li>01<sub>H</sub> <b>TOM5_1</b>, Output of TOM5, channel 1</li> <li>02<sub>H</sub> <b>TOM5_2</b>, Output of TOM5, channel 2</li> <li>03<sub>H</sub> <b>TOM5_3</b>, Output of TOM5, channel 3</li> <li>04<sub>H</sub> <b>TOM5_4</b>, Output of TOM5, channel 4</li> <li>05<sub>H</sub> <b>TOM5_5</b>, Output of TOM5, channel 5</li> <li>06<sub>H</sub> <b>TOM5_6</b>, Output of TOM5, channel 6</li> <li>07<sub>H</sub> <b>TOM5_7</b>, Output of TOM5, channel 7</li> <li>08<sub>H</sub> <b>TOM5_8</b>, Output of TOM5, channel 8</li> <li>09<sub>H</sub> <b>TOM5_9</b>, Output of TOM5, channel 9</li> <li>0A<sub>H</sub> <b>TOM5_10</b>, Output of TOM5, channel 10</li> <li>0B<sub>H</sub> <b>TOM5_11</b>, Output of TOM5, channel 11</li> <li>0C<sub>H</sub> <b>TOM5_12</b>, Output of TOM5, channel 12</li> <li>0D<sub>H</sub> <b>TOM5_13</b>, Output of TOM5, channel 13</li> <li>0E<sub>H</sub> <b>TOM5_14</b>, Output of TOM5, channel 14</li> <li>0F<sub>H</sub> <b>TOM5_15</b>, Output of TOM5, channel 15</li> <li>10<sub>H</sub> <b>ATOM9_0</b>, Output of ATOM9, channel 0</li> <li>11<sub>H</sub> <b>ATOM9_1</b>, Output of ATOM9, channel 1</li> <li>12<sub>H</sub> <b>ATOM9_2</b>, Output of ATOM9, channel 2</li> <li>13<sub>H</sub> <b>ATOM9_3</b>, Output of ATOM9, channel 3</li> <li>14<sub>H</sub> <b>ATOM9_4</b>, Output of ATOM9, channel 4</li> <li>15<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5</li> <li>16<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6</li> <li>17<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7</li> <li>18<sub>H</sub> <b>ATOM10_0</b>, Output of ATOM10, channel 0</li> <li>19<sub>H</sub> <b>ATOM10_1</b>, Output of ATOM10, channel 1</li> <li>1A<sub>H</sub> <b>ATOM10_2</b>, Output of ATOM10, channel 2</li> <li>1B<sub>H</sub> <b>ATOM10_3</b>, Output of ATOM10, channel 3</li> <li>1C<sub>H</sub> <b>ATOM10_4</b>, Output of ATOM10, channel 4</li> <li>1D<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5</li> <li>1E<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6</li> <li>1F<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7</li> </ul>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=7;j=1)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=4-7)</b>	8*k-28:8*k-32	rw	<p><b>Set 7[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p> <math>00_H</math> <b>TOM5_0</b>, Output of TOM5, channel 0  <math>01_H</math> <b>TOM5_1</b>, Output of TOM5, channel 1  <math>02_H</math> <b>TOM5_2</b>, Output of TOM5, channel 2  <math>03_H</math> <b>TOM5_3</b>, Output of TOM5, channel 3  <math>04_H</math> <b>TOM5_4</b>, Output of TOM5, channel 4  <math>05_H</math> <b>TOM5_5</b>, Output of TOM5, channel 5  <math>06_H</math> <b>TOM5_6</b>, Output of TOM5, channel 6  <math>07_H</math> <b>TOM5_7</b>, Output of TOM5, channel 7  <math>08_H</math> <b>TOM5_8</b>, Output of TOM5, channel 8  <math>09_H</math> <b>TOM5_9</b>, Output of TOM5, channel 9  <math>0A_H</math> <b>TOM5_10</b>, Output of TOM5, channel 10  <math>0B_H</math> <b>TOM5_11</b>, Output of TOM5, channel 11  <math>0C_H</math> <b>TOM5_12</b>, Output of TOM5, channel 12  <math>0D_H</math> <b>TOM5_13</b>, Output of TOM5, channel 13  <math>0E_H</math> <b>TOM5_14</b>, Output of TOM5, channel 14  <math>0F_H</math> <b>TOM5_15</b>, Output of TOM5, channel 15  <math>10_H</math> <b>ATOM9_0</b>, Output of ATOM9, channel 0  <math>11_H</math> <b>ATOM9_1</b>, Output of ATOM9, channel 1  <math>12_H</math> <b>ATOM9_2</b>, Output of ATOM9, channel 2  <math>13_H</math> <b>ATOM9_3</b>, Output of ATOM9, channel 3  <math>14_H</math> <b>ATOM9_4</b>, Output of ATOM9, channel 4  <math>15_H</math> <b>ATOM9_5</b>, Output of ATOM9, channel 5  <math>16_H</math> <b>ATOM9_6</b>, Output of ATOM9, channel 6  <math>17_H</math> <b>ATOM9_7</b>, Output of ATOM9, channel 7  <math>18_H</math> <b>ATOM10_0</b>, Output of ATOM10, channel 0  <math>19_H</math> <b>ATOM10_1</b>, Output of ATOM10, channel 1  <math>1A_H</math> <b>ATOM10_2</b>, Output of ATOM10, channel 2  <math>1B_H</math> <b>ATOM10_3</b>, Output of ATOM10, channel 3  <math>1C_H</math> <b>ATOM10_4</b>, Output of ATOM10, channel 4  <math>1D_H</math> <b>ATOM10_5</b>, Output of ATOM10, channel 5  <math>1E_H</math> <b>ATOM10_6</b>, Output of ATOM10, channel 6  <math>1F_H</math> <b>ATOM10_7</b>, Output of ATOM10, channel 7     </p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## GTM\_MSCSETiCONj (i=7;j=2)

## MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0				SEL11				0				SEL10		
r					rw				r				rw		

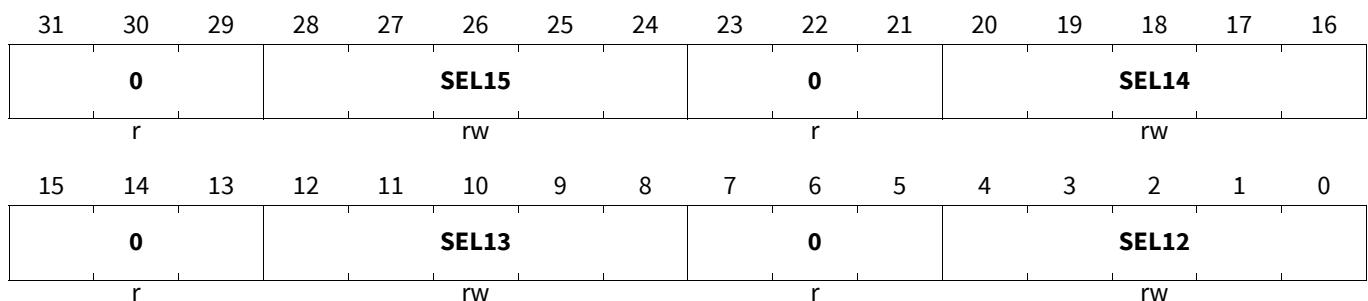
  

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0				SEL9				0				SEL8		
r					rw				r				rw		

Field	Bits	Type	Description
SELk (k=8-11)	8*k-60:8*k-64	rw	<p><b>Set 7[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>TOM5_0</b>, Output of TOM5, channel 0      01<sub>H</sub> <b>TOM5_1</b>, Output of TOM5, channel 1      02<sub>H</sub> <b>TOM5_2</b>, Output of TOM5, channel 2      03<sub>H</sub> <b>TOM5_3</b>, Output of TOM5, channel 3      04<sub>H</sub> <b>TOM5_4</b>, Output of TOM5, channel 4      05<sub>H</sub> <b>TOM5_5</b>, Output of TOM5, channel 5      06<sub>H</sub> <b>TOM5_6</b>, Output of TOM5, channel 6      07<sub>H</sub> <b>TOM5_7</b>, Output of TOM5, channel 7      08<sub>H</sub> <b>TOM5_8</b>, Output of TOM5, channel 8      09<sub>H</sub> <b>TOM5_9</b>, Output of TOM5, channel 9      0A<sub>H</sub> <b>TOM5_10</b>, Output of TOM5, channel 10      0B<sub>H</sub> <b>TOM5_11</b>, Output of TOM5, channel 11      0C<sub>H</sub> <b>TOM5_12</b>, Output of TOM5, channel 12      0D<sub>H</sub> <b>TOM5_13</b>, Output of TOM5, channel 13      0E<sub>H</sub> <b>TOM5_14</b>, Output of TOM5, channel 14      0F<sub>H</sub> <b>TOM5_15</b>, Output of TOM5, channel 15      10<sub>H</sub> <b>ATOM9_0</b>, Output of ATOM9, channel 0      11<sub>H</sub> <b>ATOM9_1</b>, Output of ATOM9, channel 1      12<sub>H</sub> <b>ATOM9_2</b>, Output of ATOM9, channel 2      13<sub>H</sub> <b>ATOM9_3</b>, Output of ATOM9, channel 3      14<sub>H</sub> <b>ATOM9_4</b>, Output of ATOM9, channel 4      15<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5      16<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6      17<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7      18<sub>H</sub> <b>ATOM10_0</b>, Output of ATOM10, channel 0      19<sub>H</sub> <b>ATOM10_1</b>, Output of ATOM10, channel 1      1A<sub>H</sub> <b>ATOM10_2</b>, Output of ATOM10, channel 2      1B<sub>H</sub> <b>ATOM10_3</b>, Output of ATOM10, channel 3      1C<sub>H</sub> <b>ATOM10_4</b>, Output of ATOM10, channel 4      1D<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5      1E<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6      1F<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=7;j=3)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 7[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <ul style="list-style-type: none"> <li>00<sub>H</sub> <b>TOM5_0</b>, Output of TOM5, channel 0</li> <li>01<sub>H</sub> <b>TOM5_1</b>, Output of TOM5, channel 1</li> <li>02<sub>H</sub> <b>TOM5_2</b>, Output of TOM5, channel 2</li> <li>03<sub>H</sub> <b>TOM5_3</b>, Output of TOM5, channel 3</li> <li>04<sub>H</sub> <b>TOM5_4</b>, Output of TOM5, channel 4</li> <li>05<sub>H</sub> <b>TOM5_5</b>, Output of TOM5, channel 5</li> <li>06<sub>H</sub> <b>TOM5_6</b>, Output of TOM5, channel 6</li> <li>07<sub>H</sub> <b>TOM5_7</b>, Output of TOM5, channel 7</li> <li>08<sub>H</sub> <b>TOM5_8</b>, Output of TOM5, channel 8</li> <li>09<sub>H</sub> <b>TOM5_9</b>, Output of TOM5, channel 9</li> <li>0A<sub>H</sub> <b>TOM5_10</b>, Output of TOM5, channel 10</li> <li>0B<sub>H</sub> <b>TOM5_11</b>, Output of TOM5, channel 11</li> <li>0C<sub>H</sub> <b>TOM5_12</b>, Output of TOM5, channel 12</li> <li>0D<sub>H</sub> <b>TOM5_13</b>, Output of TOM5, channel 13</li> <li>0E<sub>H</sub> <b>TOM5_14</b>, Output of TOM5, channel 14</li> <li>0F<sub>H</sub> <b>TOM5_15</b>, Output of TOM5, channel 15</li> <li>10<sub>H</sub> <b>ATOM9_0</b>, Output of ATOM9, channel 0</li> <li>11<sub>H</sub> <b>ATOM9_1</b>, Output of ATOM9, channel 1</li> <li>12<sub>H</sub> <b>ATOM9_2</b>, Output of ATOM9, channel 2</li> <li>13<sub>H</sub> <b>ATOM9_3</b>, Output of ATOM9, channel 3</li> <li>14<sub>H</sub> <b>ATOM9_4</b>, Output of ATOM9, channel 4</li> <li>15<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5</li> <li>16<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6</li> <li>17<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7</li> <li>18<sub>H</sub> <b>ATOM10_0</b>, Output of ATOM10, channel 0</li> <li>19<sub>H</sub> <b>ATOM10_1</b>, Output of ATOM10, channel 1</li> <li>1A<sub>H</sub> <b>ATOM10_2</b>, Output of ATOM10, channel 2</li> <li>1B<sub>H</sub> <b>ATOM10_3</b>, Output of ATOM10, channel 3</li> <li>1C<sub>H</sub> <b>ATOM10_4</b>, Output of ATOM10, channel 4</li> <li>1D<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5</li> <li>1E<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6</li> <li>1F<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7</li> </ul>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=8;j=0)

MSC Set i Control j Register

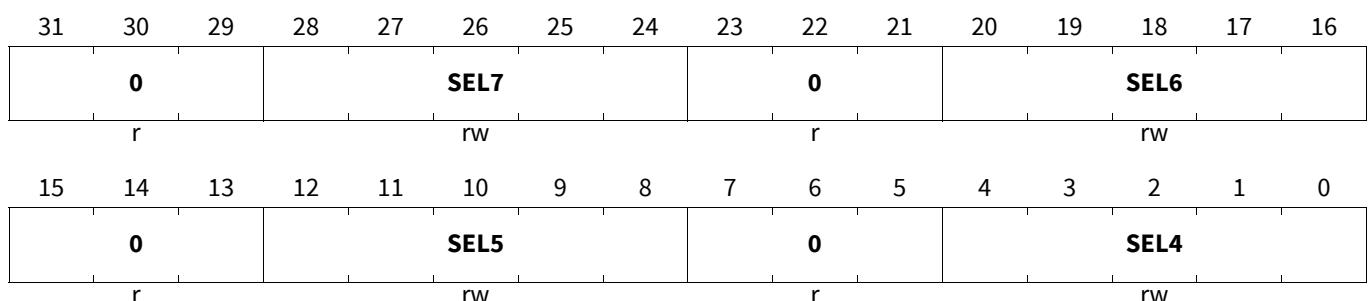
(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0				SEL3			0			SEL2				
r					rw			r			rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0				SEL1			0			SEL0				
r					rw			r			rw				

Field	Bits	Type	Description
SELk (k=0-3)	8*k+4:8*k	rw	<p><b>Set 8[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>ATOM11_0</b>, Output of ATOM11, channel 0      01<sub>H</sub> <b>ATOM11_1</b>, Output of ATOM11, channel 1      02<sub>H</sub> <b>ATOM11_2</b>, Output of ATOM11, channel 2      03<sub>H</sub> <b>ATOM11_3</b>, Output of ATOM11, channel 3      04<sub>H</sub> <b>ATOM11_4</b>, Output of ATOM11, channel 4      05<sub>H</sub> <b>ATOM11_5</b>, Output of ATOM11, channel 5      06<sub>H</sub> <b>ATOM11_6</b>, Output of ATOM11, channel 6      07<sub>H</sub> <b>ATOM11_7</b>, Output of ATOM11, channel 7      08<sub>H</sub> <b>ATOM10_0</b>, Output of ATOM10, channel 0      09<sub>H</sub> <b>ATOM10_1</b>, Output of ATOM10, channel 1      0A<sub>H</sub> <b>ATOM10_2</b>, Output of ATOM10, channel 2      0B<sub>H</sub> <b>ATOM10_3</b>, Output of ATOM10, channel 3      0C<sub>H</sub> <b>ATOM10_4</b>, Output of ATOM10, channel 4      0D<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5      0E<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6      0F<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7      10<sub>H</sub> <b>ATOM9_0</b>, Output of ATOM9, channel 0      11<sub>H</sub> <b>ATOM9_1</b>, Output of ATOM9, channel 1      12<sub>H</sub> <b>ATOM9_2</b>, Output of ATOM9, channel 2      13<sub>H</sub> <b>ATOM9_3</b>, Output of ATOM9, channel 3      14<sub>H</sub> <b>ATOM9_4</b>, Output of ATOM9, channel 4      15<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5      16<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6      17<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7      18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0      19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1      1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2      1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3      1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4      1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5      1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6      1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</p>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=8;j=1)****MSC Set i Control j Register**(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=4-7)</b>	8*k-28:8*k-32	rw	<p><b>Set 8[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>ATOM11_0</b>, Output of ATOM11, channel 0      01<sub>H</sub> <b>ATOM11_1</b>, Output of ATOM11, channel 1      02<sub>H</sub> <b>ATOM11_2</b>, Output of ATOM11, channel 2      03<sub>H</sub> <b>ATOM11_3</b>, Output of ATOM11, channel 3      04<sub>H</sub> <b>ATOM11_4</b>, Output of ATOM11, channel 4      05<sub>H</sub> <b>ATOM11_5</b>, Output of ATOM11, channel 5      06<sub>H</sub> <b>ATOM11_6</b>, Output of ATOM11, channel 6      07<sub>H</sub> <b>ATOM11_7</b>, Output of ATOM11, channel 7      08<sub>H</sub> <b>ATOM10_0</b>, Output of ATOM10, channel 0      09<sub>H</sub> <b>ATOM10_1</b>, Output of ATOM10, channel 1      0A<sub>H</sub> <b>ATOM10_2</b>, Output of ATOM10, channel 2      0B<sub>H</sub> <b>ATOM10_3</b>, Output of ATOM10, channel 3      0C<sub>H</sub> <b>ATOM10_4</b>, Output of ATOM10, channel 4      0D<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5      0E<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6      0F<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7      10<sub>H</sub> <b>ATOM9_0</b>, Output of ATOM9, channel 0      11<sub>H</sub> <b>ATOM9_1</b>, Output of ATOM9, channel 1      12<sub>H</sub> <b>ATOM9_2</b>, Output of ATOM9, channel 2      13<sub>H</sub> <b>ATOM9_3</b>, Output of ATOM9, channel 3      14<sub>H</sub> <b>ATOM9_4</b>, Output of ATOM9, channel 4      15<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5      16<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6      17<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7      18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0      19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1      1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2      1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3      1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4      1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5      1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6      1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

GTM\_MSCSETiCONj (i=8;j=2)

MSC Set i Control j Register

(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0				SEL11			0					SEL10		
r					rw			r					rw		

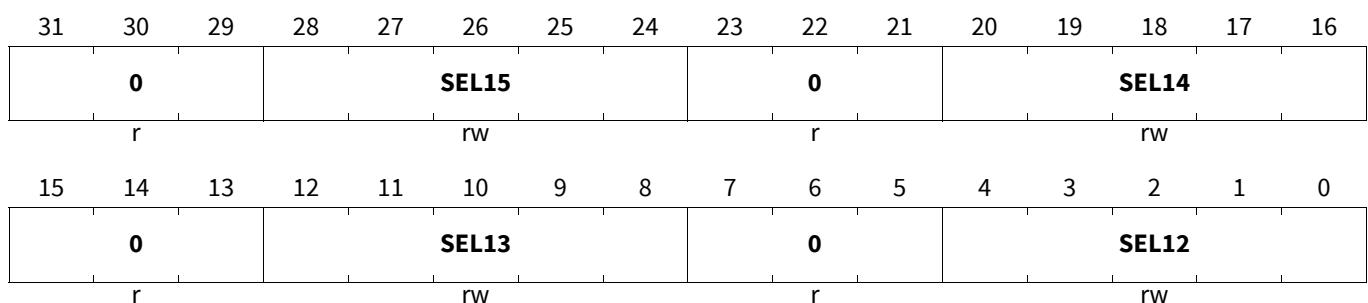
  

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0				SEL9			0					SEL8		
r					rw			r					rw		

Field	Bits	Type	Description
SELk (k=8-11)	8*k-60:8*k-64	rw	<p><b>Set 8[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>ATOM11_0</b>, Output of ATOM11, channel 0      01<sub>H</sub> <b>ATOM11_1</b>, Output of ATOM11, channel 1      02<sub>H</sub> <b>ATOM11_2</b>, Output of ATOM11, channel 2      03<sub>H</sub> <b>ATOM11_3</b>, Output of ATOM11, channel 3      04<sub>H</sub> <b>ATOM11_4</b>, Output of ATOM11, channel 4      05<sub>H</sub> <b>ATOM11_5</b>, Output of ATOM11, channel 5      06<sub>H</sub> <b>ATOM11_6</b>, Output of ATOM11, channel 6      07<sub>H</sub> <b>ATOM11_7</b>, Output of ATOM11, channel 7      08<sub>H</sub> <b>ATOM10_0</b>, Output of ATOM10, channel 0      09<sub>H</sub> <b>ATOM10_1</b>, Output of ATOM10, channel 1      0A<sub>H</sub> <b>ATOM10_2</b>, Output of ATOM10, channel 2      0B<sub>H</sub> <b>ATOM10_3</b>, Output of ATOM10, channel 3      0C<sub>H</sub> <b>ATOM10_4</b>, Output of ATOM10, channel 4      0D<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5      0E<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6      0F<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7      10<sub>H</sub> <b>ATOM9_0</b>, Output of ATOM9, channel 0      11<sub>H</sub> <b>ATOM9_1</b>, Output of ATOM9, channel 1      12<sub>H</sub> <b>ATOM9_2</b>, Output of ATOM9, channel 2      13<sub>H</sub> <b>ATOM9_3</b>, Output of ATOM9, channel 3      14<sub>H</sub> <b>ATOM9_4</b>, Output of ATOM9, channel 4      15<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5      16<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6      17<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7      18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0      19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1      1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2      1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3      1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4      1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5      1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6      1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
0	31:29, 23:21, 15:13, 7:5	r	<b>Reserved</b> Read as 0, shall be written with 0.

**GTM\_MSCSETiCONj (i=8;j=3)****MSC Set i Control j Register****(09FF00<sub>H</sub>+i\*10<sub>H</sub>+j\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELk (k=12-15)</b>	8*k-92:8*k-96	rw	<p><b>Set 8[k] Input Selection</b></p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00<sub>H</sub> <b>ATOM11_0</b>, Output of ATOM11, channel 0      01<sub>H</sub> <b>ATOM11_1</b>, Output of ATOM11, channel 1      02<sub>H</sub> <b>ATOM11_2</b>, Output of ATOM11, channel 2      03<sub>H</sub> <b>ATOM11_3</b>, Output of ATOM11, channel 3      04<sub>H</sub> <b>ATOM11_4</b>, Output of ATOM11, channel 4      05<sub>H</sub> <b>ATOM11_5</b>, Output of ATOM11, channel 5      06<sub>H</sub> <b>ATOM11_6</b>, Output of ATOM11, channel 6      07<sub>H</sub> <b>ATOM11_7</b>, Output of ATOM11, channel 7      08<sub>H</sub> <b>ATOM10_0</b>, Output of ATOM10, channel 0      09<sub>H</sub> <b>ATOM10_1</b>, Output of ATOM10, channel 1      0A<sub>H</sub> <b>ATOM10_2</b>, Output of ATOM10, channel 2      0B<sub>H</sub> <b>ATOM10_3</b>, Output of ATOM10, channel 3      0C<sub>H</sub> <b>ATOM10_4</b>, Output of ATOM10, channel 4      0D<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5      0E<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6      0F<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7      10<sub>H</sub> <b>ATOM9_0</b>, Output of ATOM9, channel 0      11<sub>H</sub> <b>ATOM9_1</b>, Output of ATOM9, channel 1      12<sub>H</sub> <b>ATOM9_2</b>, Output of ATOM9, channel 2      13<sub>H</sub> <b>ATOM9_3</b>, Output of ATOM9, channel 3      14<sub>H</sub> <b>ATOM9_4</b>, Output of ATOM9, channel 4      15<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5      16<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6      17<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7      18<sub>H</sub> <b>ATOM8_0</b>, Output of ATOM8, channel 0      19<sub>H</sub> <b>ATOM8_1</b>, Output of ATOM8, channel 1      1A<sub>H</sub> <b>ATOM8_2</b>, Output of ATOM8, channel 2      1B<sub>H</sub> <b>ATOM8_3</b>, Output of ATOM8, channel 3      1C<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4      1D<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5      1E<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6      1F<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</p>
<b>0</b>	31:29, 23:21, 15:13, 7:5	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## MSCi Input Low Control Register

## GTM\_MSCiINLCON (i=0)

## MSCi Input Low Control Register

(09FF90<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq Low x Output Selection</b> GTM output gtm_mscqltinl[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET1</b> , Outputs SET1[15:0] selected 10 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 11 <sub>B</sub> <b>SET3</b> , Outputs SET3[15:0] selected

## MSCi Input High Control Register

## GTM\_MSCiINHCON (i=0)

## MSCi Input High Control Register

(09FF94<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq High x Output Selection</b> GTM output gtm_mscqaltinh[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET1</b> , Outputs SET1[15:0] selected 10 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 11 <sub>B</sub> <b>SET3</b> , Outputs SET3[15:0] selected

## Generic Timer Module (GTM)

## MSCi Input Low Extended Control Register

## GTM\_MSCiINLEXTCON (i=0)

MSCi Input Low Extended Control Register (09FF98<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq LowExtended x Output Selection</b> GTM output gtm_mscqaltinext[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET1</b> , Outputs SET1[15:0] selected 10 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 11 <sub>B</sub> <b>SET3</b> , Outputs SET3[15:0] selected

## GTM\_MSCiINLCON (i=1)

MSCi Input Low Control Register

(09FF90<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq Low x Output Selection</b> GTM output gtm_mscqltinl[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET1</b> , Outputs SET1[15:0] selected 10 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 11 <sub>B</sub> <b>SET3</b> , Outputs SET3[15:0] selected

## Generic Timer Module (GTM)

## GTM\_MSCiINHCON (i=1)

## MSCi Input High Control Register

(09FF94<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq High x Output Selection</b> GTM output gtm_mscqaltinh[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET1</b> , Outputs SET1[15:0] selected 10 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 11 <sub>B</sub> <b>SET3</b> , Outputs SET3[15:0] selected

## GTM\_MSCiINLEXTCON (i=1)

MSCi Input Low Extended Control Register (09FF98<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq LowExtended x Output Selection</b> GTM output gtm_mscqaltinext[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET1</b> , Outputs SET1[15:0] selected 10 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 11 <sub>B</sub> <b>SET3</b> , Outputs SET3[15:0] selected

## Generic Timer Module (GTM)

## GTM\_MSCiINLCON (i=2)

## MSCi Input Low Control Register

(09FF90<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq Low x Output Selection</b> GTM output gtm_mscqltinl[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 10 <sub>B</sub> <b>SET6</b> , Outputs SET6[15:0] selected 11 <sub>B</sub> <b>SET7</b> , Outputs SET7[15:0] selected

## GTM\_MSCiINHCON (i=2)

## MSCi Input High Control Register

(09FF94<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq High x Output Selection</b> GTM output gtm_mscqaltnh[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 10 <sub>B</sub> <b>SET5</b> , Outputs SET5[15:0] selected 11 <sub>B</sub> <b>SET4</b> , Outputs SET4[15:0] selected

## Generic Timer Module (GTM)

## GTM\_MSCiINLEXTCON (i=2)

MSCi Input Low Extended Control Register (09FF98<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq LowExtended x Output Selection</b> GTM output gtm_mscqaltinext[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET0</b> , Outputs SET0[15:0] selected 01 <sub>B</sub> <b>SET2</b> , Outputs SET2[15:0] selected 10 <sub>B</sub> <b>SET5</b> , Outputs SET5[15:0] selected 11 <sub>B</sub> <b>SET4</b> , Outputs SET4[15:0] selected

## GTM\_MSCiINLCON (i=3)

## MSCi Input Low Control Register

(09FF90<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq Low x Output Selection</b> GTM output gtm_mscltinl[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET7</b> , Outputs SET7[15:0] selected 01 <sub>B</sub> <b>SET8</b> , Outputs SET8[15:0] selected 10 <sub>B</sub> <b>SET6</b> , Outputs SET6[15:0] selected 11 <sub>B</sub> <b>SET5</b> , Outputs SET5[15:0] selected

## Generic Timer Module (GTM)

## GTM\_MSCiINHCON (i=3)

## MSCi Input High Control Register

(09FF94<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq High x Output Selection</b> GTM output gtm_mscqaltinh[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET7</b> , Outputs SET7[15:0] selected 01 <sub>B</sub> <b>SET8</b> , Outputs SET8[15:0] selected 10 <sub>B</sub> <b>SET6</b> , Outputs SET6[15:0] selected 11 <sub>B</sub> <b>SET5</b> , Outputs SET5[15:0] selected

## GTM\_MSCiINLEXTCON (i=3)

MSCi Input Low Extended Control Register (09FF98<sub>H</sub>+i\*12)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL15</b>	<b>SEL14</b>	<b>SEL13</b>	<b>SEL12</b>	<b>SEL11</b>	<b>SEL10</b>	<b>SEL9</b>	<b>SEL8</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL7</b>	<b>SEL6</b>	<b>SEL5</b>	<b>SEL4</b>	<b>SEL3</b>	<b>SEL2</b>	<b>SEL1</b>	<b>SEL0</b>								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>SELx (x=0-15)</b>	2*x+1:2*x	rw	<b>GTM MSCq LowExtended x Output Selection</b> GTM output gtm_mscqaltinext[x] is controlled by the timer output. 00 <sub>B</sub> <b>SET7</b> , Outputs SET7[15:0] selected 01 <sub>B</sub> <b>SET8</b> , Outputs SET8[15:0] selected 10 <sub>B</sub> <b>SET6</b> , Outputs SET6[15:0] selected 11 <sub>B</sub> <b>SET5</b> , Outputs SET5[15:0] selected

## Generic Timer Module (GTM)

## 26.3.6 EDSADC to GTM TIM Connections

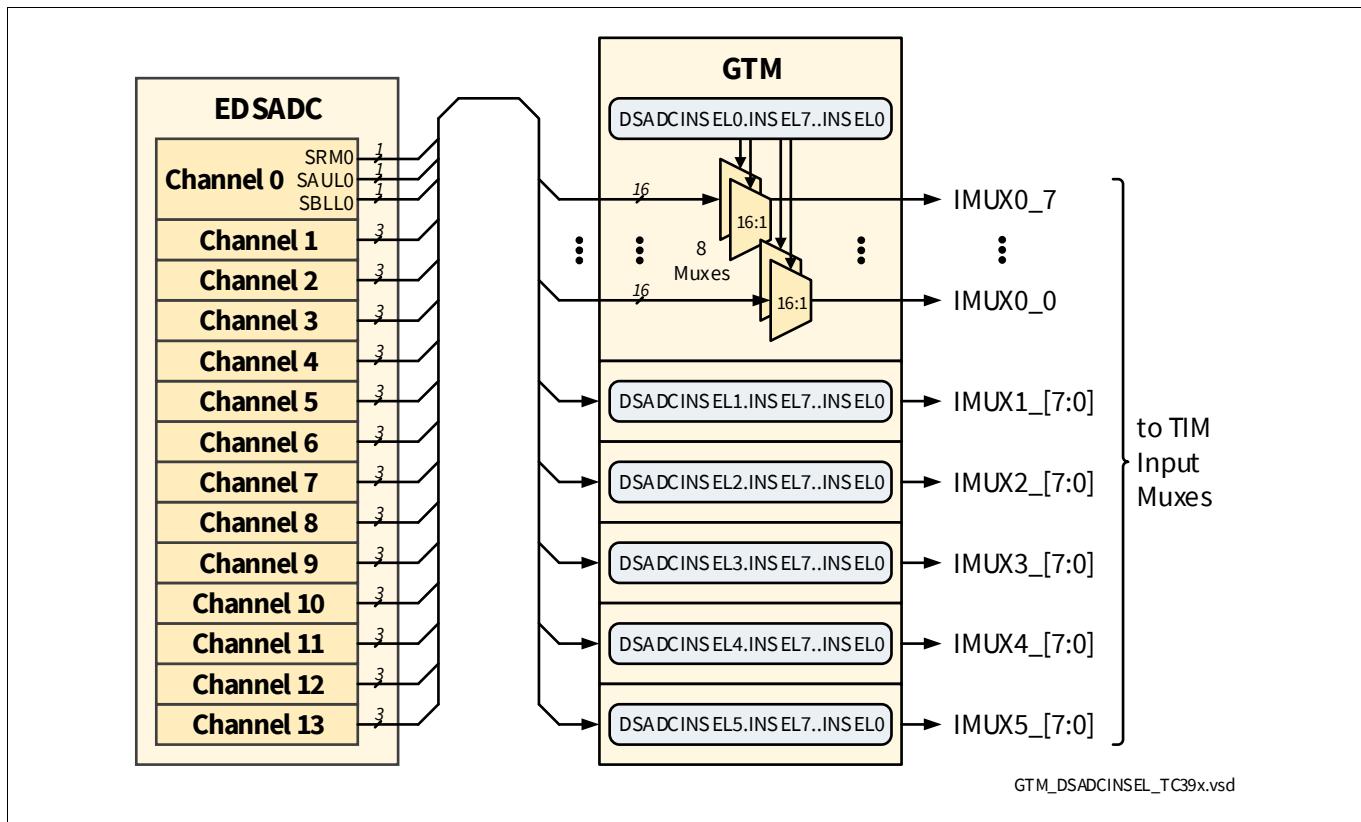


Figure 20 EDSADC to GTM Connections Overview

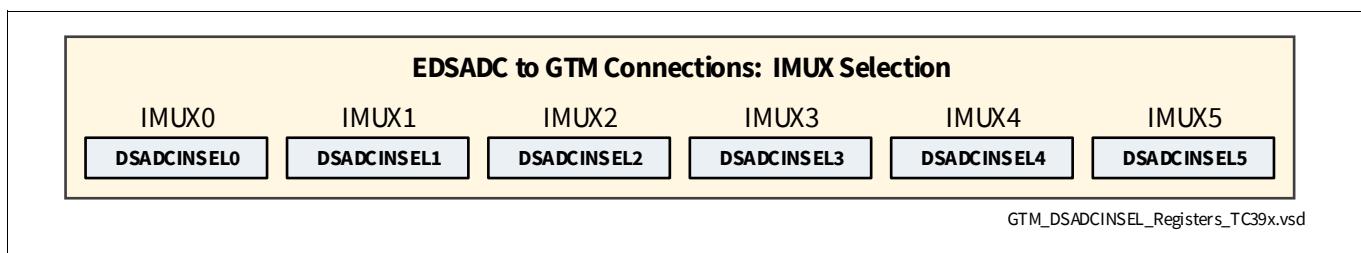


Figure 21 EDSADC to GTM Connections Registers Overview

Table 335 EDSADC to GTM Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
DSADCINSEL0	DSADC Input Select 0 Register (i=0)	INSEL0..INSEL7	<a href="#">Page 341</a>
DSADCINSEL1	DSADC Input Select 1 Register (i=1)	INSEL0..INSEL7	<a href="#">Page 345</a>
DSADCINSEL2	DSADC Input Select 2 Register (i=2)	INSEL0..INSEL7	<a href="#">Page 350</a>
DSADCINSEL3	DSADC Input Select 3 Register (i=3)	INSEL0..INSEL7	<a href="#">Page 354</a>
DSADCINSEL4	DSADC Input Select 4 Register (i=4)	INSEL0..INSEL7	<a href="#">Page 359</a>
DSADCINSEL5	DSADC Input Select 5 Register (i=5)	INSEL0..INSEL7	<a href="#">Page 363</a>

## Generic Timer Module (GTM)

### DSADC Input Select i Register

**GTM\_DSADCINSELi (i=0)**

**DSADC Input Select i Register**

**(09FE00<sub>H</sub>+i\*4)**

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>INSEL7</b>				<b>INSEL6</b>				<b>INSEL5</b>				<b>INSEL4</b>			
rw					rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>INSEL3</b>				<b>INSEL2</b>				<b>INSEL1</b>				<b>INSEL0</b>			
rw					rw				rw				rw		

Field	Bits	Type	Description
<b>INSELj (j=0)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0      1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1      2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2      3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3      4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4      5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5      6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6      7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7      8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8      9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9      A<sub>H</sub> <b>SAUL0</b>, Input signal is DSADC_SAUL0      B<sub>H</sub> <b>SBLL0</b>, Input signal is DSADC_SBLL0      C<sub>H</sub> <b>SAUL1</b>, Input signal is DSADC_SAUL1      D<sub>H</sub> <b>SBLL1</b>, Input signal is DSADC_SBLL1      E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10      F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=1)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL1</b>, Input signal is DSADC_SAUL1  <math>B_H</math> <b>SBLL1</b>, Input signal is DSADC_SBLL1  <math>C_H</math> <b>SAUL0</b>, Input signal is DSADC_SAUL0  <math>D_H</math> <b>SBLL0</b>, Input signal is DSADC_SBLL0  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11       </p>
<b>INSELj (j=2)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL2</b>, Input signal is DSADC_SAUL2  <math>B_H</math> <b>SBLL2</b>, Input signal is DSADC_SBLL2  <math>C_H</math> <b>SAUL3</b>, Input signal is DSADC_SAUL3  <math>D_H</math> <b>SBLL3</b>, Input signal is DSADC_SBLL3  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11       </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=3)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL3</b>, Input signal is DSADC_SAUL3  <math>B_H</math> <b>SBLL3</b>, Input signal is DSADC_SBLL3  <math>C_H</math> <b>SAUL2</b>, Input signal is DSADC_SAUL2  <math>D_H</math> <b>SBLL2</b>, Input signal is DSADC_SBLL2  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>
<b>INSELj (j=4)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL4</b>, Input signal is DSADC_SAUL4  <math>B_H</math> <b>SBLL4</b>, Input signal is DSADC_SBLL4  <math>C_H</math> <b>SAUL5</b>, Input signal is DSADC_SAUL5  <math>D_H</math> <b>SBLL5</b>, Input signal is DSADC_SBLL5  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=5)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL5</b>, Input signal is DSADC_SAUL5  <math>B_H</math> <b>SBLL5</b>, Input signal is DSADC_SBLL5  <math>C_H</math> <b>SAUL4</b>, Input signal is DSADC_SAUL4  <math>D_H</math> <b>SBLL4</b>, Input signal is DSADC_SBLL4  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11       </p>
<b>INSELj (j=6)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>B_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6  <math>C_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>D_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11       </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=7)</b>	$4^*j+3:4^*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>B_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7  <math>C_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>D_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>

**GTM\_DSADCINSELi (i=1)**

DSADC Input Select i Register

(09FE00<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INSEL7				INSEL6				INSEL5				INSEL4			
rw					rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INSEL3				INSEL2				INSEL1				INSEL0			

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSEL<sub>j</sub> (j=0)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADC<sub>n</sub> GTM connection</b></p> <p>This bit field defines which DSADC<sub>n</sub> output is connected if the channel input mux is configured as DSADC input for TIM<sub>i</sub> channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li>1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li>2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>A<sub>H</sub> <b>SAUL0</b>, Input signal is DSADC_SAUL0</li> <li>B<sub>H</sub> <b>SBLL0</b>, Input signal is DSADC_SBLL0</li> <li>C<sub>H</sub> <b>SAUL1</b>, Input signal is DSADC_SAUL1</li> <li>D<sub>H</sub> <b>SBLL1</b>, Input signal is DSADC_SBLL1</li> <li>E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>
<b>INSEL<sub>j</sub> (j=1)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADC<sub>n</sub> GTM connection</b></p> <p>This bit field defines which DSADC<sub>n</sub> output is connected if the channel input mux is configured as DSADC input for TIM<sub>i</sub> channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li>1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li>2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>A<sub>H</sub> <b>SAUL1</b>, Input signal is DSADC_SAUL1</li> <li>B<sub>H</sub> <b>SBLL1</b>, Input signal is DSADC_SBLL1</li> <li>C<sub>H</sub> <b>SAUL0</b>, Input signal is DSADC_SAUL0</li> <li>D<sub>H</sub> <b>SBLL0</b>, Input signal is DSADC_SBLL0</li> <li>E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=2)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li><math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li><math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li><math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li><math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li><math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li><math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li><math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li><math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li><math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li><math>A_H</math> <b>SAUL2</b>, Input signal is DSADC_SAUL2</li> <li><math>B_H</math> <b>SBLL2</b>, Input signal is DSADC_SBLL2</li> <li><math>C_H</math> <b>SAUL3</b>, Input signal is DSADC_SAUL3</li> <li><math>D_H</math> <b>SBLL3</b>, Input signal is DSADC_SBLL3</li> <li><math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li><math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>
<b>INSELj (j=3)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li><math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li><math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li><math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li><math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li><math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li><math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li><math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li><math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li><math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li><math>A_H</math> <b>SAUL3</b>, Input signal is DSADC_SAUL3</li> <li><math>B_H</math> <b>SBLL3</b>, Input signal is DSADC_SBLL3</li> <li><math>C_H</math> <b>SAUL2</b>, Input signal is DSADC_SAUL2</li> <li><math>D_H</math> <b>SBLL2</b>, Input signal is DSADC_SBLL2</li> <li><math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li><math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=4)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li>1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li>2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>A<sub>H</sub> <b>SAUL4</b>, Input signal is DSADC_SAUL4</li> <li>B<sub>H</sub> <b>SBLL4</b>, Input signal is DSADC_SBLL4</li> <li>C<sub>H</sub> <b>SAUL5</b>, Input signal is DSADC_SAUL5</li> <li>D<sub>H</sub> <b>SBLL5</b>, Input signal is DSADC_SBLL5</li> <li>E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>
<b>INSELj (j=5)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li>1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li>2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>A<sub>H</sub> <b>SAUL5</b>, Input signal is DSADC_SAUL5</li> <li>B<sub>H</sub> <b>SBLL5</b>, Input signal is DSADC_SBLL5</li> <li>C<sub>H</sub> <b>SAUL4</b>, Input signal is DSADC_SAUL4</li> <li>D<sub>H</sub> <b>SBLL4</b>, Input signal is DSADC_SBLL4</li> <li>E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=6)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>B_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6  <math>C_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>D_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>
<b>INSELj (j=7)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>B_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7  <math>C_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>D_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>

## Generic Timer Module (GTM)

## GTM\_DSADCINSELi (i=2)

## DSADC Input Select i Register

(09FE00<sub>H</sub>+i\*4)

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>INSEL7</b>				<b>INSEL6</b>				<b>INSEL5</b>				<b>INSEL4</b>			
	rw			rw				rw				rw			rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>INSEL3</b>				<b>INSEL2</b>				<b>INSEL1</b>				<b>INSEL0</b>			

Field	Bits	Type	Description
<b>INSELj (j=0)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li>1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li>2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>A<sub>H</sub> <b>SAUL8</b>, Input signal is DSADC_SAUL8</li> <li>B<sub>H</sub> <b>SBLL8</b>, Input signal is DSADC_SBLL8</li> <li>C<sub>H</sub> <b>SAUL9</b>, Input signal is DSADC_SAUL9</li> <li>D<sub>H</sub> <b>SBLL9</b>, Input signal is DSADC_SBLL9</li> <li>E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=1)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL9</b>, Input signal is DSADC_SAUL9  <math>B_H</math> <b>SBLL9</b>, Input signal is DSADC_SBLL9  <math>C_H</math> <b>SAUL8</b>, Input signal is DSADC_SAUL8  <math>D_H</math> <b>SBLL8</b>, Input signal is DSADC_SBLL8  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>
<b>INSELj (j=2)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL10</b>, Input signal is DSADC_SAUL10  <math>B_H</math> <b>SBLL10</b>, Input signal is DSADC_SBLL10  <math>C_H</math> <b>SAUL11</b>, Input signal is DSADC_SAUL11  <math>D_H</math> <b>SBLL11</b>, Input signal is DSADC_SBLL11  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=3)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL11</b>, Input signal is DSADC_SAUL11  <math>B_H</math> <b>SBLL11</b>, Input signal is DSADC_SBLL11  <math>C_H</math> <b>SAUL10</b>, Input signal is DSADC_SAUL10  <math>D_H</math> <b>SBLL10</b>, Input signal is DSADC_SBLL10  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>
<b>INSELj (j=4)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0  <math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1  <math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>A_H</math> <b>SAUL12</b>, Input signal is DSADC_SAUL12  <math>B_H</math> <b>SBLL12</b>, Input signal is DSADC_SBLL12  <math>C_H</math> <b>SAUL13</b>, Input signal is DSADC_SAUL13  <math>D_H</math> <b>SBLL13</b>, Input signal is DSADC_SBLL13  <math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11         </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=5)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li>1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li>2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>A<sub>H</sub> <b>SAUL13</b>, Input signal is DSADC_SAUL13</li> <li>B<sub>H</sub> <b>SBLL13</b>, Input signal is DSADC_SBLL13</li> <li>C<sub>H</sub> <b>SAUL12</b>, Input signal is DSADC_SAUL12</li> <li>D<sub>H</sub> <b>SBLL12</b>, Input signal is DSADC_SBLL12</li> <li>E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>
<b>INSELj (j=6)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li>1<sub>H</sub> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li>2<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>3<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>4<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>5<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>6<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>7<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>8<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>9<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>A<sub>H</sub> <b>SAUL0</b>, Input signal is DSADC_SAUL0</li> <li>B<sub>H</sub> <b>SBLL0</b>, Input signal is DSADC_SBLL0</li> <li>C<sub>H</sub> <b>SAUL1</b>, Input signal is DSADC_SAUL1</li> <li>D<sub>H</sub> <b>SBLL1</b>, Input signal is DSADC_SBLL1</li> <li>E<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>F<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=7)</b>	$4^*j+3:4^*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>SRM0</b>, Input signal is DSADC_SRM0</li> <li><math>1_H</math> <b>SRM1</b>, Input signal is DSADC_SRM1</li> <li><math>2_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li><math>3_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li><math>4_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li><math>5_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li><math>6_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li><math>7_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li><math>8_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li><math>9_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li><math>A_H</math> <b>SAUL1</b>, Input signal is DSADC_SAUL1</li> <li><math>B_H</math> <b>SBLL1</b>, Input signal is DSADC_SBLL1</li> <li><math>C_H</math> <b>SAULO</b>, Input signal is DSADC_SAULO</li> <li><math>D_H</math> <b>SBLL0</b>, Input signal is DSADC_SBLL0</li> <li><math>E_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li><math>F_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11</li> </ul>

**GTM\_DSADCINSELi (i=3)**

DSADC Input Select i Register

(09FE00<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INSEL7				INSEL6				INSEL5				INSEL4			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INSEL3				INSEL2				INSEL1				INSEL0			

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSEL<sub>j</sub> (j=0)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADC<sub>n</sub> GTM connection</b></p> <p>This bit field defines which DSADC<sub>n</sub> output is connected if the channel input mux is configured as DSADC input for TIM<sub>i</sub> channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>1<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>2<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>3<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>4<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>5<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>6<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>7<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>8<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>9<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li>A<sub>H</sub> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li>B<sub>H</sub> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li>C<sub>H</sub> <b>SAUL2</b>, Input signal is DSADC_SAUL2</li> <li>D<sub>H</sub> <b>SBLL2</b>, Input signal is DSADC_SBLL2</li> <li>E<sub>H</sub> <b>SAUL3</b>, Input signal is DSADC_SAUL3</li> <li>F<sub>H</sub> <b>SBLL3</b>, Input signal is DSADC_SBLL3</li> </ul>
<b>INSEL<sub>j</sub> (j=1)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADC<sub>n</sub> GTM connection</b></p> <p>This bit field defines which DSADC<sub>n</sub> output is connected if the channel input mux is configured as DSADC input for TIM<sub>i</sub> channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>1<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>2<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>3<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>4<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>5<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>6<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>7<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>8<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>9<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li>A<sub>H</sub> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li>B<sub>H</sub> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li>C<sub>H</sub> <b>SAUL3</b>, Input signal is DSADC_SAUL3</li> <li>D<sub>H</sub> <b>SBLL3</b>, Input signal is DSADC_SBLL3</li> <li>E<sub>H</sub> <b>SAUL2</b>, Input signal is DSADC_SAUL2</li> <li>F<sub>H</sub> <b>SBLL2</b>, Input signal is DSADC_SBLL2</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=2)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li><math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li><math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li><math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li><math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li><math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li><math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li><math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li><math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li><math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li><math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li><math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li><math>C_H</math> <b>SAUL4</b>, Input signal is DSADC_SAUL4</li> <li><math>D_H</math> <b>SBLL4</b>, Input signal is DSADC_SBLL4</li> <li><math>E_H</math> <b>SAUL5</b>, Input signal is DSADC_SAUL5</li> <li><math>F_H</math> <b>SBLL5</b>, Input signal is DSADC_SBLL5</li> </ul>
<b>INSELj (j=3)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li><math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li><math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li><math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li><math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li><math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li><math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li><math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li><math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li><math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li><math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li><math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li><math>C_H</math> <b>SAUL5</b>, Input signal is DSADC_SAUL5</li> <li><math>D_H</math> <b>SBLL5</b>, Input signal is DSADC_SBLL5</li> <li><math>E_H</math> <b>SAUL4</b>, Input signal is DSADC_SAUL4</li> <li><math>F_H</math> <b>SBLL4</b>, Input signal is DSADC_SBLL4</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=4)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>D_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6  <math>E_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>F_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7         </p>
<b>INSELj (j=5)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>D_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7  <math>E_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>F_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6         </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=6)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL8</b>, Input signal is DSADC_SAUL8  <math>D_H</math> <b>SBLL8</b>, Input signal is DSADC_SBLL8  <math>E_H</math> <b>SAUL9</b>, Input signal is DSADC_SAUL9  <math>F_H</math> <b>SBLL9</b>, Input signal is DSADC_SBLL9         </p>
<b>INSELj (j=7)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL9</b>, Input signal is DSADC_SAUL9  <math>D_H</math> <b>SBLL9</b>, Input signal is DSADC_SBLL9  <math>E_H</math> <b>SAUL8</b>, Input signal is DSADC_SAUL8  <math>F_H</math> <b>SBLL8</b>, Input signal is DSADC_SBLL8         </p>

## Generic Timer Module (GTM)

## GTM\_DSADCINSELi (i=4)

## DSADC Input Select i Register

(09FE00<sub>H</sub>+i\*4)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INSEL7				INSEL6				INSEL5				INSEL4			
rw					rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INSEL3				INSEL2				INSEL1				INSEL0			
rw					rw				rw				rw		

Field	Bits	Type	Description
INSELj (j=0)	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2      1<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3      2<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4      3<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5      4<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6      5<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7      6<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8      7<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9      8<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10      9<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11      A<sub>H</sub> <b>SRM12</b>, Input signal is DSADC_SRM12      B<sub>H</sub> <b>SRM13</b>, Input signal is DSADC_SRM13      C<sub>H</sub> <b>SAUL10</b>, Input signal is DSADC_SAUL10      D<sub>H</sub> <b>SBLL10</b>, Input signal is DSADC_SBLL10      E<sub>H</sub> <b>SAUL11</b>, Input signal is DSADC_SAUL11      F<sub>H</sub> <b>SBLL11</b>, Input signal is DSADC_SBLL11   </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=1)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>1<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>2<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>3<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>4<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>5<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>6<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>7<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>8<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>9<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li>A<sub>H</sub> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li>B<sub>H</sub> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li>C<sub>H</sub> <b>SAUL11</b>, Input signal is DSADC_SAUL11</li> <li>D<sub>H</sub> <b>SBLL11</b>, Input signal is DSADC_SBLL11</li> <li>E<sub>H</sub> <b>SAUL10</b>, Input signal is DSADC_SAUL10</li> <li>F<sub>H</sub> <b>SBLL10</b>, Input signal is DSADC_SBLL10</li> </ul>
<b>INSELj (j=2)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>1<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>2<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>3<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>4<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>5<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>6<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>7<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>8<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>9<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li>A<sub>H</sub> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li>B<sub>H</sub> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li>C<sub>H</sub> <b>SAUL12</b>, Input signal is DSADC_SAUL12</li> <li>D<sub>H</sub> <b>SBLL12</b>, Input signal is DSADC_SBLL12</li> <li>E<sub>H</sub> <b>SAUL13</b>, Input signal is DSADC_SAUL13</li> <li>F<sub>H</sub> <b>SBLL13</b>, Input signal is DSADC_SBLL13</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=3)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL13</b>, Input signal is DSADC_SAUL13  <math>D_H</math> <b>SBLL13</b>, Input signal is DSADC_SBLL13  <math>E_H</math> <b>SAUL12</b>, Input signal is DSADC_SAUL12  <math>F_H</math> <b>SBLL12</b>, Input signal is DSADC_SBLL12         </p>
<b>INSELj (j=4)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL0</b>, Input signal is DSADC_SAUL0  <math>D_H</math> <b>SBLL0</b>, Input signal is DSADC_SBLL0  <math>E_H</math> <b>SAUL1</b>, Input signal is DSADC_SAUL1  <math>F_H</math> <b>SBLL1</b>, Input signal is DSADC_SBLL1         </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=5)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL1</b>, Input signal is DSADC_SAUL1  <math>D_H</math> <b>SBLL1</b>, Input signal is DSADC_SBLL1  <math>E_H</math> <b>SAUL0</b>, Input signal is DSADC_SAUL0  <math>F_H</math> <b>SBLL0</b>, Input signal is DSADC_SBLL0       </p>
<b>INSELj (j=6)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL2</b>, Input signal is DSADC_SAUL2  <math>D_H</math> <b>SBLL2</b>, Input signal is DSADC_SBLL2  <math>E_H</math> <b>SAUL3</b>, Input signal is DSADC_SAUL3  <math>F_H</math> <b>SBLL3</b>, Input signal is DSADC_SBLL3       </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=7)</b>	$4^*j+3:4^*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li><math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li><math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li><math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li><math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li><math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li><math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li><math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li><math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li><math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li><math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li><math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li><math>C_H</math> <b>SAUL3</b>, Input signal is DSADC_SAUL3</li> <li><math>D_H</math> <b>SBLL3</b>, Input signal is DSADC_SBLL3</li> <li><math>E_H</math> <b>SAUL2</b>, Input signal is DSADC_SAUL2</li> <li><math>F_H</math> <b>SBLL2</b>, Input signal is DSADC_SBLL2</li> </ul>

**GTM\_DSADCINSELi (i=5)****DSADC Input Select i Register****(09FE00<sub>H</sub>+i\*4)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>INSEL7</b>				<b>INSEL6</b>				<b>INSEL5</b>				<b>INSEL4</b>			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>INSEL3</b>				<b>INSEL2</b>				<b>INSEL1</b>				<b>INSELO</b>			
rw				rw				rw				rw			

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSEL<sub>j</sub> (j=0)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADC<sub>n</sub> GTM connection</b></p> <p>This bit field defines which DSADC<sub>n</sub> output is connected if the channel input mux is configured as DSADC input for TIM<sub>i</sub> channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>1<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>2<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>3<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>4<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>5<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>6<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>7<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>8<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>9<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li>A<sub>H</sub> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li>B<sub>H</sub> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li>C<sub>H</sub> <b>SAUL4</b>, Input signal is DSADC_SAUL4</li> <li>D<sub>H</sub> <b>SBLL4</b>, Input signal is DSADC_SBLL4</li> <li>E<sub>H</sub> <b>SAUL5</b>, Input signal is DSADC_SAUL5</li> <li>F<sub>H</sub> <b>SBLL5</b>, Input signal is DSADC_SBLL5</li> </ul>
<b>INSEL<sub>j</sub> (j=1)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADC<sub>n</sub> GTM connection</b></p> <p>This bit field defines which DSADC<sub>n</sub> output is connected if the channel input mux is configured as DSADC input for TIM<sub>i</sub> channel j.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>SRM2</b>, Input signal is DSADC_SRM2</li> <li>1<sub>H</sub> <b>SRM3</b>, Input signal is DSADC_SRM3</li> <li>2<sub>H</sub> <b>SRM4</b>, Input signal is DSADC_SRM4</li> <li>3<sub>H</sub> <b>SRM5</b>, Input signal is DSADC_SRM5</li> <li>4<sub>H</sub> <b>SRM6</b>, Input signal is DSADC_SRM6</li> <li>5<sub>H</sub> <b>SRM7</b>, Input signal is DSADC_SRM7</li> <li>6<sub>H</sub> <b>SRM8</b>, Input signal is DSADC_SRM8</li> <li>7<sub>H</sub> <b>SRM9</b>, Input signal is DSADC_SRM9</li> <li>8<sub>H</sub> <b>SRM10</b>, Input signal is DSADC_SRM10</li> <li>9<sub>H</sub> <b>SRM11</b>, Input signal is DSADC_SRM11</li> <li>A<sub>H</sub> <b>SRM12</b>, Input signal is DSADC_SRM12</li> <li>B<sub>H</sub> <b>SRM13</b>, Input signal is DSADC_SRM13</li> <li>C<sub>H</sub> <b>SAUL5</b>, Input signal is DSADC_SAUL5</li> <li>D<sub>H</sub> <b>SBLL5</b>, Input signal is DSADC_SBLL5</li> <li>E<sub>H</sub> <b>SAUL4</b>, Input signal is DSADC_SAUL4</li> <li>F<sub>H</sub> <b>SBLL4</b>, Input signal is DSADC_SBLL4</li> </ul>

**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>INSELj (j=2)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>D_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6  <math>E_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>F_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7         </p>
<b>INSELj (j=3)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL7</b>, Input signal is DSADC_SAUL7  <math>D_H</math> <b>SBLL7</b>, Input signal is DSADC_SBLL7  <math>E_H</math> <b>SAUL6</b>, Input signal is DSADC_SAUL6  <math>F_H</math> <b>SBLL6</b>, Input signal is DSADC_SBLL6         </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=4)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL8</b>, Input signal is DSADC_SAUL8  <math>D_H</math> <b>SBLL8</b>, Input signal is DSADC_SBLL8  <math>E_H</math> <b>SAUL9</b>, Input signal is DSADC_SAUL9  <math>F_H</math> <b>SBLL9</b>, Input signal is DSADC_SBLL9         </p>
<b>INSELj (j=5)</b>	$4*j+3:4*j$	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL9</b>, Input signal is DSADC_SAUL9  <math>D_H</math> <b>SBLL9</b>, Input signal is DSADC_SBLL9  <math>E_H</math> <b>SAUL8</b>, Input signal is DSADC_SAUL8  <math>F_H</math> <b>SBLL8</b>, Input signal is DSADC_SBLL8         </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>INSELj (j=6)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL10</b>, Input signal is DSADC_SAUL10  <math>D_H</math> <b>SBLL10</b>, Input signal is DSADC_SBLL10  <math>E_H</math> <b>SAUL11</b>, Input signal is DSADC_SAUL11  <math>F_H</math> <b>SBLL11</b>, Input signal is DSADC_SBLL11         </p>
<b>INSELj (j=7)</b>	4*j+3:4*j	rw	<p><b>In Selection for DSADCn GTM connection</b></p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p> <math>0_H</math> <b>SRM2</b>, Input signal is DSADC_SRM2  <math>1_H</math> <b>SRM3</b>, Input signal is DSADC_SRM3  <math>2_H</math> <b>SRM4</b>, Input signal is DSADC_SRM4  <math>3_H</math> <b>SRM5</b>, Input signal is DSADC_SRM5  <math>4_H</math> <b>SRM6</b>, Input signal is DSADC_SRM6  <math>5_H</math> <b>SRM7</b>, Input signal is DSADC_SRM7  <math>6_H</math> <b>SRM8</b>, Input signal is DSADC_SRM8  <math>7_H</math> <b>SRM9</b>, Input signal is DSADC_SRM9  <math>8_H</math> <b>SRM10</b>, Input signal is DSADC_SRM10  <math>9_H</math> <b>SRM11</b>, Input signal is DSADC_SRM11  <math>A_H</math> <b>SRM12</b>, Input signal is DSADC_SRM12  <math>B_H</math> <b>SRM13</b>, Input signal is DSADC_SRM13  <math>C_H</math> <b>SAUL11</b>, Input signal is DSADC_SAUL11  <math>D_H</math> <b>SBLL11</b>, Input signal is DSADC_SBLL11  <math>E_H</math> <b>SAUL10</b>, Input signal is DSADC_SAUL10  <math>F_H</math> <b>SBLL10</b>, Input signal is DSADC_SBLL10         </p>

## Generic Timer Module (GTM)

## 26.3.7 GTM to EDSADC Connections

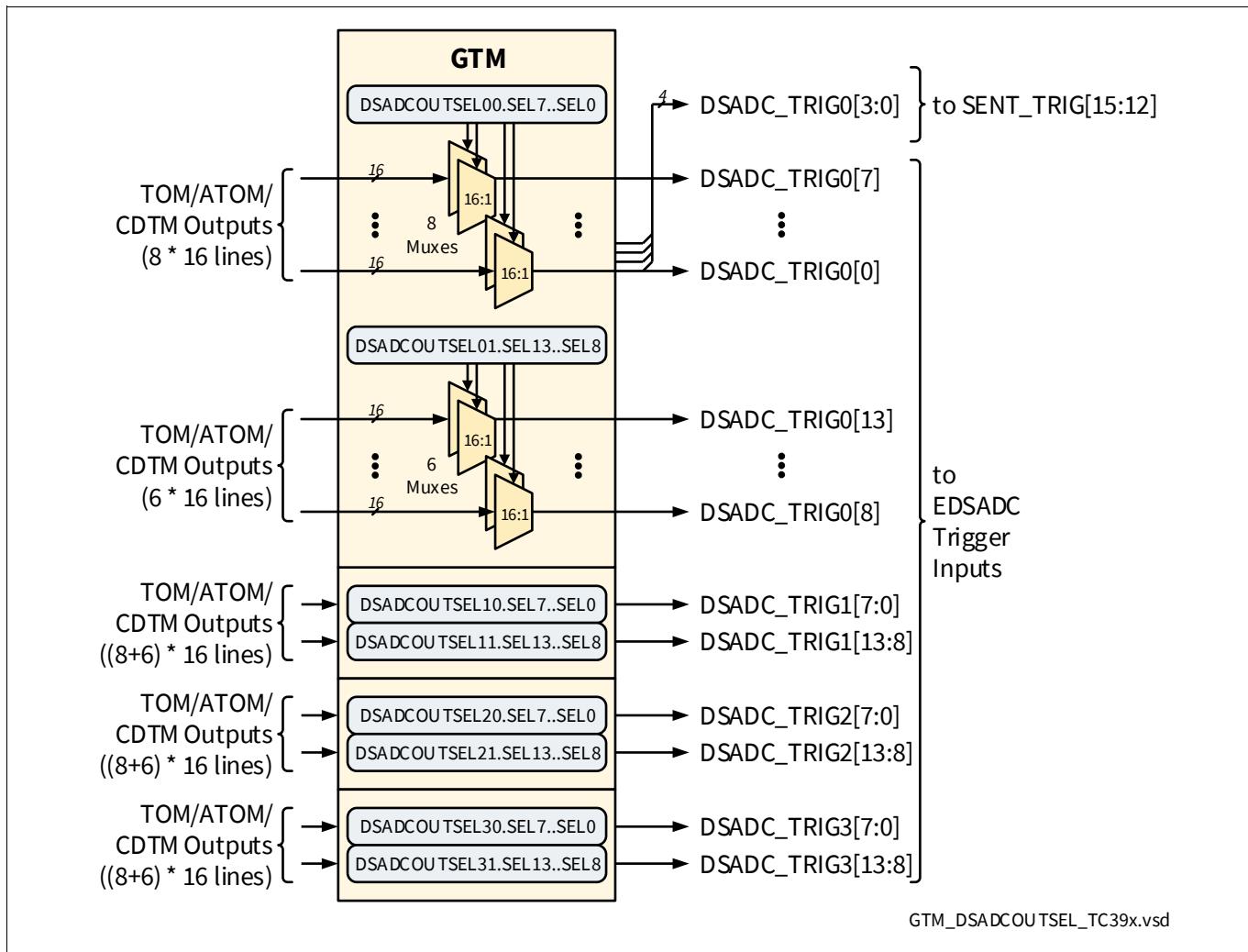


Figure 22 GTM to EDSADC Connections Overview

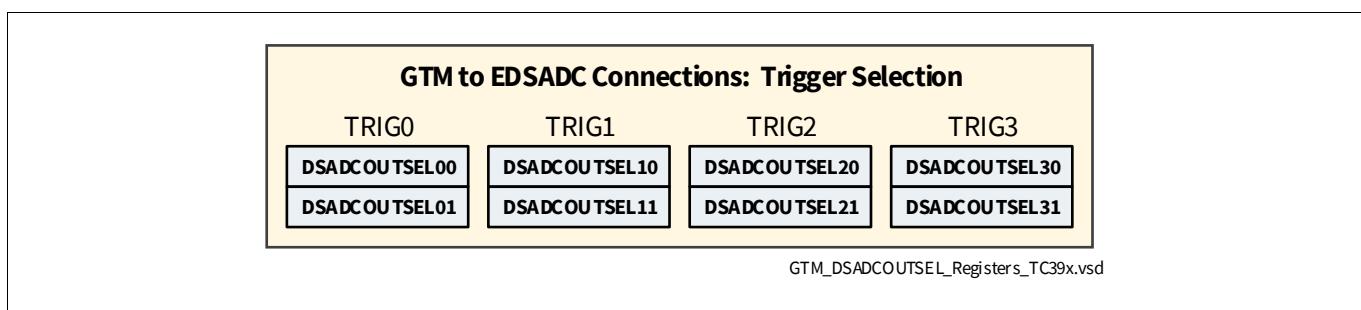


Figure 23 GTM to EDSADC Connections Registers Overview

Table 336 GTM to EDSADC Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
DSADCOUTSEL00	DSADC Output Select 00 Register (i=0)	SEL0..SEL7	<a href="#">Page 369</a>
DSADCOUTSEL01	DSADC Output Select 01 Register (i=0)	SEL8..SEL13	<a href="#">Page 370</a>
DSADCOUTSEL10	DSADC Output Select 10 Register (i=1)	SEL0..SEL7	<a href="#">Page 371</a>

**Generic Timer Module (GTM)****Table 336 GTM to EDSADC Connections Registers Overview (cont'd)**

Register	Long Name	Selection Bitfields	Page
DSADCOUTSEL11	DSADC Output Select 11 Register (i=1)	SEL8..SEL13	<a href="#">Page 372</a>
DSADCOUTSEL20	DSADC Output Select 20 Register (i=2)	SEL0..SEL7	<a href="#">Page 373</a>
DSADCOUTSEL21	DSADC Output Select 21 Register (i=2)	SEL8..SEL13	<a href="#">Page 374</a>
DSADCOUTSEL30	DSADC Output Select 30 Register (i=3)	SEL0..SEL7	<a href="#">Page 375</a>
DSADCOUTSEL31	DSADC Output Select 31 Register (i=3)	SEL8..SEL13	<a href="#">Page 376</a>

**Table 337 GTM to EDSADC Connections Overview**

Signal	SELi	EDSADC/SENT Trigger Inputs			
		x = 0	x = 1	x = 2	x = 3
DSADC_TRIGx_0	SEL0	ITR0A SENT: TRIG12	ITR0B	ITR0M	ITR0N
DSADC_TRIGx_1	SEL1	ITR1A SENT: TRIG13	ITR1B	ITR1M	ITR1N
DSADC_TRIGx_2	SEL2	ITR2A SENT: TRIG14	ITR2B	ITR2M	ITR2N
DSADC_TRIGx_3	SEL3	ITR3A SENT: TRIG15	ITR3B	ITR3M	ITR3N
DSADC_TRIGx_4	SEL4	ITR4A	ITR4B	ITR4M	ITR4N
DSADC_TRIGx_5	SEL5	ITR5A	ITR5B	ITR5M	ITR5N
DSADC_TRIGx_6	SEL6	ITR6A	ITR6B	ITR6M	ITR6N
DSADC_TRIGx_7	SEL7	ITR7A	ITR7B	ITR7M	ITR7N
DSADC_TRIGx_8	SEL8	ITR8A	ITR8B	ITR8M	ITR8N
DSADC_TRIGx_9	SEL9	ITR9A	ITR9B	ITR9M	ITR9N
DSADC_TRIGx_10	SEL10	ITR10A	ITR10B	ITR10M	ITR10N
DSADC_TRIGx_11	SEL11	ITR11A	ITR11B	ITR11M	ITR11N
DSADC_TRIGx_12	SEL12	ITR12A	ITR12B	ITR12M	ITR12N
DSADC_TRIGx_13	SEL13	ITR13A	ITR13B	ITR13M	ITR13N

**DSADC Output Select i0 Register****GTM\_DSADCOUTSELi0 (i=0)****DSADC Output Select i0 Register**(09FE20<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw				rw				rw				rw			

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=0-7)</b>	4*x+3:4*x	rw	<p><b>Output Selection for DSADCx GTM connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</li> <li><math>1_H</math> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</li> <li><math>2_H</math> <b>TOM0_13</b>, Output of TOM0, channel 13</li> <li><math>3_H</math> <b>TOM0_14</b>, Output of TOM0, channel 14</li> <li><math>4_H</math> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</li> <li><math>5_H</math> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</li> <li><math>6_H</math> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</li> <li><math>7_H</math> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</li> <li><math>8_H</math> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</li> <li><math>9_H</math> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</li> <li><math>A_H</math> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</li> <li><math>B_H</math> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</li> <li><math>C_H</math> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</li> <li><math>D_H</math> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</li> <li><math>E_H</math> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</li> <li><math>F_H</math> Reserved, do not use</li> </ul>

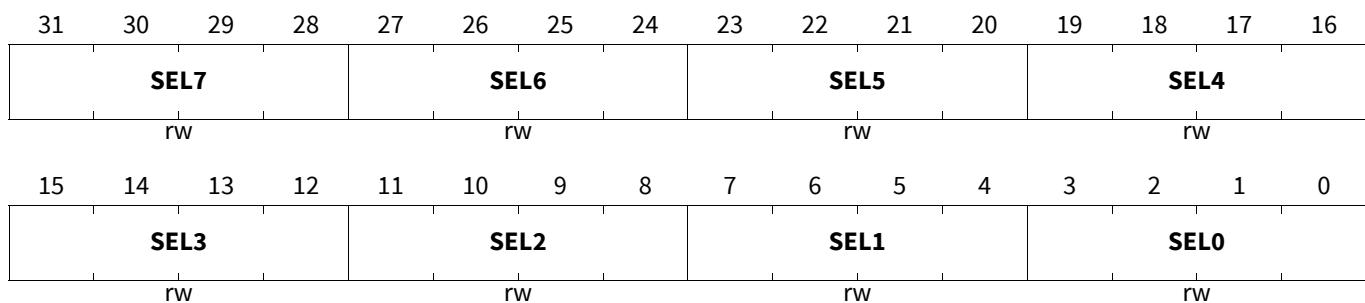
## DSADC Output Select i1 Register

**GTM\_DSADCOUTSELi1 (i=0)****DSADC Output Select i1 Register****(09FE24<sub>H</sub>+i\*8)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				<b>0</b>					<b>SEL13</b>			<b>SEL12</b>			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				<b>SEL11</b>			<b>SEL10</b>		<b>SEL9</b>			<b>SEL8</b>			

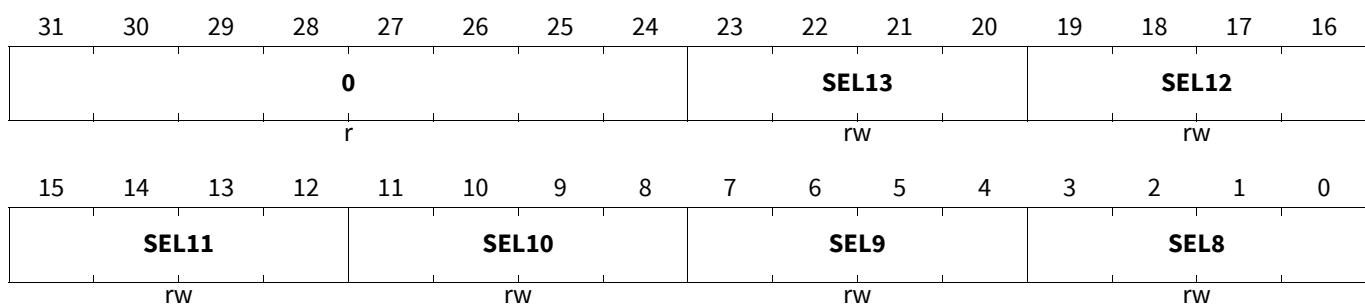
## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=8-13)</b>	4*x-29:4*x-32	rw	<p><b>Output Selection for GTM to DSADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</li> <li>1<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</li> <li>2<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13</li> <li>3<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14</li> <li>4<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</li> <li>5<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</li> <li>6<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</li> <li>7<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</li> <li>8<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</li> <li>9<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</li> <li>A<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</li> <li>B<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</li> <li>C<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</li> <li>D<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</li> <li>E<sub>H</sub> <b>CDTM6_DTM5_2, ATOM6_6</b>, Dead-time output of ATOM6, channel 6</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>0</b>	31:24	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

**GTM\_DSADCOUTSELi0 (i=1)****DSADC Output Select i0 Register**(09FE20<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=0-7)</b>	4*x+3:4*x	rw	<p><b>Output Selection for DSADCx GTM connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</li> <li><math>1_H</math> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</li> <li><math>2_H</math> <b>TOM2_13</b>, Output of TOM2, channel 13</li> <li><math>3_H</math> <b>TOM2_14</b>, Output of TOM2, channel 14</li> <li><math>4_H</math> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</li> <li><math>5_H</math> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</li> <li><math>6_H</math> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</li> <li><math>7_H</math> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</li> <li><math>8_H</math> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</li> <li><math>9_H</math> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</li> <li><math>A_H</math> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</li> <li><math>B_H</math> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</li> <li><math>C_H</math> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</li> <li><math>D_H</math> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</li> <li><math>E_H</math> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</li> <li><math>F_H</math> Reserved, do not use</li> </ul>

**GTM\_DSADCOUTSELi1 (i=1)****DSADC Output Select i1 Register**(09FE24<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=8-13)</b>	4*x-29:4*x-32	rw	<p><b>Output Selection for GTM to DSADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</li> <li>1<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</li> <li>2<sub>H</sub> <b>TOM2_13</b>, Output of TOM2, channel 13</li> <li>3<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14</li> <li>4<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</li> <li>5<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</li> <li>6<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</li> <li>7<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</li> <li>8<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</li> <li>9<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</li> <li>A<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</li> <li>B<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</li> <li>C<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6</li> <li>D<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</li> <li>E<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>0</b>	31:24	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## GTM\_DSADCOUTSELi0 (i=2)

## **DSADC Output Select i0 Register**

(09FE20<sub>H</sub>+i\*8)

**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

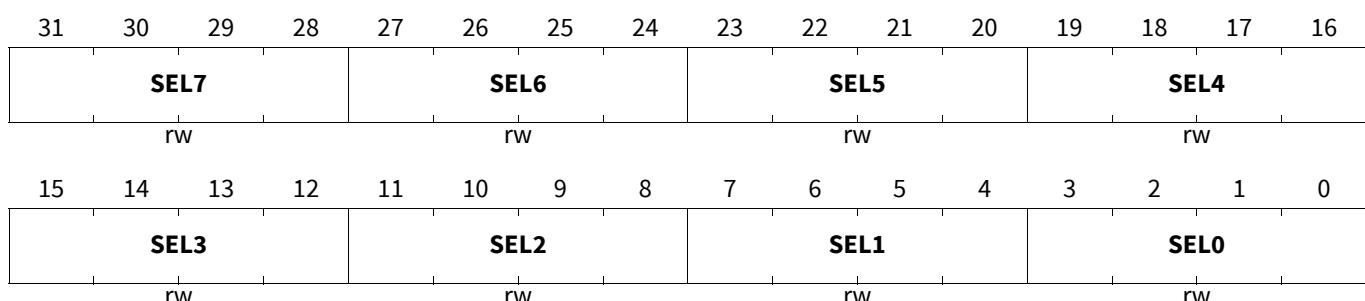
Field	Bits	Type	Description																																
<b>SELx (x=0-7)</b>	4*x+3:4*x	rw	<p><b>Output Selection for DSADCx GTM connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td></tr> <tr><td>1<sub>H</sub></td><td><b>TOM1_14</b>, Output of TOM1, channel 14</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>TOM3_14</b>, Output of TOM3, channel 14</td></tr> <tr><td>4<sub>H</sub></td><td><b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</td></tr> <tr><td>5<sub>H</sub></td><td><b>TOM4_14</b>, Output of TOM4, channel 14</td></tr> <tr><td>6<sub>H</sub></td><td><b>TOM5_7</b>, Output of TOM5, channel 7</td></tr> <tr><td>7<sub>H</sub></td><td><b>TOM5_14</b>, Output of TOM5, channel 14</td></tr> <tr><td>8<sub>H</sub></td><td><b>ATOM7_6</b>, Output of ATOM7, channel 6</td></tr> <tr><td>9<sub>H</sub></td><td><b>ATOM7_7</b>, Output of ATOM7, channel 7</td></tr> <tr><td>A<sub>H</sub></td><td><b>ATOM8_6</b>, Output of ATOM8, channel 6</td></tr> <tr><td>B<sub>H</sub></td><td><b>ATOM8_7</b>, Output of ATOM8, channel 7</td></tr> <tr><td>C<sub>H</sub></td><td><b>ATOM9_6</b>, Output of ATOM9, channel 6</td></tr> <tr><td>D<sub>H</sub></td><td><b>ATOM9_7</b>, Output of ATOM9, channel 7</td></tr> <tr><td>E<sub>H</sub></td><td><b>ATOM11_6</b>, Output of ATOM11, channel 6</td></tr> <tr><td>F<sub>H</sub></td><td>Reserved, do not use</td></tr> </tbody> </table>	0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	1 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14	2 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7	3 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14	4 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7	5 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14	6 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7	7 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14	8 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6	9 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7	A <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6	B <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7	C <sub>H</sub>	<b>ATOM9_6</b> , Output of ATOM9, channel 6	D <sub>H</sub>	<b>ATOM9_7</b> , Output of ATOM9, channel 7	E <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6	F <sub>H</sub>	Reserved, do not use
0 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																																		
1 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14																																		
2 <sub>H</sub>	<b>CDTM3_DTM1_3, TOM3_7</b> , Dead-time output of TOM3, channel 7																																		
3 <sub>H</sub>	<b>TOM3_14</b> , Output of TOM3, channel 14																																		
4 <sub>H</sub>	<b>CDTM4_DTM1_3, TOM4_7</b> , Dead-time output of TOM4, channel 7																																		
5 <sub>H</sub>	<b>TOM4_14</b> , Output of TOM4, channel 14																																		
6 <sub>H</sub>	<b>TOM5_7</b> , Output of TOM5, channel 7																																		
7 <sub>H</sub>	<b>TOM5_14</b> , Output of TOM5, channel 14																																		
8 <sub>H</sub>	<b>ATOM7_6</b> , Output of ATOM7, channel 6																																		
9 <sub>H</sub>	<b>ATOM7_7</b> , Output of ATOM7, channel 7																																		
A <sub>H</sub>	<b>ATOM8_6</b> , Output of ATOM8, channel 6																																		
B <sub>H</sub>	<b>ATOM8_7</b> , Output of ATOM8, channel 7																																		
C <sub>H</sub>	<b>ATOM9_6</b> , Output of ATOM9, channel 6																																		
D <sub>H</sub>	<b>ATOM9_7</b> , Output of ATOM9, channel 7																																		
E <sub>H</sub>	<b>ATOM11_6</b> , Output of ATOM11, channel 6																																		
F <sub>H</sub>	Reserved, do not use																																		

**GTM\_DSADCOUTSELi1 (i=2)****DSADC Output Select i1 Register****(09FE24<sub>H</sub>+i\*8)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				SEL13				SEL12							
r									rw						rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL11				SEL10				SEL9				SEL8			
rw				rw				rw				rw			rw

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=8-13)</b>	4*x-29:4*x-32	rw	<p><b>Output Selection for GTM to DSADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>1<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14</li> <li>2<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</li> <li>3<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14</li> <li>4<sub>H</sub> <b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</li> <li>5<sub>H</sub> <b>TOM4_14</b>, Output of TOM4, channel 14</li> <li>6<sub>H</sub> <b>TOM5_7</b>, Output of TOM5, channel 7</li> <li>7<sub>H</sub> <b>TOM5_14</b>, Output of TOM5, channel 14</li> <li>8<sub>H</sub> <b>ATOM7_6</b>, Output of ATOM7, channel 6</li> <li>9<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7</li> <li>A<sub>H</sub> <b>ATOM8_6</b>, Output of ATOM8, channel 6</li> <li>B<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</li> <li>C<sub>H</sub> <b>ATOM9_6</b>, Output of ATOM9, channel 6</li> <li>D<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7</li> <li>E<sub>H</sub> <b>ATOM11_6</b>, Output of ATOM11, channel 6</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>0</b>	31:24	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

**GTM\_DSADCOUTSELi0 (i=3)****DSADC Output Select i0 Register**(09FE20<sub>H</sub>+i\*8)**Application Reset Value: 0000 0000<sub>H</sub>**

Field	Bits	Type	Description
<b>SELx (x=0-7)</b>	4*x+3:4*x	rw	<p><b>Output Selection for DSADCx GTM connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</li> <li>1<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6</li> <li>2<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7</li> <li>3<sub>H</sub> <b>ATOM11_7</b>, Output of ATOM11, channel 7</li> <li>4<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

## GTM\_DSADCOUTSELi1 (i=3)

## DSADC Output Select i1 Register

(09FE24<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				SEL13				SEL12							
r								rw							rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL11				SEL10				SEL9				SEL8			
rw				rw				rw							rw

Field	Bits	Type	Description
SELx (x=8-13)	4*x-29:4*x-32	rw	<p><b>Output Selection for GTM to DSADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <p>0<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6      1<sub>H</sub> <b>ATOM10_6</b>, Output of ATOM10, channel 6      2<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7      3<sub>H</sub> <b>ATOM11_7</b>, Output of ATOM11, channel 7      4<sub>H</sub> Reserved, do not use      ...      F<sub>H</sub> Reserved, do not use</p>
0	31:24	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

### 26.3.8 EVADC to GTM Connections

The number of FCxBFL and CBFLOUTx signals from the EVADC to the MCS data inputs is product specific. See the following table for the connections available in this device.

**Table 338 MCS Data Input Signal Connections**

MCS Status Input	Input
MCSSTAT0	FC0BFL
MCSSTAT1	FC1BFL
MCSSTAT2	FC2BFL
MCSSTAT3	FC3BFL
MCSSTAT4	FC4BFL
MCSSTAT5	FC5BFL
MCSSTAT6	FC6BFL
MCSSTAT7	FC7BFL
MCSSTAT8	CBFLOUT0
MCSSTAT9	CBFLOUT1
MCSSTAT10	CBFLOUT2
MCSSTAT11	CBFLOUT3
all other	Reserved

## Generic Timer Module (GTM)

## 26.3.9 GTM to EVADC Connections

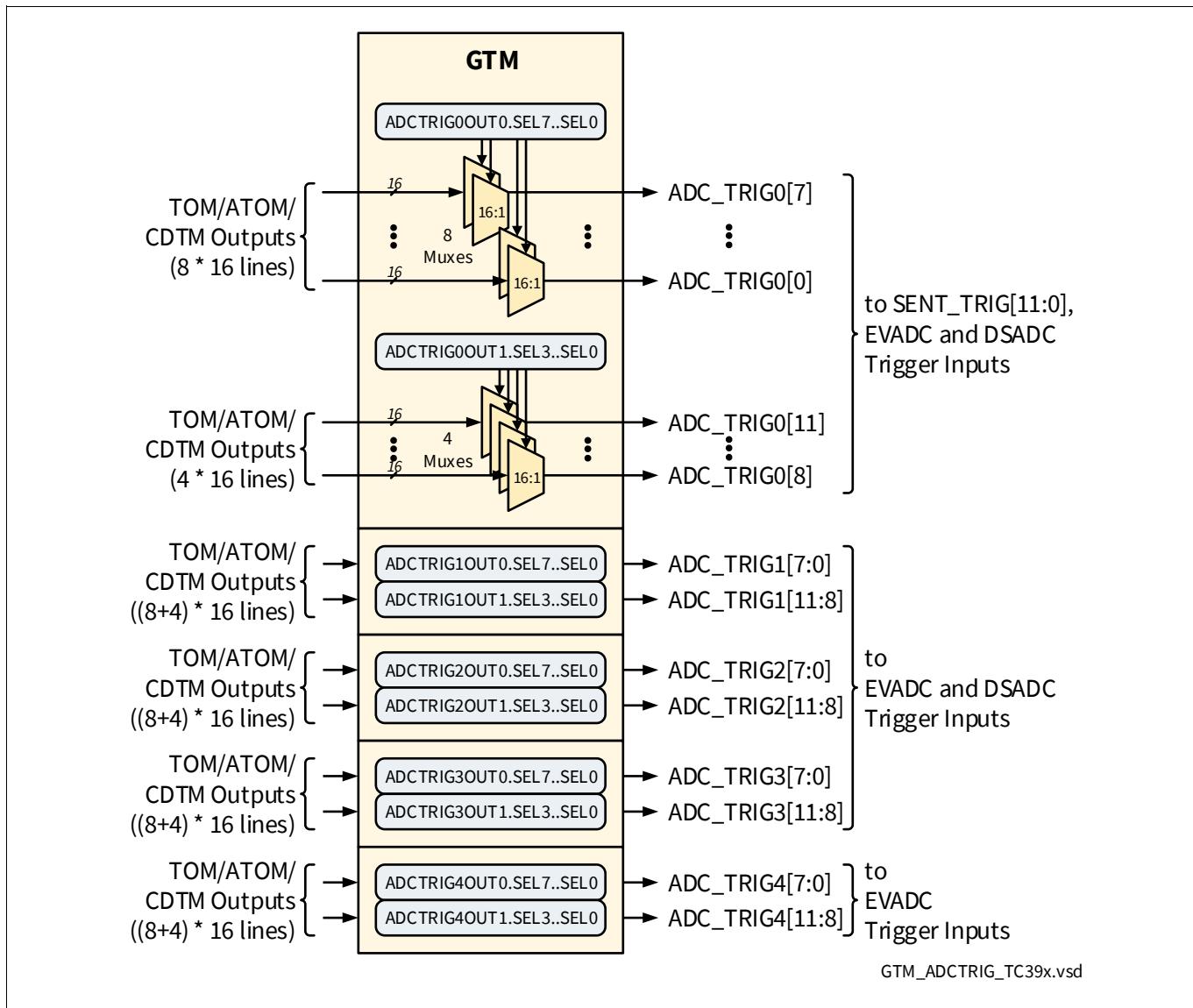


Figure 24 GTM to EVADC Connections Overview

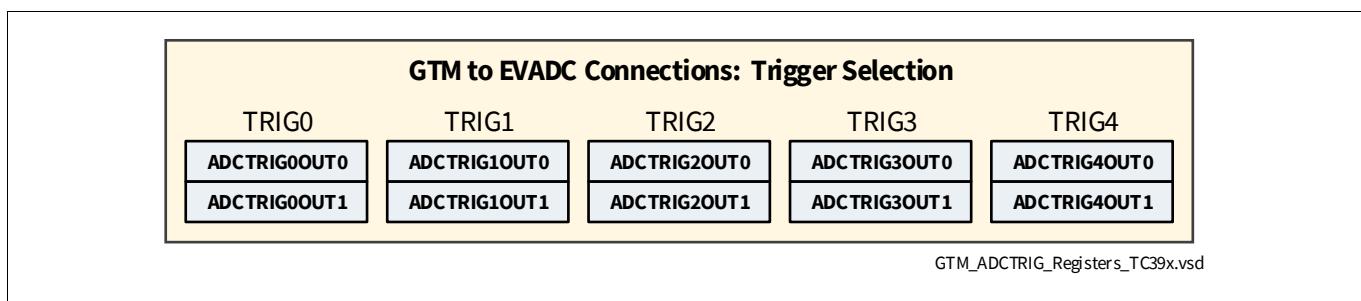


Figure 25 GTM to EVADC Connections Registers Overview

**Generic Timer Module (GTM)****Table 339 GTM to EVADC Connections Registers Overview**

<b>Register</b>	<b>Long Name</b>	<b>Selection Bitfields</b>	<b>Page</b>
ADCTRIG0OUT0	ADC Trigger 0 Output Select 0 Register (i=0)	SEL0..SEL7	<a href="#">Page 380</a>
ADCTRIG0OUT1	ADC Trigger 0 Output Select 1 Register (i=0)	SEL0..SEL3	<a href="#">Page 382</a>
ADCTRIG1OUT0	ADC Trigger 1 Output Select 0 Register (i=1)	SEL0..SEL7	<a href="#">Page 383</a>
ADCTRIG1OUT1	ADC Trigger 1 Output Select 1 Register (i=1)	SEL0..SEL3	<a href="#">Page 386</a>
ADCTRIG2OUT0	ADC Trigger 2 Output Select 0 Register (i=2)	SEL0..SEL7	<a href="#">Page 387</a>
ADCTRIG2OUT1	ADC Trigger 2 Output Select 1 Register (i=2)	SEL0..SEL3	<a href="#">Page 389</a>
ADCTRIG3OUT0	ADC Trigger 3 Output Select 0 Register (i=3)	SEL0..SEL7	<a href="#">Page 390</a>
ADCTRIG3OUT1	ADC Trigger 3 Output Select 1 Register (i=3)	SEL0..SEL3	<a href="#">Page 393</a>
ADCTRIG4OUT0	ADC Trigger 4 Output Select 0 Register (i=4)	SEL0..SEL7	<a href="#">Page 395</a>
ADCTRIG4OUT1	ADC Trigger 4 Output Select 1 Register (i=4)	SEL0..SEL3	<a href="#">Page 397</a>

**Table 340 Connections of ADC\_TRIGx Signals to ADC/SENT Modules**

<b>GTM Trigger Signal</b>	<b>EVADC</b>			<b>EDSADC</b>	<b>SENT</b>
<b>ADC_TRIGO</b>					
ADC_TRIGO_[7:0]	FC[7:0]REQTRI	G[7:0]REQGTA	G[7:0]REQTRI	ITR[7:0]C	TRIG[7:0]
ADC_TRIGO_[11:8]	-	G[11:8]REQGTA	G[11:8]REQTRI	ITR[11:8]C	TRIG[11:8]
<b>ADC_TRIG1</b>					
ADC_TRIG1_[7:0]	FC[7:0]REQTRJ	G[7:0]REQGTB	G[7:0]REQTRJ	ITR[7:0]D	-
ADC_TRIG1_[11:8]	FC[3:2]REQTRL FC[7:6]REQTRL	G[11:8]REQGTB	G[11:8]REQTRJ	ITR[11:8]D	-
<b>ADC_TRIG2</b>					
ADC_TRIG2_-[7:0]	FC[7:0]REQTRK	G[7:0]REQGTK	G[7:0]REQTRK	ITR[7:0]K	-
ADC_TRIG2_[11:8]	FC[3:2]REQTRM FC[7:6]REQTRM	G[11:8]REQGTK	G[11:8]REQTRK	ITR[11:8]K	-
<b>ADC_TRIG3</b>					
ADC_TRIG3_[7:0]	-	G[7:0]REQGTL	G[7:0]REQTRL	ITR[7:0]L	-
ADC_TRIG3_[11:8]	FC[1:0]REQTRL FC[5:4]REQTRL	G[11:8]REQGTL	G[11:8]REQTRL	ITR[11:8]L	-
<b>ADC_TRIG4</b>					
ADC_TRIG4_[7:0]	-	G[7:0]REQGTL	G[7:0]REQTRL	-	-
ADC_TRIG4_[9:8]	FC[1:0]REQTRM	G[9:8]REQGTL	G[9:8]REQTRL	-	-
ADC_TRIG4_[10]	FC4REQTRM FC5REQTRL	G[10]REQGTL	G[10]REQTRL	-	-
ADC_TRIG4_[11]	-	G[11]REQGTL	G[11]REQTRL	-	-

## Generic Timer Module (GTM)

## ADC Trigger i Output Select 0 Register

## GTM\_ADCTRIGiOUT0 (i=0)

ADC Trigger i Output Select 0 Register

(09FE40<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw				rw				rw					rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw				rw				rw					rw		

Field	Bits	Type	Description																																
SELx (x=0-2)	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <table> <tr> <td>0<sub>H</sub></td><td>No trigger</td></tr> <tr> <td>1<sub>H</sub></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr> <td>2<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr> <td>3<sub>H</sub></td><td><b>TOM0_13</b>, Output of TOM0, channel 13</td></tr> <tr> <td>4<sub>H</sub></td><td><b>TOM0_14</b>, Output of TOM0, channel 14</td></tr> <tr> <td>5<sub>H</sub></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr> <td>6<sub>H</sub></td><td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td></tr> <tr> <td>7<sub>H</sub></td><td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td></tr> <tr> <td>8<sub>H</sub></td><td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td></tr> <tr> <td>9<sub>H</sub></td><td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td></tr> <tr> <td>A<sub>H</sub></td><td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td></tr> <tr> <td>B<sub>H</sub></td><td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td></tr> <tr> <td>C<sub>H</sub></td><td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td></tr> <tr> <td>D<sub>H</sub></td><td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td></tr> <tr> <td>E<sub>H</sub></td><td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td></tr> <tr> <td>F<sub>H</sub></td><td><b>TOM2_13</b>, Output of TOM2, channel 13</td></tr> </table>	0 <sub>H</sub>	No trigger	1 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	2 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	3 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13	4 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14	5 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	6 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	7 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	8 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	9 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	A <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	B <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	C <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	D <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	E <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	F <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13
0 <sub>H</sub>	No trigger																																		
1 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																																		
2 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																																		
3 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13																																		
4 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14																																		
5 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																																		
6 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																																		
7 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																																		
8 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																																		
9 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																																		
A <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																																		
B <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6																																		
C <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																																		
D <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																																		
E <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																																		
F <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13																																		

**Generic Timer Module (GTM)**

Field	Bits	Type	Description																																
<b>SELx (x=3-4)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td>No trigger</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>TOM0_13</b>, Output of TOM0, channel 13</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>TOM0_14</b>, Output of TOM0, channel 14</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</td> </tr> <tr> <td>C<sub>H</sub></td> <td><b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</td> </tr> <tr> <td>D<sub>H</sub></td> <td><b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</td> </tr> <tr> <td>E<sub>H</sub></td> <td><b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</td> </tr> <tr> <td>F<sub>H</sub></td> <td><b>TOM2_13</b>, Output of TOM2, channel 13</td> </tr> </tbody> </table>	0 <sub>H</sub>	No trigger	1 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	2 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	3 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13	4 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14	5 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	6 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	7 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	8 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	9 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	A <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	B <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4	C <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5	D <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4	E <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5	F <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13
0 <sub>H</sub>	No trigger																																		
1 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6																																		
2 <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7																																		
3 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13																																		
4 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14																																		
5 <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4																																		
6 <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5																																		
7 <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6																																		
8 <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																																		
9 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																																		
A <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																																		
B <sub>H</sub>	<b>CDTM2_DTM5_0, ATOM2_4</b> , Dead-time output of ATOM2, channel 4																																		
C <sub>H</sub>	<b>CDTM2_DTM5_1, ATOM2_5</b> , Dead-time output of ATOM2, channel 5																																		
D <sub>H</sub>	<b>CDTM3_DTM5_0, ATOM3_4</b> , Dead-time output of ATOM3, channel 4																																		
E <sub>H</sub>	<b>CDTM3_DTM5_1, ATOM3_5</b> , Dead-time output of ATOM3, channel 5																																		
F <sub>H</sub>	<b>TOM2_13</b> , Output of TOM2, channel 13																																		

## Generic Timer Module (GTM)

Field	Bits	Type	Description																																
<b>SELx (x=5-7)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <table> <tbody> <tr><td>0<sub>H</sub></td><td>No trigger</td></tr> <tr><td>1<sub>H</sub></td><td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td></tr> <tr><td>2<sub>H</sub></td><td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td></tr> <tr><td>3<sub>H</sub></td><td><b>TOM0_13</b>, Output of TOM0, channel 13</td></tr> <tr><td>4<sub>H</sub></td><td><b>TOM0_14</b>, Output of TOM0, channel 14</td></tr> <tr><td>5<sub>H</sub></td><td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td></tr> <tr><td>6<sub>H</sub></td><td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td></tr> <tr><td>7<sub>H</sub></td><td><b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</td></tr> <tr><td>8<sub>H</sub></td><td><b>CDTM5_DTM5_1, ATOM5_5</b>, Dead-time output of ATOM5, channel 5</td></tr> <tr><td>9<sub>H</sub></td><td><b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</td></tr> <tr><td>A<sub>H</sub></td><td><b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</td></tr> <tr><td>B<sub>H</sub></td><td><b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</td></tr> <tr><td>C<sub>H</sub></td><td><b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</td></tr> <tr><td>D<sub>H</sub></td><td><b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</td></tr> <tr><td>E<sub>H</sub></td><td><b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</td></tr> <tr><td>F<sub>H</sub></td><td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td></tr> </tbody> </table>	0 <sub>H</sub>	No trigger	1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	2 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	3 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13	4 <sub>H</sub>	<b>TOM0_14</b> , Output of TOM0, channel 14	5 <sub>H</sub>	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	6 <sub>H</sub>	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	7 <sub>H</sub>	<b>CDTM5_DTM5_0, ATOM5_4</b> , Dead-time output of ATOM5, channel 4	8 <sub>H</sub>	<b>CDTM5_DTM5_1, ATOM5_5</b> , Dead-time output of ATOM5, channel 5	9 <sub>H</sub>	<b>CDTM0_DTM1_2, TOM0_6</b> , Dead-time output of TOM0, channel 6	A <sub>H</sub>	<b>CDTM0_DTM1_3, TOM0_7</b> , Dead-time output of TOM0, channel 7	B <sub>H</sub>	<b>CDTM0_DTM5_0, ATOM0_4</b> , Dead-time output of ATOM0, channel 4	C <sub>H</sub>	<b>CDTM0_DTM5_1, ATOM0_5</b> , Dead-time output of ATOM0, channel 5	D <sub>H</sub>	<b>CDTM0_DTM5_2, ATOM0_6</b> , Dead-time output of ATOM0, channel 6	E <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7	F <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7
0 <sub>H</sub>	No trigger																																		
1 <sub>H</sub>	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																																		
2 <sub>H</sub>	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																																		
3 <sub>H</sub>	<b>TOM0_13</b> , Output of TOM0, channel 13																																		
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E <sub>H</sub>	<b>CDTM0_DTM5_3, ATOM0_7</b> , Dead-time output of ATOM0, channel 7																																		
F <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																																		

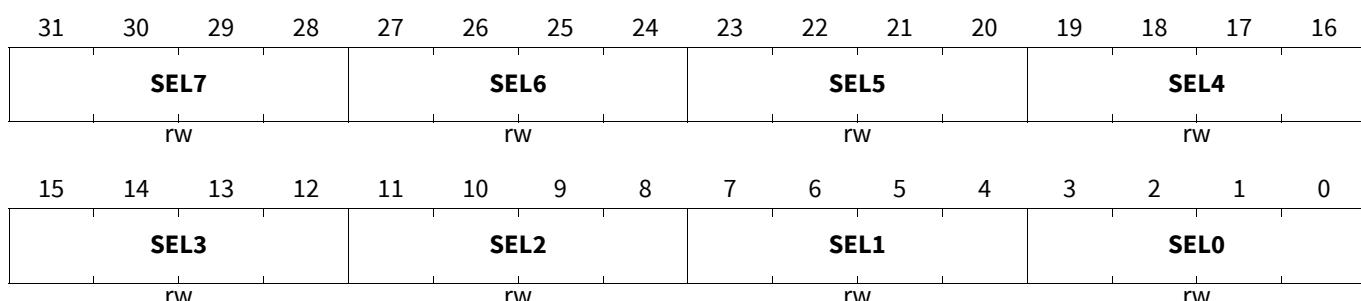
## ADC Trigger i Output Select 1 Register

**GTM\_ADCTRIGiOUT1 (i=0)****ADC Trigger i Output Select 1 Register****(09FE44<sub>H</sub>+i\*8)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
rw				rw				rw				rw			

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=0-3)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</li> <li>2<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</li> <li>3<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13</li> <li>4<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14</li> <li>5<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</li> <li>6<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</li> <li>7<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</li> <li>8<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</li> <li>9<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</li> <li>A<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</li> <li>B<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</li> <li>C<sub>H</sub> <b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</li> <li>D<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</li> <li>E<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</li> <li>F<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15</li> </ul>
<b>0</b>	31:16	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

**GTM\_ADCTRIGiOUT0 (i=1)****ADC Trigger i Output Select 0 Register**(09FE40<sub>H</sub>+i\*8)**Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

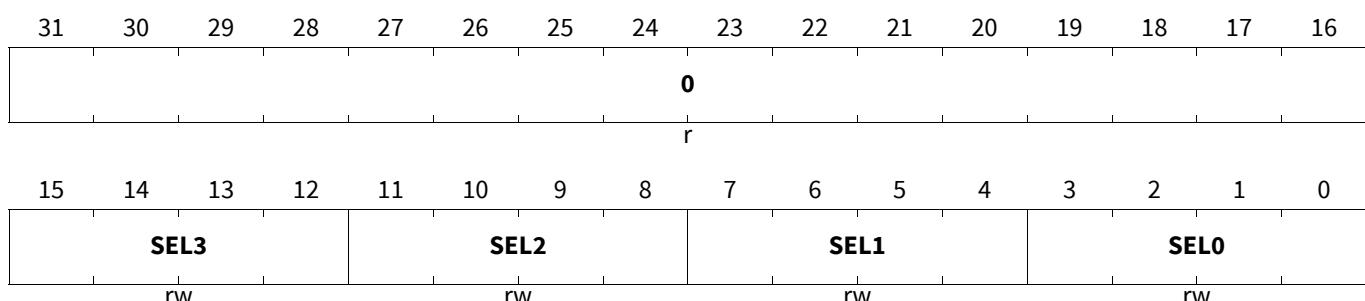
Field	Bits	Type	Description
<b>SELx (x=0-2)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0<sub>H</sub> No trigger      1<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6      2<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7      3<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13      4<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14      5<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4      6<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5      7<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6      8<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7      9<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14      A<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15      B<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      C<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      D<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      E<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7      F<sub>H</sub> <b>TOM3_13</b>, Output of TOM3, channel 13   </p>

**Generic Timer Module (GTM)**

Field	Bits	Type	Description																																
<b>SELx (x=3-4)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <table> <tbody> <tr> <td>0<sub>H</sub></td> <td>No trigger</td> </tr> <tr> <td>1<sub>H</sub></td> <td><b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</td> </tr> <tr> <td>2<sub>H</sub></td> <td><b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</td> </tr> <tr> <td>3<sub>H</sub></td> <td><b>TOM1_13</b>, Output of TOM1, channel 13</td> </tr> <tr> <td>4<sub>H</sub></td> <td><b>TOM1_14</b>, Output of TOM1, channel 14</td> </tr> <tr> <td>5<sub>H</sub></td> <td><b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</td> </tr> <tr> <td>6<sub>H</sub></td> <td><b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</td> </tr> <tr> <td>7<sub>H</sub></td> <td><b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</td> </tr> <tr> <td>8<sub>H</sub></td> <td><b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</td> </tr> <tr> <td>9<sub>H</sub></td> <td><b>TOM1_14</b>, Output of TOM1, channel 14</td> </tr> <tr> <td>A<sub>H</sub></td> <td><b>TOM1_15</b>, Output of TOM1, channel 15</td> </tr> <tr> <td>B<sub>H</sub></td> <td><b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</td> </tr> <tr> <td>C<sub>H</sub></td> <td><b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</td> </tr> <tr> <td>D<sub>H</sub></td> <td><b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</td> </tr> <tr> <td>E<sub>H</sub></td> <td><b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</td> </tr> <tr> <td>F<sub>H</sub></td> <td><b>TOM3_13</b>, Output of TOM3, channel 13</td> </tr> </tbody> </table>	0 <sub>H</sub>	No trigger	1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6	2 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7	3 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13	4 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14	5 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4	6 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5	7 <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6	8 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7	9 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14	A <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15	B <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6	C <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7	D <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6	E <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7	F <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13
0 <sub>H</sub>	No trigger																																		
1 <sub>H</sub>	<b>CDTM1_DTM1_2, TOM1_6</b> , Dead-time output of TOM1, channel 6																																		
2 <sub>H</sub>	<b>CDTM1_DTM1_3, TOM1_7</b> , Dead-time output of TOM1, channel 7																																		
3 <sub>H</sub>	<b>TOM1_13</b> , Output of TOM1, channel 13																																		
4 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14																																		
5 <sub>H</sub>	<b>CDTM1_DTM5_0, ATOM1_4</b> , Dead-time output of ATOM1, channel 4																																		
6 <sub>H</sub>	<b>CDTM1_DTM5_1, ATOM1_5</b> , Dead-time output of ATOM1, channel 5																																		
7 <sub>H</sub>	<b>CDTM1_DTM5_2, ATOM1_6</b> , Dead-time output of ATOM1, channel 6																																		
8 <sub>H</sub>	<b>CDTM1_DTM5_3, ATOM1_7</b> , Dead-time output of ATOM1, channel 7																																		
9 <sub>H</sub>	<b>TOM1_14</b> , Output of TOM1, channel 14																																		
A <sub>H</sub>	<b>TOM1_15</b> , Output of TOM1, channel 15																																		
B <sub>H</sub>	<b>CDTM2_DTM5_2, ATOM2_6</b> , Dead-time output of ATOM2, channel 6																																		
C <sub>H</sub>	<b>CDTM2_DTM5_3, ATOM2_7</b> , Dead-time output of ATOM2, channel 7																																		
D <sub>H</sub>	<b>CDTM3_DTM5_2, ATOM3_6</b> , Dead-time output of ATOM3, channel 6																																		
E <sub>H</sub>	<b>CDTM3_DTM5_3, ATOM3_7</b> , Dead-time output of ATOM3, channel 7																																		
F <sub>H</sub>	<b>TOM3_13</b> , Output of TOM3, channel 13																																		

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=5-7)</b>	$4^*x+3:4^*x$	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0<sub>H</sub> No trigger      1<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14      2<sub>H</sub> <b>TOM2_15</b>, Output of TOM2, channel 15      3<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13      4<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14      5<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6      6<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7      7<sub>H</sub> <b>CDTM5_DTM5_2, ATOM5_6</b>, Dead-time output of ATOM5, channel 6      8<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7      9<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6      A<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7      B<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4      C<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5      D<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6      E<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7      F<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7   </p>

**GTM\_ADCTRIGiOUT1 (i=1)****ADC Trigger i Output Select 1 Register****(09FE44<sub>H</sub>+i\*8)****Application Reset Value: 0000 0000<sub>H</sub>**

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=0-3)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</li> <li>2<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>3<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13</li> <li>4<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14</li> <li>5<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</li> <li>6<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</li> <li>7<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</li> <li>8<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</li> <li>9<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14</li> <li>A<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15</li> <li>B<sub>H</sub> <b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</li> <li>C<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</li> <li>D<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</li> <li>E<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</li> <li>F<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</li> </ul>
0	31:16	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## GTM\_ADCTRIGiOUT0 (i=2)

## **ADC Trigger i Output Select 0 Register**

(09FE40<sub>H</sub>+i\*8)

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
	rw				rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
	rw				rw				rw				rw		

## Generic Timer Module (GTM)

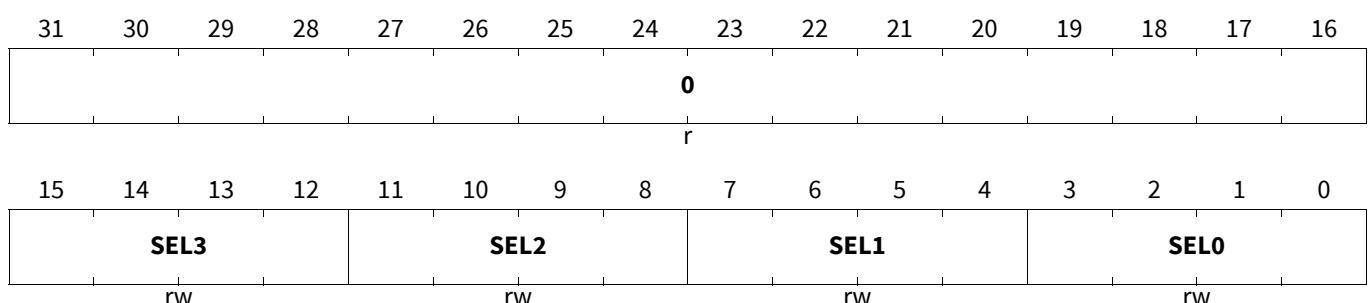
Field	Bits	Type	Description
<b>SELx (x=0-2)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</li> <li>2<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</li> <li>3<sub>H</sub> <b>CDTM0_DTM1_1(_N), TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</li> <li>4<sub>H</sub> <b>CDTM0_DTM1_2(_N), TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</li> <li>5<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</li> <li>6<sub>H</sub> <b>TOM0_11</b>, Output of TOM0, channel 11</li> <li>7<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15</li> <li>8<sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</li> <li>9<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li>A<sub>H</sub> <b>CDTM1_DTM1_1(_N), TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</li> <li>B<sub>H</sub> <b>CDTM1_DTM1_2(_N), TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</li> <li>C<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>D<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li>E<sub>H</sub> <b>TOM1_15</b>, Output of TOM1, channel 15</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>SELx (x=3-4)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3</li> <li>2<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4</li> <li>3<sub>H</sub> <b>CDTM0_DTM1_1(_N), TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5</li> <li>4<sub>H</sub> <b>CDTM0_DTM1_2(_N), TOM0_6_N</b>, Inverted dead-time output of TOM0, channel 6</li> <li>5<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</li> <li>6<sub>H</sub> <b>TOM0_11</b>, Output of TOM0, channel 11</li> <li>7<sub>H</sub> <b>TOM0_15</b>, Output of TOM0, channel 15</li> <li>8<sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3</li> <li>9<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li>A<sub>H</sub> <b>CDTM1_DTM1_1(_N), TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5</li> <li>B<sub>H</sub> <b>CDTM1_DTM1_2(_N), TOM1_6_N</b>, Inverted dead-time output of TOM1, channel 6</li> <li>C<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>D<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li>E<sub>H</sub> <b>TOM1_15</b>, Output of TOM1, channel 15</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=5-7)</b>	$4^*x+3:4^*x$	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0<sub>H</sub> No trigger      1<sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3      2<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4      3<sub>H</sub> <b>CDTM0_DTM1_1(_N), TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5      4<sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3      5<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4      6<sub>H</sub> <b>CDTM1_DTM1_1(_N), TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5      7<sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3      8<sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4      9<sub>H</sub> <b>CDTM2_DTM1_1(_N), TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5      A<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4      B<sub>H</sub> <b>CDTM3_DTM1_1(_N), TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5      C<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7      D<sub>H</sub> <b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4      E<sub>H</sub> <b>CDTM4_DTM1_1(_N), TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5      F<sub>H</sub> <b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7   </p>

**GTM\_ADCTRIGiOUT1 (i=2)**

ADC Trigger i Output Select 1 Register

(09FE44<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=0-3)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <p>0<sub>H</sub> No trigger      1<sub>H</sub> <b>CDTM0_DTM0_3, TOM0_3</b>, Dead-time output of TOM0, channel 3      2<sub>H</sub> <b>CDTM0_DTM1_0, TOM0_4</b>, Dead-time output of TOM0, channel 4      3<sub>H</sub> <b>CDTM0_DTM1_1(_N), TOM0_5_N</b>, Inverted dead-time output of TOM0, channel 5      4<sub>H</sub> <b>CDTM1_DTM0_3, TOM1_3</b>, Dead-time output of TOM1, channel 3      5<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4      6<sub>H</sub> <b>CDTM1_DTM1_1(_N), TOM1_5_N</b>, Inverted dead-time output of TOM1, channel 5      7<sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3      8<sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4      9<sub>H</sub> <b>CDTM2_DTM1_1(_N), TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5      A<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7      B<sub>H</sub> <b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3      C<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4      D<sub>H</sub> <b>CDTM3_DTM1_1(_N), TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5      E<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7      F<sub>H</sub> <b>CDTM4_DTM0_3, ATOM4_3</b>, Dead-time output of TOM4, channel 3   </p>
0	31:16	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

**GTM\_ADCTRIGiOUT0 (i=3)****ADC Trigger i Output Select 0 Register**(09FE40<sub>H</sub>+i\*8)**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
rw				rw				rw					rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
													rw		

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=0-2)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0<sub>H</sub> No trigger</p> <p>1<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</p> <p>2<sub>H</sub> <b>CDTM0_DTM5_1(_N), ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</p> <p>3<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</p> <p>4<sub>H</sub> <b>CDTM1_DTM5_1(_N), ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</p> <p>5<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</p> <p>6<sub>H</sub> <b>CDTM2_DTM5_1(_N), ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</p> <p>7<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</p> <p>8<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</p> <p>9<sub>H</sub> <b>CDTM3_DTM5_1(_N), ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</p> <p>A<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</p> <p>B<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</p> <p>C<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</p> <p>D<sub>H</sub> <b>CDTM4_DTM5_1(_N), ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</p> <p>E<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</p> <p>F<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14</p>

## Generic Timer Module (GTM)

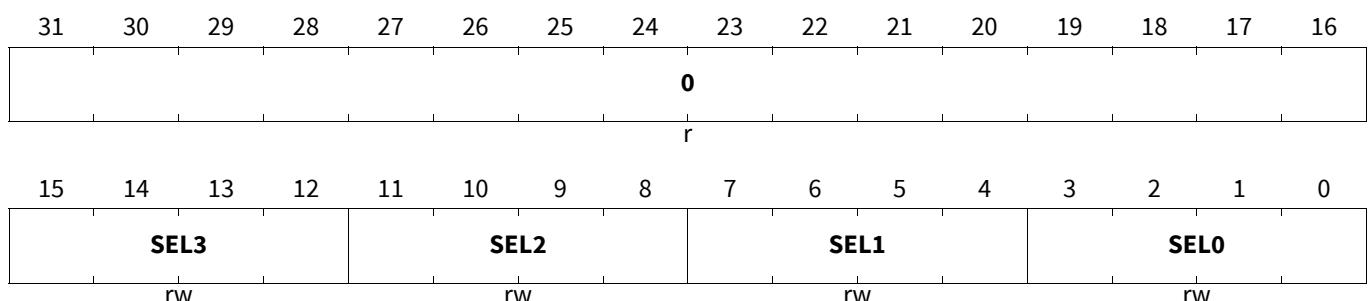
Field	Bits	Type	Description
<b>SELx (x=3-4)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</li> <li>2<sub>H</sub> <b>CDTM0_DTM5_1(_N), ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</li> <li>3<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</li> <li>4<sub>H</sub> <b>CDTM1_DTM5_1(_N), ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</li> <li>5<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li>6<sub>H</sub> <b>CDTM2_DTM5_1(_N), ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</li> <li>7<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</li> <li>8<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</li> <li>9<sub>H</sub> <b>CDTM3_DTM5_1(_N), ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</li> <li>A<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</li> <li>B<sub>H</sub> <b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</li> <li>C<sub>H</sub> <b>CDTM4_DTM5_1(_N), ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</li> <li>D<sub>H</sub> <b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</li> <li>E<sub>H</sub> Reserved, do not use</li> <li>F<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14</li> </ul>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=5-7)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0<sub>H</sub> No trigger      1<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3      2<sub>H</sub> <b>CDTM0_DTM5_1(_N), ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5      3<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3      4<sub>H</sub> <b>CDTM1_DTM5_1(_N), ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5      5<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      6<sub>H</sub> <b>CDTM2_DTM5_1(_N), ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5      7<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3      8<sub>H</sub> <b>CDTM3_DTM5_1(_N), ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5      9<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3      A<sub>H</sub> <b>CDTM4_DTM5_1(_N), ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5      B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3      C<sub>H</sub> <b>CDTM5_DTM5_1(_N), ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5      D<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4      E<sub>H</sub> <b>CDTM6_DTM5_1(_N), ATOM6_5_N</b>, Inverted dead-time output of ATOM6, channel 5      F<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7   </p>

**GTM\_ADCTRIGiOUT1 (i=3)**

ADC Trigger i Output Select 1 Register

(09FE44<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=0-3)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM0_DTM4_3, ATOM0_3</b>, Dead-time output of ATOM0, channel 3</li> <li>2<sub>H</sub> <b>CDTM0_DTM5_1(_N), ATOM0_5_N</b>, Inverted dead-time output of ATOM0, channel 5</li> <li>3<sub>H</sub> <b>CDTM1_DTM4_3, ATOM1_3</b>, Dead-time output of ATOM1, channel 3</li> <li>4<sub>H</sub> <b>CDTM1_DTM5_1(_N), ATOM1_5_N</b>, Inverted dead-time output of ATOM1, channel 5</li> <li>5<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li>6<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</li> <li>7<sub>H</sub> <b>CDTM2_DTM5_1(_N), ATOM2_5_N</b>, Inverted dead-time output of ATOM2, channel 5</li> <li>8<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</li> <li>9<sub>H</sub> <b>CDTM3_DTM4_3, ATOM3_3</b>, Dead-time output of ATOM3, channel 3</li> <li>A<sub>H</sub> <b>CDTM3_DTM5_1(_N), ATOM3_5_N</b>, Inverted dead-time output of ATOM3, channel 5</li> <li>B<sub>H</sub> <b>CDTM4_DTM4_3, ATOM4_3</b>, Dead-time output of ATOM4, channel 3</li> <li>C<sub>H</sub> <b>CDTM4_DTM5_1(_N), ATOM4_5_N</b>, Inverted dead-time output of ATOM4, channel 5</li> <li>D<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</li> <li>E<sub>H</sub> <b>CDTM5_DTM5_1(_N), ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</li> <li>F<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</li> </ul>
<b>0</b>	31:16	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

## GTM\_ADCTRIGiOUT0 (i=4)

ADC Trigger i Output Select 0 Register

(09FE40<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description
SELx (x=0-2)	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0<sub>H</sub> No trigger</p> <p>1<sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</p> <p>2<sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</p> <p>3<sub>H</sub> <b>CDTM2_DTM1_1(_N), TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</p> <p>4<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</p> <p>5<sub>H</sub> <b>TOM2_11</b>, Output of TOM2, channel 11</p> <p>6<sub>H</sub> <b>TOM2_12</b>, Output of TOM2, channel 12</p> <p>7<sub>H</sub> <b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</p> <p>8<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</p> <p>9<sub>H</sub> <b>CDTM3_DTM1_1(_N), TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</p> <p>A<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</p> <p>B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</p> <p>C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</p> <p>D<sub>H</sub> <b>CDTM5_DTM5_1(_N), ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</p> <p>E<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</p> <p>F<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14</p>

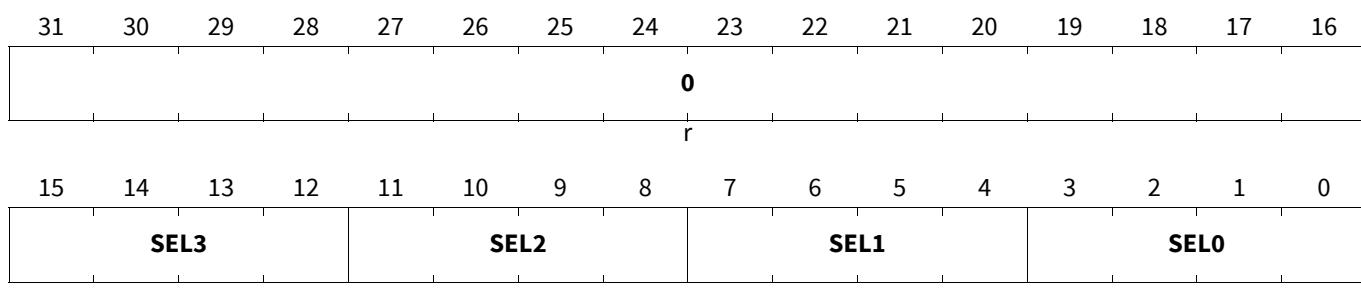
**Generic Timer Module (GTM)**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>SELx (x=3-4)</b>	$4^*x+3:4^*x$	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM2_DTM0_3, TOM2_3</b>, Dead-time output of TOM2, channel 3</li> <li>2<sub>H</sub> <b>CDTM2_DTM1_0, TOM2_4</b>, Dead-time output of TOM2, channel 4</li> <li>3<sub>H</sub> <b>CDTM2_DTM1_1(_N), TOM2_5_N</b>, Inverted dead-time output of TOM2, channel 5</li> <li>4<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</li> <li>5<sub>H</sub> <b>TOM2_11</b>, Output of TOM2, channel 11</li> <li>6<sub>H</sub> <b>TOM2_12</b>, Output of TOM2, channel 12</li> <li>7<sub>H</sub> <b>CDTM3_DTM0_3, TOM3_3</b>, Dead-time output of TOM3, channel 3</li> <li>8<sub>H</sub> <b>CDTM3_DTM1_0, TOM3_4</b>, Dead-time output of TOM3, channel 4</li> <li>9<sub>H</sub> <b>CDTM3_DTM1_1(_N), TOM3_5_N</b>, Inverted dead-time output of TOM3, channel 5</li> <li>A<sub>H</sub> <b>CDTM3_DTM1_3, TOM3_7</b>, Dead-time output of TOM3, channel 7</li> <li>B<sub>H</sub> <b>CDTM5_DTM4_3, ATOM5_3</b>, Dead-time output of ATOM5, channel 3</li> <li>C<sub>H</sub> <b>CDTM5_DTM5_0, ATOM5_4</b>, Dead-time output of ATOM5, channel 4</li> <li>D<sub>H</sub> <b>CDTM5_DTM5_1(_N), ATOM5_5_N</b>, Inverted dead-time output of ATOM5, channel 5</li> <li>E<sub>H</sub> <b>CDTM5_DTM5_3, ATOM5_7</b>, Dead-time output of ATOM5, channel 7</li> <li>F<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14</li> </ul>
<b>SELx (x=5-7)</b>	$4^*x+3:4^*x$	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>TOM4_14</b>, Output of TOM4, channel 14</li> <li>2<sub>H</sub> <b>TOM5_14</b>, Output of TOM5, channel 14</li> <li>3<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5</li> <li>4<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7</li> <li>5<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5</li> <li>6<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</li> <li>7<sub>H</sub> <b>TOM5_5</b>, Output of TOM5, channel 5</li> <li>8<sub>H</sub> <b>TOM5_7</b>, Output of TOM5, channel 7</li> <li>9<sub>H</sub> <b>ATOM9_5</b>, Output of ATOM9, channel 5</li> <li>A<sub>H</sub> <b>ATOM9_7</b>, Output of ATOM9, channel 7</li> <li>B<sub>H</sub> <b>ATOM10_5</b>, Output of ATOM10, channel 5</li> <li>C<sub>H</sub> <b>ATOM10_7</b>, Output of ATOM10, channel 7</li> <li>D<sub>H</sub> <b>ATOM11_5</b>, Output of ATOM11, channel 5</li> <li>E<sub>H</sub> <b>ATOM11_7</b>, Output of ATOM11, channel 7</li> <li>F<sub>H</sub> <b>TOM5_4</b>, Output of TOM5, channel 4</li> </ul>

## Generic Timer Module (GTM)

## GTM\_ADCTRIGiOUT1 (i=4)

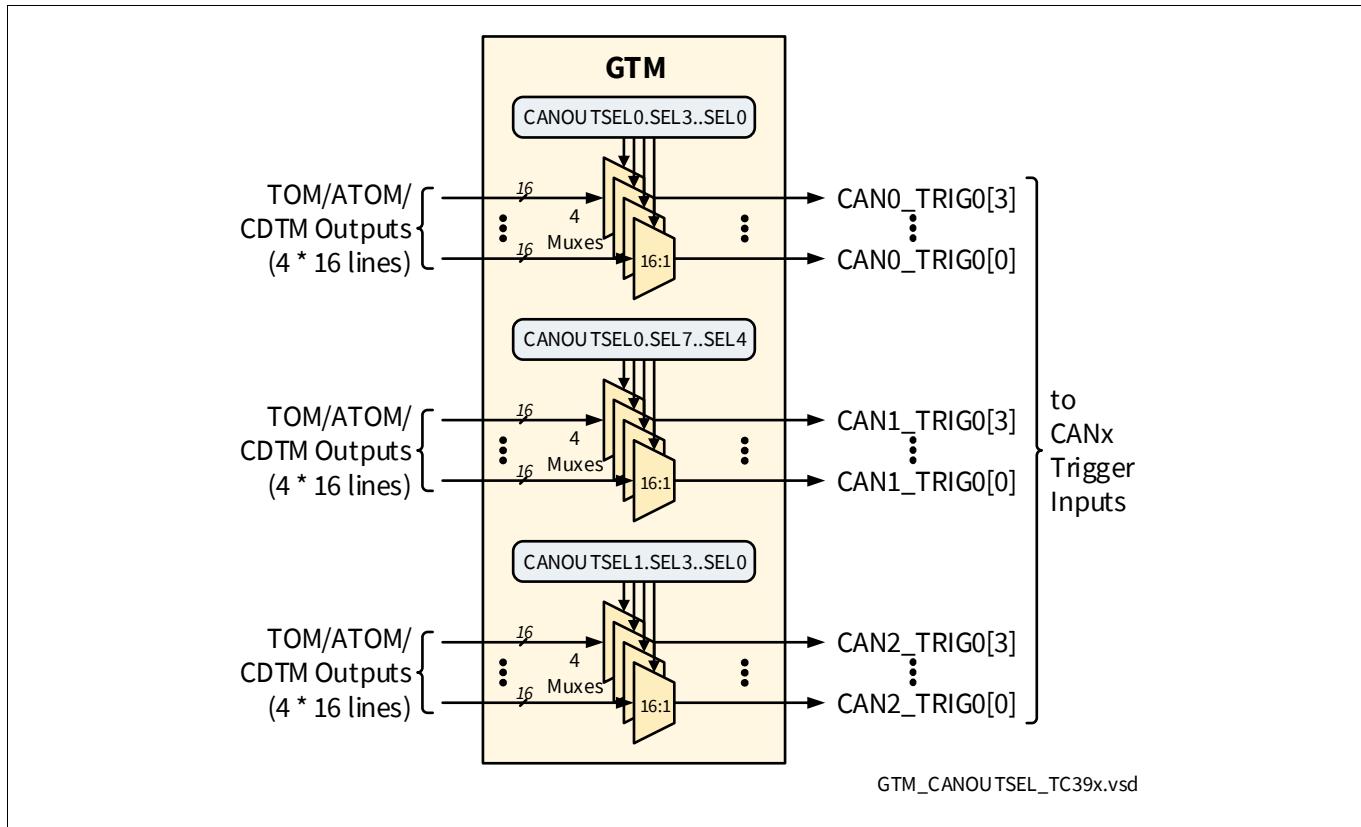
ADC Trigger i Output Select 1 Register

(09FE44<sub>H</sub>+i\*8)Application Reset Value: 0000 0000<sub>H</sub>

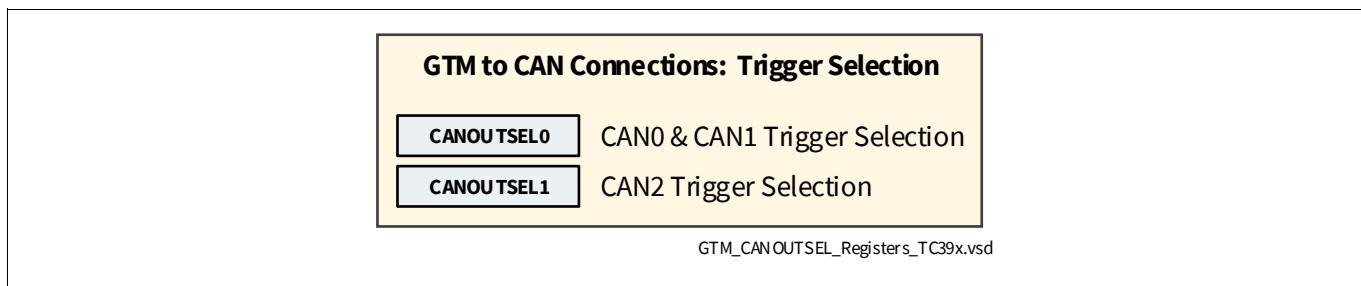
Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	<p><b>Output Selection for GTM to ADCx connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <p>0<sub>H</sub> No trigger</p> <p>1<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14</p> <p>2<sub>H</sub> <b>TOM3_14</b>, Output of TOM3, channel 14</p> <p>3<sub>H</sub> <b>TOM4_14</b>, Output of TOM4, channel 14</p> <p>4<sub>H</sub> <b>CDTM6_DTM5_0, ATOM6_4</b>, Dead-time output of ATOM6, channel 4</p> <p>5<sub>H</sub> <b>CDTM6_DTM5_1(_N), ATOM6_5_N</b>, Inverted dead-time output of ATOM6, channel 5</p> <p>6<sub>H</sub> <b>CDTM6_DTM5_3, ATOM6_7</b>, Dead-time output of ATOM6, channel 7</p> <p>7<sub>H</sub> <b>ATOM7_4</b>, Output of ATOM7, channel 4</p> <p>8<sub>H</sub> <b>ATOM7_5</b>, Output of ATOM7, channel 5</p> <p>9<sub>H</sub> <b>ATOM7_7</b>, Output of ATOM7, channel 7</p> <p>A<sub>H</sub> <b>ATOM8_4</b>, Output of ATOM8, channel 4</p> <p>B<sub>H</sub> <b>ATOM8_5</b>, Output of ATOM8, channel 5</p> <p>C<sub>H</sub> <b>ATOM8_7</b>, Output of ATOM8, channel 7</p> <p>D<sub>H</sub> <b>CDTM4_DTM1_0, TOM4_4</b>, Dead-time output of TOM4, channel 4</p> <p>E<sub>H</sub> <b>CDTM4_DTM1_1(_N), TOM4_5_N</b>, Inverted dead-time output of TOM4, channel 5</p> <p>F<sub>H</sub> <b>CDTM4_DTM1_3, TOM4_7</b>, Dead-time output of TOM4, channel 7</p>
0	31:16	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

### 26.3.10 GTM to CAN/TTCAN Connections



**Figure 26** GTM to CAN/TTCAN Connections Overview



**Figure 27** GTM to CAN/TTCAN Connections Registers Overview

#### CAN0/CAN1 Output Select Register

This register holds the selection for the trigger outputs to the CAN0/CAN1 modules. Bit fields SEL0..3 define the selection for triggers 0..3 for CAN0, while bit fields SEL4..7 define the selection for triggers 0..3 for CAN1.

## Generic Timer Module (GTM)

**GTM\_CANOUTSEL0****CAN0/CAN1 Output Select Register****(09FFDC<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SEL7	rw	SEL6	rw	SEL5	rw	SEL4	rw

SEL3	rw	SEL2	rw	SEL1	rw	SEL0	rw

Field	Bits	Type	Description
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x.</p> <p>0<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4      1<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5      2<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11      3<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12      4<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      5<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      6<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      7<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      8<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6      9<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7      A<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13      B<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14      C<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      D<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      E<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      F<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7       </p>

## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li>1<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</li> <li>2<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li>3<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12</li> <li>4<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</li> <li>5<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</li> <li>6<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</li> <li>7<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li>8<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</li> <li>9<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>A<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13</li> <li>B<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14</li> <li>C<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</li> <li>D<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</li> <li>E<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</li> <li>F<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</li> </ul>
<b>SELx (x=2-3)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li>1<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</li> <li>2<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li>3<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12</li> <li>4<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</li> <li>5<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</li> <li>6<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</li> <li>7<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li>8<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

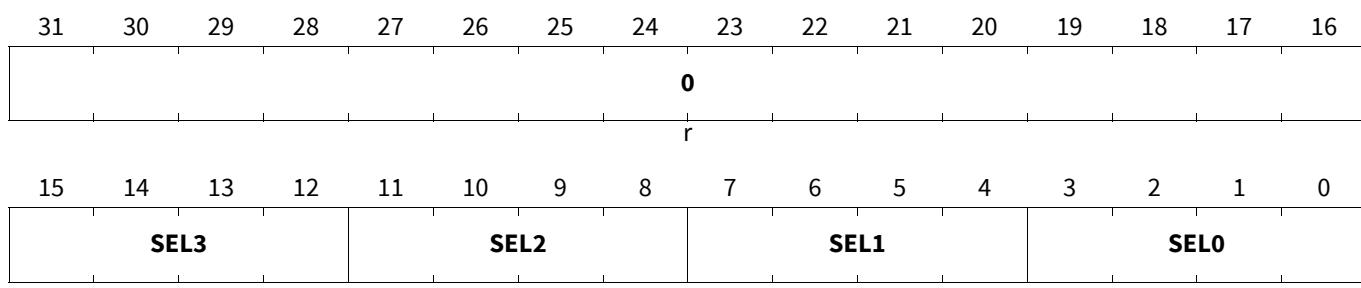
## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SELx (x=4-5)</b>	$4^*x+3:4^*x$	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li><math>1_H</math> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</li> <li><math>2_H</math> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li><math>3_H</math> <b>TOM1_12</b>, Output of TOM1, channel 12</li> <li><math>4_H</math> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</li> <li><math>5_H</math> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</li> <li><math>6_H</math> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</li> <li><math>7_H</math> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li><math>8_H</math> Reserved, do not use</li> <li>...</li> <li><math>F_H</math> Reserved, do not use</li> </ul>
<b>SELx (x=6-7)</b>	$4^*x+3:4^*x$	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x.</p> <ul style="list-style-type: none"> <li><math>0_H</math> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li><math>1_H</math> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</li> <li><math>2_H</math> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li><math>3_H</math> <b>TOM1_12</b>, Output of TOM1, channel 12</li> <li><math>4_H</math> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</li> <li><math>5_H</math> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</li> <li><math>6_H</math> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</li> <li><math>7_H</math> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li><math>8_H</math> Reserved, do not use</li> <li>...</li> <li><math>F_H</math> Reserved, do not use</li> </ul>

### CAN2 Output Select Register

This register holds the selection for the trigger outputs 0..3 to the CAN2 module.

## Generic Timer Module (GTM)

**GTM\_CANOUTSEL1****CAN2 Output Select Register****(09FFE0<sub>H</sub>)****Application Reset Value: XXXX 0000<sub>H</sub>**

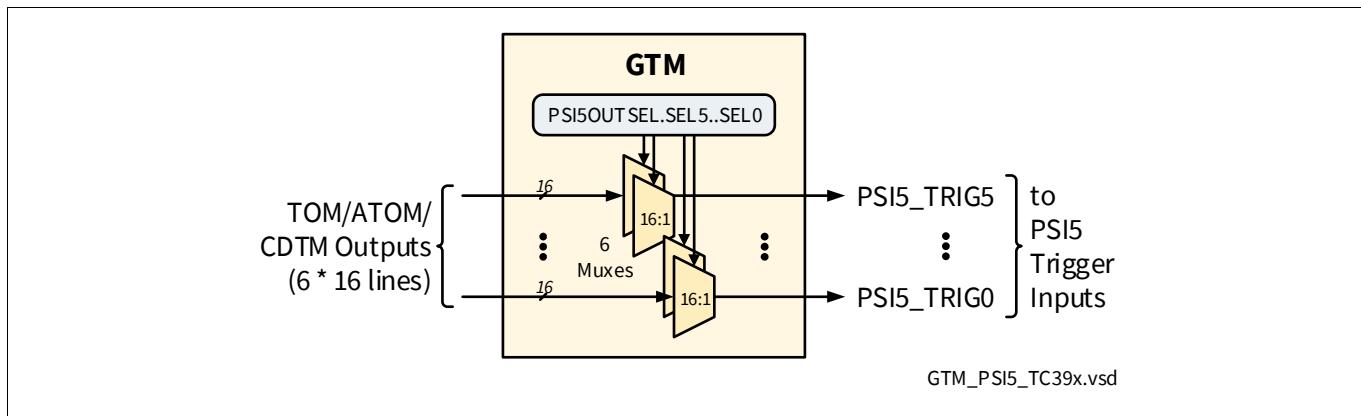
Field	Bits	Type	Description
<b>SELx (x=0)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN2 node trigger x.</p> <p>0<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4      1<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5      2<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11      3<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12      4<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0      5<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1      6<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2      7<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3      8<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6      9<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7      A<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13      B<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14      C<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4      D<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5      E<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6      F<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7       </p>

**Generic Timer Module (GTM)**

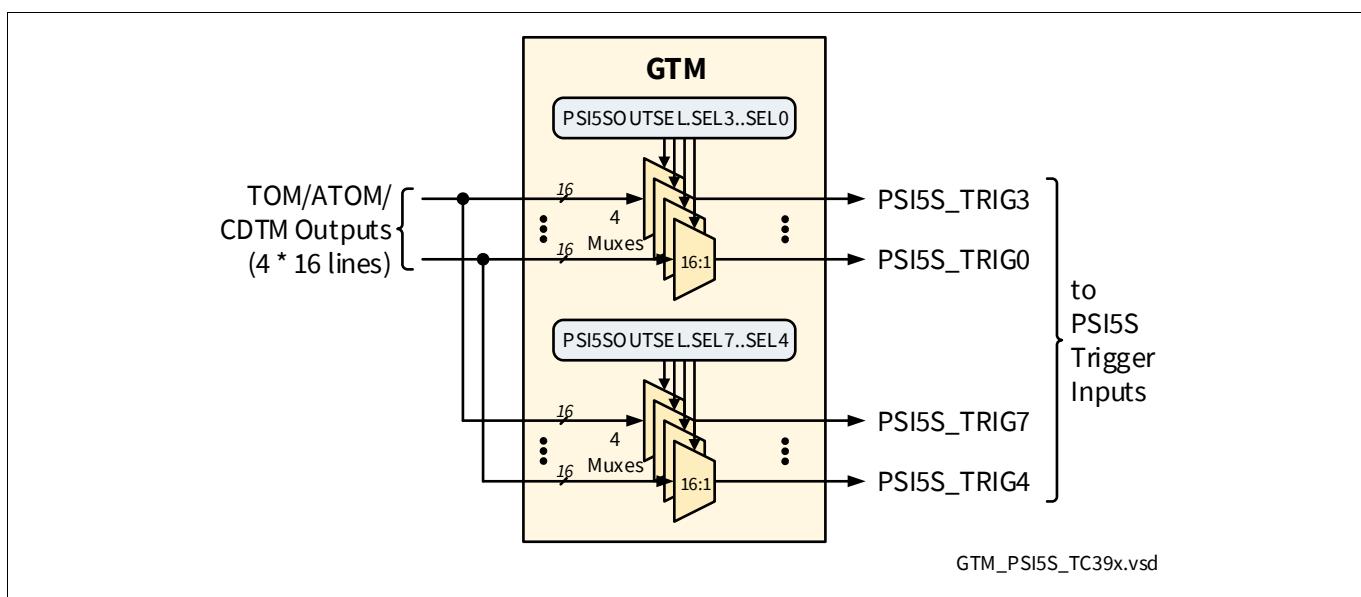
<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
<b>SELx (x=1)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN2 node trigger x.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li>1<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</li> <li>2<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li>3<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12</li> <li>4<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</li> <li>5<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</li> <li>6<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</li> <li>7<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li>8<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</li> <li>9<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>A<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13</li> <li>B<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14</li> <li>C<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</li> <li>D<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</li> <li>E<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</li> <li>F<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</li> </ul>
<b>SELx (x=2-3)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to CAN connection x</b></p> <p>This bit field defines which TOM/ATOM channel output is used as CAN2 node trigger x.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> <b>CDTM1_DTM1_0, TOM1_4</b>, Dead-time output of TOM1, channel 4</li> <li>1<sub>H</sub> <b>CDTM1_DTM1_1, TOM1_5</b>, Dead-time output of TOM1, channel 5</li> <li>2<sub>H</sub> <b>TOM1_11</b>, Output of TOM1, channel 11</li> <li>3<sub>H</sub> <b>TOM1_12</b>, Output of TOM1, channel 12</li> <li>4<sub>H</sub> <b>CDTM2_DTM4_0, ATOM2_0</b>, Dead-time output of ATOM2, channel 0</li> <li>5<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</li> <li>6<sub>H</sub> <b>CDTM2_DTM4_2, ATOM2_2</b>, Dead-time output of ATOM2, channel 2</li> <li>7<sub>H</sub> <b>CDTM2_DTM4_3, ATOM2_3</b>, Dead-time output of ATOM2, channel 3</li> <li>8<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>0</b>	31:16	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

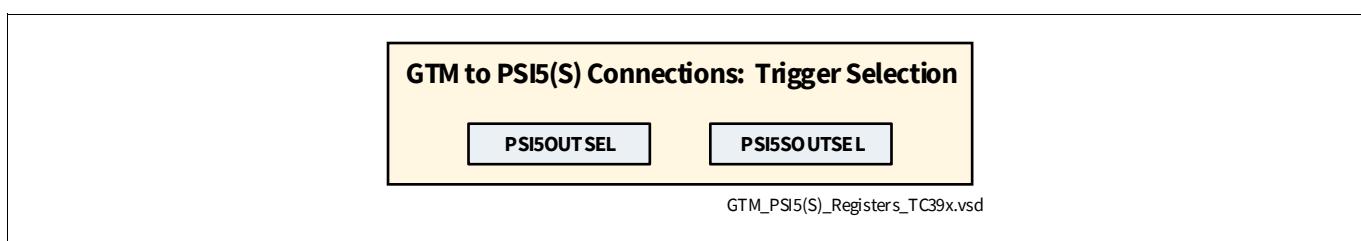
### 26.3.11 GTM to PSI5(S) Connections



**Figure 28 GTM to PSI5 Connections Overview**



**Figure 29 GTM to PSI5S Connections Overview**



**Figure 30 GTM to PSI5(S) Connections Registers Overview**

**Generic Timer Module (GTM)****PSI5 Output Select Register****GTM\_PSI5OUTSEL****PSI5 Output Select Register****(09FFCC<sub>H</sub>)****Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0									SEL5			SEL4			
				r						rw					rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
				rw			rw		rw				rw		rw

Field	Bits	Type	Description
<b>SELx (x=0-5)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to PSI5x connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as PSI5 trigger x.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</li> <li>2<sub>H</sub> <b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</li> <li>3<sub>H</sub> <b>TOM2_13</b>, Output of TOM2, channel 13</li> <li>4<sub>H</sub> <b>TOM2_14</b>, Output of TOM2, channel 14</li> <li>5<sub>H</sub> <b>CDTM2_DTM5_0, ATOM2_4</b>, Dead-time output of ATOM2, channel 4</li> <li>6<sub>H</sub> <b>CDTM2_DTM5_1, ATOM2_5</b>, Dead-time output of ATOM2, channel 5</li> <li>7<sub>H</sub> <b>CDTM2_DTM5_2, ATOM2_6</b>, Dead-time output of ATOM2, channel 6</li> <li>8<sub>H</sub> <b>CDTM2_DTM5_3, ATOM2_7</b>, Dead-time output of ATOM2, channel 7</li> <li>9<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</li> <li>A<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</li> <li>B<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13</li> <li>C<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14</li> <li>D<sub>H</sub> Reserved, do not use</li> <li>...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>0</b>	31:24	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

### PSI5-S Output Select Register

#### GTM\_PSI5SOUTSEL

#### PSI5-S Output Select Register

(09FFD0<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>SEL7</b>				<b>SEL6</b>				<b>SEL5</b>				<b>SEL4</b>			
rw					rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SEL3</b>				<b>SEL2</b>				<b>SEL1</b>				<b>SEL0</b>			
rw					rw				rw				rw		

Field	Bits	Type	Description
SELx (x=0,4)	4*x+3:4*x	rw	<p><b>Output Selection for GTM to PSI5-S connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <p>0<sub>H</sub> No trigger</p> <p>1<sub>H</sub> <b>CDTM0_DTM1_2, TOM0_6</b>, Dead-time output of TOM0, channel 6</p> <p>2<sub>H</sub> <b>CDTM0_DTM1_3, TOM0_7</b>, Dead-time output of TOM0, channel 7</p> <p>3<sub>H</sub> <b>TOM0_13</b>, Output of TOM0, channel 13</p> <p>4<sub>H</sub> <b>TOM0_14</b>, Output of TOM0, channel 14</p> <p>5<sub>H</sub> <b>CDTM0_DTM5_0, ATOM0_4</b>, Dead-time output of ATOM0, channel 4</p> <p>6<sub>H</sub> <b>CDTM0_DTM5_1, ATOM0_5</b>, Dead-time output of ATOM0, channel 5</p> <p>7<sub>H</sub> <b>CDTM0_DTM5_2, ATOM0_6</b>, Dead-time output of ATOM0, channel 6</p> <p>8<sub>H</sub> <b>CDTM0_DTM5_3, ATOM0_7</b>, Dead-time output of ATOM0, channel 7</p> <p>9<sub>H</sub> Reserved, do not use</p> <p>... F<sub>H</sub> Reserved, do not use</p>

## Generic Timer Module (GTM)

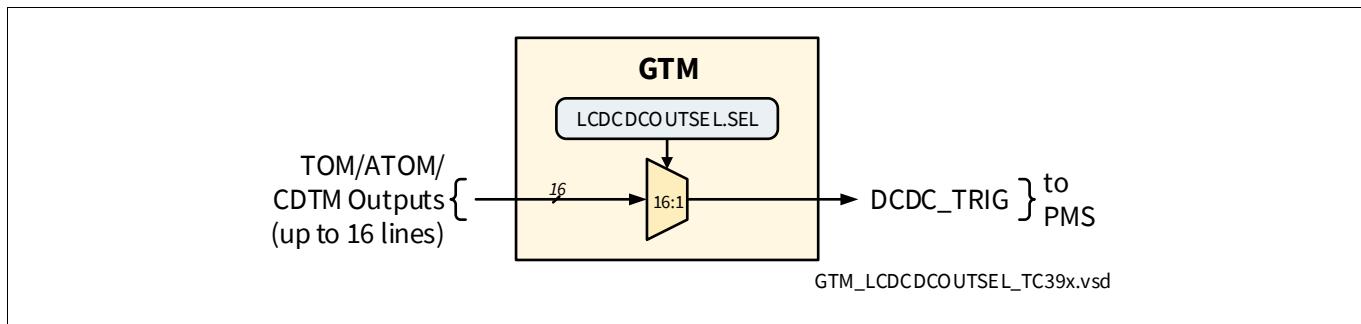
Field	Bits	Type	Description
<b>SELx (x=1,5)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to PSI5-S connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</li> <li>2<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>3<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13</li> <li>4<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14</li> <li>5<sub>H</sub> <b>CDTM1_DTM5_0, ATOM1_4</b>, Dead-time output of ATOM1, channel 4</li> <li>6<sub>H</sub> <b>CDTM1_DTM5_1, ATOM1_5</b>, Dead-time output of ATOM1, channel 5</li> <li>7<sub>H</sub> <b>CDTM1_DTM5_2, ATOM1_6</b>, Dead-time output of ATOM1, channel 6</li> <li>8<sub>H</sub> <b>CDTM1_DTM5_3, ATOM1_7</b>, Dead-time output of ATOM1, channel 7</li> <li>9<sub>H</sub> Reserved, do not use</li> <li>... ...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>
<b>SELx (x=2,6)</b>	4*x+3:4*x	rw	<p><b>Output Selection for GTM to PSI5-S connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM1_DTM1_2, TOM1_6</b>, Dead-time output of TOM1, channel 6</li> <li>2<sub>H</sub> <b>CDTM1_DTM1_3, TOM1_7</b>, Dead-time output of TOM1, channel 7</li> <li>3<sub>H</sub> <b>TOM1_13</b>, Output of TOM1, channel 13</li> <li>4<sub>H</sub> <b>TOM1_14</b>, Output of TOM1, channel 14</li> <li>5<sub>H</sub> <b>CDTM3_DTM5_0, ATOM3_4</b>, Dead-time output of ATOM3, channel 4</li> <li>6<sub>H</sub> <b>CDTM3_DTM5_1, ATOM3_5</b>, Dead-time output of ATOM3, channel 5</li> <li>7<sub>H</sub> <b>CDTM3_DTM5_2, ATOM3_6</b>, Dead-time output of ATOM3, channel 6</li> <li>8<sub>H</sub> <b>CDTM3_DTM5_3, ATOM3_7</b>, Dead-time output of ATOM3, channel 7</li> <li>9<sub>H</sub> Reserved, do not use</li> <li>... ...</li> <li>F<sub>H</sub> Reserved, do not use</li> </ul>

**Generic Timer Module (GTM)**

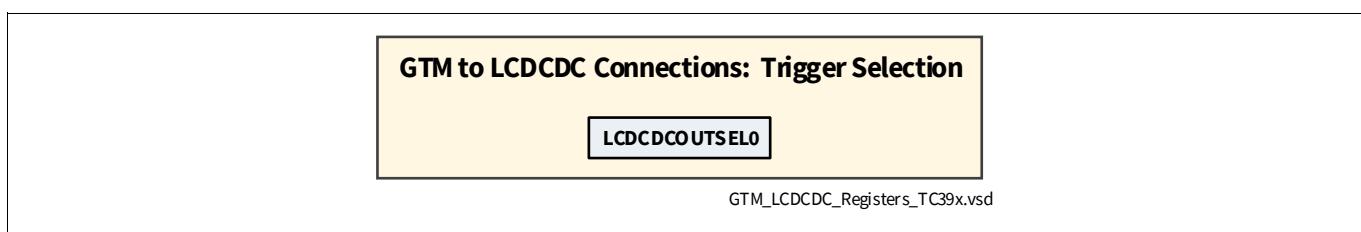
<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>																								
<b>SELx (x=3,7)</b>	$4^*x+3:4^*x$	rw	<p><b>Output Selection for GTM to PSI5-S connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <table> <tr> <td><math>0_H</math></td> <td>No trigger</td> </tr> <tr> <td><math>1_H</math></td> <td><b>CDTM2_DTM1_2, TOM2_6</b>, Dead-time output of TOM2, channel 6</td> </tr> <tr> <td><math>2_H</math></td> <td><b>CDTM2_DTM1_3, TOM2_7</b>, Dead-time output of TOM2, channel 7</td> </tr> <tr> <td><math>3_H</math></td> <td><b>TOM2_13</b>, Output of TOM2, channel 13</td> </tr> <tr> <td><math>4_H</math></td> <td><b>TOM2_14</b>, Output of TOM2, channel 14</td> </tr> <tr> <td><math>5_H</math></td> <td><b>CDTM4_DTM5_0, ATOM4_4</b>, Dead-time output of ATOM4, channel 4</td> </tr> <tr> <td><math>6_H</math></td> <td><b>CDTM4_DTM5_1, ATOM4_5</b>, Dead-time output of ATOM4, channel 5</td> </tr> <tr> <td><math>7_H</math></td> <td><b>CDTM4_DTM5_2, ATOM4_6</b>, Dead-time output of ATOM4, channel 6</td> </tr> <tr> <td><math>8_H</math></td> <td><b>CDTM4_DTM5_3, ATOM4_7</b>, Dead-time output of ATOM4, channel 7</td> </tr> <tr> <td><math>9_H</math></td> <td>Reserved, do not use</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td><math>F_H</math></td> <td>Reserved, do not use</td> </tr> </table>	$0_H$	No trigger	$1_H$	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6	$2_H$	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7	$3_H$	<b>TOM2_13</b> , Output of TOM2, channel 13	$4_H$	<b>TOM2_14</b> , Output of TOM2, channel 14	$5_H$	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4	$6_H$	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5	$7_H$	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6	$8_H$	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7	$9_H$	Reserved, do not use	...		$F_H$	Reserved, do not use
$0_H$	No trigger																										
$1_H$	<b>CDTM2_DTM1_2, TOM2_6</b> , Dead-time output of TOM2, channel 6																										
$2_H$	<b>CDTM2_DTM1_3, TOM2_7</b> , Dead-time output of TOM2, channel 7																										
$3_H$	<b>TOM2_13</b> , Output of TOM2, channel 13																										
$4_H$	<b>TOM2_14</b> , Output of TOM2, channel 14																										
$5_H$	<b>CDTM4_DTM5_0, ATOM4_4</b> , Dead-time output of ATOM4, channel 4																										
$6_H$	<b>CDTM4_DTM5_1, ATOM4_5</b> , Dead-time output of ATOM4, channel 5																										
$7_H$	<b>CDTM4_DTM5_2, ATOM4_6</b> , Dead-time output of ATOM4, channel 6																										
$8_H$	<b>CDTM4_DTM5_3, ATOM4_7</b> , Dead-time output of ATOM4, channel 7																										
$9_H$	Reserved, do not use																										
...																											
$F_H$	Reserved, do not use																										

## Generic Timer Module (GTM)

### 26.3.12 GTM to LC DC/DC Connection



**Figure 31 GTM to LCDCDC Connections Overview**



**Figure 32 GTM to LCDCDC Connections Registers Overview**

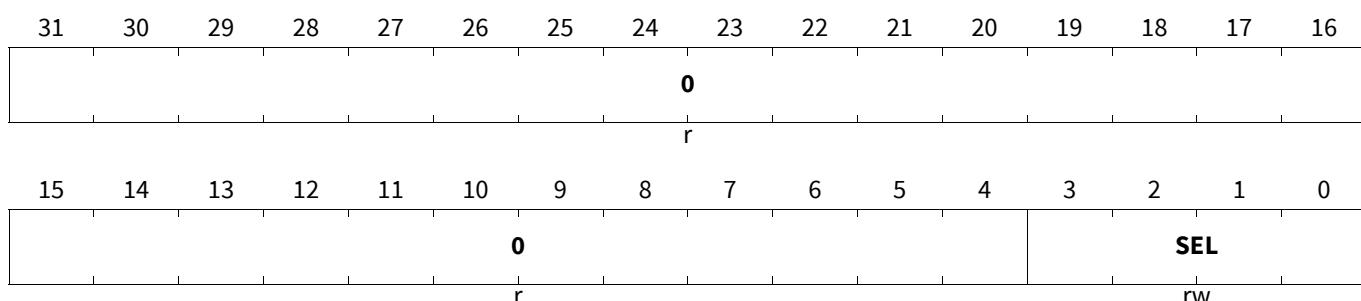
### LCDCDC Output Select Register

#### GTM\_LCDCDCOUTSEL

#### LCDCDC Output Select Register

(09FFD4<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>



## Generic Timer Module (GTM)

Field	Bits	Type	Description
<b>SEL</b>	3:0	rw	<p><b>Output Selection for GTM to LCDCDC connection</b></p> <p>This bit field defines which TOM/ATOM channel output is used as LCDCDC signal.</p> <ul style="list-style-type: none"> <li>0<sub>H</sub> No trigger</li> <li>1<sub>H</sub> <b>CDTM0_DTM4_1, ATOM0_1</b>, Dead-time output of ATOM0, channel 1</li> <li>2<sub>H</sub> <b>CDTM1_DTM4_1, ATOM1_1</b>, Dead-time output of ATOM1, channel 1</li> <li>3<sub>H</sub> <b>CDTM2_DTM4_1, ATOM2_1</b>, Dead-time output of ATOM2, channel 1</li> <li>4<sub>H</sub> <b>CDTM3_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM3, channel 1</li> <li>5<sub>H</sub> <b>CDTM4_DTM4_1, ATOM3_1</b>, Dead-time output of ATOM4, channel 1</li> <li>6<sub>H</sub> <b>CDTM0_DTM0_1, TOM0_1</b>, Dead-time output of TOM0, channel 1</li> <li>7<sub>H</sub> <b>CDTM1_DTM0_1, TOM1_1</b>, Dead-time output of TOM1, channel 1</li> <li>8<sub>H</sub> <b>CDTM2_DTM0_1, TOM2_1</b>, Dead-time output of TOM2, channel 1</li> <li>9<sub>H</sub> <b>CDTM3_DTM0_1, TOM3_1</b>, Dead-time output of TOM3, channel 1</li> <li>A<sub>H</sub> <b>CDTM4_DTM0_1, TOM4_1</b>, Dead-time output of TOM4, channel 1</li> <li>B<sub>H</sub> Reserved, do not use</li> <li>... F<sub>H</sub> Reserved, do not use</li> </ul>
<b>0</b>	31:4	r	<p><b>Reserved</b></p> <p>Read as 0, shall be written with 0.</p>

## Generic Timer Module (GTM)

### 26.4 ARU Parameters

The following sections list the device-specific parameters of the ARU.

#### 26.4.1 ARU Write Address Overview

The ARU write address map for the TC39x is specified in the following table.

**Table 341 ARU Write Addresses**

GTM Data Source	ARU Address
ARU_ACCESS	0x000
TIM0_WRADDR[0..7]	0x001..0x008
TIM1_WRADDR[0..7]	0x009..0x010
TIM2_WRADDR[0..7]	0x011..0x018
TIM3_WRADDR[0..7]	0x019..0x020
TIM4_WRADDR[0..7]	0x021..0x028
TIM5_WRADDR[0..7]	0x029..0x030
TIM6_WRADDR[0..7]	0x031..0x038
unused	0x039..0x050
F2A0_WRADDR[0..7]	0x051..0x058
F2A1_WRADDR[0..7]	0x059..0x060
BRC_WRADDR[0..21]	0x061..0x076
MCS0_WRADDR[0..23]	0x077..0x08E
MCS1_WRADDR[0..23]	0x08F..0x0A6
MCS2_WRADDR[0..23]	0x0A7..0x0BE
MCS3_WRADDR[0..23]	0x0BF..0x0D6
MCS4_WRADDR[0..23]	0x0D7..0x0EE
MCS5_WRADDR[0..23]	0x0EF..0x106
MCS6_WRADDR[0..23]	0x107..0x11E
ATOM0_WRADDR[0..7]	0x11F..0x126
ATOM1_WRADDR[0..7]	0x127..0x12E
ATOM2_WRADDR[0..7]	0x12F..0x136
ATOM3_WRADDR[0..7]	0x137..0x13E
ATOM4_WRADDR[0..7]	0x13F..0x146
ATOM5_WRADDR[0..7]	0x147..0x14E
ATOM6_WRADDR[0..7]	0x14F..0x156
ATOM7_WRADDR[0..7]	0x157..0x15E
ATOM8_WRADDR[0..7]	0x15F..0x166
ATOM9_WRADDR[0..7]	0x167..0x16E
ATOM10_WRADDR[0..7]	0x16F..0x176
ATOM11_WRADDR[0..7]	0x177..0x17E
DPLL_WRADDR[0..31]	0x17F..0x19E

## Generic Timer Module (GTM)

**Table 341 ARU Write Addresses (cont'd)**

GTM Data Source	ARU Address
TIM7_WRADDR[0..7]	0x19F..0x1A6
F2A2_WRADDR[0..7]	0x1A7..0x1AE
MCS7_WRADDR[0..23]	0x1AF..0x1C6
MCS8_WRADDR[0..23]	0x1C7..0x1DE
MCS9_WRADDR[0..23]	0x1DF..0x1F6
unused	0x1F7..0x1FD
ARU_EMPTY_ADDR	0x1FE
ARU_FULL_ADDR	0x1FF

### 26.4.2 ARU Port Partitioning

All GTM sub-modules which are reading from ARU can be connected to one of two ARU read ports. Therefore, it can be read from two different ARU addresses in parallel.

**Table 342 GTM ARU Partitioning**

Modules	ARU-0 port	ARU-1 port
ATOM0	X	
ATOM1		X
ATOM2	X	
ATOM3		X
ATOM4	X	
ATOM5		X
ATOM6	X	
ATOM7		X
ATOM8	X	
ATOM9		X
ATOM10	X	
ATOM11	X	
MCS0	X	
MCS1		X
MCS2	X	
MCS3		X
MCS4	X	
MCS5		X
MCS6	X	
MCS7		X
MCS8	X	
MCS9		X

## Generic Timer Module (GTM)

**Table 342 GTM ARU Partitioning (cont'd)**

Modules	ARU-0 port	ARU-1 port
DPLL		X
BRC	X	
PSM0	X	
PSM1		X
PSM2	X	

### 26.4.3 ARU Read ID

Each ARU connected data destination is defined by a combination of ARU port (ARU0 or ARU1) and an ARU read ID. The two ARU counter are addressing two ARU read IDs in parallel. Depending on the ARU mode, both counter may have different values at different point in time (i.e. in dynamic routing mode). The maximum ARU round-trip time is determined by the value of the last ARU read ID. The following table describes the detailed addressing of GTM sub-modules by ARU read IDs.

The following table shows the ARU read IDs for TC39xB silicon. As this is the superset it is identical to the table shown in the family spec. The unused IDs are marked with “-”.

**Table 343 GTM Read IDs for TC39x**

ARU read ID (dec)	ARU0	ARU1	GTM read ID (dec)	ARU0	ARU1
0	reserved	reserved	64	ATOM4 channel 3	DPLL action 31
1	<b>ARU0</b>	<b>ARU1</b>	65	MCS4 channel 7	MCS3 channel 7
2	<b>BRC</b> channel 0	<b>DPLL</b> action0	66	ATOM4 channel 4	<b>ATOM3</b> channel 0
3	<b>PSM0</b> channel 0	<b>PSM1</b> channel 0	67	<b>MCS6</b> channel 0	<b>MCS5</b> channel 0
4	BRC channel 1	DPLL action 1	68	ATOM4 channel 5	ATOM3 channel 1
5	PSM0 channel 1	PSM1 channel 1	69	MCS6 channel 1	MCS5 channel 1
6	BRC channel 2	DPLL action 2	70	ATOM4 channel 6	ATOM3 channel 2
7	PSM0 channel 2	PSM1 channel 2	71	MCS6 channel 2	MCS5 channel 2
8	BRC channel 3	DPLL action 3	72	ATOM4 channel 7	ATOM3 channel 3
9	PSM0 channel 3	PSM1 channel 3	73	MCS6 channel 3	MCS5 channel 3
10	BRC channel 4	DPLL action 4	74	<b>ATOM6</b> channel 0	ATOM3 channel 4
11	PSM0 channel 4	PSM1 channel 4	75	MCS6 channel 4	MCS5 channel 4
12	BRC channel 5	DPLL action 5	76	ATOM6 channel 1	ATOM3 channel 5
13	PSM0 channel 5	PSM1 channel 5	77	MCS6 channel 5	MCS5 channel 5
14	BRC channel 6	DPLL action 6	78	ATOM6 channel 2	ATOM3 channel 6
15	PSM0 channel 6	PSM1 channel 6	79	MCS6 channel 6	MCS5 channel 6
16	BRC channel 7	DPLL action 7	80	ATOM6 channel 3	ATOM3 channel 7
17	PSM0 channel 7	PSM1 channel 7	81	MCS6 channel 7	MCS5 channel 7
18	BRC channel 8	DPLL action 8	82	ATOM6 channel 4	<b>ATOM5</b> channel 0
19	<b>MCS0</b> channel 0	<b>MCS1</b> channel 0	83	<b>ATOM8</b> channel 0	<b>ATOM7</b> channel 0

## Generic Timer Module (GTM)

Table 343 GTM Read IDs for TC39x (cont'd)

ARU read ID (dec)	ARU0	ARU1	GTM read ID (dec)	ARU0	ARU1
20	BRC channel 9	DPLL action 9	84	ATOM6 channel 5	ATOM5 channel 1
21	MCS0 channel 1	MCS1 channel 1	85	ATOM8 channel 1	ATOM7 channel 1
22	BRC channel 10	DPLL action 10	86	ATOM6 channel 6	ATOM5 channel 2
23	MCS0 channel 2	MCS1 channel 2	87	ATOM8 channel 2	ATOM7 channel 2
24	BRC channel 11	DPLL action 11	88	ATOM6 channel 7	ATOM5 channel 3
25	MCS0 channel 3	MCS1 channel 3	89	ATOM8 channel 3	ATOM7 channel 3
26	<b>ATOM0</b> channel 0	DPLL action 12	90	<b>MCS8</b> channel 0	ATOM5 channel 4
27	MCS0 channel 4	MCS1 channel 4	91	ATOM8 channel 4	ATOM7 channel 4
28	ATOM0 channel 1	DPLL action 13	92	MCS8 channel 1	ATOM5 channel 5
29	MCS0 channel 5	MCS1 channel 5	93	ATOM8 channel 5	ATOM7 channel 5
30	ATOM0 channel 2	DPLL action 14	94	MCS8 channel 2	ATOM5 channel 6
31	MCS0 channel 6	MCS1 channel 6	95	ATOM8 channel 6	ATOM7 channel 6
32	ATOM0 channel 3	DPLL action 15	96	MCS8 channel 3	ATOM5 channel 7
33	MCS0 channel 7	MCS1 channel 7	97	ATOM8 channel 7	ATOM7 channel 7
34	ATOM0 channel 4	DPLL action 16	98	MCS8 channel 4	<b>MCS7</b> channel 0
35	MCS2 channel 0	<b>ATOM1</b> channel 0	99	<b>ATOM10</b> channel 0	<b>ATOM9</b> channel 0
36	ATOM0 channel 5	DPLL action 17	100	MCS8 channel 5	MCS7 channel 1
37	MCS2 channel 1	ATOM1 channel 1	101	ATOM10 channel 1	ATOM9 channel 1
38	ATOM0 channel 6	DPLL action 18	102	MCS8 channel 6	MCS7 channel 2
39	MCS2 channel 2	ATOM1 channel 2	103	ATOM10 channel 2	ATOM9 channel 2
40	ATOM0 channel 7	DPLL action 19	104	MCS8 channel 7	MCS7 channel 3
41	MCS2 channel 3	ATOM1 channel 3	105	ATOM10 channel 3	ATOM9 channel 3
42	<b>ATOM2</b> channel 0	DPLL action 20	106	<b>PSM2</b> channel 0	MCS7 channel 4
43	MCS2 channel 4	ATOM1 channel 4	107	ATOM10 channel 4	ATOM9 channel 4
44	ATOM2 channel 1	DPLL action 21	108	PSM2 channel 1	MCS7 channel 5
45	MCS2 channel 5	ATOM1 channel 5	109	ATOM10 channel 5	ATOM9 channel 5
46	ATOM2 channel 2	DPLL action 22	110	PSM2 channel 2	MCS7 channel 6
47	MCS2 channel 6	ATOM1 channel 6	111	ATOM10 channel 6	ATOM9 channel 6
48	ATOM2 channel 3	DPLL action 23	112	PSM2 channel 3	MCS7 channel 7
49	MCS2 channel 7	ATOM1 channel 7	113	ATOM10 channel 7	ATOM9 channel 6
50	ATOM2 channel 4	DPLL action 24	114	PSM2 channel 4	<b>MCS9</b> channel 0
51	<b>MCS4</b> channel 0	<b>MCS3</b> channel 0	115	<b>ATOM11</b> channel 0	MCS9 channel 1
52	ATOM2 channel 5	DPLL action 25	116	PSM2 channel 5	MCS9 channel 2
53	MCS4 channel 1	MCS3 channel 1	117	ATOM11 channel 1	-
54	ATOM2 channel 6	DPLL action 26	118	PSM2 channel 6	MCS9 channel 3
55	MCS4 channel 2	MCS3 channel 2	119	ATOM11 channel 2	-
56	ATOM2 channel 7	DPLL action 27	120	PSM2 channel 7	MCS9 channel 4

## Generic Timer Module (GTM)

**Table 343 GTM Read IDs for TC39x (cont'd)**

ARU read ID (dec)	ARU0	ARU1	GTM read ID (dec)	ARU0	ARU1
57	MCS4 channel 3	MCS3 channel 3	121	ATOM11 channel 3	-
58	<b>ATOM4</b> channel 0	DPLL action 28	122	ATOM11 channel 4	MCS9 channel 5
59	MCS4 channel 4	MCS3 channel 4	123	ATOM11 channel 5	-
60	ATOM4 channel 1	DPLL action 29	124	-	MCS9 channel 6
61	MCS4 channel 5	MCS3 channel 5	125	ATOM11 channel 6	-
62	ATOM4 channel 2	DPLL action 30	126	-	MCS9 channel 7
63	MCS4 channel 6	MCS3 channel 6	127	ATOM11 channel 7	-

**Generic Timer Module (GTM)****26.5 Revision History****Table 344 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
V2.2.9		
	Cleaned up DSADC register structure, easing readability	
	Connectivity table removed from customer specification, as no added value for programming the GTM.	
V2.2.10		
<a href="#">Page 411</a>	Added tables on ARU Write Addresses, ARU Port Partitioning; updated ARU Read ID table	
<a href="#">Page 2</a>	Cleanup of Table 1	
<a href="#">Page 38</a>	Added connection diagrams and register overview tables	
<a href="#">Page 38</a>	Added missing register(s)	
V2.2.11		
<a href="#">Page 38</a>	Added missing registers GTM_ICM_IRQG_CLS_k_MEI	
<a href="#">Table 333</a>	Added package information to TOUTy table	
<a href="#">Table 337</a>	Added GTM to EDSADC connection information	
<a href="#">Table 340</a>	Added GTM to EVADC/EDSADC/SENT connection information	
<a href="#">Figure 22</a> , <a href="#">Figure 24</a>	Updated figures regarding EVADC/EDSADC/SENT connections	
V2.2.11		
<a href="#">Page 38</a>	Register Overview - GTM Protection Mechanism corrected	
<a href="#">Page 38</a>	GTM_CCMi_CFG register now only includes EN_CMP_MON for cluster 1, therefore changed reset value.	
	GTM_CMU_CLK_z_CTRL remark that certain bitfields are only valid, if a DPLL is existent, as TC33x has no DPLL.	
	GTM_TIMnINSEL removed TINxx information	
V2.2.12		
	no changes for TC38x	
V2.2.13		
<a href="#">Page 398</a>	CANOUTSEL fixed	
	Adding registers, which are changing among AURIX family members, but were missing inside the TC38x appendix.	
V2.2.15		
	Remarks inside OCDS Registers, concerning status, if TBU channel 3, DPLL or MCS do not exist on a device.	
	CCMi_HW_CONF gets proper bit descriptions, as constants have been all 0x0.	
V2.2.18		
	IRQ_NOTIFY registers: Remark, that due to bit property rw, these registers have to be written to reset.	

**Generic Timer Module (GTM)****Table 344 Revision History (cont'd)**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
	DTMAUXINSEL: Corrected. Non existing sideband signals and pins are out of this list.	
	CANOUTSEL corrected to be matching with design.	
V2.2.19		
	CMU_CLK_z_CTRL registers completely listed	
V2.2.20		
	Changes have no impact on this document.	
V2.2.21		
	Changes have no impact on this document.	
V2.2.22		
	Changes have no impact on this document.	
V2.2.23		
	Changes have no impact on this document.	
V2.2.24		
	Corrected typo on MSC registers.	

**Capture/Compare Unit 6 (CCU6)****27 Capture/Compare Unit 6 (CCU6)**

This chapter describes the specific properties of the product TC39x-B, which is a member of the product family TC3XX.

The functionality of the CCU6 is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

**27.1 TC39x-B Specific Register Set****Table 345 Register Address Space - CCU6**

Module	Base Address	End Address	Note
CCU60	F0002A00 <sub>H</sub>	F0002AFF <sub>H</sub>	FPI slave interface
CCU61	F0002B00 <sub>H</sub>	F0002BFF <sub>H</sub>	FPI slave interface

**Note:** *Register MOSEL controls the trigger signals from both CCU6 kernels (CCU60 and CCU61) of the CCU6 module, and is only available in the address space of kernel CCU60.*

**Register Overview Tables of CCU6****Table 346 Register Overview - CCU60 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_CLC	Clock Control Register	0000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_MCFG	Module Configuration Register	0004 <sub>H</sub>	U,SV	U,SV,P	See Family Spec	See Family Spec
CCU60_ID	Module Identification Register	0008 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
CCU60_MOSEL	CCU60 Module Output Select Register	000C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PISEL0	Port Input Select Register 0	0010 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PISEL2	Port Input Select Register 2	0014 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_KCSR	Kernel State Control Sensitivity Register	001C <sub>H</sub>	U,SV	U,SV,P,OEN	See Family Spec	See Family Spec
CCU60_T12	Timer T12 Counter Register	0020 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Capture/Compare Unit 6 (CCU6)****Table 346 Register Overview - CCU60 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
CCU60_T12PR	Timer 12 Period Register	0024 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T12DTC	Dead-Time Control Register for Timer12	0028 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC6xR (x=0-2)	Capture/Compare Register for Channel CC6x	0030 <sub>H</sub> +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC6xSR (x=0-2)	Capture/Compare Shadow Reg. for Channel CC6x	0040 <sub>H</sub> +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T13	Timer T13 Counter Register	0050 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T13PR	Timer 13 Period Register	0054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC63R	Compare Register for T13	0058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC63SR	Compare Shadow Register for T13	005C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CMPSTAT	Compare State Register	0060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CMPMOD IF	Compare State Modification Register	0064 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T12MSEL	T12 Mode Select Register	0068 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR0	Timer Control Register 0	0070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR2	Timer Control Register 2	0074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR4	Timer Control Register 4	0078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Capture/Compare Unit 6 (CCU6)

Table 346 Register Overview - CCU60 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_MODCTR	Modulation Control Register	0080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TRPCTR	Trap Control Register	0084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PSLR	Passive State Level Register	0088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMOUT_S	Multi-Channel Mode Output Shadow Register	008C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMOUT	Multi-Channel Mode Output Register	0090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMCTR	Multi-Channel Mode Control Register	0094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IMON	Input Monitoring Register	0098 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_LI	Lost Indicator Register	009C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IS	Interrupt Status Register	00A0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_ISS	Interrupt Status Set Register	00A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_ISR	Interrupt Status Reset Register	00A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_INP	Interrupt Node Pointer Register	00AC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IEN	Interrupt Enable Register	00B0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_OCS	OCDS Control and Status Register	00E8 <sub>H</sub>	U,SV	SV,P,OEN	See Family Spec	See Family Spec

**Capture/Compare Unit 6 (CCU6)****Table 346 Register Overview - CCU60 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
CCU60_KRSTCLR	Kernel Reset Status Clear Register	00EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_KRST1	Kernel Reset Register 1	00F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_KRST0	Kernel Reset Register 0	00F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_ACCENO	Access Enable Register 0	00FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

**Table 347 Register Overview - CCU61 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
CCU61_CLC	Clock Control Register	0000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_MCFG	Module Configuration Register	0004 <sub>H</sub>	U,SV	U,SV,P	See Family Spec	See Family Spec
CCU61_ID	Module Identification Register	0008 <sub>H</sub>	U,SV	BE	See Family Spec	See Family Spec
CCU61_PISEL0	Port Input Select Register 0	0010 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_PISEL2	Port Input Select Register 2	0014 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_KCSR	Kernel State Control Sensitivity Register	001C <sub>H</sub>	U,SV	U,SV,P,OEN	See Family Spec	See Family Spec
CCU61_T12	Timer T12 Counter Register	0020 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T12PR	Timer 12 Period Register	0024 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Capture/Compare Unit 6 (CCU6)****Table 347 Register Overview - CCU61 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
CCU61_T12DTC	Dead-Time Control Register for Timer12	0028 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC6xR (x=0-2)	Capture/Compare Register for Channel CC6x	0030 <sub>H</sub> +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC6xSR (x=0-2)	Capture/Compare Shadow Reg. for Channel CC6x	0040 <sub>H</sub> +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T13	Timer T13 Counter Register	0050 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T13PR	Timer 13 Period Register	0054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC63R	Compare Register for T13	0058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC63SR	Compare Shadow Register for T13	005C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CMPSTAT	Compare State Register	0060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CMPMOD IF	Compare State Modification Register	0064 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T12MSEL	T12 Mode Select Register	0068 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR0	Timer Control Register 0	0070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR2	Timer Control Register 2	0074 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR4	Timer Control Register 4	0078 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MODCTR	Modulation Control Register	0080 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Capture/Compare Unit 6 (CCU6)

Table 347 Register Overview - CCU61 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_TRPCTR	Trap Control Register	0084 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_PSLR	Passive State Level Register	0088 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMOUT_S	Multi-Channel Mode Output Shadow Register	008C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMOUT	Multi-Channel Mode Output Register	0090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMCTR	Multi-Channel Mode Control Register	0094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IMON	Input Monitoring Register	0098 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_LI	Lost Indicator Register	009C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IS	Interrupt Status Register	00A0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_ISS	Interrupt Status Set Register	00A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_ISR	Interrupt Status Reset Register	00A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_INP	Interrupt Node Pointer Register	00AC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IEN	Interrupt Enable Register	00B0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_OCS	OCDS Control and Status Register	00E8 <sub>H</sub>	U,SV	SV,P,OEN	See Family Spec	See Family Spec
CCU61_KRSTCLR	Kernel Reset Status Clear Register	00EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec

**Capture/Compare Unit 6 (CCU6)****Table 347 Register Overview - CCU61 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
CCU61_KRST1	Kernel Reset Register 1	00F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_KRST0	Kernel Reset Register 0	00F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_ACCEN0	Access Enable Register 0	00FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

**27.2 TC39x-B Specific Registers**

No deviations from the Family Spec

**27.3 Connectivity****Table 348 Connections of CCU60**

<b>Interface Signals</b>	<b>connects</b>	<b>Description</b>	
CCU60:CC60	to	IOM:MON1(2)	T12 PWM channel 60
		IOM:REF1(6)	
		P02.0:ALT(7)	
		P02.6:ALT(7)	
		P11.12:ALT(7)	
		P15.6:ALT(7)	
		P34.2:ALT(7)	
CCU60:CC61	to	IOM:MON1(1)	T12 PWM channel 61
		IOM:REF1(5)	
		P02.2:ALT(7)	
		P02.7:ALT(7)	
		P11.11:ALT(7)	
		P15.5:ALT(7)	
		P34.4:ALT(7)	
CCU60:CC62	to	IOM:MON1(0)	T12 PWM channel 62
		IOM:REF1(4)	
		P02.4:ALT(7)	
		P02.8:ALT(7)	
		P11.10:ALT(7)	
		P15.4:ALT(7)	
		P33.14:ALT(7)	
CCU60:CC60INA	from	P02.0:IN	T12 capture input 60

**Capture/Compare Unit 6 (CCU6)****Table 348 Connections of CCU60 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CCU60:CC61INA	from	P02.2:IN	T12 capture input 61
CCU60:CC62INA	from	P02.4:IN	T12 capture input 62
CCU60:CC60INB	from	P00.1:IN	T12 capture input 60
CCU60:CC61INB	from	P00.3:IN	T12 capture input 61
CCU60:CC62INB	from	P00.5:IN	T12 capture input 62
CCU60:CC60INC	from	P02.6:IN	T12 capture input 60
CCU60:CC61INC	from	P02.7:IN	T12 capture input 61
CCU60:CC62INC	from	P02.8:IN	T12 capture input 62
CCU60:CC60IND	from	PMS:pms_wut_underflow	T12 capture input 60
CCU60:CC62IND	from	SCU:E_PDOUT(4)	T12 capture input 62
CCU60:CCPOS0A	from	P02.6:IN	Hall capture input 0
CCU60:CCPOS1A	from	P02.7:IN	Hall capture input 1
CCU60:CCPOS2A	from	P02.8:IN	Hall capture input 2
CCU60:CCPOS0B	from	CCU61:SR(2)	Hall capture input 0
CCU60:CCPOS1B	from	P40.1:IN	Hall capture input 1
CCU60:CCPOS2B	from	P40.3:IN	Hall capture input 2
CCU60:CCPOS0C	from	P10.4:IN	Hall capture input 0
CCU60:CCPOS1C	from	P10.7:IN	Hall capture input 1
CCU60:CCPOS2C	from	P10.8:IN	Hall capture input 2
CCU60:CCPOS0D	from	P40.0:IN	Hall capture input 0
CCU60:CCPOS1D	from	P40.2:IN	Hall capture input 1
CCU60:CCPOS2D	from	P40.4:IN	Hall capture input 2
CCU60:COUT60	to	SCU:E_REQ0(1) IOM:MON1(3) IOM:REF1(3) P02.1:ALT(7) P11.9:ALT(7) P15.7:ALT(7) P34.3:ALT(7)	T12 PWM channel 60
CCU60:COUT61	to	IOM:MON1(4) IOM:REF1(2) P02.3:ALT(7) P11.6:ALT(7) P15.8:ALT(7) P34.5:ALT(7)	T12 PWM channel 61

**Capture/Compare Unit 6 (CCU6)****Table 348 Connections of CCU60 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CCU60:COUT62	to	IOM:MON1(5)	T12 PWM channel 62
		IOM:REF1(1)	
		P02.5:ALT(7)	
		P11.3:ALT(7)	
		P14.0:ALT(7)	
		P33.15:ALT(7)	
CCU60:COUT63	to	IOM:MON1(6)	T13 PWM channel 63
		IOM:REF1(0)	
		P00.0:ALT(7)	
		P11.2:ALT(7)	
		P14.1:ALT(7)	
		P32.4:ALT(7)	
		P34.1:ALT(7)	
		PMS:dcdc_sync_ccu6	
CCU60:CTRAPA	from	P00.11:IN	Trap input capture
CCU60:TRAPB	from	CCU60:WHE_N	Trap input capture
CCU60:TRAPC	from	EVADC:FC0BFLOUT	Trap input capture
CCU60:TRAPD	from	SCU:E_PDOUT(0)	Trap input capture
CCU60:SR(0)	to	HSM:EXT_INT(10)	Service request
CCU60:SR(1)	to	CCU60:T13HRH	Service request
CCU60:SR(2)	to	CCU61:CCPOS0B	Service request
		CCU61:T12HRG	
		CCU61:T13HRG	
CCU60:SR(3)	to	EVADC:G0REQTRA	Service request
		EVADC:G1REQTRA	
		EVADC:G2REQTRA	
		EVADC:G3REQTRA	
		EVADC:G4REQTRA	
		EVADC:G5REQTRA	
		EVADC:G6REQTRA	
		EVADC:G7REQTRA	
		EVADC:G8REQTRA	
		EVADC:G9REQTRA	
		EVADC:G10REQTRA	
		EVADC:G11REQTRA	
CCU60:T12HRA	from	SCU:scu_cctrig0	External timer start 12
CCU60:T13HRA	from	SCU:scu_cctrig0	External timer start 13
CCU60:T12HRB	from	P00.7:IN	External timer start 12

**Capture/Compare Unit 6 (CCU6)****Table 348 Connections of CCU60 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CCU60:T13HRB	from	P00.8:IN	External timer start 13
CCU60:T12HRC	from	P00.9:IN	External timer start 12
CCU60:T13HRC	from	P00.9:IN	External timer start 13
CCU60:T12HRD	from	GTM:CCU6_TRIGGER(0)	External timer start 12
CCU60:T13HRD	from	GTM:CCU6_TRIGGER(1)	External timer start 13
CCU60:T12HRE	from	P00.0:IN	External timer start 12
CCU60:T12HRF	from	GPT120:T6OFL	External timer start 12
CCU60:T13HRF	from	GPT120:T6OFL	External timer start 13
CCU60:T12HRG	from	CCU61:SR(2)	External timer start 12
CCU60:T13HRG	from	CCU61:SR(2)	External timer start 13
CCU60:T12HRH	from	SCU:E_PDOUT(0)	External timer start 12
CCU60:T13HRH	from	CCU60:SR(1)	External timer start 13
CCU60:TRIG(0)	to	EVADC:G0REQGTC EVADC:G1REQGTC EVADC:G2REQGTC EVADC:G3REQGTC EVADC:G4REQGTC EVADC:G5REQGTC EVADC:G6REQGTC EVADC:G7REQGTC EVADC:G8REQGTC EVADC:G9REQGTC EVADC:G10REQGTC EVADC:G11REQGTC	Output select trigger
CCU60:TRIG(1)	to	EVADC:G0REQGTD EVADC:G1REQGTD EVADC:G2REQGTD EVADC:G3REQGTD EVADC:G4REQGTD EVADC:G5REQGTD EVADC:G6REQGTD EVADC:G7REQGTD EVADC:G8REQGTD EVADC:G9REQGTD EVADC:G10REQGTD EVADC:G11REQGTD	Output select trigger

**Capture/Compare Unit 6 (CCU6)****Table 348 Connections of CCU60 (cont'd)**

Interface Signals	connects		Description
CCU60:TRIG(2)	to	EVADC:G0REQGTE	Output select trigger
		EVADC:G1REQGTE	
		EVADC:G2REQGTE	
		EVADC:G3REQGTE	
		EVADC:G4REQGTE	
		EVADC:G5REQGTE	
		EVADC:G6REQGTE	
		EVADC:G7REQGTE	
		EVADC:G8REQGTE	
		EVADC:G9REQGTE	
		EVADC:G10REQGTE	
		EVADC:G11REQGTE	
CCU60:WHE_N	to	CCU60:CTRAPB	Set wrong hall event negative

**Table 349 Connections of CCU61**

Interface Signals	connects		Description
CCU61:CC60	to	IOM:MON1(8)	T12 PWM channel 60
		IOM:REF1(13)	
		P00.1:ALT(7)	
		P00.7:ALT(7)	
		P20.8:ALT(7)	
		P33.13:ALT(7)	
CCU61:CC61	to	IOM:MON1(9)	T12 PWM channel 61
		IOM:REF1(12)	
		P00.3:ALT(7)	
		P00.8:ALT(7)	
		P20.9:ALT(7)	
		P33.11:ALT(7)	
CCU61:CC62	to	IOM:MON1(10)	T12 PWM channel 62
		IOM:REF1(11)	
		P00.5:ALT(7)	
		P00.9:ALT(7)	
		P20.10:ALT(7)	
		P33.9:ALT(7)	
CCU61:CC60INA	from	P00.1:IN	T12 capture input 60
CCU61:CC61INA	from	P00.3:IN	T12 capture input 61
CCU61:CC62INA	from	P00.5:IN	T12 capture input 62
CCU61:CC60INB	from	P02.0:IN	T12 capture input 60

**Capture/Compare Unit 6 (CCU6)****Table 349 Connections of CCU61 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CCU61:CC61INB	from	P02.2:IN	T12 capture input 61
CCU61:CC62INB	from	P02.4:IN	T12 capture input 62
CCU61:CC60INC	from	P00.7:IN	T12 capture input 60
CCU61:CC61INC	from	P00.8:IN	T12 capture input 61
CCU61:CC62INC	from	P00.9:IN	T12 capture input 62
CCU61:CC60IND	from	PMS:pms_wut_underflow	T12 capture input 60
CCU61:CC61IND	from	CAN0:INT(12)	T12 capture input 61
CCU61:CC62IND	from	SCU:E_PDOUT(5)	T12 capture input 62
CCU61:CCPOS0A	from	P00.7:IN	Hall capture input 0
CCU61:CCPOS1A	from	P00.8:IN	Hall capture input 1
CCU61:CCPOS2A	from	P00.9:IN	Hall capture input 2
CCU61:CCPOS0B	from	CCU60:SR(2)	Hall capture input 0
CCU61:CCPOS1B	from	P40.6:IN	Hall capture input 1
CCU61:CCPOS2B	from	P40.8:IN	Hall capture input 2
CCU61:CCPOS0C	from	P33.7:IN	Hall capture input 0
CCU61:CCPOS1C	from	P33.6:IN	Hall capture input 1
CCU61:CCPOS2C	from	P33.5:IN	Hall capture input 2
CCU61:CCPOS0D	from	P40.5:IN	Hall capture input 0
CCU61:CCPOS1D	from	P40.7:IN	Hall capture input 1
CCU61:CCPOS2D	from	P40.9:IN	Hall capture input 2
CCU61:COUT60	to	SCU:E_REQ1(1) IOM:MON1(11) IOM:REF1(10) P00.2:ALT(7) P20.11:ALT(7) P33.12:ALT(7)	T12 PWM channel 60
CCU61:COUT61	to	IOM:MON1(12) IOM:REF1(9) P00.4:ALT(7) P20.12:ALT(7) P33.10:ALT(7)	T12 PWM channel 61
CCU61:COUT62	to	IOM:MON1(13) IOM:REF1(8) P00.6:ALT(7) P20.13:ALT(7) P33.8:ALT(7)	T12 PWM channel 62

## Capture/Compare Unit 6 (CCU6)

Table 349 Connections of CCU61 (cont'd)

Interface Signals	connects	Description	
CCU61:COUT63	to	HSPDM:HWRUN(0)	T13 PWM channel 63
		IOM:MON1(7)	
		IOM:REF1(7)	
		P00.10:ALT(7)	
		P00.12:ALT(7)	
		P20.7:ALT(7)	
CCU61:CTRAPA	from	P00.0:IN	Trap input capture
CCU61:CTRAPB	from	CCU61:WHE_N	Trap input capture
CCU61:CTRAPC	from	P33.4:IN	Trap input capture
CCU61:CTRAPD	from	SCU:E_PDOUT(1)	Trap input capture
CCU61:SR(0)	to	HSM:EXT_INT(11)	Service request
CCU61:SR(1)	to	CCU61:T13HRH	Service request
CCU61:SR(2)	to	CCU60:CCPOS0B	Service request
		CCU60:T12HRG	
		CCU60:T13HRG	
CCU61:SR(3)	to	EVADC:G0REQTRB	Service request
		EVADC:G1REQTRB	
		EVADC:G2REQTRB	
		EVADC:G3REQTRB	
		EVADC:G4REQTRB	
		EVADC:G5REQTRB	
		EVADC:G6REQTRB	
		EVADC:G7REQTRB	
		EVADC:G8REQTRB	
		EVADC:G9REQTRB	
		EVADC:G10REQTRB	
		EVADC:G11REQTRB	
CCU61:T12HRA	from	SCU:scu_cctrigo	External timer start 12
CCU61:T13HRA	from	SCU:scu_cctrigo	External timer start 13
CCU61:T12HRB	from	P02.6:IN	External timer start 12
CCU61:T13HRB	from	P02.7:IN	External timer start 13
CCU61:T12HRC	from	P02.8:IN	External timer start 12
CCU61:T13HRC	from	P02.8:IN	External timer start 13
CCU61:T12HRD	from	GTM:CCU6_TRIG(2)	External timer start 12
CCU61:T13HRD	from	GTM:CCU6_TRIG(3)	External timer start 13
CCU61:T12HRE	from	P00.11:IN	External timer start 12
CCU61:T13HRE	from	CAN0:INT(15)	External timer start 13
CCU61:T12HRF	from	GPT120:T6OFL	External timer start 12

## Capture/Compare Unit 6 (CCU6)

**Table 349 Connections of CCU61 (cont'd)**

Interface Signals	connects		Description
CCU61:T13HRF	from	GPT120:T6OFL	External timer start 13
CCU61:T12HRG	from	CCU60:SR(2)	External timer start 12
CCU61:T13HRG	from	CCU60:SR(2)	External timer start 13
CCU61:T12HRH	from	SCU:E_PDOUT(1)	External timer start 12
CCU61:T13HRH	from	CCU61:SR(1)	External timer start 13
CCU61:WHE_N	to	CCU61:CTRAPB	Set wrong hall event negative

## 27.4 Revision History

**Table 350 Revision History**

Reference	Change to Previous Version	Comment
V3.0.0	No change	

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**General Purpose Timer Unit (GPT12)**

## 28 General Purpose Timer Unit (GPT12)

This chapter describes the specific properties of the product TC39x-B, which is a member of the product family TC3XX.

The functionality of the GPT12 is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

### 28.1 TC39x-B Specific Register Set

**Table 351 Register Address Space - GPT12**

Module	Base Address	End Address	Note
GPT120	F0001800 <sub>H</sub>	F00018FF <sub>H</sub>	FPI slave interface

#### Register Overview Table

See corresponding AURIX™ TC3xx Platform family specification.

### 28.2 TC39x-B Specific Registers

No deviations from the Family Spec

**General Purpose Timer Unit (GPT12)****28.3 Connectivity****Table 352 Connections of GPT120**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
GPT120:CAPINA	from	P13.2:IN	Trigger input to capture value of timer T5 into CAPREL register
GPT120:CAPINB	from	SCU:scu_pdrout(6)	Trigger input to capture value of timer T5 into CAPREL register
GPT120:T2EUDA	from	P00.8:IN	Count direction control input of timer T2
GPT120:T3EUDA	from	P02.7:IN	Count direction control input of core timer T3
GPT120:T4EUDA	from	P00.9:IN	Count direction control input of timer T4
GPT120:T5EUDA	from	P21.6:IN	Count direction control input of timer T5
GPT120:T6EUDA	from	P20.0:IN	Count direction control input of core timer T6
GPT120:T2EUDB	from	P33.6:IN	Count direction control input of timer T2
GPT120:T3EUDB	from	P10.7:IN	Count direction control input of core timer T3
GPT120:T4EUDB	from	P33.5:IN	Count direction control input of timer T4
GPT120:T5EUDB	from	P10.1:IN	Count direction control input of timer T5
GPT120:T6EUDB	from	P10.0:IN	Count direction control input of core timer T6
GPT120:T2INA	from	P00.7:IN	Trigger/gate input of timer T2
GPT120:T3INA	from	P02.6:IN	Trigger/gate input of core timer T3
GPT120:T4INA	from	P02.8:IN	Trigger/gate input of timer T4
GPT120:T5INA	from	P21.7:IN	Trigger/gate input of timer T5
GPT120:T6INA	from	P20.3:IN	Trigger/gate input of core timer T6
GPT120:T2INB	from	P33.7:IN	Trigger/gate input of timer T2
GPT120:T3INB	from	P10.4:IN	Trigger/gate input of core timer T3
GPT120:T4INB	from	P10.8:IN	Trigger/gate input of timer T4
GPT120:T5INB	from	P10.3:IN	Trigger/gate input of timer T5
GPT120:T6INB	from	P10.2:IN	Trigger/gate input of core timer T6
GPT120:T3INC	from	SCU:scu_pdrout(4)	Trigger/gate input of core timer T3
GPT120:T6OFL	to	CCU60:T12HRF CCU60:T13HRF CCU61:T12HRF CCU61:T13HRF	Overflow/underflow signal of timer T6
GPT120:T3OUT	to	SCU:ext_req_in(42) P10.6:ALT(4) P21.6:ALT(7)	External output for overflow/underflow detection of core timer T3
GPT120:T6OUT	to	SCU:ext_req_in(52) P10.5:ALT(5) P21.7:ALT(7)	External output for overflow/underflow detection of core timer T6
GPT120:CIRQ_INT	to	INT:gpt120_CIRQ_INT	GPT120 CAPREL Service Request

## General Purpose Timer Unit (GPT12)

**Table 352 Connections of GPT120 (cont'd)**

Interface Signals	connects		Description
GPT120:T2_INT	to	INT:gpt120_T2_INT	GPT120 T2 Overflow/Underflow Service Request
GPT120:T3_INT	to	INT:gpt120_T3_INT	GPT120 T3 Overflow/Underflow Service Request
GPT120:T4_INT	to	INT:gpt120_T4_INT	GPT120 T4 Overflow/Underflow Service Request
GPT120:T5_INT	to	INT:gpt120_T5_INT	GPT120 T5 Overflow/Underflow Service Request
GPT120:T6_INT	to	INT:gpt120_T6_INT	GPT120 T6 Overflow/Underflow Service Request

## 28.4 Revision History

**Table 353 Revision History**

Reference	Change to Previous Version	Comment
<b>V2.2.3</b>		
---	No change	
<b>V3.0.0</b>		
-	No change.	
<b>V3.0.1</b>		
-	No functional changes.	-
<b>V3.0.2</b>		
	No functional changes.	

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**Converter Control Block (CONVCTRL)**

## 29 Converter Control Block (CONVCTRL)

This chapter describes the specific properties of the product TC39x-B, which is a member of the product family TC3xx.

The functionality of the CONVCTRL is described in the TC3xx family documentation. The complete product description consists of the family documentation and this product-specific appendix.

### 29.1 TC39x-B-Specific IP Configuration

The functional description describes the features and operating modes of the converter control block in a general way. This section summarizes the configuration that is available in a specific product.

**Table 354 TC39x-B specific configuration of CONVERTER**

Parameter	CONVCTRL
FPI base address	F0025000 <sub>H</sub>
FPI address range	100 <sub>H</sub>
Application Reset and Kernel Reset	Application Reset
Name of the config sector value	CFS Value
CFS value for register VRCFG	000000C3 <sub>H</sub>

### 29.2 TC39x-B Specific Register Set

**Table 355 Register Address Space - CONVERTER**

Module	Base Address	End Address	Note
CONVCTRL	F0025000 <sub>H</sub>	F00250FF <sub>H</sub>	FPI slave interface

#### Register Overview Table

See main family chapter.

### 29.3 TC39x-B Specific Registers

No deviations from the Family Spec

## Converter Control Block (CONVCTRL)

### 29.4 Connectivity

The CONVCTRL is connected to its environment through a number of input and output signals.

**Table 356 Digital Connections for Product TC39x-B**

Signal	Dir.	Source/Destin.	Description
<b>General</b>			
PHSYNC	O	EVADC, EDSADC	Synchronization signal for analog clocks
CC_ALARM	O	SMU	Alarm signal from safety logic

**Table 357 List of CONVERTER Interface Signals**

Interface Signals	I/O	Description
PHSYNC	out	<b>Phase synchronization signal</b>
CC_ALARM	out	<b>Safety Alarm Signal</b>

### 29.5 Revision History

**Table 358 Revision History for the Appendix**

Reference	Change to Previous Version	Comment
V3.0.0		
-	No change	
V3.0.1	No functional change.	

## Enhanced Versatile Analog-to-Digital Converter (EVADC)

### 30 Enhanced Versatile Analog-to-Digital Converter (EVADC)

This chapter describes the specific properties of the product TC39x-B, which is a member of the product family TC3XX.

The functionality of the EVADC is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

#### 30.1 TC39x-B-Specific IP Configuration

The functional description describes the features and operating modes of the A/D Converters in a general way. This section summarizes the configuration that is available in a specific product.

Each converter group is equipped with a separate analog converter module and a dedicated analog input multiplexer.

**Table 359 General Converter Configuration TC39x-B**

Converter Group	Input Channels	Converter Cluster	Common Service Req. Group	Associated Standard Reference Pins <sup>1)</sup>
<b>Primary Groups</b>				
G0	CH0 ... CH7	Primary	C0	$V_{AREF2}, V_{AGND2}$
G1	CH0 ... CH7	Primary	C1	$V_{AREF2}, V_{AGND2}$
G2	CH0 ... CH7	Primary	C0	$V_{AREF2}, V_{AGND2}$
G3	CH0 ... CH7	Primary	C1	$V_{AREF2}, V_{AGND2}$
G4	CH0 ... CH7	Primary	C0	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
G5	CH0 ... CH7	Primary	C1	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
G6	CH0 ... CH7	Primary	C0	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
G7	CH0 ... CH7	Primary	C1	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
<b>Secondary Groups</b>				
G8	CH0 ... CH15	Secondary	C0	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
G9	CH0 ... CH15	Secondary	C1	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
G10	CH0 ... CH15	Secondary	C0	$V_{AREF2}, V_{AGND2}$
G11	CH0 ... CH15	Secondary	C1	$V_{AREF2}, V_{AGND2}$
<b>Fast Compare Channels</b>				
FC0	CH0	FastCompare	C0	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
FC1	CH0	FastCompare	C1	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
FC2	CH0	FastCompare	C0	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
FC3	CH0	FastCompare	C1	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$
FC4	CH0	FastCompare	C0	$V_{AREF2}, V_{AGND2}$
FC5	CH0	FastCompare	C1	$V_{AREF2}, V_{AGND2}$
FC6	CH0	FastCompare	C0	$V_{AREF2}, V_{AGND2}$
FC7	CH0	FastCompare	C1	$V_{AREF2}/V_{AREF3}, V_{AGND2}/V_{AGND3}$

1) The availability of reference pins  $V_{AREF3}/V_{AGND3}$  depends on the device package.

In small packages the respective groups/channels are connected to  $V_{AREF2}/V_{AGND2}$ , in big packages they are connected to  $V_{AREF3}/V_{AGND3}$ .

## Enhanced Versatile Analog-to-Digital Converter (EVADC)

### Synchronization Groups

Up to 4 converter kernels can be connected to synchronization groups to achieve parallel conversion of several input channels.

Not all channels can be synchronized to each other, but certain groups can be formed.

**Table 360** summarizes which kernels can be synchronized for parallel conversions.

**Table 360 Synchronization Groups**

ADC Kernel	Synchr. Group	Master selected by control input Clx <sup>1)</sup>			
		Cl0 <sup>2)</sup>	Cl1	Cl2	Cl3
G0 (Prim.)	A	G0	G1	G2	G3
G1 (Prim.)	A	G1	G0	G2	G3
G2 (Prim.)	A	G2	G0	G1	G3
G3 (Prim.)	A	G3	G0	G1	G2
G4 (Prim.)	B	G4	G5	G6	G7
G5 (Prim.)	B	G5	G4	G6	G7
G6 (Prim.)	B	G6	G4	G5	G7
G7 (Prim.)	B	G7	G4	G5	G6
G8 (Sec.)	C	G8	G9	G10	G11
G9 (Sec.)	C	G9	G8	G10	G11
G10 (Sec.)	C	G10	G8	G9	G11
G11 (Sec.)	C	G11	G8	G9	G10

1) The control input is selected by bitfield STSEL in register GxSYNCTR.

Select the corresponding ready inputs accordingly by bits EVALRx.

2) Control input Cl0 always selects the own control signals of the corresponding ADC kernel. This selection is meant for the synchronization master or for stand-alone operation.

### Hardware Connections Between Groups

Certain groups can forward their result values to Fast Compare channels via the HDI. **Table 361** shows these connections.

**Table 361 Hardware Connections to Fast Compare Channels**

Source Group	Target Channel
G0 (Prim.)	FC0CH0
G1 (Prim.)	FC1CH0
G2 (Prim.)	FC2CH0
G3 (Prim.)	FC3CH0
G4 (Prim.)	FC4CH0
G5 (Prim.)	FC5CH0
G6 (Prim.)	FC6CH0
G7 (Prim.)	FC7CH0

---

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 362 TC39x-B specific configuration of EVADC**

Parameter	EVADC
<b>Number of available primary groups</b>	8
<b>Number of available secondary groups</b>	4
<b>Number of available Fast Compare channels</b>	8
<b>FPI base address</b>	$F0020000_H$
<b>FPI address range</b>	$4000_H$

## 30.2 TC39x-B Specific Register Set

**Table 363 Register Address Space - EVADC**

Module	Base Address	End Address	Note
EVADC	$F0020000_H$	$F0023FFF_H$	FPI slave interface

### Register Overview Table

See main family chapter.

## Enhanced Versatile Analog-to-Digital Converter (EVADC)

### 30.3 Connectivity

The EVADC is connected to its environment through a number of analog input signals and also digital input and output signals. These connections establish communication with other peripherals, with the system blocks, and with external components. The following tables list:

- [Analog Module Connections](#)
- [Digital Module Connections](#)

#### 30.3.1 Analog Module Connections

The EVADC module accepts a number of analog input signals. The analog input multiplexers select the input channels to be converted from the signals available in this product.

**Note:** *If an analog input channel is connected to an I/O port pin, make sure the output driver and/or pull devices and/or the digital input path are disabled during normal operation ( $Px\_PDISC.PDISy = 1$ ). For diagnostic functions (MD, PDD) ports must be configured differently (see family description).*

The exact number of analog input channels and the available connection to port pins depend on the employed product type and package (refer to [Table 359](#) and to the corresponding Data Sheets).

A summary of channels can be found in the table below.

**Note:** *Most analog input pins are also connected either to other channels of the EVADC or to channels of the EDSADC. These connections are listed in column “Overlay”*

#### Special Markings

- Input channels marked “PDD” provide a pull-down device for pull-down diagnostics.  
Note: G9CH3, G10CH3: No PDD because of IO pads, G11CH3: No PDD because already provided by G0CH7.
- Input channels marked “MD” can activate the pullup and pulldown devices for multiplexer diagnostics.  
Note: G10CH1/2: No MD because not supported by P33, G11CH1/2: No MD to avoid influence on G0CH5/6.
- Input channels marked “AL” cannot select the input thresholds (via the Port Driver mode Registers) and, therefore, the strength of pullup and pulldown devices. These inputs are fixed to automotive levels.
- Input channels marked “AltRef” can be selected as an alternate reference voltage for conversions on channels of the same group.
- Input channels marked “FixRef” cannot select an alternate reference voltage, but only the corresponding standard reference voltage.

**Table 364 Analog Input Connections for Product TC39x-B**

Signal	Source	Overlay	Description
<b>Reference Inputs</b>			
$V_{AREF}$	VAREF2/3	-	positive analog reference
$V_{AGND}$	VAGND2/3	-	negative analog reference
<b>Analog Inputs for Group 0 (Primary)</b>			
G0CH0 (AltRef)	AN0	EDS3PA	analog input channel 0 of group 0
G0CH1 (MD, AL)	AN1	EDS3NA	analog input channel 1 of group 0
G0CH2 (MD, AL)	AN2	EDS0PA	analog input channel 2 of group 0
G0CH3	AN3	EDS0NA	analog input channel 3 of group 0

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 364 Analog Input Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Source</b>	<b>Overlay</b>	<b>Description</b>
G0CH4 (FixRef, ARefG11)	AN4	G11CH0	analog input channel 4 of group 0
G0CH5 (FixRef)	AN5	G11CH1	analog input channel 5 of group 0
G0CH6 (FixRef)	AN6	G11CH2	analog input channel 6 of group 0
G0CH7 (PDD, FixRef)	AN7	G11CH3	analog input channel 7 of group 0

**Analog Inputs for Group 1 (Primary)**

G1CH0 (AltRef)	AN8	G11CH4	analog input channel 0 of group 1
G1CH1 (MD, AL)	AN9	G11CH5	analog input channel 1 of group 1
G1CH2 (MD, AL)	AN10	G11CH6	analog input channel 2 of group 1
G1CH3 (PDD)	AN11	G11CH7	analog input channel 3 of group 1
G1CH4	AN12	EDS0PB	analog input channel 4 of group 1
G1CH5	AN13	EDS0NB	analog input channel 5 of group 1
G1CH6	AN14	EDS3PB	analog input channel 6 of group 1
G1CH7	AN15	EDS3NB	analog input channel 7 of group 1

**Analog Inputs for Group 2 (Primary)**

G2CH0 (AltRef)	AN16	FC0CH0	analog input channel 0 of group 2
G2CH1 (MD)	AN17	FC1CH0/SENT10A	analog input channel 1 of group 2
G2CH2 (MD)	AN18	G11CH8/SENT11A	analog input channel 2 of group 2
G2CH3 (PDD)	AN19	G11CH9/SENT12A	analog input channel 3 of group 2
G2CH4	AN20	EDS2PA	analog input channel 4 of group 2
G2CH5	AN21	EDS2NA	analog input channel 5 of group 2
G2CH6	AN22	-	analog input channel 6 of group 2
G2CH7	AN23	-	analog input channel 7 of group 2

**Analog Inputs for Group 3 (Primary)**

G3CH0 (AltRef)	AN24	EDS2PB/SENT0A	analog input channel 0 of group 3
G3CH1 (MD)	AN25	EDS2NB/SENT1A	analog input channel 1 of group 3
G3CH2 (MD)	AN26	G11CH10/SENT2A	analog input channel 2 of group 3
G3CH3 (PDD)	AN27	G11CH11/SENT3A	analog input channel 3 of group 3
G3CH4	AN28	G4CH4/SENT13A	analog input channel 4 of group 3
G3CH5	AN29	G4CH5/SENT14A	analog input channel 5 of group 3
G3CH6	AN30	G4CH6	analog input channel 6 of group 3
G3CH7	AN31	G4CH7	analog input channel 7 of group 3

**Analog Inputs for Group 4 (Primary)**

G4CH0 (AltRef)	AN40	G8CH8	analog input channel 0 of group 4
G4CH1 (MD, AL)	AN41	G8CH9	analog input channel 1 of group 4
G4CH2 (MD, AL)	AN42	G8CH10	analog input channel 2 of group 4
G4CH3 (PDD, FixRef)	AN43	G8CH11	analog input channel 3 of group 4
G4CH4	AN28	G3CH4/SENT13A	analog input channel 4 of group 4

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 364 Analog Input Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Source</b>	<b>Overlay</b>	<b>Description</b>
G4CH5	AN29	G3CH5/SENT14A	analog input channel 5 of group 4
G4CH6	AN30	G3CH6	analog input channel 6 of group 4
G4CH7	AN31	G3CH7	analog input channel 7 of group 4
<b>Analog Inputs for Group 5 (Primary)</b>			
G5CH0 (AltRef)	AN48	-	analog input channel 0 of group 5
G5CH1 (MD, AL)	AN49	-	analog input channel 1 of group 5
G5CH2 (MD, AL)	AN50	EDS9PA	analog input channel 2 of group 5
G5CH3 (PDD)	AN51	EDS9NA	analog input channel 3 of group 5
G5CH4	AN52	EDS6PA	analog input channel 4 of group 5
G5CH5	AN53	EDS6NA	analog input channel 5 of group 5
G5CH6	AN54	EDS6PB/SENT20A	analog input channel 6 of group 5
G5CH7	AN55	EDS6NB/SENT21A	analog input channel 7 of group 5
<b>Analog Inputs for Group 6 (Primary)</b>			
G6CH0 (AltRef)	AN56	-	analog input channel 0 of group 6
G6CH1 (MD, AL)	AN57	-	analog input channel 1 of group 6
G6CH2 (MD, AL)	AN58	EDS10PA	analog input channel 2 of group 6
G6CH3 (PDD)	AN59	EDS10NA	analog input channel 3 of group 6
G6CH4	AN60	EDS7PA	analog input channel 4 of group 6
G6CH5	AN61	EDS7NA	analog input channel 5 of group 6
G6CH6	AN62	EDS7PB/SENT22A	analog input channel 6 of group 6
G6CH7	AN63	EDS7NB/SENT23A	analog input channel 7 of group 6
<b>Analog Inputs for Group 7 (Primary)</b>			
G7CH0 (AltRef)	AN64	SENT24A	analog input channel 0 of group 7
G7CH1 (MD, AL)	AN65	-	analog input channel 1 of group 7
G7CH2 (MD, AL)	AN66	EDS11PA	analog input channel 2 of group 7
G7CH3 (PDD)	AN67	EDS11NA/SENT15A	analog input channel 3 of group 7
G7CH4	AN68	EDS8PA/SENT16A	analog input channel 4 of group 7
G7CH5	AN69	EDS8NA/SENT17A	analog input channel 5 of group 7
G7CH6	AN70	EDS9PB/EDS12PA/ SENT18A	analog input channel 6 of group 7
G7CH7	AN71	EDS9NB/EDS12NA/ SENT19A	analog input channel 7 of group 7
<b>Analog Inputs for Group 8 (Secondary)</b>			
G8CH0 (AltRef)	AN32	G11CH12/SENT4A	analog input channel 0 of group 8
G8CH1 (MD)	AN33	G11CH13/SENT5A	analog input channel 1 of group 8
G8CH2 (MD, AL)	AN34	G11CH14	analog input channel 2 of group 8
G8CH3 (PDD)	AN35	G11CH15	analog input channel 3 of group 8
G8CH4	AN36	EDS1PA/SENT6A	analog input channel 4 of group 8

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 364 Analog Input Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Source</b>	<b>Overlay</b>	<b>Description</b>
G8CH5	AN37	EDS1NA/SENT7A	analog input channel 5 of group 8
G8CH6	AN38	EDS1PB/SENT8A	analog input channel 6 of group 8
G8CH7	AN39	EDS1NB/SENT9A	analog input channel 7 of group 8
G8CH8	AN40	G4CH0 (AltRef)	analog input channel 8 of group 8
G8CH9	AN41	G4CH1 (MD, AL)	analog input channel 9 of group 8
G8CH10	AN42	G4CH2 (MD, AL)	analog input channel 10 of group 8
G8CH11	AN43	G4CH3 (PDD)	analog input channel 11 of group 8
G8CH12	AN44	EDS1PC	analog input channel 12 of group 8
G8CH13	AN45	EDS1NC	analog input channel 13 of group 8
G8CH14	AN46	EDS1PD	analog input channel 14 of group 8
G8CH15	AN47	EDS1ND	analog input channel 15 of group 8

**Analog Inputs for Group 9 (Secondary)**

G9CH0 (AltRef)	P00.12	FC2CH0	analog input channel 0 of group 9
G9CH1 (MD)	P00.11	FC3CH0	analog input channel 1 of group 9
G9CH2 (MD)	P00.10	EDS4PB	analog input channel 2 of group 9
G9CH3	P00.9	EDS4NB	analog input channel 3 of group 9
G9CH4	P00.8	EDS4PA	analog input channel 4 of group 9
G9CH5	P00.7	EDS4NA	analog input channel 5 of group 9
G9CH6	P00.6	-	analog input channel 6 of group 9
G9CH7	P00.5	-	analog input channel 7 of group 9
G9CH8	P00.4	EDS5PB	analog input channel 8 of group 9
G9CH9	P00.3	EDS5NB	analog input channel 9 of group 9
G9CH10	P00.2	EDS5PA	analog input channel 10 of group 9
G9CH11	P00.1	EDS5NA	analog input channel 11 of group 9
G9CH12	P01.5	-	analog input channel 12 of group 9
G9CH13	P01.4	-	analog input channel 13 of group 9
G9CH14	P01.3	-	analog input channel 14 of group 9
G9CH15	P02.11	-	analog input channel 15 of group 9

**Analog Inputs for Group 10 (Secondary)**

G10CH0 (AltRef)	P33.7	-	analog input channel 0 of group 10
G10CH1	P33.6	-	analog input channel 1 of group 10
G10CH2	P33.5	-	analog input channel 2 of group 10
G10CH3	P33.4	-	analog input channel 3 of group 10
G10CH4	P33.3	FC4CH0	analog input channel 4 of group 10
G10CH5	P33.2	FC5CH0	analog input channel 5 of group 10
G10CH6	P33.1	FC6CH0	analog input channel 6 of group 10
G10CH7	P33.0	FC7CH0	analog input channel 7 of group 10
G10CH8	P34.4	-	analog input channel 8 of group 10

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 364 Analog Input Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Source</b>	<b>Overlay</b>	<b>Description</b>
G10CH9	P34.3	-	analog input channel 9 of group 10
G10CH10	P34.2	-	analog input channel 10 of group 10
G10CH11	P34.1	-	analog input channel 11 of group 10
G10CH12	-	-	analog input channel 12 of group 10
G10CH13	-	-	analog input channel 13 of group 10
G10CH14	-	-	analog input channel 14 of group 10
G10CH15	$V_{EDSADC}$	-	Selected supervision signal from the EDSADC

**Analog Inputs for Group 11 (Secondary)**

G11CH0 (AltRef)	AN4	G0CH4	analog input channel 0 of group 11
G11CH1	AN5	G0CH5	analog input channel 1 of group 11
G11CH2	AN6	G0CH6	analog input channel 2 of group 11
G11CH3	AN7	G0CH7	analog input channel 3 of group 11
G11CH4	AN8	G1CH0 (AltRef)	analog input channel 4 of group 11
G11CH5	AN9	G1CH1 (MD, AL)	analog input channel 5 of group 11
G11CH6	AN10	G1CH2 (MD, AL)	analog input channel 6 of group 11
G11CH7	AN11	G1CH3 (PDD)	analog input channel 7 of group 11
G11CH8	AN18	G2CH2(MD)/SENT11A	analog input channel 8 of group 11
G11CH9	AN19	G2CH3(PDD)/SENT12A	analog input channel 9 of group 11
G11CH10	AN26	G3CH2 (MD)/SENT2A	analog input channel 10 of group 11
G11CH11	AN27	G3CH3 (PDD)/SENT3A	analog input channel 11 of group 11
G11CH12	AN32	G8CH0/SENT4A	analog input channel 12 of group 11
G11CH13	AN33	G8CH1 (MD)/SENT5A	analog input channel 13 of group 11
G11CH14	AN34	G8CH2 (MD, AL)	analog input channel 14 of group 11
G11CH15	AN35	G8CH3 (PDD)	analog input channel 15 of group 11

**Analog Inputs for Fast Compare Channels**

FC0CH0	AN16	G2CH0	analog input channel of FC channel 0
FC1CH0	AN17	G2CH1/SENT10A	analog input channel of FC channel 1
FC2CH0	P00.12	G9CH0 (AltRef)	analog input channel of FC channel 2
FC3CH0	P00.11	G9CH1 (MD, AL)	analog input channel of FC channel 3
FC4CH0	P33.3	G10CH4	analog input channel of FC channel 4
FC5CH0	P33.2	G10CH5	analog input channel of FC channel 5
FC6CH0	P33.1	G10CH6	analog input channel of FC channel 6
FC7CH0	P33.0	G10CH7	analog input channel of FC channel 7

**Common Input Signals (x = 0-7, 8-11, z = 0-7)**

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 364 Analog Input Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Source</b>	<b>Overlay</b>	<b>Description</b>
GxCH28, FCzCH28	$V_{ANACOMM}$	-	common reference signal, available to all converters, used for production testing, can be fed to the converters through pin AN11
GxCH29, FCzCH29	$V_{MTS}$	-	module test signal, comparator supply voltage $V_{DDK}$
GxCH30, FCzCH30	$V_{AGND}$	-	negative reference voltage
GxCH31, FCzCH31	$V_{AREF}$	-	positive reference voltage

## Enhanced Versatile Analog-to-Digital Converter (EVADC)

### 30.3.2 Digital Module Connections

The EVADC module accepts a number of digital input signals and generates a number of output signals. This section summarizes the connection of these signals to other on-chip modules or to external resources via port pins.

**Table 365 Digital Connections for Product TC39x-B**

Signal	Dir.	Source/Destin.	Description
<b>Gate Inputs for Primary and Secondary Groups (x = 0-7, 8-11, input line selected via bitfield GTSEL = [yyyy<sub>B</sub>])</b>			
GxREQGTA	I	GTM_adcx_trig0	[0000 <sub>B</sub> ] GTM ADC trigger 0
GxREQGBT	I	GTM_adcx_trig1	[0001 <sub>B</sub> ] GTM ADC trigger 1
GxREQGTC	I	CCU6061 TRIG0	[0010 <sub>B</sub> ] CCU6061 trigger output 0
GxREQGTD	I	CCU6061 TRIG1	[0011 <sub>B</sub> ] CCU6061 trigger output 1
GxREQGTE	I	CCU6061 TRIG2	[0100 <sub>B</sub> ] CCU6061 trigger output 2
GxREQGTF	I	-	[0101 <sub>B</sub> ] Gating input F, group x
GxREQGTG	I	GTM_adcx_trig4	[0110 <sub>B</sub> ] GTM ADC trigger 4
GxREQGTH	I	-	[0111 <sub>B</sub> ] Gating input H, group x
GxREQGTI	I	-	[1000 <sub>B</sub> ] Gating input I, group x
GxREQGTJ	I	-	[1001 <sub>B</sub> ] Gating input J, group x
GxREQGTK	I	GTM_adcx_trig2	[1010 <sub>B</sub> ] GTM ADC trigger 2
GxREQGTL	I	GTM_adcx_trig3	[1011 <sub>B</sub> ] GTM ADC trigger 3
GyREQGTM	I	eru_pdout_y	[1100 <sub>B</sub> ] ERU pattern detection output y (y = 0 - 7)
G8REQGTM	I	eru_pdout_0	[1100 <sub>B</sub> ] ERU pattern detection output 0
G9REQGTM	I	eru_pdout_1	[1100 <sub>B</sub> ] ERU pattern detection output 1
G10REQGTM	I	eru_pdout_2	[1100 <sub>B</sub> ] ERU pattern detection output 2
G11REQGTM	I	eru_pdout_3	[1100 <sub>B</sub> ] ERU pattern detection output 3
GxREQGTN	I	-	[1101 <sub>B</sub> ] Gating input N, group x
GxREQGTO	I	-	[1110 <sub>B</sub> ] Gating input O, group x
GxREQGTP	I	[internal]	[1111 <sub>B</sub> ] Extend inputs to the selected internal trigger source (see GxTRCTR)
GxREQGTYSEL	O	GxREQTRyP <sup>1)</sup>	Selected gating signal of the respective source
<b>Trigger Inputs for Primary and Secondary Groups (x = 0-7, 8-11, input line selected via bitfield XTSEL = [yyyy<sub>B</sub>])</b>			
GxREQTRA	I	CCU60_SR3	[0000 <sub>B</sub> ] CCU60 service request output 3
GxREQTRB	I	CCU61_SR3	[0001 <sub>B</sub> ] CCU61 service request output 3
GxREQTRC	I	HSPDM_adc_trig	[0010 <sub>B</sub> ] HSPDM chirp trigger
GxREQTRD	I	-	[0011 <sub>B</sub> ] Trigger input D, group x
GxREQTRE	I	-	[0100 <sub>B</sub> ] Trigger input E, group x
GxREQTRF	I	-	[0101 <sub>B</sub> ] Trigger input F, group x
GxREQTRG	I	GTM_adcx_trig4	[0110 <sub>B</sub> ] GTM ADC trigger 4

## Enhanced Versatile Analog-to-Digital Converter (EVADC)

Table 365 Digital Connections for Product TC39x-B (cont'd)

Signal	Dir.	Source/Destin.	Description
GyREQTRH	I	eru_iout_y	[0111 <sub>B</sub> ] ERU interrupt output y (y = 0 - 7)
G8REQTRH	I	eru_iout_0	[0111 <sub>B</sub> ] ERU interrupt output 0
G9REQTRH	I	eru_iout_1	[0111 <sub>B</sub> ] ERU interrupt output 1
G10REQTRH	I	eru_iout_2	[0111 <sub>B</sub> ] ERU interrupt output 2
G11REQTRH	I	eru_iout_3	[0111 <sub>B</sub> ] ERU interrupt output 3
GxREQTRI	I	GTM_adcx_trig0	[1000 <sub>B</sub> ] GTM ADC trigger 0
GxREQTRJ	I	GTM_adcx_trig1	[1001 <sub>B</sub> ] GTM ADC trigger 1
GxREQTRK	I	GTM_adcx_trig2	[1010 <sub>B</sub> ] GTM ADC trigger 2
GxREQTRL	I	GTM_adcx_trig3	[1011 <sub>B</sub> ] GTM ADC trigger 3
GxREQTRM	I	vadc_gxsr1	[1100 <sub>B</sub> ] Service request 1, group x
GxREQTRN	I	vadc_c0sr1	[1101 <sub>B</sub> ] Service request 1, common group 0
GxREQTRO	I	vadc_c1sr1	[1110 <sub>B</sub> ] Service request 1, common group 1
GxREQTRYP	I	GxREQGTYSEL <sup>1)</sup>	[1111 <sub>B</sub> ] Extend triggers to selected gating input of the respective source
GxREQTRYSEL	O	-	Selected trigger signal of the respective source

Trigger/Gate Inputs for Fast Compare Channels (z = 0-7, input line selected via bitfield XTSEL = [yyyy<sub>B</sub>])

FCzREQTRA	I	-	[0000 <sub>B</sub> ] Trigger input A
FCzREQTRB	I	-	[0001 <sub>B</sub> ] Trigger input B
FCzREQTRC	I	-	[0010 <sub>B</sub> ] Trigger input C
FCzREQTRD	I	-	[0011 <sub>B</sub> ] Trigger input D
FCzREQTRE	I	-	[0100 <sub>B</sub> ] Trigger input E
FCzREQTRF	I	-	[0101 <sub>B</sub> ] Trigger input F
FCzREQTRG	I	-	[0110 <sub>B</sub> ] Trigger input G
FCzREQTRH	I	-	[0111 <sub>B</sub> ] Trigger input H
FCzREQTRI	I	GTM_adcz_trig0	[1000 <sub>B</sub> ] GTM ADCz trigger 0
FCzREQTRJ	I	GTM_adcz_trig1	[1001 <sub>B</sub> ] GTM ADCz trigger 1
FCzREQTRK	I	GTM_adcz_trig2	[1010 <sub>B</sub> ] GTM ADCz trigger 2
FC0REQTRL	I	GTM_adc8_trig3	[1011 <sub>B</sub> ] GTM ADC8 trigger 3
FC1REQTRL	I	GTM_adc9_trig3	[1011 <sub>B</sub> ] GTM ADC9 trigger 3
FC2REQTRL	I	GTM_adc8_trig1	[1011 <sub>B</sub> ] GTM ADC8 trigger 1
FC3REQTRL	I	GTM_adc9_trig1	[1011 <sub>B</sub> ] GTM ADC9 trigger 1
FC4REQTRL	I	GTM_adc10_trig3	[1011 <sub>B</sub> ] GTM ADC10 trigger 3
FC5REQTRL	I	GTM_adc11_trig3	[1011 <sub>B</sub> ] GTM ADC11 trigger 3
FC6REQTRL	I	GTM_adc10_trig1	[1011 <sub>B</sub> ] GTM ADC10 trigger 1
FC7REQTRL	I	GTM_adc11_trig1	[1011 <sub>B</sub> ] GTM ADC11 trigger 1
FC0REQTRM	I	GTM_adc8_trig4	[1100 <sub>B</sub> ] GTM ADC8 trigger 4
FC1REQTRM	I	GTM_adc9_trig4	[1100 <sub>B</sub> ] GTM ADC9 trigger 4

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 365 Digital Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Dir.</b>	<b>Source/Destin.</b>	<b>Description</b>
FC2REQTRM	I	GTM_adc8_trig2	[1100 <sub>B</sub> ] GTM ADC8 trigger 2
FC3REQTRM	I	GTM_adc9_trig2	[1100 <sub>B</sub> ] GTM ADC9 trigger 2
FC4REQTRM	I	GTM_adc10_trig4	[1100 <sub>B</sub> ] GTM ADC10 trigger 4
FC5REQTRM	I	GTM_adc10_trig4	[1100 <sub>B</sub> ] GTM ADC10 trigger 4
FC6REQTRM	I	GTM_adc11_trig2	[1100 <sub>B</sub> ] GTM ADC11 trigger 2
FC7REQTRM	I	GTM_adc11_trig2	[1100 <sub>B</sub> ] GTM ADC11 trigger 2
FCzREQTRN	I	-	[1101 <sub>B</sub> ] Trigger input N
FCzREQTRO	I	-	[1110 <sub>B</sub> ] Trigger input O
FCzREQTRP	I	-	[1111 <sub>B</sub> ] Trigger input P

**Global Signals and Service Request Lines For Primary/Secondary Groups: x = 0-7, 8-11, for Fast Compare Channels: z = 0-7**

GxDATA[20:0]	O	Fast Compare channel, RIF, GTM	Result values written to RES15
GxWR	O	Fast Compare channel, RIF, GTM	Write signal for GxDATA
EMUX00	O	P02.6, P33.3	Control of external analog multiplexer interface 0
EMUX01	O	P02.7, P33.2	
EMUX02	O	P02.8, P33.1	
EMUX10	O	P00.6, P33.6	Control of external analog multiplexer interface 1
EMUX11	O	P00.7, P33.5	
EMUX12	O	P00.8, P33.4	
CBFLOUT0	O	GTM_CDTM0_DTM03, GTM_CDTM0_DTM43, GTM_MCSSTAT8, GTM_TIM1_CH0, GTM_TIM1_CH4, GTM_TIM2_CH0, GTM_TIM2_CH4	Common boundary flag output 0
CBFLOUT1	O	GTM_CDTM1_DTM03, GTM_CDTM1_DTM43, GTM_MCSSTAT9, GTM_TIM1_CH1, GTM_TIM1_CH5, GTM_TIM2_CH1, GTM_TIM2_CH5	Common boundary flag output 1
CBFLOUT2	O	GTM_CDTM2_DTM03, GTM_CDTM2_DTM43, GTM_MCSSTAT10, GTM_TIM1_CH2, GTM_TIM1_CH6, GTM_TIM2_CH2, GTM_TIM2_CH6	Common boundary flag output 2

## Enhanced Versatile Analog-to-Digital Converter (EVADC)

Table 365 Digital Connections for Product TC39x-B (cont'd)

Signal	Dir.	Source/Destin.	Description
CBFLOUT3	O	GTM_CDTM3_DTM03, GTM_CDTM3_DTM43, GTM_MCSSTAT11, GTM_TIM1_CH3, GTM_TIM1_CH7, GTM_TIM2_CH3, GTM_TIM2_CH7	Common boundary flag output 3
FC0BFLOUT	O	CCU60_CTRAPC, P00.5, P33.4	Boundary flag output of FC channel 0
FC0BFL	O	GTM_MCSSTAT0, GTM_tim_0_muxin_0_0 GTM_tim_1_muxin_0_0 GTM_tim_2_muxin_0_0 GTM_tim_4_muxin_0_0	Boundary flag level of FC channel 0
FC0BFSEL	I	GTM_MCSTRIG1	Boundary flag (FC channel 0) source select
FC0BFDAT	I	GTM_MCSTRIG0	Boundary flag (FC channel 0) alternate data
FC1BFLOUT	O	P10.1, P33.6	Boundary flag output of FC channel 1
FC1BFL	O	GTM_MCSSTAT1, GTM_tim_0_muxin_1_0 GTM_tim_1_muxin_1_0 GTM_tim_2_muxin_1_0 GTM_tim_4_muxin_1_0	Boundary flag level of FC channel 1
FC1BFSEL	I	GTM_MCSTRIG3	Boundary flag (FC channel 1) source select
FC1BFDAT	I	GTM_MCSTRIG2	Boundary flag (FC channel 1) alternate data
FC2BFLOUT	O	P00.7, P33.0, P33.5	Boundary flag output of FC channel 2
FC2BFL	O	GTM_MCSSTAT2, GTM_tim_0_muxin_2_0 GTM_tim_1_muxin_2_0 GTM_tim_2_muxin_2_0 GTM_tim_4_muxin_2_0	Boundary flag level of FC channel 2
FC2BFSEL	I	GTM_MCSTRIG5	Boundary flag (FC channel 2) source select
FC2BFDAT	I	GTM_MCSTRIG4	Boundary flag (FC channel 2) alternate data
FC3BFLOUT	O	P10.2, P33.2, P33.7	Boundary flag output of FC channel 3
FC3BFL	O	GTM_MCSSTAT3, GTM_tim_0_muxin_3_0 GTM_tim_1_muxin_3_0 GTM_tim_2_muxin_3_0 GTM_tim_3_muxin_3_0 GTM_tim_4_muxin_3_0	Boundary flag level of FC channel 3
FC3BFSEL	I	GTM_MCSTRIG7	Boundary flag (FC channel 3) source select
FC3BFDAT	I	GTM_MCSTRIG6	Boundary flag (FC channel 3) alternate data

## Enhanced Versatile Analog-to-Digital Converter (EVADC)

Table 365 Digital Connections for Product TC39x-B (cont'd)

Signal	Dir.	Source/Destin.	Description
FC4BFLOUT	O	GTM_CDTM4_DTM03, GTM_CDTM4_DTM43, P00.4, P01.8, P33.1	Boundary flag output of FC channel 4
FC4BFL	O	GTM_MCSSTAT4, GTM_tim_0_muxin_4_0 GTM_tim_1_muxin_4_0 GTM_tim_2_muxin_4_0 GTM_tim_3_muxin_4_0 GTM_tim_4_muxin_4_0	Boundary flag level of FC channel 4
FC4BFSEL	I	GTM_MCSTRIG9	Boundary flag (FC channel 4) source select
FC4BFDAT	I	GTM_MCSTRIG8	Boundary flag (FC channel 4) alternate data
FC5BFLOUT	O	GTM_CDTM5_DTM43, P00.6, P01.9, P33.3	Boundary flag output of FC channel 5
FC5BFL	O	GTM_MCSSTAT5, GTM_tim_0_muxin_5_0 GTM_tim_1_muxin_5_0 GTM_tim_2_muxin_5_0 GTM_tim_3_muxin_5_0 GTM_tim_4_muxin_5_0	Boundary flag level of FC channel 5
FC5BFSEL	I	GTM_MCSTRIG11	Boundary flag (FC channel 5) source select
FC5BFDAT	I	GTM_MCSTRIG10	Boundary flag (FC channel 5) alternate data
FC6BFLOUT	O	GTM_CDTM6_DTM43, P01.10, P10.0, P34.4	Boundary flag output of FC channel 6
FC6BFL	O	GTM_MCSSTAT6, GTM_tim_0_muxin_6_0 GTM_tim_1_muxin_6_0 GTM_tim_2_muxin_6_0 GTM_tim_3_muxin_6_0 GTM_tim_4_muxin_6_0	Boundary flag level of FC channel 6
FC6BFSEL	I	GTM_MCSTRIG13	Boundary flag (FC channel 6) source select
FC6BFDAT	I	GTM_MCSTRIG12	Boundary flag (FC channel 6) alternate data
FC7BFLOUT	O	P01.11, P10.6, P34.5	Boundary flag output of FC channel 7
FC7BFL	O	GTM_MCSSTAT7, GTM_tim_0_muxin_7_0 GTM_tim_1_muxin_7_0 GTM_tim_2_muxin_7_0 GTM_tim_3_muxin_7_0 GTM_tim_4_muxin_7_0	Boundary flag level of FC channel 7
FC7BFSEL	I	GTM_MCSTRIG15	Boundary flag (FC channel 7) source select
FC7BFDAT	I	GTM_MCSTRIG14	Boundary flag (FC channel 7) alternate data
G0SR0 - G1SR0	O	ICU, HSM	Service request 0 of group 0 - 1
G2SR0 - G11SR0	O	ICU	Service request 0 of group 2 - 11
G0SR1 - G1SR1	O	ICU, HSM	Service request 1 of group 0 - 1

**Enhanced Versatile Analog-to-Digital Converter (EVADC)**
**Table 365 Digital Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Dir.</b>	<b>Source/Destin.</b>	<b>Description</b>
G2SR1 - G11SR1	O	ICU	Service request 1 of group 2 - 11
GxSR2	O	ICU	Service request 2 of group x
GxSR3	O	ICU	Service request 3 of group x
FCzSR0	O	ICU	Service request 0 of FC channel z
C0SR0	O	ICU, GTM_TIM0_CH0, GTM_TIM1_CH4, GTM_TIM2_CH0	Service request 0 of common block 0
C0SR1	O	ICU, GTM_TIM0_CH2, GTM_TIM1_CH6, GTM_TIM2_CH2	Service request 1 of common block 0
C0SR2	O	ICU, GTM_TIM0_CH4, GTM_TIM1_CH0, GTM_TIM2_CH4	Service request 2 of common block 0
C0SR3	O	ICU, GTM_TIM0_CH6, GTM_TIM1_CH2, GTM_TIM2_CH6	Service request 3 of common block 0
C1SR0	O	ICU, GTM_TIM0_CH1, GTM_TIM1_CH5, GTM_TIM2_CH1	Service request 0 of common block 1
C1SR1	O	ICU, GTM_TIM0_CH3, GTM_TIM1_CH7, GTM_TIM2_CH3	Service request 1 of common block 1
C1SR2	O	ICU, GTM_TIM0_CH5, GTM_TIM1_CH1, GTM_TIM2_CH5	Service request 2 of common block 1
C1SR3	O	ICU, GTM_TIM0_CH7, GTM_TIM1_CH3, GTM_TIM2_CH7	Service request 3 of common block 1

**System-Internal Connections (x = 0-7, 8-11)**

PHSYNC	I	Phase synchronizer	Synchronization signal for analog clocks
otgb0[15:0]	O	OTGM	Alternate trigger buses for additional trace signals
otgb1[15:0]	O	OTGM	indicating the input signal sample phase (see OCS)

1) Internal signal connection.

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**Enhanced Versatile Analog-to-Digital Converter (EVADC)**

### 30.4 Revision History

This is a summary of the modifications that have been applied to this chapter.

**Table 366 Revision History**

Reference	Change to Previous Version	Comment
V3.0.0		
<a href="#">Page 4</a>	Clarify functionality of channel CH29 (see end of table).	
V3.0.1		
-	No functional changes.	-
V3.0.2		
-	No functional changes.	-
V3.0.3		
-	No functional changes.	-
V3.0.4		
-	No functional changes.	-
V3.0.5		
-	No functional changes.	-

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

### 31 Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

This chapter describes the specific properties of the product TC39x-B, which is a member of the product family TC3XX.

The functionality of the EDSADC is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

#### 31.1 TC39x-B-Specific IP Configuration

The functional description describes the features and operating modes of the A/D Converters in a general way. This section summarizes the configuration that is available in a specific product.

The EDSADC features a number of channels, some with an analog input multiplexer.

**Table 367 General Converter Configuration TC39x-B**

Channel	Analog Inputs	Digital Inputs	Reference Pins	Notes
0	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
1	4	2	$V_{AREF1}, V_{AGND1}$	4:1 analog multiplexer
2	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
3	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
4	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
5	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
6	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
7	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
8	1	2	$V_{AREF1}, V_{AGND1}$	
9	2	2	$V_{AREF1}, V_{AGND1}$	2:1 analog multiplexer
10	1	2	$V_{AREF1}, V_{AGND1}$	
11	1	2	$V_{AREF1}, V_{AGND1}$	
12	1	2	$V_{AREF1}, V_{AGND1}$	
13	1	2	$V_{AREF1}, V_{AGND1}$	

**Table 368 TC39x-B specific configuration of EDSADC**

Parameter	EDSADC
Number of available channels	14
FPI base address	$F0024000_H$
FPI address range	$1000_H$
Application- or Kernel Reset	Application Reset

#### 31.2 TC39x-B Specific Register Set

**Table 369 Register Address Space - EDSADC**

Module	Base Address	End Address	Note
EDSADC	$F0024000_H$	$F0024FFF_H$	FPI slave interface

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**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)****Register Overview Table**

See main family chapter.

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

### 31.3 Connectivity

The EDSADC is connected to its environment through a number of analog input signals and also digital input and output signals. These connections establish communication with other peripherals, with the system blocks, and with external components. The following tables list:

- [Analog Module Connections](#)
- [Digital Module Connections](#)

#### 31.3.1 Analog Module Connections

The EDSADC module accepts a positive and a negative analog input signal to be used as a differential input. Each analog input can also be used in single-ended mode.

**Note:** *If an analog input channel is connected to an I/O port pin, make sure the output driver and/or the digital input path are disabled during normal operation ( $Px\_PDISC.PDISy = 1$ ).*

The exact number of analog input channels and the available connection to port pins depend on the employed product type and package (refer to [Table 367](#) and to the corresponding Data Sheets).

A summary of channels can be found in the table below.

**Note:** *Most analog input pins are also connected to channels of the EVADC. These connections are listed in column “Overlay”*

**Table 370 Analog Input Connections for Product TC39x-B**

Signal	Source	Overlay	Description
<b>Reference Inputs</b>			
$V_{AREF}$	VAREF1	-	positive analog reference
$V_{AGND}$	VAGND1	-	negative analog reference
<b>Analog Inputs (input line selected via bitfield INMUX = [yy<sub>B</sub>])</b>			
EDS0PA	AN2	G0CH2 (MD)	[00 <sub>B</sub> ] positive analog input of channel 0, pin A
EDS0NA	AN3	G0CH3	[00 <sub>B</sub> ] negative analog input of channel 0, pin A
EDS0PB	AN12	G1CH4	[01 <sub>B</sub> ] positive analog input of channel 0, pin B
EDS0NB	AN13	G1CH5	[01 <sub>B</sub> ] negative analog input of channel 0, pin B
EDS1PA	AN36	G8CH4/SENT6A	[00 <sub>B</sub> ] positive analog input of channel 1, pin A
EDS1NA	AN37	G8CH5/SENT7A	[00 <sub>B</sub> ] negative analog input of channel 1, pin A
EDS1PB	AN38	G8CH6/SENT8A	[01 <sub>B</sub> ] positive analog input of channel 1, pin B
EDS1NB	AN39	G8CH7/SENT9A	[01 <sub>B</sub> ] negative analog input of channel 1, pin B
EDS1PC	AN44	G8CH12	[10 <sub>B</sub> ] positive analog input of channel 1, pin C
EDS1NC	AN45	G8CH13	[10 <sub>B</sub> ] negative analog input of channel 1, pin C
EDS1PD	AN46	G8CH14	[11 <sub>B</sub> ] positive analog input of channel 1, pin D
EDS1ND	AN47	G8CH15	[11 <sub>B</sub> ] negative analog input of channel 1, pin D
EDS2PA	AN20	G2CH4	[00 <sub>B</sub> ] positive analog input of channel 2, pin A
EDS2NA	AN21	G2CH5	[00 <sub>B</sub> ] negative analog input of channel 2, pin A
EDS2PB	AN24	G3CH0 (AltRef)/SENT0A	[01 <sub>B</sub> ] positive analog input of channel 2, pin B

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

Table 370 Analog Input Connections for Product TC39x-B (cont'd)

Signal	Source	Overlay	Description
EDS2NB	AN25	G3CH1 (MD) / SENT1A	[01 <sub>B</sub> ] negative analog input of channel 2, pin B
EDS3PA	AN0	G0CH0 (AltRef)	[00 <sub>B</sub> ] positive analog input of channel 3, pin A
EDS3NA	AN1	G0CH1 (MD)	[00 <sub>B</sub> ] negative analog input of channel 3, pin A
EDS3PB	AN14	G1CH6	[01 <sub>B</sub> ] positive analog input of channel 3, pin B
EDS3NB	AN15	G1CH7	[01 <sub>B</sub> ] negative analog input of channel 3, pin B
EDS4PA	P00.8	G9CH4	[00 <sub>B</sub> ] positive analog input of channel 4, pin A
EDS4NA	P00.7	G9CH5	[00 <sub>B</sub> ] negative analog input of channel 4, pin A
EDS4PB	P00.10	G9CH2	[01 <sub>B</sub> ] positive analog input of channel 4, pin B
EDS4NB	P00.9	G9CH3	[01 <sub>B</sub> ] negative analog input of channel 4, pin B
EDS5PA	P00.2	G9CH10	[00 <sub>B</sub> ] positive analog input of channel 5, pin A
EDS5NA	P00.1	G9CH11	[00 <sub>B</sub> ] negative analog input of channel 5, pin A
EDS5PB	P00.4	G9CH8	[01 <sub>B</sub> ] positive analog input of channel 5, pin B
EDS5NB	P00.3	G9CH9	[01 <sub>B</sub> ] negative analog input of channel 5, pin B
EDS6PA	AN52	G5CH4	[00 <sub>B</sub> ] positive analog input of channel 6, pin A
EDS6NA	AN53	G5CH5	[00 <sub>B</sub> ] negative analog input of channel 6, pin A
EDS6PB	AN54	G5CH6	[01 <sub>B</sub> ] positive analog input of channel 6, pin B
EDS6NB	AN55	G6CH7	[01 <sub>B</sub> ] negative analog input of channel 6, pin B
EDS7PA	AN60	G6CH4	[00 <sub>B</sub> ] positive analog input of channel 7, pin A
EDS7NA	AN61	G6CH5	[00 <sub>B</sub> ] negative analog input of channel 7, pin A
EDS7PB	AN62	G6CH6	[01 <sub>B</sub> ] positive analog input of channel 7, pin B
EDS7NB	AN63	G6CH7	[01 <sub>B</sub> ] negative analog input of channel 7, pin B
EDS8PA	AN68	G7CH4 / SENT16A	[00 <sub>B</sub> ] positive analog input of channel 8
EDS8NA	AN69	G7CH5 / SENT17A	[00 <sub>B</sub> ] negative analog input of channel 8
EDS9PA	AN50	G5CH2 (MD)	[00 <sub>B</sub> ] positive analog input of channel 9
EDS9NA	AN51	G5CH3 (PDD)	[00 <sub>B</sub> ] negative analog input of channel 9
EDS9PB	AN70	G7CH6 / EDS12PA / SENT18A	[01 <sub>B</sub> ] positive analog input of channel 9
EDS9NB	AN71	G7CH7 / EDS12NA / SENT19A	[01 <sub>B</sub> ] negative analog input of channel 9
EDS10PA	AN58	G6CH2 (MD)	[00 <sub>B</sub> ] positive analog input of channel 10
EDS10NA	AN59	G6CH3 (PDD)	[00 <sub>B</sub> ] negative analog input of channel 10
EDS11PA	AN66	G7CH2 (MD)	[00 <sub>B</sub> ] positive analog input of channel 11
EDS11NA	AN67	G7CH3 (PDD) / SENT15A	[00 <sub>B</sub> ] negative analog input of channel 11

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**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 370 Analog Input Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Source</b>	<b>Overlay</b>	<b>Description</b>
EDS12PA	AN70	G7CH6 / EDS9PB / SENT18A	[00 <sub>B</sub> ] positive analog input of channel 12
EDS12NA	AN71	G7CH7 / EDS9NB / SENT19A	[00 <sub>B</sub> ] negative analog input of channel 12
EDS13PA	AN72	-	[00 <sub>B</sub> ] positive analog input of channel 13
EDS13NA	AN73	-	[00 <sub>B</sub> ] negative analog input of channel 13

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

### 31.3.2 Digital Module Connections

The EDSADC module accepts a number of digital input signals and generates a number of output signals. This section summarizes the connection of these signals to other on-chip modules or to external resources via port pins.

**Note:** *The input signals ITRxA ... ITRxP can be used for both trigger functions and gating functions.  
The trigger input line is selected via bitfield TRSEL = [yyyy<sub>B</sub>], the data input line (DSDIN...) is selected via bitfield DSRCEX = [yyy<sub>B</sub>], the clock input line (DSCIN...) is selected via bitfield CSRCEX = [yyy<sub>B</sub>].*

**Table 371 Digital Connections for Product TC39x-B**

Signal	Dir.	Source/Destin.	Description
<b>Channel 0</b>			
DSDIN0A	I	P00.12	[00X <sub>B</sub> ] Data bitstream channel 0 input A
DSDIN0B	I	P33.6	[01X <sub>B</sub> ] Data bitstream channel 0 input B
DSDIN0C	I	-	[10X <sub>B</sub> ] Data bitstream channel 0 input C
DSDIN0D	I	-	[11X <sub>B</sub> ] Data bitstream channel 0 input D
DSCIN0A	I	P00.11	[011 <sub>B</sub> ] Modulator clock channel 0 input A
DSCIN0B	I	P33.5	[100 <sub>B</sub> ] Modulator clock channel 0 input B
DSCIN0C	I	-	[101 <sub>B</sub> ] Modulator clock channel 0 input C
DSCOUT0	O	P00.11, P33.5	Modulator clock channel 0 output
ITR0A	I	GTM:DSADC_TRIG0(0)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR0B	I	GTM:DSADC_TRIG1(0)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR0C	I	GTM:ADC_TRIG0(0)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR0D	I	GTM:ADC_TRIG1(0)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR0E	I	P33.0	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR0F	I	P33.4	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR0G	I	SCU_PDOUT0	[0110 <sub>B</sub> ] ERU pattern detection output 0
ITR0H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 0, input H
ITR0I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 0, input I
ITR0J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 0, input J
ITR0K	I	GTM:ADC_TRIG2(0)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR0L	I	GTM:ADC_TRIG3(0)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR0M	I	GTM:DSADC_TRIG2(0)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR0N	I	GTM:DSADC_TRIG3(0)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR0O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 0, input O
ITR0P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 0, input P
SRM0	O	ICU, GTM:DSADC_SRM(0)	Service request output main channel 0
SRA0	O	ICU	Service request output aux. channel 0
SAUL0	O	GTM:DSADC_SAUL(0)	Signal above upper limit ind., channel 0
SBLL0	O	GTM:DSADC_SBLL(0)	Signal below lower limit ind., channel 0
SWIB0	O	GTM:DTMA0(2)	Signal within band ind., channel 0

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

Signal	Dir.	Source/Destin.	Description
DATA0[16:0]	O	GTM	Result values of channel 0
WR0	O	GTM	Write signal for DATA0
<b>Channel 1</b>			
DSDIN1A	I	P00.10	[00X <sub>B</sub> ] Data bitstream channel 1 input A
DSDIN1B	I	P33.4	[01X <sub>B</sub> ] Data bitstream channel 1 input B
DSDIN1C	I	-	[10X <sub>B</sub> ] Data bitstream channel 1 input C
DSDIN1D	I	-	[11X <sub>B</sub> ] Data bitstream channel 1 input D
DSCIN1A	I	P00.9	[011 <sub>B</sub> ] Modulator clock channel 1 input A
DSCIN1B	I	P33.3	[100 <sub>B</sub> ] Modulator clock channel 1 input B
DSCIN1C	I	-	[101 <sub>B</sub> ] Modulator clock channel 1 input C
DSCOUT1	O	P00.9, P33.3	Modulator clock channel 1 output
ITR1A	I	GTM:DSADC_TRIG0(1)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR1B	I	GTM:DSADC_TRIG1(1)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR1C	I	GTM:ADC_TRIG0(1)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR1D	I	GTM:ADC_TRIG1(1)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR1E	I	P33.1	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR1F	I	P33.5	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR1G	I	SCU_PDOUT1	[0110 <sub>B</sub> ] ERU pattern detection output 1
ITR1H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 1, input H
ITR1I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 1, input I
ITR1J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 1, input J
ITR1K	I	GTM:ADC_TRIG2(1)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR1L	I	GTM:ADC_TRIG3(1)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR1M	I	GTM:DSADC_TRIG2(1)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR1N	I	GTM:DSADC_TRIG3(1)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR1O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 1, input O
ITR1P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 1, input P
SRM1	O	ICU, GTM:DSADC_SRM(1)	Service request output main channel 1
SRA1	O	ICU	Service request output aux. channel 1
SAUL1	O	GTM:DSADC_SAUL(1)	Signal above upper limit ind., channel 1
SBLL1	O	GTM:DSADC_SBLL(1)	Signal below lower limit ind., channel 1
SWIB1	O	GTM:DTMA1(2)	Signal within band ind., channel 1
DATA1[16:0]	O	GTM	Result values of channel 1
WR1	O	GTM	Write signal for DATA1
<b>Channel 2</b>			
DSDIN2A	I	P00.6	[00X <sub>B</sub> ] Data bitstream channel 2 input A
DSDIN2B	I	P33.2	[01X <sub>B</sub> ] Data bitstream channel 2 input B
DSDIN2C	I	-	[10X <sub>B</sub> ] Data bitstream channel 2 input C

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

Table 371 Digital Connections for Product TC39x-B (cont'd)

Signal	Dir.	Source/Destin.	Description
DSDIN2D	I	-	[11X <sub>B</sub> ] Data bitstream channel 2 input D
DSCIN2A	I	P00.5	[011 <sub>B</sub> ] Modulator clock channel 2 input A
DSCIN2B	I	P33.1	[100 <sub>B</sub> ] Modulator clock channel 2 input B
DSCIN2C	I	-	[101 <sub>B</sub> ] Modulator clock channel 2 input C
DSCOUT2	O	P00.5, P33.1	Modulator clock channel 2 output
ITR2A	I	GTM:DSADC_TRIG0(2)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR2B	I	GTM:DSADC_TRIG1(2)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR2C	I	GTM:ADC_TRIG0(2)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR2D	I	GTM:ADC_TRIG1(2)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR2E	I	P33.2	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR2F	I	P33.6	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR2G	I	SCU_PDOUT2	[0110 <sub>B</sub> ] ERU pattern detection output 2
ITR2H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 2, input H
ITR2I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 2, input I
ITR2J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 2, input J
ITR2K	I	GTM:ADC_TRIG2(2)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR2L	I	GTM:ADC_TRIG3(2)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR2M	I	GTM:DSADC_TRIG2(2)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR2N	I	GTM:DSADC_TRIG3(2)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR2O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 2, input O
ITR2P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 2, input P
SRM2	O	ICU, GTM:DSADC_SRM(2)	Service request output main channel 2
SRA2	O	ICU	Service request output aux. channel 2
SAUL2	O	GTM:DSADC_SAUL(2)	Signal above upper limit ind., channel 2
SBLL2	O	GTM:DSADC_SBLL(2)	Signal below lower limit ind., channel 2
SWIB2	O	GTM:DTMA2(2)	Signal within band ind., channel 2
DATA2[16:0]	O	GTM	Result values of channel 2
WR2	O	GTM	Write signal for DATA2

## Channel 3

DSDIN3A	I	P00.4	[00X <sub>B</sub> ] Data bitstream channel 3 input A
DSDIN3B	I	P02.8	[01X <sub>B</sub> ] Data bitstream channel 3 input B
DSDIN3C	I	-	[10X <sub>B</sub> ] Data bitstream channel 3 input C
DSDIN3D	I	-	[11X <sub>B</sub> ] Data bitstream channel 3 input D
DSCIN3A	I	P00.3	[011 <sub>B</sub> ] Modulator clock channel 3 input A
DSCIN3B	I	P02.7	[100 <sub>B</sub> ] Modulator clock channel 3 input B
DSCIN3C	I	-	[101 <sub>B</sub> ] Modulator clock channel 3 input C
DSCOUT3	O	P00.3, P02.7	Modulator clock channel 3 output
ITR3A	I	GTM:DSADC_TRIG0(3)	[0000 <sub>B</sub> ] GTM DSADC trigger 0

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

Table 371 Digital Connections for Product TC39x-B (cont'd)

Signal	Dir.	Source/Destin.	Description
ITR3B	I	GTM:DSADC_TRIG1(3)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR3C	I	GTM:ADC_TRIG0(3)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR3D	I	GTM:ADC_TRIG1(3)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR3E	I	P02.8	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR3F	I	P00.9	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR3G	I	SCU_PDOUT3	[0110 <sub>B</sub> ] ERU pattern detection output 3
ITR3H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 3, input H
ITR3I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 3, input I
ITR3J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 3, input J
ITR3K	I	GTM:ADC_TRIG2(3)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR3L	I	GTM:ADC_TRIG3(3)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR3M	I	GTM:DSADC_TRIG2(3)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR3N	I	GTM:DSADC_TRIG3(3)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR3O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 3, input O
ITR3P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 3, input P
SRM3	O	ICU, GTM:DSADC_SRM(3), HSM_EXT_INT23	Service request output main channel 3
SRA3	O	ICU	Service request output aux. channel 3
SAUL3	O	GTM:DSADC_SAUL(3)	Signal above upper limit ind., channel 3
SBLL3	O	GTM:DSADC_SBLL(3)	Signal below lower limit ind., channel 3
SWIB3	O	GTM:DTMA3(2)	Signal within band ind., channel 3
DATA3[16:0]	O	GTM	Result values of channel 3
WR3	O	GTM	Write signal for DATA3
<b>Channel 4</b>			
DSDIN4A	I	P00.8	[00X <sub>B</sub> ] Data bitstream channel 4 input A
DSDIN4B	I	P02.6	[01X <sub>B</sub> ] Data bitstream channel 4 input B
DSDIN4C	I	-	[10X <sub>B</sub> ] Data bitstream channel 4 input C
DSDIN4D	I	-	[11X <sub>B</sub> ] Data bitstream channel 4 input D
DSCIN4A	I	P00.7	[011 <sub>B</sub> ] Modulator clock channel 4 input A
DSCIN4B	I	P02.5	[100 <sub>B</sub> ] Modulator clock channel 4 input B
DSCIN4C	I	-	[101 <sub>B</sub> ] Modulator clock channel 4 input C
DSCOUT4	O	P00.7, P02.5	Modulator clock channel 4 output
ITR4A	I	GTM:DSADC_TRIG0(4)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR4B	I	GTM:DSADC_TRIG1(4)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR4C	I	GTM:ADC_TRIG0(4)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR4D	I	GTM:ADC_TRIG1(4)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR4E	I	P02.7	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR4F	I	P00.6	[0101 <sub>B</sub> ] Trigger/gate via port input

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

Table 371 Digital Connections for Product TC39x-B (cont'd)

Signal	Dir.	Source/Destin.	Description
ITR4G	I	SCU_PDOUT4	[0110 <sub>B</sub> ] ERU pattern detection output 4
ITR4H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 4, input H
ITR4I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 4, input I
ITR4J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 4, input J
ITR4K	I	GTM:ADC_TRIG2(4)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR4L	I	GTM:ADC_TRIG3(4)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR4M	I	GTM:DSADC_TRIG2(4)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR4N	I	GTM:DSADC_TRIG3(4)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR4O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 4, input O
ITR4P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 4, input P
SRM4	O	ICU, GTM:DSADC_SRM(4)	Service request output main channel 4
SRA4	O	ICU	Service request output aux. channel 4
SAUL4	O	GTM:DSADC_SAUL(4)	Signal above upper limit ind., channel 4
SBLL4	O	GTM:DSADC_SBLL(4)	Signal below lower limit ind., channel 4
SWIB4	O	GTM:DTMA4(2)	Signal within band ind., channel 4
DATA4[16:0]	O	GTM	Result values of channel 4
WR4	O	GTM	Write signal for DATA4

## Channel 5

DSDIN5A	I	P00.2	[00X <sub>B</sub> ] Data bitstream channel 5 input A
DSDIN5B	I	P02.4	[01X <sub>B</sub> ] Data bitstream channel 5 input B
DSDIN5C	I	-	[10X <sub>B</sub> ] Data bitstream channel 5 input C
DSDIN5D	I	-	[11X <sub>B</sub> ] Data bitstream channel 5 input D
DSCIN5A	I	P00.1	[011 <sub>B</sub> ] Modulator clock channel 5 input A
DSCIN5B	I	P02.3	[100 <sub>B</sub> ] Modulator clock channel 5 input B
DSCIN5C	I	-	[101 <sub>B</sub> ] Modulator clock channel 5 input C
DSCOUT5	O	P00.1, P02.3	Modulator clock channel 5 output
ITR5A	I	GTM:DSADC_TRIG0(5)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR5B	I	GTM:DSADC_TRIG1(5)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR5C	I	GTM:ADC_TRIG0(5)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR5D	I	GTM:ADC_TRIG1(5)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR5E	I	P02.6	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR5F	I	P00.3	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR5G	I	SCU_PDOUT5	[0110 <sub>B</sub> ] ERU pattern detection output 5
ITR5H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 5, input H
ITR5I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 5, input I
ITR5J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 5, input J
ITR5K	I	GTM:ADC_TRIG2(5)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR5L	I	GTM:ADC_TRIG3(5)	[1011 <sub>B</sub> ] GTM ADC trigger 3

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Dir.</b>	<b>Source/Destin.</b>	<b>Description</b>
ITR5M	I	GTM:DSADC_TRIG2(5)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR5N	I	GTM:DSADC_TRIG3(5)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR5O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 5, input O
ITR5P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 5, input P
SRM5	O	ICU, GTM:DSADC_SRM(5)	Service request output main channel 5
SRA5	O	ICU	Service request output aux. channel 5
SAUL5	O	GTM:DSADC_SAUL(5)	Signal above upper limit ind., channel 5
SBLL5	O	GTM:DSADC_SBLL(5)	Signal below lower limit ind., channel 5
SWIB5	O	-	Signal within band ind., channel 5
DATA5[16:0]	O	GTM	Result values of channel 5
WR5	O	GTM	Write signal for DATA5

**Channel 6**

DSDIN6A	I	P00.13	[00X <sub>B</sub> ] Data bitstream channel 6 input A
DSDIN6B	I	-	[01X <sub>B</sub> ] Data bitstream channel 6 input B
DSDIN6C	I	-	[10X <sub>B</sub> ] Data bitstream channel 6 input C
DSDIN6D	I	-	[11X <sub>B</sub> ] Data bitstream channel 6 input D
DSCIN6A	I	P00.14	[011 <sub>B</sub> ] Modulator clock channel 6 input A
DSCIN6B	I	-	[100 <sub>B</sub> ] Modulator clock channel 6 input B
DSCIN6C	I	-	[101 <sub>B</sub> ] Modulator clock channel 6 input C
DSCOUT6	O	P00.14	Modulator clock channel 6 output
ITR6A	I	GTM:DSADC_TRIG0(6)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR6B	I	GTM:DSADC_TRIG1(6)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR6C	I	GTM:ADC_TRIG0(6)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR6D	I	GTM:ADC_TRIG1(6)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR6E	I	P01.0	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR6F	I	P00.15	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR6G	I	SCU_PDOUT6	[0110 <sub>B</sub> ] ERU pattern detection output 6
ITR6H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 6, input H
ITR6I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 6, input I
ITR6J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 6, input J
ITR6K	I	GTM:ADC_TRIG2(6)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR6L	I	GTM:ADC_TRIG3(6)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR6M	I	GTM:DSADC_TRIG2(6)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR6N	I	GTM:DSADC_TRIG3(6)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR6O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 6, input O
ITR6P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 6, input P
SRM6	O	ICU, GTM:DSADC_SRM(6)	Service request output main channel 6
SRA6	O	ICU	Service request output aux. channel 6

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Dir.</b>	<b>Source/Destin.</b>	<b>Description</b>
SAUL6	O	GTM:DSADC_SAUL(6)	Signal above upper limit ind., channel 6
SBLL6	O	GTM:DSADC_SBLL(6)	Signal below lower limit ind., channel 6
SWIB6	O	-	Signal within band ind., channel 6
DATA6[16:0]	O	GTM	Result values of channel 6
WR6	O	GTM	Write signal for DATA6
<b>Channel 7</b>			
DSDIN7A	I	P01.15	[00X <sub>B</sub> ] Data bitstream channel 7 input A
DSDIN7B	I	P00.2	[01X <sub>B</sub> ] Data bitstream channel 7 input B
DSDIN7C	I	-	[10X <sub>B</sub> ] Data bitstream channel 7 input C
DSDIN7D	I	-	[11X <sub>B</sub> ] Data bitstream channel 7 input D
DSCIN7A	I	P01.2	[011 <sub>B</sub> ] Modulator clock channel 7 input A
DSCIN7B	I	P00.1	[100 <sub>B</sub> ] Modulator clock channel 7 input B
DSCIN7C	I	-	[101 <sub>B</sub> ] Modulator clock channel 7 input C
DSCOUT7	O	P01.2, P00.1	Modulator clock channel 7 output
ITR7A	I	GTM:DSADC_TRIG0(7)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR7B	I	GTM:DSADC_TRIG1(7)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR7C	I	GTM:ADC_TRIG0(7)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR7D	I	GTM:ADC_TRIG1(7)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR7E	I	P01.4	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR7F	I	P01.3	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR7G	I	SCU_PDOUT7	[0110 <sub>B</sub> ] ERU pattern detection output 7
ITR7H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 7, input H
ITR7I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 7, input I
ITR7J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 7, input J
ITR7K	I	GTM:ADC_TRIG2(7)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR7L	I	GTM:ADC_TRIG3(7)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR7M	I	GTM:DSADC_TRIG2(7)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR7N	I	GTM:DSADC_TRIG3(7)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR7O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 7, input O
ITR7P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 7, input P
SRM7	O	ICU, GTM:DSADC_SRM(7)	Service request output main channel 7
SRA7	O	ICU	Service request output aux. channel 7
SAUL7	O	GTM:DSADC_SAUL(7)	Signal above upper limit ind., channel 7
SBLL7	O	GTM:DSADC_SBLL(7)	Signal below lower limit ind., channel 7
SWIB7	O	-	Signal within band ind., channel 7
DATA7[16:0]	O	GTM	Result values of channel 7
WR7	O	GTM	Write signal for DATA7
<b>Channel 8</b>			

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

Signal	Dir.	Source/Destin.	Description
DSDIN8A	I	P01.6	[00X <sub>B</sub> ] Data bitstream channel 8 input A
DSDIN8B	I	-	[01X <sub>B</sub> ] Data bitstream channel 8 input B
DSDIN8C	I	-	[10X <sub>B</sub> ] Data bitstream channel 8 input C
DSDIN8D	I	-	[11X <sub>B</sub> ] Data bitstream channel 8 input D
DSCIN8A	I	P01.5	[011 <sub>B</sub> ] Modulator clock channel 8 input A
DSCIN8B	I	-	[100 <sub>B</sub> ] Modulator clock channel 8 input B
DSCIN8C	I	-	[101 <sub>B</sub> ] Modulator clock channel 8 input C
DSCOUT8	O	P01.5	Modulator clock channel 8 output
ITR8A	I	GTM:DSADC_TRIG0(8)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR8B	I	GTM:DSADC_TRIG1(8)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR8C	I	GTM:ADC_TRIG0(8)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR8D	I	GTM:ADC_TRIG1(8)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR8E	I	P01.1	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR8F	I	P01.7	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR8G	I	SCU_PDOUT0	[0110 <sub>B</sub> ] ERU pattern detection output 0
ITR8H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 8, input H
ITR8I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 8, input I
ITR8J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 8, input J
ITR8K	I	GTM:ADC_TRIG2(8)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR8L	I	GTM:ADC_TRIG3(8)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR8M	I	GTM:DSADC_TRIG2(8)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR8N	I	GTM:DSADC_TRIG3(8)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR8O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 8, input O
ITR8P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 8, input P
SRM8	O	ICU, GTM:DSADC_SRM(8)	Service request output main channel 8
SRA8	O	ICU	Service request output aux. channel 8
SAUL8	O	GTM:DSADC_SAUL(8)	Signal above upper limit ind., channel 8
SBLL8	O	GTM:DSADC_SBLL(8)	Signal below lower limit ind., channel 8
SWIB8	O	-	Signal within band ind., channel 8
DATA8[16:0]	O	GTM	Result values of channel 8
WR8	O	GTM	Write signal for DATA8

**Channel 9**

DSDIN9A	I	P01.8	[00X <sub>B</sub> ] Data bitstream channel 9 input A
DSDIN9B	I	-	[01X <sub>B</sub> ] Data bitstream channel 9 input B
DSDIN9C	I	-	[10X <sub>B</sub> ] Data bitstream channel 9 input C
DSDIN9D	I	-	[11X <sub>B</sub> ] Data bitstream channel 9 input D
DSCIN9A	I	P01.9	[011 <sub>B</sub> ] Modulator clock channel 9 input A
DSCIN9B	I	-	[100 <sub>B</sub> ] Modulator clock channel 9 input B

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Dir.</b>	<b>Source/Destin.</b>	<b>Description</b>
DSCIN9C	I	-	[101 <sub>B</sub> ] Modulator clock channel 9 input C
DSCOUT9	O	P01.9	Modulator clock channel 9 output
ITR9A	I	GTM:DSADC_TRIG0(9)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR9B	I	GTM:DSADC_TRIG1(9)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR9C	I	GTM:ADC_TRIG0(9)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR9D	I	GTM:ADC_TRIG1(9)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR9E	I	P01.11	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR9F	I	P01.10	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR9G	I	SCU_PDOUT1	[0110 <sub>B</sub> ] ERU pattern detection output 1
ITR9H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 9, input H
ITR9I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 9, input I
ITR9J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 9, input J
ITR9K	I	GTM:ADC_TRIG2(9)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR9L	I	GTM:ADC_TRIG3(9)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR9M	I	GTM:DSADC_TRIG2(9)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR9N	I	GTM:DSADC_TRIG3(9)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR9O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 9, input O
ITR9P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 9, input P
SRM9	O	ICU, GTM:DSADC_SRM(9)	Service request output main channel 9
SRA9	O	ICU	Service request output aux. channel 9
SAUL9	O	GTM:DSADC_SAUL(9)	Signal above upper limit ind., channel 9
SBLL9	O	GTM:DSADC_SBLL(9)	Signal below lower limit ind., channel 9
SWIB9	O	-	Signal within band ind., channel 9
DATA9[16:0]	O	GTM	Result values of channel 9
WR9	O	GTM	Write signal for DATA9

**Channel 10**

DSDIN10A	I	P01.12	[00X <sub>B</sub> ] Data bitstream channel 10 input A
DSDIN10B	I	-	[01X <sub>B</sub> ] Data bitstream channel 10 input B
DSDIN10C	I	-	[10X <sub>B</sub> ] Data bitstream channel 10 input C
DSDIN10D	I	-	[11X <sub>B</sub> ] Data bitstream channel 10 input D
DSCIN10A	I	P01.13	[011 <sub>B</sub> ] Modulator clock channel 10 input A
DSCIN10B	I	-	[100 <sub>B</sub> ] Modulator clock channel 10 input B
DSCIN10C	I	-	[101 <sub>B</sub> ] Modulator clock channel 10 input C
DSCOUT10	O	P01.13	Modulator clock channel 10 output
ITR10A	I	GTM:DSADC_TRIG0(10)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR10B	I	GTM:DSADC_TRIG1(10)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR10C	I	GTM:ADC_TRIG0(10)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR10D	I	GTM:ADC_TRIG1(10)	[0011 <sub>B</sub> ] GTM ADC trigger 1

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

Signal	Dir.	Source/Destin.	Description
ITR10E	I	P01.13	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR10F	I	P01.12	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR10G	I	SCU_PDOUT2	[0110 <sub>B</sub> ] ERU pattern detection output 2
ITR10H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 10, input H
ITR10I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 10, input I
ITR10J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 10, input J
ITR10K	I	GTM:ADC_TRIG2(10)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR10L	I	GTM:ADC_TRIG3(10)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR10M	I	GTM:DSADC_TRIG2(10)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR10N	I	GTM:DSADC_TRIG3(10)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR10O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 10, input O
ITR10P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 10, input P
SRM10	O	ICU, GTM:DSADC_SRM(10)	Service request output main channel 10
SRA10	O	ICU	Service request output aux. channel 10
SAUL10	O	GTM:DSADC_SAUL(10)	Signal above upper limit ind., channel 10
SBLL10	O	GTM:DSADC_SBLL(10)	Signal below lower limit ind., channel 10
SWIB10	O	-	Signal within band ind., channel 10
DATA10[16:0]	O	GTM	Result values of channel 10
WR10	O	GTM	Write signal for DATA10

**Channel 11**

DSDIN11A	I	P01.14	[00X <sub>B</sub> ] Data bitstream channel 11 input A
DSDIN11B	I	-	[01X <sub>B</sub> ] Data bitstream channel 11 input B
DSDIN11C	I	-	[10X <sub>B</sub> ] Data bitstream channel 11 input C
DSDIN11D	I	-	[11X <sub>B</sub> ] Data bitstream channel 11 input D
DSCIN11A	I	P01.15	[011 <sub>B</sub> ] Modulator clock channel 11 input A
DSCIN11B	I	-	[100 <sub>B</sub> ] Modulator clock channel 11 input B
DSCIN11C	I	-	[101 <sub>B</sub> ] Modulator clock channel 11 input C
DSCOUT11	O	P01.15	Modulator clock channel 11 output
ITR11A	I	GTM:DSADC_TRIG0(11)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR11B	I	GTM:DSADC_TRIG1(11)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR11C	I	GTM:ADC_TRIG0(11)	[0010 <sub>B</sub> ] GTM ADC trigger 0
ITR11D	I	GTM:ADC_TRIG1(11)	[0011 <sub>B</sub> ] GTM ADC trigger 1
ITR11E	I	P01.15	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR11F	I	P01.14	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR11G	I	SCU_PDOUT3	[0110 <sub>B</sub> ] ERU pattern detection output 3
ITR11H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 11, input H
ITR11I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 11, input I
ITR11J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 11, input J

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Dir.</b>	<b>Source/Destin.</b>	<b>Description</b>
ITR11K	I	GTM:ADC_TRIG2(11)	[1010 <sub>B</sub> ] GTM ADC trigger 2
ITR11L	I	GTM:ADC_TRIG3(11)	[1011 <sub>B</sub> ] GTM ADC trigger 3
ITR11M	I	GTM:DSADC_TRIG2(11)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR11N	I	GTM:DSADC_TRIG3(11)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR11O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 11, input O
ITR11P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 11, input P
SRM11	O	ICU, GTM:DSADC_SRM(11)	Service request output main channel 11
SRA11	O	ICU	Service request output aux. channel 11
SAUL11	O	GTM:DSADC_SAUL(11)	Signal above upper limit ind., channel 11
SBLL11	O	GTM:DSADC_SBLL(11)	Signal below lower limit ind., channel 11
SWIB11	O	-	Signal within band ind., channel 11
DATA11[16:0]	O	GTM	Result values of channel 11
WR11	O	GTM	Write signal for DATA11

**Channel 12**

DSDIN12A	I	P02.12	[00X <sub>B</sub> ] Data bitstream channel 12 input A
DSDIN12B	I	-	[01X <sub>B</sub> ] Data bitstream channel 12 input B
DSDIN12C	I	-	[10X <sub>B</sub> ] Data bitstream channel 12 input C
DSDIN12D	I	-	[11X <sub>B</sub> ] Data bitstream channel 12 input D
DSCIN12A	I	P02.13	[011 <sub>B</sub> ] Modulator clock channel 12 input A
DSCIN12B	I	-	[100 <sub>B</sub> ] Modulator clock channel 12 input B
DSCIN12C	I	-	[101 <sub>B</sub> ] Modulator clock channel 12 input C
DSCOUT12	O	P02.13	Modulator clock channel 12 output
ITR12A	I	GTM:DSADC_TRIG0(12)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR12B	I	GTM:DSADC_TRIG1(12)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR12C	I	-	[0010 <sub>B</sub> ] Trigger/gate, channel 12, input C
ITR12D	I	-	[0011 <sub>B</sub> ] Trigger/gate, channel 12, input D
ITR12E	I	P02.13	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR12F	I	P02.12	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR12G	I	SCU_PDOUT4	[0110 <sub>B</sub> ] ERU pattern detection output 4
ITR12H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 12, input H
ITR12I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 12, input I
ITR12J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 12, input J
ITR12K	I	-	[1010 <sub>B</sub> ] Trigger/gate, channel 13, input K
ITR12L	I	-	[1011 <sub>B</sub> ] Trigger/gate, channel 13, input L
ITR12M	I	GTM:DSADC_TRIG2(12)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR12N	I	GTM:DSADC_TRIG3(12)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR12O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 12, input O
ITR12P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 12, input P

**Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**
**Table 371 Digital Connections for Product TC39x-B (cont'd)**

<b>Signal</b>	<b>Dir.</b>	<b>Source/Destin.</b>	<b>Description</b>
SRM12	O	ICU, GTM:DSADC_SRM(12)	Service request output main channel 12
SRA12	O	ICU	Service request output aux. channel 12
SAUL12	O	GTM:DSADC_SAUL(12)	Signal above upper limit ind., channel 12
SBLL12	O	GTM:DSADC_SBLL(12)	Signal below lower limit ind., channel 12
SWIB12	O	-	Signal within band ind., channel 12
DATA12[16:0]	O	GTM	Result values of channel 12
WR12	O	GTM	Write signal for DATA12

**Channel 13**

DSDIN13A	I	P02.14	[00X <sub>B</sub> ] Data bitstream channel 13 input A
DSDIN13B	I	-	[01X <sub>B</sub> ] Data bitstream channel 13 input B
DSDIN13C	I	-	[10X <sub>B</sub> ] Data bitstream channel 13 input C
DSDIN13D	I	-	[11X <sub>B</sub> ] Data bitstream channel 13 input D
DSCIN13A	I	P02.15	[011 <sub>B</sub> ] Modulator clock channel 13 input A
DSCIN13B	I	-	[100 <sub>B</sub> ] Modulator clock channel 13 input B
DSCIN13C	I	-	[101 <sub>B</sub> ] Modulator clock channel 13 input C
DSCOUT13	O	P02.15	Modulator clock channel 13 output
ITR13A	I	GTM:DSADC_TRIG0(13)	[0000 <sub>B</sub> ] GTM DSADC trigger 0
ITR13B	I	GTM:DSADC_TRIG1(13)	[0001 <sub>B</sub> ] GTM DSADC trigger 1
ITR13C	I	-	[0010 <sub>B</sub> ] Trigger/gate, channel 12, input C
ITR13D	I	-	[0011 <sub>B</sub> ] Trigger/gate, channel 12, input D
ITR13E	I	P02.15	[0100 <sub>B</sub> ] Trigger/gate via port input
ITR13F	I	P02.14	[0101 <sub>B</sub> ] Trigger/gate via port input
ITR13G	I	SCU_PDOUT5	[0110 <sub>B</sub> ] ERU pattern detection output 5
ITR13H	I	-	[0111 <sub>B</sub> ] Trigger/gate, channel 13, input H
ITR13I	I	-	[1000 <sub>B</sub> ] Trigger/gate, channel 13, input I
ITR13J	I	-	[1001 <sub>B</sub> ] Trigger/gate, channel 13, input J
ITR13K	I	-	[1010 <sub>B</sub> ] Trigger/gate, channel 13, input K
ITR13L	I	-	[1011 <sub>B</sub> ] Trigger/gate, channel 13, input L
ITR13M	I	GTM:DSADC_TRIG2(13)	[1100 <sub>B</sub> ] GTM DSADC trigger 2
ITR13N	I	GTM:DSADC_TRIG3(13)	[1101 <sub>B</sub> ] GTM DSADC trigger 3
ITR13O	I	-	[1110 <sub>B</sub> ] Trigger/gate, channel 13, input O
ITR13P	I	-	[1111 <sub>B</sub> ] Trigger/gate, channel 13, input P
SRM13	O	ICU, GTM:DSADC_SRM(13)	Service request output main channel 13
SRA13	O	ICU	Service request output aux. channel 13
SAUL13	O	GTM:DSADC_SAUL(13)	Signal above upper limit ind., channel 13
SBLL13	O	GTM:DSADC_SBLL(13)	Signal below lower limit ind., channel 13
SWIB13	O	-	Signal within band ind., channel 13
DATA13[16:0]	O	GTM	Result values of channel 13

## Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

**Table 371 Digital Connections for Product TC39x-B (cont'd)**

Signal	Dir.	Source/Destin.	Description
WR13	O	GTM	Write signal for DATA13
<b>General</b>			
PHSYNC	I	Phase synchronizer	Synchronization signal for analog clocks
MODCLK	I	SCU: $f_{SPB}$	Module clock
RESET	I	SCU	Reset signal (general)
SGNA	I	P00.4	Sign input A (carrier signal)
SGNB	I	P33.13	Sign input B (carrier signal)
CGPWMP	O	P00.6, P02.1, P33.12	Positive PWM signal of carrier generator
CGPWMN	O	P00.5, P02.0, P33.11	Negative PWM signal of carrier generator

## 31.4 Revision History

This is a summary of the modifications that have been applied to this chapter.

**Table 372 Revision History**

Reference	Change to Previous Version	Comment
<b>V3.0.0</b>		
-	No change.	
<b>V3.0.1</b>		
-	No functional change.	
<b>V3.0.2</b>		
-	No functional change.	
<b>V3.0.3</b>		
<a href="#">Page 6</a>	Corrected source “GTM:DSADC_TRIG3(0)” for signal ITR0N.	
<b>V3.0.4</b>		
<a href="#">Page 1</a>	Changed value for channel 9.	
<b>V3.0.5</b>		
-	No functional change.	
<b>V3.0.6</b>		
-	No functional change.	

## Inter-Integrated Circuit (I2C)

### 32 Inter-Integrated Circuit (I2C)

This chapter describes the Inter-Integrated Circuit (short I2C) Module of the TC39x-B.

#### 32.1 TC39x-B Specific IP Configuration

See features in family spec.

No product specific configuration for I2C

#### 32.2 TC39x-B Specific Register Set

##### Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

**Table 373 Register Address Space - I2C**

Module	Base Address	End Address	Note
I2C0	F00C0000 <sub>H</sub>	F00D00FF <sub>H</sub>	FPI slave interface
I2C1	F00E0000 <sub>H</sub>	F00F00FF <sub>H</sub>	FPI slave interface

##### Register Overview Table

There are no product specific register for this module.

#### 32.3 TC39x-B Specific Registers

There are no product specific register for this module.

#### 32.4 Connectivity

The tables below list all the connections of I2C instances.

**Table 374 Connections of I2C0**

Interface Signals	connects	Description	
I2C0:SCL	to	P02.5:ALT(5)	Serial Clock Output
		P13.1:ALT(6)	
		P15.4:ALT(6)	
I2C0:SDA	to	P02.4:ALT(5)	Serial Data Output
		P13.2:ALT(6)	
		P15.5:ALT(6)	
I2C0:SDAA	from	P02.4:IN	Serial Data Input 0
I2C0:SDAB	from	P13.2:IN	Serial Data Input 1
I2C0:SDAC	from	P15.5:IN	Serial Data Input 2
I2C0:SLEEP	from	SCU:scu_syst_sleep_n	Sleep Request
I2C0:DTR_INT	to	INT:i2c0.DTR_INT	I2C Data Transfer Request
I2C0:ERR_INT	to	INT:i2c0.ERR_INT	I2C Error Service Request
I2C0:P_INT	to	INT:i2c0.P_INT	I2C Kernel Service Request

**Inter-Integrated Circuit (I2C)****Table 375 Connections of I2C1**

Interface Signals	connects		Description
I2C1:SCL	to	P11.14:ALT(6)	Serial Clock Output
		P13.9:ALT(6)	
I2C1:SDA	to	P11.13:ALT(6)	Serial Data Output
		P13.12:ALT(6)	
I2C1:SDAA	from	P11.13:IN	Serial Data Input 0
I2C1:SDAB	from	P13.12:IN	Serial Data Input 1
I2C1:SLEEP	from	SCU:scu_syst_sleep_n	Sleep Request
I2C1:DTR_INT	to	INT:i2c1.DTR_INT	I2C Data Transfer Request
I2C1:ERR_INT	to	INT:i2c1.ERR_INT	I2C Error Service Request
I2C1:P_INT	to	INT:i2c1.P_INT	I2C Kernel Service Request

**32.5 Revision History****Table 376 Revision History**

Reference	Change to Previous Version	Comment
V2.3.4		
Page 1	No functional changes. Formal changes in Connectivity tables.	
V2.3.5	- No functional changes.	
V2.3.6	- No functional changes.	

## High Speed Serial Link (HSSL)

### 33 High Speed Serial Link (HSSL)

This section provides information regarding the implementation of the module HSSL specifically for device TC39x-B.

#### 33.1 TC39x-B Specific IP Configuration

See features in family spec.

No product specific configuration for HSSL

#### 33.2 TC39x-B Specific Register Set

##### 33.2.1 Address Map

**Table 377 Register Address Space - HSSL**

Module	Base Address	End Address	Note
HSSL0	F0080000 <sub>H</sub>	F00803FF <sub>H</sub>	FPI slave interface
HSSL1	F00A0000 <sub>H</sub>	F00A03FF <sub>H</sub>	FPI slave interface

*Note:* The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

#### 33.3 TC39x-B Specific Registers

TIDADD register reset information for HSSL0: The TIDADD register contains the address from which the target ID is fetched. After the Power-On Reset, System Reset, and Application Reset the start-up software writes this register with the address of CBS\_JTAGID register. After Kernel Reset, the start-up software is not executed, and the reset value is not changed.

TIDADD register reset information for HSSL1: The application software should write this register after any reset with this address of CBS\_JTAGID register or some other customer defined address value.

#### 33.4 Connectivity

**Table 378 Connections of HSSL0**

Interface Signals	connects		Description
HSSL0:sri_rph_err	to	SMU:sri_rph_err=SMU:hssl.hssl0_sri_rph_err.sri_rph_err	SRI read phase error
HSSL0:COK_INT(3:0)	to	INT:hssl0.COK_INT(3:0)	Channel OK Service Request
HSSL0:RDI_INT(3:0)	to	INT:hssl0.RDI_INT(3:0)	Channel Read Data Service Request
HSSL0:ERR_INT(3:0)	to	INT:hssl0.ERR_INT(3:0)	Channel Error Service Request

## High Speed Serial Link (HSSL)

**Table 378 Connections of HSSL0 (cont'd)**

Interface Signals	connects		Description
HSSL0:TRG_INT(3:0)	to	INT:hssl0.TRG_INT(3:0)	Channel Trigger Interrupt Service Request m
HSSL0:EXI_INT	to	INT:hssl0.EXI_INT	HSSL Exception Service Request

**Table 379 Connections of HSSL1**

Interface Signals	connects		Description
HSSL1:sri_rph_err	to	SMU:sri_rph_err=SMU:hssl1_sri_rph_err.sri_rph_err	SRI read phase error
HSSL1:COK_INT(3:0)	to	INT:hssl1.COK_INT(3:0)	Channel OK Service Request
HSSL1:RDI_INT(3:0)	to	INT:hssl1.RDI_INT(3:0)	Channel Read Data Service Request
HSSL1:ERR_INT(3:0)	to	INT:hssl1.ERR_INT(3:0)	Channel Error Service Request
HSSL1:TRG_INT(3:0)	to	INT:hssl1.TRG_INT(3:0)	Channel Trigger Interrupt Service Request m
HSSL1:EXI_INT	to	INT:hssl1.EXI_INT	HSSL Exception Service Request

## 33.5 Revision History

**Table 380 Revision History**

Reference	Change to Previous Version	Comment
<b>V3.0.16</b>		
<a href="#">Page 2</a>	Previous versions removed from revision history.	
<b>V3.0.17</b>		
<a href="#">Page 1</a>	Updated Connections table.	
<b>V3.0.18</b>		
-	No changes.	
<b>V3.0.19</b>		
-	No changes.	

### 33.6 High Speed Communication Tunnel (HSCT)

This section provides information regarding the implementation of the module HSCT specifically for device TC39x-B.

#### 33.6.1 TC39x-B Specific IP Configuration

See features in family spec.

No product specific configuration for HSCT

No differences between the instances of the HSCT in TC39x-B.

#### 33.6.2 TC39x-B Specific Register Set

There are no device specific registers in TC39x-B.

##### 33.6.2.1 Address Map

**Table 381 Register Address Space - HSCT**

Module	Base Address	End Address	Note
HSCT0	F0090000 <sub>H</sub>	F009FFFF <sub>H</sub>	FPI slave interface
HSCT1	F00B0000 <sub>H</sub>	F00BFFFF <sub>H</sub>	FPI slave interface

*Note:* The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

#### 33.6.3 TC39x-B Specific Registers

There are no module specific registers for the HSCT.

The common SYSCLK output functionality is controlled by the HSCT0 register INIT.

#### 33.6.4 Connectivity

The LVDS TX output of HSCT0 is connected to P21.4 and P21.5, the LVDS RX input to P21.2 and P21.3.

The LVDS TX output of HSCT1 is connected to P22.2 and P22.3, the LVDS RX input to P21.0 and P21.1.

The SYSCLK input/output is connected to P20.0. For more details see the pinning chapter.

The HSCT0 module forwards to the HSCT1 module its SYSCLK signal, which is in this case named CLKA\_REF\_NXT.

**Table 382 Connections of HSCT0**

Interface Signals	connects		Description
HSCT0:CLKA_REF_NXT	to	HSCT1:SYSCLK_IN	Forward clka_ref_i to next HSCT PHY instance
HSCT0:RXDN	from	TC39x-B:P21.2	Rx data
HSCT0:RXDP	from	TC39x-B:P21.3	Rx data
HSCT0:SYSCLK_IN	from	CCU:CLKA_REF_HSCT	Reference clock
HSCT0:SYSCLK_OUT	to	P20.0:ALT(5)	sys clock output
HSCT0:TXDN	to	TC39x-B:P21.4	Tx data

**Table 382 Connections of HSCT0 (cont'd)**

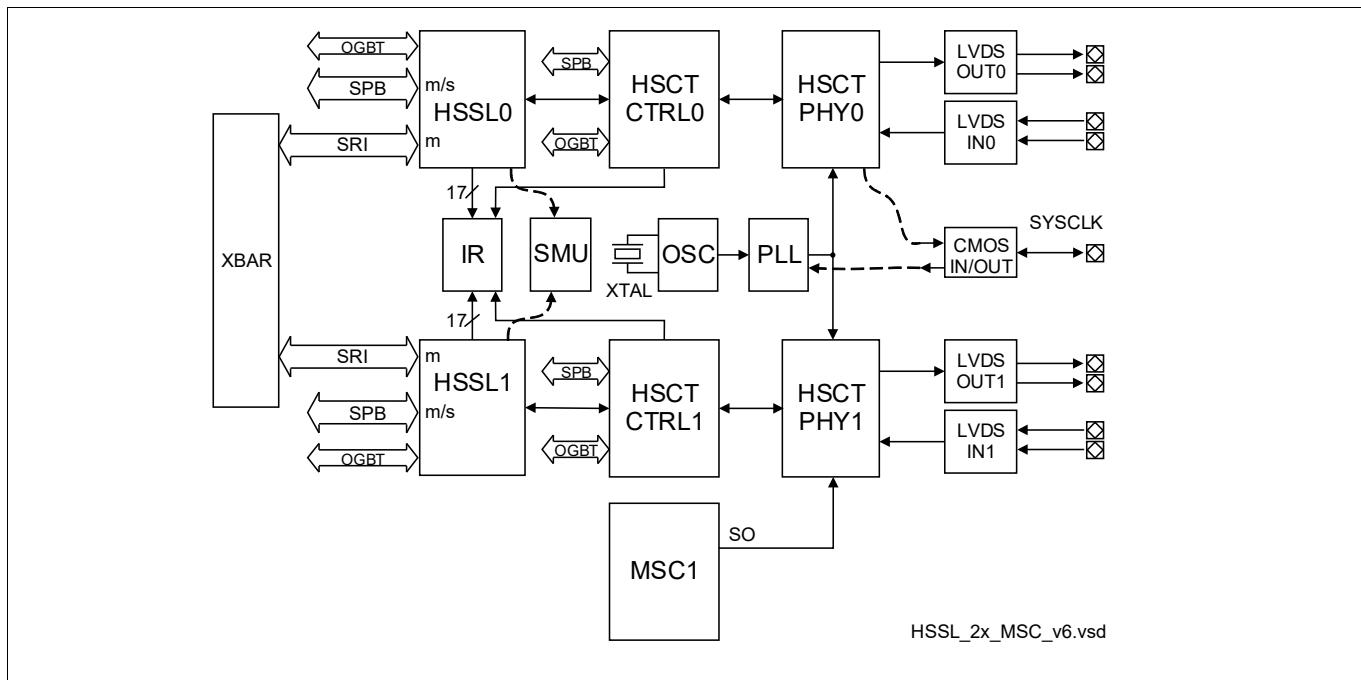
<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
HSCT0:TXDP	to	TC39x-B:P21.5	Tx data
HSCT0:INT	to	INT:hsct0.INT	HSCT Service Request

**Table 383 Connections of HSCT1**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
HSCT1:RXDN	from	TC39x-B:P21.0	Rx data
HSCT1:RXDP	from	TC39x-B:P21.1	Rx data
HSCT1:SYSCLK_IN	from	HSCT0:CLKA_REF_NXT	Reference clock
HSCT1:TXDN	to	TC39x-B:P22.2	Tx data
HSCT1:TXDP	to	TC39x-B:P22.3	Tx data
HSCT1:INT	to	INT:hsct1.INT	HSCT Service Request

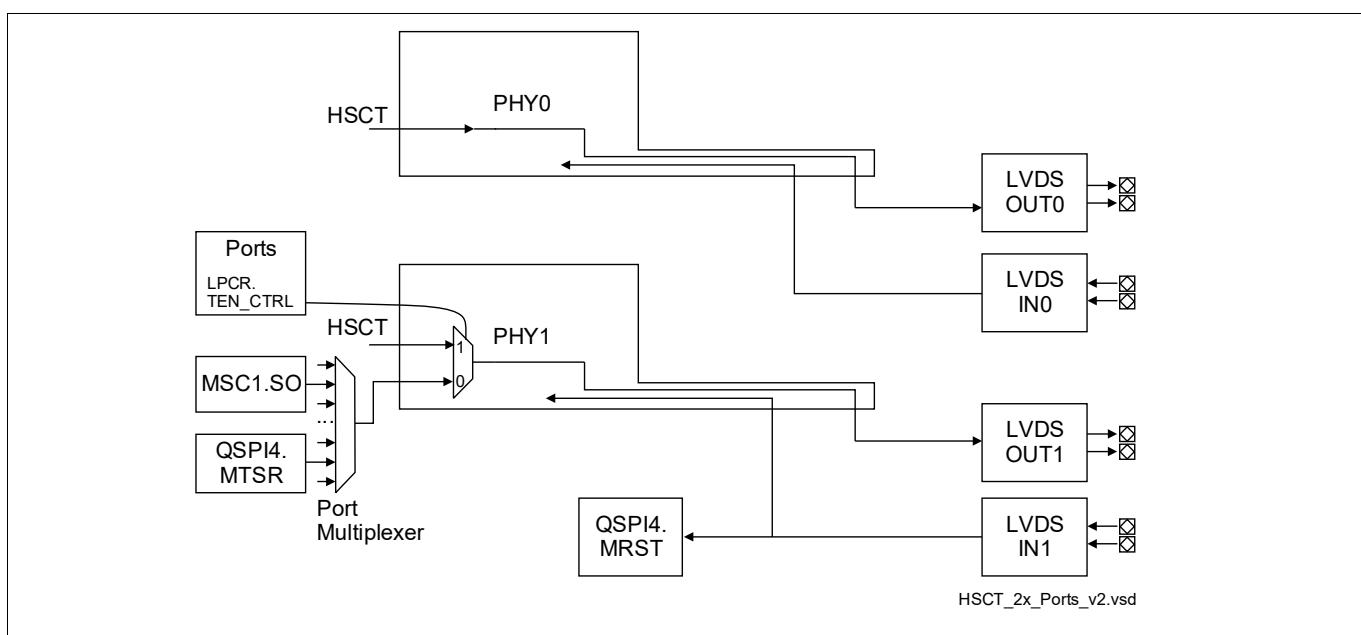
### 33.6.5 Multi-HSCT Support and Restrictions

This device contains two HSCT instances. Both instances share one PLL and one SysClk pin. Therefore, if both modules are active at the same time, they can either operate as two masters or two slaves. If both HSCT modules on one device are used as slaves, the corresponding master modules connected to these slaves must be from one device and use the same clock. For an overview of the HSSL/HSCT subsystem, see [Figure 33](#).



**Figure 33 HSCT Subsystem Overview**

The output LVDS pads of the HSCT1 are shared with an MSC and a QSPI module, and the input LVDS pads are shared with QSPI. The software can select which module drives the LVDS output pad by configuring the port register LPCRx.TEN\_CTRL, see [Figure 34](#).



**Figure 34 Pin Sharing Overview**

### 33.6.6 Device Specific Baud Rates

Additionally to the standard baud rates of the HSCT module described in the general module specification, this device supports the following baud rates, based on  $f_{SYSCLK} = 25\text{MHz}$ :

- 6.25 MBaud for the low speed mode
- 200MBaud for high speed mode, 1 Master - 1 Slave connection
- 100MBaud for high speed mode, 1 Master - 2 Slaves connection

### 33.6.7 Revision History

**Table 384 Revision History**

Reference	Change to Previous Version	Comment
<b>V2.3.11</b>		
<a href="#">Page 5</a>	The restriction “The HSCT1 module is intended to be used with baud rate of 200MBaud” is removed for TC39x.	0000056742-24
<a href="#">Page 6</a>	Previous versions removed from revision history.	none
<a href="#">Page 3</a>	Typo corrected.	none
<b>V2.3.12</b>		
<a href="#">Page 3</a>	Connection “pll_wrapper_ana_0:CLKA_REF_HSCT” updated to “CCU:CLKA_REF_HSCT”. Some further formal changes in connections table.	
<b>V2.3.13</b>		
-	No functional changes.	
<b>V2.3.14</b>		
<a href="#">Page 3</a>	Updated headline.	
<b>V2.3.15</b>		
-	No functional changes.	

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**Asynchronous Serial Interface (ASCLIN)****34 Asynchronous Serial Interface (ASCLIN)**

Text with reference to family spec.

**34.1 TC39x-B Specific IP Configuration**

No product specific configuration for ASCLIN

**Asynchronous Serial Interface (ASCLIN)****34.2 TC39x-B Specific Register Set****Register Address Space Table****Table 385 Register Address Space - ASCLIN**

<b>Module</b>	<b>Base Address</b>	<b>End Address</b>	<b>Note</b>
ASCLIN0	F0000600 <sub>H</sub>	F00006FF <sub>H</sub>	FPI slave interface
ASCLIN1	F0000700 <sub>H</sub>	F00007FF <sub>H</sub>	FPI slave interface
ASCLIN2	F0000800 <sub>H</sub>	F00008FF <sub>H</sub>	FPI slave interface
ASCLIN3	F0000900 <sub>H</sub>	F00009FF <sub>H</sub>	FPI slave interface
ASCLIN4	F0000A00 <sub>H</sub>	F0000AFF <sub>H</sub>	FPI slave interface
ASCLIN5	F0000B00 <sub>H</sub>	F0000BFF <sub>H</sub>	FPI slave interface
ASCLIN6	F0000C00 <sub>H</sub>	F0000CFF <sub>H</sub>	FPI slave interface
ASCLIN7	F0000D00 <sub>H</sub>	F0000dff <sub>H</sub>	FPI slave interface
ASCLIN8	F0000E00 <sub>H</sub>	F0000EFF <sub>H</sub>	FPI slave interface
ASCLIN9	F0000F00 <sub>H</sub>	F0000FFF <sub>H</sub>	FPI slave interface
ASCLIN10	F02C0A00 <sub>H</sub>	F02C0AFF <sub>H</sub>	FPI slave interface
ASCLIN11	F02C0B00 <sub>H</sub>	F02C0BFF <sub>H</sub>	FPI slave interface

**Register Overview Table****Table 386 Register Overview - ASCLIN (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN0_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN1_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN2_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN3_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN4_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN5_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)**
**Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN6_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN7_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN8_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN9_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN10_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN11_CLC	Clock Control Register	000 <sub>H</sub>	See Family Spec
ASCLIN0_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN1_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN2_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN3_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN4_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN5_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN6_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN7_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN8_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN9_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN10_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN11_IOCR	Input and Output Control Register	004 <sub>H</sub>	See Family Spec
ASCLIN0_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN1_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN2_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN3_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN4_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN5_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN6_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN7_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN8_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN9_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN10_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN11_ID	Module Identification Register	008 <sub>H</sub>	See Family Spec
ASCLIN0_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN1_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN2_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN3_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN4_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN5_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN6_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN7_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN8_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN9_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN10_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec
ASCLIN11_TXFIFOCON	TX FIFO Configuration Register	00C <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN0_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN1_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN2_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN3_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN4_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN5_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN6_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN7_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN8_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN9_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN10_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN11_RXFIFOCON	RX FIFO Configuration Register	010 <sub>H</sub>	See Family Spec
ASCLIN0_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN1_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN2_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN3_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN4_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN5_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN6_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN7_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN8_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN9_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN10_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN11_BITCON	Bit Configuration Register	014 <sub>H</sub>	See Family Spec
ASCLIN0_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN1_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN2_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN3_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN4_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN5_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN6_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN7_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN8_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN9_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN10_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN11_FRAMECON	Frame Control Register	018 <sub>H</sub>	See Family Spec
ASCLIN0_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN1_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN2_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN3_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN4_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN5_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN6_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN7_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN8_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN9_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN10_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN11_DATCON	Data Configuration Register	01C <sub>H</sub>	See Family Spec
ASCLIN0_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN1_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN2_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN3_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN4_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN5_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN6_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN7_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN8_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN9_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN10_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN11_BRG	Baud Rate Generation Register	020 <sub>H</sub>	See Family Spec
ASCLIN0_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN1_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN2_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN3_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN4_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN5_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN6_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN7_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN8_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN9_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN10_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN11_BRD	Baud Rate Detection Register	024 <sub>H</sub>	See Family Spec
ASCLIN0_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN1_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN2_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN3_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN4_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN5_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN6_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN7_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN8_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN9_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN10_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec
ASCLIN11_LINCON	LIN Control Register	028 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN0_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN1_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN2_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN3_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN4_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN5_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN6_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN7_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN8_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN9_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN10_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN11_LINBTIMER	LIN Break Timer Register	02C <sub>H</sub>	See Family Spec
ASCLIN0_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN1_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN2_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN3_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN4_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN5_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN6_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN7_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN8_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN9_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN10_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN11_LINHTIMER	LIN Header Timer Register	030 <sub>H</sub>	See Family Spec
ASCLIN0_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN1_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN2_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN3_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN4_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN5_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN6_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN7_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN8_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN9_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN10_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN11_FLAGS	Flags Register	034 <sub>H</sub>	See Family Spec
ASCLIN0_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN1_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN2_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN3_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN4_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN5_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN6_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN7_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN8_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN9_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN10_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN11_FLAGSSET	Flags Set Register	038 <sub>H</sub>	See Family Spec
ASCLIN0_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN1_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN2_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN3_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN4_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN5_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN6_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN7_FLAGSCLEAR	Flags Clear Register	03C <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN8_FLAGSCLEA R	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN9_FLAGSCLEA R	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN10_FLAGSCLE AR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN11_FLAGSCLE AR	Flags Clear Register	03C <sub>H</sub>	See Family Spec
ASCLIN0_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN1_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN2_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN3_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN4_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN5_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN6_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN7_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN8_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN9_FLAGSENA BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN10_FLAGSENA_BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN11_FLAGSENA_BLE	Flags Enable Register	040 <sub>H</sub>	See Family Spec
ASCLIN0_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN1_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN2_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN3_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN4_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN5_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN6_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN7_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN8_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN9_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN10_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec
ASCLIN11_TXDATA	Transmit Data Register	044 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN0_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN1_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN2_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN3_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN4_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN5_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN6_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN7_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN8_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN9_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN10_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN11_RXDATA	Receive Data Register	048 <sub>H</sub>	See Family Spec
ASCLIN0_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN1_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN2_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN3_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN4_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN5_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN6_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN7_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN8_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN9_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN10_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN11_CSR	Clock Selection Register	04C <sub>H</sub>	See Family Spec
ASCLIN0_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN1_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN2_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN3_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN4_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN5_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN6_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN7_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN8_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN9_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN10_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN11_RXDATAD	Receive Data Debug Register	050 <sub>H</sub>	See Family Spec
ASCLIN0_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN1_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN2_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN3_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN4_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN5_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN6_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN7_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN8_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN9_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN10_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN11_OCS	OCDS Control and Status	0E8 <sub>H</sub>	See Family Spec
ASCLIN0_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN1_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN2_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN3_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN4_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN5_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN6_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN7_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN8_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN9_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN10_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN11_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	See Family Spec
ASCLIN0_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN1_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN2_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN3_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN4_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN5_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN6_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN7_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN8_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN9_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN10_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN11_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	See Family Spec
ASCLIN0_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN1_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN2_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN3_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN4_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN5_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN6_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN7_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN8_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN9_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN10_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec
ASCLIN11_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	See Family Spec

**Asynchronous Serial Interface (ASCLIN)****Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ASCLIN0_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN1_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN2_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN3_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN4_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN5_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN6_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN7_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN8_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN9_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN10_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN11_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	See Family Spec
ASCLIN0_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN1_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec

## Asynchronous Serial Interface (ASCLIN)

**Table 386 Register Overview - ASCLIN (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN3_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN4_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN5_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN6_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN7_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN8_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN9_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN10_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec
ASCLIN11_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	See Family Spec

### 34.3 TC39x-B Specific Registers

No deviations from the Family Spec

### 34.4 Connectivity

**Table 387 Connections of ASCLIN0**

Interface Signals	connects		Description
ASCLIN0:ACTSA	from	P14.9:IN	Clear to send input
ASCLIN0:ACTSD	from	ASCLIN0:ARTS	Clear to send input

## Asynchronous Serial Interface (ASCLIN)

**Table 387 Connections of ASCLIN0 (cont'd)**

Interface Signals	connects		Description
ASCLIN0:ARTS	to	P14.7:ALT(2)	Ready to send output
		ASCLIN0:ACTSD	
ASCLIN0:ARXA	from	P14.1:IN	Receive input
ASCLIN0:ARXB	from	P15.3:IN	Receive input
ASCLIN0:ARXC	from	P01.8:IN	Receive input
ASCLIN0:ARXD	from	P33.10:IN	Receive input
ASCLIN0:ARXE	from	P13.11:IN	Receive input
ASCLIN0:ASCLK	to	P14.0:ALT(6)	Shift clock output
		P15.2:ALT(6)	
ASCLIN0:ATX	to	IOM:MON2(12)	Transmit output
		IOM:REF2(12)	
		P01.13:ALT(2)	
		P13.10:ALT(2)	
		P14.0:ALT(2)	
		P14.1:ALT(2)	
		P15.2:ALT(2)	
		P15.3:ALT(2)	
		P33.9:ALT(6)	
ASCLIN0:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN0:TX_INT	to	INT:asclin0.TX_INT	ASCLIN Transmit Service Request
ASCLIN0:RX_INT	to	INT:asclin0.RX_INT	ASCLIN Receive Service Request
ASCLIN0:ERR_INT	to	INT:asclin0.ERR_INT	ASCLIN Error Service Request

**Table 388 Connections of ASCLIN1**

Interface Signals	connects		Description
ASCLIN1:ACTSA	from	P20.7:IN	Clear to send input
ASCLIN1:ACTSB	from	P32.4:IN	Clear to send input
ASCLIN1:ACTSD	from	ASCLIN1:ARTS	Clear to send input
ASCLIN1:ARTS	to	P20.6:ALT(2)	Ready to send output
		P23.1:ALT(2)	
		ASCLIN1:ACTSD	
ASCLIN1:ARXA	from	P15.1:IN	Receive input
ASCLIN1:ARXB	from	P15.5:IN	Receive input
ASCLIN1:ARXC	from	P20.9:IN	Receive input
ASCLIN1:ARXD	from	P14.8:IN	Receive input
ASCLIN1:ARXE	from	P11.10:IN	Receive input
ASCLIN1:ARXF	from	P33.13:IN	Receive input
ASCLIN1:ARXG	from	P02.3:IN	Receive input

**Asynchronous Serial Interface (ASCLIN)****Table 388 Connections of ASCLIN1 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
ASCLIN1:ASCLK	to	P15.0:ALT(6)	Shift clock output
		P20.10:ALT(6)	
		P33.11:ALT(2)	
		P33.12:ALT(4)	
ASCLIN1:ASLSO	to	P14.3:ALT(4)	Slave select signal output
		P20.8:ALT(2)	
		P33.10:ALT(4)	
ASCLIN1:ATX	to	IOM:MON2(13)	Transmit output
		IOM:REF2(13)	
		P02.2:ALT(2)	
		P11.12:ALT(2)	
		P14.10:ALT(4)	
		P14.15:ALT(2)	
		P15.0:ALT(2)	
		P15.1:ALT(2)	
		P15.4:ALT(2)	
		P15.5:ALT(2)	
		P20.10:ALT(2)	
		P33.12:ALT(2)	
		P33.13:ALT(2)	
ASCLIN1:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN1:TX_INT	to	INT:asclin1.TX_INT	ASCLIN Transmit Service Request
ASCLIN1:RX_INT	to	INT:asclin1.RX_INT	ASCLIN Receive Service Request
ASCLIN1:ERR_INT	to	INT:asclin1.ERR_INT	ASCLIN Error Service Request

**Table 389 Connections of ASCLIN2**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
ASCLIN2:ACTSA	from	P10.7:IN	Clear to send input
ASCLIN2:ACTSB	from	P33.5:IN	Clear to send input
ASCLIN2:ACTSD	from	ASCLIN2:ARTS	Clear to send input
ASCLIN2:ARTS	to	P10.8:ALT(2)	Ready to send output
		P33.4:ALT(2)	
		ASCLIN2:ACTSD	
ASCLIN2:ARXA	from	P14.3:IN	Receive input
ASCLIN2:ARXB	from	P02.1:IN	Receive input
ASCLIN2:ARXC	from	P02.10:IN	Receive input
ASCLIN2:ARXD	from	P10.6:IN	Receive input
ASCLIN2:ARXE	from	P33.8:IN	Receive input

**Asynchronous Serial Interface (ASCLIN)****Table 389 Connections of ASCLIN2 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
ASCLIN2:ARXF	from	P32.6:IN	Receive input
ASCLIN2:ARXG	from	P02.0:IN	Receive input
ASCLIN2:ASCLK	to	P02.4:ALT(2)	Shift clock output
		P10.6:ALT(2)	
		P14.2:ALT(6)	
		P33.7:ALT(2)	
		P33.9:ALT(4)	
ASCLIN2:ASLSO	to	P02.3:ALT(2)	Slave select signal output
		P10.5:ALT(6)	
		P33.6:ALT(2)	
ASCLIN2:ATX	to	IOM:MON2(14)	Transmit output
		IOM:REF2(14)	
		P02.0:ALT(2)	
		P02.9:ALT(2)	
		P10.5:ALT(2)	
		P14.2:ALT(2)	
		P14.3:ALT(2)	
		P32.5:ALT(2)	
		P33.8:ALT(2)	
		P33.9:ALT(2)	
ASCLIN2:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN2:TX_INT	to	INT:asclin2.TX_INT	ASCLIN Transmit Service Request
ASCLIN2:RX_INT	to	INT:asclin2.RX_INT	ASCLIN Receive Service Request
ASCLIN2:ERR_INT	to	INT:asclin2.ERR_INT	ASCLIN Error Service Request

**Table 390 Connections of ASCLIN3**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
ASCLIN3:ACTSA	from	P00.12:IN	Clear to send input
ASCLIN3:ACTSD	from	ASCLIN3:ARTS	Clear to send input
ASCLIN3:ARTS	to	P00.9:ALT(3)	Ready to send output
		ASCLIN3:ACTSD	
ASCLIN3:ARXA	from	P15.7:IN	Receive input
ASCLIN3:ARXB	from	P11.0:IN	Receive input
ASCLIN3:ARXC	from	P20.3:IN	Receive input
ASCLIN3:ARXD	from	P32.2:IN	Receive input
ASCLIN3:ARXE	from	P00.1:IN	Receive input
ASCLIN3:ARXF	from	P21.6:IN	Receive input
ASCLIN3:ARXGN	from	TC39x-B:P21.2	Differential Receive input (low active)

## Asynchronous Serial Interface (ASCLIN)

**Table 390 Connections of ASCLIN3 (cont'd)**

Interface Signals	connects		Description
ASCLIN3:ARXGP	from	TC39x-B:P21.3	Differential Receive input (high active)
ASCLIN3:ARXH	from	P13.12:IN	Receive input
ASCLIN3:ASCLK	to	P00.0:ALT(2)	Shift clock output
		P00.2:ALT(2)	
		P11.1:ALT(2)	
		P11.4:ALT(2)	
		P15.6:ALT(6)	
		P15.8:ALT(6)	
		P20.0:ALT(3)	
		P21.5:ALT(2)	
		P21.7:ALT(3)	
		P32.3:ALT(4)	
		P33.2:ALT(2)	
ASCLIN3:ASLSO	to	P00.3:ALT(2)	Slave select signal output
		P12.1:ALT(2)	
		P14.3:ALT(5)	
		P21.2:ALT(2)	
		P21.6:ALT(2)	
		P33.1:ALT(2)	
ASCLIN3:ATX	to	IOM:MON2(15)	Transmit output
		IOM:REF2(15)	
		P00.0:ALT(3)	
		P00.1:ALT(2)	
		P11.0:ALT(2)	
		P11.1:ALT(3)	
		P13.9:ALT(2)	
		P15.6:ALT(2)	
		P15.7:ALT(2)	
		P20.0:ALT(2)	
		P20.3:ALT(2)	
		P21.7:ALT(2)	
		P22.1:ALT(2)	
		P32.2:ALT(2)	
		P32.3:ALT(2)	
ASCLIN3:ATXN	to	P22.0:ALT(2)	Differential Transmit output (low active)
ASCLIN3:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN3:TX_INT	to	INT:asclin3.TX_INT	ASCLIN Transmit Service Request

## Asynchronous Serial Interface (ASCLIN)

**Table 390 Connections of ASCLIN3 (cont'd)**

Interface Signals	connects		Description
ASCLIN3:RX_INT	to	INT:asclin3.RX_INT	ASCLIN Receive Service Request
ASCLIN3:ERR_INT	to	INT:asclin3.ERR_INT	ASCLIN Error Service Request

**Table 391 Connections of ASCLIN4**

Interface Signals	connects		Description
ASCLIN4:ACTSD	from	ASCLIN4:ARTS	Clear to send input
ASCLIN4:ARTS	to	ASCLIN4:ACTSD	Ready to send output
ASCLIN4:ARXA	from	P00.12:IN	Receive input
ASCLIN4:ARXB	from	P34.2:IN	Receive input
ASCLIN4:ARXC	from	P22.6:IN	Receive input
ASCLIN4:ARXD	from	P22.9:IN	Receive input
ASCLIN4:ASCLK	to	P00.10:ALT(2) P22.7:ALT(2) P34.3:ALT(2)	Shift clock output
ASCLIN4:ASLSO	to	P00.11:ALT(2) P22.4:ALT(2) P22.11:ALT(2) P34.4:ALT(2)	Slave select signal output
ASCLIN4:ATX	to	P00.9:ALT(5) P22.5:ALT(2) P22.10:ALT(2) P34.1:ALT(2)	Transmit output
ASCLIN4:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN4:TX_INT	to	INT:asclin4.TX_INT	ASCLIN Transmit Service Request
ASCLIN4:RX_INT	to	INT:asclin4.RX_INT	ASCLIN Receive Service Request
ASCLIN4:ERR_INT	to	INT:asclin4.ERR_INT	ASCLIN Error Service Request

**Table 392 Connections of ASCLIN5**

Interface Signals	connects		Description
ASCLIN5:ACTSD	from	ASCLIN5:ARTS	Clear to send input
ASCLIN5:ARTS	to	ASCLIN5:ACTSD	Ready to send output
ASCLIN5:ARXA	from	P00.6:IN	Receive input
ASCLIN5:ARXB	from	P33.4:IN	Receive input
ASCLIN5:ARXC	from	P22.3:IN	Receive input
ASCLIN5:ARXD	from	P14.15:IN	Receive input
ASCLIN5:ASCLK	to	P14.12:ALT(2) P22.8:ALT(2) P33.3:ALT(2)	Shift clock output

## Asynchronous Serial Interface (ASCLIN)

**Table 392 Connections of ASCLIN5 (cont'd)**

Interface Signals	connects		Description
ASCLIN5:ASLSO	to	P14.8:ALT(2)	Slave select signal output
		P33.5:ALT(7)	
ASCLIN5:ATX	to	P00.7:ALT(2)	Transmit output
		P14.14:ALT(2)	
		P22.2:ALT(2)	
		P33.0:ALT(2)	
ASCLIN5:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN5:TX_INT	to	INT:asclin5.TX_INT	ASCLIN Transmit Service Request
ASCLIN5:RX_INT	to	INT:asclin5.RX_INT	ASCLIN Receive Service Request
ASCLIN5:ERR_INT	to	INT:asclin5.ERR_INT	ASCLIN Error Service Request

**Table 393 Connections of ASCLIN6**

Interface Signals	connects		Description
ASCLIN6:ACTSD	from	ASCLIN6:ARTS	Clear to send input
ASCLIN6:ARTS	to	ASCLIN6:ACTSD	Ready to send output
ASCLIN6:ARXA	from	P23.3:IN	Receive input
ASCLIN6:ARXB	from	P01.0:IN	Receive input
ASCLIN6:ARXC	from	P32.6:IN	Receive input
ASCLIN6:ARXD	from	P10.9:IN	Receive input
ASCLIN6:ARXE	from	P22.0:IN	Receive input
ASCLIN6:ARXF	from	P23.1:IN	Receive input
ASCLIN6:ASCLK	to	P02.14:ALT(2)	Shift clock output
		P10.11:ALT(2)	
		P23.1:ALT(7)	
ASCLIN6:ASLSO	to	P02.12:ALT(4)	Slave select signal output
		P10.13:ALT(2)	
		P23.4:ALT(2)	
ASCLIN6:ATX	to	P01.1:ALT(4)	Transmit output
		P02.15:ALT(4)	
		P10.10:ALT(2)	
		P22.0:ALT(7)	
		P23.5:ALT(2)	
		P32.7:ALT(2)	
ASCLIN6:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN6:TX_INT	to	INT:asclin6.TX_INT	ASCLIN Transmit Service Request
ASCLIN6:RX_INT	to	INT:asclin6.RX_INT	ASCLIN Receive Service Request
ASCLIN6:ERR_INT	to	INT:asclin6.ERR_INT	ASCLIN Error Service Request

**Asynchronous Serial Interface (ASCLIN)**
**Table 394 Connections of ASCLIN7**

Interface Signals	connects		Description
ASCLIN7:ACTSD	from	ASCLIN7:ARTS	Clear to send input
ASCLIN7:ARTS	to	ASCLIN7:ACTSD	Ready to send output
ASCLIN7:ARXA	from	P14.15:IN	Receive input
ASCLIN7:ARXB	from	P01.8:IN	Receive input
ASCLIN7:ARXC	from	P23.2:IN	Receive input
ASCLIN7:ARXD	from	P13.11:IN	Receive input
ASCLIN7:ARXE	from	P22.1:IN	Receive input
ASCLIN7:ARXF	from	P22.4:IN	Receive input
ASCLIN7:ASCLK	to	P01.10:ALT(2) P13.13:ALT(2) P14.12:ALT(3)	Shift clock output
ASCLIN7:ASLSO	to	P01.11:ALT(2) P13.15:ALT(2) P14.8:ALT(3)	Slave select signal output
ASCLIN7:ATX	to	P01.9:ALT(2) P01.12:ALT(2) P13.12:ALT(2) P14.14:ALT(3) P22.1:ALT(7) P23.3:ALT(2)	Transmit output
ASCLIN7:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN7:TX_INT	to	INT:asclin7.TX_INT	ASCLIN Transmit Service Request
ASCLIN7:RX_INT	to	INT:asclin7.RX_INT	ASCLIN Receive Service Request
ASCLIN7:ERR_INT	to	INT:asclin7.ERR_INT	ASCLIN Error Service Request

**Table 395 Connections of ASCLIN8**

Interface Signals	connects		Description
ASCLIN8:ACTSD	from	ASCLIN8:ARTS	Clear to send input
ASCLIN8:ARTS	to	ASCLIN8:ACTSD	Ready to send output
ASCLIN8:ARXA	from	P02.9:IN	Receive input
ASCLIN8:ARXB	from	P02.10:IN	Receive input
ASCLIN8:ARXC	from	P33.1:IN	Receive input
ASCLIN8:ARXD	from	P33.6:IN	Receive input
ASCLIN8:ARXE	from	P34.5:IN	Receive input
ASCLIN8:ASCLK	to	P02.8:ALT(3)	Shift clock output
ASCLIN8:ASLSO	to	P02.11:ALT(3)	Slave select signal output

## Asynchronous Serial Interface (ASCLIN)

**Table 395 Connections of ASCLIN8 (cont'd)**

Interface Signals	connects		Description
ASCLIN8:ATX	to	P02.9:ALT(3)	Transmit output
		P33.7:ALT(4)	
		P34.5:ALT(2)	
ASCLIN8:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN8:TX_INT	to	INT:asclin8.TX_INT	ASCLIN Transmit Service Request
ASCLIN8:RX_INT	to	INT:asclin8.RX_INT	ASCLIN Receive Service Request
ASCLIN8:ERR_INT	to	INT:asclin8.ERR_INT	ASCLIN Error Service Request

**Table 396 Connections of ASCLIN9**

Interface Signals	connects		Description
ASCLIN9:ACTSD	from	ASCLIN9:ARTS	Clear to send input
ASCLIN9:ARTS	to	ASCLIN9:ACTSD	Ready to send output
ASCLIN9:ARXA	from	P01.5:IN	Receive input
ASCLIN9:ARXB	from	P01.7:IN	Receive input
ASCLIN9:ARXC	from	P14.7:IN	Receive input
ASCLIN9:ARXD	from	P14.9:IN	Receive input
ASCLIN9:ARXE	from	P20.6:IN	Receive input
ASCLIN9:ARXF	from	P20.7:IN	Receive input
ASCLIN9:ASCLK	to	P01.6:ALT(3)	Shift clock output
ASCLIN9:ASLSO	to	P01.4:ALT(3)	Slave select signal output
ASCLIN9:ATX	to	P01.7:ALT(3)	Transmit output
		P14.7:ALT(4)	
		P20.7:ALT(2)	
ASCLIN9:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN9:TX_INT	to	INT:asclin9.TX_INT	ASCLIN Transmit Service Request
ASCLIN9:RX_INT	to	INT:asclin9.RX_INT	ASCLIN Receive Service Request
ASCLIN9:ERR_INT	to	INT:asclin9.ERR_INT	ASCLIN Error Service Request

**Table 397 Connections of ASCLIN10**

Interface Signals	connects		Description
ASCLIN10:ACTSD	from	ASCLIN10:ARTS	Clear to send input
ASCLIN10:ARTS	to	ASCLIN10:ACTSD	Ready to send output
ASCLIN10:ARXA	from	P00.4:IN	Receive input
ASCLIN10:ARXB	from	P00.8:IN	Receive input
ASCLIN10:ARXC	from	P13.0:IN	Receive input
ASCLIN10:ARXD	from	P13.1:IN	Receive input
ASCLIN10:ASCLK	to	P13.2:ALT(2)	Shift clock output
ASCLIN10:ASLSO	to	P13.3:ALT(2)	Slave select signal output

## Asynchronous Serial Interface (ASCLIN)

**Table 397 Connections of ASCLIN10 (cont'd)**

Interface Signals	connects		Description
ASCLIN10:ATX	to	P00.8:ALT(3)	Transmit output
		P13.0:ALT(2)	
ASCLIN10:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN10:TX_INT	to	INT:asclin10.TX_INT	ASCLIN Transmit Service Request
ASCLIN10:RX_INT	to	INT:asclin10.RX_INT	ASCLIN Receive Service Request
ASCLIN10:ERR_INT	to	INT:asclin10.ERR_INT	ASCLIN Error Service Request

**Table 398 Connections of ASCLIN11**

Interface Signals	connects		Description
ASCLIN11:ACTSD	from	ASCLIN11:ARTS	Clear to send input
ASCLIN11:ARTS	to	ASCLIN11:ACTSD	Ready to send output
ASCLIN11:ARXA	from	P10.0:IN	Receive input
ASCLIN11:ARXB	from	P10.4:IN	Receive input
ASCLIN11:ARXC	from	P21.0:IN	Receive input
ASCLIN11:ARXD	from	P21.1:IN	Receive input
ASCLIN11:ARXE	from	P21.2:IN	Receive input
ASCLIN11:ARXF	from	P21.5:IN	Receive input
ASCLIN11:ASCLK	to	P21.3:ALT(2)	Shift clock output
ASCLIN11:ASLSO	to	P21.4:ALT(2)	Slave select signal output
ASCLIN11:ATX	to	P10.0:ALT(2)	Transmit output
		P21.0:ALT(2)	
		P21.5:ALT(3)	
ASCLIN11:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN11:TX_INT	to	INT:asclin11.TX_INT	ASCLIN Transmit Service Request
ASCLIN11:RX_INT	to	INT:asclin11.RX_INT	ASCLIN Receive Service Request
ASCLIN11:ERR_INT	to	INT:asclin11.ERR_INT	ASCLIN Error Service Request

## 34.5 Revision History

**Table 399 Revision History**

Reference	Change to Previous Version	Comment
V3.2.6		
Page 2	Register tables updated.	
	No functional change in connectivity tables.	
V3.2.7	- No functional changes.	
V3.2.8	- No functional changes.	

**RESTRICTED**

**AURIX™ TC39x-B**

**NDA Required**



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**Asynchronous Serial Interface (ASCLIN)**

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**Queued Synchronous Peripheral Interface (QSPI)****35      Queued Synchronous Peripheral Interface (QSPI)****35.1    TC39x-B Specific IP Configuration****Table 400   TC39x-B specific configuration of QSPI**

Parameter	QSPI0	QSPI1	QSPI2	QSPI3	QSPI4	QSPI5
<b>QSPI module has HSIC</b>			X	X		

## Queued Synchronous Peripheral Interface (QSPI)

### 35.2 TC39x-B Specific Register Set

**Table 401 Register Address Space - QSPI**

Module	Base Address	End Address	Note
QSPI0	F0001C00 <sub>H</sub>	F0001CFF <sub>H</sub>	Register block QSPI0
QSPI1	F0001D00 <sub>H</sub>	F0001dff <sub>H</sub>	Register block QSPI1
QSPI2	F0001E00 <sub>H</sub>	F0001EFF <sub>H</sub>	Register block QSPI2
QSPI3	F0001F00 <sub>H</sub>	F0001FFF <sub>H</sub>	Register block QSPI3
QSPI4	F0002000 <sub>H</sub>	F00020FF <sub>H</sub>	Register block QSPI4
QSPI5	F0002100 <sub>H</sub>	F00021FF <sub>H</sub>	Register block QSPI5

### Register Overview Tables of QSPI

**Table 402 Register Overview - QSPI0 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_PISEL	Port Input Select Register	004 <sub>H</sub>	U,SV	SV,P	Application Reset	<a href="#">14</a>
QSPI0_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI0_GLOBALCON	Global Configuration Register	010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_GLOBALCON1	Global Configuration Register 1	014 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_BACON	Basic Configuration Register	018 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI0_ECONz (z=0-7)	Configuration Extension z	020 <sub>H</sub> +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_STATUS	Status Register	040 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_STATUS1	Status Register 1	044 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_SSOC	Slave Select Output Control Register	048 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

Table 402 Register Overview - QSPI0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_FLAGSCLEAR	Flags Clear Register	054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_XXLCON	Extra Large Data Configuration Register	058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_MIXENTRY	MIX_ENTRY Register	05C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_BACONENTRY	BACON_ENTRY Register	060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_DATAENTRYRYx (x=0-7)	DATA_ENTRY Register x	064 <sub>H</sub> +x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_RXEXIT	RX_EXIT Register	090 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI0_RXEXITID	RX_EXIT Debug Register	094 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI0_MC	Move Counter Register	0A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_MCCON	Move Counter control Register	0A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_OCS	OCDS Control and Status	0E8 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
QSPI0_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

**Table 402 Register Overview - QSPI0 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
QSPI0_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
QSPI0_ACCEN0	Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

**Table 403 Register Overview - QSPI1 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
QSPI1_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_PISEL	Port Input Select Register	004 <sub>H</sub>	U,SV	SV,P	Application Reset	<b>15</b>
QSPI1_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI1_GLOBALCON	Global Configuration Register	010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_GLOBALCON1	Global Configuration Register 1	014 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_BACON	Basic Configuration Register	018 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI1_ECONz (z=0-7)	Configuration Extension z	020 <sub>H</sub> +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_STATUS	Status Register	040 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_STATUS1	Status Register 1	044 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_SSOC	Slave Select Output Control Register	048 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_FLAGSCLR	Flags Clear Register	054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

**Table 403 Register Overview - QSPI1 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
QSPI1_XXLCON	Extra Large Data Configuration Register	058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_MIXENTRY	MIX_ENTRY Register	05C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_BACONENTRY	BACON_ENTRY Register	060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_DATAENTRYR <sub>x</sub> (x=0-7)	DATA_ENTRY Register x	064 <sub>H</sub> +x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_RXEXIT	RX_EXIT Register	090 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI1_RXEXITD	RX_EXIT Debug Register	094 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI1_MC	Move Counter Register	0A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_MCCON	Move Counter control Register	0A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_OCS	OCDS Control and Status	0E8 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
QSPI1_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
QSPI1_ACCEN0	Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

**Table 404 Register Overview - QSPI2 (ascending Offset Address)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
QSPI2_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_PISEL	Port Input Select Register	004 <sub>H</sub>	U,SV	SV,P	Application Reset	<b>16</b>
QSPI2_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI2_GLOBALCON	Global Configuration Register	010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_GLOBALCON1	Global Configuration Register 1	014 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_BACON	Basic Configuration Register	018 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI2_ECONz (z=0-7)	Configuration Extension z	020 <sub>H</sub> +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_STATUS	Status Register	040 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_STATUS1	Status Register 1	044 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_SSOC	Slave Select Output Control Register	048 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_FLAGSCLR	Flags Clear Register	054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_XXLCON	Extra Large Data Configuration Register	058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MIXENTRY	MIX_ENTRY Register	05C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_BACONENTRY	BACON_ENTRY Register	060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

Table 404 Register Overview - QSPI2 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI2_DATAENT RYx (x=0-7)	DATA_ENTRY Register x	064 <sub>H</sub> +x* 4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_RXEXIT	RX_EXIT Register	090 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI2_RXEXITD	RX_EXIT Debug Register	094 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI2_CAPCON	Capture Control Register	0A0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MC	Move Counter Register	0A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MCCON	Move Counter control Register	0A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_OCS	OCDS Control and Status	0E8 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
QSPI2_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
QSPI2_ACCEN0	Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

**Table 405 Register Overview - QSPI3 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI3_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_PISEL	Port Input Select Register	004 <sub>H</sub>	U,SV	SV,P	Application Reset	<b>17</b>
QSPI3_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI3_GLOBALCON	Global Configuration Register	010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_GLOBALCON1	Global Configuration Register 1	014 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_BACON	Basic Configuration Register	018 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI3_ECONz (z=0-7)	Configuration Extension z	020 <sub>H</sub> +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_STATUS	Status Register	040 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_STATUS1	Status Register 1	044 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_SSOC	Slave Select Output Control Register	048 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_FLAGSCLEAR	Flags Clear Register	054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_XXLCON	Extra Large Data Configuration Register	058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MIXENTRY	MIX_ENTRY Register	05C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_BACONENTRY	BACON_ENTRY Register	060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

**Table 405 Register Overview - QSPI3 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
QSPI3_DATAENT RYx (x=0-7)	DATA_ENTRY Register x	064 <sub>H</sub> +x* 4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_RXEXIT	RX_EXIT Register	090 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI3_RXEXITD	RX_EXIT Debug Register	094 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI3_CAPCON	Capture Control Register	0A0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MC	Move Counter Register	0A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MCCON	Move Counter control Register	0A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_OCS	OCDS Control and Status	0E8 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
QSPI3_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
QSPI3_ACCEN0	Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

**Table 406 Register Overview - QSPI4 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI4_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI4_PISEL	Port Input Select Register	004 <sub>H</sub>	U,SV	SV,P	Application Reset	<b>19</b>
QSPI4_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI4_GLOBALCON	Global Configuration Register	010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI4_GLOBALCON1	Global Configuration Register 1	014 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI4_BACON	Basic Configuration Register	018 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI4_ECONz (z=0-7)	Configuration Extension z	020 <sub>H</sub> +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI4_STATUS	Status Register	040 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_STATUS1	Status Register 1	044 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_SSOC	Slave Select Output Control Register	048 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI4_FLAGSCLEAR	Flags Clear Register	054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_XXLCON	Extra Large Data Configuration Register	058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_MIXENTRY	MIX_ENTRY Register	05C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_BACONENTRY	BACON_ENTRY Register	060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

Table 406 Register Overview - QSPI4 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI4_DATAENT RYx (x=0-7)	DATA_ENTRY Register x	064 <sub>H</sub> +x* 4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_RXEXIT	RX_EXIT Register	090 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI4_RXEXITD	RX_EXIT Debug Register	094 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI4_MC	Move Counter Register	0A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_MCCON	Move Counter control Register	0A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI4_OCS	OCDS Control and Status	0E8 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
QSPI4_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI4_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI4_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI4_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
QSPI4_ACCEN0	Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

Table 407 Register Overview - QSPI5 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI5_CLC	Clock Control Register	000 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI5_PISEL	Port Input Select Register	004 <sub>H</sub>	U,SV	SV,P	Application Reset	20

## Queued Synchronous Peripheral Interface (QSPI)

Table 407 Register Overview - QSPI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI5_ID	Module Identification Register	008 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI5_GLOBALCON	Global Configuration Register	010 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI5_GLOBALCON1	Global Configuration Register 1	014 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI5_BACON	Basic Configuration Register	018 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI5_ECONz (z=0-7)	Configuration Extension z	020 <sub>H</sub> +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI5_STATUS	Status Register	040 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_STATUS1	Status Register 1	044 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_SSOC	Slave Select Output Control Register	048 <sub>H</sub>	U,SV	SV,P	Application Reset	See Family Spec
QSPI5_FLAGSCLEAR	Flags Clear Register	054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_XXLCON	Extra Large Data Configuration Register	058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_MIXENTRY	MIX_ENTRY Register	05C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_BACONENTRY	BACON_ENTRY Register	060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_DATAENTRYR <sub>x</sub> (x=0-7)	DATA_ENTRY Register x	064 <sub>H</sub> +x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_RXEXIT	RX_EXIT Register	090 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

**Table 407 Register Overview - QSPI5 (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
QSPI5_RXEXITD	RX_EXIT Debug Register	094 <sub>H</sub>	U,SV	BE	Application Reset	See Family Spec
QSPI5_MC	Move Counter Register	0A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_MCCON	Move Counter control Register	0A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI5_OCS	OCDS Control and Status	0E8 <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
QSPI5_KRSTCLR	Kernel Reset Status Clear Register	0EC <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI5_KRST1	Kernel Reset Register 1	0F0 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI5_KRST0	Kernel Reset Register 0	0F4 <sub>H</sub>	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI5_ACCEN1	Access Enable Register 1	0F8 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
QSPI5_ACCENO	Access Enable Register 0	0FC <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec

## Queued Synchronous Peripheral Interface (QSPI)

### 35.3 TC39x-B Specific Registers

#### 35.3.1 Register block QSPI

##### Port Input Select Register

The PISEL register controls the input signal selection of the SSC module.

**QSPI0\_PISEL**

**Port Input Select Register** **(004<sub>H</sub>)** **Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	<b>SLSIS</b>			0	<b>SCIS</b>			0	<b>SRIS</b>			0	<b>MRIS</b>		
r	rw	r		rw	r	rw	r	rw	r	rw	r	rw	r	rw	

Field	Bits	Type	Description
<b>MRIS</b>	2:0	rw	<b>Master Mode Receive Input Select</b> MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) <b>000<sub>B</sub> P20.12,</b> <b>001<sub>B</sub> P22.9,</b> <b>010<sub>B</sub> P22.6,</b>
<b>SRIS</b>	6:4	rw	<b>Slave Mode Receive Input Select</b> SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) <b>000<sub>B</sub> P20.14,</b> <b>001<sub>B</sub> P22.10,</b> <b>010<sub>B</sub> P22.5,</b>
<b>SCIS</b>	10:8	rw	<b>Slave Mode Clock Input Select</b> SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) <b>000<sub>B</sub> P20.11,</b> <b>001<sub>B</sub> P22.8,</b> <b>010<sub>B</sub> P22.7,</b>

## Queued Synchronous Peripheral Interface (QSPI)

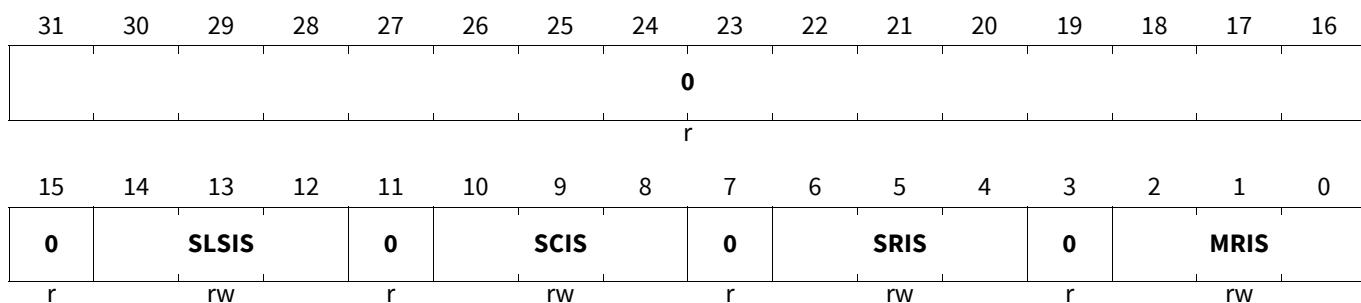
Field	Bits	Type	Description
<b>SLSIS</b>	14:12	rw	<b>Slave Mode Slave Select Input Selection</b> The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) $000_B$ no input $001_B$ <b>P20.13</b> , $010_B$ <b>P20.9</b> ,
<b>0</b>	3, 7, 11, 31:15	r	<b>Reserved</b> Read as 0; should be written with 0.

### QSPI1\_PISEL

#### Port Input Select Register

(004<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>



Field	Bits	Type	Description
<b>MRIS</b>	2:0	rw	<b>Master Mode Receive Input Select</b> MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) $000_B$ <b>P10.1</b> , $001_B$ <b>P11.3</b> ,
<b>SRIS</b>	6:4	rw	<b>Slave Mode Receive Input Select</b> SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) $000_B$ <b>P10.3</b> , $001_B$ <b>P11.9</b> , $010_B$ <b>P10.4</b> ,

## Queued Synchronous Peripheral Interface (QSPI)

Field	Bits	Type	Description
<b>SCIS</b>	10:8	rw	<p><b>Slave Mode Clock Input Select</b></p> <p>SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p><math>000_B</math> <b>P10.2</b>,  <math>001_B</math> <b>P11.6</b>,</p>
<b>SLSIS</b>	14:12	rw	<p><b>Slave Mode Slave Select Input Selection</b></p> <p>The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p><math>000_B</math> no input  <math>001_B</math> <b>P11.10</b>,</p>
<b>0</b>	3, 7, 11, 31:15	r	<p><b>Reserved</b></p> <p>Read as 0; should be written with 0.</p>

### QSPI2\_PISEL

#### Port Input Select Register

(004<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>SLSIS</b>			<b>0</b>	<b>SCIS</b>			<b>0</b>	<b>SRIS</b>			<b>0</b>	<b>MRIS</b>		
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw		

Field	Bits	Type	Description
<b>MRIS</b>	2:0	rw	<p><b>Master Mode Receive Input Select</b></p> <p>MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p><math>000_B</math> <b>P15.4</b>,  <math>001_B</math> <b>P15.7</b>,  <math>010_B</math> <b>P21.3 P21.2</b>,  <math>011_B</math> <b>P34.4</b>,  <math>100_B</math> <b>P15.2</b>,  <math>101_B</math> <b>P14.10 P14.9</b>,</p>

## Queued Synchronous Peripheral Interface (QSPI)

Field	Bits	Type	Description
<b>SRIS</b>	6:4	rw	<b>Slave Mode Receive Input Select</b> SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) $000_B$ <b>P15.5</b> , $001_B$ <b>P15.6</b> , $011_B$ <b>P34.5</b> ,
<b>SCIS</b>	10:8	rw	<b>Slave Mode Clock Input Select</b> SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) $000_B$ <b>P15.3</b> , $001_B$ <b>P15.8</b> , $011_B$ <b>P33.14</b> ,
<b>SLSIS</b>	14:12	rw	<b>Slave Mode Slave Select Input Selection</b> The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) $000_B$ no input $001_B$ <b>P15.2</b> , $010_B$ <b>P15.1</b> ,
<b>0</b>	3, 7, 11, 31:15	r	<b>Reserved</b> Read as 0; should be written with 0.

### QSPI3\_PISEL

#### Port Input Select Register

(004<sub>H</sub>)

Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								0							
									r						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0</b>	<b>SLSIS</b>			<b>0</b>	<b>SCIS</b>			<b>0</b>	<b>SRIS</b>			<b>0</b>	<b>MRIS</b>		
r				r				r				r			rw

## Queued Synchronous Peripheral Interface (QSPI)

Field	Bits	Type	Description
<b>MRIS</b>	2:0	rw	<b>Master Mode Receive Input Select</b> MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) $000_B$ <b>P02.5</b> , $001_B$ <b>P10.7</b> , $010_B$ <b>P01.5</b> ,
<b>SRIS</b>	6:4	rw	<b>Slave Mode Receive Input Select</b> SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) $000_B$ <b>P02.6</b> , $001_B$ <b>P10.6</b> , $010_B$ <b>P01.6</b> ,
<b>SCIS</b>	10:8	rw	<b>Slave Mode Clock Input Select</b> SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) $000_B$ <b>P02.7</b> , $001_B$ <b>P10.8</b> , $010_B$ <b>P01.7</b> ,
<b>SLSIS</b>	14:12	rw	<b>Slave Mode Slave Select Input Selection</b> The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) $000_B$ no input $001_B$ <b>P02.4</b> , $010_B$ <b>P01.3</b> ,
<b>0</b>	3, 7, 11, 31:15	r	<b>Reserved</b> Read as 0; should be written with 0.

## Queued Synchronous Peripheral Interface (QSPI)

### QSPI4\_PISEL

#### Port Input Select Register

(004<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	<b>SLSIS</b>		0	<b>SCIS</b>		0	<b>SRIS</b>		0	<b>MRIS</b>		0			
r	rw		r	rw		r	rw		rw	r		r	rw		

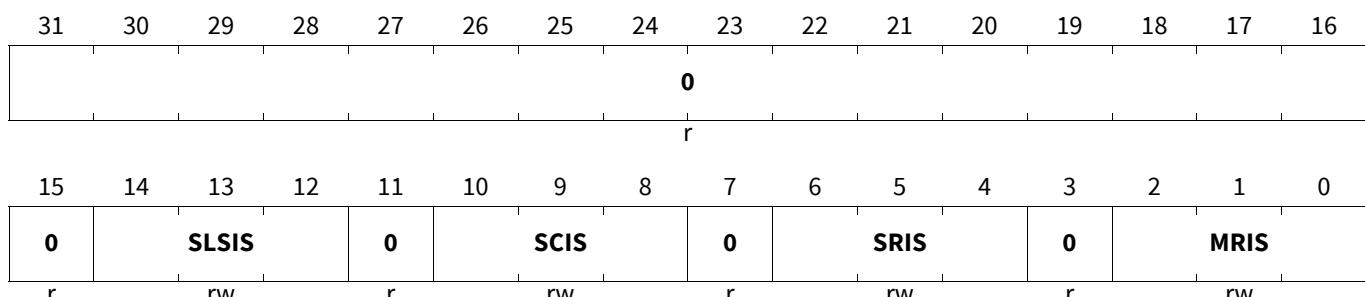
Field	Bits	Type	Description
<b>MRIS</b>	2:0	rw	<b>Master Mode Receive Input Select</b> MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) <b>000<sub>B</sub> P33.13,</b> <b>001<sub>B</sub> P22.1,</b> <b>010<sub>B</sub> P21.3 P21.2,</b> <b>011<sub>B</sub> P21.1 P21.0,</b>
<b>SRIS</b>	6:4	rw	<b>Slave Mode Receive Input Select</b> SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) <b>000<sub>B</sub> P33.12,</b> <b>001<sub>B</sub> P22.0,</b>
<b>SCIS</b>	10:8	rw	<b>Slave Mode Clock Input Select</b> SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) <b>000<sub>B</sub> P33.11,</b> <b>001<sub>B</sub> P22.3,</b>
<b>SLSIS</b>	14:12	rw	<b>Slave Mode Slave Select Input Selection</b> The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) <b>000<sub>B</sub> no input</b> <b>001<sub>B</sub> P33.10,</b> <b>010<sub>B</sub> P22.2,</b>

## Queued Synchronous Peripheral Interface (QSPI)

Field	Bits	Type	Description
0	3, 7, 11, 31:15	r	<b>Reserved</b> Read as 0; should be written with 0.

### QSPI5\_PISEL

#### Port Input Select Register

(004<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

Field	Bits	Type	Description
MRIS	2:0	rw	<b>Master Mode Receive Input Select</b> MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 <sub>B</sub> <b>P15.10</b> , 001 <sub>B</sub> <b>P14.5</b> ,
SRIS	6:4	rw	<b>Slave Mode Receive Input Select</b> SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 <sub>B</sub> <b>P15.14</b> , 001 <sub>B</sub> <b>P14.6</b> ,
SCIS	10:8	rw	<b>Slave Mode Clock Input Select</b> SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 <sub>B</sub> <b>P15.15</b> , 001 <sub>B</sub> <b>P14.13</b> ,

## Queued Synchronous Peripheral Interface (QSPI)

Field	Bits	Type	Description
SLSIS	14:12	rw	<b>Slave Mode Slave Select Input Selection</b> The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) 000 <sub>B</sub> no input 001 <sub>B</sub> <b>P15.11</b> ,
0	3, 7, 11, 31:15	r	<b>Reserved</b> Read as 0; should be written with 0.

### 35.4 Connectivity

The tables below list all the connections of QSPI instances.

**Table 408 Connections of QSPI0**

Interface Signals	connects		Description
QSPI0:MRST	to	IOM:MON2(0)	Slave SPI data output
		IOM:REF2(0)	
		P20.12:ALT(3)	
		P22.6:ALT(4)	
		P22.9:ALT(4)	
QSPI0:MRSTA	from	P20.12:IN	Master SPI data input
QSPI0:MRSTB	from	P22.9:IN	Master SPI data input
QSPI0:MRSTC	from	P22.6:IN	Master SPI data input
QSPI0:MTSR	to	P20.12:ALT(4)	Master SPI data output
		P20.14:ALT(3)	
		P22.5:ALT(4)	
		P22.10:ALT(4)	
QSPI0:MTSRA	from	P20.14:IN	Slave SPI data input
QSPI0:MTSRB	from	P22.10:IN	Slave SPI data input
QSPI0:MTSRC	from	P22.5:IN	Slave SPI data input
QSPI0:SCLK	to	P20.11:ALT(3)	Master SPI clock output
		P20.13:ALT(5)	
		P22.7:ALT(4)	
		P22.8:ALT(4)	
QSPI0:SCLKA	from	P20.11:IN	Slave SPI clock inputs
QSPI0:SCLKB	from	P22.8:IN	Slave SPI clock inputs
QSPI0:SCLKC	from	P22.7:IN	Slave SPI clock inputs
QSPI0:SLSIA	from	P20.13:IN	Slave select input
QSPI0:SLSIB	from	P20.9:IN	Slave select input

## Queued Synchronous Peripheral Interface (QSPI)

**Table 408 Connections of QSPI0 (cont'd)**

Interface Signals	connects		Description
QSPI0:SLSO(0)	to	P20.8:ALT(3)	Master slave select output
QSPI0:SLSO(1)	to	P20.9:ALT(3)	Master slave select output
QSPI0:SLSO(2)	to	P20.13:ALT(3)	Master slave select output
QSPI0:SLSO(3)	to	P11.10:ALT(3)	Master slave select output
QSPI0:SLSO(4)	to	P11.11:ALT(3)	Master slave select output
QSPI0:SLSO(5)	to	P11.2:ALT(3)	Master slave select output
QSPI0:SLSO(6)	to	P20.10:ALT(3)	Master slave select output
QSPI0:SLSO(7)	to	P33.5:ALT(2)	Master slave select output
QSPI0:SLSO(8)	to	P20.6:ALT(3)	Master slave select output
QSPI0:SLSO(9)	to	P20.3:ALT(3)	Master slave select output
QSPI0:SLSO(10)	to	P22.11:ALT(4)	Master slave select output
QSPI0:SLSO(11)	to	P23.6:ALT(4)	Master slave select output
QSPI0:SLSO(12)	to	P22.4:ALT(4)	Master slave select output
QSPI0:SLSO(13)	to	P15.0:ALT(3)	Master slave select output
QSPI0:TX_INT	to	INT:qspi0.TX_INT	QSPI Transmit Service Request
QSPI0:RX_INT	to	INT:qspi0.RX_INT	QSPI Receive Service Request
QSPI0:ERR_INT	to	INT:qspi0.ERR_INT	QSPI Error Service Request
QSPI0:PT_INT	to	INT:qspi0.PT_INT	QSPI Phase Transition Service Request
QSPI0:U_INT	to	INT:qspi0.U_INT	QSPI User Defined Service Request
QSPI0:HC_INT	to	INT:qspi0.HC_INT	QSPI High Speed Capture Service Request

**Table 409 Connections of QSPI1**

Interface Signals	connects		Description
QSPI1:MRST	to	IOM:MON2(1)	Slave SPI data output
		IOM:REF2(1)	
		P10.1:ALT(3)	
		P10.6:ALT(6)	
		P11.3:ALT(3)	
QSPI1:MRSTA	from	P10.1:IN	Master SPI data input
QSPI1:MRSTB	from	P11.3:IN	Master SPI data input
QSPI1:MTSR	to	P10.1:ALT(2)	Master SPI data output
		P10.3:ALT(3)	
		P10.4:ALT(4)	
		P11.9:ALT(3)	
QSPI1:MTSRA	from	P10.3:IN	Slave SPI data input
QSPI1:MTSRB	from	P11.9:IN	Slave SPI data input
QSPI1:MTSRC	from	P10.4:IN	Slave SPI data input

## Queued Synchronous Peripheral Interface (QSPI)

**Table 409 Connections of QSPI1 (cont'd)**

Interface Signals	connects		Description
QSPI1:SCLK	to	P10.2:ALT(3)	Master SPI clock output
		P11.6:ALT(3)	
QSPI1:SCLKA	from	P10.2:IN	Slave SPI clock inputs
QSPI1:SCLKB	from	P11.6:IN	Slave SPI clock inputs
QSPI1:SLSIA	from	P11.10:IN	Slave select input
QSPI1:SLSO(0)	to	P20.8:ALT(4)	Master slave select output
QSPI1:SLSO(1)	to	P20.9:ALT(4)	Master slave select output
QSPI1:SLSO(2)	to	P20.13:ALT(4)	Master slave select output
QSPI1:SLSO(3)	to	P11.10:ALT(4)	Master slave select output
QSPI1:SLSO(4)	to	P11.11:ALT(4)	Master slave select output
QSPI1:SLSO(5)	to	P11.2:ALT(4)	Master slave select output
QSPI1:SLSO(6)	to	P33.10:ALT(2)	Master slave select output
QSPI1:SLSO(7)	to	P33.5:ALT(3)	Master slave select output
QSPI1:SLSO(8)	to	P10.4:ALT(3)	Master slave select output
QSPI1:SLSO(9)	to	P10.5:ALT(4)	Master slave select output
QSPI1:SLSO(10)	to	P10.0:ALT(3)	Master slave select output
QSPI1:TX_INT	to	INT:qspi1.TX_INT	QSPI Transmit Service Request
QSPI1:RX_INT	to	INT:qspi1.RX_INT	QSPI Receive Service Request
QSPI1:ERR_INT	to	INT:qspi1.ERR_INT	QSPI Error Service Request
QSPI1:PT_INT	to	INT:qspi1.PT_INT	QSPI Phase Transition Service Request
QSPI1:U_INT	to	INT:qspi1.U_INT	QSPI User Defined Service Request
QSPI1:HC_INT	to	INT:qspi1.HC_INT	QSPI High Speed Capture Service Request

**Table 410 Connections of QSPI2**

Interface Signals	connects		Description
QSPI2:HSICINA	from	P15.2:IN	Hghspeed capture channel
QSPI2:HSICINB	from	P15.3:IN	Hghspeed capture channel
QSPI2:MRST	to	IOM:MON2(2)	Slave SPI data output
		IOM:REF2(2)	
		P15.4:ALT(3)	
		P15.7:ALT(3)	
		P34.4:ALT(4)	
QSPI2:MRSTA	from	P15.4:IN	Master SPI data input
QSPI2:MRSTB	from	P15.7:IN	Master SPI data input
QSPI2:MRSTCN	from	TC39x-B:P21.2	Master SPI data input (LVDS N line)
QSPI2:MRSTCP	from	TC39x-B:P21.3	Master SPI data input (LVDS P line)
QSPI2:MRSTD	from	P34.4:IN	Master SPI data input
QSPI2:MRSTE	from	P15.2:IN	Master SPI data input

## Queued Synchronous Peripheral Interface (QSPI)

**Table 410 Connections of QSPI2 (cont'd)**

Interface Signals	connects		Description
QSPI2:MRSTFN	from	TC39x-B:P14.9	Master SPI data input (LVDS N line)
QSPI2:MRSTFP	from	TC39x-B:P14.10	Master SPI data input (LVDS P line)
QSPI2:MTSR	to	P13.3:ALT(3)	Master SPI data output
		P15.5:ALT(3)	
		P15.6:ALT(3)	
		P34.5:ALT(4)	
QSPI2:MTSRA	from	P15.5:IN	Slave SPI data input
QSPI2:MTSRB	from	P15.6:IN	Slave SPI data input
QSPI2:MTSRD	from	P34.5:IN	Slave SPI data input
QSPI2:MTSRN	to	TC39x-B:P13.2	Master SPI data output (LVDS N line)
QSPI2:MTSRP	to	TC39x-B:P13.3	Master SPI data output (LVDS P line)
QSPI2:SCLK	to	P13.1:ALT(3)	Master SPI clock output
		P15.3:ALT(3)	
		P15.6:ALT(5)	
		P15.8:ALT(3)	
		P33.1:ALT(3)	
		P33.14:ALT(3)	
QSPI2:SCLKA	from	P15.3:IN	Slave SPI clock inputs
QSPI2:SCLKB	from	P15.8:IN	Slave SPI clock inputs
QSPI2:SCLKD	from	P33.14:IN	Slave SPI clock inputs
QSPI2:SCLKN	to	TC39x-B:P13.0	Master SPI clock output (LVDS N line)
QSPI2:SCLKP	to	TC39x-B:P13.1	Master SPI clock output (LVDS P line)
QSPI2:SLSIA	from	P15.2:IN	Slave select input
QSPI2:SLSIB	from	P15.1:IN	Slave select input
QSPI2:SLSO(0)	to	P15.2:ALT(3)	Master slave select output
QSPI2:SLSO(1)	to	P14.2:ALT(3)	Master slave select output
QSPI2:SLSO(2)	to	P14.6:ALT(3)	Master slave select output
QSPI2:SLSO(3)	to	P14.3:ALT(3)	Master slave select output
QSPI2:SLSO(4)	to	P14.7:ALT(3)	Master slave select output
QSPI2:SLSO(5)	to	P15.1:ALT(3)	Master slave select output
QSPI2:SLSO(6)	to	P33.13:ALT(4)	Master slave select output
QSPI2:SLSO(7)	to	P20.10:ALT(4)	Master slave select output
QSPI2:SLSO(8)	to	P20.6:ALT(4)	Master slave select output
QSPI2:SLSO(9)	to	P20.3:ALT(4)	Master slave select output
QSPI2:SLSO(10)	to	P33.2:ALT(3)	Master slave select output
		P34.3:ALT(4)	
QSPI2:SLSO(11)	to	P33.6:ALT(3)	Master slave select output
		P33.15:ALT(3)	

## Queued Synchronous Peripheral Interface (QSPI)

**Table 410 Connections of QSPI2 (cont'd)**

Interface Signals	connects		Description
QSPI2:SLSO(12)	to	P32.6:ALT(4)	Master slave select output
		P33.4:ALT(3)	
QSPI2:TX_INT	to	INT:qspi2.TX_INT	QSPI Transmit Service Request
QSPI2:RX_INT	to	INT:qspi2.RX_INT	QSPI Receive Service Request
QSPI2:ERR_INT	to	INT:qspi2.ERR_INT	QSPI Error Service Request
QSPI2:PT_INT	to	INT:qspi2.PT_INT	QSPI Phase Transition Service Request
QSPI2:U_INT	to	INT:qspi2.U_INT	QSPI User Defined Service Request
QSPI2:HC_INT	to	INT:qspi2.HC_INT	QSPI High Speed Capture Service Request

**Table 411 Connections of QSPI3**

Interface Signals	connects		Description
QSPI3:HSICINA	from	P33.9:IN	Hightspeed capture channel
QSPI3:HSICINB	from	P33.10:IN	Hightspeed capture channel
QSPI3:MRST	to	IOM:MON2(3)	Slave SPI data output
		IOM:REF2(3)	
		P01.5:ALT(4)	
		P02.5:ALT(3)	
		P10.7:ALT(3)	
QSPI3:MRSTA	from	P02.5:IN	Master SPI data input
QSPI3:MRSTB	from	P10.7:IN	Master SPI data input
QSPI3:MRSTC	from	P01.5:IN	Master SPI data input
QSPI3:MTSR	to	P01.6:ALT(4)	Master SPI data output
		P02.6:ALT(3)	
		P10.6:ALT(3)	
QSPI3:MTSRA	from	P02.6:IN	Slave SPI data input
QSPI3:MTSRB	from	P10.6:IN	Slave SPI data input
QSPI3:MTSRC	from	P01.6:IN	Slave SPI data input
QSPI3:SCLK	to	P01.7:ALT(4)	Master SPI clock output
		P02.7:ALT(3)	
		P10.8:ALT(3)	
QSPI3:SCLKA	from	P02.7:IN	Slave SPI clock inputs
QSPI3:SCLKB	from	P10.8:IN	Slave SPI clock inputs
QSPI3:SCLKC	from	P01.7:IN	Slave SPI clock inputs
QSPI3:SLSIA	from	P02.4:IN	Slave select input
QSPI3:SLSIB	from	P01.3:IN	Slave select input
QSPI3:SLSO(0)	to	P02.4:ALT(3)	Master slave select output
QSPI3:SLSO(1)	to	P02.0:ALT(3)	Master slave select output
QSPI3:SLSO(2)	to	P02.1:ALT(3)	Master slave select output

## Queued Synchronous Peripheral Interface (QSPI)

**Table 411 Connections of QSPI3 (cont'd)**

Interface Signals	connects		Description
QSPI3:SLSO(3)	to	P00.5:ALT(3)	Master slave select output
		P02.2:ALT(3)	
QSPI3:SLSO(4)	to	P00.2:ALT(6)	Master slave select output
		P02.3:ALT(3)	
QSPI3:SLSO(5)	to	P02.8:ALT(2)	Master slave select output
		P02.12:ALT(2)	
QSPI3:SLSO(6)	to	P00.8:ALT(2)	Master slave select output
		P02.15:ALT(2)	
QSPI3:SLSO(7)	to	P00.9:ALT(2)	Master slave select output
		P02.13:ALT(2)	
QSPI3:SLSO(8)	to	P10.5:ALT(3)	Master slave select output
QSPI3:SLSO(9)	to	P01.3:ALT(4)	Master slave select output
QSPI3:SLSO(10)	to	P01.4:ALT(4)	Master slave select output
QSPI3:TX_INT	to	INT:qspi3.TX_INT	QSPI Transmit Service Request
QSPI3:RX_INT	to	INT:qspi3.RX_INT	QSPI Receive Service Request
QSPI3:ERR_INT	to	INT:qspi3.ERR_INT	QSPI Error Service Request
QSPI3:PT_INT	to	INT:qspi3.PT_INT	QSPI Phase Transition Service Request
QSPI3:U_INT	to	INT:qspi3.U_INT	QSPI User Defined Service Request
QSPI3:HC_INT	to	INT:qspi3.HC_INT	QSPI High Speed Capture Service Request

**Table 412 Connections of QSPI4**

Interface Signals	connects		Description
QSPI4:MRST	to	IOM:MON2(4)	Slave SPI data output
		IOM:REF2(4)	
		P22.1:ALT(3)	
		P33.13:ALT(3)	
QSPI4:MRSTA	from	P33.13:IN	Master SPI data input
QSPI4:MRSTB	from	P22.1:IN	Master SPI data input
QSPI4:MRSTCN	from	TC39x-B:P21.2	Master SPI data input (LVDS N line)
QSPI4:MRSTCP	from	TC39x-B:P21.3	Master SPI data input (LVDS P line)
QSPI4:MRSTDN	from	TC39x-B:P21.0	Master SPI data input (LVDS N line)
QSPI4:MRSTDP	from	TC39x-B:P21.1	Master SPI data input (LVDS P line)
QSPI4:MTSR	to	P22.0:ALT(3)	Master SPI data output
		P22.3:ALT(4)	
		P33.12:ALT(3)	
QSPI4:MTSRA	from	P33.12:IN	Slave SPI data input
QSPI4:MTSRB	from	P22.0:IN	Slave SPI data input
QSPI4:MTSRN	to	TC39x-B:P22.2	Master SPI data output (LVDS N line)

## Queued Synchronous Peripheral Interface (QSPI)

**Table 412 Connections of QSPI4 (cont'd)**

Interface Signals	connects		Description
QSPI4:MTSRP	to	TC39x-B:P22.0	Master SPI data output (LVDS P line)
		TC39x-B:P22.3	
QSPI4:SCLK	to	P22.1:ALT(4)	Master SPI clock output
		P22.3:ALT(3)	
		P33.11:ALT(3)	
QSPI4:SCLKA	from	P33.11:IN	Slave SPI clock inputs
QSPI4:SCLKB	from	P22.3:IN	Slave SPI clock inputs
QSPI4:SCLKN	to	TC39x-B:P22.0	Master SPI clock output (LVDS N line)
QSPI4:SCLKP	to	TC39x-B:P22.1	Master SPI clock output (LVDS P line)
		TC39x-B:P22.3	
QSPI4:SLSIA	from	P33.10:IN	Slave select input
QSPI4:SLSIB	from	P22.2:IN	Slave select input
QSPI4:SLSO(0)	to	P33.10:ALT(3)	Master slave select output
QSPI4:SLSO(1)	to	P33.9:ALT(3)	Master slave select output
QSPI4:SLSO(2)	to	P33.3:ALT(3)	Master slave select output
		P33.8:ALT(3)	
QSPI4:SLSO(3)	to	P22.2:ALT(3)	Master slave select output
QSPI4:SLSO(4)	to	P02.12:ALT(3)	Master slave select output
		P23.5:ALT(3)	
QSPI4:SLSO(5)	to	P02.15:ALT(3)	Master slave select output
		P23.4:ALT(3)	
QSPI4:SLSO(6)	to	P02.13:ALT(3)	Master slave select output
		P23.1:ALT(3)	
QSPI4:SLSO(7)	to	P02.1:ALT(2)	Master slave select output
		P33.7:ALT(3)	
QSPI4:TX_INT	to	INT:qspi4.TX_INT	QSPI Transmit Service Request
QSPI4:RX_INT	to	INT:qspi4.RX_INT	QSPI Receive Service Request
QSPI4:ERR_INT	to	INT:qspi4.ERR_INT	QSPI Error Service Request
QSPI4:PT_INT	to	INT:qspi4.PT_INT	QSPI Phase Transition Service Request
QSPI4:U_INT	to	INT:qspi4.U_INT	QSPI User Defined Service Request
QSPI4:HC_INT	to	INT:qspi4.HC_INT	QSPI High Speed Capture Service Request

**Table 413 Connections of QSPI5**

Interface Signals	connects		Description
QSPI5:MRST	to	P14.5:ALT(3)	Slave SPI data output
		P15.10:ALT(3)	
QSPI5:MRSTA	from	P15.10:IN	Master SPI data input
QSPI5:MRSTB	from	P14.5:IN	Master SPI data input

## Queued Synchronous Peripheral Interface (QSPI)

**Table 413 Connections of QSPI5 (cont'd)**

Interface Signals	connects		Description
QSPI5:MTSR	to	P14.6:ALT(2)	Master SPI data output
		P15.14:ALT(3)	
QSPI5:MTSRA	from	P15.14:IN	Slave SPI data input
QSPI5:MTSRB	from	P14.6:IN	Slave SPI data input
QSPI5:SCLK	to	P14.10:ALT(2)	Master SPI clock output
		P14.13:ALT(3)	
		P15.15:ALT(3)	
QSPI5:SCLKA	from	P15.15:IN	Slave SPI clock inputs
QSPI5:SCLKB	from	P14.13:IN	Slave SPI clock inputs
QSPI5:SLSIA	from	P15.11:IN	Slave select input
QSPI5:SLSO(0)	to	P15.13:ALT(3)	Master slave select output
QSPI5:SLSO(1)	to	P15.12:ALT(3)	Master slave select output
QSPI5:SLSO(2)	to	P15.11:ALT(3)	Master slave select output
QSPI5:SLSO(3)	to	P15.6:ALT(4)	Master slave select output
QSPI5:SLSO(4)	to	P13.14:ALT(3)	Master slave select output
QSPI5:SLSO(5)	to	P13.9:ALT(3)	Master slave select output
QSPI5:SLSO(6)	to	P14.12:ALT(6)	Master slave select output
QSPI5:SLSO(7)	to	P14.14:ALT(6)	Master slave select output
QSPI5:SLSO(8)	to	P14.15:ALT(6)	Master slave select output
QSPI5:TX_INT	to	INT:qspi5.TX_INT	QSPI Transmit Service Request
QSPI5:RX_INT	to	INT:qspi5.RX_INT	QSPI Receive Service Request
QSPI5:ERR_INT	to	INT:qspi5.ERR_INT	QSPI Error Service Request
QSPI5:PT_INT	to	INT:qspi5.PT_INT	QSPI Phase Transition Service Request
QSPI5:U_INT	to	INT:qspi5.U_INT	QSPI User Defined Service Request
QSPI5:HC_INT	to	INT:qspi5.HC_INT	QSPI High Speed Capture Service Request

## 35.5 Revision History

**Table 414 Revision History**

Reference	Change to Previous Version	Comment
V3.0.20		
	No functional change.	

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**Single Edge Nibble Transmission (SENT)**

## 36 Single Edge Nibble Transmission (SENT)

This document describes the SENT Interface specific appendix for the product TC39x-B.

### 36.1 TC39x-B Specific IP Configuration

See features in family spec.

**Table 415 TC39x-B specific configuration of SENT**

Parameter	SENT
Number of SENT channels for this device	25

## Single Edge Nibble Transmission (SENT)

### 36.2 TC39x-B Specific Register Set

#### Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

**Table 416 Register Address Space - SENT**

Module	Base Address	End Address	Note
SENT	F0003000 <sub>H</sub>	F003AFF <sub>H</sub>	FPI slave interface

#### Register Overview Table

There are no product specific register for this module.

### 36.3 TC39x-B Specific Registers

There are no product specific register for this module.

### 36.4 Connectivity

This section describes the connectivity of the SENT module.

#### 36.4.1 Interrupt and DMA Controller Service Requests

The trigger outputs of the SENT module are connected via the Interrupt router. The request lines are connected as shown in [Connections of SENT](#).

#### 36.4.2 Trigger Inputs

The module has 8 Sent Channels and the same number of trigger inputs but not more than  $n+1 = 16$ . They can be randomly chosen by programming IOCRx.ETS. The trigger inputs (TRIG[n:0]) of the SENT module are connected to the GTM as shown in [Connections of SENT](#).

#### 36.4.3 Connections of SENT

The tables below list all the connections of SENT instances.

**Table 417 Connections of SENT**

Interface Signals	connects		Description
SENT:SENT0A	from	P40.0:IN	Receive input channel 0
SENT:SENT1A	from	P40.1:IN	Receive input channel 1
SENT:SENT2A	from	P40.2:IN	Receive input channel 2
SENT:SENT3A	from	P40.3:IN	Receive input channel 3
SENT:SENT4A	from	P40.4:IN	Receive input channel 4
SENT:SENT5A	from	P40.5:IN	Receive input channel 5
SENT:SENT6A	from	P40.6:IN	Receive input channel 6
SENT:SENT7A	from	P40.7:IN	Receive input channel 7
SENT:SENT8A	from	P40.8:IN	Receive input channel 8
SENT:SENT9A	from	P40.9:IN	Receive input channel 9

**Single Edge Nibble Transmission (SENT)****Table 417 Connections of SENT (cont'd)**

<b>Interface Signals</b>	<b>connects</b>	<b>Description</b>
SENT:SENT10A	from P40.10:IN	Receive input channel 10
SENT:SENT11A	from P40.11:IN	Receive input channel 11
SENT:SENT12A	from P40.12:IN	Receive input channel 12
SENT:SENT13A	from P40.13:IN	Receive input channel 13
SENT:SENT14A	from P40.14:IN	Receive input channel 14
SENT:SENT15A	from P40.15:IN	Receive input channel 15
SENT:SENT16A	from P41.0:IN	Receive input channel 16
SENT:SENT17A	from P41.1:IN	Receive input channel 17
SENT:SENT18A	from P41.2:IN	Receive input channel 18
SENT:SENT19A	from P41.3:IN	Receive input channel 19
SENT:SENT20A	from P41.4:IN	Receive input channel 20
SENT:SENT21A	from P41.5:IN	Receive input channel 21
SENT:SENT22A	from P41.6:IN	Receive input channel 22
SENT:SENT23A	from P41.7:IN	Receive input channel 23
SENT:SENT24A	from P41.8:IN	Receive input channel 24
SENT:SENT0B	from P00.1:IN	Receive input channel 0
SENT:SENT1B	from P00.2:IN	Receive input channel 1
SENT:SENT2B	from P00.3:IN	Receive input channel 2
SENT:SENT3B	from P00.4:IN	Receive input channel 3
SENT:SENT4B	from P00.5:IN	Receive input channel 4
SENT:SENT5B	from P00.6:IN	Receive input channel 5
SENT:SENT6B	from P00.7:IN	Receive input channel 6
SENT:SENT7B	from P00.8:IN	Receive input channel 7
SENT:SENT8B	from P00.9:IN	Receive input channel 8
SENT:SENT9B	from P00.10:IN	Receive input channel 9
SENT:SENT10B	from P00.11:IN	Receive input channel 10
SENT:SENT11B	from P00.12:IN	Receive input channel 11
SENT:SENT12B	from P02.4:IN	Receive input channel 12
SENT:SENT13B	from P02.3:IN	Receive input channel 13
SENT:SENT14B	from P02.2:IN	Receive input channel 14
SENT:SENT15B	from P01.1:IN	Receive input channel 15
SENT:SENT16B	from P01.9:IN	Receive input channel 16
SENT:SENT17B	from P01.8:IN	Receive input channel 17
SENT:SENT18B	from P01.10:IN	Receive input channel 18
SENT:SENT19B	from P01.11:IN	Receive input channel 19
SENT:SENT20B	from P02.9:IN	Receive input channel 20
SENT:SENT21B	from P02.10:IN	Receive input channel 21
SENT:SENT22B	from P02.11:IN	Receive input channel 22

## Single Edge Nibble Transmission (SENT)

**Table 417 Connections of SENT (cont'd)**

Interface Signals	connects	Description
SENT:SENT23B	from P02.12:IN	Receive input channel 23
SENT:SENT24B	from P02.13:IN	Receive input channel 24
SENT:SENT0C	from P02.8:IN	Receive input channel 0
SENT:SENT1C	from P02.7:IN	Receive input channel 1
SENT:SENT2C	from P02.6:IN	Receive input channel 2
SENT:SENT3C	from P02.5:IN	Receive input channel 3
SENT:SENT4C	from P33.6:IN	Receive input channel 4
SENT:SENT5C	from P33.5:IN	Receive input channel 5
SENT:SENT6C	from P33.4:IN	Receive input channel 6
SENT:SENT7C	from P33.3:IN	Receive input channel 7
SENT:SENT8C	from P33.2:IN	Receive input channel 8
SENT:SENT9C	from P33.1:IN	Receive input channel 9
SENT:SENT10C	from P32.5:IN	Receive input channel 10
SENT:SENT11C	from P32.6:IN	Receive input channel 11
SENT:SENT12C	from P32.7:IN	Receive input channel 12
SENT:SENT13C	from P33.0:IN	Receive input channel 13
SENT:SENT14C	from P33.7:IN	Receive input channel 14
SENT:SENT15C	from P10.9:IN	Receive input channel 15
SENT:SENT16C	from P10.10:IN	Receive input channel 16
SENT:SENT17C	from P10.14:IN	Receive input channel 17
SENT:SENT18C	from P10.13:IN	Receive input channel 18
SENT:SENT19C	from P10.11:IN	Receive input channel 19
SENT:SENT20C	from P31.8:IN	Receive input channel 20
SENT:SENT21C	from P31.9:IN	Receive input channel 21
SENT:SENT22C	from P31.10:IN	Receive input channel 22
SENT:SENT23C	from P31.11:IN	Receive input channel 23
SENT:SENT24C	from P31.12:IN	Receive input channel 24
SENT:SENT10D	from P15.2:IN	Receive input channel 10
SENT:SENT11D	from P15.4:IN	Receive input channel 11
SENT:SENT17D	from P14.0:IN	Receive input channel 17
SENT:SENT18D	from P14.1:IN	Receive input channel 18
SENT:SPC(0)	to P00.1:ALT(6)	Transmit output
SENT:SPC(1)	to P02.7:ALT(6)	Transmit output
SENT:SPC(2)	to P00.3:ALT(6)	Transmit output
SENT:SPC(3)	to P00.4:ALT(6)	Transmit output
SENT:SPC(4)	to P00.5:ALT(6)	Transmit output
SENT:SPC(5)	to P00.6:ALT(6)	Transmit output
SENT:SPC(6)	to P00.7:ALT(6)	Transmit output

## Single Edge Nibble Transmission (SENT)

**Table 417 Connections of SENT (cont'd)**

Interface Signals	connects		Description
SENT:SPC(7)	to	P00.8:ALT(6)	Transmit output
SENT:SPC(8)	to	P00.9:ALT(6)	Transmit output
SENT:SPC(9)	to	P00.10:ALT(6)	Transmit output
SENT:TRIG(15:0)	from	GTM:SENT.TRIG(15:0)	GTM timer output vector
SENT:TRIGO(9:0)	to	INT:sent.TRIGO(9:0)	SENT TRIGO=m Service Request

## 36.5 Revision History

**Table 418 Revision History**

Reference	Change to Previous Version	Comment
<b>V2.1.9</b>		
<a href="#">Page 2</a>	Cross References corrected.	
<a href="#">Page 5</a>	Revision History updated. Removed older versions from Revision History.	
<b>V2.1.10</b>		
<a href="#">Page 1</a>	Second sentence changed to internal audience only due to customer confusion. No functional change.	
<a href="#">Page 2</a>	Minor notation update in connection table, no functional change.	

## Micro Second Channel (MSC)

### 37 Micro Second Channel (MSC)

This chapter describes the Micro Second Channel (MSC) Module of the TC39x-B.

#### 37.1 TC39x-B Specific IP Configuration

See features in family spec.

No product specific configuration for MSC

#### 37.2 TC39x-B Specific Register Set

##### Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

**Table 419 Register Address Space - MSC**

Module	Base Address	End Address	Note
MSC0	F0002600 <sub>H</sub>	F00026FF <sub>H</sub>	FPI slave interface
MSC1	F0002700 <sub>H</sub>	F00027FF <sub>H</sub>	FPI slave interface
MSC2	F0002800 <sub>H</sub>	F00028FF <sub>H</sub>	FPI slave interface
MSC3	F0002900 <sub>H</sub>	F00029FF <sub>H</sub>	FPI slave interface

##### Register Overview Table

There are no product specific register for this module.

#### 37.3 TC39x-B Specific Registers

There are no product specific register for this module.

#### 37.4 Connectivity

The tables below list all the connections of MSC instances.

**Table 420 Connections of MSC0**

Interface Signals	connects		Description
MSC0:EMGSTOPMSC	from	SCU:scu_emgstop	Emergency stop signal from SCU
MSC0:EN(0)	to	P10.2:ALT(4)	Chip Select
		P10.3:ALT(4)	
		P10.4:ALT(5)	
		P11.11:ALT(5)	
		P14.10:ALT(3)	
		P15.5:ALT(5)	

**Micro Second Channel (MSC)****Table 420 Connections of MSC0 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
MSC0:EN(1)	to	P10.1:ALT(4)	Chip Select
		P11.2:ALT(5)	
		P13.0:ALT(4)	
		P14.9:ALT(3)	
		P15.3:ALT(5)	
MSC0:FCLN	to	P13.0:ALT(5)	Shift-clock inverted part of the differential signal
MSC0:FCLP	to	SCU:E_REQ0(3)	Shift-clock direct part of the differential signal
		P11.6:ALT(5)	
		P13.1:ALT(5)	
		P13.2:ALT(4)	
MSC0:INJ0	from	P00.0:IN	Injection signal from port
MSC0:INJ1	from	P10.5:IN	Injection signal from port
MSC0:SDI(0)	from	P11.10:IN	Upstream asynchronous input signal
MSC0:SDI(1)	from	P10.2:IN	Upstream asynchronous input signal
MSC0:SDI(2)	from	P14.3:IN	Upstream asynchronous input signal
MSC0:SDI(3)	from	P11.3:IN	Upstream asynchronous input signal
MSC0:SON	to	P13.2:ALT(5)	Data output - inverted part of the differential signal
MSC0:SOP	to	P11.9:ALT(5)	Data output - direct part of the differential signal
		P13.3:ALT(5)	
MSC0:ALTINL(15:0)	from	GTM:MSC0.ALTINL(15:0)	GTM timer output vector - low part
MSC0:ALTINLEXT(15:0)	from	GTM:MSC0.ALTINLEXT(15:0)	GTM timer output vector - low extension part
MSC0:ALTINH(15:0)	from	GTM:MSC0.ALTINH(15:0)	GTM timer output vector - high part
MSC0:ALTINHEXT(15:0)	from	GTM:MSC0.ALTINHEXT(15:0)	GTM timer output vector - high extension part
MSC0:SR0_INT	to	INT:msc0.SR0_INT	MSC Service Request 0
MSC0:SR1_INT	to	INT:msc0.SR1_INT	MSC Service Request 1
MSC0:SR2_INT	to	INT:msc0.SR2_INT	MSC Service Request 2
MSC0:SR3_INT	to	INT:msc0.SR3_INT	MSC Service Request 3
MSC0:SR4_INT	to	INT:msc0.SR4_INT	MSC Service Request 4

**Table 421 Connections of MSC1**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
MSC1:EMGSTOPMSC	from	SCU:scu_emgstop	Emergency stop signal from SCU
MSC1:EN(0)	to	P23.4:ALT(5)	Chip Select
		P32.4:ALT(5)	
MSC1:EN(1)	to	P23.5:ALT(5)	Chip Select

**Micro Second Channel (MSC)****Table 421 Connections of MSC1 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
MSC1:FCLN	to	P22.0:ALT(5)	Shift-clock inverted part of the differential signal
MSC1:FCLP	to	P22.1:ALT(5)	Shift-clock direct part of the differential signal
MSC1:INJ0	from	P23.3:IN	Injection signal from port
MSC1:INJ1	from	P33.13:IN	Injection signal from port
MSC1:SDI(0)	from	P23.1:IN	Upstream asynchronous input signal
MSC1:SDI(1)	from	P02.3:IN	Upstream asynchronous input signal
MSC1:SDI(2)	from	P32.4:IN	Upstream asynchronous input signal
MSC1:SON	to	P22.2:ALT(5)	Data output - inverted part of the differential signal
MSC1:SOP	to	P22.3:ALT(5)	Data output - direct part of the differential signal
MSC1:ALTINL(15:0)	from	GTM:MSC1.ALTINL(15:0)	GTM timer output vector - low part
MSC1:ALTINLEXT(15:0)	from	GTM:MSC1.ALTINLEXT(15:0)	GTM timer output vector - low extension part
MSC1:ALTINH(15:0)	from	GTM:MSC1.ALTINH(15:0)	GTM timer output vector - high part
MSC1:ALTINHEXT(15:0)	from	GTM:MSC1.ALTINHEXT(15:0)	GTM timer output vector - high extension part
MSC1:SR0_INT	to	INT:msc1.SR0_INT	MSC Service Request 0
MSC1:SR1_INT	to	INT:msc1.SR1_INT	MSC Service Request 1
MSC1:SR2_INT	to	INT:msc1.SR2_INT	MSC Service Request 2
MSC1:SR3_INT	to	INT:msc1.SR3_INT	MSC Service Request 3
MSC1:SR4_INT	to	INT:msc1.SR4_INT	MSC Service Request 4

**Table 422 Connections of MSC2**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
MSC2:EMGSTOPMSC	from	SCU:scu_emgstop	Emergency stop signal from SCU
MSC2:EN(0)	to	P13.4:ALT(4)	Chip Select
		P14.14:ALT(4)	
MSC2:EN(1)	to	P14.13:ALT(4)	Chip Select
MSC2:EN(2)	to	P14.11:ALT(4)	Chip Select
MSC2:FCLN	to	P13.4:ALT(5)	Shift-clock inverted part of the differential signal
MSC2:FCLP	to	P13.5:ALT(5)	Shift-clock direct part of the differential signal
MSC2:INJ0	from	P13.13:IN	Injection signal from port
MSC2:INJ1	from	P14.15:IN	Injection signal from port
MSC2:SDI(0)	from	P14.12:IN	Upstream asynchronous input signal
MSC2:SDI(1)	from	P14.11:IN	Upstream asynchronous input signal

**Micro Second Channel (MSC)****Table 422 Connections of MSC2 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
MSC2:SON	to	P13.6:ALT(5)	Data output - inverted part of the differential signal
MSC2:SOP	to	P13.7:ALT(5)	Data output - direct part of the differential signal
		P14.11:ALT(5)	
MSC2:ALTINL(15:0)	from	GTM:MSC2.ALTINL(15:0)	GTM timer output vector - low part
MSC2:ALTINLEXT(15:0)	from	GTM:MSC2.ALTINLEXT(15:0)	GTM timer output vector - low extension part
MSC2:ALTINH(15:0)	from	GTM:MSC2.ALTINH(15:0)	GTM timer output vector - high part
MSC2:ALTINHEXT(15:0)	from	GTM:MSC2.ALTINHEXT(15:0)	GTM timer output vector - high extension part
MSC2:SR0_INT	to	INT:msc2.SR0_INT	MSC Service Request 0
MSC2:SR1_INT	to	INT:msc2.SR1_INT	MSC Service Request 1
MSC2:SR2_INT	to	INT:msc2.SR2_INT	MSC Service Request 2
MSC2:SR3_INT	to	INT:msc2.SR3_INT	MSC Service Request 3
MSC2:SR4_INT	to	INT:msc2.SR4_INT	MSC Service Request 4

**Table 423 Connections of MSC3**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
MSC3:EMGSTOPMSC	from	SCU:scu_emgstop	Emergency stop signal from SCU
MSC3:EN(0)	to	P15.14:ALT(4)	Chip Select
MSC3:EN(1)	to	P15.15:ALT(4)	Chip Select
MSC3:FCLN	to	P15.10:ALT(4)	Shift-clock inverted part of the differential signal
MSC3:FCLP	to	P15.11:ALT(4)	Shift-clock direct part of the differential signal
MSC3:INJ0	from	P13.11:IN	Injection signal from port
MSC3:INJ1	from	P14.15:IN	Injection signal from port
MSC3:SDI(0)	from	P13.10:IN	Upstream asynchronous input signal
MSC3:SON	to	P15.12:ALT(4)	Data output - inverted part of the differential signal
MSC3:SOP	to	P15.13:ALT(4)	Data output - direct part of the differential signal
MSC3:ALTINL(15:0)	from	GTM:MSC3.ALTINL(15:0)	GTM timer output vector - low part
MSC3:ALTINLEXT(15:0)	from	GTM:MSC3.ALTINLEXT(15:0)	GTM timer output vector - low extension part
MSC3:ALTINH(15:0)	from	GTM:MSC3.ALTINH(15:0)	GTM timer output vector - high part
MSC3:ALTINHEXT(15:0)	from	GTM:MSC3.ALTINHEXT(15:0)	GTM timer output vector - high extension part
MSC3:SR0_INT	to	INT:msc3.SR0_INT	MSC Service Request 0
MSC3:SR1_INT	to	INT:msc3.SR1_INT	MSC Service Request 1

## Micro Second Channel (MSC)

**Table 423 Connections of MSC3 (cont'd)**

Interface Signals	connects		Description
MSC3:SR2_INT	to	INT:msc3.SR2_INT	MSC Service Request 2
MSC3:SR3_INT	to	INT:msc3.SR3_INT	MSC Service Request 3
MSC3:SR4_INT	to	INT:msc3.SR4_INT	MSC Service Request 4

## 37.5 Revision History

**Table 424 Revision History**

Reference	Change to Previous Version	Comment
<b>V5.0.10</b>		
<a href="#">Page 1</a>	Connections table update, no functional change.	
<a href="#">Page 5</a>	Clean up revision history.	

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CAN Interface (MCMCAN)

## 38 CAN Interface (MCMCAN)

This section describes the MCMCAN Interface specific appendix for the product TC39x-B.

### 38.1 TC39x-B Specific IP Configuration

**Table 425** TC39x-B specific configuration of CAN

Parameter	CAN0	CAN1	CAN2
<b>Node size in byte</b>	1024	1024	1024
<b>Number of CAN Nodes</b>	4	4	4
<b>Number of TTCAN Nodes</b>	1		
<b>RAM size in byte</b>	32768	16384	16384
<b>Maximum Number of Standard ID Filter Messages per node</b>	128	128	128
<b>Maximum Number of Extended ID Filter Messages per node</b>	64	64	64
<b>Maximum Number of RxFIFO structures per node</b>	2	2	2
<b>Maximum Number of Messages in a Rx buffer per node</b>	64	64	64
<b>Maximum Number of Tx Event Messages per node</b>	32	32	32
<b>Maximum Number of Tx Messages in a Tx Buffer per node</b>	32	32	32
<b>Maximum Number of Trigger Messages per TTCAN node</b>	64		

---

CAN Interface (MCMCAN)**38.2 TC39x-B Specific Register Set****Register Address Space Table****Table 426 Register Address Space - CAN**

Module	Base Address	End Address	Note
CAN0	F0200000 <sub>H</sub>	F0208FFF <sub>H</sub>	Bus Interface
CAN1	F0210000 <sub>H</sub>	F0218FFF <sub>H</sub>	Bus Interface
CAN2	F0220000 <sub>H</sub>	F0228FFF <sub>H</sub>	Bus Interface

**Register Overview Table****Table 427 Register Overview - CAN (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
CAN0_RAM	Embedded SRAM for messages (008000 <sub>H</sub> Byte)	000000 <sub>H</sub>	
CAN1_RAM	Embedded SRAM for messages (004000 <sub>H</sub> Byte)	000000 <sub>H</sub>	
CAN2_RAM	Embedded SRAM for messages (004000 <sub>H</sub> Byte)	000000 <sub>H</sub>	
CAN0_CLC	CAN Clock Control Register	008000 <sub>H</sub>	See Family Spec
CAN1_CLC	CAN Clock Control Register	008000 <sub>H</sub>	See Family Spec
CAN2_CLC	CAN Clock Control Register	008000 <sub>H</sub>	See Family Spec
CAN0_ID	Module Identification Register	008008 <sub>H</sub>	See Family Spec
CAN1_ID	Module Identification Register	008008 <sub>H</sub>	See Family Spec
CAN2_ID	Module Identification Register	008008 <sub>H</sub>	See Family Spec
CAN0_MCR	Module Control Register	008030 <sub>H</sub>	See Family Spec
CAN1_MCR	Module Control Register	008030 <sub>H</sub>	<b>18</b>

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN2_MCR	Module Control Register	008030 <sub>H</sub>	<a href="#">18</a>
CAN0_BUFAADR	Buffer receive address and transmit address	008034 <sub>H</sub>	See Family Spec
CAN0_MECR	Measure Control Register	008040 <sub>H</sub>	See Family Spec
CAN0_MESTAT	Measure Status Register	008044 <sub>H</sub>	See Family Spec
CAN0_ACCENCTR0	Access Enable Register Control 0	0080DC <sub>H</sub>	See Family Spec
CAN1_ACCENCTR0	Access Enable Register Control 0	0080DC <sub>H</sub>	See Family Spec
CAN2_ACCENCTR0	Access Enable Register Control 0	0080DC <sub>H</sub>	See Family Spec
CAN0_OCS	OCDS Control and Status	0080E8 <sub>H</sub>	See Family Spec
CAN1_OCS	OCDS Control and Status	0080E8 <sub>H</sub>	See Family Spec
CAN2_OCS	OCDS Control and Status	0080E8 <sub>H</sub>	See Family Spec
CAN0_KRSTCLR	Kernel Reset Status Clear Register	0080EC <sub>H</sub>	See Family Spec
CAN1_KRSTCLR	Kernel Reset Status Clear Register	0080EC <sub>H</sub>	See Family Spec
CAN2_KRSTCLR	Kernel Reset Status Clear Register	0080EC <sub>H</sub>	See Family Spec
CAN0_KRST1	Kernel Reset Register 1	0080F0 <sub>H</sub>	See Family Spec
CAN1_KRST1	Kernel Reset Register 1	0080F0 <sub>H</sub>	See Family Spec

**CAN Interface (MCMCAN)****Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN2_KRST1	Kernel Reset Register 1	0080F0 <sub>H</sub>	See Family Spec
CAN0_KRST0	Kernel Reset Register 0	0080F4 <sub>H</sub>	See Family Spec
CAN1_KRST0	Kernel Reset Register 0	0080F4 <sub>H</sub>	See Family Spec
CAN2_KRST0	Kernel Reset Register 0	0080F4 <sub>H</sub>	See Family Spec
CAN0_ACCEN0	Access Enable Register 0	0080FC <sub>H</sub>	See Family Spec
CAN1_ACCEN0	Access Enable Register 0	0080FC <sub>H</sub>	See Family Spec
CAN2_ACCEN0	Access Enable Register 0	0080FC <sub>H</sub>	See Family Spec
CAN0_ACCENODEi0 (i=0-3)	Access Enable Register CAN Node i 0	008100 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_ACCENODEi0 (i=0-3)	Access Enable Register CAN Node i 0	008100 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_ACCENODEi0 (i=0-3)	Access Enable Register CAN Node i 0	008100 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_STARTADRI (i=0-3)	Start Address Node i	008108 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_STARTADRI (i=0-3)	Start Address Node i	008108 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_STARTADRI (i=0-3)	Start Address Node i	008108 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_ENDADRI (i=0-3)	End Address Node i	00810C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN1_ENDADRI (i=0-3)	End Address Node i	00810C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_ENDADRI (i=0-3)	End Address Node i	00810C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_ISREGi (i=0-3)	Interrupt Signalling Register i	008110 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_ISREGi (i=0-3)	Interrupt Signalling Register i	008110 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_ISREGi (i=0-3)	Interrupt Signalling Register i	008110 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_GRINT1i (i=0-3)	Interrupt routing for Groups 1 i	008114 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_GRINT1i (i=0-3)	Interrupt routing for Groups 1 i	008114 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_GRINT1i (i=0-3)	Interrupt routing for Groups 1 i	008114 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_GRINT2i (i=0-3)	Interrupt routing for Groups 2 i	008118 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_GRINT2i (i=0-3)	Interrupt routing for Groups 2 i	008118 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_GRINT2i (i=0-3)	Interrupt routing for Groups 2 i	008118 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NTCCRi (i=0-3)	Node i Timer Clock Control Register	008120 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NTCCRi (i=0-3)	Node i Timer Clock Control Register	008120 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_NTCCRi (i=0-3)	Node i Timer Clock Control Register	008120 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN0_NTATTRi (i=0-3)	Node i Timer A Transmit Trigger Register	008124 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NTATTRi (i=0-3)	Node i Timer A Transmit Trigger Register	008124 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_NTATTRi (i=0-3)	Node i Timer A Transmit Trigger Register	008124 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NTBTRi (i=0-3)	Node i Timer B Transmit Trigger Register	008128 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NTBTRi (i=0-3)	Node i Timer B Transmit Trigger Register	008128 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_NTBTRi (i=0-3)	Node i Timer B Transmit Trigger Register	008128 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NTCTTRi (i=0-3)	Node i Timer C Transmit Trigger Register	00812C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NTCTTRi (i=0-3)	Node i Timer C Transmit Trigger Register	00812C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_NTCTTRi (i=0-3)	Node i Timer C Transmit Trigger Register	00812C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NTRTRi (i=0-3)	Node i Timer Receive Timeout Register	008130 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NTRTRi (i=0-3)	Node i Timer Receive Timeout Register	008130 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_NTRTRi (i=0-3)	Node i Timer Receive Timeout Register	008130 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NPCRi (i=0-3)	Node i Port Control Register	008140 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NPCRi (i=0-3)	Node i Port Control Register	008140 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN2_NPCRi (i=0-3)	Node i Port Control Register	008140 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TTCRi (i=0)	Time Trigger Control Register	0081F0 <sub>H</sub>	See Family Spec
CAN0_CRELi (i=0-3)	Core Release Register i	008200 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_CRELi (i=0-3)	Core Release Register i	008200 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_CRELi (i=0-3)	Core Release Register i	008200 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_ENDNi (i=0-3)	Endian Register i	008204 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_ENDNi (i=0-3)	Endian Register i	008204 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_ENDNi (i=0-3)	Endian Register i	008204 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_DBTPi (i=0-3)	Data Bit Timing & Prescaler Register i	00820C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_DBTPi (i=0-3)	Data Bit Timing & Prescaler Register i	00820C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_DBTPi (i=0-3)	Data Bit Timing & Prescaler Register i	00820C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TESTi (i=0-3)	Test Register i	008210 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TESTi (i=0-3)	Test Register i	008210 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TESTi (i=0-3)	Test Register i	008210 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN0_RWDi (i=0-3)	RAM Watchdog i	008214 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_RWDi (i=0-3)	RAM Watchdog i	008214 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_RWDi (i=0-3)	RAM Watchdog i	008214 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_CCCRi (i=0-3)	CC Control Register i	008218 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_CCCRi (i=0-3)	CC Control Register i	008218 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_CCCRi (i=0-3)	CC Control Register i	008218 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NBTPi (i=0-3)	Nominal Bit Timing & Prescaler Register i	00821C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NBTPi (i=0-3)	Nominal Bit Timing & Prescaler Register i	00821C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_NBTPi (i=0-3)	Nominal Bit Timing & Prescaler Register i	00821C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TSCCI (i=0-3)	Timestamp Counter Configuration i	008220 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TSCCI (i=0-3)	Timestamp Counter Configuration i	008220 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TSCCI (i=0-3)	Timestamp Counter Configuration i	008220 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TSCVi (i=0-3)	Timestamp Counter Value i	008224 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TSCVi (i=0-3)	Timestamp Counter Value i	008224 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN2_TSCVi (i=0-3)	Timestamp Counter Value i	008224 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TOCCI (i=0-3)	Timeout Counter Configuration i	008228 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TOCCI (i=0-3)	Timeout Counter Configuration i	008228 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TOCCI (i=0-3)	Timeout Counter Configuration i	008228 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TOCVi (i=0-3)	Timeout Counter Value i	00822C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TOCVi (i=0-3)	Timeout Counter Value i	00822C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TOCVi (i=0-3)	Timeout Counter Value i	00822C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_ECRi (i=0-3)	Error Counter Register i	008240 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_ECRi (i=0-3)	Error Counter Register i	008240 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_ECRi (i=0-3)	Error Counter Register i	008240 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_PSRI (i=0-3)	Protocol Status Register i	008244 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_PSRI (i=0-3)	Protocol Status Register i	008244 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_PSRI (i=0-3)	Protocol Status Register i	008244 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TDCRI (i=0-3)	Transmitter Delay Compensation Register i	008248 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN1_TDCR <sub>i</sub> (i=0-3)	Transmitter Delay Compensation Register i	008248 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TDCR <sub>i</sub> (i=0-3)	Transmitter Delay Compensation Register i	008248 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_IR <sub>i</sub> (i=0-3)	Interrupt Register i	008250 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_IR <sub>i</sub> (i=0-3)	Interrupt Register i	008250 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_IR <sub>i</sub> (i=0-3)	Interrupt Register i	008250 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_IE <sub>i</sub> (i=0-3)	Interrupt Enable i	008254 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_IE <sub>i</sub> (i=0-3)	Interrupt Enable i	008254 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_IE <sub>i</sub> (i=0-3)	Interrupt Enable i	008254 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_GFC <sub>i</sub> (i=0-3)	Global Filter Configuration i	008280 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_GFC <sub>i</sub> (i=0-3)	Global Filter Configuration i	008280 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_GFC <sub>i</sub> (i=0-3)	Global Filter Configuration i	008280 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_SIDFC <sub>i</sub> (i=0-3)	Standard ID Filter Configuration i	008284 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_SIDFC <sub>i</sub> (i=0-3)	Standard ID Filter Configuration i	008284 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_SIDFC <sub>i</sub> (i=0-3)	Standard ID Filter Configuration i	008284 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN0_XIDFCi (i=0-3)	Extended ID Filter Configuration i	008288 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_XIDFCi (i=0-3)	Extended ID Filter Configuration i	008288 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_XIDFCi (i=0-3)	Extended ID Filter Configuration i	008288 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_XIDAMI (i=0-3)	Extended ID AND Mask i	008290 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_XIDAMI (i=0-3)	Extended ID AND Mask i	008290 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_XIDAMI (i=0-3)	Extended ID AND Mask i	008290 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_HPMSi (i=0-3)	High Priority Message Status i	008294 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_HPMSi (i=0-3)	High Priority Message Status i	008294 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_HPMSi (i=0-3)	High Priority Message Status i	008294 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NDAT1i (i=0-3)	New Data 1 i	008298 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NDAT1i (i=0-3)	New Data 1 i	008298 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_NDAT1i (i=0-3)	New Data 1 i	008298 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_NDAT2i (i=0-3)	New Data 2 i	00829C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_NDAT2i (i=0-3)	New Data 2 i	00829C <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN2_NDAT2i (i=0-3)	New Data 2 i	00829C <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_RXF0Ci (i=0-3)	Rx FIFO 0 Configuration i	0082A0 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_RXF0Ci (i=0-3)	Rx FIFO 0 Configuration i	0082A0 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_RXF0Ci (i=0-3)	Rx FIFO 0 Configuration i	0082A0 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_RXF0Si (i=0-3)	Rx FIFO 0 Status i	0082A4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_RXF0Si (i=0-3)	Rx FIFO 0 Status i	0082A4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_RXF0Si (i=0-3)	Rx FIFO 0 Status i	0082A4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_RXF0Ai (i=0-3)	Rx FIFO 0 Acknowledge i	0082A8 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_RXF0Ai (i=0-3)	Rx FIFO 0 Acknowledge i	0082A8 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_RXF0Ai (i=0-3)	Rx FIFO 0 Acknowledge i	0082A8 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_RXBCi (i=0-3)	Rx Buffer Configuration i	0082AC <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_RXBCi (i=0-3)	Rx Buffer Configuration i	0082AC <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_RXBCi (i=0-3)	Rx Buffer Configuration i	0082AC <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_RXF1Ci (i=0-3)	Rx FIFO 1 Configuration i	0082B0 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec

**CAN Interface (MCMCAN)****Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN1_RXF1Ci (i=0-3)	Rx FIFO 1 Configuration i	0082B0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_RXF1Ci (i=0-3)	Rx FIFO 1 Configuration i	0082B0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_RXF1Si (i=0-3)	Rx FIFO 1 Status i	0082B4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_RXF1Si (i=0-3)	Rx FIFO 1 Status i	0082B4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_RXF1Si (i=0-3)	Rx FIFO 1 Status i	0082B4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_RXF1Ai (i=0-3)	Rx FIFO 1 Acknowledge i	0082B8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_RXF1Ai (i=0-3)	Rx FIFO 1 Acknowledge i	0082B8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_RXF1Ai (i=0-3)	Rx FIFO 1 Acknowledge i	0082B8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_RXESCi (i=0-3)	Rx Buffer/FIFO Element Size Configuration i	0082BC <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_RXESCi (i=0-3)	Rx Buffer/FIFO Element Size Configuration i	0082BC <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_RXESCi (i=0-3)	Rx Buffer/FIFO Element Size Configuration i	0082BC <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXBCi (i=0-3)	Tx Buffer Configuration i	0082C0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TXBCi (i=0-3)	Tx Buffer Configuration i	0082C0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXBCi (i=0-3)	Tx Buffer Configuration i	0082C0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN0_TXFQSi (i=0-3)	Tx FIFO/Queue Status i	0082C4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_TXFQSi (i=0-3)	Tx FIFO/Queue Status i	0082C4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_TXFQSi (i=0-3)	Tx FIFO/Queue Status i	0082C4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_TXESCi (i=0-3)	Tx Buffer Element Size Configuration i	0082C8 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_TXESCi (i=0-3)	Tx Buffer Element Size Configuration i	0082C8 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_TXESCi (i=0-3)	Tx Buffer Element Size Configuration i	0082C8 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_TXBRPi (i=0-3)	Tx Buffer Request Pending i	0082CC <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_TXBRPi (i=0-3)	Tx Buffer Request Pending i	0082CC <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_TXBRPi (i=0-3)	Tx Buffer Request Pending i	0082CC <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_TXBARI (i=0-3)	Tx Buffer Add Request i	0082D0 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_TXBARI (i=0-3)	Tx Buffer Add Request i	0082D0 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN2_TXBARI (i=0-3)	Tx Buffer Add Request i	0082D0 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN0_TXBCRi (i=0-3)	Tx Buffer Cancellation Request i	0082D4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec
CAN1_TXBCRi (i=0-3)	Tx Buffer Cancellation Request i	0082D4 <sub>H</sub> +i*40 0 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN2_TXBCRi (i=0-3)	Tx Buffer Cancellation Request i	0082D4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXBTOi (i=0-3)	Tx Buffer Transmission Occurred i	0082D8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TXBTOi (i=0-3)	Tx Buffer Transmission Occurred i	0082D8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXBTOi (i=0-3)	Tx Buffer Transmission Occurred i	0082D8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXBCFi (i=0-3)	Tx Buffer Cancellation Finished i	0082DC <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TXBCFi (i=0-3)	Tx Buffer Cancellation Finished i	0082DC <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXBCFi (i=0-3)	Tx Buffer Cancellation Finished i	0082DC <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXBIEi (i=0-3)	Tx Buffer Transmission Interrupt Enable i	0082E0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TXBIEi (i=0-3)	Tx Buffer Transmission Interrupt Enable i	0082E0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXBIEi (i=0-3)	Tx Buffer Transmission Interrupt Enable i	0082E0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXBCIEi (i=0-3)	Tx Buffer Cancellation Finished Interrupt Enable i	0082E4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TXBCIEi (i=0-3)	Tx Buffer Cancellation Finished Interrupt Enable i	0082E4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXBCIEi (i=0-3)	Tx Buffer Cancellation Finished Interrupt Enable i	0082E4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXEFCi (i=0-3)	Tx Event FIFO Configuration i	0082F0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN1_TXEFCi (i=0-3)	Tx Event FIFO Configuration i	0082F0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXEFCi (i=0-3)	Tx Event FIFO Configuration i	0082F0 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXEFSi (i=0-3)	Tx Event FIFO Status i	0082F4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TXEFSi (i=0-3)	Tx Event FIFO Status i	0082F4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXEFSi (i=0-3)	Tx Event FIFO Status i	0082F4 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TXEFAi (i=0-3)	Tx Event FIFO Acknowledge i	0082F8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN1_TXEFAi (i=0-3)	Tx Event FIFO Acknowledge i	0082F8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN2_TXEFAi (i=0-3)	Tx Event FIFO Acknowledge i	0082F8 <sub>H</sub> +i*400 <sub>H</sub>	See Family Spec
CAN0_TTTMCi (i=0)	TT Trigger Memory Configuration i	008300 <sub>H</sub>	See Family Spec
CAN0_TTRMCi (i=0)	TT Reference Message Configuration i	008304 <sub>H</sub>	See Family Spec
CAN0_TTOCFi (i=0)	TT Operation Configuration i	008308 <sub>H</sub>	See Family Spec
CAN0_TTMLMi (i=0)	TT Matrix Limits i	00830C <sub>H</sub>	See Family Spec
CAN0_TURCFi (i=0)	TUR Configuration i	008310 <sub>H</sub>	See Family Spec
CAN0_TTOCNI (i=0)	TT Operation Control i	008314 <sub>H</sub>	See Family Spec

## CAN Interface (MCMCAN)

**Table 427 Register Overview - CAN (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
CAN0_TTGTPi (i=0)	TT Global Time Preset i	008318 <sub>H</sub>	See Family Spec
CAN0_TTTMKi (i=0)	TT Time Mark i	00831C <sub>H</sub>	See Family Spec
CAN0_TTIRi (i=0)	TT Interrupt Register i	008320 <sub>H</sub>	See Family Spec
CAN0_TTIEi (i=0)	TT Interrupt Enable i	008324 <sub>H</sub>	See Family Spec
CAN0_TTOSTi (i=0)	TT Operation Status i	00832C <sub>H</sub>	See Family Spec
CAN0_TURNAi (i=0)	TUR Numerator Actual i	008330 <sub>H</sub>	See Family Spec
CAN0_TTLGTi (i=0)	TT Local & Global Time i	008334 <sub>H</sub>	See Family Spec
CAN0_TTCTCi (i=0)	TT Cycle Time & Count i	008338 <sub>H</sub>	See Family Spec
CAN0_TTCPTi (i=0)	TT Capture Time i	00833C <sub>H</sub>	See Family Spec
CAN0_TTCSMi (i=0)	TT Cycle Sync Mark i	008340 <sub>H</sub>	See Family Spec

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**CAN Interface (MCMCAN)**

### 38.3 TC39x-B Specific Registers

#### 38.3.1 Bus Interface

##### Module Control Register

The Module Control Register MCR contains basic settings that determine the operation of the MCMCAN module. The write access to the lowest byte of the MCR register becomes only valid, if and only if, MCR.CCCE and MCR.CI are already set during write access. To switch the clocks on or off, the bits of MCR.CCCE and MCR.CI have to be reset afterwards. Before this sequence hasn't taken place, no write access to the corresponding nodes, can be done.

**Note:** *If the baud rate logic is supplied from an unstable clock source, or no clock at all, the CAN functionality is not guaranteed.*

To be able to change the clock settings the following programming sequence needs to be met:

```
uwTemp = CANn_MCR.U;
uwTemp |= (0xC0000000 | CLKSELx);
CANn_MCR.U = uwTemp;
uwTemp &= ~0xC0000000;
CANn_MCR.U = uwTemp;
```

The clock settings for CAN nodes becomes active.

To be able to start the RAM initialization, the following programming sequence need to be met:

```
CANn_MCR |= 0xC0000000;
Wait until CANn_MCR.RBUSY is 0b
Set CANn_MCR.RINIT to 0b
Set CANn_MCR.RINIT to 1b
Dummy read CANn_MCR
Wait until CANn_MCR.RBUSY is 0b
Set CANn_MCR.RINIT to 0b
CANn_MCR &= ~0xC0000000;
RAM initialization is finished
```

##### CAN1\_MCR

##### Module Control Register

(008030<sub>H</sub>)

**Application Reset Value: 0000 0000<sub>H</sub>**

##### CAN2\_MCR

##### Module Control Register

(008030<sub>H</sub>)

**Application Reset Value: 0000 0000<sub>H</sub>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCCE	CI	RINIT	RBUSY		0						0				
rw	rw	rw	rh		r						r				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0				CLKSEL3	CLKSEL2	CLKSEL1	CLKSEL0				
				r				rw	rw	rw	rw				

## CAN Interface (MCMCAN)

Field	Bits	Type	Description
<b>CLKSEL0</b>	1:0	rw	<b>Clock Select 0</b> This bitfield is MCR.CI and MCR.CCCE protected. 00 <sub>B</sub> No clock supplied 01 <sub>B</sub> The asynchronous clock source is switched on 10 <sub>B</sub> The synchronous clock source is switched on 11 <sub>B</sub> Both clock sources are switched on
<b>CLKSEL1</b>	3:2	rw	<b>Clock Select 1</b> This bitfield is MCR.CI and MCR.CCCE protected. 00 <sub>B</sub> No clock supplied 01 <sub>B</sub> The asynchronous clock source is switched on 10 <sub>B</sub> The synchronous clock source is switched on 11 <sub>B</sub> Both clock sources are switched on
<b>CLKSEL2</b>	5:4	rw	<b>Clock Select 2</b> This bitfield is MCR.CI and MCR.CCCE protected. 00 <sub>B</sub> No clock supplied 01 <sub>B</sub> The asynchronous clock source is switched on 10 <sub>B</sub> The synchronous clock source is switched on 11 <sub>B</sub> Both clock sources are switched on
<b>CLKSEL3</b>	7:6	rw	<b>Clock Select 3</b> This bitfield is MCR.CI and MCR.CCCE protected. 00 <sub>B</sub> No clock supplied 01 <sub>B</sub> The asynchronous clock source is switched on 10 <sub>B</sub> The synchronous clock source is switched on 11 <sub>B</sub> Both clock sources are switched on
<b>RBUSY</b>	28	rh	<b>RAM BUSY</b> This bit shows that the RAM Initialization is running. This bit is set back to 0b by hardware when the RAM intialization is completed.
<b>RINIT</b>	29	rw	<b>RAM Init</b> This bit is MCR.CI and MCR.CCCE protected. This bit starts the initialization of the RAM block to all 0x0. The RAM initialization is started only when this bit is changed from 0b to 1b and also RBUSY is 0b.
<b>CI</b>	30	rw	<b>Change Init</b> Needs to be set to enable and disable clocks. 0 <sub>B</sub> Change Init disabled 1 <sub>B</sub> Change Init enabled (takes effect with CCCE:=1)
<b>CCCE</b>	31	rw	<b>Clock and RAM Change Enable</b> Needs to be set to enable and disable the clocks. 0 <sub>B</sub> Clock and RAM Change disabled 1 <sub>B</sub> Clock and RAM Change enabled (takes effect with CI:=1)
<b>0</b>	23:8, 27:24	r	<b>Reserved</b> Shall read 0; shall be written with 0.

## 38.4 Connectivity

## CAN Interface (MCMCAN)

**Table 428 Connections of CAN0**

Interface Signals	connects		Description
CAN0:DSTDBG	from	DMU:scu_entered_dest_dbg	Destructive Debug entered
CAN0:DXSCLK	to	TCU:dxs_clk	DXS Clock, DAP module clock
CAN0:ECTT(1)	from	P02.4:IN	External CAN time trigger input
CAN0:ECTT(2)	from	P02.5:IN	External CAN time trigger input
CAN0:ECTT(4:3)	from	SCU:scu_iout(3:2)	External CAN time trigger input
CAN0:ECTT(5)	from	ERAY0:TINT0	External CAN time trigger input
CAN0:ECTT(6)	from	ERAY0:TINT1	External CAN time trigger input
CAN0:INT(5:0)	to	HSM:EXT_INT(18:13)	CAN interrupt request
CAN0:INT(12)	to	GTM:TIM0_IN1(13)	CAN interrupt request
		GTM:TIM1_IN1(13)	
		GTM:TIM2_IN1(13)	
		GTM:TIM3_IN1(13)	
		CCU61:CC61IND	
CAN0:INT(13)	to	GTM:TIM0_IN2(13)	CAN interrupt request
		GTM:TIM1_IN2(13)	
		GTM:TIM2_IN2(13)	
		GTM:TIM3_IN2(13)	
CAN0:INT(14)	to	GTM:TIM0_IN3(13)	CAN interrupt request
		GTM:TIM1_IN3(13)	
		GTM:TIM2_IN3(13)	
		GTM:TIM3_IN3(13)	
CAN0:INT(15)	to	GTM:TIM0_IN4(13)	CAN interrupt request
		GTM:TIM1_IN4(13)	
		GTM:TIM2_IN4(13)	
		GTM:TIM3_IN4(13)	
		CCU61:T13HRE	
CAN0:STM0_SR0_INT	from	STM0:SR0_INT	System Timer Service Request 0
CAN0:STM0_SR1_INT	from	STM0:SR1_INT	System Timer Service Request 1
CAN0:STM1_SR0_INT	from	STM1:SR0_INT	System Timer Service Request 0
CAN0:STM1_SR1_INT	from	STM1:SR1_INT	System Timer Service Request 1
CAN0:STM2_SR0_INT	from	STM2:SR0_INT	System Timer Service Request 0
CAN0:STM2_SR1_INT	from	STM2:SR1_INT	System Timer Service Request 1
CAN0:TTCPT_TRIG(4)	from	SCU:scu_iout(4)	Capture time trigger input
CAN0:TRIG(3:0)	from	GTM:CAN0.TRIG(3:0)	GTM timer output vector
CAN0:INT(15:0)	to	INT:mcmcan0.INT(15:0)	CAN Service Request

**CAN Interface (MCMCAN)****Table 429 Connections of CAN00**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN00:RXDA	from	P02.1:IN	CAN receive input node 0
CAN00:RXDB	from	P20.7:IN	CAN receive input node 0
CAN00:RXDC	from	P12.0:IN	CAN receive input node 0
CAN00:RXDD	from	P33.12:IN	CAN receive input node 0
CAN00:RXDE	from	P33.7:IN	CAN receive input node 0
CAN00:RXDF	from	P01.8:IN	CAN receive input node 0
CAN00:RXDG	from	P34.2:IN	CAN receive input node 0
CAN00:RXDH	from	P02.14:IN	CAN receive input node 0
CAN00:TXD	to	IOM:MON2(5) IOM:REF2(5) P01.13:ALT(4) P02.0:ALT(5) P02.13:ALT(4) P12.1:ALT(5) P20.8:ALT(5) P33.8:ALT(5) P33.13:ALT(5) P34.1:ALT(4)	CAN transmit output node 0

**Table 430 Connections of CAN01**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN01:RXDA	from	P15.3:IN	CAN receive input node 1
CAN01:RXDB	from	P14.1:IN	CAN receive input node 1
CAN01:RXDC	from	P01.4:IN	CAN receive input node 1
CAN01:RXDD	from	P33.10:IN	CAN receive input node 1
CAN01:RXDE	from	P02.10:IN	CAN receive input node 1
CAN01:TXD	to	IOM:MON2(6) IOM:REF2(6) P01.3:ALT(5) P02.9:ALT(5) P14.0:ALT(5) P15.2:ALT(5) P33.9:ALT(5)	CAN transmit output node 1

**CAN Interface (MCMCAN)****Table 431 Connections of CAN1**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN1:DSTDBG	from	DMU:scu_entered_dest_dbg	Destructive Debug entered
CAN1:STM0_SR0_INT	from	STM0:SR0_INT	System Timer Service Request 0
CAN1:STM0_SR1_INT	from	STM0:SR1_INT	System Timer Service Request 1
CAN1:STM1_SR0_INT	from	STM1:SR0_INT	System Timer Service Request 0
CAN1:STM1_SR1_INT	from	STM1:SR1_INT	System Timer Service Request 1
CAN1:STM2_SR0_INT	from	STM2:SR0_INT	System Timer Service Request 0
CAN1:STM2_SR1_INT	from	STM2:SR1_INT	System Timer Service Request 1
CAN1:TRIG(3:0)	from	GTM:CAN1.TRIG(3:0)	GTM timer output vector
CAN1:INT(15:0)	to	INT:mcmcan1.INT(15:0)	CAN Service Request

**Table 432 Connections of CAN02**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN02:RXDA	from	P15.1:IN	CAN receive input node 2
CAN02:RXDB	from	P02.3:IN	CAN receive input node 2
CAN02:RXDC	from	P32.6:IN	CAN receive input node 2
CAN02:RXDD	from	P14.8:IN	CAN receive input node 2
CAN02:RXDE	from	P10.2:IN	CAN receive input node 2
CAN02:TXD	to	IOM:MON2(7) IOM:REF2(7) P02.2:ALT(5) P10.3:ALT(6) P14.10:ALT(5) P15.0:ALT(5) P32.5:ALT(6)	CAN transmit output node 2

**Table 433 Connections of CAN2**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN2:DSTDBG	from	DMU:scu_entered_dest_dbg	Destructive Debug entered
CAN2:STM0_SR0_INT	from	STM0:SR0_INT	System Timer Service Request 0
CAN2:STM0_SR1_INT	from	STM0:SR1_INT	System Timer Service Request 1
CAN2:STM1_SR0_INT	from	STM1:SR0_INT	System Timer Service Request 0
CAN2:STM1_SR1_INT	from	STM1:SR1_INT	System Timer Service Request 1
CAN2:STM2_SR0_INT	from	STM2:SR0_INT	System Timer Service Request 0
CAN2:STM2_SR1_INT	from	STM2:SR1_INT	System Timer Service Request 1
CAN2:TRIG(3:0)	from	GTM:CAN2.TRIG(3:0)	GTM timer output vector
CAN2:INT(15:0)	to	INT:mcmcan2.INT(15:0)	CAN Service Request

**CAN Interface (MCMCAN)****Table 434 Connections of CAN03**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN03:RXDA	from	P00.3:IN	CAN receive input node 3
CAN03:RXDB	from	P32.2:IN	CAN receive input node 3
CAN03:RXDC	from	P20.0:IN	CAN receive input node 3
CAN03:RXDD	from	P11.10:IN	CAN receive input node 3
CAN03:RXDE	from	P20.9:IN	CAN receive input node 3
CAN03:RXDF	from	P01.0:IN	CAN receive input node 3
CAN03:TXD	to	IOM:MON2(8) IOM:REF2(8) P00.2:ALT(5) P01.2:ALT(3) P11.12:ALT(5) P20.3:ALT(5) P20.10:ALT(5) P32.3:ALT(5)	CAN transmit output node 3

**Table 435 Connections of CAN10**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN10:RXDA	from	P00.1:IN	CAN receive input node 0
CAN10:RXDB	from	P14.7:IN	CAN receive input node 0
CAN10:RXDC	from	P23.0:IN	CAN receive input node 0
CAN10:RXDD	from	P13.1:IN	CAN receive input node 0
CAN10:TXD	to	P00.0:ALT(5) P13.0:ALT(7) P14.9:ALT(4) P23.1:ALT(5)	CAN transmit output node 0

**Table 436 Connections of CAN11**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN11:RXDA	from	P02.4:IN	CAN receive input node 1
CAN11:RXDB	from	P00.5:IN	CAN receive input node 1
CAN11:RXDC	from	P23.7:IN	CAN receive input node 1
CAN11:RXDD	from	P11.7:IN	CAN receive input node 1
CAN11:TXD	to	P00.4:ALT(3) P02.5:ALT(2) P11.0:ALT(5) P23.6:ALT(5)	CAN transmit output node 1

**CAN Interface (MCMCAN)****Table 437 Connections of CAN12**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN12:RXDA	from	P20.6:IN	CAN receive input node 2
CAN12:RXDB	from	P10.8:IN	CAN receive input node 2
CAN12:RXDC	from	P23.3:IN	CAN receive input node 2
CAN12:RXDD	from	P11.8:IN	CAN receive input node 2
CAN12:TXD	to	P10.7:ALT(6) P11.1:ALT(5) P20.7:ALT(5) P23.2:ALT(5)	CAN transmit output node 2

**Table 438 Connections of CAN13**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN13:RXDA	from	P14.7:IN	CAN receive input node 3
CAN13:RXDB	from	P33.5:IN	CAN receive input node 3
CAN13:RXDC	from	P22.5:IN	CAN receive input node 3
CAN13:RXDD	from	P11.13:IN	CAN receive input node 3
CAN13:TXD	to	P11.4:ALT(5) P14.6:ALT(4) P22.4:ALT(6) P33.4:ALT(7)	CAN transmit output node 3

**Table 439 Connections of CAN20**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN20:RXDA	from	P10.5:IN	CAN receive input node 0
CAN20:RXDB	from	P10.8:IN	CAN receive input node 0
CAN20:RXDC	from	P34.2:IN	CAN receive input node 0
CAN20:RXDD	from	P02.14:IN	CAN receive input node 0
CAN20:RXDE	from	P01.8:IN	CAN receive input node 0
CAN20:RXDF	from	P11.14:IN	CAN receive input node 0
CAN20:TXD	to	P01.13:ALT(5) P02.13:ALT(5) P10.6:ALT(5) P10.7:ALT(5) P11.5:ALT(5) P34.1:ALT(5)	CAN transmit output node 0

**CAN Interface (MCMCAN)****Table 440 Connections of CAN21**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN21:RXDA	from	P00.3:IN	CAN receive input node 1
CAN21:RXDB	from	P13.12:IN	CAN receive input node 1
CAN21:RXDC	from	P20.0:IN	CAN receive input node 1
CAN21:RXDD	from	P32.2:IN	CAN receive input node 1
CAN21:RXDE	from	P01.0:IN	CAN receive input node 1
CAN21:RXDF	from	P22.7:IN	CAN receive input node 1
CAN21:TXD	to	P00.2:ALT(3) P01.2:ALT(5) P13.9:ALT(5) P20.3:ALT(6) P22.6:ALT(5) P32.3:ALT(6)	CAN transmit output node 1

**Table 441 Connections of CAN22**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN22:RXDA	from	P33.13:IN	CAN receive input node 2
CAN22:RXDB	from	P32.7:IN	CAN receive input node 2
CAN22:RXDC	from	P23.6:IN	CAN receive input node 2
CAN22:RXDD	from	P14.14:IN	CAN receive input node 2
CAN22:RXDE	from	P22.9:IN	CAN receive input node 2
CAN22:TXD	to	P14.13:ALT(5) P22.8:ALT(5) P23.5:ALT(6) P32.6:ALT(5) P33.12:ALT(5)	CAN transmit output node 2

**Table 442 Connections of CAN23**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN23:RXDA	from	P14.10:IN	CAN receive input node 3
CAN23:RXDB	from	P23.3:IN	CAN receive input node 3
CAN23:RXDC	from	P14.15:IN	CAN receive input node 3
CAN23:RXDD	from	P13.5:IN	CAN receive input node 3
CAN23:RXDE	from	P22.11:IN	CAN receive input node 3

**CAN Interface (MCMCAN)****Table 442 Connections of CAN23 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
CAN23:TXD	to	P13.4:ALT(7)	CAN transmit output node 3
		P14.9:ALT(2)	
		P14.14:ALT(5)	
		P22.10:ALT(5)	
		P23.2:ALT(4)	

**Note:** For the connectivity of the MCMCAN module to the STM module, please refer to the User Manual, chapter MCMCAN User Interface under CAN Transmit Trigger Inputs section.

**38.5 Revision History****Table 443 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
<b>V1.19.8</b>		
<a href="#">Page 1</a>	Update of “specific configuration of CAN” table.	
<a href="#">Page 18</a>	CAN_MCR register bit field “reserved” fixed.	
<b>V1.19.9</b>		
-	No change for TC39x-B.	
<b>V1.19.10</b>		
<a href="#">Page 26</a>	Added note at the end of connections tables.	
<b>V1.19.11</b>		
-	No functional changes.	
<b>V1.19.12</b>		
<a href="#">Page 1</a>	Update of “specific configuration of CAN” table.	
<b>V1.19.13</b>		
<a href="#">Page 18</a>	Updated information on bit implementation in A-step.	

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**FlexRay™ Protocol Controller (E-Ray)****39        FlexRay™ Protocol Controller (E-Ray)**

Text with reference to family spec.

**39.1      TC39x-B Specific IP Configuration**

No product specific configuration for ERAY

**FlexRay™ Protocol Controller (E-Ray)****39.2 TC39x-B Specific Register Set****Register Address Space Table****Table 444 Register Address Space - ERAY**

Module	Base Address	End Address	Note
ERAY0	F001C000 <sub>H</sub>	F001CFFF <sub>H</sub>	FPI slave interface
ERAY1	F0017000 <sub>H</sub>	F0017FFF <sub>H</sub>	FPI slave interface

**Register Overview Table****Table 445 Register Overview - ERAY (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
ERAY0_CLC	Clock Control Register	0000 <sub>H</sub>	See Family Spec
ERAY1_CLC	Clock Control Register	0000 <sub>H</sub>	See Family Spec
ERAY0_CUST1	Busy and Input Buffer Control Register	0004 <sub>H</sub>	See Family Spec
ERAY1_CUST1	Busy and Input Buffer Control Register	0004 <sub>H</sub>	See Family Spec
ERAY0_ID	Module Identification Register	0008 <sub>H</sub>	See Family Spec
ERAY1_ID	Module Identification Register	0008 <sub>H</sub>	See Family Spec
ERAY0_CUST3	Customer Interface Timeout Counter Register	000C <sub>H</sub>	See Family Spec
ERAY1_CUST3	Customer Interface Timeout Counter Register	000C <sub>H</sub>	See Family Spec
ERAY0_TEST1	Test Register 1	0010 <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_TEST1	Test Register 1	0010 <sub>H</sub>	See Family Spec
ERAY0_TEST2	Test Register 2	0014 <sub>H</sub>	See Family Spec
ERAY1_TEST2	Test Register 2	0014 <sub>H</sub>	See Family Spec
ERAY0_LCK	Lock Register	001C <sub>H</sub>	See Family Spec
ERAY1_LCK	Lock Register	001C <sub>H</sub>	See Family Spec
ERAY0_EIR	Error Service Request Select Register	0020 <sub>H</sub>	See Family Spec
ERAY1_EIR	Error Service Request Select Register	0020 <sub>H</sub>	See Family Spec
ERAY0_SIR	Status Service Request Register	0024 <sub>H</sub>	See Family Spec
ERAY1_SIR	Status Service Request Register	0024 <sub>H</sub>	See Family Spec
ERAY0_EILS	Error Service Request Line Select	0028 <sub>H</sub>	See Family Spec
ERAY1_EILS	Error Service Request Line Select	0028 <sub>H</sub>	See Family Spec
ERAY0_SILS	Status Service Request Line Select	002C <sub>H</sub>	See Family Spec
ERAY1_SILS	Status Service Request Line Select	002C <sub>H</sub>	See Family Spec
ERAY0_EIES	Error Service Request Enable Set	0030 <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_EIES	Error Service Request Enable Set	0030 <sub>H</sub>	See Family Spec
ERAY0_EIER	Error Service Request Enable Reset	0034 <sub>H</sub>	See Family Spec
ERAY1_EIER	Error Service Request Enable Reset	0034 <sub>H</sub>	See Family Spec
ERAY0_SIES	Status Service Request Enable Set	0038 <sub>H</sub>	See Family Spec
ERAY1_SIES	Status Service Request Enable Set	0038 <sub>H</sub>	See Family Spec
ERAY0_SIER	Status Service Request Enable Reset	003C <sub>H</sub>	See Family Spec
ERAY1_SIER	Status Service Request Enable Reset	003C <sub>H</sub>	See Family Spec
ERAY0_ILE	Service Request Line Enable	0040 <sub>H</sub>	See Family Spec
ERAY1_ILE	Service Request Line Enable	0040 <sub>H</sub>	See Family Spec
ERAY0_T0C	Timer 0 Configuration	0044 <sub>H</sub>	See Family Spec
ERAY1_T0C	Timer 0 Configuration	0044 <sub>H</sub>	See Family Spec
ERAY0_T1C	Timer 1 Configuration	0048 <sub>H</sub>	See Family Spec
ERAY1_T1C	Timer 1 Configuration	0048 <sub>H</sub>	See Family Spec
ERAY0_STPW1	Stop Watch Register 1	004C <sub>H</sub>	See Family Spec

**FlexRay™ Protocol Controller (E-Ray)****Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_STPW1	Stop Watch Register 1	004C <sub>H</sub>	See Family Spec
ERAY0_STPW2	Stop Watch Register 2	0050 <sub>H</sub>	See Family Spec
ERAY1_STPW2	Stop Watch Register 2	0050 <sub>H</sub>	See Family Spec
ERAY0_SUCC1	SUC Configuration Register 1	0080 <sub>H</sub>	See Family Spec
ERAY1_SUCC1	SUC Configuration Register 1	0080 <sub>H</sub>	See Family Spec
ERAY0_SUCC2	SUC Configuration Register 2	0084 <sub>H</sub>	See Family Spec
ERAY1_SUCC2	SUC Configuration Register 2	0084 <sub>H</sub>	See Family Spec
ERAY0_SUCC3	SUC Configuration Register 3	0088 <sub>H</sub>	See Family Spec
ERAY1_SUCC3	SUC Configuration Register 3	0088 <sub>H</sub>	See Family Spec
ERAY0_NEMC	NEM Configuration Register	008C <sub>H</sub>	See Family Spec
ERAY1_NEMC	NEM Configuration Register	008C <sub>H</sub>	See Family Spec
ERAY0_PRTC1	PRT Configuration Register 1	0090 <sub>H</sub>	See Family Spec
ERAY1_PRTC1	PRT Configuration Register 1	0090 <sub>H</sub>	See Family Spec
ERAY0_PRTC2	PRT Configuration Register 2	0094 <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_PRTC2	PRT Configuration Register 2	0094 <sub>H</sub>	See Family Spec
ERAY0_MHDC	MHD Configuration Register	0098 <sub>H</sub>	See Family Spec
ERAY1_MHDC	MHD Configuration Register	0098 <sub>H</sub>	See Family Spec
ERAY0_GTUC01	GTU Configuration Register 1	00A0 <sub>H</sub>	See Family Spec
ERAY1_GTUC01	GTU Configuration Register 1	00A0 <sub>H</sub>	See Family Spec
ERAY0_GTUC02	GTU Configuration Register 2	00A4 <sub>H</sub>	See Family Spec
ERAY1_GTUC02	GTU Configuration Register 2	00A4 <sub>H</sub>	See Family Spec
ERAY0_GTUC03	GTU Configuration Register 3	00A8 <sub>H</sub>	See Family Spec
ERAY1_GTUC03	GTU Configuration Register 3	00A8 <sub>H</sub>	See Family Spec
ERAY0_GTUC04	GTU Configuration Register 4	00AC <sub>H</sub>	See Family Spec
ERAY1_GTUC04	GTU Configuration Register 4	00AC <sub>H</sub>	See Family Spec
ERAY0_GTUC05	GTU Configuration Register 5	00B0 <sub>H</sub>	See Family Spec
ERAY1_GTUC05	GTU Configuration Register 5	00B0 <sub>H</sub>	See Family Spec
ERAY0_GTUC06	GTU Configuration Register 6	00B4 <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_GTUC06	GTU Configuration Register 6	00B4 <sub>H</sub>	See Family Spec
ERAY0_GTUC07	GTU Configuration Register 7	00B8 <sub>H</sub>	See Family Spec
ERAY1_GTUC07	GTU Configuration Register 7	00B8 <sub>H</sub>	See Family Spec
ERAY0_GTUC08	GTU Configuration Register 8	00BC <sub>H</sub>	See Family Spec
ERAY1_GTUC08	GTU Configuration Register 8	00BC <sub>H</sub>	See Family Spec
ERAY0_GTUC09	GTU Configuration Register 9	00C0 <sub>H</sub>	See Family Spec
ERAY1_GTUC09	GTU Configuration Register 9	00C0 <sub>H</sub>	See Family Spec
ERAY0_GTUC10	GTU Configuration Register 10	00C4 <sub>H</sub>	See Family Spec
ERAY1_GTUC10	GTU Configuration Register 10	00C4 <sub>H</sub>	See Family Spec
ERAY0_GTUC11	GTU Configuration Register 11	00C8 <sub>H</sub>	See Family Spec
ERAY1_GTUC11	GTU Configuration Register 11	00C8 <sub>H</sub>	See Family Spec
ERAY0_CCSV	Communication Controller Status Vector	0100 <sub>H</sub>	See Family Spec
ERAY1_CCSV	Communication Controller Status Vector	0100 <sub>H</sub>	See Family Spec
ERAY0_CCEV	Communication Controller Error Vector	0104 <sub>H</sub>	See Family Spec

**FlexRay™ Protocol Controller (E-Ray)****Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_CCEV	Communication Controller Error Vector	0104 <sub>H</sub>	See Family Spec
ERAY0_SCV	Slot Counter Value	0110 <sub>H</sub>	See Family Spec
ERAY1_SCV	Slot Counter Value	0110 <sub>H</sub>	See Family Spec
ERAY0_MTCCV	Macrotick and Cycle Counter Value	0114 <sub>H</sub>	See Family Spec
ERAY1_MTCCV	Macrotick and Cycle Counter Value	0114 <sub>H</sub>	See Family Spec
ERAY0_RCV	Rate Correction Value	0118 <sub>H</sub>	See Family Spec
ERAY1_RCV	Rate Correction Value	0118 <sub>H</sub>	See Family Spec
ERAY0_OCV	Offset Correction Value	011C <sub>H</sub>	See Family Spec
ERAY1_OCV	Offset Correction Value	011C <sub>H</sub>	See Family Spec
ERAY0_SFS	SYNC Frame Status	0120 <sub>H</sub>	See Family Spec
ERAY1_SFS	SYNC Frame Status	0120 <sub>H</sub>	See Family Spec
ERAY0_SWNIT	Symbol Window and Network Idle Time Status	0124 <sub>H</sub>	See Family Spec
ERAY1_SWNIT	Symbol Window and Network Idle Time Status	0124 <sub>H</sub>	See Family Spec
ERAY0_ACS	Aggregated Channel Status	0128 <sub>H</sub>	See Family Spec

**FlexRay™ Protocol Controller (E-Ray)****Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_ACS	Aggregated Channel Status	0128 <sub>H</sub>	See Family Spec
ERAY0_ESIDn (n=01-15)	Even Sync ID Symbol Window n	0130 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY1_ESIDn (n=01-15)	Even Sync ID Symbol Window n	0130 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY0_OSIDn (n=01-15)	Odd Sync ID Symbol Window n	0170 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY1_OSIDn (n=01-15)	Odd Sync ID Symbol Window n	0170 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY0_NM Vx (x=1-3)	Network Management Vector x	01B0 <sub>H</sub> +(x-1)*4	See Family Spec
ERAY1_NM Vx (x=1-3)	Network Management Vector x	01B0 <sub>H</sub> +(x-1)*4	See Family Spec
ERAY0_MRC	Message RAM Configuration	0300 <sub>H</sub>	See Family Spec
ERAY1_MRC	Message RAM Configuration	0300 <sub>H</sub>	See Family Spec
ERAY0_FRF	FIFO Rejection Filter	0304 <sub>H</sub>	See Family Spec
ERAY1_FRF	FIFO Rejection Filter	0304 <sub>H</sub>	See Family Spec
ERAY0_FRFM	FIFO Rejection Filter Mask	0308 <sub>H</sub>	See Family Spec
ERAY1_FRFM	FIFO Rejection Filter Mask	0308 <sub>H</sub>	See Family Spec
ERAY0_FCL	FIFO Critical Level	030C <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_FCL	FIFO Critical Level	030C <sub>H</sub>	See Family Spec
ERAY0_MHDS	Message Handler Status	0310 <sub>H</sub>	See Family Spec
ERAY1_MHDS	Message Handler Status	0310 <sub>H</sub>	See Family Spec
ERAY0_LDTS	Last Dynamic Transmit Slot	0314 <sub>H</sub>	See Family Spec
ERAY1_LDTS	Last Dynamic Transmit Slot	0314 <sub>H</sub>	See Family Spec
ERAY0_FSR	FIFO Status Register	0318 <sub>H</sub>	See Family Spec
ERAY1_FSR	FIFO Status Register	0318 <sub>H</sub>	See Family Spec
ERAY0_MHDF	Message Handler Constraints Flags	031C <sub>H</sub>	See Family Spec
ERAY1_MHDF	Message Handler Constraints Flags	031C <sub>H</sub>	See Family Spec
ERAY0_TXRQ1	Transmission Request Register 1	0320 <sub>H</sub>	See Family Spec
ERAY1_TXRQ1	Transmission Request Register 1	0320 <sub>H</sub>	See Family Spec
ERAY0_TXRQ2	Transmission Request Register 2	0324 <sub>H</sub>	See Family Spec
ERAY1_TXRQ2	Transmission Request Register 2	0324 <sub>H</sub>	See Family Spec
ERAY0_TXRQ3	Transmission Request Register 3	0328 <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_TXRQ3	Transmission Request Register 3	0328 <sub>H</sub>	See Family Spec
ERAY0_TXRQ4	Transmission Request Register 4	032C <sub>H</sub>	See Family Spec
ERAY1_TXRQ4	Transmission Request Register 4	032C <sub>H</sub>	See Family Spec
ERAY0_NDAT1	New Data Register 1	0330 <sub>H</sub>	See Family Spec
ERAY1_NDAT1	New Data Register 1	0330 <sub>H</sub>	See Family Spec
ERAY0_NDAT2	New Data Register 2	0334 <sub>H</sub>	See Family Spec
ERAY1_NDAT2	New Data Register 2	0334 <sub>H</sub>	See Family Spec
ERAY0_NDAT3	New Data Register 3	0338 <sub>H</sub>	See Family Spec
ERAY1_NDAT3	New Data Register 3	0338 <sub>H</sub>	See Family Spec
ERAY0_NDAT4	New Data Register 4	033C <sub>H</sub>	See Family Spec
ERAY1_NDAT4	New Data Register 4	033C <sub>H</sub>	See Family Spec
ERAY0_MBSC1	Message Buffer Status Changed 1	0340 <sub>H</sub>	See Family Spec
ERAY1_MBSC1	Message Buffer Status Changed 1	0340 <sub>H</sub>	See Family Spec
ERAY0_MBSC2	Message Buffer Status Changed 2	0344 <sub>H</sub>	See Family Spec

**FlexRay™ Protocol Controller (E-Ray)****Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_MBSC2	Message Buffer Status Changed 2	0344 <sub>H</sub>	See Family Spec
ERAY0_MBSC3	Message Buffer Status Changed 3	0348 <sub>H</sub>	See Family Spec
ERAY1_MBSC3	Message Buffer Status Changed 3	0348 <sub>H</sub>	See Family Spec
ERAY0_MBSC4	Message Buffer Status Changed 4	034C <sub>H</sub>	See Family Spec
ERAY1_MBSC4	Message Buffer Status Changed 4	034C <sub>H</sub>	See Family Spec
ERAY0_NDIC1	New Data Interrupt Control 1	03A8 <sub>H</sub>	See Family Spec
ERAY1_NDIC1	New Data Interrupt Control 1	03A8 <sub>H</sub>	See Family Spec
ERAY0_NDIC2	New Data Interrupt Control 2	03AC <sub>H</sub>	See Family Spec
ERAY1_NDIC2	New Data Interrupt Control 2	03AC <sub>H</sub>	See Family Spec
ERAY0_NDIC3	New Data Interrupt Control 3	03B0 <sub>H</sub>	See Family Spec
ERAY1_NDIC3	New Data Interrupt Control 3	03B0 <sub>H</sub>	See Family Spec
ERAY0_NDIC4	New Data Interrupt Control 4	03B4 <sub>H</sub>	See Family Spec
ERAY1_NDIC4	New Data Interrupt Control 4	03B4 <sub>H</sub>	See Family Spec
ERAY0_MSIC1	Message Buffer Status Changed Interrupt Control 1	03B8 <sub>H</sub>	See Family Spec

**FlexRay™ Protocol Controller (E-Ray)****Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_MSIC1	Message Buffer Status Changed Interrupt Control 1	03B8 <sub>H</sub>	See Family Spec
ERAY0_MSIC2	Message Buffer Status Changed Interrupt Control 2	03BC <sub>H</sub>	See Family Spec
ERAY1_MSIC2	Message Buffer Status Changed Interrupt Control 2	03BC <sub>H</sub>	See Family Spec
ERAY0_MSIC3	Message Buffer Status Changed Interrupt Control 3	03C0 <sub>H</sub>	See Family Spec
ERAY1_MSIC3	Message Buffer Status Changed Interrupt Control 3	03C0 <sub>H</sub>	See Family Spec
ERAY0_MSIC4	Message Buffer Status Changed Interrupt Control 4	03C4 <sub>H</sub>	See Family Spec
ERAY1_MSIC4	Message Buffer Status Changed Interrupt Control 4	03C4 <sub>H</sub>	See Family Spec
ERAY0_CREL	Core Release Register	03F0 <sub>H</sub>	See Family Spec
ERAY1_CREL	Core Release Register	03F0 <sub>H</sub>	See Family Spec
ERAY0_ENDIAN	Endian Register	03F4 <sub>H</sub>	See Family Spec
ERAY1_ENDIAN	Endian Register	03F4 <sub>H</sub>	See Family Spec
ERAY0_WRDSn (n=01-64)	Write Data Section n	0400 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY1_WRDSn (n=01-64)	Write Data Section n	0400 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY0_WRHS1	Write Header Section 1	0500 <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_WRHS1	Write Header Section 1	0500 <sub>H</sub>	See Family Spec
ERAY0_WRHS2	Write Header Section 2	0504 <sub>H</sub>	See Family Spec
ERAY1_WRHS2	Write Header Section 2	0504 <sub>H</sub>	See Family Spec
ERAY0_WRHS3	Write Header Section 3	0508 <sub>H</sub>	See Family Spec
ERAY1_WRHS3	Write Header Section 3	0508 <sub>H</sub>	See Family Spec
ERAY0_IBCM	Input Buffer Command Mask	0510 <sub>H</sub>	See Family Spec
ERAY1_IBCM	Input Buffer Command Mask	0510 <sub>H</sub>	See Family Spec
ERAY0_IBCR	Input Buffer Command Request	0514 <sub>H</sub>	See Family Spec
ERAY1_IBCR	Input Buffer Command Request	0514 <sub>H</sub>	See Family Spec
ERAY0_RDDSn (n=01-64)	Read Data Section n	0600 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY1_RDDSn (n=01-64)	Read Data Section n	0600 <sub>H</sub> +(n-1)*4	See Family Spec
ERAY0_RDHS1	Read Header Section 1	0700 <sub>H</sub>	See Family Spec
ERAY1_RDHS1	Read Header Section 1	0700 <sub>H</sub>	See Family Spec
ERAY0_RDHS2	Read Header Section 2	0704 <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
ERAY1_RDHS2	Read Header Section 2	0704 <sub>H</sub>	See Family Spec
ERAY0_RDHS3	Read Header Section 3	0708 <sub>H</sub>	See Family Spec
ERAY1_RDHS3	Read Header Section 3	0708 <sub>H</sub>	See Family Spec
ERAY0_MBS	Message Buffer Status	070C <sub>H</sub>	See Family Spec
ERAY1_MBS	Message Buffer Status	070C <sub>H</sub>	See Family Spec
ERAY0_OBCM	Output Buffer Command Mask	0710 <sub>H</sub>	See Family Spec
ERAY1_OBCM	Output Buffer Command Mask	0710 <sub>H</sub>	See Family Spec
ERAY0_OBCR	Output Buffer Command Request	0714 <sub>H</sub>	See Family Spec
ERAY1_OBCR	Output Buffer Command Request	0714 <sub>H</sub>	See Family Spec
ERAY0_OTSS	OCDS Trigger Set Select	0870 <sub>H</sub>	See Family Spec
ERAY1_OTSS	OCDS Trigger Set Select	0870 <sub>H</sub>	See Family Spec
ERAY0_OCS	OCDS Control and Status	08E8 <sub>H</sub>	See Family Spec
ERAY1_OCS	OCDS Control and Status	08E8 <sub>H</sub>	See Family Spec
ERAY0_KRSTCLR	Kernel Reset Status Clear Register	08EC <sub>H</sub>	See Family Spec

## FlexRay™ Protocol Controller (E-Ray)

**Table 445 Register Overview - ERAY (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
ERAY1_KRSTCLR	Kernel Reset Status Clear Register	08EC <sub>H</sub>	See Family Spec
ERAY0_KRST1	Kernel Reset Register 1	08F0 <sub>H</sub>	See Family Spec
ERAY1_KRST1	Kernel Reset Register 1	08F0 <sub>H</sub>	See Family Spec
ERAY0_KRST0	Kernel Reset Register 0	08F4 <sub>H</sub>	See Family Spec
ERAY1_KRST0	Kernel Reset Register 0	08F4 <sub>H</sub>	See Family Spec
ERAY0_ACCENO	Access Enable Register 0	08FC <sub>H</sub>	See Family Spec
ERAY1_ACCENO	Access Enable Register 0	08FC <sub>H</sub>	See Family Spec

### 39.3 TC39x-B Specific Registers

No deviations from the Family Spec

### 39.4 Connectivity

**Table 446 Connections of ERAY0**

Interface Signals	connects	Description	
ERAY0:MT	to	CCU:eray_mt	Macrotick-clock from CC (synchronous to fpi clock)
		GTM:TIM0_IN7(13)	
		GTM:TIM1_IN7(13)	
		GTM:TIM2_IN7(13)	
		GTM:TIM3_IN7(13)	
		SCU:E_REQ2(3)	
ERAY0:RXDA0	from	P14.8:IN	Receive Channel A0
ERAY0:RXDA1	from	P11.9:IN	Receive Channel A1
ERAY0:RXDA2	from	P02.1:IN	Receive Channel A2
ERAY0:RXDA3	from	P14.1:IN	Receive Channel A3
ERAY0:RXDB0	from	P14.7:IN	Receive Channel B0

**FlexRay™ Protocol Controller (E-Ray)****Table 446 Connections of ERAY0 (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
ERAY0:RXDB1	from	P11.10:IN	Receive Channel B1
ERAY0:RXDB2	from	P02.3:IN	Receive Channel B2
ERAY0:RXDB3	from	P14.1:IN	Receive Channel B3
ERAY0:STPWT(3:0)	from	SCU:E_PDOUT(3:0)	StoP Watch Trigger signal
ERAY0:TINT0	to	CAN0:ECTT(5)	Timer Interrupt 0 (high-active)
ERAY0:TINT1	to	CAN0:ECTT(6)	Timer Interrupt 1 (high-active)
ERAY0:TXDA	to	P02.0:ALT(6) P11.3:ALT(4) P14.0:ALT(3) P14.10:ALT(6)	Transmit Channel A
ERAY0:TXDB	to	P02.2:ALT(6) P11.12:ALT(4) P14.0:ALT(4) P14.5:ALT(6)	Transmit Channel B
ERAY0:TXENA	to	P02.4:ALT(6) P11.6:ALT(4) P14.9:ALT(6)	Transmit Enable Channel A
ERAY0:TXENB	to	P02.5:ALT(6) P11.6:ALT(2) P11.11:ALT(6) P14.6:ALT(6) P14.9:ALT(5)	Transmit Enable Channel B
ERAY0:sleep_n	from	SCU:scu_syst_sleep_n	turn-off request from processor
ERAY0:INT0_INT	to	INT:eray0.INT0_INT	E-RAY Service Request 0
ERAY0:INT1_INT	to	INT:eray0.INT1_INT	E-RAY Service Request 1
ERAY0:TINT0_INT	to	INT:eray0.TINT0_INT	E-RAY Timer Interrupt 0 Service Request
ERAY0:TINT1_INT	to	INT:eray0.TINT1_INT	E-RAY Timer Interrupt 1 Service Request
ERAY0:NDATE0_INT	to	INT:eray0.NDATE0_INT	E-RAY New Data 0 Service Request
ERAY0:NDATE1_INT	to	INT:eray0.NDATE1_INT	E-RAY New Data 1 Service Request
ERAY0:MBSC0_INT	to	INT:eray0.MBSC0_INT	E-RAY Message Buffer Status Changed 0 Service Request
ERAY0:MBSC1_INT	to	INT:eray0.MBSC1_INT	E-RAY Message Buffer Status Changed 1 Service Request
ERAY0:OBUSY	to	INT:eray0.OBUSY	E-RAY Output Buffer Busy Service Request
ERAY0:IBUSY_INT	to	INT:eray0.IBUSY_INT	E-RAY Input Buffer Busy Service Request

## FlexRay™ Protocol Controller (E-Ray)

**Table 447 Connections of ERAY1**

Interface Signals	connects		Description
ERAY1:MT	to	GTM:TIM4_IN7(13)	Macrotick-clock from CC (synchronous to fpi clock)
		GTM:TIM5_IN7(13)	
		SCU:E_REQ7(3)	
ERAY1:RXDA0	from	P14.8:IN	Receive Channel A0
ERAY1:RXDA1	from	P01.1:IN	Receive Channel A1
ERAY1:RXDB0	from	P14.7:IN	Receive Channel B0
ERAY1:RXDB1	from	P01.8:IN	Receive Channel B1
ERAY1:STPWT(3:0)	from	SCU:E_PDOOUT(3:0)	StoP Watch Trigger signal
ERAY1:TXDA	to	P01.12:ALT(6)	Transmit Channel A
		P14.10:ALT(7)	
ERAY1:TXDB	to	P01.13:ALT(6)	Transmit Channel B
		P14.5:ALT(7)	
ERAY1:TXENA	to	P01.14:ALT(6)	Transmit Enable Channel A
		P14.9:ALT(7)	
ERAY1:TXENB	to	P02.15:ALT(6)	Transmit Enable Channel B
		P14.6:ALT(7)	
ERAY1:sleep_n	from	SCU:scu_syst_sleep_n	turn-off request from processor
ERAY1:INT0_INT	to	INT:eray1.INT0_INT	E-RAY Service Request 0
ERAY1:INT1_INT	to	INT:eray1.INT1_INT	E-RAY Service Request 1
ERAY1:TINT0_INT	to	INT:eray1.TINT0_INT	E-RAY Timer Interrupt 0 Service Request
ERAY1:TINT1_INT	to	INT:eray1.TINT1_INT	E-RAY Timer Interrupt 1 Service Request
ERAY1:NDAT0_INT	to	INT:eray1.NDAT0_INT	E-RAY New Data 0 Service Request
ERAY1:NDAT1_INT	to	INT:eray1.NDAT1_INT	E-RAY New Data 1 Service Request
ERAY1:MBSC0_INT	to	INT:eray1.MBSC0_INT	E-RAY Message Buffer Status Changed 0 Service Request
ERAY1:MBSC1_INT	to	INT:eray1.MBSC1_INT	E-RAY Message Buffer Status Changed 1 Service Request
ERAY1:OBUSY	to	INT:eray1.OBUSY	E-RAY Output Buffer Busy Service Request
ERAY1:IBUSY_INT	to	INT:eray1.IBUSY_INT	E-RAY Input Buffer Busy Service Request

## 39.5 Revision History

**Table 448 Revision History**

Reference	Change to Previous Version	Comment
V3.2.9		
Page 2	Headline completed by “Specific Register Set”. No functional changes in the connectivity tables.	
V3.2.10		

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**FlexRay™ Protocol Controller (E-Ray)****Table 448 Revision History (cont'd)**

Reference	Change to Previous Version	Comment
-	No functional change.	
<b>V3.2.11</b>		
-	No functional change.	

## Peripheral Sensor Interface (PSI5)

### 40 Peripheral Sensor Interface (PSI5)

This chapter describes the Peripheral Sensor Interface (short PSI5) Module of the TC39x-B.

#### 40.1 TC39x-B Specific IP Configuration

See features in family spec.

**Table 449 TC39x-B specific configuration of PSI5**

Parameter	PSI5
Number of PSI5 channels for this device	4

#### 40.2 TC39x-B Specific Register Set

##### Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

**Table 450 Register Address Space - PSI5**

Module	Base Address	End Address	Note
PSI5	F0005000 <sub>H</sub>	F0005AFF <sub>H</sub>	FPI slave interface

##### Register Overview Tables of PSI5

**Table 451 Register Overview - PSI5 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_CLC	Clock Control Register	000 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
	Reserved (004 <sub>H</sub> Byte)	004 <sub>H</sub>	BE	BE		
PSI5_ID	Module Identification Register	008 <sub>H</sub>	SV,U	BE	Application Reset	See Family Spec
PSI5_FDR	PSI5 Fractional Divider Register	00C <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_FDRL	Fractional Divider Register for Lower Bit Rate	010 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_FDRH	Fractional Divider Register for Higher Bit Rate	014 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec

## Peripheral Sensor Interface (PSI5)

Table 451 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_FDRT	Fractional Divider Register for Time Stamp	018 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_TSRA	Module Time Stamp Register A	01C <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_TSRB	Time Stamp Register B	020 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_TSRC	Module Time Stamp Register C	024 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
	Reserved (004 <sub>H</sub> Byte)	028 <sub>H</sub>	BE	BE		
PSI5_GCR	Global Control Register	02C <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_IOC Rx (x=0-3)	Input and Output Control Register x	030 <sub>H</sub> +x*90 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RCRAx (x=0-3)	Receiver Control Register A x	034 <sub>H</sub> +x*90 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RCRBx (x=0-3)	Receiver Control Register B x	038 <sub>H</sub> +x*90 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RCRCx (x=0-3)	Receiver Control Register C x	03C <sub>H</sub> +x*90 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_WDTxw (w=0-6;x=0-3)	Watch Dog Timer Register xw	040 <sub>H</sub> +x*90 <sub>H</sub> +w*4	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RSRx (x=0-3)	Receive Status Register x	05C <sub>H</sub> +x*90 <sub>H</sub>	SV,U	BE	Application Reset	See Family Spec
PSI5_SDSxz (x=0-3;z=0-5)	Serial Data and Status Register xz	060 <sub>H</sub> +x*90 <sub>H</sub> +z*4	SV,U	BE	Application Reset	See Family Spec
PSI5_SPTSCx (x=0-3)	Start of Pulse Time Stamp Capture Register x	078 <sub>H</sub> +x*90 <sub>H</sub>	SV,U	BE	Application Reset	See Family Spec

## Peripheral Sensor Interface (PSI5)

Table 451 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_SFTSCx (x=0-3)	Start of Frame Time Stamp Capture Register x	07C <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	BE	Application Reset	See Family Spec
PSI5_RDRLx (x=0-3)	Receive Data Register Low x	080 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	BE	Application Reset	See Family Spec
PSI5_RDRHx (x=0-3)	Receive Data Register High x	084 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	BE	Application Reset	See Family Spec
PSI5_PGCx (x=0-3)	Pulse Generation Control Register x	088 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_CTVx (x=0-3)	Channel Trigger Value Register x	08C <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_SCRx (x=0-3)	Send Control Register x	090 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_SDRLx (x=0-3)	Send Data Register Low x	094 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SDRHx (x=0-3)	Send Data Register High x	098 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SSRLx (x=0-3)	Send Shift Register Low x	09C <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SSRHx (x=0-3)	Send Shift Register High x	0A0 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SORLx (x=0-3)	Send Output Register Low x	0A4 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SORHx (x=0-3)	Send Output Register High x	0A8 <sub>H</sub> +x* 90 <sub>H</sub>	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_INTOV	Interrupt Overview Register	2F8 <sub>H</sub>	SV,U	BE	Application Reset	See Family Spec
PSI5_INPx (x=0-3)	Interrupt Node Pointer Register x	2FC <sub>H</sub> +x* 4	SV,U	SV,E,P	Application Reset	See Family Spec

## Peripheral Sensor Interface (PSI5)

Table 451 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_INTSTATAx (x=0-3)	Interrupt Status Register A x	310 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_INTSTATBx (x=0-3)	Interrupt Status Register B x	324 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_INTSETAx (x=0-3)	Interrupt Set Register A x	338 <sub>H</sub> +x* 4	nBE	SV,E,P	Application Reset	See Family Spec
PSI5_INTSETBx (x=0-3)	Interrupt Set Register B x	34C <sub>H</sub> +x* 4	nBE	SV,E,P	Application Reset	See Family Spec
PSI5_INTCLRAx (x=0-3)	Interrupt Clear Register A x	360 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_INTCLRBx (x=0-3)	Interrupt Clear Register A x	374 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_INENAx (x=0-3)	Interrupt Enable Register A x	388 <sub>H</sub> +x* 4	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_INENBx (x=0-3)	Interrupt Enable Register B x	39C <sub>H</sub> +x* 4	SV,U	SV,E,P	Application Reset	See Family Spec
	Reserved (01C <sub>H</sub> Byte)	3B0 <sub>H</sub>	BE	BE		
PSI5_OCS	OCDS Control and Status	3CC <sub>H</sub>	U,SV	SV,P	Debug Reset	See Family Spec
PSI5_ACCEN0	Access Enable Register 0	3D0 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
PSI5_ACCEN1	Access Enable Register 1	3D4 <sub>H</sub>	U,SV	SV,SE	Application Reset	See Family Spec
PSI5_KRST0	Kernel Reset Register 0	3D8 <sub>H</sub>	U,SV	SV,P,E	Application Reset	See Family Spec
PSI5_KRST1	Kernel Reset Register 1	3DC <sub>H</sub>	U,SV	SV,P,E	Application Reset	See Family Spec

## Peripheral Sensor Interface (PSI5)

Table 451 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_KRSTCLR	Kernel Reset Status Clear Register	3E0 <sub>H</sub>	U,SV	SV,P,E	Application Reset	See Family Spec
PSI5_RFCx (x=0-3)	Receive FIFO Control Register x	3E4 <sub>H</sub> +x* 4	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_RDFx (x=0-3)	Receive Data FIFO x	3F8 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RSIOVx (x=0-3)	RSI Overview Register x	40C <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RMIOVx (x=0-3)	RMI Overview Register x	420 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_NBIOVx (x=0-3)	NBI Overview Register x	434 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_TEIOVx (x=0-3)	TEI Overview Register x	448 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_CRCIOVx (x=0-3)	CRCI Overview Register x	45C <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RDIOVx (x=0-3)	RDI Overview Register x	470 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_NFIOVx (x=0-3)	NFI Overview Register x	484 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_MEIOVx (x=0-3)	MEI Overview Register x	498 <sub>H</sub> +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RSISETx (x=0-3)	RSI Overview Set Register x	4AC <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RMISETx (x=0-3)	RMI Overview Set Register x	4C0 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NBISETx (x=0-3)	NBI Overview Set Register x	4D4 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec

## Peripheral Sensor Interface (PSI5)

Table 451 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_TEISETx (x=0-3)	TEI Overview Set Register x	4E8 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_CRCISETx (x=0-3)	CRCI Overview Set Register x	4FC <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RDISETx (x=0-3)	RDI Overview Set Register x	510 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NFISETx (x=0-3)	NFI Overview Set Register x	524 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_MEISETx (x=0-3)	MEI Overview Set Register x	538 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RSICL Rx (x=0-3)	RSI Overview Clear Register x	54C <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RMICL Rx (x=0-3)	RMI Overview Clear Register x	560 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NBICL Rx (x=0-3)	NBI Overview Clear Register x	574 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_TEICL Rx (x=0-3)	TEI Overview Clear Register x	588 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_CRCICL Rx (x=0-3)	CRCI Overview Clear Register x	59C <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RDICL Rx (x=0-3)	RDI Overview Clear Register x	5B0 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NFICL Rx (x=0-3)	NFI Overview Clear Register x	5C4 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_MEICL Rx (x=0-3)	MEI Overview Clear Register x	5D8 <sub>H</sub> +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
	Reserved (014 <sub>H</sub> Byte)	5EC <sub>H</sub>	BE	BE		

## Peripheral Sensor Interface (PSI5)

**Table 451 Register Overview - PSI5 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_RDMLxy (x=0-3;y=0-31)	Receive Data Memory Low xy	$600_{\text{H}}+x^*$ $100_{\text{H}}+y^*$ 8	SV,U	BE	Application Reset	See Family Spec
PSI5_RDMHxy (x=0-3;y=0-31)	Receive Data Memory High xy	$604_{\text{H}}+x^*$ $100_{\text{H}}+y^*$ 8	SV,U	BE	Application Reset	See Family Spec
	Reserved (100 <sub>H</sub> Byte)	A00 <sub>H</sub>	BE	BE		

### 40.3 TC39x-B Specific Registers

There are no product specific registers for this module.

### 40.4 Connectivity

The tables below list all the connections of PSI5 instances.

**Table 452 Connections of PSI5**

Interface Signals	connects		Description
PSI5:RX0A	from	P00.1:IN	RXD inputs (receive data) channel 0
PSI5:RX1A	from	P00.3:IN	RXD inputs (receive data) channel 1
PSI5:RX2A	from	P00.5:IN	RXD inputs (receive data) channel 2
PSI5:RX3A	from	P13.10:IN	RXD inputs (receive data) channel 3
PSI5:RX0B	from	P02.3:IN	RXD inputs (receive data) channel 0
PSI5:RX1B	from	P02.5:IN	RXD inputs (receive data) channel 1
PSI5:RX2B	from	P02.7:IN	RXD inputs (receive data) channel 2
PSI5:RX3B	from	P13.13:IN	RXD inputs (receive data) channel 3
PSI5:RX0C	from	P33.1:IN	RXD inputs (receive data) channel 0
PSI5:RX1C	from	P33.3:IN	RXD inputs (receive data) channel 1
PSI5:RX2C	from	P33.5:IN	RXD inputs (receive data) channel 2
PSI5:RX3C	from	P10.6:IN	RXD inputs (receive data) channel 3
PSI5:TX(0)	to	IOM:REF1(14) P00.2:ALT(4) P02.2:ALT(4) P33.2:ALT(4)	TXD outputs (send data)
PSI5:TX(1:0)	to	IOM:MON1(15:14)	TXD outputs (send data)
PSI5:TX(1)	to	P00.4:ALT(4) P02.6:ALT(4) P33.4:ALT(4)	TXD outputs (send data)

## Peripheral Sensor Interface (PSI5)

**Table 452 Connections of PSI5 (cont'd)**

Interface Signals	connects		Description
PSI5:TX(2)	to	IOM:REF1(15)	TXD outputs (send data)
		P00.6:ALT(4)	
		P02.8:ALT(4)	
		P33.6:ALT(4)	
PSI5:TX(3)	to	P10.5:ALT(7)	TXD outputs (send data)
		P13.11:ALT(4)	
		P13.15:ALT(4)	
PSI5:TRIG(5:0)	from	GTM:PSI5.TRIG(5:0)	GTM timer output vector - synchronized
PSI5:TRIGO(7:0)	to	INT:psi5.TRIGO(7:0)	PSI5 Service Request

## 40.5 Revision History

**Table 453 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.17.11</b>		
	Register Overview table added.	
<b>Page 7</b>	No functional changes. Formal changes in Connectivity tables.	
	Revision History entries up to V1.17.10 removed.	
<b>V1.17.12</b>		
<b>Page 1</b>	Second sentence changed to internal audience only due to customer confusion. No functional change.	

## Peripheral Sensor Interface with Serial PHY Connection (PSI5-S)

### 41 Peripheral Sensor Interface with Serial PHY Connection (PSI5-S)

This chapter describes the Peripheral Sensor Interface with Serial PHY Connection (short PSI5-S) Module of the TC39x-B.

#### 41.1 TC39x-B Specific IP Configuration

See features in family spec.

**Table 454 TC39x-B specific configuration of PSI5S**

Parameter	PSI5S
Number of channels for this device	8

#### 41.2 TC39x-B Specific Register Set

##### Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

**Table 455 Register Address Space - PSI5S**

Module	Base Address	End Address	Note
PSI5S	F0007000 <sub>H</sub>	F0007FFF <sub>H</sub>	FPI slave interface

##### Register Overview Table

There are no product specific register for this module.

#### 41.3 TC39x-B Specific Registers

There are no product specific register for this module.

#### 41.4 Connectivity

The tables below list all the connections of PSI5-S instances.

**Table 456 Connections of PSI5S**

Interface Signals	connects		Description
PSI5S:CLK	to	P02.4:ALT(4)	PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
		P33.10:ALT(5)	
PSI5S:RXA	from	P00.3:IN	RX data input
PSI5S:RXB	from	P02.5:IN	RX data input
PSI5S:RXC	from	P33.5:IN	RX data input
PSI5S:TX	to	P00.4:ALT(2)	TX data output
		P02.6:ALT(2)	
		P33.6:ALT(7)	

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**Peripheral Sensor Interface with Serial PHY Connection (PSI5-S)**
**Table 456 Connections of PSI5S (cont'd)**

Interface Signals	connects		Description
PSI5S:TRIG(7:0)	from	GTM:PSI5S.TRIG(7:0)	GTM timer output vector
PSI5S:TRIGO(7:0)	to	INT:psi5s.TRIGO(7:0)	PSI5-S Service Request

## 41.5 Revision History

**Table 457 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.12.10</b>		
<a href="#">Page 1</a>	Connections table update, no functional change.	
<a href="#">Page 2</a>	Clean up revision history.	

**Gigabit Ethernet MAC (GETH)****42 Gigabit Ethernet MAC (GETH)**

This document describes the GETH Interface specific appendix for the product TC39x-B.

**42.1 TC39x-B Specific IP Configuration**

No product specific configuration for GETH

**42.2 TC39x-B Specific Register Set****Register Address Space Table**

The address space for the module registers is defined in [Register Address Space Table](#).

**Table 458 Register Address Space - GETH**

Module	Base Address	End Address	Note
GETH	F001D000 <sub>H</sub>	F001F0FF <sub>H</sub>	FPI bus interface

**Register Overview Table****Table 459 Register Overview - GETH (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_CON FIGURATION	MAC Configuration Register	0000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_EXT_ CONFIGURATION	MAC Extended Configuration Register	0004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">18</a>
GETH_MAC_PAC KET_FILTER	MAC Packet Filter Register	0008 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_WAT CHDOG_TIMEOUT	MAC Watchdog Timeout Register	000C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLA N_TAG_CTRL	MAC VLAN Tag Control Register	0050 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLA N_TAG_DATA	MAC VLAN Tag Data Register	0054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLA N_TAG_FILTER_i (i=0-7)	MAC VLAN Tag Filter i Register	0054 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLA N_HASH_TABLE	MAC VLAN Hash Table Register	0058 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_MAC_VLA_N_INCL	MAC VLAN Tag Inclusion or Replacement Register	0060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLA_N_INCL_Q_i (i=0-3)	MAC VLAN Tag Inclusion or Replacement Register per Queue	0060 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INNER_VLAN_INCL_i (i=0-3)	MAC Inner VLAN Tag Inclusion or Replacement Register	0064 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_Q0_TX_FLOW_CTRL	MAC Queue 0 TX Flow Control Register	0070 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_FLOW_CTRL	MAC Receive Flow Control Register	0090 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL4	MAC Receive Queue Control 4 register	0094 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL0	MAC Receive Queue Control 0 Register	00A0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL1	MAC Receive Queue Control 1 Register	00A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL2	MAC Receive Queue Control 2 Register	00A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INTERRUPT_STATUS	MAC Interrupt Status Register	00B0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INTERRUPT_ENABLE	MAC Interrupt Enable Register	00B4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_TX_STATUS	MAC Receive Transmit Status Register	00B8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PMT_CONTROL_STATUS	MAC PMT Control and Status Register	00C0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_PACKET_FILTER	MAC Wake-up Packet Filter Register	00C4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_RWK_FILTER_COMMAND_0	MAC Wake-up Filter Command 0 Register	00C4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_OFFSET_0	MAC Wake-up Filter Offset 0 Register	00C4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_CRC_i(i=0-1)	MAC Wake-up Filter CRC i Register	00C4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_BYTE_MASK_i(i=0-3)	MAC Wake-up i Filter Byte Mask register	00C4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_CONTROL_STATUS	MAC LPI Control and Status Register	00D0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_TIMERS_CONTROL	MAC LPI Timers Control Register	00D4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_ENTRY_TIMER	MAC LPI Entry Timer Register	00D8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_1US_TIC_COUNTER	MAC One Microsecond Tic Counter Register	00DC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PHY_INTERFACE_CONTROL_STATUS	MAC PHY Interface Control and Status Register	00F8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VERSION	MAC Version Register	0110 <sub>H</sub>	U,SV	U,SV,P	Application Reset	20
GETH_MAC_DEBUG	MAC Debug Register	0114 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE0	MAC Hardware Feature Register 0	011C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE1	MAC Hardware Feature Register 1	0120 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE2	MAC Hardware Feature Register 2	0124 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_MAC_HW_FEATURE3	MAC Hardware Feature Register 3	0128 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_MDOI_O_ADDRESS	MAC MDIO Address Register	0200 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_MDOI_O_DATA	MAC MDIO Data Register	0204 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_CSR_SW_CTRL	MAC CSR Software Controls Register	0230 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESS0_HIGH	MAC Address 0 High Register	0300 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESS0_LOW	MAC Address 0 Low Register	0304 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESSi_HIGH (i=1-31)	MAC Address i High Register	0308 <sub>H</sub> +(i-1)*8	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESSi_LOW (i=1-31)	MAC Address i Low Register	030C <sub>H</sub> +(i-1)*8	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMCCONTROL	MMC Control Register	0700 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMCRX_INTERRUPT	MMC Receive Interrupts Register	0704 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMCTX_INTERRUPT	MMC Transmit Interrupts Register	0708 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMCRX_INTERRUPT_MASK	MMC Receive Interrupts Mask Register	070C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMCTX_INTERRUPT_MASK	MMC Transmit Interrupts Mask Register	0710 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OCTET_COUNT_GOOD_BAD	Good And Bad Transmitted Octet Count Register	0714 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_TX_PACKET_COUNT_GOOD_BAD	Good And Bad Transmitted Packets Count Register	0718 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_BROADCAST_PACKETS_GOOD	Good Transmitted Broadcast Packets Count Register	071C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTICAST_PACKETS_GOOD	Good Transmitted Multicast Packets Count Register	0720 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_64OCTS_PACKETS_GOOD_BAD	Good And Bad 64 Octets Packets Transmitted Count Register	0724 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_65TO127OCTS_PACKETS_GOOD_BAD	Good And Bad 65to127 Octets Packets Transmitted Count Register	0728 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_128TO255OCTS_PACKETS_GOOD_BAD	Good And Bad 128to255 Octets Packets Transmitted Count Register	072C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_256TO511OCTS_PACKETS_GOOD_BAD	Good And Bad 256to511 Octets Packets Transmitted Count Register	0730 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_512TO1023OCTS_PACKETS_GOOD_BAD	Good And Bad 512to1023 Octets Packets Transmitted Count Register	0734 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_1024TO_MAX_OCTS_PACKETS_GOOD_BAD	Good And Bad 1024toMax Octets Packets Transmitted Count Register	0738 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_UNICAST_PACKETS_GOOD_BAD	Good Transmitted Unicast Packets Count Register	073C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTICAST_PACKETS_GOOD_BAD	Good And Bad Transmitted Multicast Packets Count Register	0740 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_BROADCAST_PACKETS_GOOD_BAD	Good And Bad Transmitted Broadcast Packets Count Register	0744 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_UNDERFLOW_ERROR_PACKETS	Transmitted Underflow Error Packets Count Register	0748 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_TX_SINGL_E_COLLISION_GOOD_PACKETS	Good Transmitted Single Collision Count Register	074C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTI_PLE_COLLISION_GOOD_PACKETS	Transmitted Multiple Collision Count Register	0750 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_DEFERRED_PACKETS	Transmitted Deferred Packets Count Register	0754 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_LATE_COLLISION_PACKETS	Transmitted Late Collision Packets Count Register	0758 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_EXCESSIVE_COLLISION_PACKETS	Transmitted Excessive Collision Packets Count Register	075C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_CARRIER_ERROR_PACKETS	Transmitted Carrier Error Packets Count Register	0760 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OCTET_COUNT_GOOD	Good Transmitted Octet Count Register	0764 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PACKET_COUNT_GOOD	Good Transmitted Packet Count Register	0768 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_EXCESSIVE_DEFERRAL_ERROR	Transmitted Excessive Deferral Error Count Register	076C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PAUSE_PACKETS	Transmitted Pause Packets Count Register	0770 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_VLAN_PACKETS_GOOD	Good Transmitted VLAN Packets Count Register	0774 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OSIZE_PACKETS_GOOD	Good Transmitted Osize Packets Count Register	0778 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_PACKETS_COUNT_GOOD_BAD	Good And Bad Received Packets Count Register	0780 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OCTET_COUNT_GOOD_BAD	Good And Bad Received Octet Count Register	0784 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_RX_OCTET_COUNT_GOOD	Good Received Octet Count Register	0788 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_BROADCAST_PACKETS_GOOD	Good Received Broadcast Packets Count Register	078C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_MULTIICAST_PACKETS_GOOD	Good Received Multicast Packets Count Register	0790 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_CRC_ERROR_PACKETS	Received CRC Error Packets Count Register	0794 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_ALIGNMENT_ERROR_PACKETS	Received Alignment Error Count Register	0798 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_RUNTIME_ERROR_PACKETS	Received Runtime Error Count Register	079C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_JABBER_ERROR_PACKETS	Received Jabber Error Count Register	07A0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_UNDERSIZED_PACKETS_GOOD	Good Received Undersized Packets Count Register	07A4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OVERSIZED_PACKETS_GOOD	Good Received Oversized Packets Count Register	07A8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_64OCTETS_PACKETS_GOOD_BAD	Good And Bad 64 Octets Packets Received Count Register	07AC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_65TO127OCTETS_PACKETS_GOOD_BAD	Good And Bad 65to127 Octets Packets Received Count Register	07B0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_128TO255OCTETS_PACKETS_GOOD_BAD	Good And Bad 128to255 Octets Packets Received Count Register	07B4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_256TO511OCTETS_PACKETS_GOOD_BAD	Good And Bad 256to511 Octets Packets Received Count Register	07B8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_RX_512TO1023OCTETS_PA CKETS_GOOD_BAD	Good And Bad 512to1023 Octets Packets Received Count Register	07BC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_1024TOMAXOCTETS_P ACKETS_GOOD_BAD	Good And Bad 1024toMax Octets Packets Received Count Register	07C0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_UNICAST_PACKETS_GOOD	Good Received Unicast Packets Count Register	07C4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LENGTH_ERROR_PACKETS	Received Length Error Packets Count Register	07C8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OUT_OF_RANGE_TYPE_PACKETS	Received Out Of Range Type Count Register	07CC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_PAUSE_PACKETS	Received Pause Packets Count Register	07D0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_FIFO_OVERFLOW_PACKETS	Received FIFO Overflow Count Register	07D4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_VLAN_PACKETS_GOOD_BAD	Good And Bad Received VLAN Packets Count Register	07D8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_WATCHDOG_ERROR_PACKETS	Received Watchdog Error Count Register	07DC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_RECEIVE_ERROR_PACKETS	Received Receive Error Count Register	07E0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_CONTROL_PACKETS_GOOD	Good Received Control Packets Count Register	07E4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_LPI_USEC_CNTR	Transmitted LPI Microseconds Count Register	07EC <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_LPI_TRANSITION_CNTR	Transmitted LPI Transition Count Register	07F0 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_RX_LPI_U SEC_CNTR	Received Microseconds LPI Count Register	07F4 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LPI_T RAN_CNTR	Received LPI Transition Count Register	07F8 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_IPC_ RX_INTERRUPT_ MASK	MMC IPC Receive Interrupts Mask Register	0800 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_IPC_ RX_INTERRUPT	MMC IPC Receive Interrupts Register	0808 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_G OOD_PACKETS	Good Received RxIPv4 Packets Count Register	0810 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_H EADER_ERROR_P ACKETS	Received IPv4 Header Error Packets Count Register	0814 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_N O_PAYLOAD_PAC KETS	Received IPv4 No Payload Packets Count Register	0818 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_F RAGMENTED_PA CKETS	Received IPv4 Fragmented Packets Count Register	081C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_U DP_CHECKSUM_ DISABLED_PAC KETS	Received IPv4 UPD Checksum Disabled Packets Count Register	0820 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_G OOD_PACKETS	Good Received RxIPv6 Packets Count Register	0824 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_H EADER_ERROR_P ACKETS	Received IPv6 Header Error Packets Count Register	0828 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_N O_PAYLOAD_PAC KETS	Received IPv6 No Payload Packets Count Register	082C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_G OOD_PACKETS	Good Received UDP Packets Count Register	0830 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_E RROR_PACKETS	Received UDP Error Packets Count Register	0834 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_RXTCP_GOOD_PACKETS	Good Received TCP Packets Count Register	0838 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_ERROR_PACKETS	Received TCP Error Packets Count Register	083C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_GOOD_PACKETS	Good Received ICMP Packets Count Register	0840 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_ERROR_PACKETS	Received ICMP Error Packets Count Register	0844 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_GOOD_OCTETS	Good Received IPV4 Octets Count Register	0850 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_HEADER_ERROR_OCTETS	Received IPV4 Header Error Octets Count Register	0854 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_NO_PAYLOAD_OCTETS	Received IPV4 No Payload Octets Count Register	0858 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_FRAGMENTED_OCTETS	Received IPV4 Fragmented Octets Count Register	085C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS	Received IPV4 UDP Checksum Disabled Octets Count Register	0860 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_GOOD_OCTETS	Good Received IPV6 Octets Count Register	0864 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_HEADER_ERROR_OCTETS	Received IPV6 Header Error Octets Count Register	0868 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_NO_PAYLOAD_OCTETS	Received IPV6 No Payload Octets Count Register	086C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_GOOD_OCTETS	Good Received UDP Octets Count Register	0870 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_ERROR_OCTETS	Received UDP Error Octets Count Register	0874 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_RXTCP_GOOD_OCTETS	Good Received TCP Octets Count Register	0878 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_EROR_OCTETS	Received TCP Error Octets Count Register	087C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_GOOD_OCTETS	Good Received ICMP Octets Count Register	0880 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_ERROR_OCTETS	Received ICMP Error Octets Count Register	0884 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_CONTROL	MAC Timestamp Control Register	0B00 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SUB_SECOND_INCREMENT	MAC Sub-Second Increment Register	0B04 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_SECONDS	MAC System Time Seconds Register	0B08 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_NANOSECONDS	MAC System Time Nanoseconds Register	0B0C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_SECONDS_UPDATE	MAC System Time Seconds Update Register	0B10 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_NANOSECONDS_UPDATE	MAC System Time Nanoseconds Update Register	0B14 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_ADDEND	MAC Timestamp Addend Register	0B18 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS	MAC System Time Higher Word Seconds Register	0B1C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_STATUS	MAC Timestamp Status Register	0B20 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_MAC_TX_T IMESTAMP_STAT US_NANOSECONDS	MAC Transmit Timestamp Nanoseconds Status Register	0B30 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TX_T IMESTAMP_STAT US_SECONDS	MAC Transmit Timestamp Seconds Status Register	0B34 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_INGRESS _ASYM_CORR	MAC Timestamp Ingress Asymmetry Correction Register	0B50 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_EGRESS _ASYM_CORR	MAC Timestamp Egress Asymmetry Correction Register	0B54 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_INGRESS _CORR_NANOSEC_COND	MAC Timestamp Ingress Correction Nanoseconds Register	0B58 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_EGRESS _CORR_NANOSECOND	MAC Timestamp Egress Correction Nanoseconds Register	0B5C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_INGRESS _CORR_SUBNANOSEC	MAC Timestamp Ingress Correction Subnanoseconds Register	0B60 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME_STAMP_EGRESS _CORR_SUBNANOSEC	MAC Timestamp Egress Correction Subnanoseconds Register	0B64 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS_CONTROL	MAC PPS Control Register	0B70 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS_0_TARGET_TIME _SECONDS	MAC PPS 0 Target Time Seconds Register	0B80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS_0_TARGET_TIME _NANOSECONDS	MAC PPS 0 Target Time Nanoseconds Register	0B84 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS_0_INTERVAL	MAC PPS 0 Interval Register	0B88 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Gigabit Ethernet MAC (GETH)

Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_PPS_0_WIDTH	MAC PPS 0 Width Register	0B8C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_OPERATION_MODE	MTL Operation Mode Register	0C00 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_INTERRUPT_STATUS	MTL Interrupt Status Register	0C20 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ_0_DMA_MAP0	MTL Receive Queue and DMA Channel Mapping 0 Register	0C30 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_OPERATION_MODE	MTL Queue 0 Transmit Operation Mode Register	0D00 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_UNDERFLOW	MTL Queue 0 Transmit Underflow Counter Register	0D04 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_DEBUG	MTL Queue 0 Transmit Debug Register	0D08 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_ETS_STATUS	MTL Queue 0 Transmit Status Register	0D14 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_QUANTUM_WEIGHT	MTL Queue 0 Transmit Quantum or Weights Register	0D18 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_Q0_INTERRUPT_CONTROL_STATUS	MTL Queue 0 Interrupt Control Status Register	0D2C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ_0_OPERATION_MODE	MTL Queue 0 Receive Operation Mode Register	0D30 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ_0_MISSED_PACKET_OVERFLOW_CNT	MTL Queue 0 Receive Missed Packet and Overflow Counter Register	0D34 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ_0_DEBUG	MTL Queue 0 Receive Debug Register	0D38 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ_0_CONTROL	MTL Queue 0 Receive Control Register	0D3C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Gigabit Ethernet MAC (GETH)

Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MTL_TXQi_OPERATION_MODE (i=1-3)	MTL Queue i Transmit Operation Mode Register	0D40 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_UNDERFLOW (i=1-3)	MTL Queue i Transmit Underflow Counter Register	0D44 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_DEBUG (i=1-3)	MTL Queue i Transmit Debug Register	0D48 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_ETS_CONTROL (i=1-3)	MTL Queue i Transmit ETS Control Register	0D50 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_ETS_STATUS (i=1-3)	MTL Queue i Transmit ETS Status Register	0D54 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_QUANTUM_WEIGHT (i=1-3)	MTL Queue i Transmit Quantum or Weights Register	0D58 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_SENDSLOPECREDIT (i=1-3)	MTL Queue i Transmit SendSlopeCredit Register	0D5C <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_HICREDIT (i=1-3)	MTL Queue i Transmit HiCredit Register	0D60 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_LOCREDIT (i=1-3)	MTL Queue i Transmit LoCredit Register	0D64 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_Qi_INTERRUPT_CONTROL_STATUS (i=1-3)	MTL Queue i Interrupt Status Register	0D6C <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_OPERATION_MODE (i=1-3)	MTL Queue i Receive Operation Mode Register	0D70 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_MISSED_PACKET_OVERFLOW_COUNTER (i=1-3)	MTL Queue i Receive Missed Packet and Overflow Counter Register	0D74 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Gigabit Ethernet MAC (GETH)

Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MTL_RXQi_DEBUG (i=1-3)	MTL Queue i Receive Debug Register	0D78 <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_CONTROL (i=1-3)	MTL Queue i Receive Control Register	0D7C <sub>H</sub> +(i-1)*40 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_MODE	DMA Bus Mode Register	1000 <sub>H</sub>	U,SV	U,SV,P	Application Reset	<a href="#">20</a>
GETH_DMA_SYS_BUS_MODE	DMA System Bus Mode Register	1004 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_INTE_RRUPT_STATUS	DMA Interrupt Status Register	1008 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_DEB_UG_STATUS0	DMA Debug Status 0 Register	100C <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_DEB_UG_STATUS1	DMA Debug Status 1 Register	1010 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CONTROL (i=0-3)	DMA Channel i Control Register	1100 <sub>H</sub> +i*80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TX_CONTROL (i=0-3)	DMA Channel i Transmit Control Register	1104 <sub>H</sub> +i*80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RX_CONTROL (i=0-3)	DMA Channel i Receive Control Register	1108 <sub>H</sub> +i*80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TXDESC_LIST_ADDRESS (i=0-3)	DMA Channel i Transmit Descriptor List Address Register	1114 <sub>H</sub> +i*80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RXDESC_LIST_ADDRESS (i=0-3)	DMA Channel i Receive Descriptor List Address Register	111C <sub>H</sub> +i*80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TXDESC_TAIL_POINTER (i=0-3)	DMA Channel i Transmit Descriptor Tail Pointer Register	1120 <sub>H</sub> +i*80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
GETH_DMA_CHi_RXDESC_TAIL_P_OINTER (i=0-3)	DMA Channel i Recieve Descriptor Tail Pointer Register	1128 <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TXDESC_RING_LENGTH (i=0-3)	DMA Channel i Transmit Descriptor Ring Length Register	112C <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RXDESC_RING_LENGTH (i=0-3)	DMA Channel i Recieve Descriptor Ring Length Register	1130 <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_INTERRUPT_ENABLER (i=0-3)	DMA Channel i Interrupt Enable Register	1134 <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RX_INTERRUPT_WATCHDOG_TIMER (i=0-3)	DMA Channel i Recieve Interrupt Watchdog Timer Register	1138 <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_SLOT_FUNCTION_CONTROL_STATUS (i=0-3)	DMA Channel i Slot Function Control and Status Register	113C <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APP_TXDESC (i=0-3)	DMA Channel i Current Application Transmit Descriptor Register	1144 <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APP_RXDESC (i=0-3)	DMA Channel i Current Application Receive Descriptor Register	114C <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APP_TXBUFFER (i=0-3)	DMA Channel i Current Application Transmit Buffer Address Register	1154 <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APP_RXBUFFER (i=0-3)	DMA Channel i Current Application Receive Buffer Address Register	115C <sub>H</sub> +i* 80 <sub>H</sub>	U,SV	U,SV,P	Application Reset	See Family Spec

## Gigabit Ethernet MAC (GETH)

Table 459 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_DMA_CHi_STATUS (i=0-3)	DMA Channel i Status Register	$1160_H+i*80_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_MISS_FRAME_CNT (i=0-3)	DMA Channel i Missed Frames Count Register	$1164_H+i*80_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_CLC	Clock Control Register	$2000_H$	SV,U	SV,E,P	Application Reset	See Family Spec
GETH_ID	Module Identification Register	$2004_H$	SV,U	BE	Application Reset	See Family Spec
GETH_GPCTL	General Purpose Control Register	$2008_H$	SV,U	SV,P	Application Reset	See Family Spec
GETH_ACCENO	Access Enable Register 0	$200C_H$	U,SV	SV,SE	Application Reset	See Family Spec
GETH_ACCEN1	Access Enable Register 1	$2010_H$	U,SV	SV,SE	Application Reset	See Family Spec
GETH_KRST0	Kernel Reset Register 0	$2014_H$	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_KRST1	Kernel Reset Register 1	$2018_H$	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_KRSTCLR	Kernel Reset Status Clear Register	$201C_H$	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_ACCEN0Dx (x=0-3)	Access Enable Register 0 for DMAx	$2020_H+x*8$	U,SV	SV,SE	Application Reset	See Family Spec
GETH_ACCEN1Dx (x=0-3)	Access Enable Register 1 for DMAx	$2024_H+x*8$	U,SV	SV,SE	Application Reset	See Family Spec
GETH_SKEWCTL	Skew Control Register	$2040_H$	SV,U	SV,P	Application Reset	See Family Spec

**Gigabit Ethernet MAC (GETH)****42.3 TC39x-B Specific Registers****42.3.1 FPI bus interface****MAC Extended Configuration Register**

The MAC Extended Configuration Register establishes the operating mode of the MAC.

**GETH\_MAC\_EXT\_CONFIGURATION****MAC Extended Configuration Register**(0004<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
<b>RES_3 1</b>	<b>RES_3 0</b>						<b>EIPG</b>		<b>EIPGE N</b>	<b>RES_2 3</b>					<b>DCRC C</b>
r	r			rw			rw	r			rw	r	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES_15_14</b>										<b>GPSL</b>					
r										rw					

Field	Bits	Type	Description
<b>GPSL</b>	13:0	rw	<b>Giant Packet Size Limit</b> If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register. Value After Reset: 0x0
<b>RES_15_14</b>	15:14	r	<b>Reserved</b> Value After Reset: 0x0
<b>DCRCC</b>	16	rw	<b>Disable CRC Checking for Received Packets</b> When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. Value After Reset: 0x0
<b>SPEN</b>	17	rw	<b>Slow Protocol Detection Enable</b> When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. Value After Reset: 0x0

**Gigabit Ethernet MAC (GETH)**

Field	Bits	Type	Description
<b>USP</b>	18	rw	<b>Unicast Slow Protocol Packet Detect</b> When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2008, Section 5. Value After Reset: 0x0
<b>RES_19</b>	19	r	<b>Reserved</b> Value After Reset: 0x0
<b>HDSMS</b>	22:20	rw	<b>Maximum Size for Splitting the Header Data</b> These bits indicate the maximum header size allowed for splitting the header data in the received packet: $101_B$ - $111_B$ Reserved If the Enable Split Header Structure option is not selected, these bits are reserved and read-only (RO). Value After Reset: 0x0 $000_B$ 64 bytes $001_B$ 128 bytes $010_B$ 256 bytes $011_B$ 512 bytes $100_B$ 1024 bytes
<b>RES_23</b>	23	r	<b>Reserved</b> Value After Reset: 0x0
<b>EIPGEN</b>	24	rw	<b>Extended Inter-Packet Gap Enable</b> When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. Value After Reset: 0x0

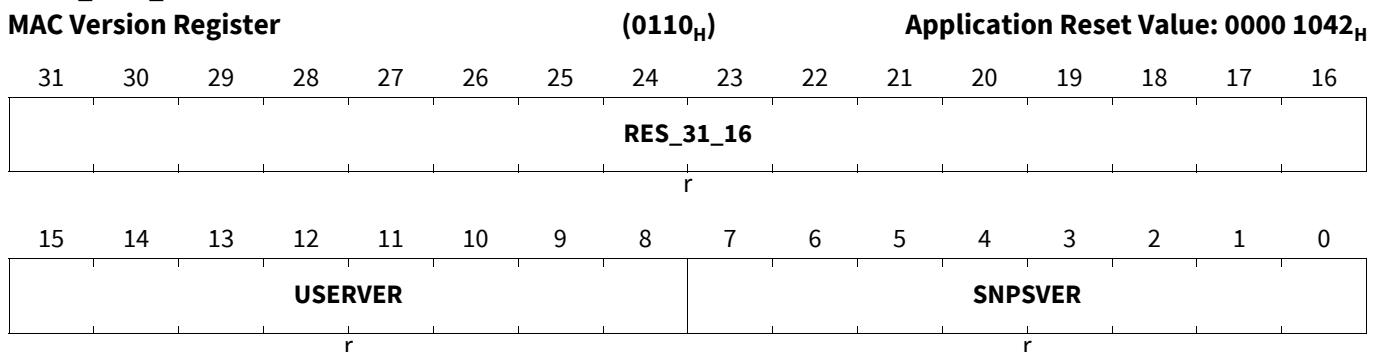
## Gigabit Ethernet MAC (GETH)

Field	Bits	Type	Description
EIPG	29:25	rw	<b>Extended Inter-Packet Gap</b> The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ----- 8'hFF - 2144 bit times Value After Reset: 0x0
RES_30	30	r	<b>Reserved</b> Value After Reset: 0x0
RES_31	31	r	<b>Reserved</b> Value After Reset: 0x0

### MAC Version Register

The version register identifies the version of the DWC\_ether\_qos. This register contains two bytes: one that Synopsys uses to identify the core release number, and the other that you set while configuring the core.

#### GETH\_MAC\_VERSION



Field	Bits	Type	Description
SNPSVER	7:0	r	<b>Synopsys-defined Version</b> IP Version
USERVER	15:8	r	<b>User-defined Version (configured with coreConsultant)</b> Value After Reset: 0x10
RES_31_16	31:16	r	<b>Reserved</b> Value After Reset: 0x0

### DMA Bus Mode Register

The Bus Mode register establishes the bus operating modes for the DMA.

## Gigabit Ethernet MAC (GETH)

## GETH\_DMA\_MODE

## DMA Bus Mode Register

(1000<sub>H</sub>)Application Reset Value: 0000 0000<sub>H</sub>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES_18_31														INTM	
r														rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_15	PR		TXPR	RES_10	RES_9	RES_8_5				TAA		DA	SWR		
r	rw		rw	r	r	r				rw		rw	rw		

Field	Bits	Type	Description
SWR	0	rw	<p><b>Software Reset</b></p> <p>When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1.</p> <p><b>Note:</b> The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>Value After Reset: 0x0</p>
DA	1	rw	<p><b>DMA Tx or Rx Arbitration Scheme</b></p> <p>This bit specifies the arbitration scheme between the Transmit and Receive paths of all channels:</p> <p>The priority between the paths is according to the priority specified in Bits[14:12] and the priority weight is specified in the TXPR bit.</p> <p>The Tx path has priority over the Rx path when the TXPR bit is set.</p> <p>Otherwise, the Rx path has priority over the Tx path.</p> <p>Value After Reset: 0x0</p> <p>0<sub>B</sub> Weighted Round-Robin with Rx:Tx or Tx:Rx 1<sub>B</sub> Fixed Priority</p>
TAA	4:2	rw	<p><b>Transmit Arbitration Algorithm</b></p> <p>This field is used to select the arbitration algorithm for the Transmit side when multiple Tx DMAs are selected.</p> <p>011-111<sub>B</sub> Reserved</p> <p>Value After Reset: 0x0</p> <p>000<sub>B</sub> Fixed priority. In fixed priority, Channel 0 has the lowest priority and the last channel has the highest priority.</p> <p>001<sub>B</sub> Weighted Strict Priority (WSP)</p> <p>010<sub>B</sub> Weighted Round-Robin (WRR)</p>

**Gigabit Ethernet MAC (GETH)**

Field	Bits	Type	Description
<b>RES_8_5</b>	8:5	r	<b>Reserved</b> Value After Reset: 0x0
<b>RES_9</b>	9	r	<b>Reserved</b> Value After Reset: 0x0
<b>RES_10</b>	10	r	<b>Reserved</b> Value After Reset: 0x0
<b>TXPR</b>	11	rw	<b>Transmit Priority</b> When set, this bit indicates that the Tx DMA has higher priority than the Rx DMA during arbitration for the system-side bus. Value After Reset: 0x0
<b>PR</b>	14:12	rw	<b>Priority Ratio</b> These bits control the priority ratio in weighted round-robin arbitration between the Rx DMA and Tx DMA. These bits are valid only when the DA bit is reset. The priority ratio is Rx:Tx or Tx:Rx depending on whether the TXPR bit is reset or set. Value After Reset: 0x0 000 <sub>B</sub> The priority ratio is 1:1 001 <sub>B</sub> The priority ratio is 2:1 010 <sub>B</sub> The priority ratio is 3:1 011 <sub>B</sub> The priority ratio is 4:1 100 <sub>B</sub> The priority ratio is 5:1 101 <sub>B</sub> The priority ratio is 6:1 110 <sub>B</sub> The priority ratio is 7:1 111 <sub>B</sub> The priority ratio is 8:1
<b>RES_15</b>	15	r	<b>Reserved</b> Value After Reset: 0x0

**Gigabit Ethernet MAC (GETH)**

Field	Bits	Type	Description
<b>INTM</b>	17:16	rw	<p><b>Interrupt Mode</b>  This field defines the interrupt mode of DWC_ether_qos.  The behavior of the following outputs changes depending on the following settings:</p> <ul style="list-style-type: none"> <li>• sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt)</li> <li>• sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt)</li> <li>• sbd_intr_o (Common Interrupt)</li> </ul> <p>It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. For more details please refer Table "DWC_ether_qos Transfer Complete Interrupt Behavior".  Value After Reset: 0x0</p> <p>00<sub>B</sub> sbd_perch_* are pulse signals for each completion events.  sbd_intr_o is also asserted and cleared only when software clears the corresponding RI/TI status bits</p> <p>01<sub>B</sub> sbd_perch_* are level signals asserted on corresponding event and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these packet transfer completion events.</p> <p>10<sub>B</sub> sbd_perch_* are level signals asserted on corresponding event and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these packet transfer completion events.</p> <p>11<sub>B</sub> Reserved</p>
<b>RES_18_31</b>	31:18	r	<p><b>Reserved</b>  Value After Reset: 0x0</p>

**42.4 Connectivity**

If for one product no signal is connected to an alternate input, it is connected to GND internally at module entity level. This allows to leave some signals unconnected in the application (i.e. RXER, CRS, COL) and save pins and external connection to GND. The tables below list all the connections of the instances.

**Table 460 Connections of GETH**

Interface Signals	connects		Description
GETH:COLA	from	P11.15:IN	Collision MII
GETH:CRSA	from	P11.14:IN	Carrier Sense MII
GETH:CRSB	from	P11.11:IN	Carrier Sense MII
GETH:CRSDVA	from	P11.11:IN	Carrier Sense / Data Valid combi-signal for RMII
GETH:CRSDVB	from	P11.14:IN	Carrier Sense / Data Valid combi-signal for RMII
GETH:GREFCLK	from	TC39x-B:P11.5	Gigabit Reference Clock input for RGMII (125 MHz high precision)

**Gigabit Ethernet MAC (GETH)****Table 460 Connections of GETH (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
GETH:MDC	to	P02.8:ALT(6)	MDIO clock
		P12.0:ALT(6)	
		P21.2:ALT(5)	
GETH:MDIO	to	P00.0:HWOUT(0)	MDIO Output
		P12.1:HWOUT(0)	
		P21.3:HWOUT(0)	
GETH:MDIOA	from	P00.0:IN	MDIO Input
GETH:MDIOC	from	P12.1:IN	MDIO Input
GETH:MDIOD	from	P21.3:IN	MDIO Input
GETH:PPS	to	P14.4:ALT(6)	Pulse Per Second
GETH:RCTLA	from	P11.11:IN	Receive Control for RGMII
GETH:REFCLKA	from	P11.12:IN	Reference Clock input for RMII (50 MHz)
GETH:RXCLKA	from	P11.12:IN	Receive Clock MII and RGMII
GETH:RXCLKB	from	P11.4:IN	Receive Clock MII and RGMII
GETH:RXCLKC	from	P12.0:IN	Receive Clock MII and RGMII
GETH:RXD0A	from	P11.10:IN	Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
GETH:RXD1A	from	P11.9:IN	Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
GETH:RXD2A	from	P11.8:IN	Receive Data 2 MII and RGMII (RGMII can use RXD2A only)
GETH:RXD3A	from	P11.7:IN	Receive Data 3 MII and RGMII (RGMII can use RXD3A only)
GETH:RXDVA	from	P11.11:IN	Receive Data Valid MII
GETH:RXDVB	from	P11.14:IN	Receive Data Valid MII
GETH:RXERA	from	P11.13:IN	Receive Error MII
GETH:RXERB	from	P21.7:IN	Receive Error MII
GETH:RXERC	from	P10.0:IN	Receive Error MII
GETH:TRIGO(9:0)	to	INT:eth.TRIGO(9:0)	Ethernet Service Request
GETH:TCTL	to	TC39x-B:P11.6	Transmit Control for RGMII
GETH:TXCLK	to	TC39x-B:P11.4	Transmit Clock Output for MII and RGMII
GETH:TXCLKA	from	P11.5:IN	Transmit Clock Input for MII
GETH:TXCLKB	from	P11.12:IN	Transmit Clock Input for MII
GETH:TXD(0)	to	TC39x-B:P11.3	Transmit Data
GETH:TXD(1)	to	TC39x-B:P11.2	Transmit Data
GETH:TXD(2)	to	TC39x-B:P11.1	Transmit Data
GETH:TXD(3)	to	TC39x-B:P11.0	Transmit Data
GETH:TXEN	to	TC39x-B:P11.6	Transmit Enable MII and RMII
GETH:TXER	to	P11.4:ALT(6)	Transmit Error MII

## Gigabit Ethernet MAC (GETH)

### 42.5 DMA Burst Lengths Limitations by the System

Not all burst lengths of the IP are supported by the system.

The GETH kernel IP supports various burst length of 1 up to 32 beats as defined in DMA\_CHi\_TX\_CONTROL.TxPBL and GETH\_DMA\_CHi\_RX\_CONTROL.RxPBL. They can be multiplied by 8 by setting DMA\_CH(#i)\_Control.PBLx8.

Other than specified in the IP only the following burst lengths are supported by the system: SINGLE, INCR4, INCR8. Note that DMA\_CH(#i)\_Control.PBLx8 must not be set with PBL values higher than 1.

### 42.6 Buffer and Descriptor Alignment

The GETH is implemented as a 32 bit peripheral. Nevertheless it is connected to 64 bit wide bus (SRI). To make full use of the possible performance of SRI and its bridges, the data buffers and the descriptors need to be aligned to 64 bit addresses.

### 42.7 Embedded FIFOs

The GETH uses two embedded FIFOs. The TX FIFO has a size of 4 kByte, the RX FIFO has a size of 8 kByte.

### 42.8 Master TAG ID

The module has 4 DMA Channels that share one master interface connecting them to the SRI bus. In order to distinguish the 4 DMAs from each other in the system, the master tag ID will dynamically be changed depending on the currently active DMA. [Table 461](#) details which ID is presented for each DMA.

**Table 461 Master TAG IDs for the Gigabit Ethernet MAC**

DMA	Master TAG ID
DMA0	0x28 <sub>H</sub>
DMA1	0x29 <sub>H</sub>
DMA2	0x2A <sub>H</sub>
DMA3	0x2B <sub>H</sub>

### 42.9 Interrupt Service Requests

The module has 10 Service Request Nodes connecting it to the interrupt system. The interrupt request lines are connected to the interrupt controller as shown in [Table 462](#).

**Table 462 Service Request Lines of Ethernet MAC**

IR SRC	GETH IP signal	GETH IP function	Description
SRC_GETH0	GETH_TRIGO0	GETH_INTR	DMA functions (sbd_intr_o), this internal line is connected via OR gate to GETH.SR0 wake up on LAN (pmt_intr_o), this internal line is connected via OR gate to GETH.SR0 wake up on EEE - LPI (lpi_intr_o), this internal line is connected via OR gate to GETH.SR0
SRC_GETH1	GETH_TRIGO1	GETH_PPS	Pulse Per Second signal from Precision Time Protocol (ptp_pps_o)
SRC_GETH2	GETH_TRIGO2	GETH_TX_DMA0	TX interrupt from DMA 0 (sbd_perch_tx_intr_o[0])
SRC_GETH3	GETH_TRIGO3	GETH_TX_DMA1	TX interrupt from DMA 1(sbd_perch_tx_intr_o[1])

## Gigabit Ethernet MAC (GETH)

**Table 462 Service Request Lines of Ethernet MAC (cont'd)**

IR SRC	GETH IP signal	GETH IP function	Description
SRC_GETH4	GETH_TRIGO4	GETH_TX_DMA2	TX interrupt from DMA 2(sbd_perch_tx_intr_o[2])
SRC_GETH5	GETH_TRIGO4	GETH_TX_DMA3	TX interrupt from DMA 3(sbd_perch_tx_intr_o[3])
SRC_GETH6	GETH_TRIGO6	GETH_RX_DMA0	RX interrupt from DMA 0 (sbd_perch_rx_intr_o[0])
SRC_GETH7	GETH_TRIGO7	GETH_RX_DMA1	RX interrupt from DMA 1(sbd_perch_rx_intr_o[1])
SRC_GETH8	GETH_TRIGO8	GETH_RX_DMA2	RX interrupt from DMA 2(sbd_perch_rx_intr_o[2])
SRC_GETH9	GETH_TRIGO9	GETH_RX_DMA3	RX interrupt from DMA 3(sbd_perch_rx_intr_o[3])

## 42.10 Clocks

The module has multiple clock inputs and outputs connecting it to the system. They are connected to the system as shown in **Table 463**.

If the application wants to use the IP in RGMII mode the application has to execute the following steps:

- Prior to the application reset the application must switch on  $f_{GETH}$  (by configuring CCUCON5.GETHDIV)
- Attach an external 125 MHz clock to input GREFCLK
- Activate the application reset
- Wait for 10  $\mu$ s

**Table 463 Clock Lines of Ethernet MAC**

Clock Line	Connected to	Description
hclk_i / $f_{AHB}$	$f_{GETH}$	AHB master interface clock
clk_csr_i / $f_{CSR}$	$f_{SPB}$	AHB slave interface clock
clk_tx_i	GETH_TXCLK (port pin)	MII transmit clock Input from PHY (10/100 MBit/s) The external PHY or oscillator provides this transmission clock. TXD[3:0] is synchronous to this clock. This is 25 MHz in 100 Mbps mode and 2.5 MHz in 10 Mbps mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_gref_i	GETH_GREFCLK (port pin)	RGMII transmit clock <b>Reference Input</b> from PHY (1000 MBit/s). The external PHY or oscillator provides this clock as reference. TXD[3:0] is not necessarily synchronous to this clock! This is always 125 MHz in 1000/100/10 MBit/s mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_tx_o	GETH_TXCLK (port pin)	RGMII transmission clock <b>Output</b> to PHY (1000 MBit/s) . TXD[3:0] is synchronous (DDR) to this 125 MHz clock to the PHY. If RGMII is downgraded to 100 MBit/s it is divided internally to 25 MHz and for 10 MBit/s to 2.5 MHz. In each case it is generated from clk_gref_i by respective division. This division is controlled automatically by evaluation of mac_speed_o[1:0] and phy_intf_sel_i[2:0]. TXCLK has the same on chip delay and output pad delay as the TXD signals and TCTL unless clock skew is selected in SKEW.

## Gigabit Ethernet MAC (GETH)

**Table 463 Clock Lines of Ethernet MAC (cont'd)**

Clock Line	Connected to	Description
clk_rx_i	GETH_RXCLK (port pin)	Receive clock from Phy. The external PHY provides this receive clock for RGMII, GMII, MII, and RMII interfaces. This clock is 125 MHz in 1 Gbps mode, 25 MHz in 100 Mbps mode, 2.5 MHz in 10 Mbps mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_rmii_i	GETH_REFCLK (port pin)	50-MHz clock used by the RMII from PHY. In 100 MBit/s Mode, it is divided internally to 25 MHz and provided to the internal MII interface. If RMII is downgraded to 10 MBit/s it is divided internally to 2.5 MHz. This division is controlled automatically by evaluation of mac_speed_o[1:0] and phy_intf_sel_i[2:0]. Needs a clock input during SW reset (GETH_BUS_MODE.SWR).
clk_ptp_ref_i	$f_{GETH}$	Reference Clock for the Time Stamp Update Logic

## 42.11 Revision History

**Table 464 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.3.10</b>		
<a href="#">Page 27</a>	Previous versions removed from revision history.	
<a href="#">Page 23</a>	Connections table changed (no functional changes).	
<b>V1.3.11</b>		
<a href="#">Page 26</a>	Typo fixed for clock line hclk_i / $f_{AHB}$ .	-
<b>V1.3.12</b>		
<a href="#">Page 26</a>	$f_{SRI}$ changed to $f_{GETH}$ as connection of clk_ptp_ref_i.	
<a href="#">Page 23</a>	Updated connection of MII and RGMII in <a href="#">Connectivity</a> .	
<a href="#">Page 23</a>	Clean up connection from TC39X:P11.x in <a href="#">Connectivity</a> .	
<b>V1.3.13</b>		
-	No functional changes.	-
<b>V1.3.14</b>		
-	No functional changes.	-
<b>V1.3.15</b>		
-	No functional changes.	-

## External Bus Unit (EBU)

### 43 External Bus Unit (EBU)

The EBU is implemented only on the TC39x devices of the AURIX™ TC3XX product family

#### 43.1 TC39x-B Specific IP Configuration

A pin multiplexing scheme has been implemented to allow the use of low power, 5 volt compatible pads for the 32 bit databus. This has the effect of imposing the following limitations on EBU configuration

- Some programming of the Ports logic is needed to ensure that the correct pads are available for EBU to operate
- SDRAM is not supported
- Use of byte control lines limits the available external address bus to A(19:0).
- Region 2 cannot be used if external bus arbitration is enabled. External bus arbitration is not supported so no advantage is gained by enabling it.
- The use of slower pads for the main databus means that extra setup time may be needed for asynchronous writes and that the clock frequency for synchronous writes may have to be reduced.
- The combined CS signal described in Section 1.3.10.7 is not available as a device I/O for the TC39x.

It is possible to programme the EBU ignoring these restrictions but doing so will result in unpredictable operation and possible lockups of the system.

#### 43.2 TC39x-B Specific Register Set

**Table 465 Register Address Space - EBU**

Module	Base Address	End Address	Note
(EBU)	82000000 <sub>H</sub>	87FFFFFF <sub>H</sub>	Access to External Memory via cached address range
	A2000000 <sub>H</sub>	A7FFFFFF <sub>H</sub>	Access to external memory via non-cached address range
EBU	F8400000 <sub>H</sub>	F840FFFF <sub>H</sub>	sri slave interface

**Table 466 Register Overview - EBU (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
EBU_CLC	EBU Clock Control Register	0000000 <sub>H</sub>	U,SV,32, 64	SV,P,E,32,6 4	Application Reset	See Family Spec
EBU_MODCON	EBU Configuration Register	0000004 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	See Family Spec	See Family Spec
EBU_MODID	EBU Module Identification Register	0000008 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_USERCON	EBU Test/Control Configuration Register	000000C <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec

**External Bus Unit (EBU)****Table 466 Register Overview - EBU (ascending Offset Address) (cont'd)**

<b>Short Name</b>	<b>Long Name</b>	<b>Offset Address</b>	<b>Access Mode</b>		<b>Reset</b>	<b>Page Number</b>
			<b>Read</b>	<b>Write</b>		
EBU_EXTBOOT	EBU External Boot Configuration Register	0000010 <sub>H</sub>	U,SV,32	SV,P,32	Application Reset	See Family Spec
EBU_ADDRSELx (x=0-2)	EBU Address Select Register x	0000018 <sub>H</sub> +x*4	U,SV,32, 64	SV,P,32,64	See Family Spec	See Family Spec
EBU_BUSRCONx (x=0-2)	EBU Bus Configuration Register	0000028 <sub>H</sub> +x*10 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_BUSRAPx (x=0-2)	EBU Bus Read Access Parameter Register	000002C <sub>H</sub> +x*10 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_BUSWCONx (x=0-2)	EBU Bus Write Configuration Register	0000030 <sub>H</sub> +x*10 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_BUSWAPx (x=0-2)	EBU Bus Write Access Parameter Register	0000034 <sub>H</sub> +x*10 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_SDRMCON	EBU SDRAM Control Register	0000068 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_SDRMOD	EBU SDRAM Mode Register	000006C <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_SDRMREF	EBU SDRAM Refresh Control Register	0000070 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_SDRSTAT	EBU SDRAM Status Register	0000074 <sub>H</sub>	U,SV,32, 64	SV,P,32,64	Application Reset	See Family Spec
EBU_ACCEN0	EBU Access Enable Register 0	00000B0 <sub>H</sub>	U,SV,32, 64	SV,SE,32,64	Application Reset	See Family Spec
EBU_ACCEN1	EBU Access Enable Register 1	00000B4 <sub>H</sub>	U,SV,32, 64	SV,SE,32,64	Application Reset	See Family Spec

**43.3 TC39x-B Specific Registers**

There are no registers specific to the TC39x

**43.4 Connectivity**

**External Bus Unit (EBU)****Table 467 Connections of EBU**

<b>Interface Signals</b>	<b>connects</b>	<b>Description</b>
EBU:A(0)	to P24.14:HWOUT(0)	Address Output
EBU:A(1)	to P24.12:HWOUT(0)	Address Output
EBU:A(2)	to P24.13:HWOUT(0)	Address Output
EBU:A(3)	to P24.11:HWOUT(0)	Address Output
EBU:A(4)	to P24.10:HWOUT(0)	Address Output
EBU:A(5)	to P24.6:HWOUT(0)	Address Output
EBU:A(6)	to P24.9:HWOUT(0)	Address Output
EBU:A(7)	to P24.15:HWOUT(0)	Address Output
EBU:A(8)	to P24.7:HWOUT(0)	Address Output
EBU:A(9)	to P24.4:HWOUT(0)	Address Output
EBU:A(10)	to P24.8:HWOUT(0)	Address Output
EBU:A(11)	to P24.0:HWOUT(0)	Address Output
EBU:A(12)	to P24.5:HWOUT(0)	Address Output
EBU:A(13)	to P24.3:HWOUT(0)	Address Output
EBU:A(14)	to P24.2:HWOUT(0)	Address Output
EBU:A(15)	to P24.1:HWOUT(0)	Address Output
EBU:A(16)	to P25.15:HWOUT(0)	Address Output
EBU:A(17)	to P25.13:HWOUT(0)	Address Output
EBU:A(18)	to P25.14:HWOUT(0)	Address Output
EBU:A(19)	to P25.12:HWOUT(0)	Address Output
EBU:A(20)	to P25.11:ALT(5)	Address Output
EBU:A(21)	to P25.10:ALT(5)	Address Output
EBU:A(22)	to P25.9:ALT(5)	Address Output
EBU:A(23)	to P25.8:ALT(5)	Address Output
EBU:AD(0)	to P30.9:HWOUT(0)	Data Bus Output
EBU:AD(1)	to P30.14:HWOUT(0)	Data Bus Output
EBU:AD(2)	to P30.13:HWOUT(0)	Data Bus Output
EBU:AD(3)	to P30.8:HWOUT(0)	Data Bus Output
EBU:AD(4)	to P30.6:HWOUT(0)	Data Bus Output
EBU:AD(5)	to P30.10:HWOUT(0)	Data Bus Output
EBU:AD(6)	to P30.15:HWOUT(0)	Data Bus Output
EBU:AD(7)	to P30.7:HWOUT(0)	Data Bus Output
EBU:AD(8)	to P30.4:HWOUT(0)	Data Bus Output
EBU:AD(9)	to P30.12:HWOUT(0)	Data Bus Output
EBU:AD(10)	to P30.11:HWOUT(0)	Data Bus Output
EBU:AD(11)	to P30.1:HWOUT(0)	Data Bus Output
EBU:AD(12)	to P30.2:HWOUT(0)	Data Bus Output

**External Bus Unit (EBU)****Table 467 Connections of EBU (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
EBU:AD(13)	to	P30.5:HWOUT(0)	Data Bus Output
EBU:AD(14)	to	P30.0:HWOUT(0)	Data Bus Output
EBU:AD(15)	to	P30.3:HWOUT(0)	Data Bus Output
EBU:AD(16)	to	P31.7:HWOUT(0)	Data Bus Output
EBU:AD(17)	to	P31.15:HWOUT(0)	Data Bus Output
EBU:AD(18)	to	P31.14:HWOUT(0)	Data Bus Output
EBU:AD(19)	to	P31.12:HWOUT(0)	Data Bus Output
EBU:AD(20)	to	P31.6:HWOUT(0)	Data Bus Output
EBU:AD(21)	to	P31.10:HWOUT(0)	Data Bus Output
EBU:AD(22)	to	P31.13:HWOUT(0)	Data Bus Output
EBU:AD(23)	to	P31.5:HWOUT(0)	Data Bus Output
EBU:AD(24)	to	P31.4:HWOUT(0)	Data Bus Output
EBU:AD(25)	to	P31.11:HWOUT(0)	Data Bus Output
EBU:AD(26)	to	P31.3:HWOUT(0)	Data Bus Output
EBU:AD(27)	to	P31.9:HWOUT(0)	Data Bus Output
EBU:AD(28)	to	P31.2:HWOUT(0)	Data Bus Output
EBU:AD(29)	to	P31.1:HWOUT(0)	Data Bus Output
EBU:AD(30)	to	P31.0:HWOUT(0)	Data Bus Output
EBU:AD(31)	to	P31.8:HWOUT(0)	Data Bus Output
EBU:ADV	to	P25.7:HWOUT(0)	Address Valid Control Signal
EBU:ADV_FDBK	from	P25.7:IN	ADV Control Signal Feedback
EBU:AD_IN(0)	from	P30.9:IN	Data Bus Input
EBU:AD_IN(1)	from	P30.14:IN	Data Bus Input
EBU:AD_IN(2)	from	P30.13:IN	Data Bus Input
EBU:AD_IN(3)	from	P30.8:IN	Data Bus Input
EBU:AD_IN(4)	from	P30.6:IN	Data Bus Input
EBU:AD_IN(5)	from	P30.10:IN	Data Bus Input
EBU:AD_IN(6)	from	P30.15:IN	Data Bus Input
EBU:AD_IN(7)	from	P30.7:IN	Data Bus Input
EBU:AD_IN(8)	from	P30.4:IN	Data Bus Input
EBU:AD_IN(9)	from	P30.12:IN	Data Bus Input
EBU:AD_IN(10)	from	P30.11:IN	Data Bus Input
EBU:AD_IN(11)	from	P30.1:IN	Data Bus Input
EBU:AD_IN(12)	from	P30.2:IN	Data Bus Input
EBU:AD_IN(13)	from	P30.5:IN	Data Bus Input
EBU:AD_IN(14)	from	P30.0:IN	Data Bus Input
EBU:AD_IN(15)	from	P30.3:IN	Data Bus Input
EBU:AD_IN(16)	from	P31.7:IN	Data Bus Input

**External Bus Unit (EBU)****Table 467 Connections of EBU (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
EBU:AD_IN(17)	from	P31.15:IN	Data Bus Input
EBU:AD_IN(18)	from	P31.14:IN	Data Bus Input
EBU:AD_IN(19)	from	P31.12:IN	Data Bus Input
EBU:AD_IN(20)	from	P31.6:IN	Data Bus Input
EBU:AD_IN(21)	from	P31.10:IN	Data Bus Input
EBU:AD_IN(22)	from	P31.13:IN	Data Bus Input
EBU:AD_IN(23)	from	P31.5:IN	Data Bus Input
EBU:AD_IN(24)	from	P31.4:IN	Data Bus Input
EBU:AD_IN(25)	from	P31.11:IN	Data Bus Input
EBU:AD_IN(26)	from	P31.3:IN	Data Bus Input
EBU:AD_IN(27)	from	P31.9:IN	Data Bus Input
EBU:AD_IN(28)	from	P31.2:IN	Data Bus Input
EBU:AD_IN(29)	from	P31.1:IN	Data Bus Input
EBU:AD_IN(30)	from	P31.0:IN	Data Bus Input
EBU:AD_IN(31)	from	P31.8:IN	Data Bus Input
EBU:A_IN(0)	from	P24.14:IN	Address Input
EBU:A_IN(1)	from	P24.12:IN	Address Input
EBU:A_IN(2)	from	P24.13:IN	Address Input
EBU:A_IN(3)	from	P24.11:IN	Address Input
EBU:A_IN(4)	from	P24.10:IN	Address Input
EBU:A_IN(5)	from	P24.6:IN	Address Input
EBU:A_IN(6)	from	P24.9:IN	Address Input
EBU:A_IN(7)	from	P24.15:IN	Address Input
EBU:A_IN(8)	from	P24.7:IN	Address Input
EBU:A_IN(9)	from	P24.4:IN	Address Input
EBU:A_IN(10)	from	P24.8:IN	Address Input
EBU:A_IN(11)	from	P24.0:IN	Address Input
EBU:A_IN(12)	from	P24.5:IN	Address Input
EBU:A_IN(13)	from	P24.3:IN	Address Input
EBU:A_IN(14)	from	P24.2:IN	Address Input
EBU:A_IN(15)	from	P24.1:IN	Address Input
EBU:BA(0)	to	P25.3:ALT(7)	Bank Address
EBU:BAA	to	P25.3:ALT(7)	Burst Address Advance
EBU:BC(0)	to	P25.8:HWOUT(0)	Byte Control
EBU:BC(1)	to	P25.9:HWOUT(0)	Byte Control
EBU:BC(2)	to	P25.10:HWOUT(0)	Byte Control
EBU:BC(3)	to	P25.11:HWOUT(0)	Byte Control
EBU:BFCLKI	from	P26.0:IN	Burst Flash Clock Feedback

**External Bus Unit (EBU)****Table 467 Connections of EBU (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
EBU:BFCLKO	to	P25.0:HWOUT(0)	Burst Flash Clock Output
EBU:CS(0)	to	P25.5:HWOUT(0)	Chip Select
EBU:CS(1)	to	P25.4:HWOUT(0)	Chip Select
EBU:CS(2)	to	P25.3:HWOUT(0)	Chip Select
EBU:CS_FDBK(0)	from	P25.5:IN	Chip Select Feedback
EBU:CS_FDBK(1)	from	P25.4:IN	Chip Select Feedback
EBU:CS_FDBK(2)	from	P25.3:IN	Chip Select Feedback
EBU:DQ(0)	to	P24.14:HWOUT(0)	Data Line
EBU:DQ(1)	to	P24.12:HWOUT(0)	Data Line
EBU:DQ(2)	to	P24.13:HWOUT(0)	Data Line
EBU:DQ(3)	to	P24.11:HWOUT(0)	Data Line
EBU:DQ(4)	to	P24.10:HWOUT(0)	Data Line
EBU:DQ(5)	to	P24.6:HWOUT(0)	Data Line
EBU:DQ(6)	to	P24.9:HWOUT(0)	Data Line
EBU:DQ(7)	to	P24.15:HWOUT(0)	Data Line
EBU:DQ(8)	to	P24.7:HWOUT(0)	Data Line
EBU:DQ(9)	to	P24.4:HWOUT(0)	Data Line
EBU:DQ(10)	to	P24.8:HWOUT(0)	Data Line
EBU:DQ(11)	to	P24.0:HWOUT(0)	Data Line
EBU:DQ(12)	to	P24.5:HWOUT(0)	Data Line
EBU:DQ(13)	to	P24.3:HWOUT(0)	Data Line
EBU:DQ(14)	to	P24.2:HWOUT(0)	Data Line
EBU:DQ(15)	to	P24.1:HWOUT(0)	Data Line
EBU:DQM(0)	to	P25.4:HWOUT(0)	SDRAM Write Data Valid
EBU:DQM(1)	to	P25.3:HWOUT(0)	SDRAM Write Data Valid
EBU:HOLDA	to	P25.3:HWOUT(0)	Hold Acknowledge
EBU:RD	to	P25.1:HWOUT(0)	Read Control
EBU:RD_FDBK	from	P25.1:IN	Read Feedback
EBU:SDCLKO	to	P25.0:HWOUT(0)	SDRAM Clock Output
EBU:WAIT	from	P25.6:IN	Wait Input
EBU:WR	to	P25.2:HWOUT(0)	Write Control
EBU:WR_FDBK	from	P25.2:IN	Write Feedback

**Table 468 List of EBU0 Interface Signals**

<b>Interface Signals</b>	<b>I/O</b>	<b>Description</b>
sx_sri		<b>sri slave interface</b>
		<b>Access to external memory via non-cached address range</b>
		<b>Access to External Memory via cached address range</b>

**External Bus Unit (EBU)****Table 468 List of EBU0 Interface Signals (cont'd)**

<b>Interface Signals</b>	<b>I/O</b>	<b>Description</b>
ADV_FDBK	in	<b>ADV Control Signal Feedback</b>
ADV	out	<b>Address Valid Control Signal</b>
HOLD	in	<b>EBU Arbitration</b>
SDCLKI	in	<b>SDRAM Clock Feedback</b>
BFCLKI	in	<b>Burst Flash Clock Feedback</b>
CKE	out	<b>SDRAM Clock Enable</b>
AD_IN(31:0)	in	<b>Data Bus Input</b>
AD(31:0)	out	<b>Data Bus Output</b>
A_IN(15:0)	in	<b>Address Input</b>
SDRAMA(13:0)	out	<b>SDRAM Address Bus</b>
RD	out	<b>Read Control</b>
RD_FDBK	in	<b>Read Feedback</b>
WR	out	<b>Write Control</b>
WR_FDBK	in	<b>Write Feedback</b>
BC(3:0)	out	<b>Byte Control</b>
CS_FDBK(2:0)	in	<b>Chip Select Feedback</b>
WAIT	in	<b>Wait Input</b>
BAA	out	<b>Burst Address Advance</b>
BA(1:0)	out	<b>Bank Address</b>
BFCLKO	out	<b>Burst Flash Clock Output</b>
SDCLKO	out	<b>SDRAM Clock Output</b>
CS(2:0)	out	<b>Chip Select</b>
HOLDA	out	<b>Hold Acknowledge</b>
DQM(1:0)	out	<b>SDRAM Write Data Valid</b>
BREQ	out	<b>Bus Request</b>
DQ(15:0)	out	<b>Data Line</b>
A(23:0)	out	<b>Address Output</b>

**43.5 Revision History****Table 469 Revision History**

<b>Reference</b>	<b>Change to Previous Version</b>	<b>Comment</b>
<b>V4.0.10</b>		
<a href="#">Page 1</a>	Non-cached/cached exchanged in register address space table.	-
<a href="#">Page 1</a>	Wrong write access mode “BE” for register CLC removed in register overview table.	
<b>V4.0.11</b>		
-	File regenerated. No functional changes	-

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**External Bus Unit (EBU)****Table 469 Revision History**

Reference	Change to Previous Version	Comment
<b>V4.0.12</b>		
-	No functional changes.	-

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**SD- and eMMC Interface (SDMMC)****44 SD- and eMMC Interface (SDMMC)**

This chapter describes the SDMMC.

**SD- and eMMC Interface (SDMMC)****44.1 TC39x-B Specific Register Set****Register Address Space Table****Table 470 Register Address Space - SDMMC**

Module	Base Address	End Address	Note
SDMMCO	F02B0000 <sub>H</sub>	F02B0FFF <sub>H</sub>	FPI slave interface

**Register Overview Table**

There are no product specific register for this module.

**44.2 TC39x-B Specific Registers**

There are no product specific register for this module.

**44.3 Connectivity****Table 471 Connections of SDMMCO**

Interface Signals	connects		Description
SDMMCO:CLK	to	P15.1:ALT(7)	card clock
SDMMCO:CMD	to	P15.3:HWOUT(0)	command out
SDMMCO:CMD_IN	from	P15.3:IN	command in
SDMMCO:DAT(0)	to	P20.7:HWOUT(0)	write data out
SDMMCO:DAT(1)	to	P20.8:HWOUT(0)	write data out
SDMMCO:DAT(2)	to	P20.10:HWOUT(0)	write data out
SDMMCO:DAT(3)	to	P20.11:HWOUT(0)	write data out
SDMMCO:DAT(4)	to	P20.12:HWOUT(0)	write data out
SDMMCO:DAT(5)	to	P20.13:HWOUT(0)	write data out
SDMMCO:DAT(6)	to	P20.14:HWOUT(0)	write data out
SDMMCO:DAT(7)	to	P15.0:HWOUT(0)	write data out
SDMMCO:DAT0_IN	from	P20.7:IN	read data in
SDMMCO:DAT1_IN	from	P20.8:IN	read data in
SDMMCO:DAT2_IN	from	P20.10:IN	read data in
SDMMCO:DAT3_IN	from	P20.11:IN	read data in
SDMMCO:DAT4_IN	from	P20.12:IN	read data in
SDMMCO:DAT5_IN	from	P20.13:IN	read data in
SDMMCO:DAT6_IN	from	P20.14:IN	read data in
SDMMCO:DAT7_IN	from	P15.0:IN	read data in

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**SD- and eMMC Interface (SDMMC)****44.4 Revision History****Table 472 Revision History**

Reference	Change to Previous Version	Comment
<b>V1.0.17</b>		
-	No functional changes.	
<b>V1.0.18</b>		
-	No functional changes.	

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**Hardware Security Module (HSM)**

## 45      **Hardware Security Module (HSM)**

The HSM is a separate processor subsystem dedicated for security tasks. It is connected as master and slave to the SPB bus.

For security reasons this module is described in a separate documentation. Please contact your Infineon representative for further information.

**Input Output Monitor (IOM)****46 Input Output Monitor (IOM)**

This document describes the IOM specific appendix for the product TC39x-B.

**46.1 TC39x-B Specific IP Configuration****Table 473 TC39x-B specific configuration of IOM**

Parameter	IOM
<b>Number of FPC channels</b>	16
<b>Number of GTM inputs</b>	8
<b>Number of LAM</b>	16
<b>Number of ECM</b>	1

**46.2 TC39x-B Specific Register Set****Register Address Space Table****Table 474 Register Address Space - IOM**

Module	Base Address	End Address	Note
IOM	F0035000 <sub>H</sub>	F00351FF <sub>H</sub>	FPI slave interface

**Register Overview Table**

There are no product specific register for this module.

**46.3 TC39x-B Specific Registers**

There are no product specific register for this module.

**46.4 Connectivity**

This section describes the connectivity of the IOMmodule.

**Table 475 Connections of IOM**

Interface Signals	connects	Description
IOM:GTM(7:0)	from GTM:TOUT(29:22)	GTM-provided inputs to EXOR combiner
IOM:MON1(0)	from CCU60:CC62	Monitor input 1
IOM:MON1(1)	from CCU60:CC61	Monitor input 1
IOM:MON0(12:0)	from GTM:TOUT(34:22)	Monitor input 0
IOM:MON1(2)	from CCU60:CC60	Monitor input 1
IOM:MON1(3)	from CCU60:COUT60	Monitor input 1
IOM:MON1(4)	from CCU60:COUT61	Monitor input 1
IOM:MON0(15:13)	from GTM:TOUT(70:68)	Monitor input 0
IOM:MON1(5)	from CCU60:COUT62	Monitor input 1

**Input Output Monitor (IOM)****Table 475 Connections of IOM (cont'd)**

<b>Interface Signals</b>	<b>connects</b>	<b>Description</b>
IOM:MON1(6)	from CCU60:COUT63	Monitor input 1
IOM:MON1(7)	from CCU61:COUT63	Monitor input 1
IOM:MON1(8)	from CCU61:CC60	Monitor input 1
IOM:MON1(9)	from CCU61:CC61	Monitor input 1
IOM:MON2(0)	from QSPI0:MRST	Monitor input 2
IOM:MON2(1)	from QSPI1:MRST	Monitor input 2
IOM:MON2(2)	from QSPI2:MRST	Monitor input 2
IOM:MON2(3)	from QSPI3:MRST	Monitor input 2
IOM:MON2(4)	from QSPI4:MRST	Monitor input 2
IOM:MON2(5)	from CAN00:TXD	Monitor input 2
IOM:MON2(6)	from CAN01:TXD	Monitor input 2
IOM:MON2(7)	from CAN02:TXD	Monitor input 2
IOM:MON2(8)	from CAN03:TXD	Monitor input 2
IOM:MON1(10)	from CCU61:CC62	Monitor input 1
IOM:MON1(11)	from CCU61:COUT60	Monitor input 1
IOM:MON1(12)	from CCU61:COUT61	Monitor input 1
IOM:MON1(13)	from CCU61:COUT62	Monitor input 1
IOM:MON1(15:14)	from PSI5:TX(1:0)	Monitor input 1
IOM:MON2(11:9)	from GTM:TOUT(106:104)	Monitor input 2
IOM:MON2(12)	from ASCLIN0:ATX ASCLIN0:ATXP	Monitor input 2
IOM:MON2(13)	from ASCLIN1:ATX ASCLIN1:ATXP	Monitor input 2
IOM:MON2(14)	from ASCLIN2:ATX ASCLIN2:ATXP	Monitor input 2
IOM:MON2(15)	from ASCLIN3:ATX ASCLIN3:ATXP	Monitor input 2
IOM:PIN(0)	from P33.0:IN	GPIO pad input to FPC
IOM:PIN(1)	from P33.1:IN	GPIO pad input to FPC
IOM:PIN(2)	from P33.2:IN	GPIO pad input to FPC
IOM:PIN(3)	from P33.3:IN	GPIO pad input to FPC
IOM:PIN(4)	from P33.4:IN	GPIO pad input to FPC
IOM:PIN(5)	from P33.5:IN	GPIO pad input to FPC
IOM:PIN(6)	from P33.6:IN	GPIO pad input to FPC
IOM:PIN(7)	from P33.7:IN	GPIO pad input to FPC
IOM:PIN(8)	from P33.8:IN	GPIO pad input to FPC
IOM:PIN(9)	from P33.9:IN	GPIO pad input to FPC
IOM:PIN(10)	from P33.10:IN	GPIO pad input to FPC
IOM:PIN(11)	from P33.11:IN	GPIO pad input to FPC

**Input Output Monitor (IOM)****Table 475 Connections of IOM (cont'd)**

<b>Interface Signals</b>	<b>connects</b>		<b>Description</b>
IOM:PIN(12)	from	P33.12:IN	GPIO pad input to FPC
IOM:PIN(13)	from	P20.12:IN	GPIO pad input to FPC
IOM:PIN(14)	from	P20.13:IN	GPIO pad input to FPC
IOM:PIN(15)	from	P20.14:IN	GPIO pad input to FPC
IOM:REF1(0)	from	CCU60:COUT63	Reference input 1
IOM:REF1(1)	from	CCU60:COUT62	Reference input 1
IOM:REF1(2)	from	CCU60:COUT61	Reference input 1
IOM:REF1(3)	from	CCU60:COUT60	Reference input 1
IOM:REF1(4)	from	CCU60:CC62	Reference input 1
IOM:REF0(15:0)	from	GTM:TOUT(15:0)	Reference input 0
IOM:REF1(5)	from	CCU60:CC61	Reference input 1
IOM:REF1(6)	from	CCU60:CC60	Reference input 1
IOM:REF1(7)	from	CCU61:COUT63	Reference input 1
IOM:REF1(8)	from	CCU61:COUT62	Reference input 1
IOM:REF1(9)	from	CCU61:COUT61	Reference input 1
IOM:REF2(0)	from	QSPI0:MRST	Reference input 2
IOM:REF2(1)	from	QSPI1:MRST	Reference input 2
IOM:REF2(2)	from	QSPI2:MRST	Reference input 2
IOM:REF2(3)	from	QSPI3:MRST	Reference input 2
IOM:REF2(4)	from	QSPI4:MRST	Reference input 2
IOM:REF2(5)	from	CAN00:TXD	Reference input 2
IOM:REF2(6)	from	CAN01:TXD	Reference input 2
IOM:REF2(7)	from	CAN02:TXD	Reference input 2
IOM:REF2(8)	from	CAN03:TXD	Reference input 2
IOM:REF1(10)	from	CCU61:COUT60	Reference input 1
IOM:REF1(11)	from	CCU61:CC62	Reference input 1
IOM:REF1(12)	from	CCU61:CC61	Reference input 1
IOM:REF1(13)	from	CCU61:CC60	Reference input 1
IOM:REF1(14)	from	PSI5:TX(0)	Reference input 1
IOM:REF1(15)	from	PSI5:TX(2)	Reference input 1
IOM:REF2(11:9)	from	GTM:TOUT(109:107)	Reference input 2
IOM:REF2(12)	from	ASCLIN0:ATX ASCLIN0:ATXP	Reference input 2
IOM:REF2(13)	from	ASCLIN1:ATX ASCLIN1:ATXP	Reference input 2
IOM:REF2(14)	from	ASCLIN2:ATX ASCLIN2:ATXP	Reference input 2
IOM:REF2(15)	from	ASCLIN3:ATX ASCLIN3:ATXP	Reference input 2

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**Input Output Monitor (IOM)****46.5 Revision History****Table 476 Revision History**

Reference	Change to Previous Version	Comment
V2.1.15		
	No changes.	

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**8-Bit Standby Controller (SCR)****47        8-Bit Standby Controller (SCR)**

The description of the SCR for all devices is covered by the family specification.

## Revision history

Document version	Date of release	Description of changes
V2.0.0	2021-02	<ul style="list-style-type: none"> <li>Version comparison table updated.</li> <li>For further changes see respective revision history of each chapter. The version comparison table below gives an overview.</li> </ul>
V1.6.0	2020-08	<ul style="list-style-type: none"> <li>Version comparison table updated.</li> <li>For further changes see respective revision history of each chapter. The version comparison table below gives an overview.</li> <li>Removed device TC3Ax from set of documentation.</li> </ul>
V1.5.0	2020-04	<ul style="list-style-type: none"> <li>Version comparison table updated.</li> <li>For further changes see respective revision history of each chapter. The version comparison table below gives an overview.</li> </ul>
V1.4.0	2019-12	<ul style="list-style-type: none"> <li>Added TC3Ax appendix as target specification.</li> <li>Version comparison table updated.</li> <li>For further changes see respective revision history of each chapter. The version comparison table below gives an overview.</li> </ul>
V1.3.0	2019-09	<ul style="list-style-type: none"> <li>Added additional device TC3Ax to AURIX™ TC3xx set of documentation.</li> <li>Version comparison table updated.</li> <li>For further changes see respective revision history of each chapter. The version comparison table below gives an overview.</li> </ul>
V1.2.0	2019-04	<ul style="list-style-type: none"> <li>Added additional device TC3Ex to AURIX™ TC3xx set of documentation.</li> <li>Version comparison table updated.</li> <li>For further changes see respective revision history of each chapter. The version comparison table below gives an overview.</li> </ul>
V1.1.0	2019-01	<ul style="list-style-type: none"> <li>Power Management System for Low-End (PMSLE) added.</li> <li>TC33x and TC33xED added.</li> <li>Changes in connectivity tables.</li> <li>Version comparison table new.</li> <li>Detailed Revision History contained in each chapter.</li> </ul>
V1.0.0	2018-08	<ul style="list-style-type: none"> <li>First revision of the User's Manual.</li> <li>Detailed OCDS information not contained. Available under NDA.</li> <li>Detailed Revision History contained in each chapter.</li> </ul>

### Version comparison table for AURIX™ TC39x-B appendix

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
Introduction	V1.0.0	V1.0.0	No
MEMMAP	V0.1.20	V0.1.21	<b>Yes, see chapter revision history</b>
FW	V1.1.0.1.17	V1.1.0.1.18	No functional changes
SRI Fabric	V1.1.16	V1.1.17	No functional changes

<b>Chapter name</b>	<b>UM V1.6.0 chapter version</b>	<b>UM V2.0.0 chapter version</b>	<b>Content changes</b>
• SBCU, EBCU	V1.2.8	V1.2.9	<b>Yes, see chapter revision history</b>
CPU	V1.1.20	V1.1.21	No functional changes
NVM Subsystem	V2.0.7	V2.0.7	No
• DMU	V2.0.11	V2.0.12	No functional changes
• NVM	V2.0.6	V2.0.6	No
LMU	V3.1.16	V3.1.16	No
DAM	V1.3.11	V1.3.12	No functional changes
SCU	V2.1.26	V2.1.27	No functional changes
CCU	see SCU	see SCU	–
PMS	V2.2.33	V2.2.34	No functional changes
PMSLE	n/a	n/a	–
MTU	V7.4.12	V7.4.13	<b>Yes, see chapter revision history</b>
PORTS	V1.8.21	V1.8.21	No
SMU	V4.0.22	V4.0.23	<b>Yes, see chapter revision history</b>
INT	V1.2.11	V1.2.11	<b>No</b>
FCE	V4.2.9	V4.2.9	No
DMA	V0.1.18	V0.1.18	No
SPU	V1.1.24	V1.1.25	No functional changes
SPU2	n/a	n/a	Chapter removed due to TC3Ax discontinuation.
BITMGR	n/a	n/a	Chapter removed due to TC3Ax discontinuation.
SPULCKSTP	V1.2.5	V1.2.5	No
EMEM	V1.4.4	V1.4.4	No
RIF	V1.0.40	V1.0.43	<b>Yes, see chapter revision history</b>
HSPDM	V0.7.9	V0.7.9	No
CIF	n/a	n/a	–
STM	V9.2.4	V9.2.4	No
GTM	V2.2.23	V2.2.24	Yes, see chapter revision history
CCU6	V3.0.0	V3.0.0	No
GPT12	V3.0.2	V3.0.2	No
CONVCTRL	V3.0.1	V3.0.1	No
EVADC	V3.0.4	V3.0.5	No functional changes
EDSADC	V3.0.5	V3.0.6	No functional changes
I2C	V2.3.6	V2.3.6	No
HSSL	V3.0.18	V3.0.19	No functional changes
• HSCT	V2.3.15	V2.3.15	No
ASCLIN	V3.2.8	V3.2.8	No

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
QSPI	V3.0.20	V3.0.20	No
MSC	V5.0.10	V5.0.10	No
SENT	V2.1.10	V2.1.10	No
MCMCAN	V1.19.13	V1.19.13	No
E-Ray	V3.2.10	V3.2.11	No functional changes
PSI5	V1.17.12	V1.17.12	No
PSI5-S	V1.12.10	V1.12.10	No
GETH	V1.3.14	V1.3.15	No functional changes
EBU	V4.0.12	V4.0.12	No
SDMMC	V1.0.18	V1.0.18	No
HSM	V2.3.9	V2.3.9	No
IOM	V2.1.15	V2.1.15	No
SCR	n/a	n/a	-

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