AURIX 2G EDSADC

Enhanced Delta-Sigma Analog-to-Digital Converter

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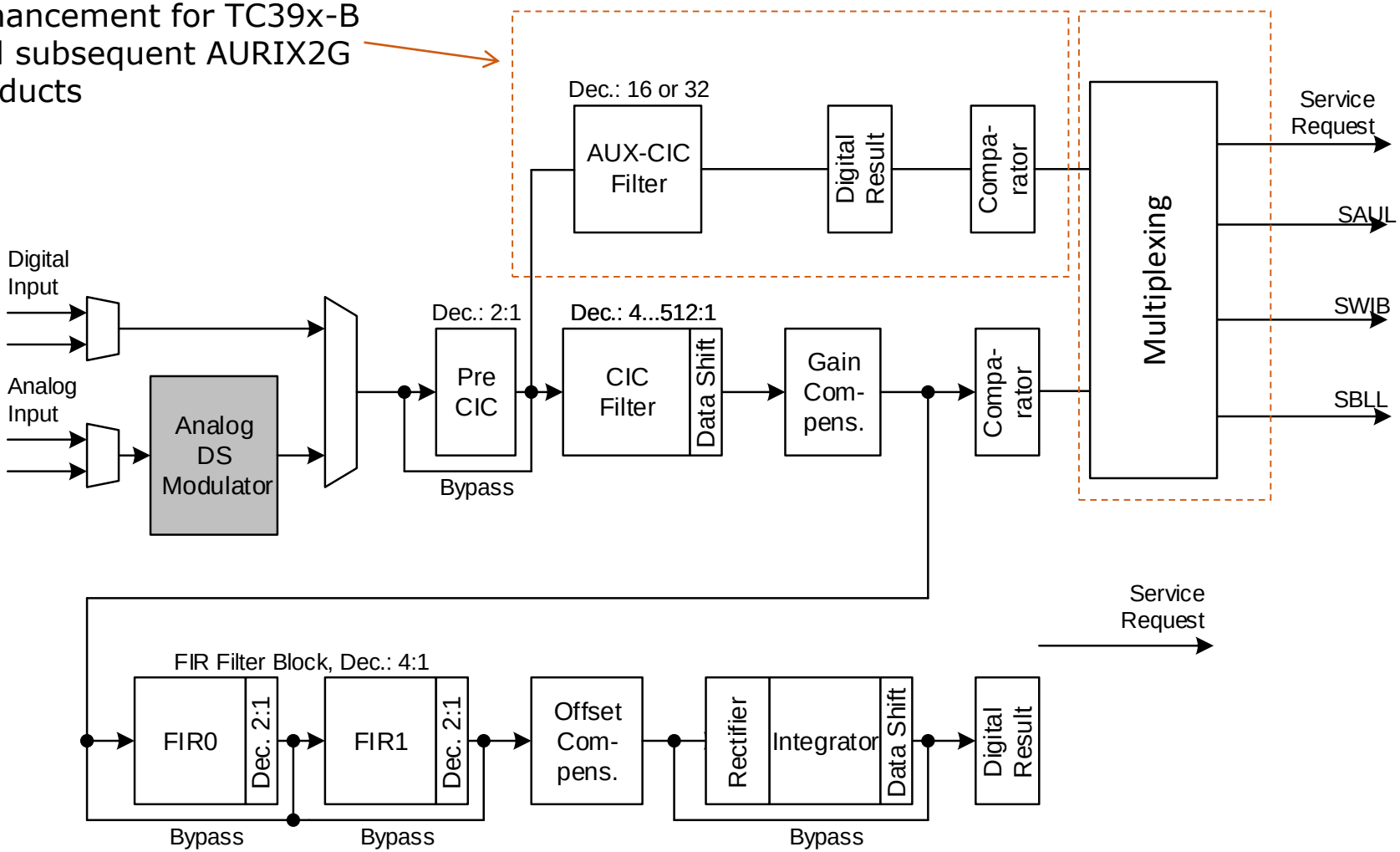
2018/5/2

AURIX™ - TC3xx
Basic Architecture – Modulator & Demodulator Chain

Enhancement for TC39x-B and subsequent AURIX2G products



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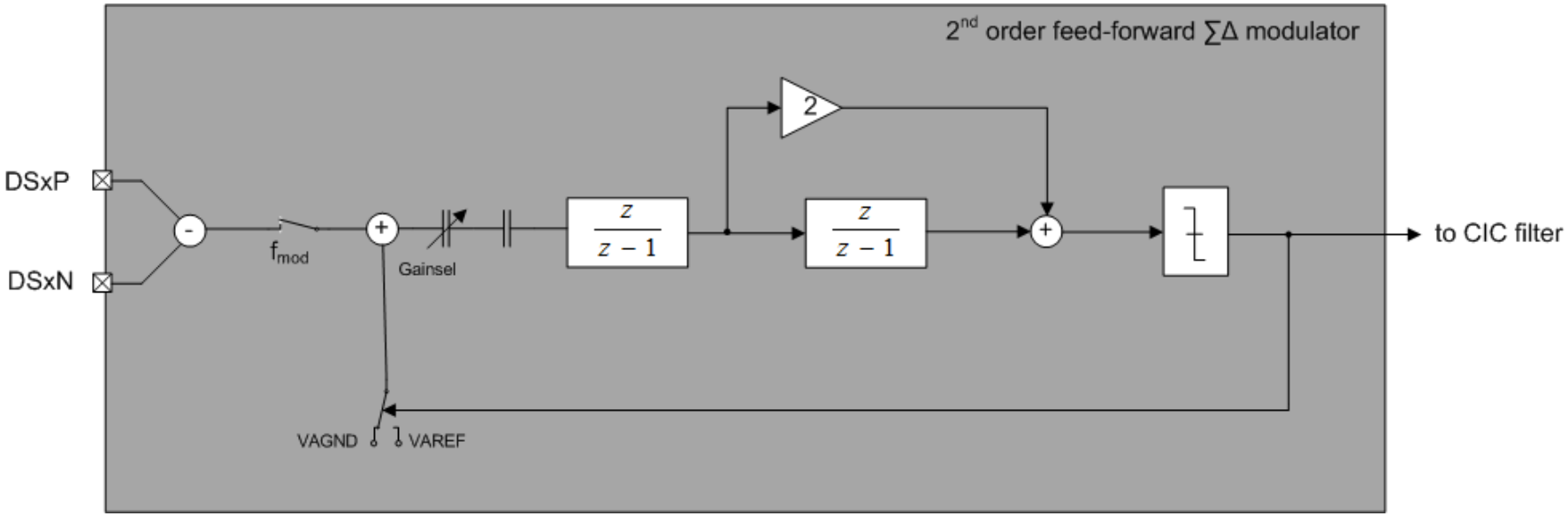
AURIX™ - TC3xx
EDSADC - 2nd order Single-Bit Feed-forward DS Modulator



- 2nd order architecture offers following benefits
  - Dead zone below required noise level
  - No explicit counter measures to remove idle tones (DC analog input signals)
  - No significant overload recovery time (<< 1µs)
  - Improved converter linearity (SFDR/THD)
  - No time continuous input buffer
    - No DC input current
  - Common mode voltage and common mode hold voltage can be disabled for single-ended measurements

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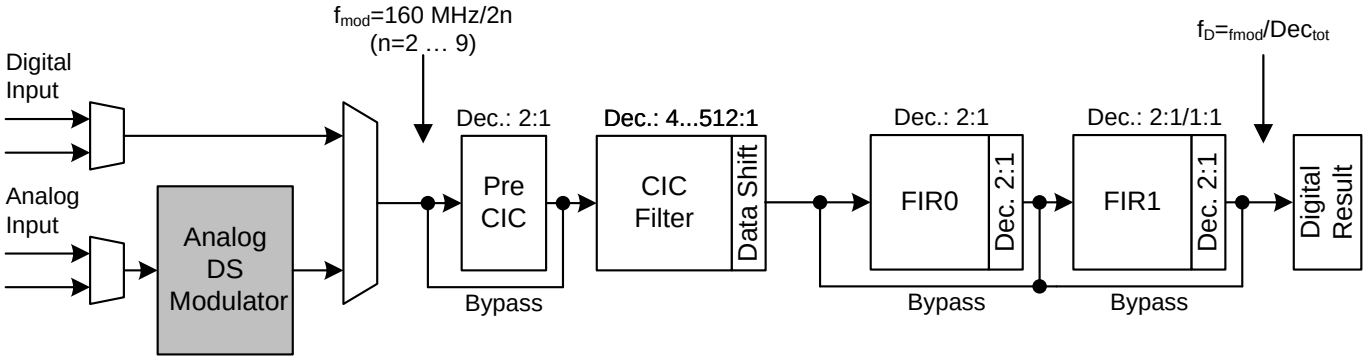
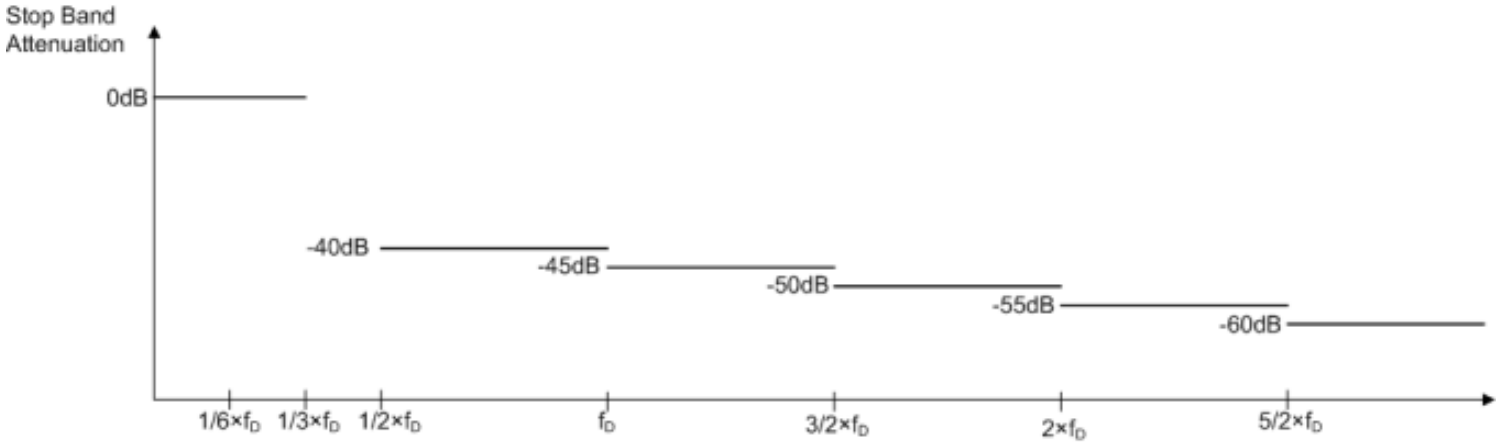
AURIX™ - TC3xx
EDSADC - Characteristics of digital Filter Chain

› Filter chain elements to control the frequency response:

$$DEC_{tot} = DEC_{pre-CIC} \cdot DEC_{CIC} \cdot DEC_{FIR0} \cdot DEC_{FIR1}$$



› Frequency response of digital filter chain:



› The pass-band frequency (f_{PB})of the digital filter chain is related to the configured output sample rate (f_D)

› The relation between pass-band frequency (f_{PB}) and output data rate (f_D)is dependent on the decimation of FIR1

- Dec_{FIR1}=2: $f_{PB}=f_D/3$
- Dec_{FIR1}=1: $f_{PB}=f_D/6$

› The stop band attenuation of the filter chain is given by the non-configurable coefficients of the FIR0 and FIR1

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AURIX™ - TC3xx
EDSADC - Operating Ranges

Modulator Frequency (f_{mod})	Input Current (I_{RMS})	f_{PB} < 10KHz		f_{PB} ≤ 30KHz		f_{PB} ≤ 50KHz		f_{PB} ≤ 100KHz	
		SNR	OSR	SNR	OSR	SNR	OSR	SNR	OSR
f_{mod}= 16MHz	6µA	≥80dB	≥267	≥80dB	≥178	≥78dB	≥107	≥71dB[2]	≥54
f_{mod}= 20MHz	7.5µA	≥80dB	≥334	≥80dB	≥222	≥78dB	≥134	≥71dB[2]	≥66
f_{mod}= 26.67MHz	10µA	≥80dB	≥445	≥80dB	≥297	≥80dB	≥178	≥74dB	≥88
f_{mod}= 40MHz	15µA	≥80dB	≥666	≥80dB	≥445	≥80dB	≥267	≥78dB	≥134

- SNR values are valid for differential input signals and selected analog gain of one
  - The use of the analog gain stages 2 and 4 decreases in each case the SNR by 3dB
- The typical RMS input current of the modulator is related to 5V input voltage and to the typical value of the switched capacitor (C_{SW})
  - $I_{RMS} = 5V \cdot f_{mod} \cdot 2 \cdot C_{sw}$
  - For gain stage 2 and 4, the RMS input current increases accordantly
- [2)]Quantization noise limits the signal to noise ratio (SNR)

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AURIX™ - TC3xx
EDSADC - Modulator Power Reduction

The power reduction mode is determined by bitfield **MODCFGx** (x=0-13).

- APC=00B: **Normal Operation**.
- APC=01B: **Slow Standby mode**
- APC=10B: **Fast Standby mode**

Field	Bits	Type	Description
APC	29:28	rw	**Automatic Power Control** 00_B Off: Modulator active while its associated bit MxRUN is set 01_B Slow standby mode on-chip modulator and voltage regulator are deactivated, external modulator clock is disabled, while the gate signal (selected trigger) is inactive 10_B Fast standby mode:on-chip modulator is deactivated, external modulator clock is disabled, while the gate signal (selected trigger) is inactive 11_B Reserved

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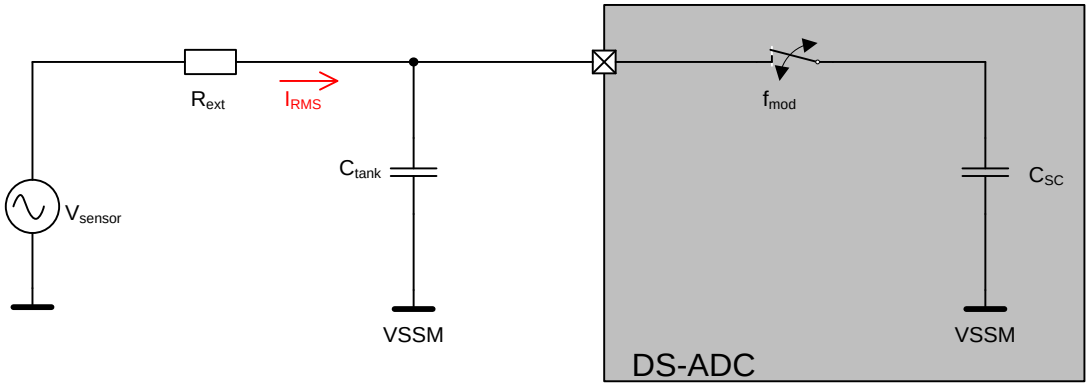
AURIX™ - TC3xx
EDSADC - Equivalent Input Impedance

› Equivalent input impedance:

Gain	C_{SC} [fF]	f_{mod} [MHz]	R_{in} [kΩ]
1	37.5	16	833
2	75	16	416
4	150	16	208
1	37.5	26.67	500
2	75	26.67	250
4	150	26.67	125

› Charged based equivalent model of DS-ADC (single-ended)



$$I_{RMS} = 2 \times C_{SC} \times f_{mod} \times V_{sensor}$$

$$R_{in} = V_{sensor} / I_{RMS}$$

$$R_{in} = 1 / (2 \times C_{SC} \times f_{mod})$$

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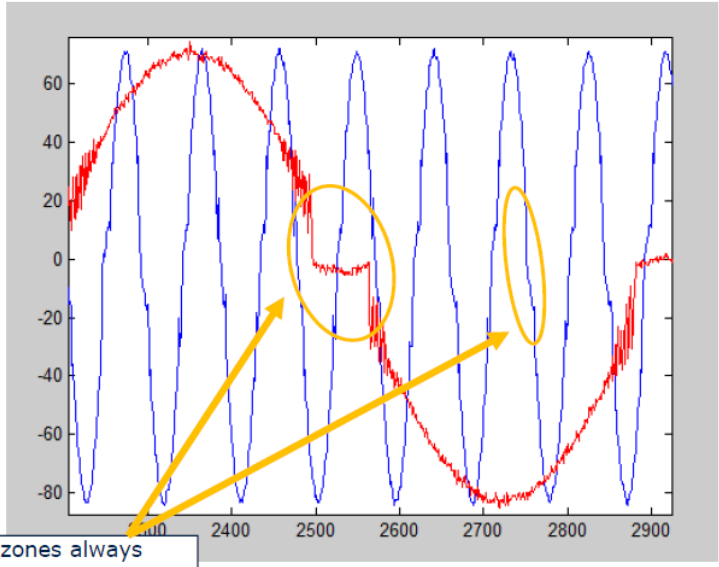
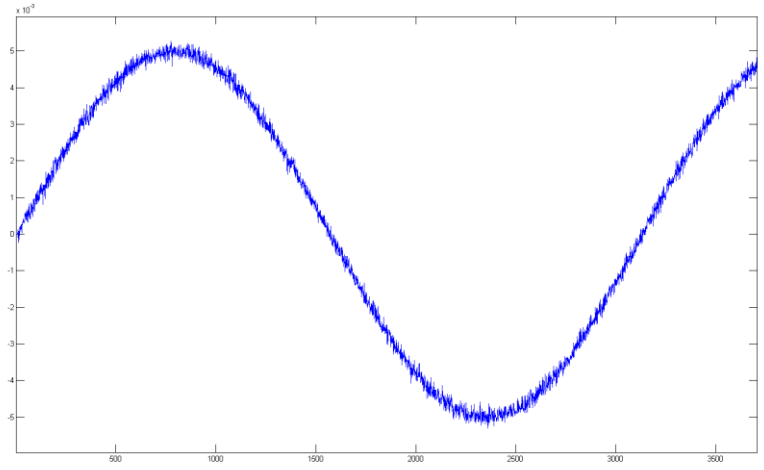
AURIX™ - TC3xx
EDSADC - Dead Zone behavior(TC275 versus TC39x-A)

› Analog input signal: sinus with 100Hz and 50mVpp



› AURIX Device3-BB:
MASH 1-1-1 modulator



› AURIX2G TC39x-A:
2nd order Single-Bit Feed-forward DS Modulator

› **As expected, the dead zone of 2nd order single-bit feed-forward DS modulator is much below the required noise level**

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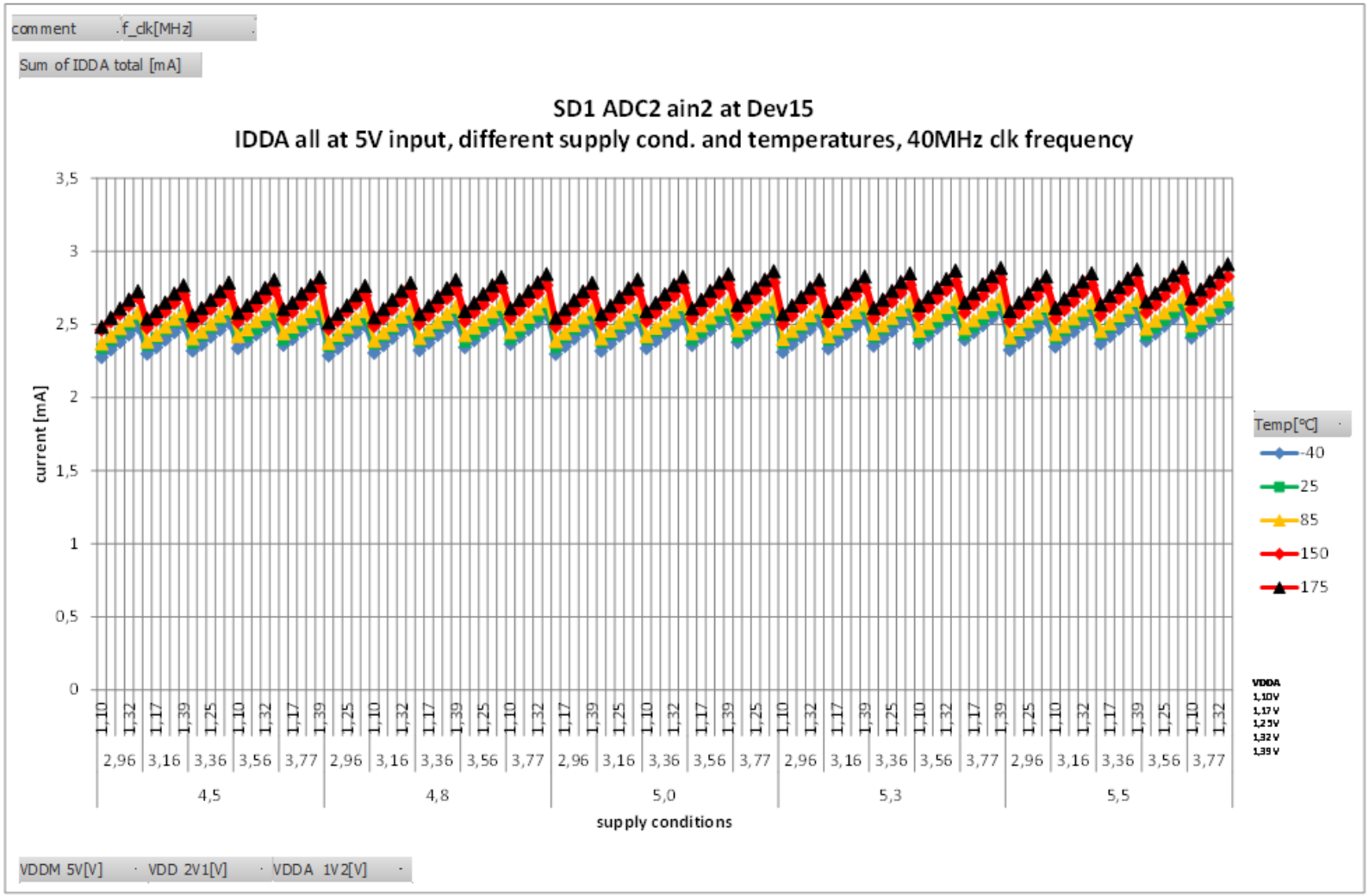
AURIX™ - TC3xx
EDSADC - Modulator Current Consumption



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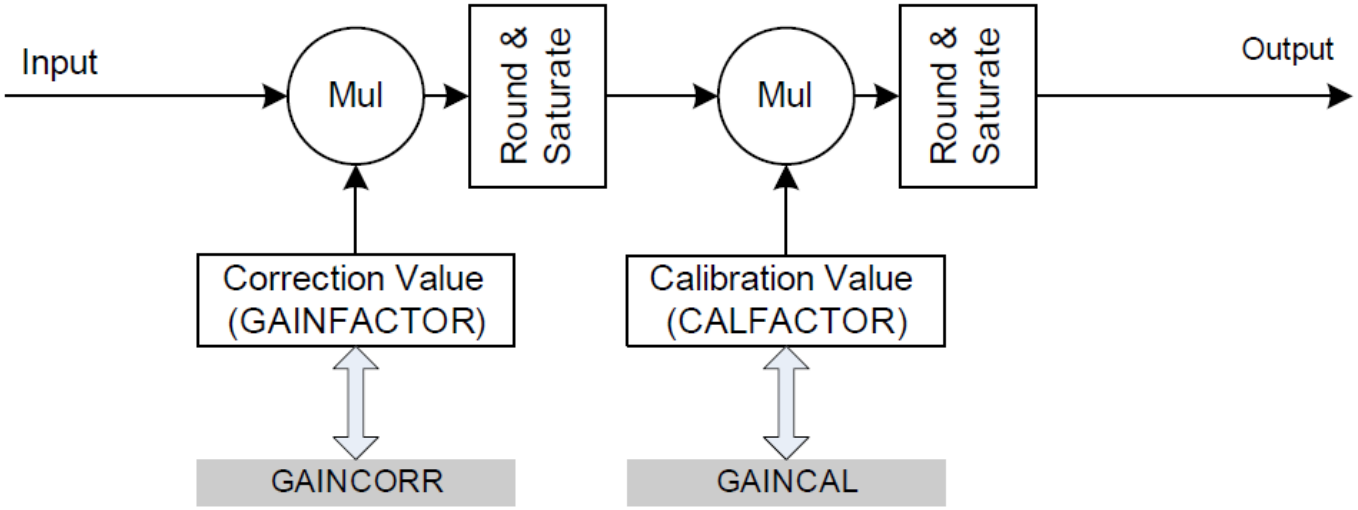
AURIX™ - TC3xx
EDSADC - Gain Calibration of DS-ADC

- Calibration concept of AURIX2G DS-ADC will not use any CPU load
  - User can start the gain calibration by setting of the related configuration bit
- Specific digital hardware multiplier will be integrated for gain calibration
- To minimize the execution time of the hardware calibration, only the digital CIC filter is enabled
- The FIR0, FIR1 filter and the integrator are disabled/bypassed automatically
- To find the tradeoff between calibration execution time and accuracy, the OSR of the CIC filter will be set to 32/64/128/256/512 automatically
- Target value after gain calibration is 25000



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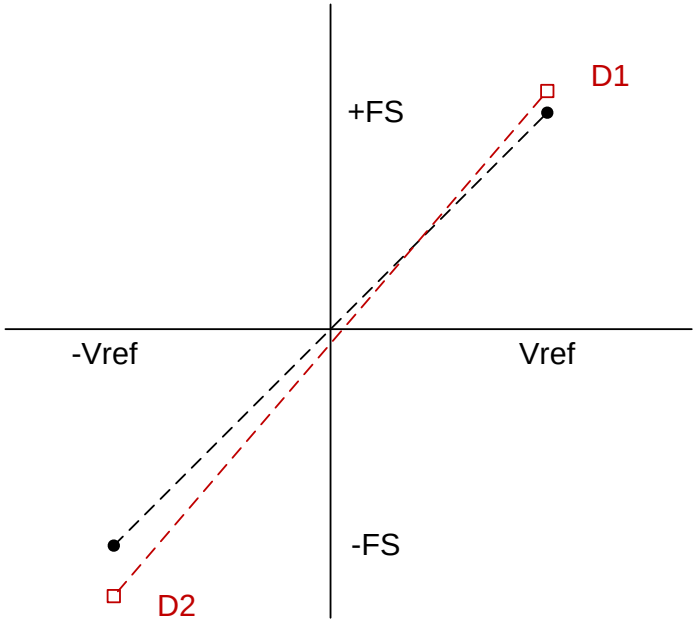
AURIX™ - TC3xx
EDSADC - Gain Calibration of DS-ADC

- An ideal DS-ADC would delivers a result range between ± digital full-scale (2xFS=25000)
- A real DS-ADC has an gain error and therefore the result range is between D1 and D2



- To calculate the gain error the digital full-scale range has to be compared with the real result range
  - GAIN= (D1 – D2)/(2xFS)
  - *(D1 – D2) is offset free !!*

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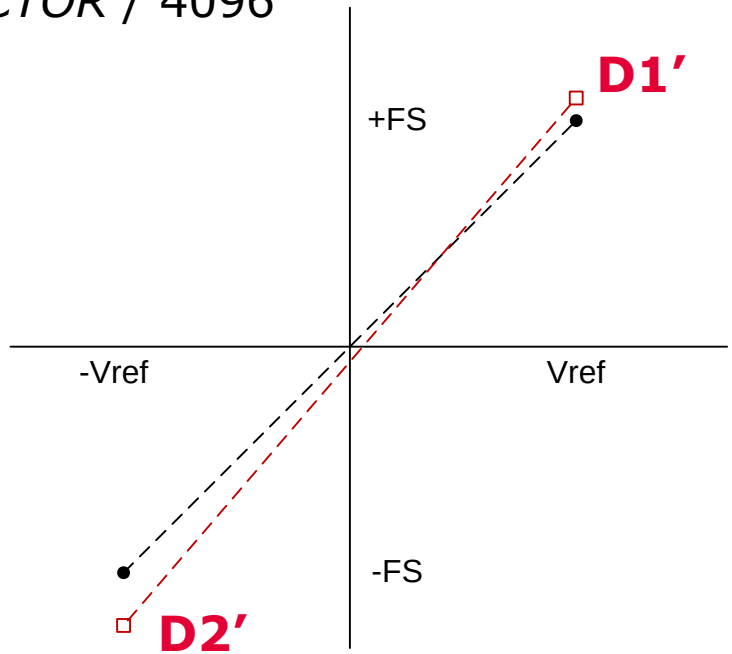
AURIX™ - TC3xx
EDSADC - Offset Calibration

- The offset will be corrected after the GAIN calibration
- The gain compensated result range has to be calculated after execution of gain calibration
  - D1’ = D1 x *CALFACTOR* / 4096
  - D2’ = D2 x *CALFACTOR* / 4096



- ***2xOffset_Correction = -(D1’ + D2’)***

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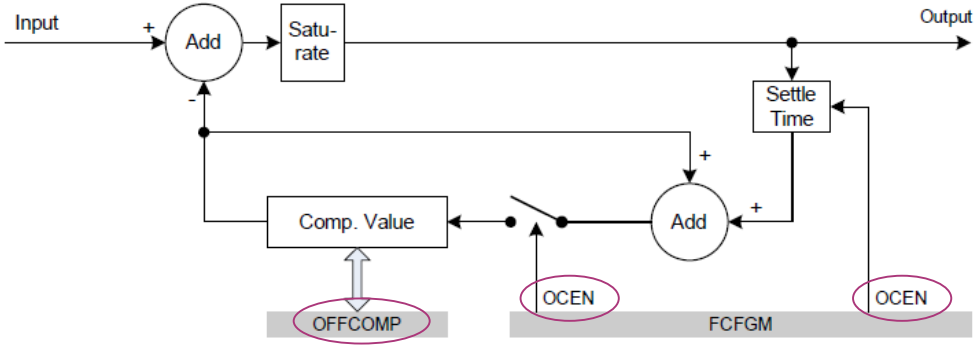
EDSADC - Offset Compensation Filter/High-Pass Filter

› Architecture of offset compensation filer/high-pass filter



› To cancel DC parts of differential analog input signals a digital 1st order high-pass filter is implemented

› In case of single ended measurements the high-pass filter has to be disabled ("OCEN")

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AURIX™ - TC3xx
EDSADC - Gain Calibration Procedure

- CALFACTOR = *4096* → multiplication by *1.0*
  - *granularity of ~1/4000 → better than 1/1000 (0.1%)*
- Use the GAINCAL multiplier to get the right constant
  - *CALFACTOR = 4096*
  - while *CALFACTOR x (D1-D2)* /4096 > 2 FS
    - *CALFACTOR = CALFACTOR -1*
  - while *CALFACTOR x (D1-D2)* /4096 < 2 FS
    - *CALFACTOR = CALFACTOR +1*

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EDSADC - Application Interaction of Input Characteristic

- To minimize the gain error of the complete signal path (sensor -> DS-ADC, a corresponding ***blocking capacitor*** (C_{tank}) at the input of the DS-ADC is needed
- The switched capacitor input characteristic of the DS-ADC creates a certain ***input current flow*** (I_{RMS}) from the sensor source into the DS-ADC
  - RMS current is dependent of modulator frequency and the value of DS-ADC internal switched capacitor load (C_{SC})
- This current creates an additional application specific gain error caused by the related voltage drop on the external protection resistor (R_{ext})
  - Application related gain error $=(1- (V_{sensor}-I_{RMS}\times R_{ext})/V_{sensor})$
- Input current of DS-ADC will be stored in UCB
  - In best case the temperature dependency of the input current is a second order effect
  - Has the temperature a significant impact of the input current the device specific values at CT, RT and HT will be stored in UCB
- The user can compensate the application related gain error by configuration of the DS-ADC internal scaling hardware multiplier (see slide 4)

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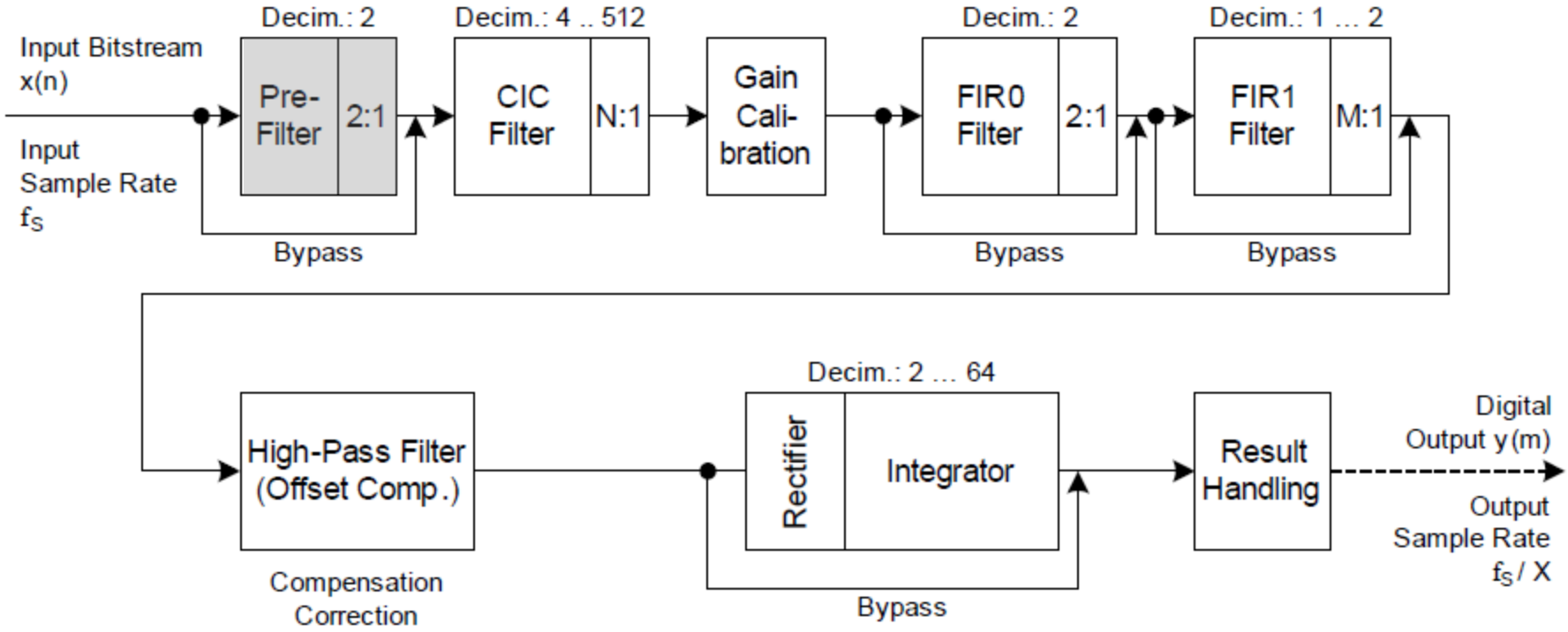
AURIX™ - TC3xx
EDSADC - Basic Architecture of digital Filter Chain



- To be backward compatible to AURIX, the Pre-Filter is only needed for a DS-Modulator frequency of 26.6MHz/40MHz
- To be backward compatible to AURIX, the Pre-Filter **should be bypassed** for a DS-Modulator frequency of **20MHz**

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AURIX™ - TC3xx
EDSADC - Overshoot Compensation for FIR filters

- Digital filters with a strong stop-band attenuation generate overshoots in case of very fast input signal changes like a step response
  - The overshoot limiter is located between CIC filter and FIR0 filter
- The overshoot will be limited based on a temporary non-linear slew rate limitation
  - IIR structure which engages only in the case where the difference of two input samples is higher than configured value (OVSCFG.SDTH)
- The deterministic group delay of the filter chain isn't change by the overshoot compensation

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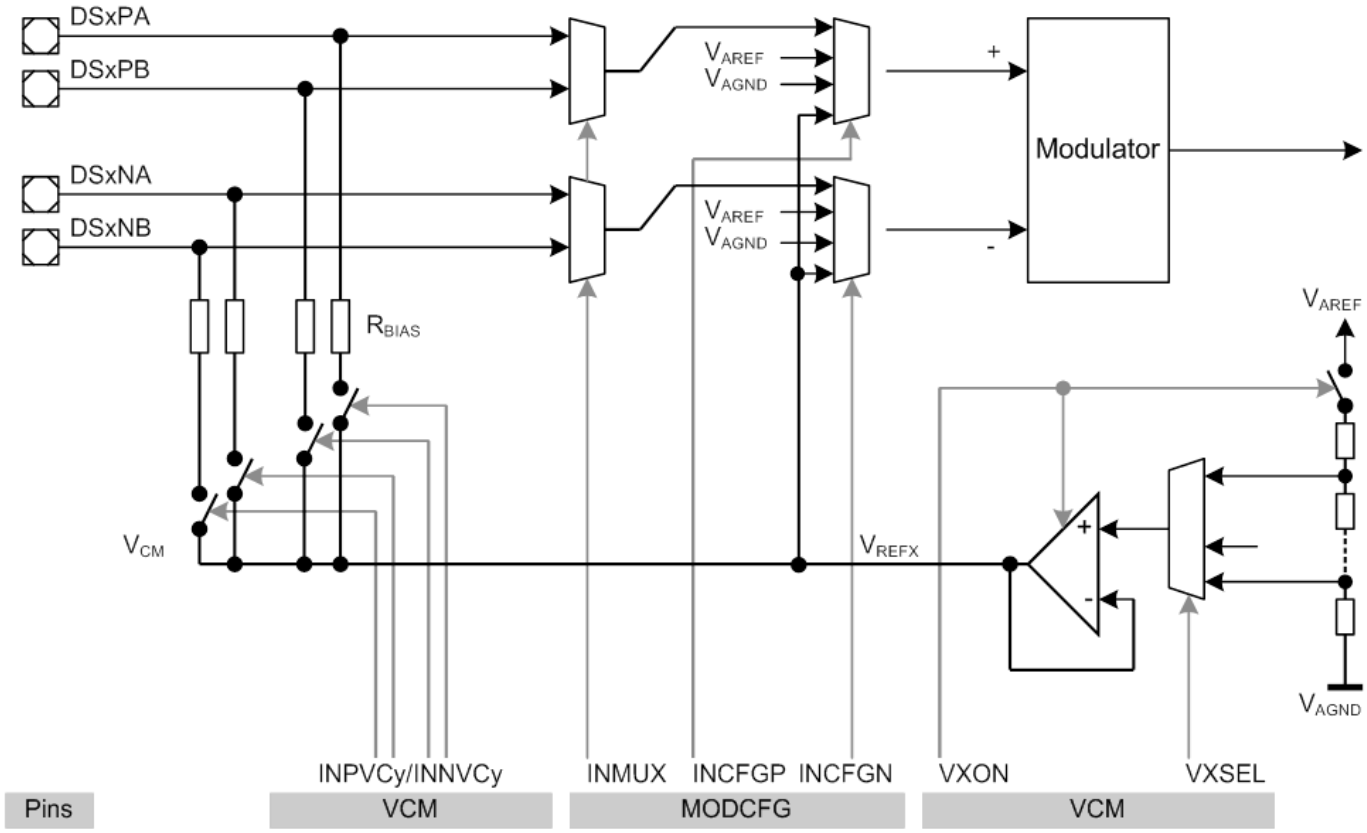
AURIX™ - TC3xx
EDSADC - Input topology of DS-ADC



- For single ended measurements the common mode voltage can be switched-off
- A central common mode voltage is used for analog input biasing and the modulator itself
  => No common mode hold voltage anymore

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EDSADC - Format Transfer of digital Result Register

- Due to the differential structure of the DS-modulator, the digital result register is coded with a 16-bit two's-complement format (sign-bit + 15 data-bits)
  - Sign-bit is stored into the MSB of the digital output register
- The output format can be changed into 16-bit unsigned format using RDM bit-field of the "DICFGx" configuration register
  - This configuration is only proposed for a single-ended measurement using quasi-differential mode
    - Negative/positive analog input of DS-Modulator is connected to the common mode voltage and DS-modulator gain setting 2 is configured
  - The unsigned configuration of the RDM bit-field added automatically 2^{15} to the output of the digital filter chain

Field	Bits	Type	Description
RDM	29	rw	**Result Display Mode** 0_B Signed: result values range from -2^{15} to $+2^{15}$ 1_B Unsigned: result values range from 0 to $+2^{16}$ (shifted by 2^{15})

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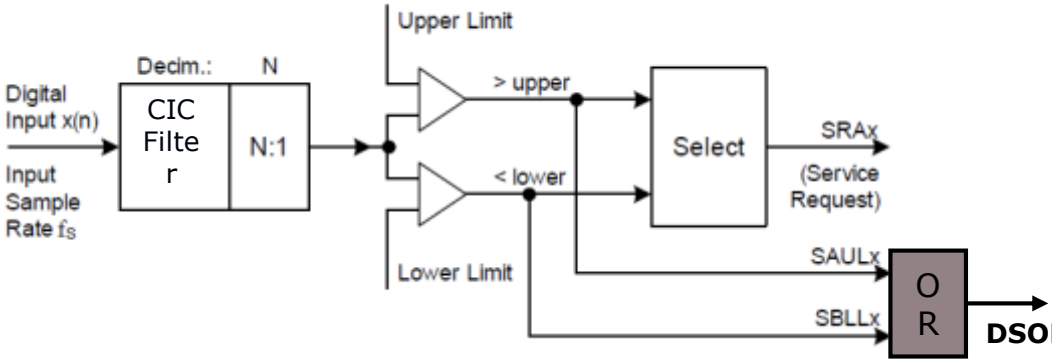
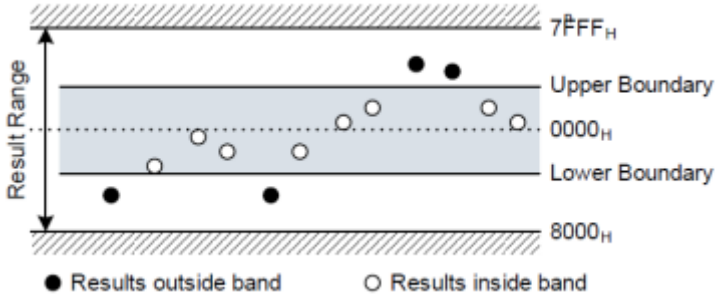
AURIX™ - TC3xx
EDSADC - Limit Checking

› Limit checking architecture



› Result Monitoring



can be connected to the DTM of GTM

- To minimize the group delay only the result of the digital decimation filter (CIC) is used for limit checking
- To supervise the reconstructed analog input signal an independent configurable upper limit and lower limit can be configured
- A service request can be generated in case of
  - Reconstructed analog input signal is inside the configured band
  - Reconstructed analog input signal is inside the configured band
  - Validation of reconstructed analog input signal is completed
- The range signals “SAULx” and “SBLLx” are generated independently from the service request configuration
  - The range signals are connected with the GTM

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EDSADC - Analog Multiplexer Setting within the Timestamp Register

- To provide the relationship of analog multiplexer position and the corresponding values of the digital result register, the currently used position of the analog multiplexer can be copied into the most recent captured timestamp value ("TIMESTAMP")
  - Bit-field "AMXCOPX" must be set to 1_B
  - Using this configuration the maximum size of the timestamp is limited to 14-bit
  - As long the integrator of the digital filter chain is not used the lowest time resolution ("TSCLK") for the timestamp counter can be used
    - In this case the maximum possible downsampling is 2^{10}
  - Together with the enabled integrator the maximum downsampling of the filter chain can be up to 2^{16}
    - In this case the resolution of the timestamp counter clock must be increased ("TSCLK")

TSTMPx (x = 0-13)
Time-Stamp Register x (x * 0100_H + 0150_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS VAL	0	0	0	0	0	0	0	0	0	0	0	0	0	AMX	
rh	r	r	r	r	r	r	r	r	r	r	r	r	r	rh	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP															
rh															

Field	Bits	Type	Description
TIMESTAMP	[15:0]	rh	**The Most Recent Captured Timestamp Value** This value is copied from the timestamp counter TSCOUNT *Note: If bit AMXCOPY in register TSCNTx (x = 0-13) is 1, bits TIMESTAMP[15:14] are replaced with a copy of bitfield AMX.*
AMX	[17:16]	rh	**Analog Multiplexer Setting** This value is copied from bitfield INMUX in register MODCFGx

TSCNTx (x=0-13)
Time-Stamp Counter x (x * 0100_H + 0154_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	AMX COPY	TSC RUN	0	TSCLK	
r	r	r	r	r	r	r	r	r	r	r	rw	rw	r	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCOUNT															
rh															

TSCLK	[17:16]	rw	**Timestamp Counter Clock Selection** 00_B $f_{TSTMP} = f_{MOD}$ 01_B $f_{TSTMP} = f_{MOD} / 2$ 10_B $f_{TSTMP} = f_{MOD} / 4$ 11_B $f_{TSTMP} = f_{MOD} / 8$
TSCRUN	18	rw	**Timestamp Counter Run Control** 0_B Timestamp counter is off 1_B Timestamp counter is counting at the rate selected by bitfield TSCLK
0	19	r	**Reserved, write 0, read as 0** No flipflop required.
AMXCOPY	20	rw	**Analog MUX Setting Copy Enable** Allows copying of bitfield AMX into bitfield TIMESTAMP (in register TSTMPx (x = 0-13)). 0_B Do not copy, timestamp uses all 16 bits 1_B Copy AMX to bits TIMESTAMP[15:14], timestamp uses lower 14 bits

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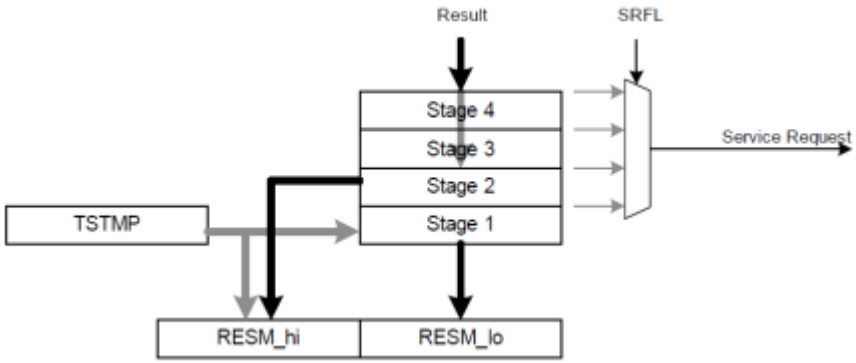
AURIX™ - TC3xx
EDSADC - Result Handling with new 4-stage FIFO feature (1)

› Result FIFO structure



› Result register read modes

Read Mode[1]	RESMx[31:16] (high)	RESMx[15:0] (low)	Notes
Single-word read mode (SSSS'RRRR)	Extended sign value	Next result value (from FIFO stage 1)	DRM = 00_B Supports 16-bit read access
Double-word read mode (NNNN'RRRR)	Subsequent res. value (from FIFO stage 2)	Next result value (from FIFO stage 1)	DRM = 10_B (NNNN = subsequ. value) Low bus load due to 32-bit read access[2]
Timestamp mode (RRRR'TTTT)	Previous result value	Timestamp from last trigger event	TSM = 1[3] Timestamp and prev. value provided once after the timestamp trigger
Intermediate read mode (TTTT'RRRR)	Timestamp from point of read access	Next result value (from FIFO stage 1)	DRM = 01_B Timestamp comes with each value

1) Selected by bitfields DRM and TSM in register DICFGx (x = 0-13).
2) In double-word read mode, a service request is only generated when the result double buffer holds 2 values.
3) The other modes assume TSM = 0.

- The FIFO based result handling offers different options ("read mode") to transfer the values of the result register to the system
- The objective of the different read modes is to optimize the memory size and the peripheral bus load
  - The Timestamp mode is introduced to offer a 16-bit based memory structure in case of an angle based timestamp trigger
  - In Timestamp mode the FIFO is transparent while the gate signal is inactive which means the results values are forwarded directly to stage 2 of the FIFO
  - When the timestamp trigger is executed (gate opens) a timestamp ("TSTMP") is generated and it will be inserted to stage 1 of the FIFO
  - Subsequent result values are then piled into the FIFO
- The service request is generated when a certain number of values is stored into the FIFO
  - The related FIFO fill level can be selected using SFRL bit-field

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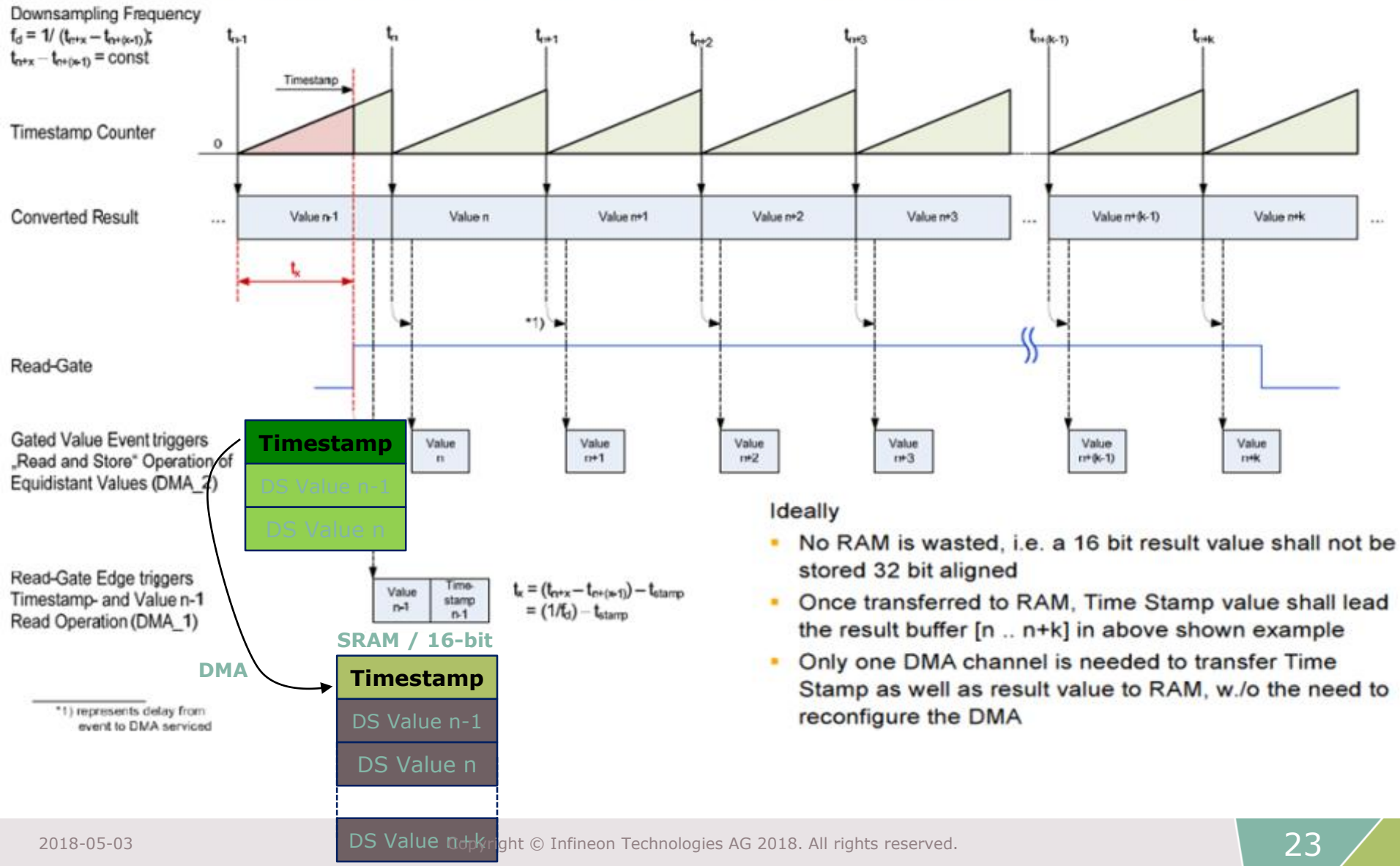
AURIX™ - TC3xx - EDSADC

Result Handling with new 4-stage FIFO feature (2)

Example: Actual Result's Age Relative To Opening Of The Gate



Ideally

- No RAM is wasted, i.e. a 16 bit result value shall not be stored 32 bit aligned
- Once transferred to RAM, Time Stamp value shall lead the result buffer [n .. n+k] in above shown example
- Only one DMA channel is needed to transfer Time Stamp as well as result value to RAM, w./o the need to reconfigure the DMA

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AURIX™ - TC3xx
EDSADC - use case

```
App_EdsadcBasic g_EdsadcBasic; /**< \brief Demo information */
void EdsadcBasicDemo_init(void)
{
   /* create module config */
   IfxEdsadc_Edsadc_Config       edsadcConfig;
   IfxEdsadc_Edsadc_initModuleConfig(&edsadcConfig, &MODULE_EDSADC);
   edsadcConfig.modulatorClockMode = IfxEdsadc_ModulatorClockGeneration_unsyncMode;
   /* initialize module */
   IfxEdsadc_Edsadc             edsadc;
   IfxEdsadc_Edsadc_initModule(&edsadc, &edsadcConfig);
   /* create channel config */
   IfxEdsadc_Edsadc_ChannelConfig edsadcChannelConfig;
   IfxEdsadc_Edsadc_initChannelConfig(&edsadcChannelConfig, &edsadc);
   /* modify default configuration */
   edsadcChannelConfig.modulator.positiveInput      = IfxEdsadc_InputConfig_inputPin;
   edsadcChannelConfig.modulator.negativeInput      = IfxEdsadc_InputConfig_inputPin;
   edsadcChannelConfig.modulator.inputGain          = IfxEdsadc_InputGain_factor1;
   edsadcChannelConfig.modulator.inputPin           = IfxEdsadc_InputPin_a;
   edsadcChannelConfig.modulator.modulatorClockFreq = 40.0e6;
   edsadcChannelConfig.combFilter.decimationFactor  = 32;
   edsadcChannelConfig.combFilter.startValue        = 32;
   edsadcChannelConfig.firFilter.fir0Enabled        = TRUE;
   edsadcChannelConfig.firFilter.fir1Enabled        = TRUE;
   edsadcChannelConfig.firFilter.offsetCompensation = IfxEdsadc_OffsetCompensationFilter_disabled;
   edsadcChannelConfig.firFilter.fir1DecimateRate   = TRUE;
   edsadcChannelConfig.firFilter.prefilterEnabled   = TRUE;
   /* initialize channels */
   for (chn = 0; chn < 1; ++chn){
      if (edsadcChannelAvailable[chn]){
         edsadcChannelConfig.channelId = (IfxEdsadc_ChannelId)chn;
         IfxEdsadc_Edsadc_initChannel(&g_EdsadcBasic.edsadcChannel[chn], &edsadcChannelConfig);
      }
   }

   /* start conversions */
   IfxEdsadc_Edsadc_startScan(&edsadc, 0x3fff, 0);
}
```

EDSADC module initialize

EDSADC channel initialize and add it to queue

EDSADC SW trigger

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