A Variable Switching Frequency Control for ZVS Three-Phase Three-Level T-type Inverter Using Hybrid Discontinuous PWM

Jianliang Chen, *Member, IEEE*, Jie Deng, Lei Ming, *Member, IEEE*, Zhen Xin, *Member, IEEE*, Wei Yin, Peng Wang

***Abstract*- In this paper, a variable switching frequency zero voltage switching (ZVS) control strategy is proposed for three-phase three-level neutral-point-clamped (3L-NPC) T-type inverter. A hybrid discontinuous pulse width modulation (DPWM) method is adopted. Full-range ZVS can be achieved at any load or modulation index without any additional sensors, auxiliary circuits, or current zero-crossing detection (ZCD) circuits. Meanwhile, neutral-point voltage self-balancing can be achieved naturally. The boundary switching frequency can be easily calculated in a digital controller based on inductor current ripple prediction instead of ZCD. The switching loss can be significantly reduced even operating at hundreds of kHz using silicon carbide MOSFETs. Owing to the high switching frequency and extremely low inductance, the power density and the dynamic response can also be improved. The size and the cost of the 3L-NPC inverter are greatly reduced. A 6 kW experimental prototype interfacing an 800 V dc with three-phase 380 V ac is developed to verify the proposed method.**

***Index Terms*- discontinuous pulse width modulation (DPWM), three-level neutral-point-clamped (3L-NPC) T-type inverter, variable switching frequency control, zero voltage switching (ZVS).**

I. Introduction

Three-level neutral-point-clamped (3L-NPC) inverters are extensively used in medium to high-voltage power conversion applications such as motor drives, energy storage systems, photovoltaic (PV) inverters, and wind turbine systems [1]-[3]. The switching frequency is generally restricted to less than 20 kHz to reduce the switching losses of IGBTs, leading to bulky size, large filter parameters, high cost, and slow dynamic response.

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Silicon carbide (SiC) MOSFETs have shown much better figure-of merit than Si counterparts, including higher switching speed and lower switching loss [4]. However, the switching frequency of commercial products using SiC devices is generally around 50 kHz because the switching loss is still a challenge in high-frequency hard switching converters. It can be concluded from the double pulse test that the turn-on loss of the SiC MOSFET is much higher than the turn-off loss [5]. Therefore, the zero voltage switching (ZVS) technique can be used to significantly improve the switching frequency, efficiency, as well as power density. Thus, the high-speed switching characteristics of SiC MOSFETs can be fully utilized.

In the past few years, there have been many studies on soft-switching techniques applied to three-level NPC converters. For the three-level T-type inverter, to achieve ZVS for the four switches in a phase-leg, as shown in Fig. 1, current must flow out of the middle point of the phase-leg before the switch Q_{3x} or Q_{4x} (x= *a, b, c*) is turned on and flow into the middle point before the switch Q_{1x} or Q_{2x} is turned on. In order to achieve this, most ZVS techniques need auxiliary circuits to inject an additional current into the middle point, so the direction of the total current can be changed. According to the positions of the auxiliary circuits, they can be classified into resonant dc-link (RDCL) inverters [5][6] and auxiliary resonant commutated pole (ARCP) inverters [7][8]. They can achieve a wide range of soft switching of main switches as well as auxiliary switches. However, the additional resonant cell may complicate the control strategy and introduce extra size, cost, and power loss.

To eliminate the auxiliary circuits, an intuitive way is to increase the inductor current ripple so that the current can change its direction in a switching cycle. This idea has been implemented in bidirectional buck-boost converter [9][26], totem-pole bridgeless power factor correction (PFC) rectifier [10], and single-phase inverter [11], [12]. To minimize the unnecessary current ripple and circulation loss, the switching frequency is taken as another control degree of freedom. The current zero-crossing detection (ZCD) circuit is usually used to determine the switching instant leading to a variable switching frequency. It can also distribute the conducted EMI spectrum and effectively reduce the EMI filter size [13].

For the three-phase inverter, it is difficult to achieve ZVS for all the switches because the three-phase currents are tightly coupled. The summation of the three-phase currents is always zero. Moreover, the switching state of any phase-leg affects the current ripple of every inductor. Due to these coupling factors,

it is very complicated to control the inductor current ripple in three phases simultaneously. To overcome this issue, two-level three-phase four-wire inverter topology is used by connecting the middle point of the ac filter capacitors and the dc-bus. Then, the inverter-side inductor current can be controlled independently similar to three single-phase half-bridge inverters [14][15]. However, the frequency variation range is so wide that the highest frequency should be limited causing increased conduction loss at around zero-crossing of grid current [15]. Similar methods are also applied to 3L-NPC T-type inverter using three independent triangular current mode (TCM) control [16]-[18]. The applicability is still limited owing to the wide switching frequency variation. In [19], three conduction modes named TCM, discontinuous conduction mode (DCM), and clamp-mode are combined to reduce the switching frequency variation range, but zero current switching (ZCS) instead of ZVS is achieved in DCM. In addition, high frequency current sensors such as shunt plus isolated op-amp, current transformer, or Rogowski coil are needed for the ZCD circuits in each phase, causing additional loss, size, or cost. Different from the ZCD, the variable switching frequency can also be calculated analytically using inductor current ripple prediction. It is an implementation-friendly method that has been proposed to achieve ZVS for two-level three-phase inverters [20][27] and two parallel interleaved three-phase inverters [21]. However, the suitability of three-level inverter has not been studied.

In this paper, a full ZVS range three-phase 3L-NPC T-type inverter without any auxiliary circuits or additional sensors is proposed. A hybrid DPWM method is adopted to decouple the three-phase inductor currents. The switching frequency can be simply calculated based on the measured voltage and current, and the frequency variation range is narrow. ZVS can be achieved for all the switches so that the switching loss is dramatically decreased. Owing to the high switching frequency and extremely low inductance, the power density, the system cost, and the dynamic response can all be optimized. This paper is organized as follows. The proposed modulation method, ZVS condition, and the variable switching frequency control are explained in Section II. The neutral-point voltage self-balancing mechanism is explained in Section III. The design considerations are analyzed in Section IV. The simulation and experimental verification are presented in Section V. Finally, Section VI concludes this article.

II. Space Vector Modulation and Variable Switching Frequency Control

The 3L-NPC T-type inverter with an *LCL* filter configuration is shown in Fig. 1. L is the inverter-side inductor. C is the filter capacitor and L_g is the grid side inductor. The inductor currents on the inverter side and the grid side are i_x (x= *a, b, c*) and i_{gx} respectively. V_{dc} is the dc voltage, and v_x are the three-phase voltage. i_f is the current ripple of the filter capacitor. I_{NP} is the neutral-point current. Q_{1x}-Q_{4x} are the four switches of each phase. The gate signals of Q_{1x} and Q_{3x} (or Q_{2x} and Q_{4x}) are complementary.

The inverter-side inductor currents i_x should be specifically designed to achieve ZVS. Note that i_x is affected by the switching states of all three phase-legs. In addition, the summation of the three-phase current i_x must be zero at any time instant. Due to these two constraints, a possible solution is to keep the switching state of one phase-leg constant during a certain time period and realize ZVS for the other two phase-legs. Therefore, an appropriate modulation method is necessary.

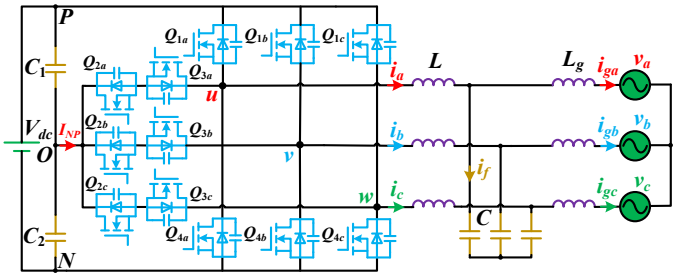
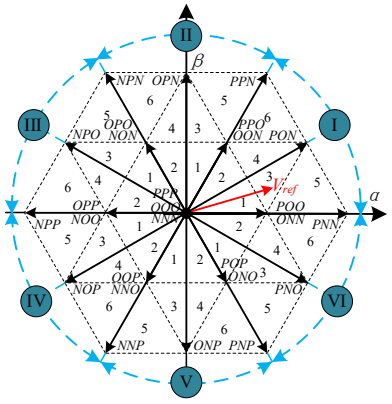


Fig. 1. Three-level neutral-point-clamped T-type inverters with *LCL* filter.

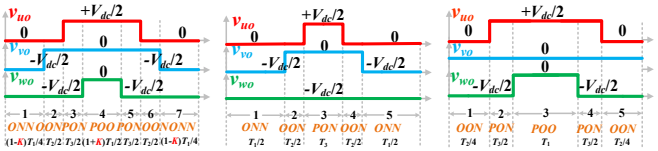
A. Analysis of Space Vector-based DPWM

For three-phase T-type inverters, the seven-segment SVPWM is widely used because of its symmetry and low harmonics. However, all the switches are kept switching, making it hard for the ZVS realization of all the switches. For the five-segment space vector modulation, at any time instant, only two phase-legs are switching at high frequency, while the other phase-leg is not switching, and is clamped to the positive, neutral-point, or negative dc-bus (namely, clamping to *P*-state, *O*-state, and *N*-state). Therefore, the five-segment space vector modulation is used in this paper because the three-phase currents are decoupled.

Fig. 2 (a) shows the widely used sectors and subsectors in a space vector plane. V_{ref} is the synthesis reference vector. The switching pattern of the SVPWM in a switching cycle is shown in Fig. 2 (b), where T_1, T_2, and T_3 are the time duration of three vectors in a switching cycle. Factor K ($-1 \le K \le 1$) is defined as the proportional allocation factor of the small vectors. For the symmetrical seven-segment SVPWM, K is set as 0. When K is -1, only negative small vectors are used. This modulation is called DPWMMIN. When K is 1, only positive small vectors are used. This modulation is called DPWMMAX. The switching patterns of DPWMMIN and DPWMMAX are shown in Fig. 2 (c) and (d), and their modulation waves are shown in Fig. 13. If factor K has a different value in different sections, various space vector-based discontinuous PWM can be obtained [22] [23].



(a) Space vector plane

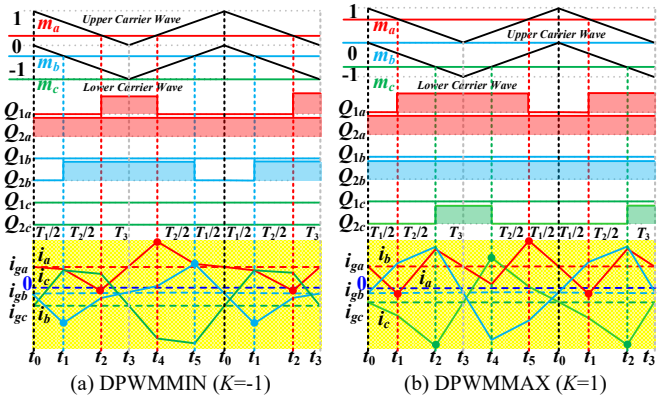


(b) SVPWM (c) DPWMMIN (K=-1) (d) DPWMMAX (K=1).

Fig. 2. Space vector plane and switching patterns of three types of space-vector modulations.

B. Inductor Current Ripple and ZVS Analysis

Taking subsector 3 of sector I as an example, the gate signals and the inductor currents i_x using DPWMMIN and DPWMMAX are shown in Fig. 3 (a) and (b), respectively. The carrier waves are two triangle waves from -1 to 0 and 0 to 1. m_x are the three-phase modulation waves. Q_{1x} (Q_{3x}) is on (off) when the corresponding modulation wave m_x is greater than the upper carrier wave. Q_{2x} (Q_{4x}) is on (off) when m_x is greater than the lower carrier wave. The inductor currents are shown at the bottom. The three straight dashed lines represent the grid-side current i_{gx}. As shown in Fig. 3 (a), the modulation wave m_a is greater than m_b, so the five-segment vector sequence is *ONN* ($T_1/2$), *OON* ($T_2/2$), *PON* (T_3), *OON* ($T_2/2$), and *ONN* ($T_1/2$). Since the modulation wave m_c is fixed at -1, phase *c* is clamped to *N*-state, and the switching state is fixed. Thus, ZVS is only needed to be achieved for the switches in phases *a* and *b*.



(a) DPWMMIN (K=-1) (b) DPWMMAX (K=1)

Fig. 3. Gate signals and inductor currents in subsector 3 of sector I.

Three assumptions for the following analysis are given here. *a*) The grid voltages v_x is constant in a switching cycle. *b*) The current ripple of i_{gx} and the line frequency reactive current generated by the filter capacitors are neglected. The average inductor current of i_x in a switching cycle is equal to the instantaneous grid current i_{gx}. *c*) The neutral-point voltage of the dc-bus is treated as constant.

In Fig. 3 (a), only two switches of phase *a* and two switches of phase *b* are switching, so ZVS is only needed to be achieved for Q_{1a} (Q_{3a}), and Q_{2b} (Q_{4b}).

Owing to the symmetry of the carrier wave, the relationships between i_x and i_{gx} are written as

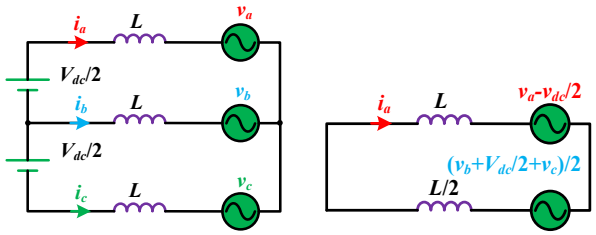
$$\begin{cases} i_x(t_0) = i_{gx}, i_x(t_0 - \Delta t) + i_x(t_0 + \Delta t) = 2i_{gx} \\ i_x(t_3) = i_{gx}, i_x(t_3 - \Delta t) + i_x(t_3 + \Delta t) = 2i_{gx} \end{cases} \quad (1)$$

To achieve ZVS, the minimum reverse current to charge/discharge the output capacitors C_{oss} of the switching devices is denoted as I_{bias}. The specific design consideration is discussed in Section IV. Since the average current i_{ga} is greater than zero in subsector 3 of sector I, $i_a(t_4)$ must be greater than i_{ga}. Thus, the inductor current flows out of the neutral-point of phase *a* before Q_{3a} is turned on, leading to a natural ZVS for Q_{3a}. In order to achieve ZVS for Q_{1a}, $i_a(t_2)$ should be lower than $-I_{bias}$ to fully discharge the output capacitors of Q_{1a}. The analysis is the same for phase *b*. Therefore, the requirements to achieve ZVS for phases *a* and *b* are

$$\begin{cases} i_a(t_2) < -I_{bias} \\ i_a(t_4) > I_{bias} \end{cases} \quad \begin{cases} i_b(t_1) < -I_{bias} \\ i_b(t_5) > I_{bias} \end{cases} \quad (2)$$

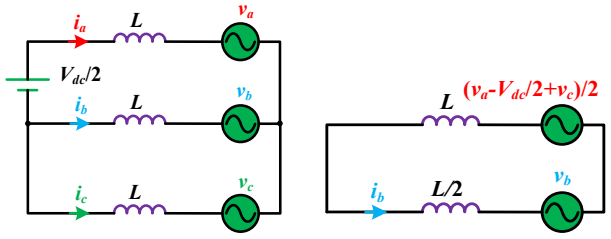
Based on (1), (2) can be rewritten as

$$\begin{cases} i_a(t_4) - i_a(t_2) > 2(|i_{ga}| + I_{bias}) \\ i_b(t_5) - i_b(t_1) > 2(|i_{gb}| + I_{bias}) \end{cases} \quad (3)$$



(a) (b)

Fig. 4. (a) Equivalent circuit for the interval from t_2 to t_4 (*PON* switching state). (b) Thevenin's equivalent circuit.



(a) (b)

Fig. 5. (a) Equivalent circuit for the interval from t_1 to t_5 (*OON* switching state). (b) Thevenin's equivalent circuit.

The switching states of all the switches from t_2 to t_4 are fixed, so the slope of the inductor current i_a is constant. The equivalent circuit is shown in Fig. 4 (a), and the simplified circuit based on Thevenin's theorem is shown in Fig. 4 (b). The inductor current i_a can be calculated as

$$L\frac{\Delta i_a}{\Delta t} = \frac{v_b + v_c + 1.5V_{dc} - 2v_a}{3} = \frac{V_{dc}}{2} - v_a \quad (4)$$

$$i_a(t_4) - i_a(t_2) = (t_4 - t_2)(0.5V_{dc} - v_a)/L \quad (5)$$

Similarly, for phase b, the time interval between t_5 and t_1 is studied. The equivalent circuit is shown in Fig. 5, and the inductor current i_b can be expressed as

$$L\frac{\Delta i_b}{\Delta t}=\frac{v_a+v_c-V_{dc}/2-2v_b}{3}=-\frac{V_{dc}}{6}-v_b \tag{6}$$

$$i_b(t_5)-i_b(t_1)=(t_1-t_5)(-V_{dc}/6-v_b)/L \tag{7}$$

In Fig. 3 (b), the analysis is similar. Still in subsector 3 of sector I, phase b is clamped to O-state, so ZVS is only needed to be achieved for two switches of phase a (Q_{1a}, Q_{3a}) and two switches of phase c (Q_{2c}, Q_{4c}).

Natural ZVS can be realized for Q_{3a} and Q_{2c}. To achieve ZVS for Q_{1a} and Q_{4c}, the current ripple for phases a and c must be large enough. The requirements are given as

$$\begin{cases} i_a(t_5)-i_a(t_1)>2(|i_{ga}|+I_{bias}) \\ i_c(t_4)-i_c(t_2)>2(|i_{gc}|+I_{bias}) \end{cases} \tag{8}$$

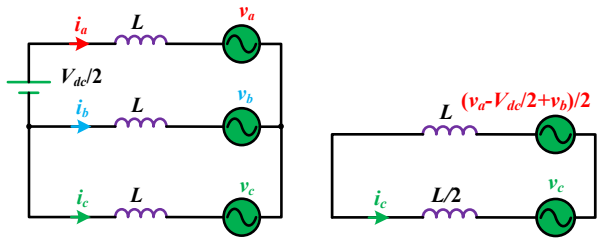


Fig. 6. (a) Equivalent circuit for the interval from t_2 to t_4 (*POO* switching state). (b) Thevenin's equivalent circuit.

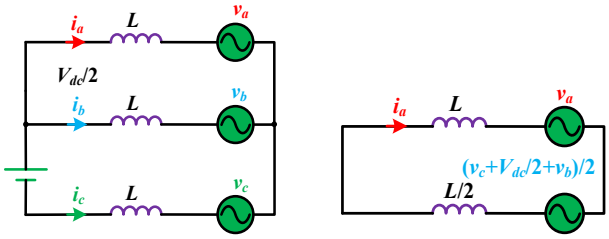


Fig. 7. (a) Equivalent circuit for the interval from t_5 to t_1 (*OON* switching state). (b) Thevenin's equivalent circuit.

The switching states of all the switches from t_2 to t_4 is fixed, so the slope of the inductor current i_c is constant. The equivalent circuit is shown in Fig. 6 (a), and the simplified circuit based on Thevenin's theorem is shown in Fig. 6 (b). The inductor current i_c can be calculated as

$$L\frac{\Delta i_c}{\Delta t}=\frac{v_a+v_b-0.5V_{dc}-2v_c}{3}=-\frac{V_{dc}}{6}-v_c \tag{9}$$

$$i_c(t_4)-i_c(t_2)=(t_4-t_2)(-V_{dc}/6-v_c)/L \tag{10}$$

Similarly, for phase a, the equivalent circuit is shown in Fig. 7, and the inductor current i_a can be expressed as

$$L\frac{\Delta i_a}{\Delta t}=\frac{v_b+v_c+V_{dc}/2-2v_a}{3}=\frac{V_{dc}}{6}-v_a \tag{11}$$

$$i_a(t_5)-i_a(t_1)=(t_1-t_5)(V_{dc}/6-v_a)/L \tag{12}$$

C. Variable Switching Frequency Control

The above-mentioned time intervals in Fig. 3 (a) can be easily expressed by the modulation wave m_x and the switching frequency f_s as

$$\begin{cases} t_1-t_5=-m_b/f_s \\ t_4-t_2=\ \ m_a/f_s \end{cases} \tag{13}$$

Substituting (5), (7), and (13) into (3), the boundary switching frequency f_{sx} to achieve ZVS is given by

$$\begin{cases} f_{sa}<\frac{m_a(0.5V_{dc}-v_a)}{2L(|i_{ga}|+I_{bias})} \\ f_{sb}<\frac{m_b(-V_{dc}-6v_b)}{12L(|i_{gb}|+I_{bias})} \end{cases} \tag{14}$$

Similarly, for DPWMMAX (K=1) in Fig. 3 (b), the time intervals can be expressed as

$$\begin{cases} t_1-t_5=(1-m_a)/f_s \\ t_4-t_2=(1+m_c)/f_s \end{cases} \tag{15}$$

Thus, the corresponding boundary switching frequency f_{sx} to achieve ZVS is given by

$$\begin{cases} f_{sa}<\frac{(m_a-1)(V_{dc}-6v_a)}{12L(|i_{ga}|+I_{bias})} \\ f_{sc}<\frac{(m_c+1)(-V_{dc}-6v_c)}{12L(|i_{gc}|+I_{bias})} \end{cases} \tag{16}$$

TABLE I
CIRCUIT PARAMETERS TO CALCULATE BOUNDARY FREQUENCY

Item	Parameter
Grid line to line voltage v_x	380 V RMS
DC voltage V_{dc}	800 V
Rated Power P_{max}	6 kW
Inductance L	8 μH
Power factor PF	1
Bias current I_{bias}	2 A

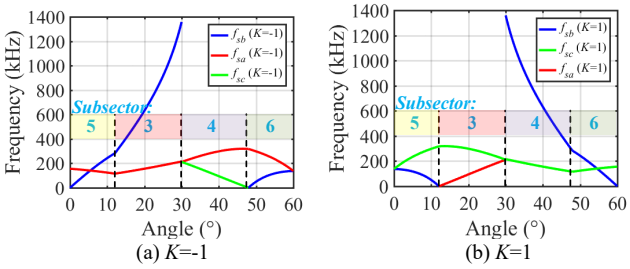


Fig. 8. Boundary frequencies in sector I.

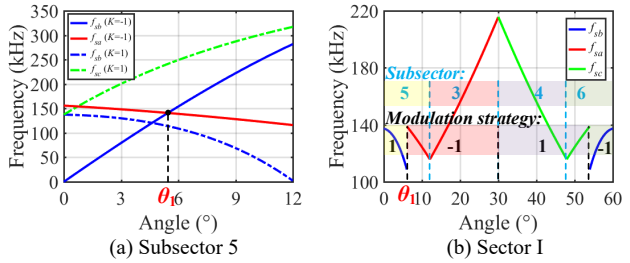


Fig. 9. Unified frequency selection in different sectors.

In other subsectors of sector I, the analysis is the same and is omitted here. Assuming that the circuit parameters are given as listed in Table I, the boundary switching frequencies in sector I can be plotted under K=±1, as shown in Fig. 8. It can be seen that the frequency curves in Fig. 8 (a) and (b) are mirror images to each other. In order to achieve ZVS for all the switches, the lower boundary switching frequency should be chosen as the unified frequency of the inverter. For example, as shown in Fig. 8 (a), in subsector 3, f_{sa} is always lower than f_{sb} under K=-1. Thus, f_{sa} is chosen as the switching frequency in this sector, and the switches of phase b are in over-ZVS mode. In subsector 4, however, the lower frequency f_{sc} approaches zero at the end, which is unfeasible in practice. The reason is that the modulation wave m_c is so close to -1 that the ON-state time duration of the switches in phase c is too short to produce

enough inductor current ripple. Thus, ZVS cannot be fully achieved in subsector 4 under K=-1 whatever the switching frequency is used. Fortunately, the other modulation method (K=1) can take over. As shown in Fig. 8 (b), ZVS can be fully realized in subsector 4 when f_{sc} (K=1) is chosen as the unified switching frequency.

It becomes more complicated in subsectors 5 and 6 because both the zero frequency and the frequency crossing occur. It is difficult to achieve full-range ZVS using either modulation method, so a combination of the two methods (K=±1) should be adopted. Fig. 9 (a) shows the zoomed frequency curves in subsector 5. Fig. 10 and Fig. 11 show the frequency curves under different DC voltages and load applications. The solid and the dashed curves are the boundary frequencies under K=-1 and K=1 respectively. θ_1 is defined as the intersection of the frequency curves f_{sa} (K=-1) and f_{sb} (K=-1). It can be seen that when K=1, f_{sb} is always lower than f_{sc}. However, f_{sb} drops to zero at the end of this subsector. Therefore, f_{sb} can only be chosen in the beginning. When K=-1, there is always an intersection θ_1 between the two frequency curves f_{sa} and f_{sb}. f_{sb} (K=-1) cannot be used because it increases from zero to a high frequency. Thus, it is obvious that f_{sb} (K=1) should be used at the beginning, and f_{sa} (K=-1) should be used at the end of subsector 5. To simplify the frequency selection, there should be only a single change point between K=±1 in this subsector. It may be better to set the change point after θ_1 in some cases, but less computation burden is needed if θ_1 is directly used. Subsector 6 is symmetrical to subsector 5, so the analysis is omitted. The final switching frequency curve in sector I is shown in Fig. 9 (b).

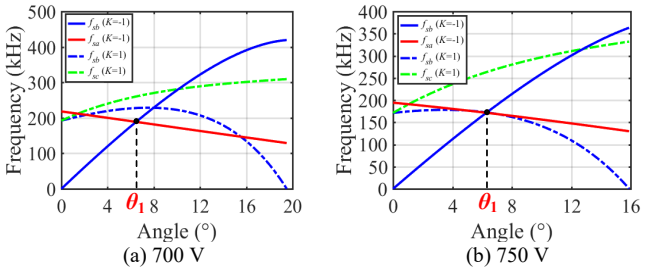


Fig. 10. Frequency curves in subsector 5 at full load.

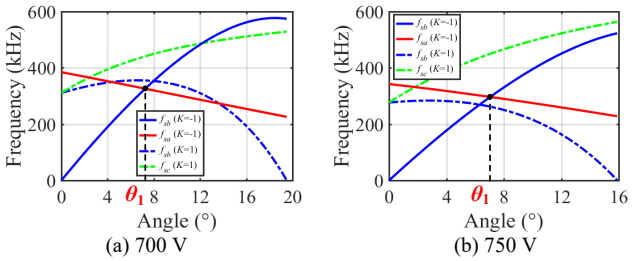


Fig. 11. Frequency curves in subsector 5 at half load.

In other sectors, the phase voltages and currents are simply mirror images or duplications of sector I except for the phase exchange. Thus, it can be proved that the frequency curves in other sectors are also the same, so the variable switching frequency in sector I at different dc-bus voltages is shown in Fig. 12 (a). The frequency curves at different loads can also be plotted, as shown in Fig. 12 (b). The switching frequency calculation equations in different subsectors are given in Table II. The selection of the two modulation methods (K=±1) and the required phase information i_{gx}, v_x, and m_x for the frequency calculation are illustrated in Table III. The proposed hybrid modulation wave in a line cycle is shown in Fig. 13.

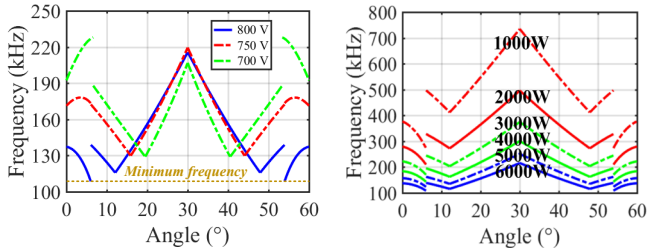


Fig. 12. Variable switching frequency curves in sector I.

TABLE II
SELECTION OF MODULATION METHODS K AND SWITCHING FREQUENCY BASED PHASE IN ALL SECTORS

K (f_s based phase x) (x=a,b,c)		Sector					
		I	II	III	IV	V	VI
Subsector	1	-1 (c)	1 (b)	-1 (a)	1 (c)	-1 (b)	1 (a)
	2	1 (a)	-1 (c)	1 (b)	-1 (a)	1 (c)	-1 (b)
	3	-1 (a)	1 (c)	-1 (b)	1 (a)	-1 (c)	1 (b)
	4	1 (c)	-1 (b)	1 (a)	-1 (c)	1 (b)	-1 (a)
	5 (begin)	1 (b)	-1 (a)	1 (c)	-1 (b)	1 (a)	-1 (c)
	5 (end)	-1 (a)	1 (c)	-1 (b)	1 (a)	-1 (c)	1 (b)
	6 (begin)	1 (c)	-1 (b)	1 (a)	-1 (c)	1 (b)	-1 (a)
	6 (end)	-1 (b)	1 (a)	-1 (c)	1 (b)	-1 (a)	1 (c)

TABLE III
SWITCHING FREQUENCY EQUATIONS IN ALL SECTORS

Subsectors	1	2	3	4
f_s equation	$\frac{(-v_x)(m_x+1)}{2L(I_{bias}+\lvert i_{gx}\rvert)}$	$\frac{(v_x)(1-m_x)}{2L(I_{bias}+\lvert i_{gx}\rvert)}$	$\frac{(\frac{1}{2}V_{dc}-v_x)m_x}{2L(I_{bias}+\lvert i_{gx}\rvert)}$	$\frac{(-\frac{1}{2}V_{dc}-v_x)m_x}{2L(I_{bias}+\lvert i_{gx}\rvert)}$
Subsectors	5 (begin)	5 (end)	6 (begin)	6 (end)
f_s equation	$\frac{(-\frac{1}{3}V_{dc}-v_x)m_x}{2L(I_{bias}+\lvert i_{gx}\rvert)}$	$\frac{(\frac{1}{3}V_{dc}-v_x)(m_x-1)}{2L(I_{bias}+\lvert i_{gx}\rvert)}$	$\frac{(-\frac{1}{3}V_{dc}-v_x)(m_x+1)}{2L(I_{bias}+\lvert i_{gx}\rvert)}$	$\frac{(\frac{1}{3}V_{dc}-v_x)m_x}{2L(I_{bias}+\lvert i_{gx}\rvert)}$

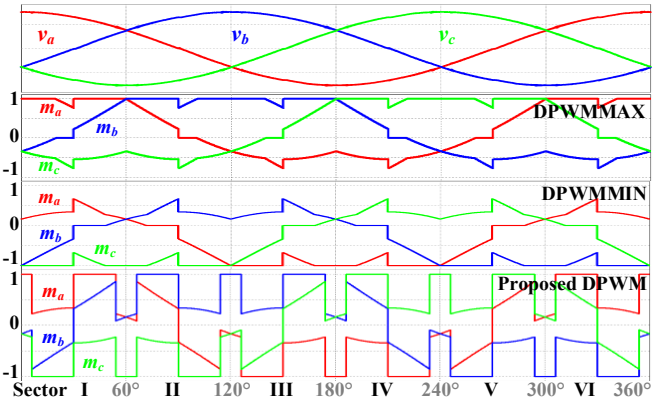


Fig. 13. Different kinds of modulation waves in a line cycle.

III. ANALYSIS OF THE NEUTRAL-POINT CURRENT AND VOLTAGE BALANCING

For the traditional seven-segment SVPWM, K is usually selected as zero so that the small negative vectors (*ONN* in Fig. 2 (b)) have the same time duration as the small positive vectors (*POO* in Fig. 2 (b)) in a switching cycle. Therefore, the influence of the neutral-point voltage caused by the small

vectors can be canceled in each switching cycle. The voltage imbalance is only affected by the medium vectors. However, for the five-segment modulation, only small negative vectors (K=-1) or small positive vectors (K=1) are used in a switching cycle, the canceling effect cannot be realized in each switching cycle. Fortunately, the effect of DPWMMAX and DPWMMIN on the neutral-point voltage is the opposite. Meanwhile, the dwell time of DPWMMAX and DPWMMIN are also the same in each sector, so the neutral-point voltage self-balancing should be achieved naturally. The detailed balancing mechanism of the proposed hybrid DPWM is analyzed as follows.

Taking subsector 3 (K=-1) and subsector 4 (K=1) in sector I as an example, the modulation waves m_x and neutral-point current are illustrated in Fig. 14. When the modulation waves m_x is between the upper and the lower carrier waves (in the shadow area), the corresponding phase-leg is in O-state. d_x is the duty cycle of the O-state, and $I_{NP,K}$ (K=±1) is the average neutral-point current in a switching cycle. [24] [25] Based on the analytical expression of the modulation waves, $I_{NP,-1}$ in subsector 3 can be expressed as

$$\begin{cases} I_{NP,-1} = i_{ga} \cdot d_a + i_{gb} \cdot d_b \\ d_a = 2 - 2 \cdot M \cdot \sin(60^\circ + \theta) \\ d_b = 2 \cdot M \cdot \sin(\theta) \end{cases} \tag{17}$$

where θ is the phase angle, and M is the modulation index. The analysis in subsector 4 is the same. As Fig. 14 (b) shows, $I_{NP,1}$ can be expressed as

$$\begin{cases} I_{NP,1} = i_{gc} \cdot d_c + i_{gb} \cdot d_b \\ d_c = 2 - 2 \cdot M \cdot \sin(60^\circ + \theta) \\ d_b = 2 \cdot M \cdot \sin(60^\circ - \theta) \end{cases} \tag{18}$$

The average neutral-point current waveform can be calculated and shown in Fig. 15 (a). It can be proved that

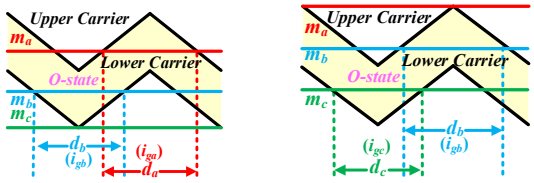
$$I_{NP,-1}(30^\circ - \theta) = -I_{NP,1}(30^\circ + \theta) \tag{19}$$

For example, $I_{NP,-1}$ at 20° is the opposite number of $I_{NP,1}$ at 40°. Thus, the neutral-point voltage self-balancing in a sector can be verified. Meanwhile, the neutral-point voltage fluctuation can be expressed as

$$\Delta V = \Delta t \, I_{NP,K} / C_{dc} \quad (K = \pm 1) \tag{20}$$

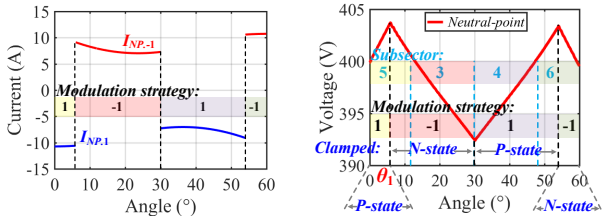
where C_{dc} is the capacitance of dc-bus capacitors. According to the equation from (17) to (20), the maximum magnitude of the dc-bus capacitor voltage ripple can be calculated, as shown in Fig. 15 (b).

The analysis of neutral-point current and voltage in other subsectors are the same. In each sector, the neutral-point current under DPWMMAX and DPWMMIN are canceled mutually. Thus, the neutral-point voltage self-balancing can be achieved naturally with the proposed hybrid DPWM modulation method.



(a) Subsector 3 (K=-1) (b) Subsector 4 (K=1)

Fig. 14. O-state in a switching cycle.



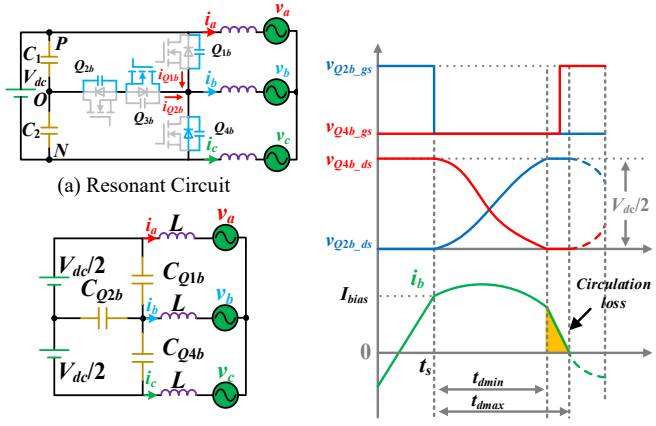
(a) Neutral-point current (b) Neutral-point voltage

Fig. 15. Neutral-point voltage and current with 440 μF dc-bus capacitor in sector I.

IV. Bias Current and Filter Design

In this Section, the design considerations of the filter parameters and the bias current are discussed based on a 6 kW inverter interfacing 800 V dc with three-phase 380 V RMS ac. The minimum switching frequency is set as 100 kHz to fully utilize the fast switching speed of SiC MOSFETs.

The inductance L not only influences the switching frequency but also affects the design of I_{bias} and the dead time t_d. Thus, they should be designed together based on the most difficult situation to achieve ZVS. It can be proved that the worst case occurs at the minimum switching frequency. As shown in Fig. 12, the minimum frequency is located at θ_1 in subsector 5 under 800 V full load condition. At this moment, the ZVS for Q_{4b} is the most difficult to be achieved. Therefore, the resonant process during the dead time before the turn-on of Q_{4b} is analyzed. Fig. 16 (a) shows the equivalent circuit. The switching state changes from PON to PNN, where Q_{1a} and Q_{4c} are turned on. The Thevenin's simplified circuit is shown in Fig. 16 (b). C_{Q1b}, C_{Q2b}, and C_{Q4b} are the output capacitors C_{oss} of Q_{1b}, Q_{2b}, and Q_{4b}.



(a) Resonant Circuit

(b) Equivalent circuit (c) Resonant waveform

Fig. 16. Analysis of the ZVS resonant process of Q_{4b} at θ_1.

According to the equivalent circuit, the resonant process can be expressed as

$$\begin{cases} v_{Q4b\_ds} + v_{Q1b\_ds} = V_{dc}, v_{Q4b\_ds} + v_{Q2b\_ds} = \frac{V_{dc}}{2} \\ v_{Q1b\_ds}(t_s) = \frac{V_{dc}}{2}, v_{Q2b\_ds}(t_s) = 0 \\ v_{Q4b\_ds}(t_s) = \frac{V_{dc}}{2}, i_b(t_s) = I_{bias} \\ C_{Q1b}\frac{dv_{Q1b\_ds}}{dt} + C_{Q2b}\frac{dv_{Q2b\_ds}}{dt} - C_{Q4b}\frac{dv_{Q4b\_ds}}{dt} = i_b \\ \frac{3Ldi_b}{2dt} + \frac{V_{dc}}{4} + \frac{3v_b}{2} - v_{Q4b\_ds} = 0 \end{cases} \quad (21)$$

where t_s is turn-off moment of Q_{2b}, and v_{Q1b_ds}, v_{Q2b_ds}, and v_{Q4b_ds} are the drain-source voltage of Q_{1b}, Q_{2b} and Q_{4b}. The waveform of the ZVS realization is shown in Fig. 16 (c) according to (21). v_{Q1b_gs}, v_{Q2b_gs}, and v_{Q4b_gs} are the gate-source voltage of Q_{1b}, Q_{2b}, and Q_{4b}. It can be seen that the resonant process starts at t_s and ends after a time duration of t_{dmin}. The inductor current i_b decreases linearly after the resonant process and becomes zero at t_{dmax}. The ZVS for Q_{4b} can be achieved if the driving signal is applied between t_{dmin} and t_{dmax}. Otherwise, C_{Q4b} will be recharged as i_b becomes negative.

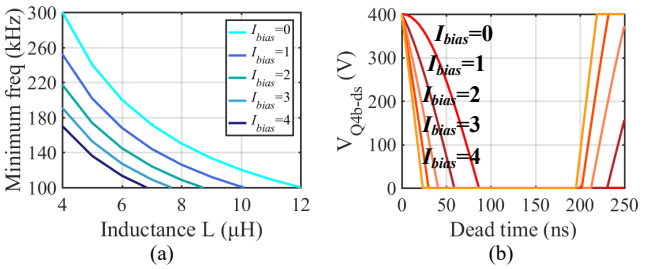


Fig. 17. Selection of inductance, bias current, and dead time. (a) Minimum switching frequency versus different L and I_{bias}. (b) Resonant voltage waveform of v_{Q4b_ds} at different I_{bias} using 8 μH L.

TABLE IV
DEAD TIME SELECTION WITH DIFFERENT BIAS CURRENTS

I_{bias} (A)	L (μH)	t_{dmin} (ns)	t_{dmax} (ns)
0	12	116	312
1	10	60	267
2	8.5	45	220
3	7.5	30	192
4	6.8	25	180

The relationship between the minimum frequency and the inductance L under different bias currents is shown in Fig. 17 (a). Two kinds of SiC MOSFETS are used in each phase-leg, whose output capacitors C_{oss} of Q_{1x}, Q_{4x}, and Q_{2x}, Q_{3x} are 75 pF and 126 pF, respectively. By substituting the parameters obtained from Fig. 17 (a) into (21), the dead time range can be calculated and given in Table IV. When L is 8 μH, the resonant voltage waveform of v_{Q4b_ds} at different I_{bias} is illustrated in Fig. 17 (b). It should be noted that extra parasitic capacitances caused by the driving circuit and the PCB may also contribute to the total capacitance. Some margins should be left when selecting I_{bias} and L. Meanwhile, lower bias current is desired to avoid high circulation loss. Considering the switching speed of the SiC devices, the circulation loss, and the tolerance of the propagation delay of the driving circuits, I_{bias} is set as 2 A. L is designed as 8 μH. The dead time is set to 80 ns.

In order to attenuate the high inductor current ripples and reduce the output current THD, an appropriate LCL filter is necessary. Film capacitors with low equivalent series inductance and high current handling capability should be selected. Similar to the conventional design method of the grid side inductance, L_g is designed based on the full load condition to minimize the switching frequency current harmonics. The capacitance C and the grid inductance L_g are designed as 4.7 μF and 40 μH in this example. The LCL resonance issue can be solved similarly to the conventional inverter including passive and active damping methods.

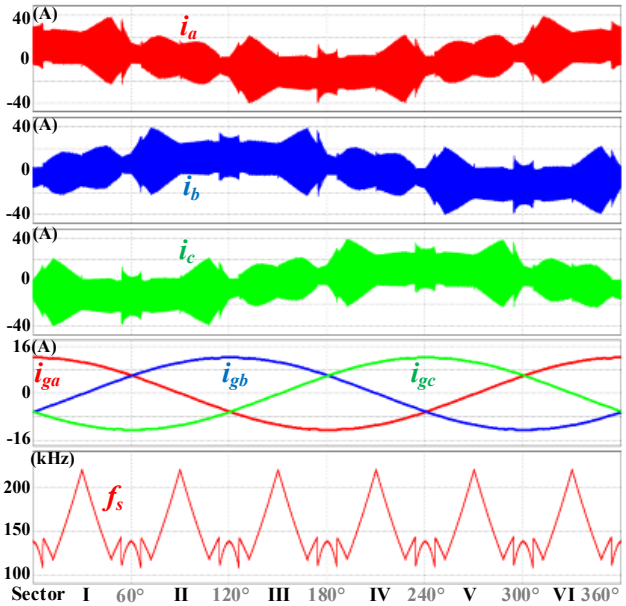
V. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the performance of the proposed method, simulation and experimental results are carried out in this Section. The specification and the parameters are obtained from Section IV and given in Table V.

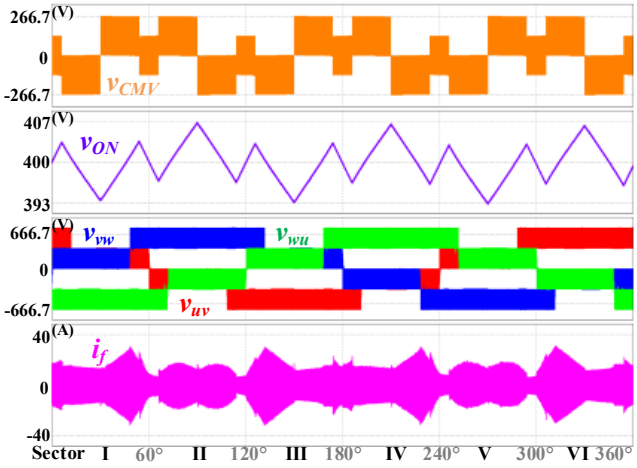
Fig. 18 shows the simulation waveform in a line cycle at full load. i_f is the current ripple of the filter capacitor. The inductor current ripple is consistent with the above discussion, and the bias current is maintained well at 2 A or -2 A in each subsector. Therefore, ZVS can be achieved for all the switches. Although the current ripple at the inverter side is high, the current ripple at the grid side is small. The common mode voltage v_{CMV} has five voltage levels including $\pm V_{dc}/3$, $\pm V_{dc}/6$, and 0. The neutral-point voltage fluctuation v_{ON} in a line cycle agrees well with the analysis in Section III, and the neutral-point voltage self-balancing can be achieved naturally. The minimum switching frequency is 100 kHz, and the maximum frequency is limited to 500 kHz. The current flowing through the filter capacitors i_f is also shown at the bottom. It mainly includes the high current ripple of i_x.

TABLE V
SPECIFICATION AND THE PARAMETERS OF THE INVERTER

Item	Parameter	Item	Parameter
DC voltage V_{dc}	800 V	Grid line voltage v_x	380 V RMS
Rated power P_{max}	6 kW	Power Factor	1
Inductance L	8 μH	Bias current I_{bias}	2 A
Capacitance C	4.7 μF	Dead time t_d	80 ns
DC capacitor C_{dc}	440 μF	Min freq. f_{smin}	100 kHz



(a) Three-phase currents and switching frequency variation



(b) Common mode voltage, neutral-point voltage, DC midpoint voltage fluctuation, and filter capacitor current

Fig. 18. Simulation waveform in a line cycle at 800-V dc full load.

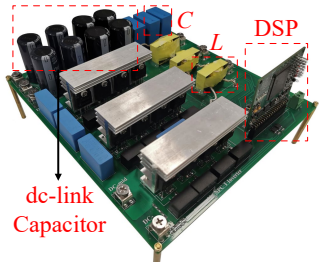
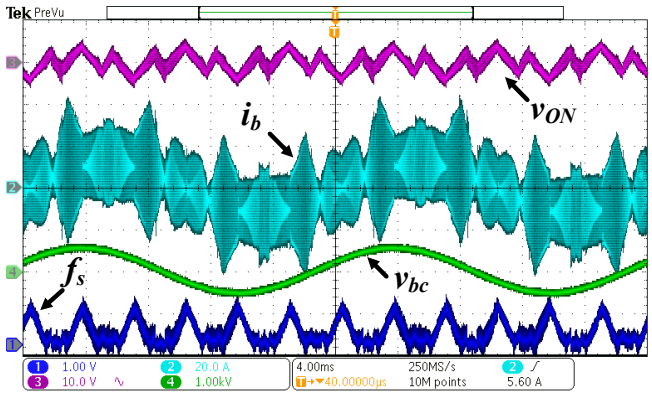


Fig. 19. Photograph of the 6-kW experimental prototype.

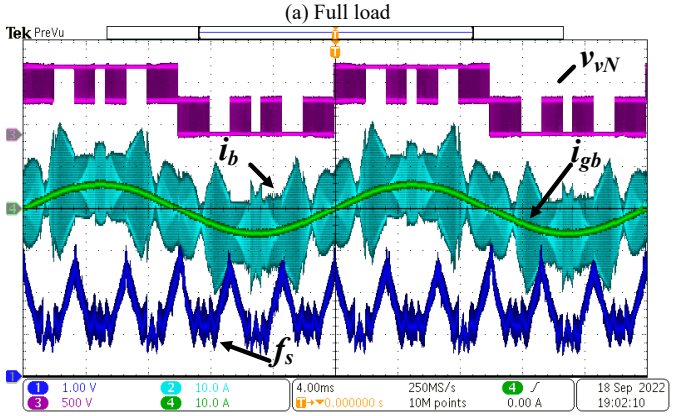
Fig. 19 shows the photograph of the experimental prototype, which is fabricated using 12 SiC MOSFETs including IMZA120R040M1H (1200V, 40mΩ) and C3M0045065K (650V, 45mΩ). Three inverter-side inductors are built with ferrite cores and Litz wire to reduce the high frequency power loss. DSP TMS320F28379S is chosen as the digital controller. The switching frequency is limited from 100 to 500 kHz to reduce the switching loss at light load. The sampling and control frequencies are set as 100 kHz.

Since the three-phase currents have similar waveforms, only one phase is discussed in detail. Fig. 20 shows the steady state waveforms under both full load, half load, and 10% load in a line cycle. The switching frequency curve f_s is generated by the digital to analog converter (DAC) in the DSP. The switching frequency variation range is 105~220 kHz at full load, 180~380 kHz at half load, and constant 500 kHz at 10% load. It can be seen that the experimental results are almost the same as the simulation. The neutral-point voltage fluctuation v_{ON} is shown in Fig. 20 (a). The self-balancing of the voltage is achieved in each sector. Compared to the full load condition, the switching frequency is higher under half load as shown in Fig. 20 (b). The bias current is still tightly controlled. Only a little error is mainly caused by the sampling inaccuracy.

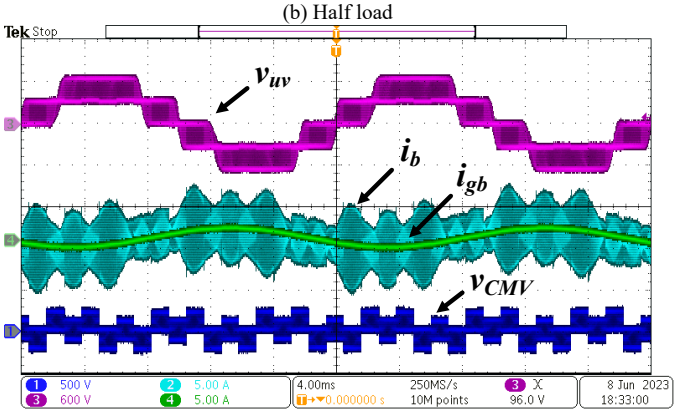
Since Q_{3a} only switches when the average output current of phase a is positive, the current before Q_{3a} is turned on is large enough to fully discharge the output capacitors of Q_{3a}. The analysis of Q_{2a} is the same. Therefore, the switches Q_{2a} and Q_{3a} can achieve ZVS naturally. Only the soft-switching of Q_{1a} and Q_{4a} should be discussed, which can be verified in Fig. 21 and 22. In Fig. 21 (a), the minimum value of i_a is around -2 A, which ensures that the drain-to-source voltage v_{Q1a_ds} decreases to zero before the driving signal v_{Q1a_gs} becomes high. From Fig. 21 (b)-(d), ZVS can all be realized because the minimum values of i_a are all lower than I_{bias}. For the bottom switch Q_{4a}, ZVS can be achieved as long as i_a is greater than 2 A before the switch is turned on. In Fig. 22 (a)-(d), all the peak currents are greater than 2 A. It can be seen that at any position, the drain-to-source voltage v_{Q4a_ds} decreases to zero before the driving signal v_{Q4a_gs} becomes high. Therefore, full-range ZVS can be achieved for all the switches.



(a) Full load

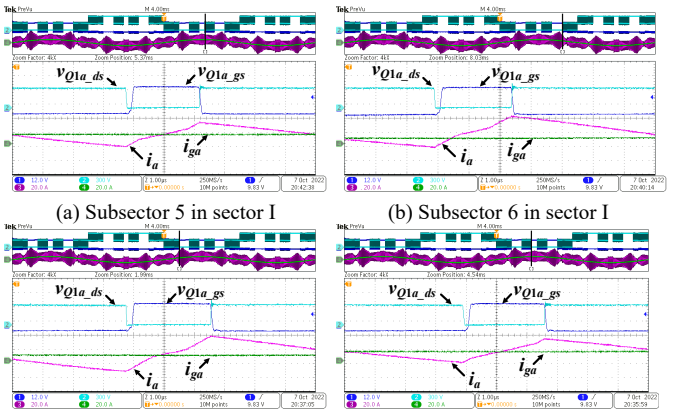


(b) Half load



(c) 10% load

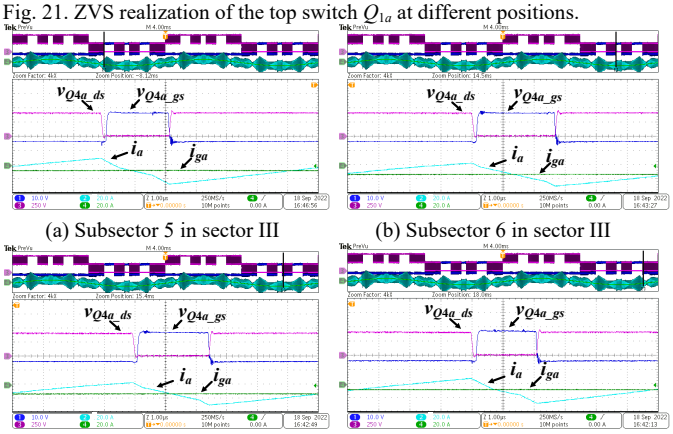
Fig. 20. Steady-state waveforms of phase b in line cycles.



(a) Subsector 5 in sector I (b) Subsector 6 in sector I

(c) Subsector 5 in sector VI (d) Subsector 6 in sector VI

Fig. 21. ZVS realization of the top switch Q_{1a} at different positions.



(a) Subsector 5 in sector III (b) Subsector 6 in sector III

(c) Subsector 5 in sector IV (d) Subsector 6 in sector IV

Fig. 22. ZVS realization of the bottom switch Q_{4a} at different positions.

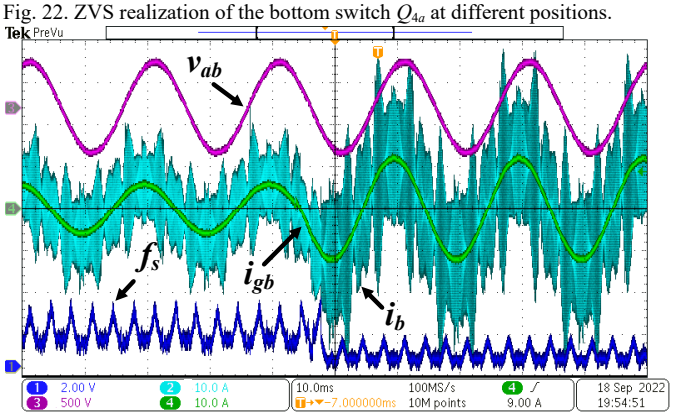


Fig. 23. Dynamic response during load step change from half to full load.

The dynamic response of the inverter is verified and shown in Fig. 23. The load step changes from half to full load. It can be seen that the bias current can always be kept at the designed value both before and after the transient. Therefore, ZVS realization can always be guaranteed. Meanwhile, the inverter closed-loop control is not affected by the proposed variable switching frequency strategy. Fast dynamic response can be achieved not only caused by the high switching frequency, but also the extremely low inductance. The comparison of the load current THD under different DC voltages and loads are shown in Fig. 24.

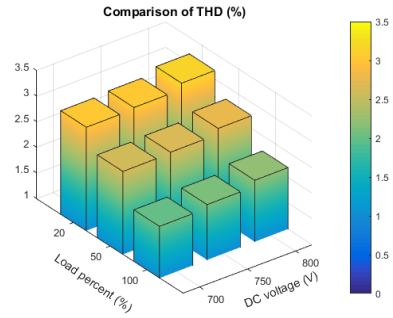
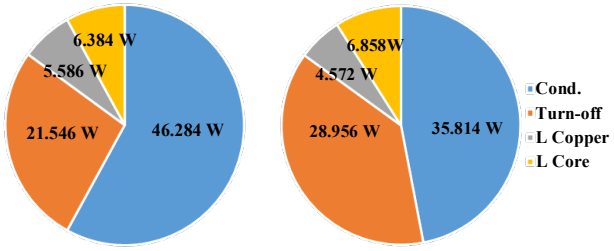


Fig. 24. The comparison of THD under different DC voltages and loads.

The power loss analysis is given as follows. It mainly includes the conduction and the turn-off losses of the switching devices, as well as the core and copper losses of the inductors. The losses from the filter capacitors and the driving circuits are so small that they can be neglected. The calculated loss breakdown at full load is illustrated in Fig. 25. Compared to the conventional hard switching inverter, the conduction loss of the proposed method is increased because of the high current ripple. However, the turn-on loss is totally eliminated, so the efficiency is more advantageous when operating at higher frequency and with lower $R_{ds(on)}$ device (or devices paralleling). The trade-off between low switching loss and large die size when selecting the power device is no longer a concern. Compared to the 800V dc-bus condition, the conduction loss at 700 V is lower because of less utilization of the *O*-state, whose conduction path includes two switches. However, the higher average switching frequency at 700 V causes that the turn-off loss is increased. Since the load current is the same as that at 800 V, the inductor current ripple and the RMS current are almost the same. Fig. 26 shows the measured efficiency at different loads under 700-V and 800-V dc. The peak efficiency is about 98.8% at 800-V dc 70% load.



(a) 800 V (b) 700 V

Fig. 25. Calculated loss breakdown at full load.

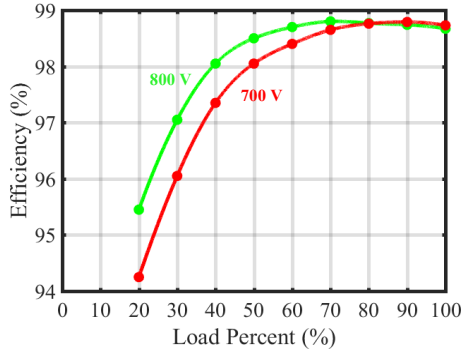


Fig. 26. Measured efficiency at different loads under 700-V and 800-V dc.

VI. Conclusion

This paper proposes a variable switching frequency control method for three-phase 3L-NPC T-type inverter to achieve full-range ZVS for all the switches. A combination of the traditional space vector modulation methods DPWMMAX and DPWMMIN is used to optimize the frequency calculation. The operating principle, the inductor current ripple, and the ZVS realization are analyzed in detail.

Instead of using the ZCD circuit, the variable switching frequency can be easily calculated in a digital controller without any high-frequency sensor or auxiliary circuit. The switching loss can be greatly reduced even operating at hundreds of kHz. The self-balancing of the dc-bus neutral-point voltage can be achieved naturally. Meanwhile, owing to the high switching frequency and low inductance of the filter, the power density and the dynamic response can be significantly increased. With the proposed variable switching frequency control method, the superior characteristics of the wide band-gap power devices can be fully exploited.

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